Optimizing Computing System Performance with a Modern USB-C Power Architecture

Abstract

The rapid adoption of USB Type-C® and USB Power Delivery (USB-PD) 3.1 has transformed power delivery in mobile computing systems. With Extended Power Range (EPR) enabling up to 240W (48V/5A), USB-C is now capable of powering high-performance notebooks and peripherals. This document reviews conventional NVDC buck-boost charger architectures and introduces an updated Renesas solution based on modern devices such as the RAA489800 bidirectional buck-boost controller combined with battery charger ICs (e.g., RAA489110 / RAA489118). These solutions enable Hybrid Power Buck-Boost (HPBB) operation, improving efficiency, flexibility, and system scalability in multi-port USB-C designs.

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Introduction

The USB Type-C® interface, standardized by the USB Implementers Forum[1](USB-IF), is transforming power delivery and connectivity in modern electronic systems—particularly in mobile computing platforms such as notebooks and tablets. Traditional designs relied on dedicated, proprietary DC input ports for external power adapters, where a battery charger IC managed both battery charging and system power regulation.

Recent industry trends have shifted toward consolidating power, data, and video through USB Type-C® ports with USB Power Delivery (USB-PD). Unlike legacy USB interfaces limited to fixed 5V operation, USB-PD enables dynamic, programmable voltage negotiation over a wide range. With USB-PD 3.1, including Extended Power Range (EPR), systems can support voltages from 5V up to 48V and currents up to 5A, delivering a maximum power of 240W. In addition, USB-PD introduces advanced features such as Programmable Power Supply (PPS) for fine-grained voltage control, bidirectional power flow for flexible source/sink roles, and Fast Role Swap (FRS) for seamless power transition. These capabilities enable a single USB-C port to efficiently power high-performance computing devices, external displays, and accessories.

As a result, USB Type-C® is rapidly replacing proprietary charging interfaces, simplifying system design and improving user experience through a unified, standards-based power architecture. This evolution also drives the need for more advanced power management solutions capable of handling higher power levels, wider voltage ranges, and multi-port system requirements.

Conventional NVDC Buck-Boost Charger Topology

This USB-C protocol provides a wider range of variable input voltages (Vin) to a battery charging system, which could be lower or higher than battery pack voltage and system bus voltage. Hence, the buck-boost converter becomes the most favorable option. Figure 1 shows the simplified diagram for a conventional narrow voltage DC (NVDC) four-switch buck-boost charging topology. This NVDC charger is comprised of four switching FETs belonging to the buck-boost converter and one BFET between the battery and system voltage bus, Vsys. The input of the buck-boost converter could be from a proprietary AC/DC wall adapter or from the USB-C port.

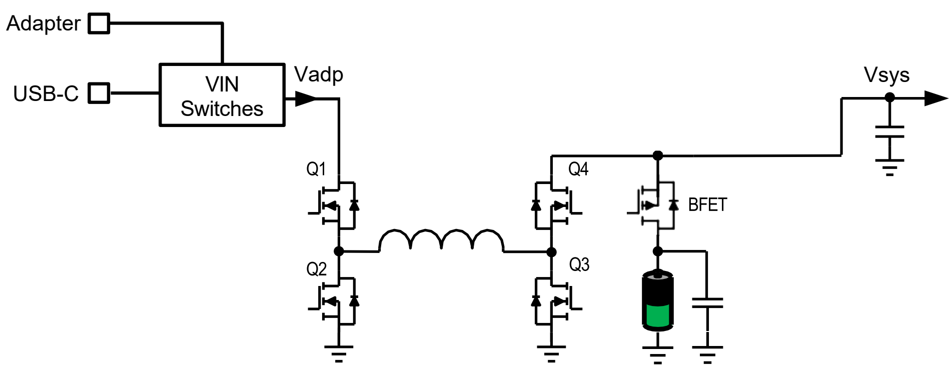

Figure 1. *Conventional NVDC Buck-Boost Charger Topology for USB-C*

Figure 2 shows the power path when input power is present. There are three operation scenarios in this mode.

i. If the battery is fully charged, the buck-boost charger will turn off the BFET. In this case, the buck-boost charger provides the output power to the system with Vsys regulated to the desired voltage.

ii. If the battery is not full and the buck-boost charger is charging the battery, the BFET is turned on. In trickle charge mode, the BFET operates in the saturation region to behave like a linear regulator (LDO), and Vsys is regulated at the target voltage. If the charger is in CC or CV mode with the BFET fully turned on, Vsys is equal to Vbat (assume no voltage drop from the BFET). Input power = system power + battery charge power, with the assumption of input power > system power.

iii. It doesn't matter if the battery is in charge status or not. As soon as the system power > input power, Vsys will show a dip. In general, the body diode in the BFET will conduct if the Vsys< Vbat-Vdrop, where the Vdrop stands for the body diode drop with a typical voltage of 0.7 V. Otherwise, with a more sophisticated control, the BFET could be turned on earlier to 'catch up' and support Vsys. In either case, the battery will be discharged and the battery power merged with the input power to support the system power.

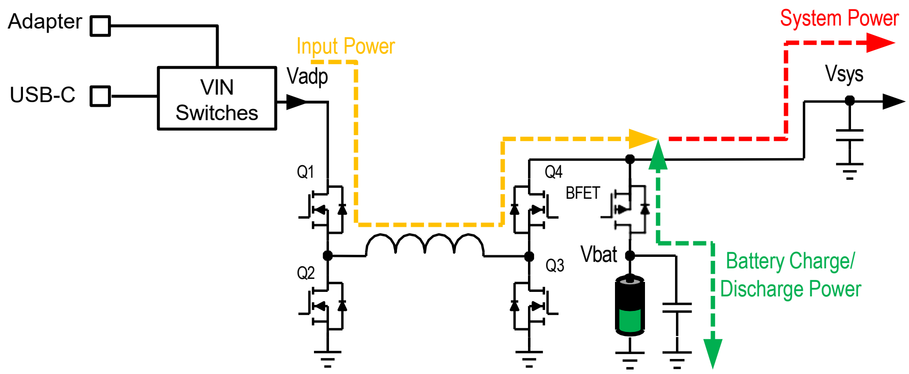

Figure 2. *NVDC Buck-Boost Charger Power Path with Input Power*

Figure 3 shows the power path in battery-only mode. This mode is relatively simpler than the previous one because the battery always provides power to the system with the BFET forced on. Vsys is equal to Vbat in this mode.

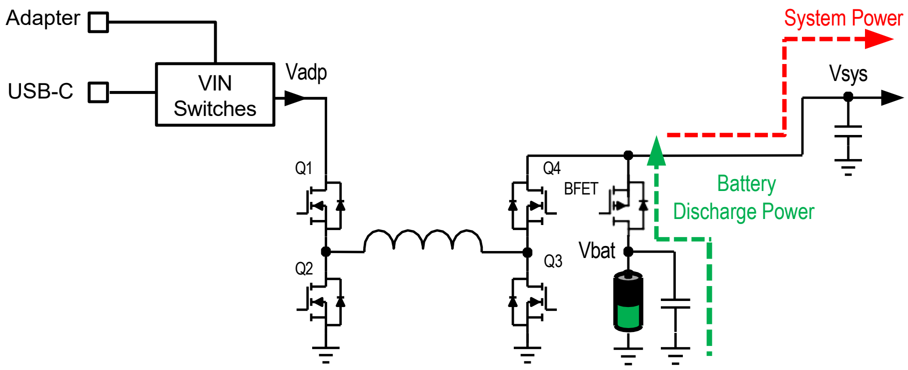

Figure 3. *NVDC Buck-Boost Charger Power Path in Battery Only Mode*

One of the typical features of a NVDC configuration is that all power flows through and is processed by the buck-boost charger, making power loss inevitable due to MOSFET switching and conduction loss, inductor core loss, copper loss, etc. The power inductor needs to be sized correctly to handle the full system's power, plus the charging power, therefore demanding a bigger inductor. Thus, a NVDC configuration is preferred for a lower power level system; e.g., 60 W or lower. One advantage of a NVDC configuration is a simple control scheme. When the system enters turbo mode, where system power is higher than adapter power, it's not necessary that the charger controls anything beyond the adapter current control. The battery naturally discharges the current through the BFET to automatically support the system.

Hybrid Power Buck-Boost (HPBB) Architecture

Figure 4 shows the new HPBB battery charger configuration. In this mode, the input power passes through bypass FETs instead of going through the buck-boost charger. Thus, the power loss is greatly reduced compared with the NVDC mode. The buck-boost charger only processes the battery charge/discharge power, and a larger inductor is not required for this configuration.

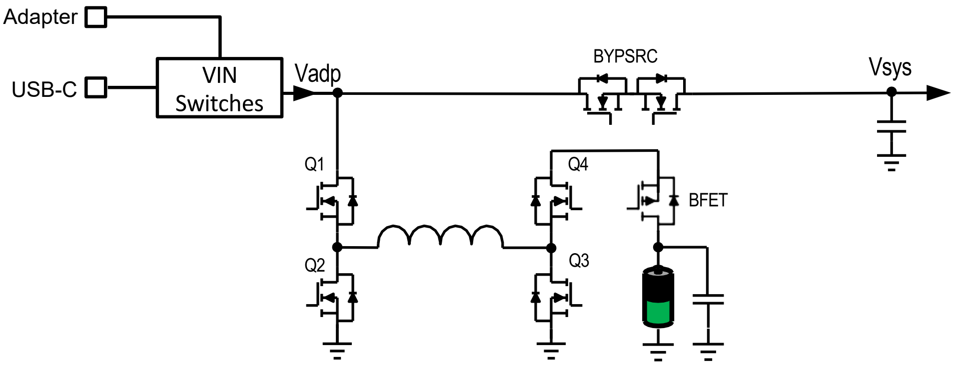

Figure 4. *Renesas HPBB Buck-Boost Charger Configuration*

When input power is present, there are two operation scenarios for this mode:

i. Input power > system power: If this condition is met, the buck-boost battery charger will not provide power to the system. Instead, the buck-boost charger can be in standby mode if the battery pack is fully charged or it is charging the battery pack. Figure 5 shows the power path in HPBB mode for this scenario.

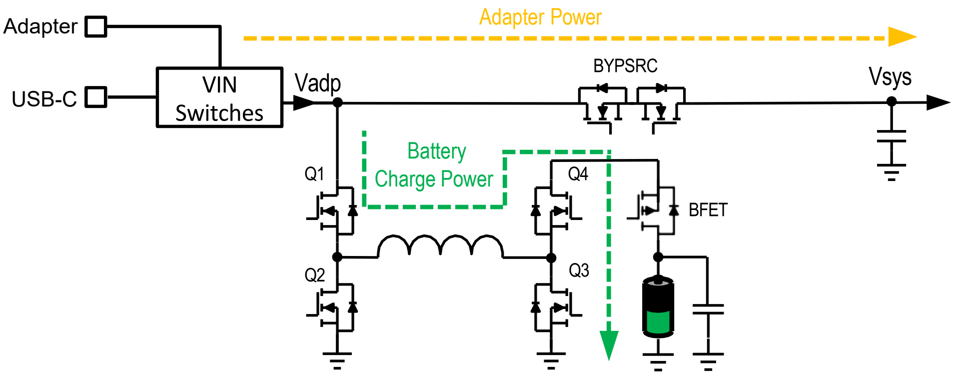

Figure 5. *Renesas HPBB Buck-Boost Charger Configuration*
*(*Input power > system power*)*

ii. Input power < system power: In this case, the battery needs to be discharged, and the buck-boost charge is operating in reverse mode to pump energy from the battery to the Vadp side. The battery power combines with the input power to support the system's power. This mode is also called 'Reverse Turbo-Boost' mode, and Figure 6 shows its power path in HPBB mode.

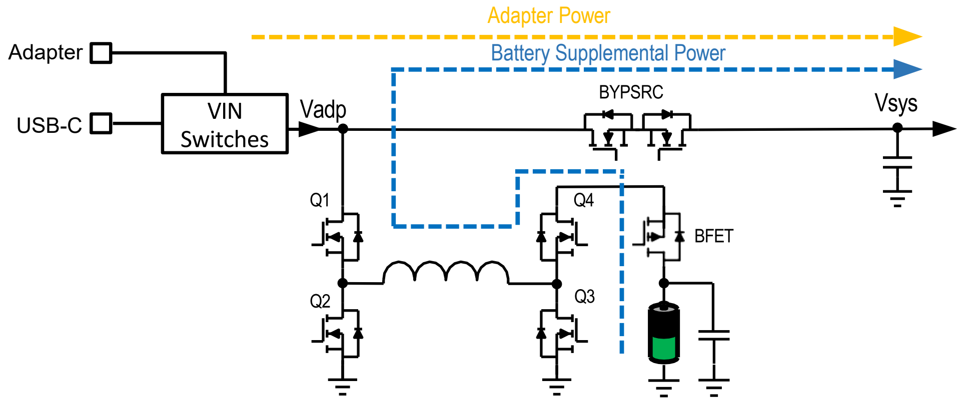

***Figure 6.** Renesas HPBB Buck-Boost Charger in 'Reverse Turbo Boost' Mode*

Introducing the Renesas RAA489110[2] 'Combo' Buck-Boost Battery Charger

The RAA489110 is a next-generation buck-boost charger product from Renesas, derived from the ISL9241 family. It supports both NVDC and HPBB configurations, providing high flexibility and optimized performance for USB Type-C power applications.

In NVDC mode, the RAA489110 automatically selects the adapter and/or the battery as the source for system power. NVDC operation also supports turbo mode by turning on the BGATE FET to regulate the adapter current at the programmed limit, while the battery supplies the remaining power required by the system.

In HPBB mode, the RAA489110 supports various operating conditions such as bypass, bypass with charging, and reverse turbo-boost mode.

By allowing both HPBB and NVDC configurations, the RAA489110 enables enhanced flexibility in system design and improves overall system performance. These two operating modes can be dynamically configured through host firmware in the embedded system controller (EC) via SMBus/I2C, allowing seamless adaptation to different power sources such as an AC/DC adapter or inputs from USB Power Delivery ports, including Extended Power Range (EPR).

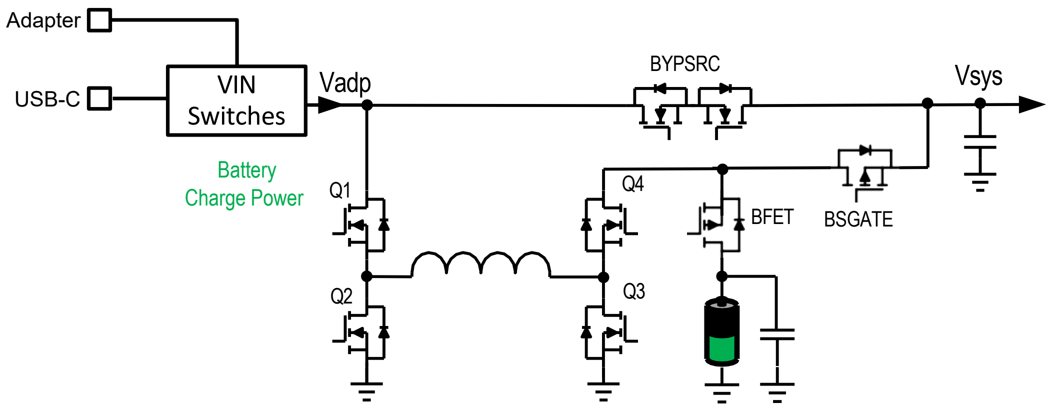

***Figure 7.** RAA489110 Combo Buck-Boost Charger Supporting Both NVDC and HPBB Configuration*

The RAA489110 provides the charging function, system bus regulation, and protection features using only NFETs for efficiency and BOM cost optimization. The advanced Renesas R3™ Technology is used to provide a highly efficient light-load charging mode. In addition, its reconfigurable control and compensation architecture allows the use of a smaller inductor while optimizing efficiency across multiple power levels.

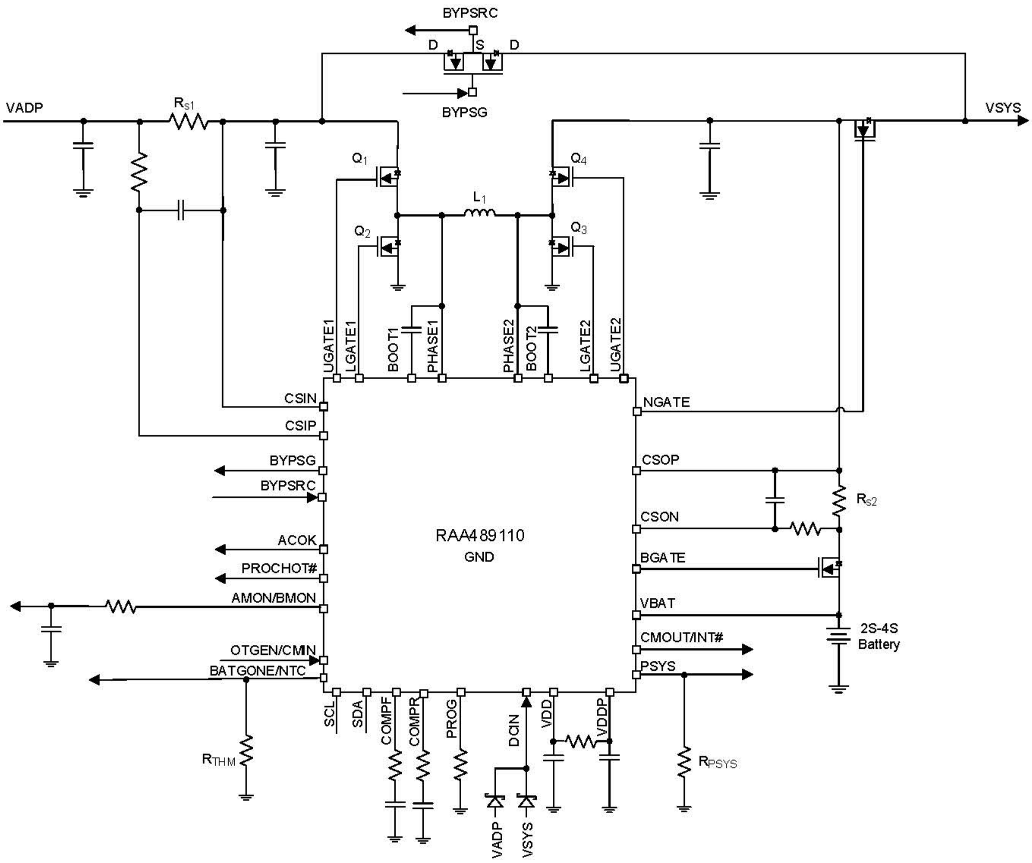

Figure 8. *RAA489110 Combo Buck-Boost Charger Typical Application Diagram*

The RAA489110 takes input power from a wide range of DC power sources (conventional adapters, travel adapters, USB type-C power ports, etc.) and safely charges battery packs with up to four-cell Li-ion series batteries. The RAA489110 also provides autonomous charging with automatic end-of-charge (EOC) termination. In HPBB mode, a firmware-controlled bypass operation allows the adapter to supply power directly to the system.

The RAA489110 supports reverse buck, boost, or buck-boost operation to the adapter port from battery packs with two- to four-cell batteries. This allows configurations to support USB Type-C Power Delivery (USB-PD) output, including Programmable Power Supply (PPS) and Extended Power Range (EPR). The RAA489110 can operate with only a battery, only an adapter, or both connected. The system power can be provided from the adapter, battery, or a combination of both. For Intel IMVP-compliant systems, the RAA489110 includes a System Power (PSYS) monitor that provides an analog signal representing total platform power. The PSYS output interfaces with a wide range of IMVP core regulators to support an IMVP-compliant power domain. The RAA489110 also includes a processor-hot (PROCHOT#) monitor and supports Supplemental Mode, meeting Intel's Vmin Adaptive Protection (VAP) requirements by maintaining the battery voltage above a defined minimum level. The RAA489110 supports SMBus/I²C serial communication, enabling flexible programming of key parameters for a highly customizable solution.

The RAA489110 keeps monitoring its operation and communicates its fault/warning status through interrupt. The integrated 8-bit ADC in the RAA489110 enables key system parameter telemetry, such as temperature (PCB and junction), adapter current/voltage, battery charge/discharge current, and system bus voltage.

The RAA489110's reconfigurable charging architecture provides high flexibility, allowing it to be used in a wide range of system configurations, including designs with multiple USB Type-C ports. While each device is typically used for a single USB-C port, it can be integrated into multi-port USB-C systems with appropriate system-level design. The RAA489110 supports USB Power Delivery (USB-PD), including Programmable Power Supply (PPS) and Extended Power Range (EPR), enabling fully compliant and scalable USB-C power solutions.

The RAA489110 has an input voltage range of 3.9 V to 30 V, with a system/battery output voltage range of 3.9 V to 18.304 V for 2- to 4-cell battery packs. It supports On-The-Go (OTG) operation with output voltages up to 20 V and can be configured for autonomous charging with automatic end-of-charge (EOC) termination without requiring communication from an embedded controller. Automatic detection allows the device to enter trickle charging mode when the battery is depleted. The device also supports a programmable two-level adapter current limit and includes a battery learn mode to calibrate the battery fuel gauge. Programmable features via SMBus or I²C interface provide a high degree of flexibility, enabling optimization for a wide range of system designs.

Design Tools from Renesas

Evaluation Board/User Guide

An evaluation board and detailed user guide for customer testing and evaluation are available for the RAA489110. A photograph of the evaluation board is shown in Figure 9.

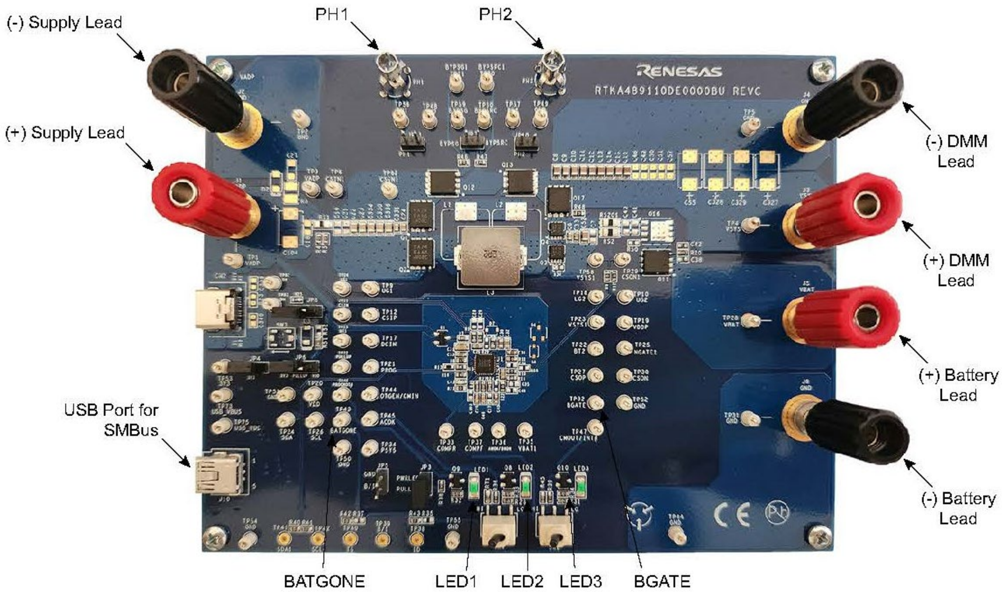

Figure 9. *RAA489110 Evaluation Board*

RAA489110 GUI

The RAA489110 GUI software offered by Renesas will help accelerate the design, testing, finalization, and debugging of your battery charger design. It connects to development boards to set various adjustable system parameters and threshold values. Figure 10 shows an example of RAA489110 GUI software windows.

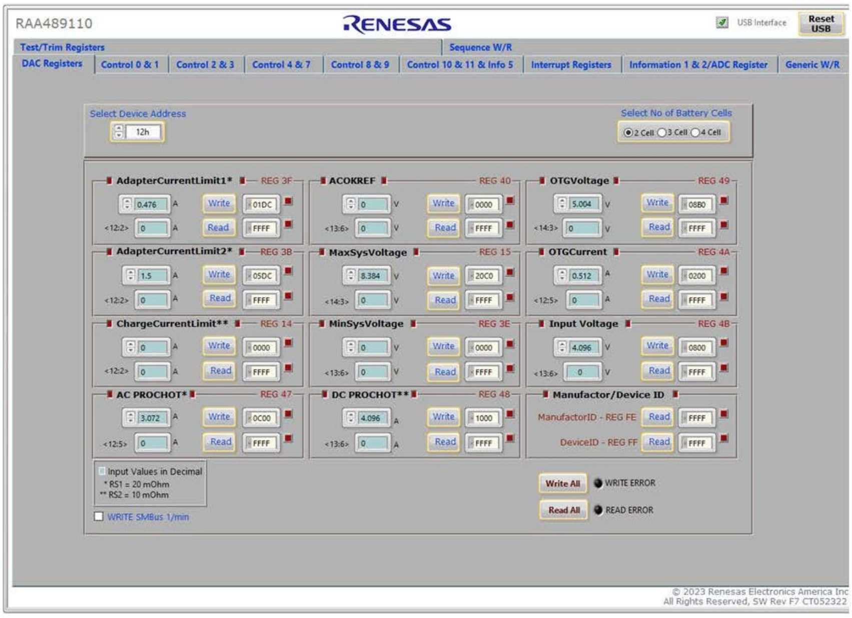

Figure 10. *Screenshot of RAA489110 GUI*

Additional Resources

For other online resources provided by Renesas for battery charger design, go to:

https://www.renesas.com/en/products/power-management/battery-management/battery-charger-ics

Conclusion

This white paper provides an overview of modern battery charging topologies and operating principles for consumer mobile computing devices such as notebooks. The battery charger is a critical component in mobile device power management because it not only charges the battery pack but also manages the overall power flow from the adapter to the computing system. In a computing system, the battery charger must operate seamlessly with system management components, such as the embedded controller (EC), to efficiently meet system power demands. The RAA489110 offers enhanced flexibility by supporting both NVDC and HPBB configurations, allowing designers to dynamically select the optimal operating mode for their application. The RAA489110 maintains a high degree of register compatibility with existing Renesas charger solutions, such as the ISL9241 family, helping to minimize development effort when migrating designs across different Renesas charger platforms. In addition, firmware developed for NVDC-based designs can be easily adapted to enable HPBB operation with minimal changes. This significantly reduces development and validation effort when deploying the RAA489110 across multiple computing platforms.

References

[1] USB Implementers Forum www.usb.org

[2] Renesas RAA489110 https://www.renesas.com/en/products/RAA489110

Revision History

Revision	Date	Description
2.00	Jun 19, 2026	USB spec related information and product information updates
1.00	Oct, 2018	Initial release.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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