Inside HVPAK: A Deep Dive into Architecture and Capabilities

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Abstract

This white paper provides basic guidelines for developers to get familiar with the HVPAK^{TM} family, explaining its high-voltage building blocks, operating principles, configuration options, and typical applications for motor-control and power-switching designs.

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1. Introduction

The HVPAK combines the GreenPAK mixed-signal logic with additional high-voltage H-/Half-bridge functionality. This white paper will focus on the second, HV part. The main HV blocks that distinguish this product line into a separate GreenPAK subfamily will be analyzed. This article will also explain what these blocks are for, how they operate, and what settings they have. It will also show the main applications using these macrocells. This tutorial will allow you to master the basic knowledge of HVPAK necessary to get your motor running.

2. HVPAK Specialized Macrocells Overview

This section will show the specialized macrocells that distinguish the HVPAK from the usual GreenPAK, describe their operating principle, and their main settings.

2.1 HV Outputs Overview

HVPAK ICs integrate N-channel power MOSFETs for High Voltage Outputs (HV OUTs) with 1.5A RMS output current capability over an input voltage range of 3.0V to 13.2V/26.4V. HV OUTs can be configured as 2x Half Bridges or x Full Bridges. See the HV OUTs block diagram in Figure 1.

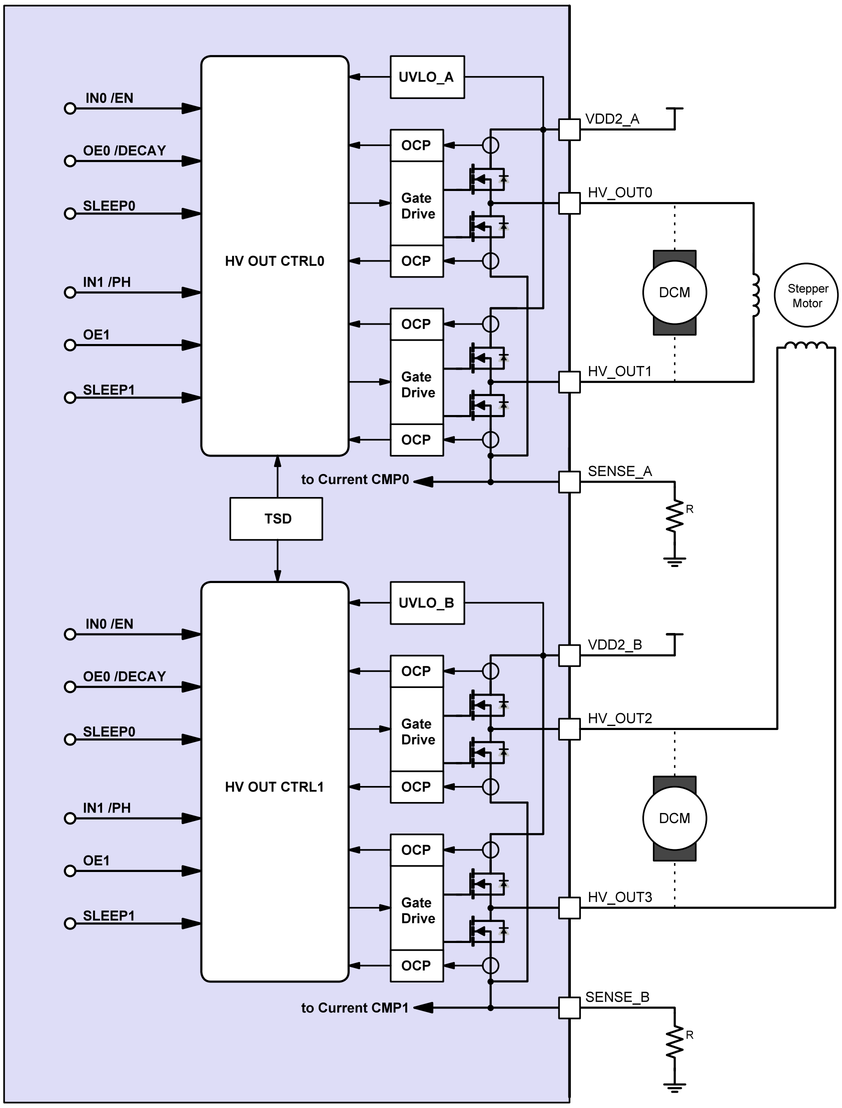


Figure 1. SLG47105 HV Outputs Overview

One Full Bridge can drive one bidirectional DC motor. Two Half Bridges allow driving two unidirectional DC motors. The SLG47105 features two full bridges, allowing the driving of one stepper motor.

HVPAK ICs integrate current sense pins for each HV OUT group. The motor current is sensed by monitoring the voltage across an external sense resistor. If the current limit feature is not needed, the SENSE PIN needs to be directly connected to ground.

HVPAK ICs include the following fault protections: overcurrent protection (OCP), undervoltage lockout (UVLO), and overtemperature protection (OTP). They also provide a low-power sleep mode.

2.1.1 HV OUTs Properties

Each HV OUT is the power output stage with integrated body diodes. The current flow of HV OUTs is under full control of the user by way of the input control logic. The output stage is designed to produce full load control under all system conditions. All protective and control features are integrated into the control and protection blocks. The sensors for current and temperature are integrated directly into the output MOSFET for maximum accuracy and dependability.

Output Mode:

- Hi-Z: High Impedance (Default). It’s the same as “PIN not used”
- LOW Side On: NMOS LOW Side Open-DRAIN
- HIGH Side On: NMOS High Side Open-DRAIN
- LOW and HIGH Side On: Push-Pull

2.1.2 HV OUTs Control

HVPAK ICs contain HV OUT CTRL macrocells to control HV OUTs. Each macrocell can drive either two unidirectional DC motors or one bidirectional DC motor. Two HV OUT CTRL can be used to drive a stepper motor. Each block has several input signals to control the outputs, as well as Fault OUT signals. Also, each block has Slew Rate Mode, HV OUT Mode, OCP, and UVLO settings.

Slew rate:

- Slow for motor driver mode (or another high load)
- Fast for pre-driver mode (to control external transistors or other logic)

In fast slew rate mode, the device can be used as a driver for external transistors, since the rise/fall times of the HV OUTs are much shorter than in regular slow slew rate mode.

HV OUT mode:

- Half Bridge Mode (Default)

This mode is the default mode for HV OUT pins. In this mode, each HV OUT can be controlled separately, and there is a possibility to drive up to four motors spinning in one direction.

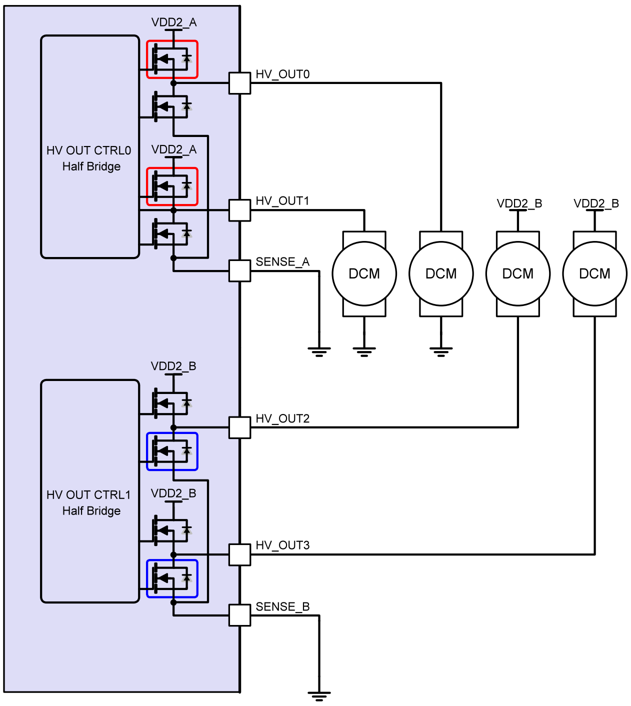


Figure 2. SLG47105 Half Bridge Mode Overview

- Full Bridge Mode

This mode is useful for driving a DC motor with the ability to change the motor rotation direction. PWM voltage regulation is active in this mode. Also, this mode can be used to drive a single Stepper Motor with the SLG47105.

In Full Bridge mode, there are two Mode control options: "IN-IN" and "PH-EN".

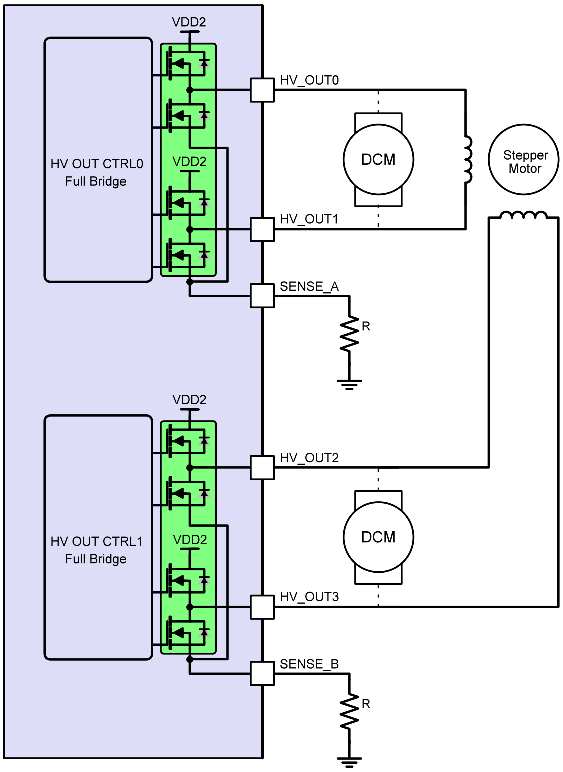


Figure 3. SLG47105 Full Bridge Mode Overview

Besides, there are two modes for current recirculation: Slow Decay and Fast Decay.

- For Slow Decay mode, the current circulates through the two low-side FETs.
- For Fast Decay mode, the current flows through the body diodes of the other diagonal two FETS.

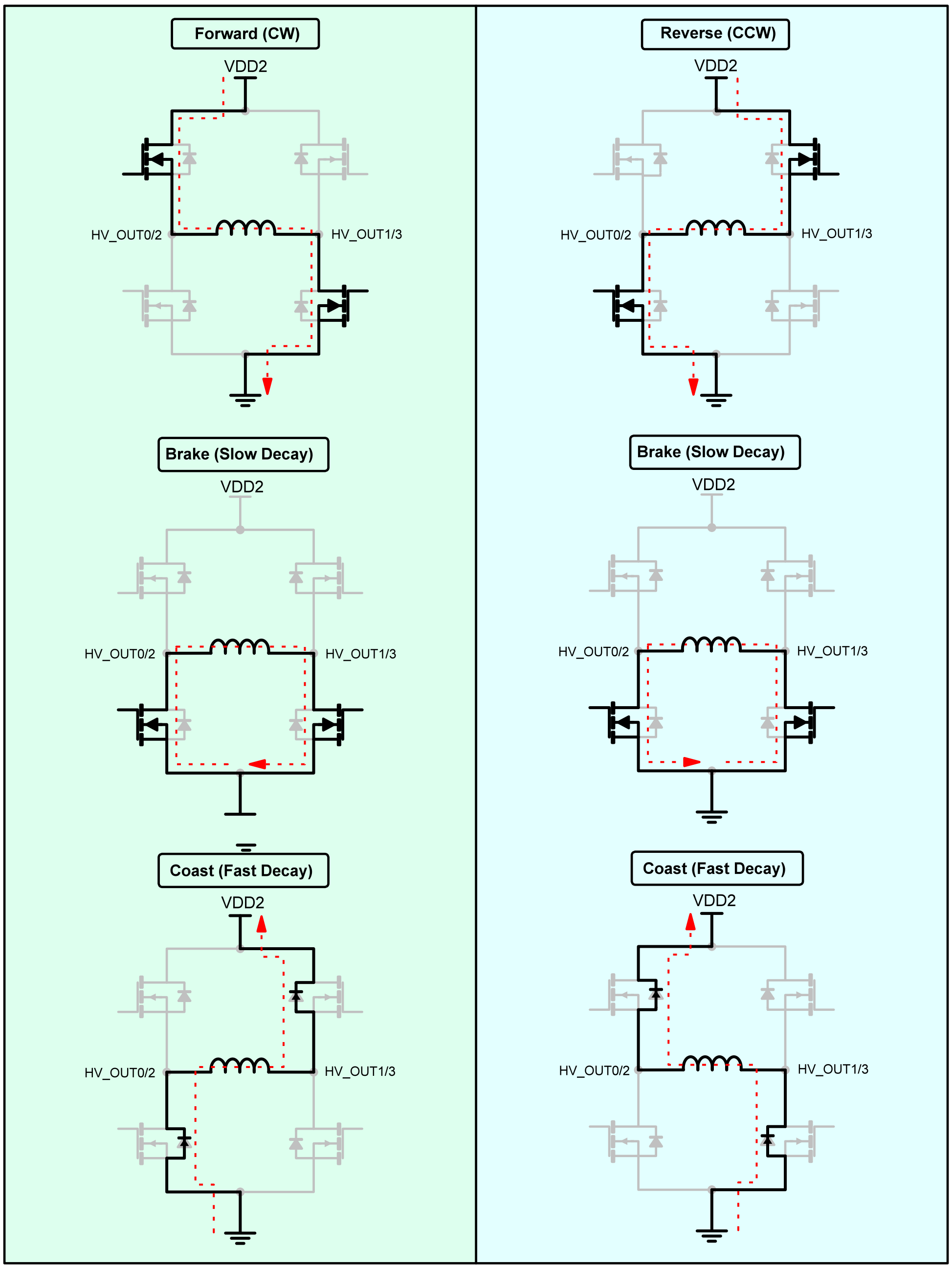


Figure 4. Decay Overview: Current Direction

PWM Current Control

The HV OUTs can be used to control the motor speed with the help of the PWM technique. Fast decay mode causes a rapid reduction in inductive current and allows the motor to coast toward zero velocity. Slow decay mode leads to a slower reduction in inductive current but produces rapid deceleration.

IN-IN mode: to configure the HV OUT CTRL for fast decay mode, apply the PWM signal to one input and keep the other input LOW; for slow decay mode, apply the PWM signal to one input and keep the other input HIGH. See Table 1 for more configuration details and Figure 5 for detailed waveforms.

Table 1. IN-IN Mode PWM Current Control

IN1	IN2	Function
PWM	0	Forward PWM, fast decay
0	PWM	Reverse PWM, fast decay
1	PWM	Forward PWM, slow decay
PWM	1	Reverse PWM, slow decay

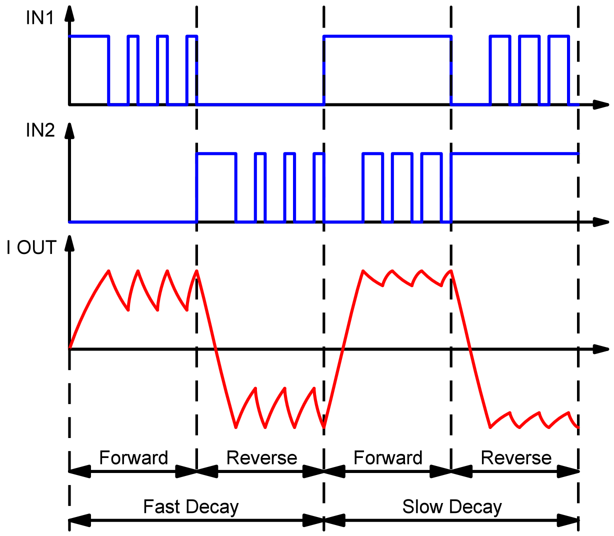


Figure 5. Decays Comparison in IN-IN Mode

PH-EN mode: to configure the HV OUT CTRL for fast decay mode, apply the PWM signal to EN input and keep Decay input HIGH; for slow decay mode, apply the PWM signal to EN input and keep Decay input LOW. Rotation direction is changed by the PH input. See Table 2 for more configuration details and Figure 6 for detailed waveforms.

Table 2. PH-EN Mode PWM Current Control

Decay	EN	PH	Function
0	PWM	0	Forward PWM, fast decay
0	PWM	1	Reverse PWM, fast decay
1	PWM	0	Forward PWM, slow decay
1	PWM	1	Reverse PWM, slow decay

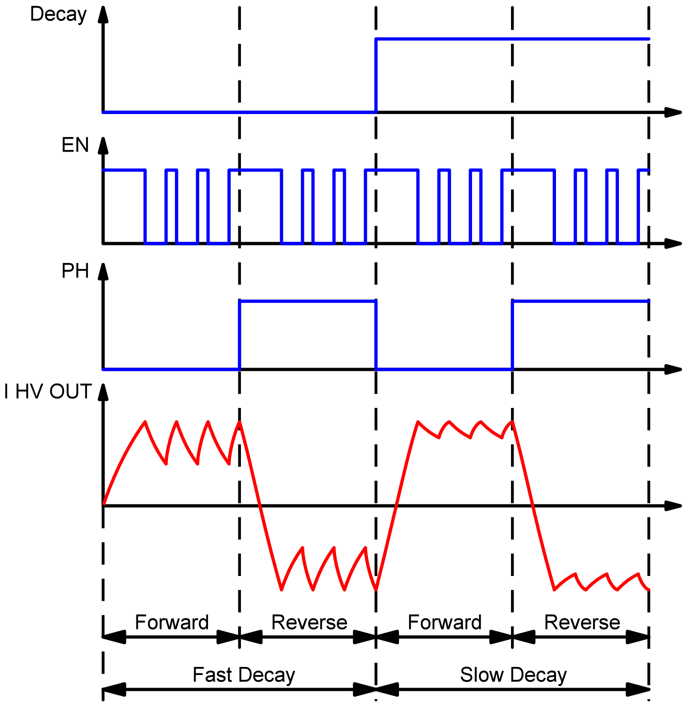


Figure 6. Decays Comparison in PH-EN Mode

2.2 Pulse Width Modulator Macrocell (PWM)

HVPAK ICs feature Pulse Width Modulator (PWM) blocks. PWM is commonly used in DC motor control, LED brightness control, and other applications.

The PWM block consists of two 8-bit counters. The first one, named PWM Period CNT, is used to create a PWM period, and the second one, named Duty Cycle CNT, is used to set the PWM Duty Cycle and to make dynamic changes in the PWM functionality.

The PWM block has an 8-bit resolution by default, but a 7-bit resolution can be selected instead to allow for a higher PWM frequency. If the 7-bit resolution is selected, the maximum value of the duty cycle counter is 127. The PWM duty cycle changes at a step of 0.4 % for the 8-bit resolution and 0.8 % for the 7-bit resolution. The duty cycle can change from true 0% to true 100%. PWM starts from the Initial duty cycle value. The block has an **UP/DOWN** internal connection that defines the direction of the duty cycle change. The duty cycle will increase if the UP/DOWN is set HIGH and decrease if set LOW.

The duty cycle in the PWM macrocell can be changed in two ways:

- The I2C Master can change the PWM Duty Cycle by I2C. The PWM Duty Cycle CNT block has two parameters: Counter Data and Current Counter Value. The Current Counter Value defines the PWM Duty Cycle. The Counter Data of PWM Duty Cycle CNT can be changed by I2C commands with a reload into the Current Counter Value.
- Matrix changeable Duty Cycle. In this case, “Duty Cycle CNT CLK” and “Duty Cycle CNT Up/Down” inputs are used. A rising edge at “Duty Cycle CNT CLK” changes the Current Counter Value according to the polarity of the “UP/DOWN” input.

Duty cycle CLK:

Duty cycle CLK selection defines the clock signal source for incrementing/decrementing the duty cycle value. It can be:

- An external clock source from the connection matrix.

- A clock pulse that is generated after the end of the PWM cycle period: PWM Period Counter overflow (ovf) selection. In this case clock pulse is generated either:
  - Every 255 (for 8-bit option) or 127 (for 7-bit option) PWM Period Clocks: select PERIOD CNT ovf.
  - Once per 2 PWM period, or every 510 (for 8-bit option) or 254 (for 7-bit option) PWM Period Clocks: select PERIOD CNT ovf/2
  - Once per 8 PWM period, or every 2040 (for 8-bit option) or 1016 (for 7-bit option) PWM Period Clocks: select PERIOD CNT ovf/8

The **PWM period (frequency)** can only be changed by changing the PWM Period CNT Clock source.

The **Keep/Stop** connection can either be selected to hold the duty cycle ("Keep" setting) or to hold the duty cycle and the OUT+ and OUT- outputs constant ("Stop" setting) when it is set HIGH.

The **Continuous/Autostop** mode is either set to "Continuous" where the PWM output duty cycle overflows when it reaches the full range value (default setting), or to" Autostop" where the PWM output stops when it reaches 0% or 100% of the duty cycle. When "Autostop" is selected, the "Boundary OSC disable" option can be activated. This allows disabling the Oscillator, used by the PWM cell, automatically when 0% or 100% of the duty cycle is reached.

As mentioned before, the PWM block consists of two 8-bit counters. The first 8-bit counter included in the block is PWM Period CNT, which sets the frequency of the PWM signal and counts from 0 to 255, and so on. There are two PWM outputs: "OUT+" and "OUT-". OUT+ is logic HIGH at the start of the period, and once the PWM period counter reaches the duty cycle value, the output changes to logic LOW until the PWM period ends. OUT+ is the positive PWM output, and OUT- is the negative PWM output that is inverted to OUT+ and shifted for deadband time if defined. Both can invert their output by register settings. See Figure 7 for details.

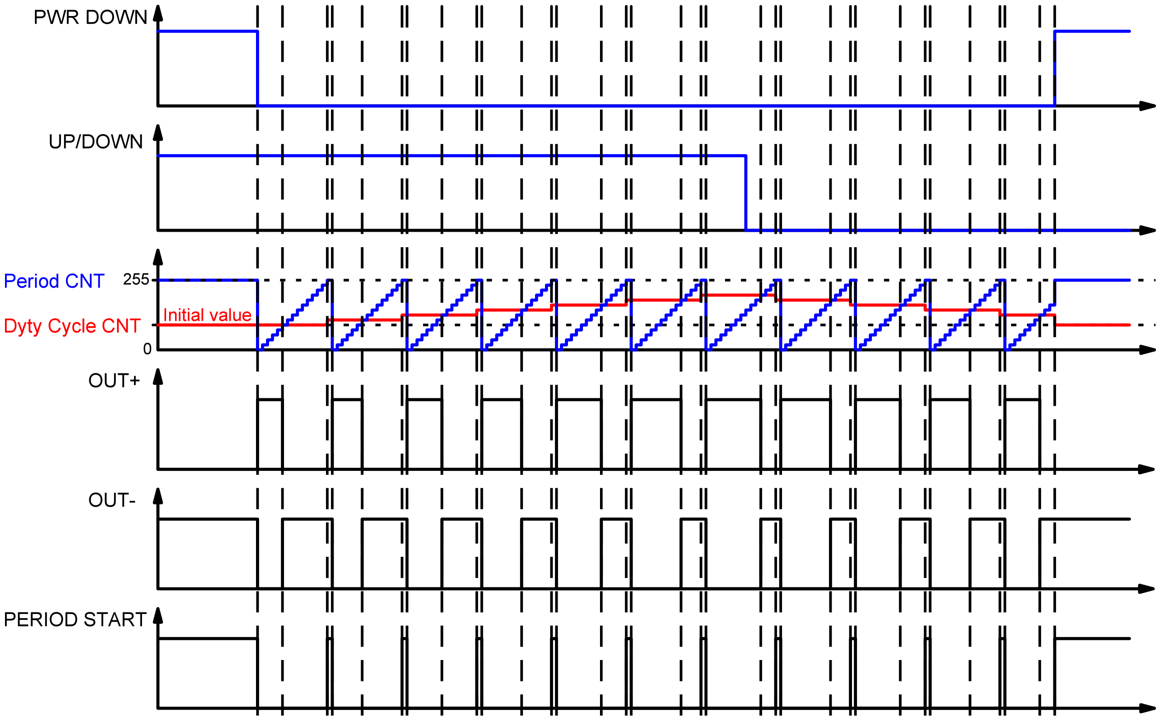


Figure 7. PWM Block Timing Diagram

In **Regular Mode** (described in this article), the Duty cycle source is set to "Duty Cycle CNT". In this mode, the value of the duty cycle is changed every rising edge on Duty Cycle CNT CLK input. The second 8-bit counter, named Duty Cycle CNT, increments or decrements the duty cycle value for the next PWM period depending on UP/DOWN input. The Duty Cycle CLK is an external clock from the matrix by default. It changes the duty cycle value by the rising edge.

In **Preset Registers Mode,** the duty cycle is changed according to 16 predefined values, named “Reg File”, every rising edge on Duty Cycle CLK input.

Selectable Preset registers are reserved to determine 16 different PWM Duty Cycle values. In Preset Registers Mode, a rising edge of “Duty Cycle CLK” changes the address read of the Reg File.

When the Reg File is selected as a source, there are three options: to use all 16 bytes, use the least significant 8 bytes, or use the most significant 8 bytes. In this case, 4 bits (when using 16-Byte Reg File) or 3 bits (when using any of the 8-byte Reg File) LSB Current Value of PWM Duty Cycle CNT is used to select data address inside the Reg File. The counter data of the Duty Cycle CNT will define the initial starting point/address in the Reg file.

2.3 Current Comparator (CCMP)

The current Comparator macrocell within HVPAK provides advanced current control. A current control circuit is provided to regulate the system in the event of an overcurrent condition, for example, an abnormal mechanical load of a DC motor. This circuit can be used for implementing constant current closed-loop systems or for current limitation.

The current is sensed by external sense resistors connected to SENSE Pins. Special current comparators are used to convert these currents to a logic level. Using a current comparator with a PWM block, the output current can be dynamically changed. For example, for a stepper motor for micro-stepping, it is possible to set 16 values for the sinusoidal current limit form.

The Current Sense Comparator (CCMP) senses current across the motors and outputs a digital signal. The Sense pins are connected to the LOW Side of HV outputs. It has two input terminals, IN+ and IN-. If IN+ is greater than IN- and the comparator’s Sleep input is Low, then CCMP output is HIGH.

Each of the Current CMP macrocells has a positive input signal that is connected to the SENSE PIN through the Selectable Gain block. The options for Selectable Gain are 4x or 8x. Each of the Current CMP macrocells has a negative input signal that can be connected to a static or dynamic variable Vref. The static Vref value is selected via registers. The dynamically changed Vref values are selected with the help of the PWM block. In this case, a 6-bit Vref is selected by 6 Least Significant bits of the Synchro Buffer, which is a part of the PWM block. Therefore, the Current Sense Comparator Vref can be changed "on the flight" from a 16-byte Register File, which is connected to the Synchro Buffer by PWM block settings, and where user-defined Vref values are stored. The Vref values are switched up or down depending on the level of the PWM macrocell Up/Down input, each pulse on DUTY_CYCLE_CLK input.

The PWM block can be active when a 16-byte Register File is used by the Current Sense Comparator.

Vref can be changed in a range from 32 mV to 2016 mV with a 32 mV step.

During power-up, the Current Sense Comparator output will remain LOW, and then become valid 12.5 µs (max) after the power-up signal goes high.

Current Regulation

For the current regulation, it is necessary to connect a sense resistor between the SENSE pin and ground. The resulting Iref current is calculated using the formula below:

$$Iref = \frac{Vref}{R_{SENSE} \cdot Gain}$$

where:

- Iref - Load Current (through controlled winding or resistive load) for selected Vref
- Vref - reference voltage of Current Sense Comparator, constant value, external source, or selectable value from Register File
- R_{SENSE} - resistance of the sense resistor
- GAIN - selectable gain (4x or 8x, selectable by the register)

The reference voltage can be set statically or dynamically. For static reference voltage setting it is required to calculate RSENSE for the selected reference voltage and the desired motor current. For dynamic reference voltage setting it is required to calculate RSENSE for the maximal user-defined reference voltage and maximal current via motor winding. 16 values in the Reg File can be used to determine the shape of motor current, for example, sine current for the stepper motor.

2.4 PWM Chopper

HVPAK ICs contain PWM Chopper macrocells. PWM chopping detection begins after a Blanking Time during PWM operations. The Blanking Time is the time when both PWM and BLANKING signals are HIGH. During the Blanking Time, the CHOP input signal is ignored, and the PWM Chopper OUT goes HIGH and continues until the PWM signal goes LOW or the CHOP signal is detected (goes HIGH). PWM Chopper OUT can be set as inverted.

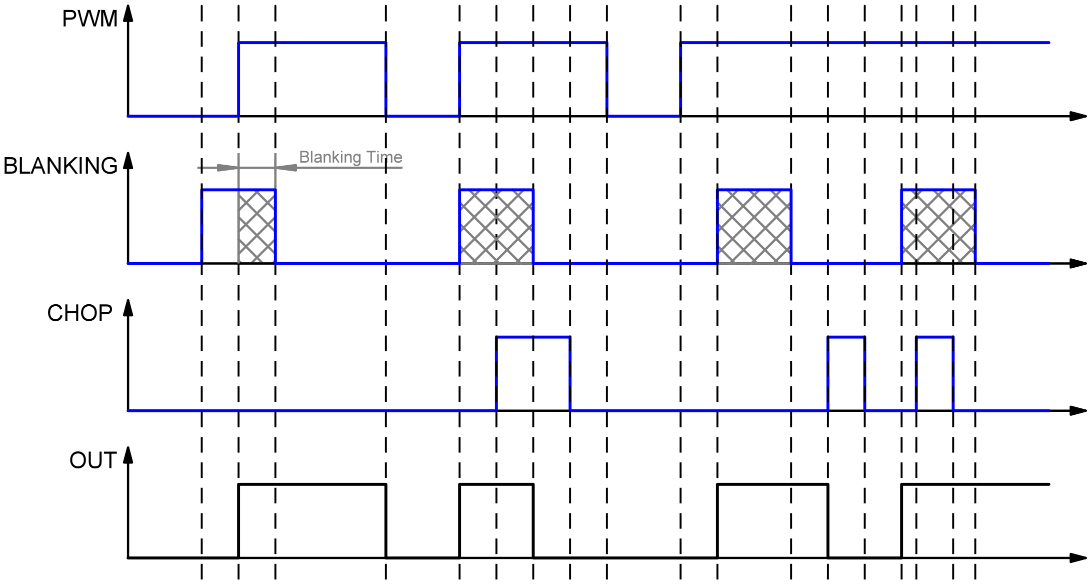


Figure 8. PWM Chopper Timing Diagram

The PWM Chopper function can be used to chop the PWM duty cycle by the Current Comparator signal. This configuration allows for the Current Comparator signal to be ignored during the blanking time tied to the motor start period. Any active signal from the Current CMP after the blanking time ends the PWM pulse period.

2.5 Differential Amplifier with Integrator and Comparator

The Differential Amplifier with Integrator and Comparator (Integrator) is useful when there is a need to keep a constant voltage at Full Bridge load (motor). Integrator PWR UP signal is active HIGH. This block operates synchronously with the PWM block.

The circuit monitors the voltage difference between the HV OUT PINs and integrates it to get an average DC voltage value. This voltage is divided by 4 and compared to the output voltage of the Vref of the comparator. If the averaged output voltage (divided by 4) is lower than Vref, UPWARD OUT goes HIGH; if the averaged output voltage (divided by 4) is higher than Vref, UPWARD Output goes LOW. If the averaged output voltage (divided by 4) is equal to Vref, Equal Output goes HIGH. These signals can be used to control the PWM duty cycle.

For correct operation, the PWM output frequency should be 44kHz or higher. The PWM duty cycle requires an update rate of at least two PWM period cycles or more. In this case, a closed-loop system controls the PWM duty cycle to ensure the constant average output voltage level.

During PWM regulation, the Full Bridge is enabled to drive current through the motor winding during the PWM on time.

The output voltage VSET can be calculated as follows:

$$VSET = Vref \cdot 4$$

where Vref - reference voltage of the Comparator.

3. Typical Applications

3.1 Constant Voltage

Only PWM, Differential Amplifier with Integrator and Comparator, and HV OUT CTRL blocks are needed to provide the motor control with constant voltage. The example design is shown in Figure 9.

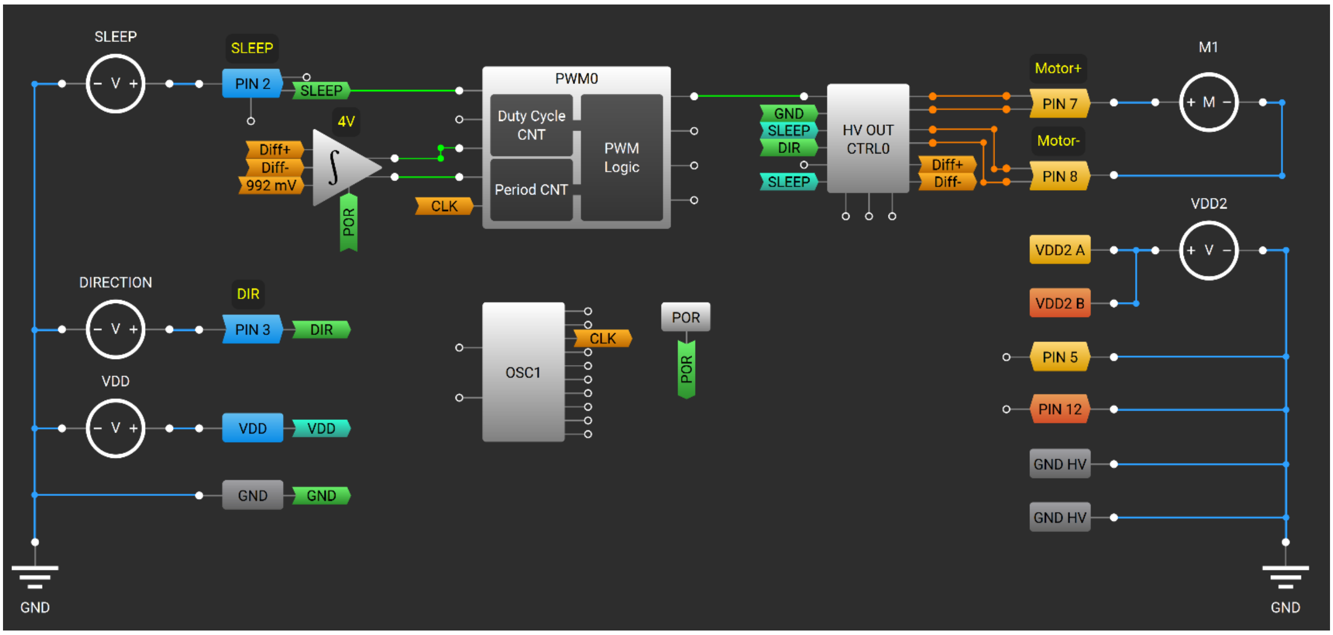
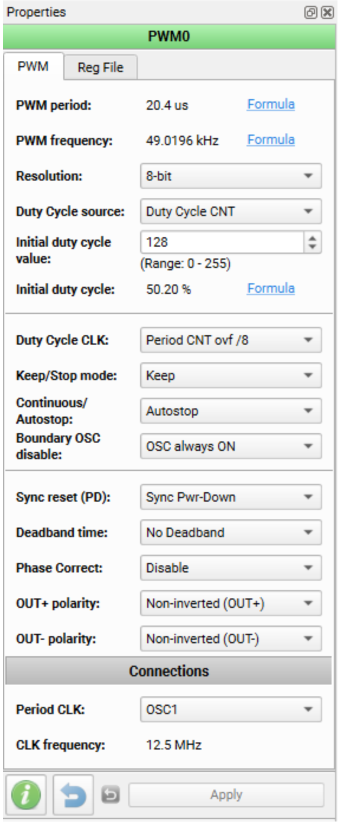


Figure 9. DC Motor Control with Constant Voltage HVPAK Design



PWM0

PWM period: 20.4 us

PWM frequency: 49.0196 kHz

Resolution: 8-bit

Duty Cycle source: Duty Cycle CNT

Initial duty cycle value: 128 (Range: 0 - 255)

Initial duty cycle: 50.20 %

Duty Cycle CLK: Period CNT ovf /8

Keep/Stop mode: Keep

Continuous/ Autostop: Autostop

Boundary OSC disable: OSC always ON

Sync reset (PD): Sync Pwr-Down

Deadband time: No Deadband

Phase Correct: Disable

OUT+ polarity: Non-inverted (OUT+)

OUT- polarity: Non-inverted (OUT-)

Connections

Period CLK: OSC1

CLK frequency: 12.5 MHz

Figure 10. PWM0 Properties

The system powers ON when the SLEEP is LOW.

The HV OUT CTRL0 block is configured as a Full Bridge. The DC motor is connected to PIN7 and PIN8. The PH input of the HV OUT CTRL0 is connected to PIN 3 (DIR). Therefore, when the DIR signal is LOW, the direction is forward, and reverse when the DIR is HIGH.

The EN input of the HV OUT CTRL0 block is connected to the PWM0 OUT+. This macrocell provides a duty cycle with ~50 kHz frequency. The initial duty cycle is 50%. The PWM0 properties are shown in Figure 10.

The Differential Amplifier with Integrator and Comparator measures the voltage on the motor between PIN7 and PIN8 and compares it with the set Vref of 992 mV (Gain = 4). Its outputs UPWARD and Equal are connected to the PWM0's UP/DOWN and KEEP accordingly. When the measured voltage is lower/higher than the desired one (Vref), the UPWARD output goes HIGH/LOW, and the PWM0 macrocell increases/decreases the duty cycle by 0.4% with the Period CNT overflow clock (every period). When the measured voltage is equal to the set reference voltage, the Equal output goes HIGH, and the PWM0 keeps the current duty cycle without any changes.

This method allows for maintaining a constant voltage on the motor regardless of the power supply or other factors.

See an example of using this feature in the application note Toy Car with Push-to-Start / Hold-to-Stop Functionality or Smart Lock Motor Driver with Voltage Regulation.

3.2 Constant Current with Fixed PWM Frequency

To create a motor control with constant current with fixed PWM frequency, the following blocks are required: CCMP, one CNT/DLY, PWM Chopper, and HV OUT CTRL. The HVPAK design is shown in Figure 11.

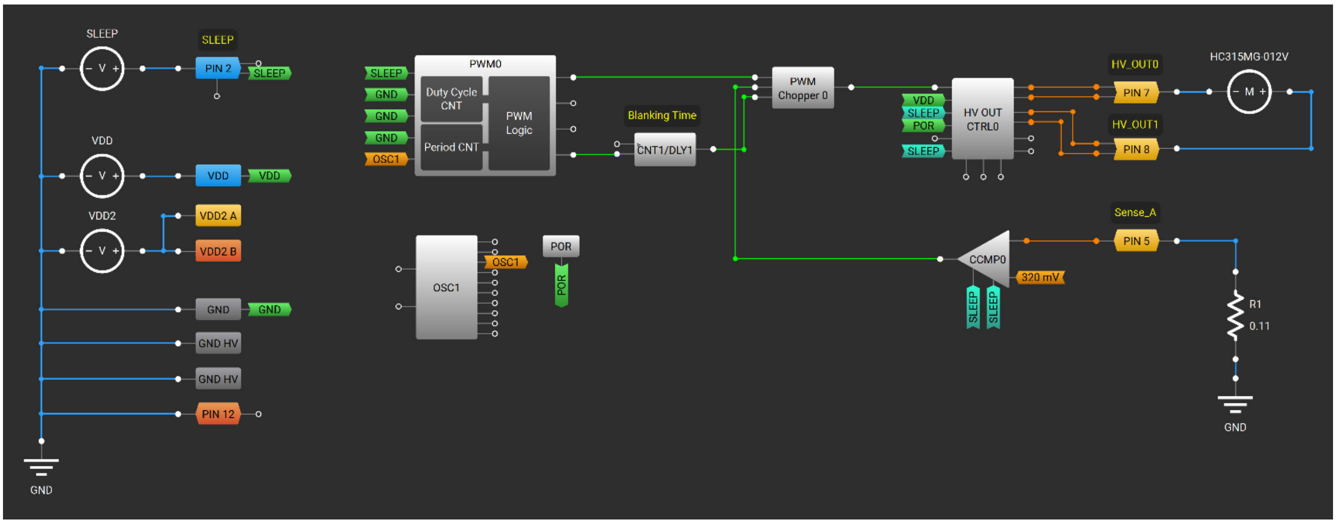


Figure 11. Constant Current Control with Fixed PWM Frequency HVPAK Design

The system powers ON when the SLEEP is LOW.

The HV OUT CTRL0 block is configured as a Full Bridge. The DC motor is connected to PIN7 and PIN8. The PH input of the HV OUT CTRL0 is connected to POR. Therefore, the direction is reversed.

The EN input of the HV OUT CTRL0 block is connected to the PWM Chopper 0 output. This macrocell provides a final PWM signal for the motor.

PWM0 provides a duty cycle of 90.2% with a 24.5 kHz frequency. This is a PWM input signal for the PWM Chopper0 and a maximum duty cycle for the motor.

The CNT1/DLY1 is configured as a falling edge delay of ~5.3 us – BLANKING input of the PWM Chopper0 and a minimum duty cycle for the motor. The blanking time allows ignoring the current spikes during HV OUTs switching.

PIN5 is connected to GND through a Rsense resistor of 0.11Ω. The CCMP0 (Gain = 8) senses the voltage drop on this sense resistor and compares it with the reference voltage Vref. The threshold current Iref is calculated using the formula below:

$$Iref = \frac{Vref}{Gain \times Rsense} = \frac{320mV}{8 \times 0.11\Omega} = 364mA$$

CCMP0 output is connected to the CHOP input of the PWM Chopper 0. When the motor current exceeds 364mA, the CCMP0 output goes HIGH. Therefore, the PWM from PWM0 will be chopped, and the PWM Chopper0 output will stay LOW until the next period. If the PWM and BLANKING inputs are HIGH, and the CHOP signal comes, the PWM Chopper0 output stays HIGH until the BLANKING signal goes LOW.

This method allows for maintaining a constant current on the motor.

See an example of using this feature in the application note Stepper Motor Driver or Power Saving Solenoid Driver.

3.3 Constant Current with PWM Fixed Off-Time

To create motor control with constant current with PWM fixed off-time, the following blocks are required: CCMP, two CNT/DLYs, two 3-bit LUTs, and HV OUT CTRL. The HVPAK design is shown in Figure 12.

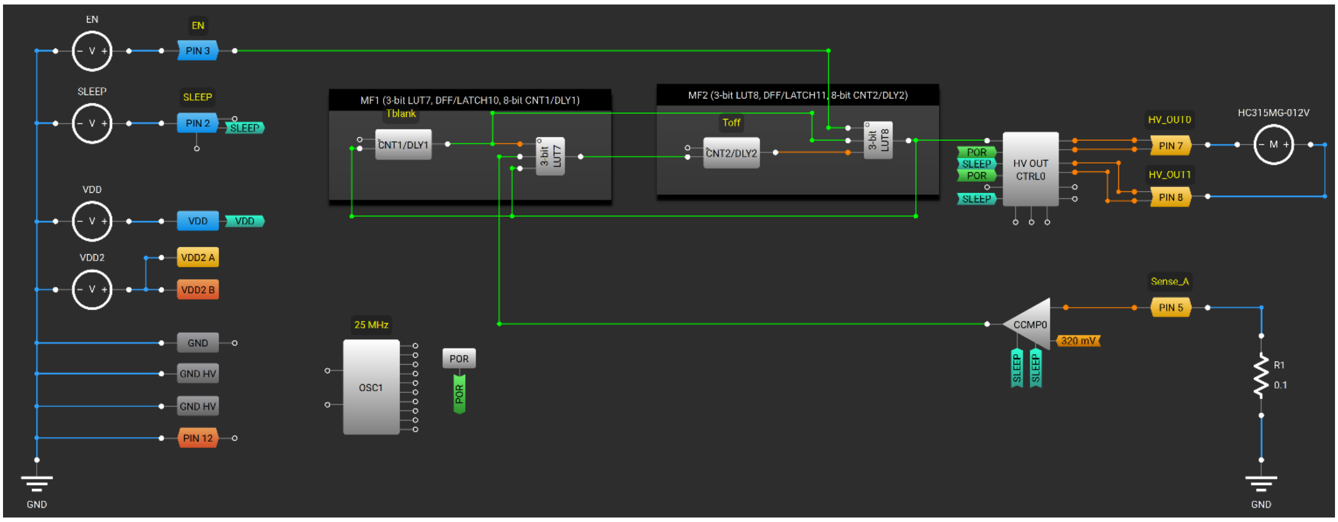


Figure 12. Constant Current Control with PWM Fixed Off-Time HVPAK Design

The system powers ON when the SLEEP is LOW and EN is HIGH.

The HV OUT CTRL0 block is configured as a Full Bridge. The DC motor is connected to PIN7 and PIN8. The PH input of the HV OUT CTRL0 is connected to POR. Therefore, the direction is reversed.

PIN5 is connected to GND through a Rsense resistor of 0.1Ω. The CCMP0 (Gain = 8) senses the voltage drop on this sense resistor and compares it with the reference voltage Vref. The threshold current Iref is calculated using the formula below:

$$Iref = \frac{Vref}{Gain \times Rsense} = \frac{320mV}{8 \times 0.1\Omega} = 400mA$$

CNT1/DLY1, 3-bit LUT7, CNT2/DLY2, and 3-bit LUT8 form the EN input signal for the HV OUT CTRL0.

When the EN on PIN3 goes HIGH, the 3-bit LUT8 goes HIGH as well. Its output is connected to the DLY IN input of the CNT1/DLY1, which is configured as a rising One shot of 3 us. This macrocell forms a minimum on-time of 3 us (Tblank). The Tblank time allows ignoring the current spikes during HV OUTs switching.

The CCMP0 output is connected to the 3-bit LUT7. When the motor current exceeds 400 mA, the CCMP0 output goes HIGH. If the CNT1/DLY1 output is LOW (3 us of minimum time to ignore the inrush current spikes), the 3-bit LUT7 output goes HIGH, enabling the falling Delay CNT2/DLY2 of 30 us. The HIGH output signal of CNT2/DLY2 turns the 3-bit LUT8 output LOW. Therefore, the enable signal of the HV OUT CTRL0 goes LOW.

The LOW output of the 3-bit LUT8 then turns the 3-bit LUT7 output LOW. The CNT2/DLY2 output goes LOW after 30 us. After this time (Toff of 30 us), the 3-bit LUT8 goes HIGH. Therefore, the enable signal of the HV OUT CTRL0 goes HIGH.

If there is still an overcurrent, the 3-bit LUT8 output goes LOW after 3 us due to the Tblank time provided by CNT1/DLY1.

If no overcurrent occurs, the enable signal of the HV OUT CTRL0 remains HIGH.

This method allows for maintaining a constant current on the motor with PWM fixed off-time.

3.4 Motor Control with Soft Start/Stop

To reduce the inrush current and ensure smooth start-up and stoppage of the DC motor, the soft start/stop functionality can be utilized. It requires just one PWM block, HV OUT CTRL, two CNT/DLYs, two LUTs, and two DFFs. See Figure 13.

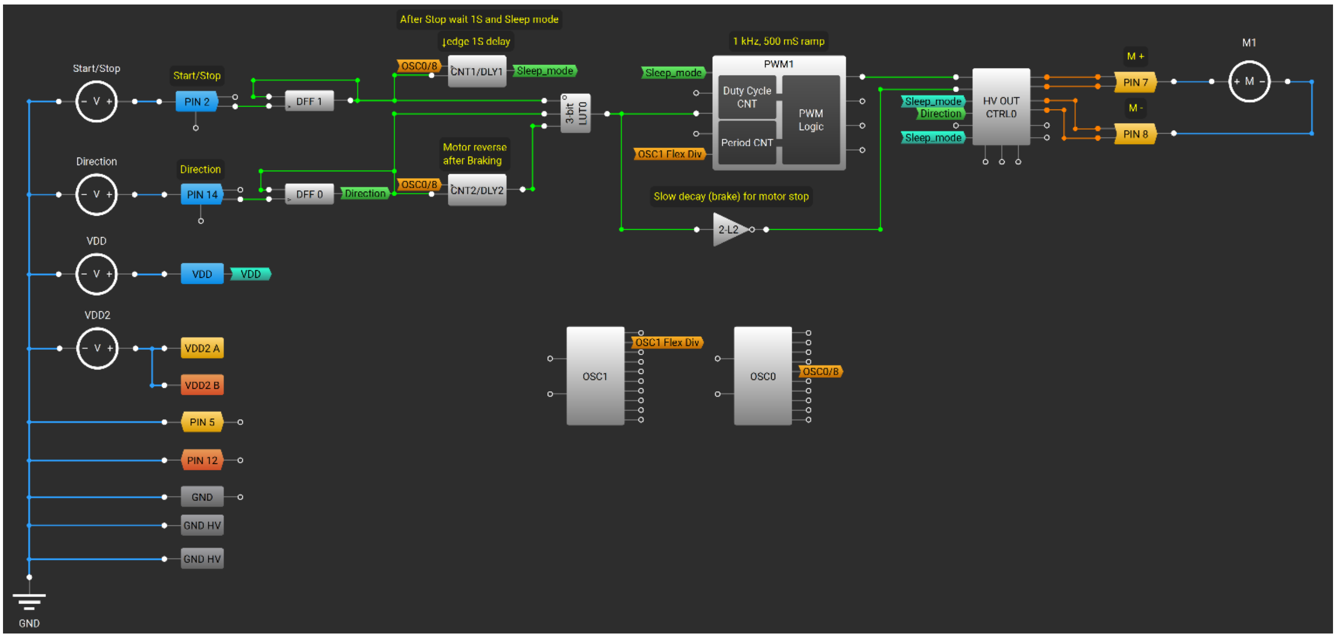


Figure 13. DC Motor Control with Soft Start/Stop HVPAK Design

The motor is connected to PIN 7 and PIN 8 of the HV OUT CTRL0 block that is configured as Full Bridge (PH-EN). The EN signal is taken from the PWM1 output. PWM1 provides a signal with 1kHz frequency.

The DFF1 latches the Start/Stop signals from PIN 2. Its output goes HIGH when the button is pressed, and the motor is running. When the button is pressed again, the DFF1 output goes LOW. The HV outputs and PWM1 blocks enter sleep mode after 1 second (CNT1/DLY1 macrocell).

The DFF0 latches the Direction signal from PIN 14. The DFF0 output is connected to the PH input of the HV OUT CTRL0 block. When the DFF0 output is LOW, the motor rotates forward, and when HIGH, the direction is reversed.

The CNT2/DLY2 delays the direction change for 800 ms, and together with the 3-bit LUT0 creates UP/DOWN logic for the PWM1 block. Therefore, when the direction is changed, the soft stop to 0% duty cycle is activated (PWM1 counting down with “Period CNT ovf /2” clock. After 800 ms, the 3-bit LUT0 output goes HIGH, and the PWM1 starts counting up to 100% with “Period CNT ovf /2” clock – soft start. In addition, the 3-bit LUT0 ensures soft start and stop when the Start/Stop button is pressed.

The 2-bit LUT2 is configured as an inverter and connected to the decay input of the HV OUT CTRL0. Thus, when the motor stops during the stop condition or direction change, the decay is slow – the motor decelerates faster compared to the fast decay. When there is no stop condition, the decay is fast, ensuring a faster current drop in the motor windings.

This method allows for bidirectional motor control with soft start and stop.

See an example of using this feature in the application note DC-DC Boost & Buzzer Driver.

3.5 Motor Stall Detection

Only one CCMP, two CNT/DLYs, and DFF are needed to provide a motor stall detection function. See Figure 14.

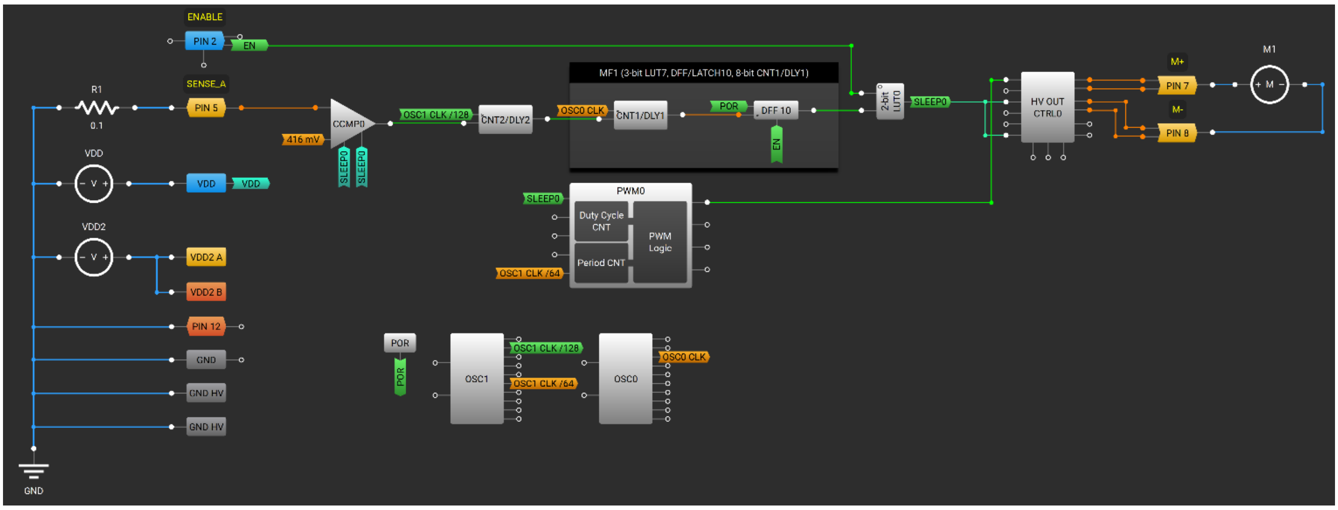


Figure 14. DC Motor Stall Detection HVPAK Design

The motor is connected to PIN 7 and PIN 8 of the HV OUT CTRL0 block that is configured as Full Bridge (PH-EN). The EN signal is taken from the PWM0 output. PWM0 provides a signal with a 1.5 kHz frequency and 50% duty cycle.

PIN5 is connected to GND through a Rsense resistor of 0.1Ω. The CCMP0 (Gain = 8) senses the voltage drop on this sense resistor and compares it with the reference voltage Vref. The threshold current Iref is calculated using the formula below:

$$Iref = \frac{Vref}{Gain \times Rsense} = \frac{416mV}{8 \times 0.1\Omega} = 520mA$$

When the stall condition occurs, the current through the motor increases and exceeds the threshold current Iref. The CCMP0 output goes HIGH. To make sure that this is a stall condition, and not a current spike, the current must exceed the threshold for a certain time (in this case, 100 ms provided with CNT1/DLY1). Since the motor is controlled by a PWM signal, there may be periods when the CCMP0 does not switch HIGH despite the stall condition. To avoid this, the CCMP0 output's falling is delayed by ~1.3 ms (2 periods of PWM0) with CNT2/DLY2.

Therefore, the CNT1/DLY1 output goes HIGH if the motor current exceeds 520 mA for more than 100 ms and clocks the DFF10. The 2-bit LUT0 puts the circuit into sleep mode if the DFF10 output is HIGH or EN signal from PIN 2 is LOW.

So, in this way, a stall detection feature for a DC motor can be implemented.

See an example of using this feature in the application note Toy Car with Push-to-Start / Hold-to-Stop Functionality.

3.6 Half Bridges Parallel Connection

The maximum current per HVPAK output pin is 1.5 A. But if there is a need to drive a load (a DC motor in this case) with a higher current, two half bridges can be connected as shown in Figure 15.

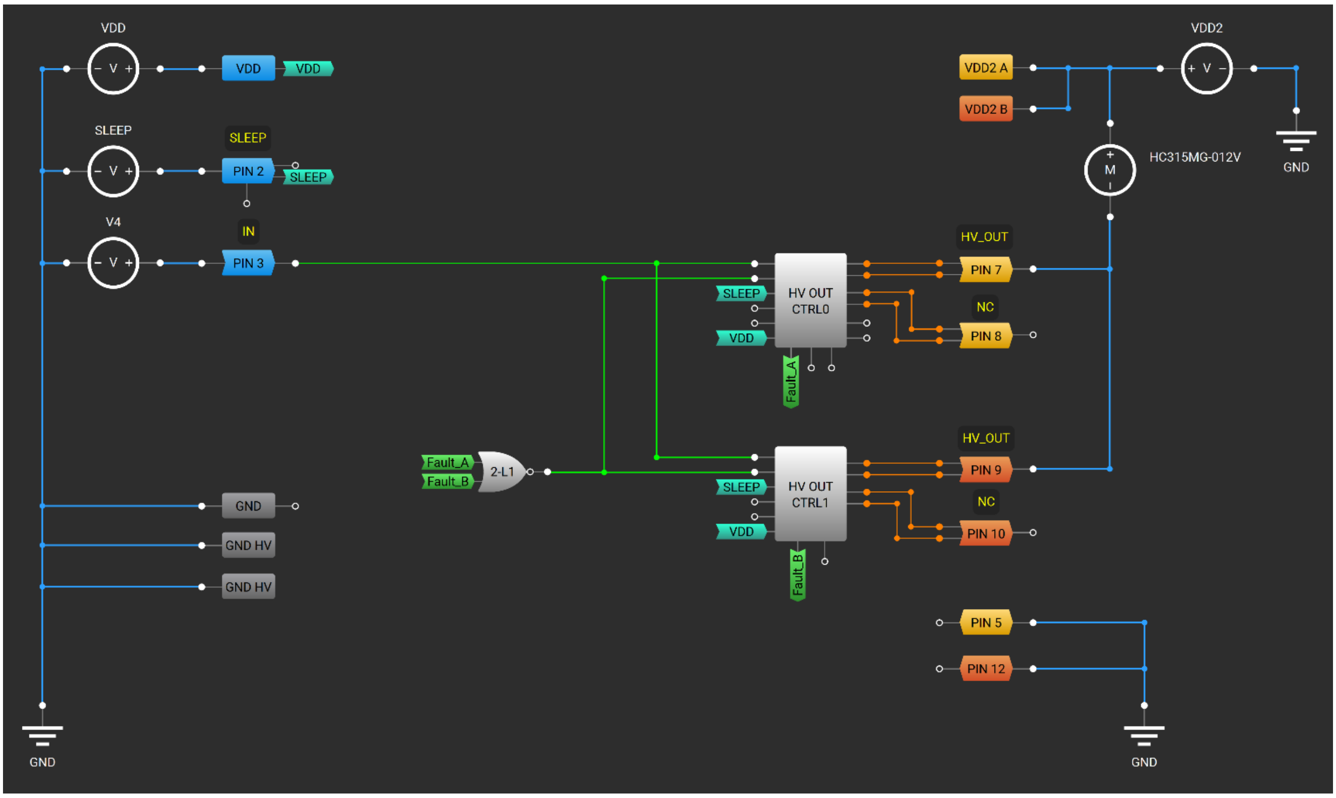


Figure 15. Half Bridges Parallel Connection HVPAK Design

When connecting PIN7 and PIN 9, it is necessary to connect VDD2_A with VDD2_B, and PIN 5 (SENSE_A) with PIN 12 (SENSE_B) as well.

HV OUT CTRL blocks are configured as half-bridges. The motor is connected between VDD2 and PIN 7 (PIN 9).

PIN 2 provides the SLEEP signal for the circuit and is connected to the Sleep0 inputs of HV OUT CTRL0 and HV OUT CTRL1 accordingly.

PIN 3 is the input signal for HV OUT CTRL blocks. When Sleep0 inputs are LOW and OE0 inputs are HIGH, the PIN 7 and PIN 9 states will be defined by the input signal from PIN 3. When the input signal is LOW, the motor is running. When the input signal is HIGH, the motor stops (brake condition).

Since HV OUT CTRL blocks are connected, their faults must be connected as well. The reason is that if any fault occurs at one of the half-bridges, it powers down this half-bridge and may cause damage to the second half-bridge. Therefore, fault signals Fault A and Fault B are connected through a 2-bit LUT1. The LUT`s output is connected to the OE0 inputs of both half bridges, ensuring turning off both half bridges in the event of any fault (OCP, Thermal).

3.7 Full Bridges Parallel Connection

The maximum current per HVPAK output pin is 1.5 A. But if there is a need to drive a load (a DC motor in this case) with a higher current, two full bridges can be connected as shown in Figure 16.

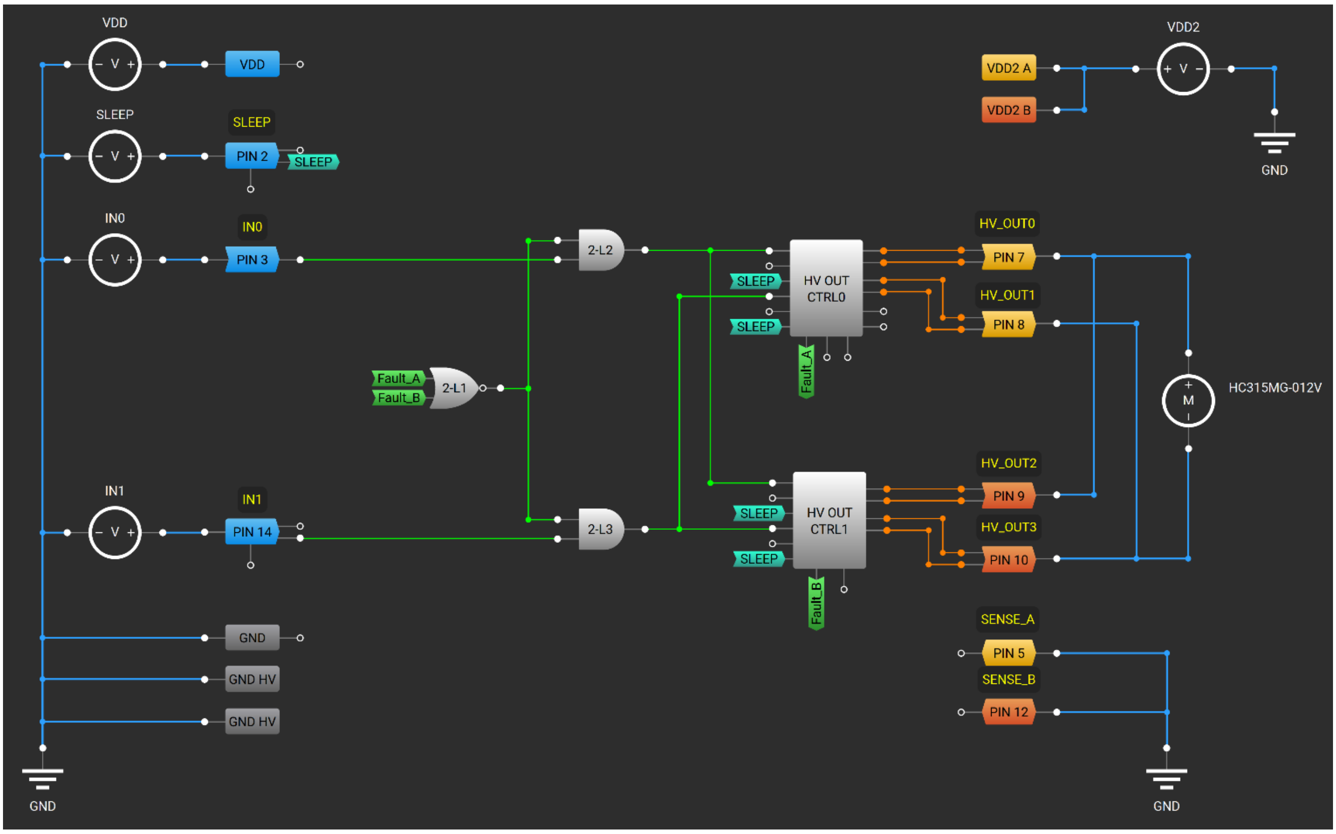


Figure 16. Full Bridges Parallel Connection HVPAK Design

When connecting PIN7 with PIN 9 and PIN 8 with PIN 10, it is necessary to connect VDD2_A with VDD2_B, and PIN 5 (SENSE_A) with PIN 12 (SENSE_B) as well.

HV OUT CTRL blocks are configured as full bridges in IN-IN mode. The motor is connected between PIN 7 (PIN 9) and PIN 8 (PIN 10).

PIN 2 provides the SLEEP signal for the circuit and is connected to the Sleep0/1 inputs of HV OUT CTRL0 and HV OUT CTRL1 accordingly.

Since HV OUT CTRL blocks are connected, their faults must be connected as well. The reason is that if any fault occurs at one of the full bridges, it powers down this full bridge and may cause damage to the second full bridge. Therefore, fault signals Fault A and Fault B are connected through a 2-bit LUT1. The LUT`s output is connected to 2-bit LUT2 and 2-bit LUT3, ensuring turning off both full bridges in the event of any fault (OCP, Thermal).

PIN 3 (PIN 14) is connected to 2-bit LUT2 (2-bit LUT3). The LUTs` outputs are connected to IN0 and IN1 of the HV OUT CTRL blocks accordingly. When Sleepx inputs are LOW, and there are no faults, the PIN 7 (PIN 8) and PIN 9 (PIN 10) states will be defined by the input signal from PIN 3 (PIN 14) and full bridge logic for the IN-IN mode.

4. Conclusions

HVPAK ICs extend the GreenPAK family by integrating mixed-signal configurability with dedicated high-voltage H-bridge and half-bridge functionality, enabling compact and efficient motor-control and power-management solutions. By focusing on the high voltage macrocells, this article has outlined the key building blocks that differentiate HVPAK from standard GreenPAK devices, explained their operating principles, and described the available configuration options. Practical application examples demonstrate how these blocks can be combined to implement common motor-drive and switching topologies with minimal external components. With this foundation, designers can confidently select, configure, and apply HVPAK devices to bring motors and other high voltage loads into operation quickly, while benefiting from the flexibility, integration, and simplicity that define the GreenPAK platform.

5. Revision History

Revision	Date	Description
1.00	April 22, 2026	Initial release