Date :Jun. 26, 2024

# RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

| Product Category | MPU/MCU | | Document No. | TN-RZ*-A0138A/E | Rev. | 1.00 |
|---|---|---|---|---|---|---|
| Title | Write access issue in case of accessing external DDR memory | | Information Category | Technical Notification | | |
| Applicable Product | RZ/V2H Group | Lot No.<br>All lots | Reference Document | RZ/V2H Group User's Manual: Hardware Rev.1.01<br>RZ/V2H Group User's Manual: Hardware (Additional document) Rev.1.01<br>RZ/V2H Group DDRTOP Application Note Rev.01.01 | | |

[Phenomenon]

Write data may be corrupted when accessing external DDR memory.

[User's manual and DDRTOP allocation note Update]

Setting the ECC on function is prohibited.

Turn on the Data mask disable function of the DDR memory controller.

[PCN]

To avoid this issue, we will revise the device.

The mass production date is '25/05, and it will replace existing products as a PCN.

# 1.1 Overview
## 1.1.3 Functions
### Table 1.1-4 On-chip SRAM and External Memory Interfaces

[Form]

| Item | Description |
|---|---|
| System RAM | • 6 Mbytes (with ECC) |
| External Bus Controller for LPDDR4/4X SDRAM (DDR) | • 2 channels<br>• Support for LPDDR4-3200 and LPDDR4X-3200<br>• Bus width: 32-bits<br>• In line ECC (16 ECC regions) supported (support for error detection interrupts)<br>• Memory size: Up to 16 Gbytes (8 Gbytes per channel)<br>• Auto-refresh, self-refresh, and IO retention supported<br>• Memory access protection for secure regions using TZC-400 (Arm® TrustZone® supported) |
| xSPI Controller (xSPI) | • 1 channel (2 chip select signals)<br>• Compliant with the xSPI protocol<br>• Protocol mode<br>1, 4, or 8 pins with SDR or DDR (1S-1S-1S, 4S-4D-4D, 8D-8D-8D)<br>2 or 4 pins with SDR (1S-2S-2S, 2S-2S-2S, 1S-4S-4S, 4S-4S-4S)<br>• Support for XiP mode<br>• Support for up to 256-Mbyte address space (support for up to 128M bytes per channel address space in boot sequence) |
| SD Card Host Interface/ Multimedia Card Interface (SD/MMC) | • 3 channels<br>• Channel 0 supports SDHI and e-MMC.<br>• Channels 1 and 2 support SDHI.<br>• SD memory I/O card interface (1-bit or 4-bit SD bus)<br>• SD, SDHC and SDXC SD memory card access supported<br>• Compliant with SD specification version 3.01<br>• Default, high-speed, UHS-I/SDR50, SDR104 and DDR50 transfer modes supported<br>• Error check function: CRC7 (command), CRC16 (data)<br>• Support for card detection and write protection<br>• MMC interface (1-bit, 4-bit, or 8-bit MMC bus)<br>• e-MMC device access supported<br>• Compliant with eMMC 4.51<br>• High-speed, HS200 and HS-DDR transfer modes supported |

[To]

| Item | Description |
|---|---|
| System RAM | • 6 Mbytes (with ECC) |
| External Bus Controller for LPDDR4/4X SDRAM (DDR) | • 2 channels<br>• Support for LPDDR4-3200 and LPDDR4X-3200<br>• Bus width: 32-bits<br>• In line ECC (16 ECC regions) supported (support for error detection interrupts)*1<br>• Memory size: Up to 16 Gbytes (8 Gbytes per channel)<br>• Auto-refresh, self-refresh, and IO retention supported<br>• Memory access protection for secure regions using TZC-400 (Arm® TrustZone® supported) |
| xSPI Controller (xSPI) | • 1 channel (2 chip select signals)<br>• Compliant with the xSPI protocol<br>• Protocol mode<br>1, 4, or 8 pins with SDR or DDR (1S-1S-1S, 4S-4D-4D, 8D-8D-8D)<br>2 or 4 pins with SDR (1S-2S-2S, 2S-2S-2S, 1S-4S-4S, 4S-4S-4S)<br>• Support for XiP mode<br>• Support for up to 256-Mbyte address space (support for up to 128M bytes per channel address space in boot sequence) |
| SD Card Host Interface/ Multimedia Card Interface (SD/MMC) | • 3 channels<br>• Channel 0 supports SDHI and e-MMC.<br>• Channels 1 and 2 support SDHI.<br>• SD memory I/O card interface (1-bit or 4-bit SD bus)<br>• SD, SDHC and SDXC SD memory card access supported<br>• Compliant with SD specification version 3.01<br>• Default, high-speed, UHS-I/SDR50, SDR104 and DDR50 transfer modes supported<br>• Error check function: CRC7 (command), CRC16 (data)<br>• Support for card detection and write protection<br>• MMC interface (1-bit, 4-bit, or 8-bit MMC bus)<br>• e-MMC device access supported<br>• Compliant with eMMC 4.51<br>• High-speed, HS200 and HS-DDR transfer modes supported |

Note 1. This function is supported by the devices other than "#AC0" and "#BC0". "#AC0" and "#BC0" do not support it. (Refer to **Table 1.1-1**)

User's Manual
3.4 LPDDR4/4X controller(DDR)
3.4.1 Overview

[Form]

### 3.4.1 Overview

This section describes the features of the DDR unit of this LSI.

This unit is an external bus controller for LPDDR4 and LPDDR4X. This unit supports LPDDR4-3200 and LPDDR4X-3200. The interface bus width is 32 bits. It supports the in-line ECC feature.

It is composed of the DDR controller block (MC) and the DDR PHY block (PHY).

For the setup of this block, refer to the Linux software package of this LSI, which contains the DDR setup codes.

[To]

### 3.4.1 Overview

This section describes the features of the DDR unit of this LSI.

This unit is an external bus controller for LPDDR4 and LPDDR4X. This unit supports LPDDR4-3200 and LPDDR4X-3200. The interface bus width is 32 bits. It supports the in-line ECC feature.*1

It is composed of the DDR controller block (MC) and the DDR PHY block (PHY).

For the setup of this block, refer to the Linux software package of this LSI, which contains the DDR setup codes.

**Note 1.** This function is supported by the devices other than "#AC0" and "#BC0". "#AC0" and "#BC0" do not support it.

User's Manual
3.4 LPDDR4/4X controller(DDR)
3.4.1.1 Features
Tabel 3.4-1 LPDDR4/4X Controller Features

[From]

| Feature | Description |
|---|---|
| DRAM I/F | • LPDDR4: 3200 Mbps (1600 MHz)<br>• LPDDR4X: 3200 Mbps (1600 MHz)<br>• Width: 32 bits (16 bits per channel)<br>• Rank: 1, 2<br>• Density: Up to 64Gb (byte mode not supported) |
| MC | • Fully pipelined command, read and write data interfaces to the controller.<br>• Advanced bank look-ahead features for high memory throughput.<br>• A programmable register interface to control memory parameters and protocols including auto pre-charge.<br>• Full initialization of memory on controller reset.<br>• Supports the Weighted Round-Robin arbitration schema for arbitrating request from the ports.<br>• ECC function for single bit and double bit error reporting, single bit error correction, and programmable removal of ECC storage.<br>• Built-in self-test (BIST) for external DRAM memories. |
| PHY | For more information, refer to the User's Manual Additional Document. |
| Low power | • Multiple low power states (power-down, self-refresh, I/O retention)<br>• Automatic or software interface |

[To]

| Feature | Description |
|---|---|
| DRAM I/F | • LPDDR4: 3200 Mbps (1600 MHz)<br>• LPDDR4X: 3200 Mbps (1600 MHz)<br>• Width: 32 bits (16 bits per channel)<br>• Rank: 1, 2<br>• Density: Up to 64Gb (byte mode not supported) |
| MC | • Fully pipelined command, read and write data interfaces to the controller.<br>• Advanced bank look-ahead features for high memory throughput.<br>• A programmable register interface to control memory parameters and protocols including auto pre-charge.<br>• Full initialization of memory on controller reset.<br>• Supports the Weighted Round-Robin arbitration schema for arbitrating request from the ports.<br>• ECC function for single bit and double bit error reporting, single bit error correction, and programmable removal of ECC storage.*1<br>• Built-in self-test (BIST) for external DRAM memories. |

Note 1. This function is supported by the devices other than "#AC0" and "#BC0". "#AC0" and "#BC0" do not support it.

User's Manual
3.4 LPDDR4/4X controller(DDR)
3.4.5.1 Interrupt List
Tabel 3.4-15 Interrupt List

[Form]

| Interrupt Signal | Description | Pulse/ Level | Min Pulse | Active Level | Clock |
|---|---|---|---|---|---|
| controller_int | Interrupt signal from the controller. This is a level-sensitive signal which will be asserted when the controller detects any interrupt conditions. An interrupt will only cause the controller_int signal to be asserted if the associated bit is set in the int_status_master parameter and cleared in the int_mask_master parameter (and the uppermost bit of the int_mask_master parameter is cleared to 0). | Level | — | High | DfiClk |
| DDR_CH0_perf_mon _data_ status[1:0] | Performance monitor signal for ch0.<br>Single cycle pulse per event.<br>[0] = Uncorrectable ECC error detected on read data.<br>[1] = ECC data correction has occurred on read data. | Pulse | 1 cycle | High | DfiClk |
| DDR_CH1_perf_mon _data_ status[1:0] | Performance monitor signal for ch1.<br>Single cycle pulse per event.<br>[0] = Uncorrectable ECC error detected on read data.<br>[1] = ECC data correction has occurred on read data. | Pulse | 1 cycle | High | DfiClk |

[To]

| Interrupt Signal | Description | Pulse/ Level | Min Pulse | Active Level | Clock |
|---|---|---|---|---|---|
| controller_int | Interrupt signal from the controller. This is a level-sensitive signal which will be asserted when the controller detects any interrupt conditions. An interrupt will only cause the controller_int signal to be asserted if the associated bit is set in the int_status_master parameter and cleared in the int_mask_master parameter (and the uppermost bit of the int_mask_master parameter is cleared to 0). | Level | — | High | DfiClk |
| DDR_CH0_perf_mon _data_ status[1:0]*1 | Performance monitor signal for ch0.<br>Single cycle pulse per event.<br>[0] = Uncorrectable ECC error detected on read data.<br>[1] = ECC data correction has occurred on read data. | Pulse | 1 cycle | High | DfiClk |
| DDR_CH1_perf_mon _data_ status[1:0]*1 | Performance monitor signal for ch1.<br>Single cycle pulse per event.<br>[0] = Uncorrectable ECC error detected on read data.<br>[1] = ECC data correction has occurred on read data. | Pulse | 1 cycle | High | DfiClk |

Note 1. This function is supported by the devices other than "#AC0" and "#BC0". "#AC0" and "#BC0" do not support it.

User's Manual
3.4 LPDDR4/4X controller(DDR)
3.4.5.1.1 controller_int
Table 3.4-16 Groups of controller_int(2/2)

[Form]

| Logic Group | Bit in the int_status_master and int_mask_master Parameters | Name of the Group Status Parameter | Name of the Group Mask Parameter | Name of the Group Acknowledge Parameter |
|---|---|---|---|---|
| User Interface | 6 | int_status_userif | int_mask_userif | int_ack_userif |
| Training | 5 | int_status_training | int_mask_training | int_ack_training |
| Reserved | 5 to 3 | — | — | — |
| Low Power Control | 2 | int_status_lowpower | int_mask_lowpower | int_ack_lowpower |
| ECC | 1 | int_status_ecc | int_mask_ecc | int_ack_ecc |
| Timeout | 0 | int_status_timeout | int_mask_timeout | int_ack_timeout |

[To]

| Logic Group | Bit in the int_status_master and int_mask_master Parameters | Name of the Group Status Parameter | Name of the Group Mask Parameter | Name of the Group Acknowledge Parameter |
|---|---|---|---|---|
| User Interface | 6 | int_status_userif | int_mask_userif | int_ack_userif |
| Training | 5 | int_status_training | int_mask_training | int_ack_training |
| Reserved | 5 to 3 | — | — | — |
| Low Power Control | 2 | int_status_lowpower | int_mask_lowpower | int_ack_lowpower |
| ECC*1 | 1 | int_status_ecc | int_mask_ecc | int_ack_ecc |
| Timeout | 0 | int_status_timeout | int_mask_timeout | int_ack_timeout |

Note 1. This function is supported by the devices other than "#AC0" and "#BC0". "#AC0" and "#BC0" do not support it.

User's Manual
3.4 LPDDR4/4X controller(DDR)
3.4.5.1.1 controller_int
Table 3.4-25 Bits of the ECC Group

[Form]

| Bit | Description |
|---|---|
| 15 to 9 | Reserved |
| 8 | An ECC correctable error has been detected in a scrubbing read operation. |
| 7 | The scrub operation triggered by setting the ecc_scrub_start parameter has completed. |
| 6 | One or more ECC writeback commands could not be executed. |
| 5, 4 | Reserved |
| 3 | Multiple uncorrectable ECC events have been detected. |
| 2 | An uncorrectable ECC event has been detected. |
| 1 | Multiple correctable ECC events have been detected. |
| 0 | A correctable ECC event has been detected. |

[To]

| Bit | Description |
|---|---|
| 15 to 9 | Reserved |
| 8 | An ECC correctable error has been detected in a scrubbing read operation. |
| 7 | The scrub operation triggered by setting the ecc_scrub_start parameter has completed. |
| 6 | One or more ECC writeback commands could not be executed. |
| 5, 4 | Reserved |
| 3 | Multiple uncorrectable ECC events have been detected. |
| 2 | An uncorrectable ECC event has been detected. |
| 1 | Multiple correctable ECC events have been detected. |
| 0 | A correctable ECC event has been detected. |

Note 1. This function is supported by the devices other than "#AC0" and "#BC0". "#AC0" and "#BC0" do not support it.

User's Manual
3.4 LPDDR4/4X controller(DDR)
3.4.5.1.2 DDR_CHn_perf_mon_data_status[1:0] (n = 0, 1)

[Form]

#### 3.4.5.1.2 DDR_CHn_perf_mon_data_status[1:0] (n = 0, 1)

This unit has a mechanism to notify the user that a correctable or uncorrectable ECC error has been detected on the read data. This signal is the edge type interrupt when it has occurred.

- Bit 0 is asserted to 1 for 1 DfiClk when an uncorrectable ECC error has been detected on the read data.
- Bit 1 is asserted to 1 for 1 DfiClk when ECC data correction has occurred on the read data.

[To]

#### 3.4.5.1.2 DDR_CHn_perf_mon_data_status[1:0] (n = 0, 1)

This unit has a mechanism to notify the user that a correctable or uncorrectable ECC error has been detected on the read data. This signal is the edge type interrupt when it has occurred.

- Bit 0 is asserted to 1 for 1 DfiClk when an uncorrectable ECC error has been detected on the read data.
- Bit 1 is asserted to 1 for 1 DfiClk when ECC data correction has occurred on the read data.

This function is supported by the devices other than "#AC0" and "#BC0". "#AC0" and "#BC0" do not support it.

User's Manual
3.4 LPDDR4/4X controller(DDR)
3.4.6 Usage Notes
Table 3.4-27 Restrictions

[Form]

| Item | Restriction |
|---|---|
| Period of DRAM inaccessibility | It has the period of DRAM inaccessibility to execute the periodic training. It is 1,280 core clock cycles every 134,217,728 core clock cycles. So, it depends only on the Bit Rate (the frequency of the core clock). It is below:<br>3200 Mbps: 1.6 µs every 167 ms |
| Density when ECC function is enabled | When the ECC function is enabled, 1/8 is used for the ECC code, so the usable density is 7/8. |

[To]

| Item | Restriction |
|---|---|
| Period of DRAM inaccessibility | It has the period of DRAM inaccessibility to execute the periodic training. It is 1,280 core clock cycles every 134,217,728 core clock cycles. So, it depends only on the Bit Rate (the frequency of the core clock). It is below:<br>3200 Mbps: 1.6 µs every 167 ms |
| Density when ECC function is enabled*1 | When the ECC function is enabled, 1/8 is used for the ECC code, so the usable density is 7/8. |

Note 1. This function is supported by the devices other than "#AC0" and "#BC0". "#AC0" and "#BC0" do not support it.

# RZ/V2H DDRTOP Application Note
# Overview sheet

[Form]

| Features of MC | Setting in this document |
|---|---|
| Programmable Address Order | Recommended setting |
| Multi-Port Arbiter | Simple Round-Robin |
| ECC Option | Minimum settings to enable |

[To]

| Features of MC | Setting in this document |
|---|---|
| Programmable Address Order | Recommended setting |
| Multi-Port Arbiter | Simple Round-Robin |
| ECC Option (*1) | Minimum settings to enable |

Note 1) This function is supported by the devices other than "#AC0" and "BC#0". "#AC0" and "#BC0" do not support it.

# RZ/V2H DDRTOP Application Note
# 01_DRAM sheet

## [Form]

| ConfigName | ConfigGroup1 | ConfigGroup2 | ConfigGroup3 | DRAM | Speed [M | Frequenc | Die Width | Die densit | Width | Rank | Density [C | BL | WLS | RD-DBI | WR-DBI | DMD |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| L4.R2W32X16D16S32.ADED | L4.R2W32X16 | L4.R2W32X16D16S32 | L4.R2W32X16D16S32.ADED | LPDDR4 | 3200 | 1600 | 16 | 16 | 32 | 2 | 64 | 16 | A | Disabled | Enabled | Disabled |
| L4.R2W32X16D16S32.ADEE | L4.R2W32X16 | L4.R2W32X16D16S32 | L4.R2W32X16D16S32.ADEE | LPDDR4 | 3200 | 1600 | 16 | 16 | 32 | 2 | 64 | 16 | A | Disabled | Enabled | Enabled |
| L4.R2W32X16D16S32.BDED | L4.R2W32X16 | L4.R2W32X16D16S32 | L4.R2W32X16D16S32.BDED | LPDDR4 | 3200 | 1600 | 16 | 16 | 32 | 2 | 64 | 16 | B | Disabled | Enabled | Disabled |
| L4.R2W32X16D16S32.BDEE | L4.R2W32X16 | L4.R2W32X16D16S32 | L4.R2W32X16D16S32.BDEE | LPDDR4 | 3200 | 1600 | 16 | 16 | 32 | 2 | 64 | 16 | B | Disabled | Enabled | Enabled |
| L4.R2W32X16D8S32.ADED | L4.R2W32X16 | L4.R2W32X16D8S32 | L4.R2W32X16D8S32.ADED | LPDDR4 | 3200 | 1600 | 16 | 8 | 32 | 2 | 32 | 16 | A | Disabled | Enabled | Disabled |
| L4.R2W32X16D8S32.ADEE | L4.R2W32X16 | L4.R2W32X16D8S32 | L4.R2W32X16D8S32.ADEE | LPDDR4 | 3200 | 1600 | 16 | 8 | 32 | 2 | 32 | 16 | A | Disabled | Enabled | Enabled |
| L4.R2W32X16D8S32.BDED | L4.R2W32X16 | L4.R2W32X16D8S32 | L4.R2W32X16D8S32.BDED | LPDDR4 | 3200 | 1600 | 16 | 8 | 32 | 2 | 32 | 16 | B | Disabled | Enabled | Disabled |
| L4.R2W32X16D8S32.BDEE | L4.R2W32X16 | L4.R2W32X16D8S32 | L4.R2W32X16D8S32.BDEE | LPDDR4 | 3200 | 1600 | 16 | 8 | 32 | 2 | 32 | 16 | B | Disabled | Enabled | Enabled |
| L4.R1W32X16D16S32.ADED | L4.R1W32X16 | L4.R1W32X16D16S32 | L4.R1W32X16D16S32.ADED | LPDDR4 | 3200 | 1600 | 16 | 16 | 32 | 1 | 32 | 16 | A | Disabled | Enabled | Disabled |
| L4.R1W32X16D16S32.ADEE | L4.R1W32X16 | L4.R1W32X16D16S32 | L4.R1W32X16D16S32.ADEE | LPDDR4 | 3200 | 1600 | 16 | 16 | 32 | 1 | 32 | 16 | A | Disabled | Enabled | Enabled |
| L4.R1W32X16D16S32.BDED | L4.R1W32X16 | L4.R1W32X16D16S32 | L4.R1W32X16D16S32.BDED | LPDDR4 | 3200 | 1600 | 16 | 16 | 32 | 1 | 32 | 16 | B | Disabled | Enabled | Disabled |
| L4.R1W32X16D16S32.BDEE | L4.R1W32X16 | L4.R1W32X16D16S32 | L4.R1W32X16D16S32.BDEE | LPDDR4 | 3200 | 1600 | 16 | 16 | 32 | 1 | 32 | 16 | B | Disabled | Enabled | Enabled |
| L4.R1W32X16D8S32.ADED | L4.R1W32X16 | L4.R1W32X16D8S32 | L4.R1W32X16D8S32.ADED | LPDDR4 | 3200 | 1600 | 16 | 8 | 32 | 1 | 16 | 16 | A | Disabled | Enabled | Disabled |
| L4.R1W32X16D8S32.ADEE | L4.R1W32X16 | L4.R1W32X16D8S32 | L4.R1W32X16D8S32.ADEE | LPDDR4 | 3200 | 1600 | 16 | 8 | 32 | 1 | 16 | 16 | A | Disabled | Enabled | Enabled |
| L4.R1W32X16D8S32.BDED | L4.R1W32X16 | L4.R1W32X16D8S32 | L4.R1W32X16D8S32.BDED | LPDDR4 | 3200 | 1600 | 16 | 8 | 32 | 1 | 16 | 16 | B | Disabled | Enabled | Disabled |
| L4.R1W32X16D8S32.BDEE | L4.R1W32X16 | L4.R1W32X16D8S32 | L4.R1W32X16D8S32.BDEE | LPDDR4 | 3200 | 1600 | 16 | 8 | 32 | 1 | 16 | 16 | B | Disabled | Enabled | Enabled |
| L4X.R2W32X8D8S32.ADED | L4X.R2W32X8 | L4X.R2W32X8D8S32 | L4X.R2W32X8D8S32.ADED | LPDDR4X | 3200 | 1600 | 8 | 8 | 32 | 2 | 64 | 16 | A | Disabled | Enabled | Disabled |
| L4X.R2W32X8D8S32.ADEE | L4X.R2W32X8 | L4X.R2W32X8D8S32 | L4X.R2W32X8D8S32.ADEE | LPDDR4X | 3200 | 1600 | 8 | 8 | 32 | 2 | 64 | 16 | A | Disabled | Enabled | Enabled |
| L4X.R2W32X8D8S32.BDED | L4X.R2W32X8 | L4X.R2W32X8D8S32 | L4X.R2W32X8D8S32.BDED | LPDDR4X | 3200 | 1600 | 8 | 8 | 32 | 2 | 64 | 16 | B | Disabled | Enabled | Disabled |
| L4X.R2W32X8D8S32.BDEE | L4X.R2W32X8 | L4X.R2W32X8D8S32 | L4X.R2W32X8D8S32.BDEE | LPDDR4X | 3200 | 1600 | 8 | 8 | 32 | 2 | 64 | 16 | B | Disabled | Enabled | Enabled |
| L4X.R2W32X16D16S32.ADED | L4X.R2W32X16 | L4X.R2W32X16D16S32 | L4X.R2W32X16D16S32.ADED | LPDDR4X | 3200 | 1600 | 16 | 16 | 32 | 2 | 64 | 16 | A | Disabled | Enabled | Disabled |
| L4X.R2W32X16D16S32.ADEE | L4X.R2W32X16 | L4X.R2W32X16D16S32 | L4X.R2W32X16D16S32.ADEE | LPDDR4X | 3200 | 1600 | 16 | 16 | 32 | 2 | 64 | 16 | A | Disabled | Enabled | Enabled |
| L4X.R2W32X16D16S32.BDED | L4X.R2W32X16 | L4X.R2W32X16D16S32 | L4X.R2W32X16D16S32.BDED | LPDDR4X | 3200 | 1600 | 16 | 16 | 32 | 2 | 64 | 16 | B | Disabled | Enabled | Disabled |
| L4X.R2W32X16D16S32.BDEE | L4X.R2W32X16 | L4X.R2W32X16D16S32 | L4X.R2W32X16D16S32.BDEE | LPDDR4X | 3200 | 1600 | 16 | 16 | 32 | 2 | 64 | 16 | B | Disabled | Enabled | Enabled |
| L4X.R2W32X16D8S32.ADED | L4X.R2W32X16 | L4X.R2W32X16D8S32 | L4X.R2W32X16D8S32.ADED | LPDDR4X | 3200 | 1600 | 16 | 8 | 32 | 2 | 32 | 16 | A | Disabled | Enabled | Disabled |
| L4X.R2W32X16D8S32.ADEE | L4X.R2W32X16 | L4X.R2W32X16D8S32 | L4X.R2W32X16D8S32.ADEE | LPDDR4X | 3200 | 1600 | 16 | 8 | 32 | 2 | 32 | 16 | A | Disabled | Enabled | Enabled |
| L4X.R2W32X16D8S32.BDED | L4X.R2W32X16 | L4X.R2W32X16D8S32 | L4X.R2W32X16D8S32.BDED | LPDDR4X | 3200 | 1600 | 16 | 8 | 32 | 2 | 32 | 16 | B | Disabled | Enabled | Disabled |
| L4X.R2W32X16D8S32.BDEE | L4X.R2W32X16 | L4X.R2W32X16D8S32 | L4X.R2W32X16D8S32.BDEE | LPDDR4X | 3200 | 1600 | 16 | 8 | 32 | 2 | 32 | 16 | B | Disabled | Enabled | Enabled |
| L4X.R1W32X16D16S32.ADED | L4X.R1W32X16 | L4X.R1W32X16D16S32 | L4X.R1W32X16D16S32.ADED | LPDDR4X | 3200 | 1600 | 16 | 16 | 32 | 1 | 32 | 16 | A | Disabled | Enabled | Disabled |
| L4X.R1W32X16D16S32.ADEE | L4X.R1W32X16 | L4X.R1W32X16D16S32 | L4X.R1W32X16D16S32.ADEE | LPDDR4X | 3200 | 1600 | 16 | 16 | 32 | 1 | 32 | 16 | A | Disabled | Enabled | Enabled |
| L4X.R1W32X16D16S32.BDED | L4X.R1W32X16 | L4X.R1W32X16D16S32 | L4X.R1W32X16D16S32.BDED | LPDDR4X | 3200 | 1600 | 16 | 16 | 32 | 1 | 32 | 16 | B | Disabled | Enabled | Disabled |
| L4X.R1W32X16D16S32.BDEE | L4X.R1W32X16 | L4X.R1W32X16D16S32 | L4X.R1W32X16D16S32.BDEE | LPDDR4X | 3200 | 1600 | 16 | 16 | 32 | 1 | 32 | 16 | B | Disabled | Enabled | Enabled |
| L4X.R1W32X16D8S32.ADED | L4X.R1W32X16 | L4X.R1W32X16D8S32 | L4X.R1W32X16D8S32.ADED | LPDDR4X | 3200 | 1600 | 16 | 8 | 32 | 1 | 16 | 16 | A | Disabled | Enabled | Disabled |
| L4X.R1W32X16D8S32.ADEE | L4X.R1W32X16 | L4X.R1W32X16D8S32 | L4X.R1W32X16D8S32.ADEE | LPDDR4X | 3200 | 1600 | 16 | 8 | 32 | 1 | 16 | 16 | A | Disabled | Enabled | Enabled |
| L4X.R1W32X16D8S32.BDED | L4X.R1W32X16 | L4X.R1W32X16D8S32 | L4X.R1W32X16D8S32.BDED | LPDDR4X | 3200 | 1600 | 16 | 8 | 32 | 1 | 16 | 16 | B | Disabled | Enabled | Disabled |
| L4X.R1W32X16D8S32.BDEE | L4X.R1W32X16 | L4X.R1W32X16D8S32 | L4X.R1W32X16D8S32.BDEE | LPDDR4X | 3200 | 1600 | 16 | 8 | 32 | 1 | 16 | 16 | B | Disabled | Enabled | Enabled |

## [To]

**Change DMD settings to Enable only**

| ConfigName | ConfigGroup1 | ConfigGroup2 | ConfigGroup3 | DRAM | Speed [M | Frequenc | Die Width | Die densit | Width | Rank | Density [C | BL | WLS | RD-DBI | WR-DBI | DMD |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| L4.R2W32X16D16S32.ADED | L4.R2W32X16 | L4.R2W32X16D16S32 | L4.R2W32X16D16S32.ADED | LPDDR4 | 3200 | 1600 | 16 | 16 | 32 | 2 | 64 | 16 | A | Disabled | Enabled | Enabled |
| L4.R2W32X16D16S32.ADEE | L4.R2W32X16 | L4.R2W32X16D16S32 | L4.R2W32X16D16S32.ADEE | LPDDR4 | 3200 | 1600 | 16 | 16 | 32 | 2 | 64 | 16 | A | Disabled | Enabled | Enabled |
| L4.R2W32X16D16S32.BDED | L4.R2W32X16 | L4.R2W32X16D16S32 | L4.R2W32X16D16S32.BDED | LPDDR4 | 3200 | 1600 | 16 | 16 | 32 | 2 | 64 | 16 | B | Disabled | Enabled | Enabled |
| L4.R2W32X16D16S32.BDEE | L4.R2W32X16 | L4.R2W32X16D16S32 | L4.R2W32X16D16S32.BDEE | LPDDR4 | 3200 | 1600 | 16 | 16 | 32 | 2 | 64 | 16 | B | Disabled | Enabled | Enabled |
| L4.R2W32X16D8S32.ADED | L4.R2W32X16 | L4.R2W32X16D8S32 | L4.R2W32X16D8S32.ADED | LPDDR4 | 3200 | 1600 | 16 | 8 | 32 | 2 | 32 | 16 | A | Disabled | Enabled | Enabled |
| L4.R2W32X16D8S32.ADEE | L4.R2W32X16 | L4.R2W32X16D8S32 | L4.R2W32X16D8S32.ADEE | LPDDR4 | 3200 | 1600 | 16 | 8 | 32 | 2 | 32 | 16 | A | Disabled | Enabled | Enabled |
| L4.R2W32X16D8S32.BDED | L4.R2W32X16 | L4.R2W32X16D8S32 | L4.R2W32X16D8S32.BDED | LPDDR4 | 3200 | 1600 | 16 | 8 | 32 | 2 | 32 | 16 | B | Disabled | Enabled | Enabled |
| L4.R2W32X16D8S32.BDEE | L4.R2W32X16 | L4.R2W32X16D8S32 | L4.R2W32X16D8S32.BDEE | LPDDR4 | 3200 | 1600 | 16 | 8 | 32 | 2 | 32 | 16 | B | Disabled | Enabled | Enabled |
| L4.R1W32X16D16S32.ADED | L4.R1W32X16 | L4.R1W32X16D16S32 | L4.R1W32X16D16S32.ADED | LPDDR4 | 3200 | 1600 | 16 | 16 | 32 | 1 | 32 | 16 | A | Disabled | Enabled | Enabled |
| L4.R1W32X16D16S32.ADEE | L4.R1W32X16 | L4.R1W32X16D16S32 | L4.R1W32X16D16S32.ADEE | LPDDR4 | 3200 | 1600 | 16 | 16 | 32 | 1 | 32 | 16 | A | Disabled | Enabled | Enabled |
| L4.R1W32X16D16S32.BDED | L4.R1W32X16 | L4.R1W32X16D16S32 | L4.R1W32X16D16S32.BDED | LPDDR4 | 3200 | 1600 | 16 | 16 | 32 | 1 | 32 | 16 | B | Disabled | Enabled | Enabled |
| L4.R1W32X16D16S32.BDEE | L4.R1W32X16 | L4.R1W32X16D16S32 | L4.R1W32X16D16S32.BDEE | LPDDR4 | 3200 | 1600 | 16 | 16 | 32 | 1 | 32 | 16 | B | Disabled | Enabled | Enabled |
| L4.R1W32X16D8S32.ADED | L4.R1W32X16 | L4.R1W32X16D8S32 | L4.R1W32X16D8S32.ADED | LPDDR4 | 3200 | 1600 | 16 | 8 | 32 | 1 | 16 | 16 | A | Disabled | Enabled | Enabled |
| L4.R1W32X16D8S32.ADEE | L4.R1W32X16 | L4.R1W32X16D8S32 | L4.R1W32X16D8S32.ADEE | LPDDR4 | 3200 | 1600 | 16 | 8 | 32 | 1 | 16 | 16 | A | Disabled | Enabled | Enabled |
| L4.R1W32X16D8S32.BDED | L4.R1W32X16 | L4.R1W32X16D8S32 | L4.R1W32X16D8S32.BDED | LPDDR4 | 3200 | 1600 | 16 | 8 | 32 | 1 | 16 | 16 | B | Disabled | Enabled | Enabled |
| L4.R1W32X16D8S32.BDEE | L4.R1W32X16 | L4.R1W32X16D8S32 | L4.R1W32X16D8S32.BDEE | LPDDR4 | 3200 | 1600 | 16 | 8 | 32 | 1 | 16 | 16 | B | Disabled | Enabled | Enabled |
| L4X.R2W32X8D8S32.ADED | L4X.R2W32X8 | L4X.R2W32X8D8S32 | L4X.R2W32X8D8S32.ADED | LPDDR4X | 3200 | 1600 | 8 | 8 | 32 | 2 | 64 | 16 | A | Disabled | Enabled | Enabled |
| L4X.R2W32X8D8S32.ADEE | L4X.R2W32X8 | L4X.R2W32X8D8S32 | L4X.R2W32X8D8S32.ADEE | LPDDR4X | 3200 | 1600 | 8 | 8 | 32 | 2 | 64 | 16 | A | Disabled | Enabled | Enabled |
| L4X.R2W32X8D8S32.BDED | L4X.R2W32X8 | L4X.R2W32X8D8S32 | L4X.R2W32X8D8S32.BDED | LPDDR4X | 3200 | 1600 | 8 | 8 | 32 | 2 | 64 | 16 | B | Disabled | Enabled | Enabled |
| L4X.R2W32X8D8S32.BDEE | L4X.R2W32X8 | L4X.R2W32X8D8S32 | L4X.R2W32X8D8S32.BDEE | LPDDR4X | 3200 | 1600 | 8 | 8 | 32 | 2 | 64 | 16 | B | Disabled | Enabled | Enabled |
| L4X.R2W32X16D16S32.ADED | L4X.R2W32X16 | L4X.R2W32X16D16S32 | L4X.R2W32X16D16S32.ADED | LPDDR4X | 3200 | 1600 | 16 | 16 | 32 | 2 | 64 | 16 | A | Disabled | Enabled | Enabled |
| L4X.R2W32X16D16S32.ADEE | L4X.R2W32X16 | L4X.R2W32X16D16S32 | L4X.R2W32X16D16S32.ADEE | LPDDR4X | 3200 | 1600 | 16 | 16 | 32 | 2 | 64 | 16 | A | Disabled | Enabled | Enabled |
| L4X.R2W32X16D16S32.BDED | L4X.R2W32X16 | L4X.R2W32X16D16S32 | L4X.R2W32X16D16S32.BDED | LPDDR4X | 3200 | 1600 | 16 | 16 | 32 | 2 | 64 | 16 | B | Disabled | Enabled | Enabled |
| L4X.R2W32X16D16S32.BDEE | L4X.R2W32X16 | L4X.R2W32X16D16S32 | L4X.R2W32X16D16S32.BDEE | LPDDR4X | 3200 | 1600 | 16 | 16 | 32 | 2 | 64 | 16 | B | Disabled | Enabled | Enabled |
| L4X.R2W32X16D8S32.ADED | L4X.R2W32X16 | L4X.R2W32X16D8S32 | L4X.R2W32X16D8S32.ADED | LPDDR4X | 3200 | 1600 | 16 | 8 | 32 | 2 | 32 | 16 | A | Disabled | Enabled | Enabled |
| L4X.R2W32X16D8S32.ADEE | L4X.R2W32X16 | L4X.R2W32X16D8S32 | L4X.R2W32X16D8S32.ADEE | LPDDR4X | 3200 | 1600 | 16 | 8 | 32 | 2 | 32 | 16 | A | Disabled | Enabled | Enabled |
| L4X.R2W32X16D8S32.BDED | L4X.R2W32X16 | L4X.R2W32X16D8S32 | L4X.R2W32X16D8S32.BDED | LPDDR4X | 3200 | 1600 | 16 | 8 | 32 | 2 | 32 | 16 | B | Disabled | Enabled | Enabled |
| L4X.R2W32X16D8S32.BDEE | L4X.R2W32X16 | L4X.R2W32X16D8S32 | L4X.R2W32X16D8S32.BDEE | LPDDR4X | 3200 | 1600 | 16 | 8 | 32 | 2 | 32 | 16 | B | Disabled | Enabled | Enabled |
| L4X.R1W32X16D16S32.ADED | L4X.R1W32X16 | L4X.R1W32X16D16S32 | L4X.R1W32X16D16S32.ADED | LPDDR4X | 3200 | 1600 | 16 | 16 | 32 | 1 | 32 | 16 | A | Disabled | Enabled | Enabled |
| L4X.R1W32X16D16S32.ADEE | L4X.R1W32X16 | L4X.R1W32X16D16S32 | L4X.R1W32X16D16S32.ADEE | LPDDR4X | 3200 | 1600 | 16 | 16 | 32 | 1 | 32 | 16 | A | Disabled | Enabled | Enabled |
| L4X.R1W32X16D16S32.BDED | L4X.R1W32X16 | L4X.R1W32X16D16S32 | L4X.R1W32X16D16S32.BDED | LPDDR4X | 3200 | 1600 | 16 | 16 | 32 | 1 | 32 | 16 | B | Disabled | Enabled | Enabled |
| L4X.R1W32X16D16S32.BDEE | L4X.R1W32X16 | L4X.R1W32X16D16S32 | L4X.R1W32X16D16S32.BDEE | LPDDR4X | 3200 | 1600 | 16 | 16 | 32 | 1 | 32 | 16 | B | Disabled | Enabled | Enabled |
| L4X.R1W32X16D8S32.ADED | L4X.R1W32X16 | L4X.R1W32X16D8S32 | L4X.R1W32X16D8S32.ADED | LPDDR4X | 3200 | 1600 | 16 | 8 | 32 | 1 | 16 | 16 | A | Disabled | Enabled | Enabled |
| L4X.R1W32X16D8S32.ADEE | L4X.R1W32X16 | L4X.R1W32X16D8S32 | L4X.R1W32X16D8S32.ADEE | LPDDR4X | 3200 | 1600 | 16 | 8 | 32 | 1 | 16 | 16 | A | Disabled | Enabled | Enabled |
| L4X.R1W32X16D8S32.BDED | L4X.R1W32X16 | L4X.R1W32X16D8S32 | L4X.R1W32X16D8S32.BDED | LPDDR4X | 3200 | 1600 | 16 | 8 | 32 | 1 | 16 | 16 | B | Disabled | Enabled | Enabled |
| L4X.R1W32X16D8S32.BDEE | L4X.R1W32X16 | L4X.R1W32X16D8S32 | L4X.R1W32X16D8S32.BDEE | LPDDR4X | 3200 | 1600 | 16 | 8 | 32 | 1 | 16 | 16 | B | Disabled | Enabled | Enabled |

# RZ/V2H DDRTOP Application Note
# 02_GenTool sheet

## [Form]

Appendix A) Example of a configuration file

For LPDDR4X (example/rzv2h_ddrparam_config_example_lpddr4x_2rank.txt)

```
//Configuration
ConfigName          = L4X.R2W32X16D16S32.ADED

//Mode switch
ModeECC             = 0     // 0=Disabled Inline-ECC, 1=Enabled Inline-ECC
ModeTrain           = 0     // 0=Train, 1=DevInit, 2=SkipTrain, 3=Train1d
ModeSim             = 0     // 0=Disabled RTL Sim mode (for silicon), 1=Enabled RTL Sim mode
```

See sheet "01_DRAM", and set ConfigName.

Select whether to use the Inline-ECC feature.

Select the training mode. For detail, see sheet "00_TrainingMode".

Select whether to use the RTL Sim mode. For detail, see sheet "00_TrainingMode".

## [To]

Appendix A) Example of a configuration file

For LPDDR4X (example/rzv2h_ddrparam_config_example_lpddr4x_2rank.txt)

```
// Configuration
ConfigName          = L4X.R2W32X16D16S32.ADEE

// Mode switch
ModeECC             = 0     // 0=Disabled Inline-ECC, 1=Enabled Inline-ECC
ModeTrain           = 0     // 0=Train, 1=DevInit, 2=SkipTrain, 3=Train1d
ModeSim             = 0     // 0=Disabled RTL Sim mode (for silicon), 1=Enabled RTL Sim mode
```

See sheet "01_DRAM", and set ConfigName.

Select whether to use the Inline-ECC feature.
Note) This function is supported by the devices other than "#AC0" and "BC#0". "#AC0" and "#BC0" do not support it.

Select the training mode. For detail, see sheet "00_TrainingMode".

Select whether to use the RTL Sim mode. For detail, see sheet "00_TrainingMode".