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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0125A/E	Rev.	1.00
Title	RZ/G2H, G2M V1.3, G2M V3.0, G2N and G2E Addition of section 22.IPMMU		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E	Lot No. All lots	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.11 (R01UH0808EJ0111)		

This technical update describes document correction of RZ/G Series, 2nd Generation product.

[Summary]

Addition of section about the restriction same as written in DMAC chapter

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZ/G2H

RZ/G2M V1.3, V3.0

RZ/G2N

RZ/G2E

[Section number and title]

Section 22. IPMMU

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. Section 22. IPMMU, Page 22-69, 22.5.3.14 Restriction for DMAC address range is added..

Current (from):

22.5.3.13 Restriction for PMB

In order to perform address translation by IPMMU normally, it is limited not to use PMB mode in secure mode. Use PMB mode only in non-secure mode.

Correct (to):

22.5.3.13 Restriction for PMB

In order to perform address translation by IPMMU normally, it is limited not to use PMB mode in secure mode. Use PMB mode only in non-secure mode.

22.5.3.14 Restriction for DMAC address range

SYS -DMAC and Audio-DMAC usage is restricted to 32bit address range in case IPMMU is used.

These restrictions are also described as below chapters of register description.

[SYS-DMAC]

23.2.28 DMA Fixed Source Address Registers 0 to 47 (DMAFIXSAR_0 to DMAFIXSAR_47)

23.2.29 DMA Fixed Destination Address Registers 0 to 47 (DMAFIXDAR_0 to DMAFIXDAR_47

23.2.30 DMA Fixed Descriptor Base Address Registers 0 to 47 (DMAFIXDPBASE_0 to DMAFIXDPBASE_47)

[Audio-DMAC]

44.2.23 DMA Fixed Source Address Registers 0 to 31 (DMAFIXSAR_0 to DMAFIXSAR_31)

44.2.24 DMA Fixed Destination Address Registers 0 to 31 (DMAFIXDAR_0 to DMAFIXDAR_31)

44.2.25 DMA Fixed Descriptor Base Address Registers 0 to 31 (DMAFIXDPBASE_0 to DMAFIXDPBASE_31)

[Description]

Add restrictions for DMAC usage written in DMAC chapter.

[Reason for Correction]

To inform this usage notes also in IPMMU chapter.

- End of Document -