Date: Jul. 14, 2017

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A082A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G10 Descriptions in the Hardware User's Manual Rev. 3.11 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G10 R5F10Yxxx	Lot No. All lots	Reference Document	RL78/G10 User's Manual: Hardware Rev.3.11 R01UH0384EJ0311 (Dec. 2016)		

This document describes misstatements found in the RL78/G10 User's Manual: Hardware Rev.3.11 (R01UH0384EJ0311).

Corrections

Applicable Item	Applicable Page	Contents
4.5.3 Example of register settings for port and alternate functions used Table4-5. Examples of Register And Output Latch Setting With Pin Functions (2/4)	Page 71	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
		Document No.	English	R01UH0384EJ0311
1	4.5.3 Example of register settings for port and alternate functions used Table4-5. Examples of Register And Output Latch Setting With Pin Functions (2/4)		Page 71	Page2

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/G10 User's Manual: Hardware Rev.3.11 Correction for Incorrect Description Notice

Document Number	Date	Description
TN-RL*-A082A/E	Jul. 14, 2017	First edition issued No.1 in corrections (This notice)

1. **4.5.3 Example of register settings for port and alternate functions used**

Table 4-5. Examples of Register And Output Latch Settings With Pin Functions (2/4) (p.71)

Incorrect)

Table 4-5. Examples of Register And Output Latch Settings With Pin Functions (2/4)

Pin	Function		Omitted	Pm	Alternate function output		16pins	10pins
	Name	I/O			SAU output function	Non-SAU		
Omitted								
P06	Omitted		Omitted	Omitted				
	SCLA0	I/O		**1**	—	×	✓	—
	Omitted			Omitted				
P07	Omitted			Omitted				
	SDAA0	I/O		**1**	SCK01=1	TO03=0	✓	—
Omitted								

Correct)

Table 4-5. Examples of Register And Output Latch Settings With Pin Functions (2/4)

Pin	Function		Omitted	Pm	Alternate function output		16pins	10pins
	Name	I/O			SAU output function	Non-SAU		
Omitted								
P06	Omitted		Omitted	Omitted				
	SCLA0	I/O		0	—	×	✓	—
	Omitted			Omitted				
P07	Omitted			Omitted				
	SDAA0	I/O		0	SCK01=1	TO03=0	✓	—
Omitted								