

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RH8-B0571A/E	Rev.	1.00
Title	RH850/U2Cx DNF Pulse width description		Information Category	Technical Notification		
Applicable Product	RH850/U2C8-EVA, U2C8, U2C4, U2C2	Lot No.	Reference Document	R01UH1018EJ0100 (User's Manual: Hardware)		
		All lot				

[Overview]

The description of the pulse width calculation formula of the DNF (digital noise filter) is incorrect.

[Change point]

The following description will be changed in User's Manual (**Red** character)

Section 2 Pin Function

2.7.2.2 Digital Filters (1) Digital Filter Characteristic

<Before>

External signal pulses shorter than the following are always suppressed.

$$s \times 1/f_s$$

External signal pulses longer than the following are always judged as valid and are passed on to the filter output.

$$(s + 1) \times 1/f_s$$

External signal pulses in the following range may be suppressed or judged as valid.

$$s \times 1/f_s \text{ to } (s + 1) \times 1/f_s$$

<After>

External signal pulses shorter than the following are always suppressed.

$$(s - 1) \times 1/f_s$$

External signal pulses longer than the following are always judged as valid and are passed on to the filter output.

$$s \times 1/f_s$$

External signal pulses in the following range may be suppressed or judged as valid.

$$(s - 1) \times 1/f_s \text{ to } s \times 1/f_s$$

Section 57 Electrical Characteristics

57.3.7.2 Interrupt, Wake-up and Error Input Timing

Table 57.45 Interrupt Timing

<Before>

Table 57.45 Interrupt Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
NMI input high level width	t _{WNIH}	*3	600			ns
		*4	150			μs
NMI input low level width	t _{WNIL}	*3	600			ns
		*4	150			μs
NMI pulse rejection width*2	t _{WNIRJ}		100		600	ns
IRQn input high level width	t _{WITH}	*3	600			ns
		*4	150			μs
IRQn input low level width	t _{WITL}	*3	600			ns
		*4	150			μs
INTPn pulse rejection width*2	t _{WIRJ}		100		600	ns
RLIN3nRX wake-up input high level width	t _{WRLINH}		(S + 1) × 1/fs*1			ns
RLIN3nRX wake-up input low level width	t _{WRLINL}		(S + 1) × 1/fs*1			ns
RLIN3nRX wake-up pulse rejection width*2	t _{WRLINRJ}		(S - 1) × 1/fs*1		(S + 1) × 1/fs*1	ns
CANnRX wake-up input high level width	t _{WCANH}		(S + 1) × 1/fs*1			ns
CANnRX wake-up input low level width	t _{WCANL}		(S + 1) × 1/fs*1			ns
CANnRX wake-up pulse rejection width*2	t _{WCANRJ}		(S - 1) × 1/fs*1		(S + 1) × 1/fs*1	ns
FLXnRXDA wake-up input high level width	t _{WFLXH}		(S + 1) × 1/fs*1			ns
FLXnRXDA wake-up input low level width	t _{WFLXL}		(S + 1) × 1/fs*1			ns
FLXnRXDA wake-up pulse rejection width*2	t _{WFLXRJ}		(S - 1) × 1/fs*1		(S + 1) × 1/fs*1	ns
ERRORINn wake-up input high level width	t _{WERRH}		(S + 1) × 1/fs*1			ns
ERRORINn wake-up input low level width	t _{WERRL}		(S + 1) × 1/fs*1			ns
ERRORINn wake-up pulse rejection width*2	t _{WERRRJ}		(S - 1) × 1/fs*1		(S + 1) × 1/fs*1	ns

Note 1. S: Number of sampling times
fs: The value given by following formula

$$f_s = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLK_LSB
PRS: 1, 2, 4, 8, ... , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

Note 3. Edge Detection or Level Detection (CLKA_LPS is operated by CLK_HSIOOSC/20)

Note 4. Level Detection (CLKA_LPS is operated by CLK_LSIOOSC)

<After>

Table 57.45 Interrupt Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
NMI input high level width	t _{WNIH}	*3	600			ns
		*4	150			μs
NMI input low level width	t _{WNIL}	*3	600			ns
		*4	150			μs
NMI pulse rejection width*2	t _{WNIRJ}		100		600	ns
IRQn input high level width	t _{WITH}	*3	600			ns
		*4	150			μs
IRQn input low level width	t _{WITL}	*3	600			ns
		*4	150			μs
INTPn pulse rejection width*2	t _{WIRJ}		100		600	ns
RLIN3nRX wake-up input high level width	t _{WRLINH}		$S \times 1/fs^{*1}$			ns
RLIN3nRX wake-up input low level width	t _{WRLINL}		$S \times 1/fs^{*1}$			ns
RLIN3nRX wake-up pulse rejection width*2	t _{WRLINRJ}		$(S - 1) \times 1/fs^{*1}$		$S \times 1/fs^{*1}$	ns
CANnRX wake-up input high level width	t _{WCANH}		$S \times 1/fs^{*1}$			ns
CANnRX wake-up input low level width	t _{WCANL}		$S \times 1/fs^{*1}$			ns
CANnRX wake-up pulse rejection width*2	t _{WCANRJ}		$(S - 1) \times 1/fs^{*1}$		$S \times 1/fs^{*1}$	ns
FLXnRXDA wake-up input high level width	t _{WFLXH}		$S \times 1/fs^{*1}$			ns
FLXnRXDA wake-up input low level width	t _{WFLXL}		$S \times 1/fs^{*1}$			ns
FLXnRXDA wake-up pulse rejection width*2	t _{WFLXRJ}		$(S - 1) \times 1/fs^{*1}$		$S \times 1/fs^{*1}$	ns
ERRORINn wake-up input high level width	t _{WERRH}		$S \times 1/fs^{*1}$			ns
ERRORINn wake-up input low level width	t _{WERL}		$S \times 1/fs^{*1}$			ns
ERRORINn wake-up pulse rejection width*2	t _{WERRRJ}		$(S - 1) \times 1/fs^{*1}$		$S \times 1/fs^{*1}$	ns

Note 1. S: Number of sampling times
fs: The value given by following formula

$$f_s = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLK_LSB
PRS: 1, 2, 4, 8, ... , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

Note 3. Edge Detection or Level Detection (CLKA_LPS is operated by CLK_HSIOSC/20)

Note 4. Level Detection (CLKA_LPS is operated by CLK_LSIOSC)

57.3.7.4 ADTRG Timing

Table 57.47 ADCKnTRGm Timing

<Before>

Table 57.47 ADCKnTRGm Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ADCKnTRGm input high level width	t _{WADH}		(S + 1) × 1/fs* ¹			ns
ADCKnTRGm input low level width	t _{WADL}		(S + 1) × 1/fs* ¹			ns
ADCKnTRGm pulse rejection width* ²	t _{WADRJ}		(S - 1) × 1/fs* ¹		(S + 1) × 1/fs* ¹	ns

Note 1. S: Number of sampling times
 fs: The value given by the following formula

$$f_s = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLKC_HSB, CLKA_ADC
 PRS: 1, 2, 4, 8, ... , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

<After>

Table 57.47 ADCKnTRGm Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ADCKnTRGm input high level width	t _{WADH}		S × 1/fs* ¹			ns
ADCKnTRGm input low level width	t _{WADL}		S × 1/fs* ¹			ns
ADCKnTRGm pulse rejection width* ²	t _{WADRJ}		(S - 1) × 1/fs* ¹		S × 1/fs* ¹	ns

Note 1. S: Number of sampling times
 fs: The value given by the following formula

$$f_s = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLKC_HSB, CLKA_ADC
 PRS: 1, 2, 4, 8, ... , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

57.3.7.5 Communication Signal Timing

Table 57.48 Control Signal

<Before>

Table 57.48 Control Signal

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SENTnRX input high level width	t _{WSENTIH}	Analog filter	600			ns
		Digital filter	$(S + 1) \times 1/fs^{*1}$			ns
SENTnRX input low level width	t _{WSENTIL}	Analog filter	600			ns
		Digital filter	$(S + 1) \times 1/fs^{*1}$			ns
SENTnRX pulse rejection width*2	t _{WSENTIRJ}	Analog filter	100		600	ns
		Digital filter	$(S - 1) \times 1/fs^{*1}$		$(S + 1) \times 1/fs^{*1}$	ns
PSI5nRX input high level width	t _{WPSI5IH}	Analog filter	600			ns
		Digital filter	$(S + 1) \times 1/fs^{*1}$			ns
PSI5nRX input low level width	t _{WPSI5IL}	Analog filter	600			ns
		Digital filter	$(S + 1) \times 1/fs^{*1}$			ns
PSI5nRX pulse rejection width*2	t _{WPSI5IRJ}	Analog filter	100		600	ns
		Digital filter	$(S - 1) \times 1/fs^{*1}$		$(S + 1) \times 1/fs^{*1}$	ns
SSIFn related terminals input high level width*3			$(S + 1) \times 1/fs^{*1}$			ns
SSIFn related terminals input low level width*3			$(S + 1) \times 1/fs^{*1}$			ns
SSIFn related terminals pulse rejection width*2*3			$(S - 1) \times 1/fs^{*1}$		$(S + 1) \times 1/fs^{*1}$	ns

Note 1. S: Number of sampling times
 fs: The value given by the following formula

$$f_s = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLKC_HSB (for SENTnRX and PSI5nRX)
 frequency of CLK_LSB (for RHSBnEMRG)
 PRS: 1, 2, 4, 8, ... , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

Note 3. The following shows the SSIF related terminals.
 SSIFnSCK, SSIFnWS, SSIFnRXD, SSIFACK

<After>

Table 57.48 Control Signal

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SENTnRX input high level width	t _{WSENTIH}	Analog filter	600			ns
		Digital filter	S × 1/fs ^{*1}			ns
SENTnRX input low level width	t _{WSENTIL}	Analog filter	600			ns
		Digital filter	S × 1/fs ^{*1}			ns
SENTnRX pulse rejection width ^{*2}	t _{WSENTIRJ}	Analog filter	100		600	ns
		Digital filter	(S - 1) × 1/fs ^{*1}		S × 1/fs ^{*1}	ns
PSI5nRX input high level width	t _{WPSI5IH}	Analog filter	600			ns
		Digital filter	S × 1/fs ^{*1}			ns
PSI5nRX input low level width	t _{WPSI5IL}	Analog filter	600			ns
		Digital filter	S × 1/fs ^{*1}			ns
PSI5nRX pulse rejection width ^{*2}	t _{WPSI5IRJ}	Analog filter	100		600	ns
		Digital filter	(S - 1) × 1/fs ^{*1}		S × 1/fs ^{*1}	ns
SSIFn related terminals input high level width ^{*3}			S × 1/fs ^{*1}			ns
SSIFn related terminals input low level width ^{*3}			S × 1/fs ^{*1}			ns
SSIFn related terminals pulse rejection width ^{*2,*3}			(S - 1) × 1/fs ^{*1}		S × 1/fs ^{*1}	ns

Note 1. S: Number of sampling times
 fs: The value given by the following formula

$$f_s = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLKC_HSB (for SENTnRX and PSI5nRX)
 frequency of CLK_LSB (for RHBnEMRG)
 PRS: 1, 2, 4, 8, ... , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

Note 3. The following shows the SSIF related terminals.
 SSIFnSCK, SSIFnWS, SSIFnRXD, SSIFACK

57.3.25 Timer Timing

Table 57.93 Timer Input Timing

<Before>

Table 57.93 Timer Input Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TAUDnIm input high level width	t_{WTDIH}		$(S + 1) \times 1/fs^{*1}$			ns
TAUDnIm input low level width	t_{WTDIL}		$(S + 1) \times 1/fs^{*1}$			ns
TAUDnIm pulse rejection width ^{*2}	t_{WTDJRJ}		$(S - 1) \times 1/fs^{*1}$		$(S + 1) \times 1/fs^{*1}$	ns
TAUJnIm input high level width	t_{WTJIH}	Analog noise filter	600^{*3}			ns
		Digital noise filter	$(S + 1) \times 1/fs^{*1}$			ns
TAUJnIm input low level width	t_{WTJIL}	Analog noise filter	600^{*3}			ns
		Digital noise filter	$(S + 1) \times 1/fs^{*1}$			ns
TAUJnIm pulse rejection width ^{*2}	t_{WTJRJ}	Analog noise filter	100		600^{*3}	ns
		Digital noise filter	$(S - 1) \times 1/fs^{*1}$		$(S + 1) \times 1/fs^{*1}$	ns
TAPAnESO input high level width ^{*4}	t_{WTPIH}	Analog noise filter	600			ns
		Digital noise filter	$(S + 1) \times 1/fs^{*1}$			ns
TAPAnESO input low level width ^{*4}	t_{WTPIL}	Analog noise filter	600			ns
		Digital noise filter	$(S + 1) \times 1/fs^{*1}$			ns
TAPAnESO pulse rejection width ^{*2, *4}	t_{WTPRJ}	Analog noise filter	100		600	ns
		Digital noise filter	$(S - 1) \times 1/fs^{*1}$		$(S + 1) \times 1/fs^{*1}$	ns
ENCAnTINm input high level width	t_{WENIH}		$(S + 1) \times 1/fs^{*1}$			ns
ENCAnTINm input low level width	t_{WENIL}		$(S + 1) \times 1/fs^{*1}$			ns
ENCAnTINm pulse rejection width ^{*2}	t_{WENRJ}		$(S - 1) \times 1/fs^{*1}$		$(S + 1) \times 1/fs^{*1}$	ns
TSG3nPTSI/ENCAnEx, TSG3nCLKI high level width	t_{WTGIH}		$(S + 1) \times 1/fs^{*1}$			ns
TSG3nPTSI/ENCAnEx, TSG3nCLKI low level width	t_{WTGIL}		$(S + 1) \times 1/fs^{*1}$			ns
TSG3nPTSI/ENCAnEx, TSG3nCLKI pulse rejection width ^{*2}	t_{WTGRJ}		$(S - 1) \times 1/fs^{*1}$		$(S + 1) \times 1/fs^{*1}$	ns

Note 1. S: Number of sampling times
fs: The value given by the following formula

$$fs = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK} : frequency of CLKA_TAUJ (for TAUJ2 and TAUJ3), CLKC_HSB (others)
PRS: 1, 2, 4, 8, ..., 128

Note 2. Input pulse shorter than the given min. value will be filtered out. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered or not).

This characteristic is not tested in production.

Note 3. When CLK_LSOSC is selected by CKS_ATAUJC register, at least one clock period of CLK_LSOSC (4.6 μs) is required for activation of input signal for that domain. Any input pulses with less than 4.6 μs width may be rejected.

Note 4. By-pass of filter is possible. For detail, see Section 2.7.2.11, ANF/DNF Type F1.

<After>

Table 57.93 Timer Input Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TAUDnIm input high level width	t _{WTDIH}		S × 1/fs ⁺¹			ns
TAUDnIm input low level width	t _{WTDIL}		S × 1/fs ⁺¹			ns
TAUDnIm pulse rejection width ^{*2}	t _{WDRJ}		(S - 1) × 1/fs ⁺¹		S × 1/fs ⁺¹	ns
TAUJnIm input high level width	t _{WTJIH}	Analog noise filter	600 ^{*3}			ns
		Digital noise filter	S × 1/fs ⁺¹			ns
TAUJnIm input low level width	t _{WTJIL}	Analog noise filter	600 ^{*3}			ns
		Digital noise filter	S × 1/fs ⁺¹			ns
TAUJnIm pulse rejection width ^{*2}	t _{WTJRJ}	Analog noise filter	100		600 ^{*3}	ns
		Digital noise filter	(S - 1) × 1/fs ⁺¹		S × 1/fs ⁺¹	ns
TAPAnESO input high level width ^{*4}	t _{WTPIH}	Analog noise filter	600			ns
		Digital noise filter	S × 1/fs ⁺¹			ns
TAPAnESO input low level width ^{*4}	t _{WTPIL}	Analog noise filter	600			ns
		Digital noise filter	S × 1/fs ⁺¹			ns
TAPAnESO pulse rejection width ^{*2, *4}	t _{WTPRJ}	Analog noise filter	100		600	ns
		Digital noise filter	(S - 1) × 1/fs ⁺¹		S × 1/fs ⁺¹	ns
ENCAnTINm input high level width	t _{WENIH}		S × 1/fs ⁺¹			ns
ENCAnTINm input low level width	t _{WENIL}		S × 1/fs ⁺¹			ns
ENCAnTINm pulse rejection width ^{*2}	t _{WENRJ}		(S - 1) × 1/fs ⁺¹		S × 1/fs ⁺¹	ns
TSG3nPTSI _m /ENCAnEx, TSG3nCLKI high level width	t _{WTGIH}		S × 1/fs ⁺¹			ns
TSG3nPTSI _m /ENCAnEx, TSG3nCLKI low level width	t _{WTGIL}		S × 1/fs ⁺¹			ns
TSG3nPTSI _m /ENCAnEx, TSG3nCLKI pulse rejection width ^{*2}	t _{WTGRJ}		(S - 1) × 1/fs ⁺¹		S × 1/fs ⁺¹	ns

Note 1. S: Number of sampling times
fs: The value given by the following formula

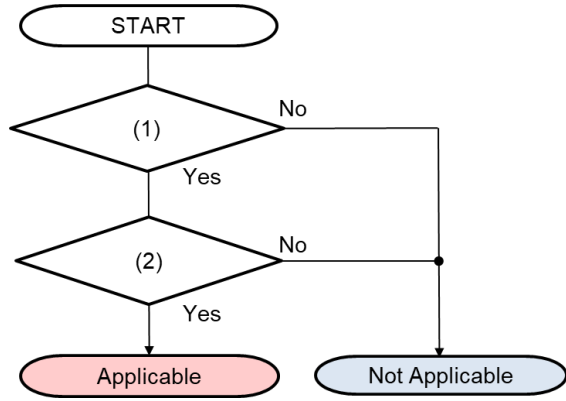
$$f_s = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLKA_TAUJ (for TAUJ2 and TAUJ3), CLKC_HSB (others)
PRS: 1, 2, 4, 8, ..., 128

- Note 2. Input pulse shorter than the given min. value will be filtered out. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered or not). This characteristic is not tested in production.
- Note 3. When CLK_LSOSC is selected by CKS_ATAUJC register, at least one clock period of CLK_LSOSC (4.6 μs) is required for activation of input signal for that domain. Any input pulses with less than 4.6 μs width may be rejected.
- Note 4. By-pass of filter is possible. For detail, see Section 2.7.2.11, ANF/DNF Type F1.

[Judgement Flow]

(1)	Is the DNF used?
(2)	Does the calculation of suppressed pulse width and passed pulse width using the formula?



END