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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A0291A/E	Rev.	1.00
Title	Point to Note on Using the Next-Access Delay Function of the Quad Serial Peripheral Interface (QSPI)		Information Category	Technical Notification		
Applicable Product	RX64M Group, RX65N Group, RX651 Group, RX66N Group, RX71M Group, RX72M Group, RX72N Group	Lot No. All	Reference Document	User's Manual: Hardware for applicable products listed under Reference Documents on the next page		

This document describes a point to note on using the next-access delay function of the quad serial peripheral interface (QSPI) in the applicable products listed above.

1. Point to Note

Setting the SPCR.SPE bit to 0 (disables the SPI function) does not initialize the internal state machine for the next-access delay function. Consequently, the first next-access delay period after the SPE bit has been set to 1 (enables the SPI function) may be shorter than the period set in the SPND.SPNDL[2:0] bits.

2. Countermeasures

2.1 In Single-SPI Mode, or after a Write Operation in Dual-/Quad-SPI Mode

When the next-access delay function is in use, set the SPE bit to 0 after all data have been transmitted. The completion of transmission can be confirmed by checking that all of the following conditions are met.

- The SPBDCR.TXBS[5:0] bits are 000000b (no data in the transmit buffer).
- The SPSR.TREND flag is 1 (transmission is completed).
- The SPSR.SPSSLF flag is 1 (the QSSL pin is negated).

2.2 After a Read Operation in Dual-/Quad-SPI Mode

The only way to finish a read operation is to set the SPE bit to 0. After having set the SPE bit to 0, proceed with two rounds of dummy transmission with the pins to be used placed at the inactive level to initialize the internal state machine. The procedure is as follows.

(1) Read the PIDR registers of the corresponding ports to obtain the levels on the QSSL and QSPCLK pins and set the results in the corresponding PODR registers to make both the QSSL and QSPCLK pins inactive.

(2) Write 0 to the bits in the PODR registers of the ports corresponding to the QIO0 to QIO3 pins.

(3) In Dual-SPI mode, switch the QSSL, QSPCLK, QIO0, and QIO1 pins to general output port pins. In Quad-SPI mode, switch the QSSL, QSPCLK, and QIO0 to QIO3 pins to general output port pins.

(4) Configure the QSPI for repeating 8-bit write operations twice; this is implemented by making the SPCMD0 and other register settings listed below.

- SPCMD0.SPNDEN = 1 (the next-access delay function is enabled), SPCMD0.SPB[3:0] = 0000b (8-bit transfer), SPCMD0.SSLKP = 0 (the QSSL signal is negated every time a transfer is completed), SPCMD0.SPRW = 0 (write

operation)

- SPBMUL0 = 00000002h (the number of transfers is 2)
- SPSCR = 00h (only SPCMD0 is used for reference)

(5) Set the SPE bit to 1 and then write a one-byte dummy value to the SPDR register twice.

(6) Wait until the two rounds of dummy transmission have been completed (that is, wait until the following conditions have been met).

- The SPBDCR.TXBS[5:0] bits are 000000b (no data in the transmit buffer).
- The SPSR.TREND flag is 1 (transmission is completed).
- The SPSR.SPSSLF flag is 1 (the QSSL pin is negated).

(7) Clear the SPSR.SPTEF and SPSR.SPSSLF flags and then set the SPE bit to 0.

(8) Set the bits in the PMR registers corresponding to the pins to be switched from operation as general output port pins to 1 (peripheral module (QSPI)).

3. Reference Documents

Applicable Product	Manual Title
RX64M Group	RX64M Group User's Manual: Hardware Rev.1.20 (R01UH0377EJ0120)
RX65N Group, RX651 Group	RX65N Group, RX651 Group User's Manual: Hardware Rev.2.40 (R01UH0590EJ0240)
RX66N Group	RX66N Group User's Manual: Hardware Rev.1.20 (R01UH0825EJ0120)
RX71M Group	RX71M Group User's Manual: Hardware Rev.1.20 (R01UH0493EJ0120)
RX72M Group	RX72M Group User's Manual: Hardware Rev.1.20 (R01UH0804EJ0120)
RX72N Group	RX72N Group User's Manual: Hardware Rev.1.20 (R01UH0824EJ0120)