Date: June. 7, 2013

RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU		Document No.	TN-RX*-A066A/E	Rev.	1.00
Title	Errata to RX62T and RX62G Groups User's Manuals Regarding CAN Module		Information Category	Technical Notification		
Applicable Product	RX62T Group RX62G Group	Lot No. All	Reference Document	RX62T Group User's Manual: Hardware Rev.1.30 (R01UH0034EJ0130) RX62G Group User's Manual: Hardware Rev.1.00 (R01UH0321EJ0100)		

This document describes corrections to the chapter "CAN module" in the User's Manuals: Hardware of the above groups.
The corrections are indicated in red in the list below.

Page and section numbers are based on the RX62T Group. Refer to the table on the last page for the corresponding pages and chapters in the RX62G group.

•Page 1075 of 1446
The description of BLIF Flag in 25.2.19 is corrected as follows:

Before correction

The BLIF bit is set to 1 if 32 consecutive dominant bits are detected on the CAN bus while the CAN module is in CAN operation mode.
After the BLIF bit is set to 1, 32 consecutive dominant bits are detected again under either of the following conditions:

- After this bit is set to 0 from 1, recessive bits are detected
- After this bit is set to 0 from 1, the CAN module enters CAN reset mode or CAN halt mode and then enters CAN operation mode again.

Corrections

The BLIF flag becomes 1 if 32 consecutive dominant bits are detected on the CAN bus while the CAN module is in CAN operation mode.
After the BLIF flag becomes 1, bus lock can be detected again after either of the following conditions is satisfied:

- After this flag is set to 0 from 1, recessive bits are detected (bus lock is resolved).
- After this flag is set to 0 from 1, the CAN module enters CAN reset mode and then enters CAN operation mode again (internal reset).

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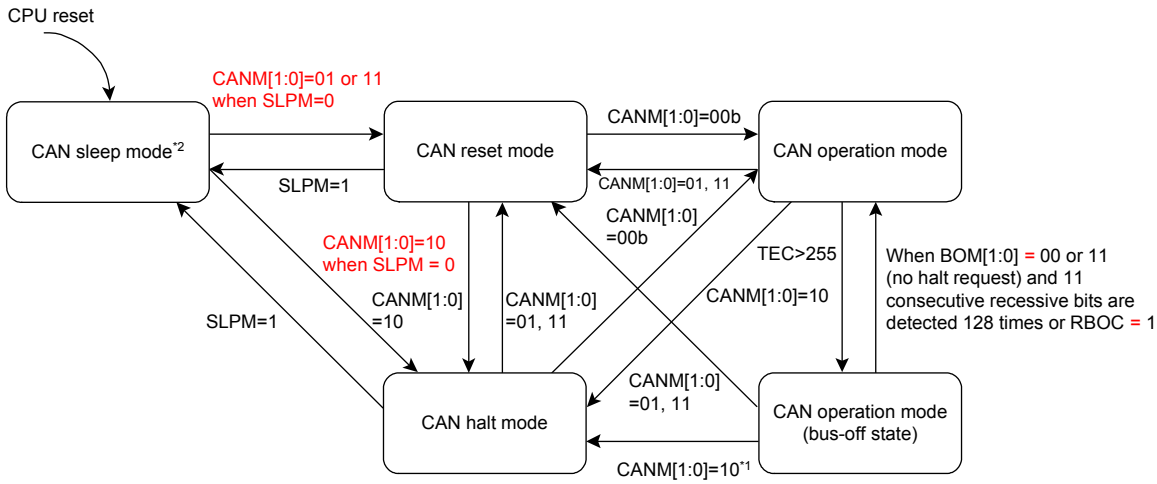
Figure 25.9 is corrected as follows:

Before correction

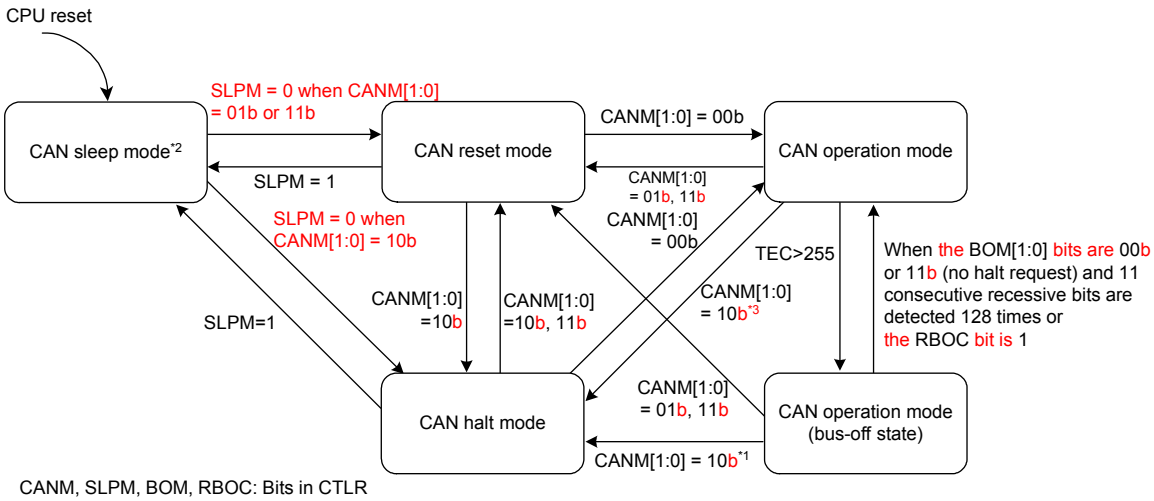


CANM, SLPM, BOM, RBOC: Bits in CTLR

Notes: 1. The transition timing from the bus-off state to CAN halt mode depends on the setting of the CTLR.BOM[1:0] bits.
— When the CTLR.BOM[1:0] bits are 01, the state transition timing is immediately after entering the bus-off state.
— When the CTLR.BOM[1:0] bits are 10, the state transition timing is at the end of the bus-off state.
— When the CTLR.BOM[1:0] bits are 11, the state transition timing is at the setting of the CTLR.CANM[1:0] bits to 10 (CAN halt mode).
2. Write 0 to only the CTLR.SLPM bit to exit CAN sleep mode. Only when the CAN module enters CAN sleep mode from CAN halt mode, the transition from CAN sleep mode to CAN halt mode is enabled

Figure 25.9 Transition between CAN Operating Modes

Corrections



CANM, SLPM, BOM, RBOC: Bits in CTLR

Note 1. The transition timing from the bus-off state to CAN halt mode depends on the setting of the CTLR.BOM[1:0] bits.
- When the CTLR.BOM[1:0] bits are 01b, the state transition timing is immediately after entering the bus-off state.
- When the CTLR.BOM[1:0] bits are 10b, the state transition timing is at the end of the bus-off state.
- When the CTLR.BOM[1:0] bits are 11b, the state transition timing is at the setting of the CTLR.CANM[1:0] bits to 10b (CAN halt mode).

Note 2. Write 0 to only the CTLR.SLPM bit to exit CAN sleep mode. Only when the CAN module enters CAN sleep mode from CAN halt mode, the transition from CAN sleep mode to CAN halt mode is enabled.

Note 3. The CAN module does not enter CAN halt mode while the CAN bus is locked in dominant state. Enter CAN reset mode instead.

Figure 25.9 Transition between CAN Operating Modes

•Page 1083 of 1446
Table 25.9 is corrected as follows:

Before correction

Table 25.9 Operation in CAN Reset Mode and CAN Halt Mode

Mode	Receiver	Transmitter	Bus-off
CAN reset mode (forcible transition) CANM[1:0] = 11	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode without waiting for the end of message transmission.	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN reset mode CANM[1:0] = 01	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode after waiting for the end of message transmission.*1*4	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN halt mode	CAN module enters CAN halt mode after waiting for the end of message reception.*2*3	CAN module enters CAN halt mode after waiting for the end of message transmission.*1*4	[When the CTLR.BOM[1:0] bits are 00] A halt request from a program will be accepted only after bus-off recovery. [When the CTLR.BOM[1:0] bits are 01] CAN module automatically enters CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the CTLR.BOM[1:0] bits are 10] CAN module automatically enters CAN halt mode after waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the CTLR.BOM[1:0] bits are 11] CAN module enters CAN halt mode (without waiting for the end of bus-off recovery) if a halt is requested by a program during bus-off.

Note 1. If several messages are requested to be transmitted, mode transition occurs after the completion of the first transmission. In a case that the CAN reset mode is being requested during suspend transmission, mode transition occurs when the bus is idle, the next transmission ends, or the CAN module becomes a receiver.
Note 2. If the CAN bus is locked at the dominant level, the program can detect this state by monitoring the BLIF flag in EIFR.
Note 3. If a CAN bus error occurs during reception after CAN halt mode is requested, the CAN module transits to CAN halt mode immediately.
Note 4. If a CAN bus error or arbitration lost occurs during transmission after CAN reset mode or CAN halt mode is requested, the CAN module transits to the requested CAN mode immediately.

Corrections

Table 25.9 Operation in CAN Reset Mode and CAN Halt Mode

Mode	Receiver	Transmitter	Bus-off
CAN reset mode (forcible transition) CANM[1:0] = 11b	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode without waiting for the end of message transmission.	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN reset mode CANM[1:0] = 01b	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode after waiting for the end of message transmission.*1,*4	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN halt mode	CAN module enters CAN halt mode after waiting for the end of message reception.*2,*3	CAN module enters CAN halt mode after waiting for the end of message transmission.*1,*2,*4	[When the BOM[1:0] bits are 00b] A halt request from a program will be accepted only after bus-off recovery. [When the BOM[1:0] bits are 01b] CAN module automatically enters CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM[1:0] bits are 10b] CAN module automatically enters CAN halt mode after waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM[1:0] bits are 11b] CAN module enters CAN halt mode (without waiting for the end of bus-off recovery) if a halt is requested by a program during bus-off.

CANM[1:0], BOM[1:0]: Bits in CTLR

Note 1. If several messages are requested to be transmitted, mode transition occurs after the completion of the first message transmission. In a case that the CAN reset mode is being requested during suspend transmission, mode transition occurs when the bus is idle, the next transmission ends, or the CAN module becomes a receiver.

Note 2. If the CAN bus is locked in dominant state, the program can detect this state by monitoring the EIFR.BLIF flag. The CAN module does not enter CAN halt mode while the CAN bus is locked in dominant state. Enter CAN reset mode instead.

Note 3. If a CAN bus error occurs during reception after CAN halt mode is requested, the CAN module enters CAN halt mode immediately. However, the CAN module does not enter CAN Halt mode when the CAN bus is locked in dominant state.

Note 4. If a CAN bus error or arbitration-lost occurs during transmission after CAN reset mode or CAN halt mode is requested, the CAN module enters the requested operating mode immediately. However, the CAN module does not enter CAN Halt mode when the CAN bus is locked in dominant state.

<Reference Documents>

Applicable Product	Manual and Document Number	Page Number, Figure/Title Number		
		BLIF Bit	Figure X.34	Table X.9
RX62T Group	RX62T Group User's Manual: Hardware Rev.1.30 (R01UH0034EJ0130)	Page 1075 25.2.19	Page 1081 Figure 25.9	Page 1083 Table 25.9
RX62G Group,	RX62G Group User's Manual: Hardware Rev.1.00 (R01UH0321EJ0100)	Page 1030 25.2.19	Page 1036 Figure 25.9	Page 1038 Table 25.9