

RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU	Document No.	TN-RX*-A065A/E	Rev.	1.00
Title	Errata to RX62N and RX621 Groups User's Manual Regarding CAN Module		Information Category	Technical Notification	
Applicable Product	RX62N Group, RX621 Group	Lot No.	Reference Document	RX62N Group, RX621 Group User's Manual: Hardware Rev.1.30 (R01UH0033EJ0130)	
		All			

This document describes corrections to the chapter "CAN module" in the RX62N Group, RX621 Group User's Manual: Hardware.

The corrections are indicated in red in the list below.

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The description of BLIF Flag in 32.2.19 is corrected as follows:

Before correction

The BLIF **bit is set to 1** if 32 consecutive dominant bits are detected on the CAN bus while the CAN module is in CAN operation mode.

After the BLIF **bit is set to 1**, **32 consecutive dominant bits are** detected again **under** either of the following conditions:

- After this **bit** is set to 0 from 1, recessive bits are detected
- After this **bit** is set to 0 from 1, the CAN module enters CAN reset mode **or CAN halt mode** and then enters CAN operation mode again.

Corrections

The BLIF **flag becomes 1** if 32 consecutive dominant bits are detected on the CAN bus while the CAN module is in CAN operation mode.

After the BLIF **flag becomes 1**, **bus lock can be** detected again **after** either of the following conditions **is satisfied**:

- After this **flag** is set to 0 from 1, recessive bits are detected (**bus lock is resolved**).
- After this **flag** is set to 0 from 1, the CAN module enters CAN reset mode and then enters CAN operation mode again (**internal reset**).

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Figure 32.9 is corrected as follows:

Before correction

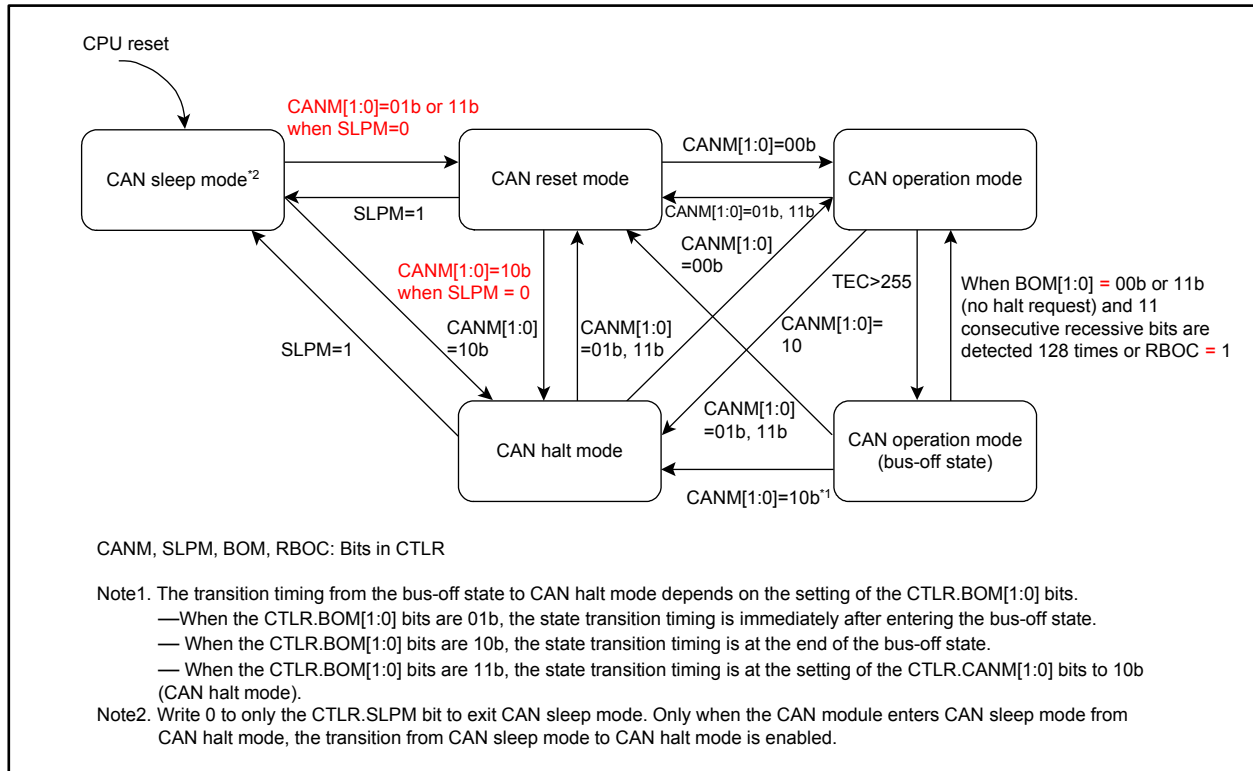


Figure 32.9 Transition between CAN Operating Modes

Corrections

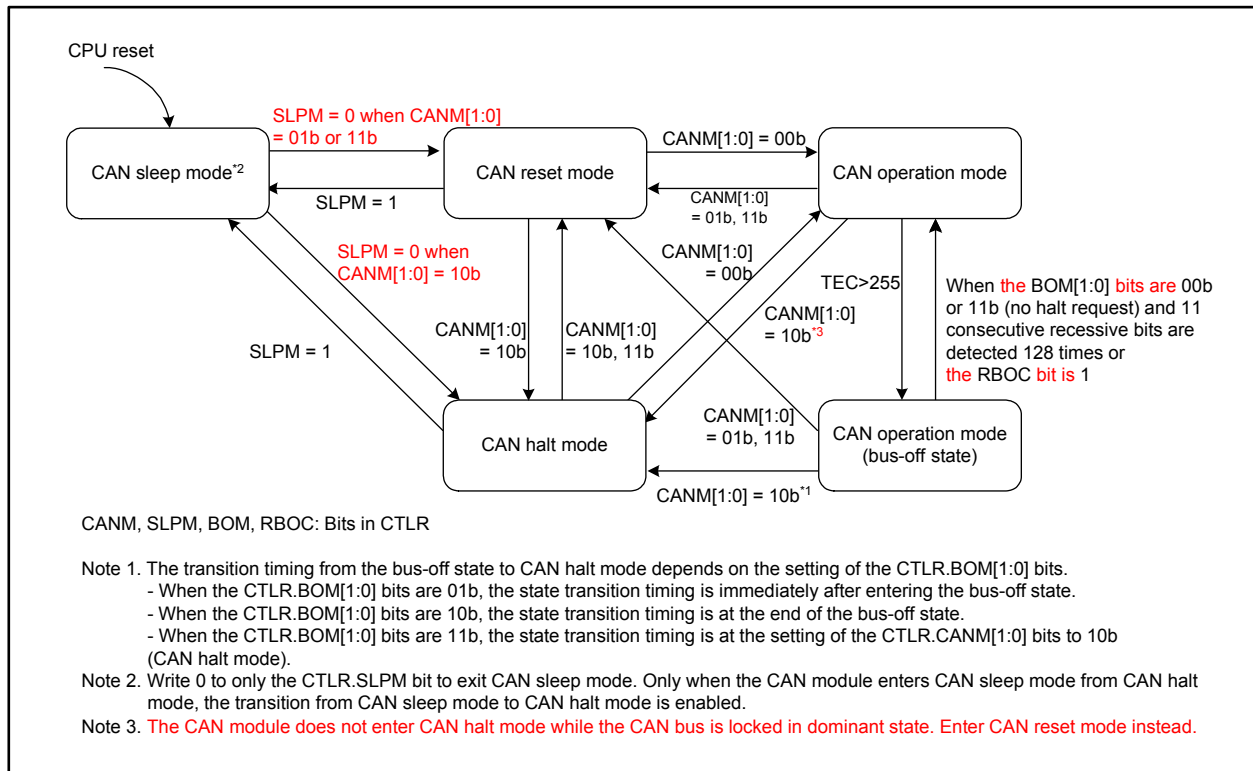


Figure 32.9 Transition between CAN Operating Modes

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 Table 32.9 is corrected as follows:

Before correction

Table 32.9 Operation in CAN Reset Mode and CAN Halt Mode

Mode	Receiver	Transmitter	Bus-off
CAN reset mode (forcible transition) CANM[1:0] = 11b	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode without waiting for the end of message transmission.	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN reset mode CANM[1:0] = 01b	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode after waiting for the end of message transmission. *1*4	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN halt mode	CAN module enters CAN halt mode after waiting for the end of message reception. *2*3	CAN module enters CAN halt mode after waiting for the end of message transmission. *1*4	[When the BOM[1:0] bits are 00b] A halt request from a program will be accepted only after bus-off recovery. [When the BOM[1:0] bits are 01b] CAN module automatically enters CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM[1:0] bits are 10b] CAN module automatically enters CAN halt mode after waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM[1:0] bits are 11b] CAN module enters CAN halt mode (without waiting for the end of bus-off recovery) if a halt is requested by a program during bus-off.

[Legend]
 BOM[1:0] bits: Bits in CTRLR

- Note 1. If several messages are requested to be transmitted, mode transition occurs after the completion of the first transmission. In a case that the CAN reset mode is being requested during suspend transmission, mode transition occurs when the bus is idle, the next transmission ends, or the CAN module becomes a receiver.
- Note 2. If the CAN bus is locked at the dominant level, the program can detect this state by monitoring the BLIF bit in EIFR.
- Note 3. If a CAN bus error occurs during reception after CAN halt mode is requested, the CAN module transits to CAN halt mode immediately.
- Note 4. If a CAN bus error or arbitration lost occurs during transmission after CAN reset mode or CAN halt mode is requested, the CAN module transits to the requested CAN mode immediately.

Corrections

Table 32.9 Operation in CAN Reset Mode and CAN Halt Mode

Mode	Receiver	Transmitter	Bus-off
CAN reset mode (forcible transition) CANM[1:0] = 11b	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode without waiting for the end of message transmission.	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN reset mode CANM[1:0] = 01b	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode after waiting for the end of message transmission. *1,*4	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN halt mode	CAN module enters CAN halt mode after waiting for the end of message reception. *2,*3	CAN module enters CAN halt mode after waiting for the end of message transmission. *1,*2,*4	[When the BOM[1:0] bits are 00b] A halt request from a program will be accepted only after bus-off recovery. [When the BOM[1:0] bits are 01b] CAN module automatically enters CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM[1:0] bits are 10b] CAN module automatically enters CAN halt mode after waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM[1:0] bits are 11b] CAN module enters CAN halt mode (without waiting for the end of bus-off recovery) if a halt is requested by a program during bus-off.

[Legend]

CANM[1:0], BOM[1:0]: Bits in CTRLR

- Note 1. If several messages are requested to be transmitted, mode transition occurs after the completion of the first message transmission. In a case that the CAN reset mode is being requested during suspend transmission, mode transition occurs when the bus is idle, the next transmission ends, or the CAN module becomes a receiver.
- Note 2. If the CAN bus is locked in dominant state, the program can detect this state by monitoring the EIFR.BLIF flag. The CAN module does not enter CAN halt mode while the CAN bus is locked in dominant state. Enter CAN reset mode instead.
- Note 3. If a CAN bus error occurs during reception after CAN halt mode is requested, the CAN module enters CAN halt mode immediately. However, the CAN module does not enter CAN Halt mode when the CAN bus is locked in dominant state.
- Note 4. If a CAN bus error or arbitration-lost occurs during transmission after CAN reset mode or CAN halt mode is requested, the CAN module enters the requested operating mode immediately. However, the CAN module does not enter CAN Halt mode when the CAN bus is locked in dominant state.