Date: Sep. 3, 2024

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A0278A/E	Rev.	1.00
Title	Errata Regarding Setting of the RCR4.RCKSEL Bit for the RX64M Group and RX71M Group MCUs		Information Category	Technical Notification		
Applicable Product	RX64M Group, RX71M Group	Lot No. All	Reference Document	User's Manual: Hardware for applicable products listed under Related Documents on the last page		

This document describes corrections to the flowcharts in section 9.10.6, Notes on Sub-Clock Oscillator, section 32.3.2, Clock and Count Mode Setting Procedure, and section 32.6.7, Initialization Procedure When the Realtime Clock is Not to be Used in User's Manual: Hardware for the applicable products. The page and figure numbers are based on those of the manual for the RX64M Group. Refer to Reference Documents on the last page for the corresponding page and figure numbers in the manuals for other groups.

• Purpose of Corrections

The procedure for setting the sub-clock is described in parts of both sections 9 and 32: section 9.10.6, Notes on Sub-clock Oscillator, section 32.3.2, Clock and Count Mode Setting Procedure, and section 32.6.7, Initialization Procedure When the Realtime Clock is Not to be Used. Although writing to the RCR4.RCKSEL bit should only proceed once, a value is set in the bit in the flowcharts in each of the sections stated above.

For this reason, setting of the RCR4.RCKSEL bit should only proceed in accord with the flowchart from the Realtime Clock section and the step should be omitted from the sub-clock setting procedures.

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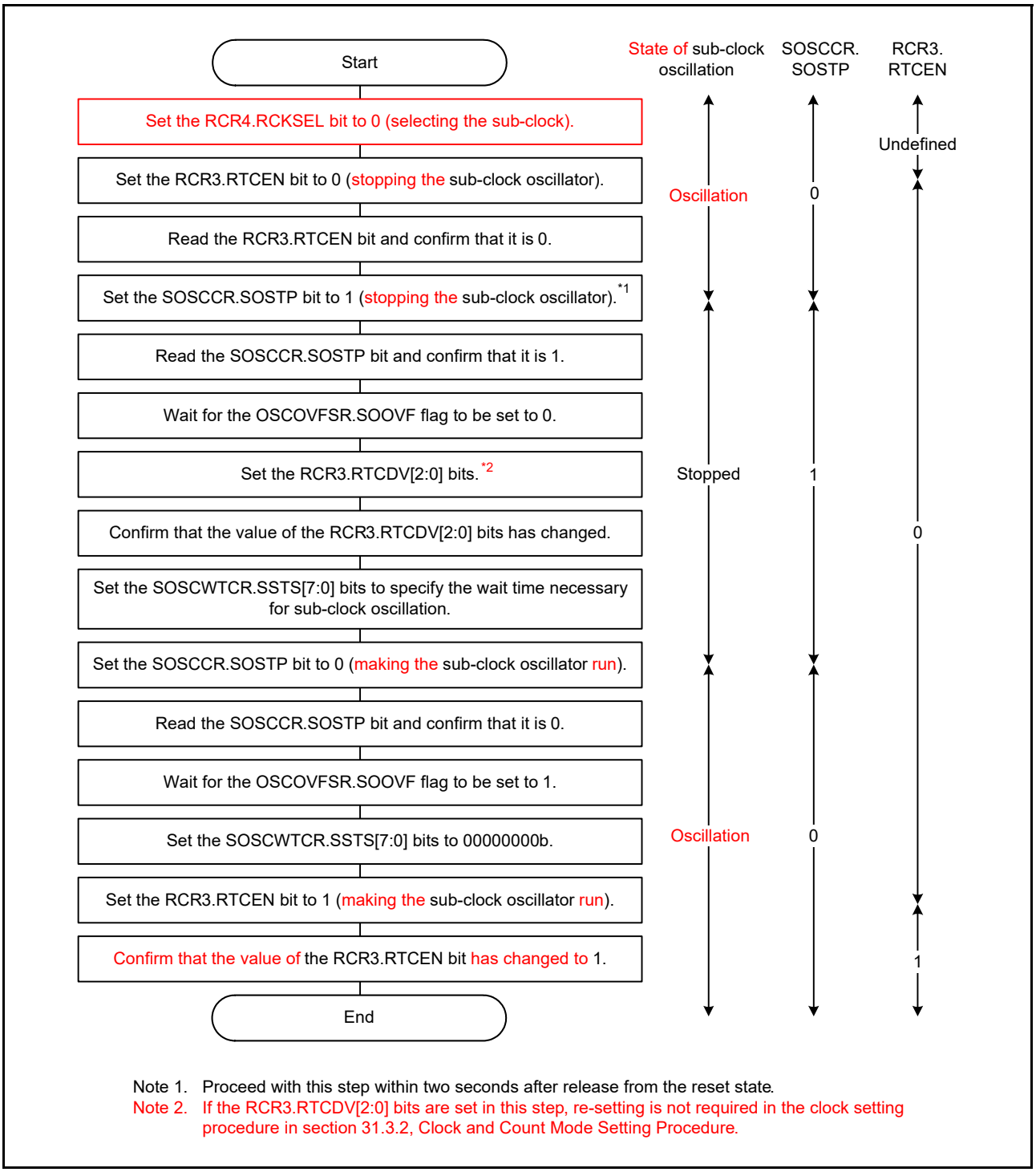
The following deletions are made in Figure 9.11, Example Flowchart of Initialization when the Sub-Clock is to be Used as the Source to Drive Counting by the Realtime Clock.

- The RCR4.RCKSEL bit setting
- Note 2

The title of Figure 9.11 is also modified.

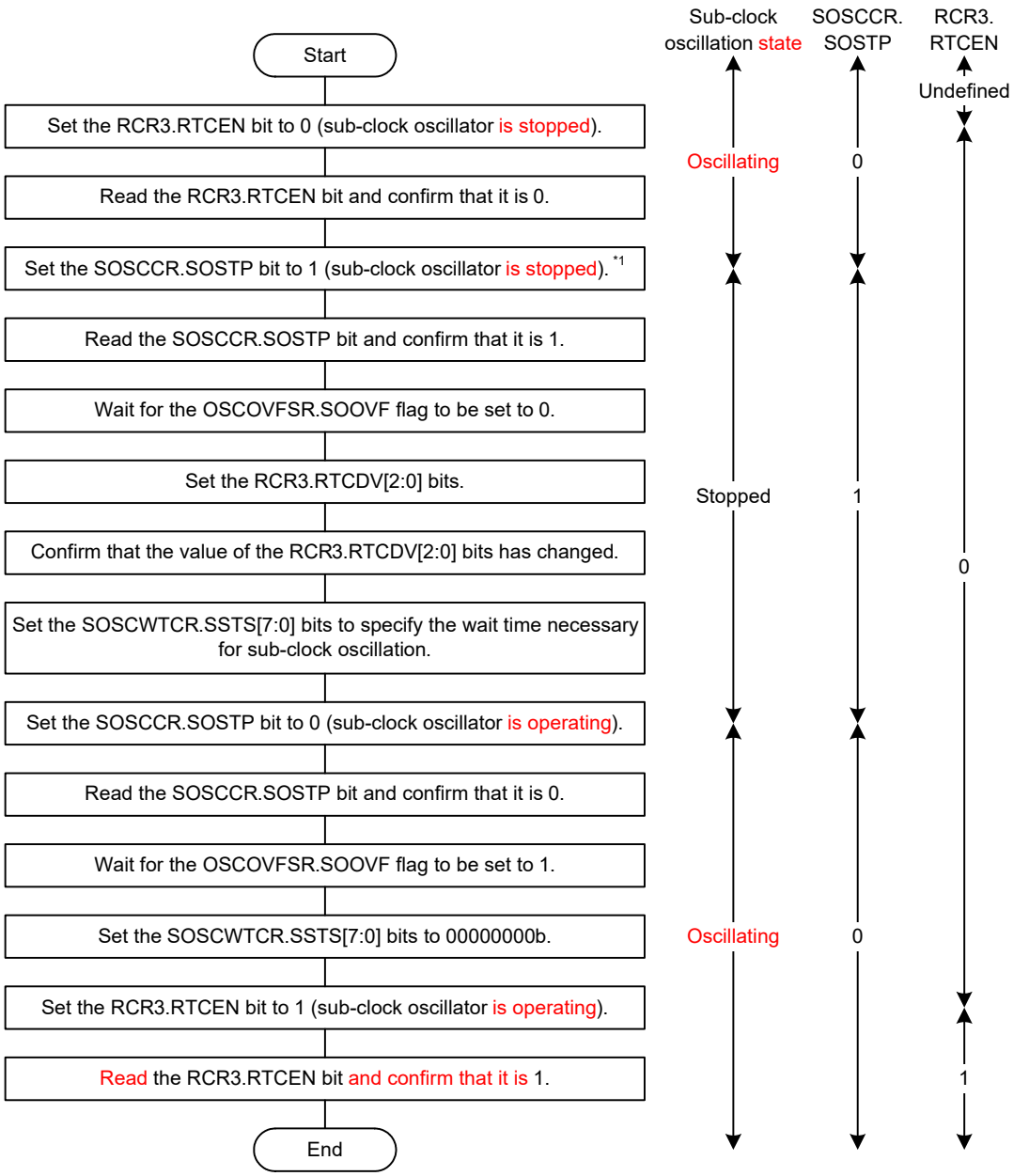
Before correction



Note 1. Proceed with this step within two seconds after release from the reset state.
Note 2. If the RCR3.RTCDV[2:0] bits are set in this step, re-setting is not required in the clock setting procedure in section 31.3.2, Clock and Count Mode Setting Procedure.

Figure 9.11 Example Flowchart of Initialization when the Sub-Clock is to be Used as the Source to Drive Counting by the Realtime Clock

After correction



Note 1. Proceed with this step within two seconds after release from the reset state.

Figure 9.11 Example of Initialization Flowchart When the Sub-Clock Is to Be Used as the Clock Source for the RTC

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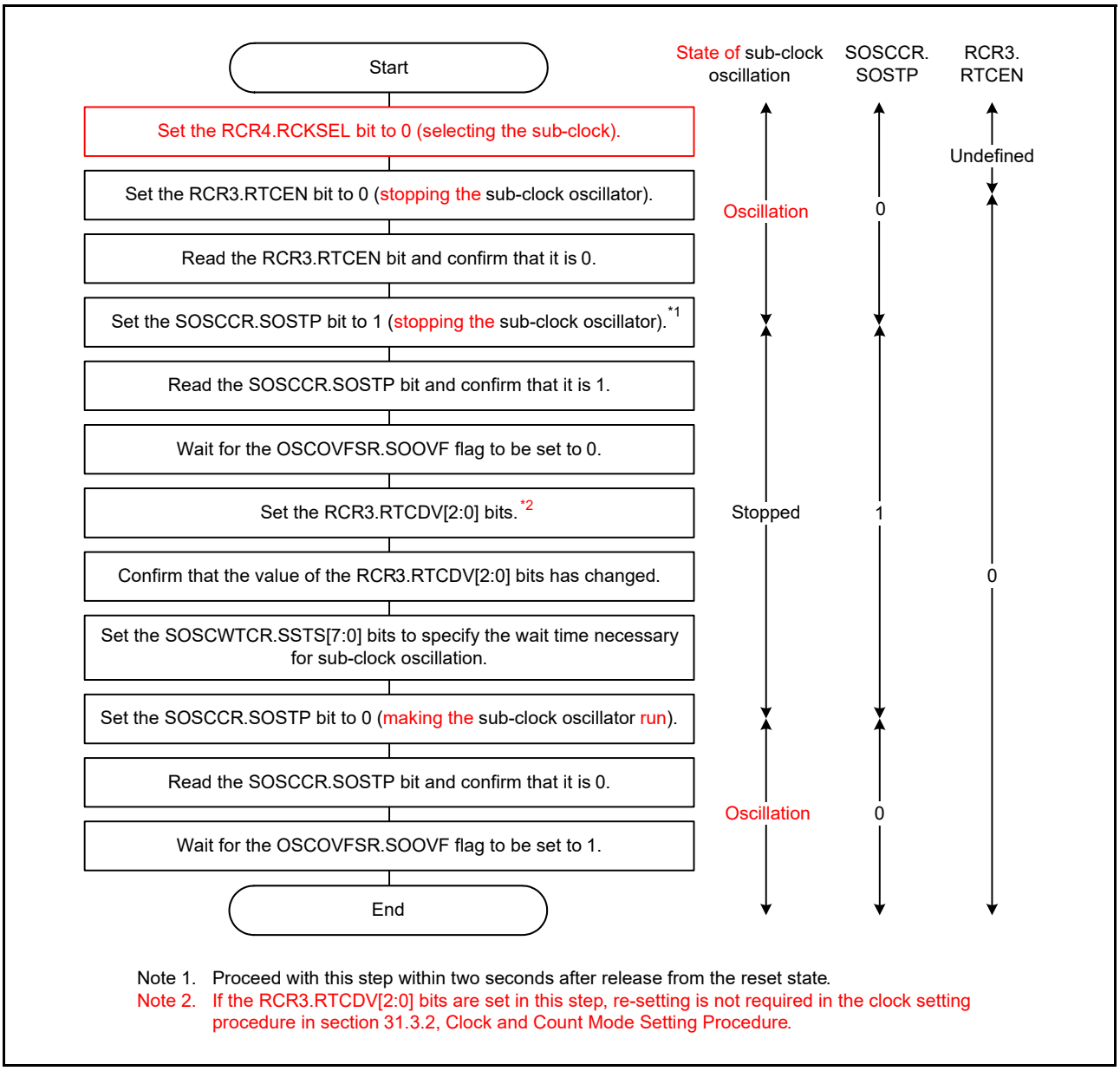
The following deletions are made in Figure 9.12, Example Flowchart for Initialization when the Sub-Clock is to be Used only as the System Clock.

- The RCR4.RCKSEL bit setting
- Note 2

The title of Figure 9.12 is also modified.

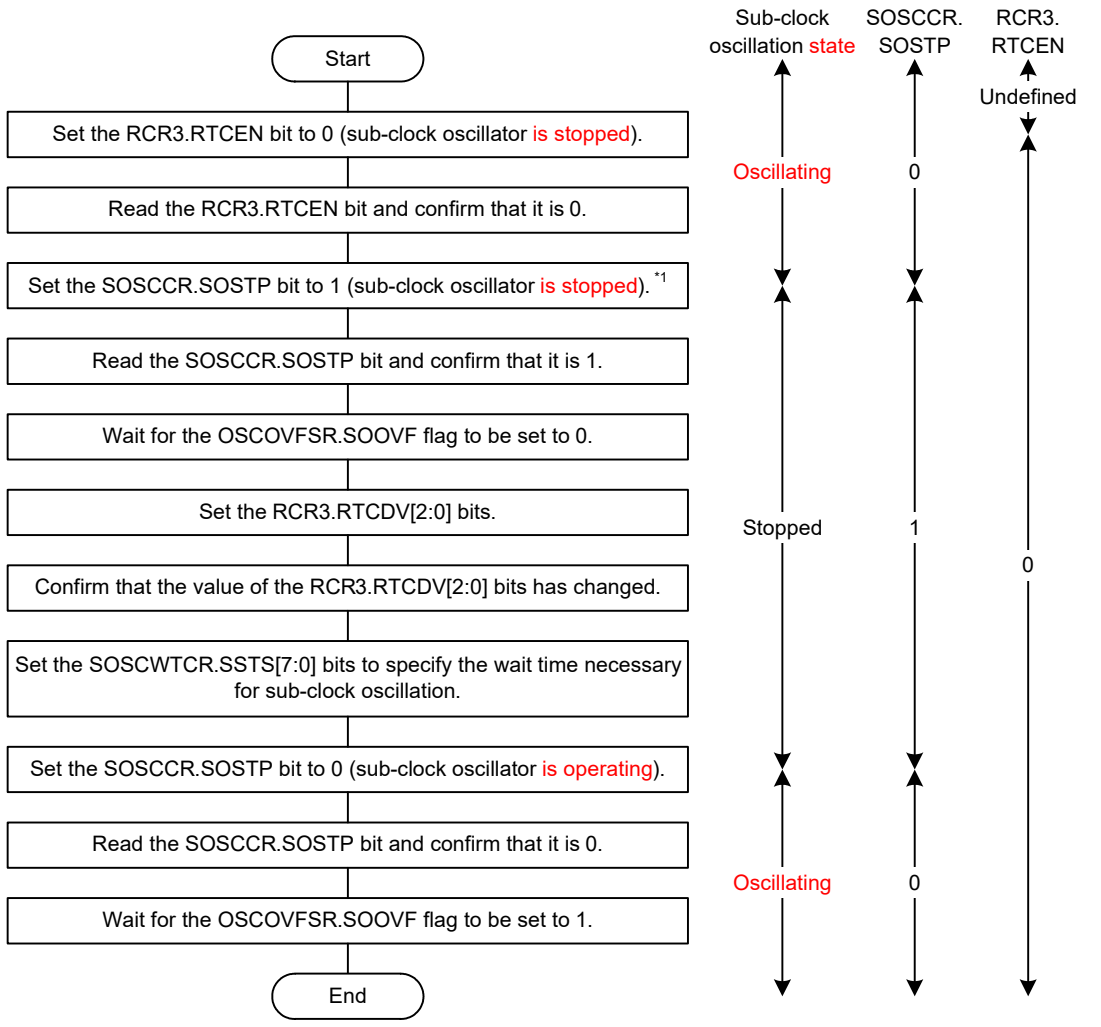
Before correction



Note 1. Proceed with this step within two seconds after release from the reset state.
Note 2. If the RCR3.RTCDV[2:0] bits are set in this step, re-setting is not required in the clock setting procedure in section 31.3.2, Clock and Count Mode Setting Procedure.

Figure 9.12 Example Flowchart for Initialization when the Sub-Clock is to be Used only as the System Clock

After correction



Note 1. Proceed with this step within two seconds after release from the reset state.

Figure 9.12 Example of Initialization Flowchart When the Sub-Clock Is Not to Be Used as the Clock Source for the RTC

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The following deletions are made in Figure 9.13, Example Flowchart for when the Sub-Clock is not to be Used.

- The RCR4.RCKSEL bit setting
- The SOSCCR2.SOSTP2 bit setting
- Note 1

Before correction

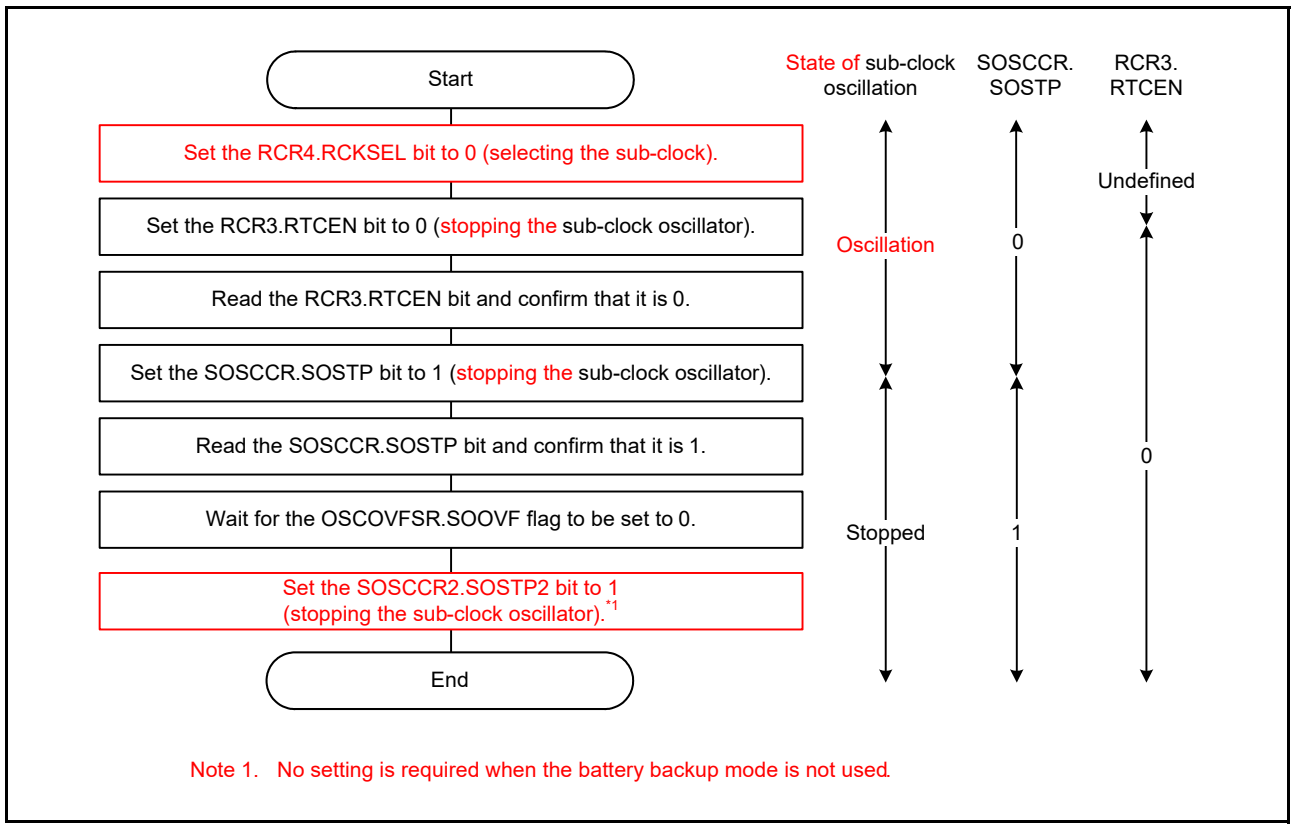

Figure 9.13 Example Flowchart for when the Sub-Clock is not to be Used

After correction

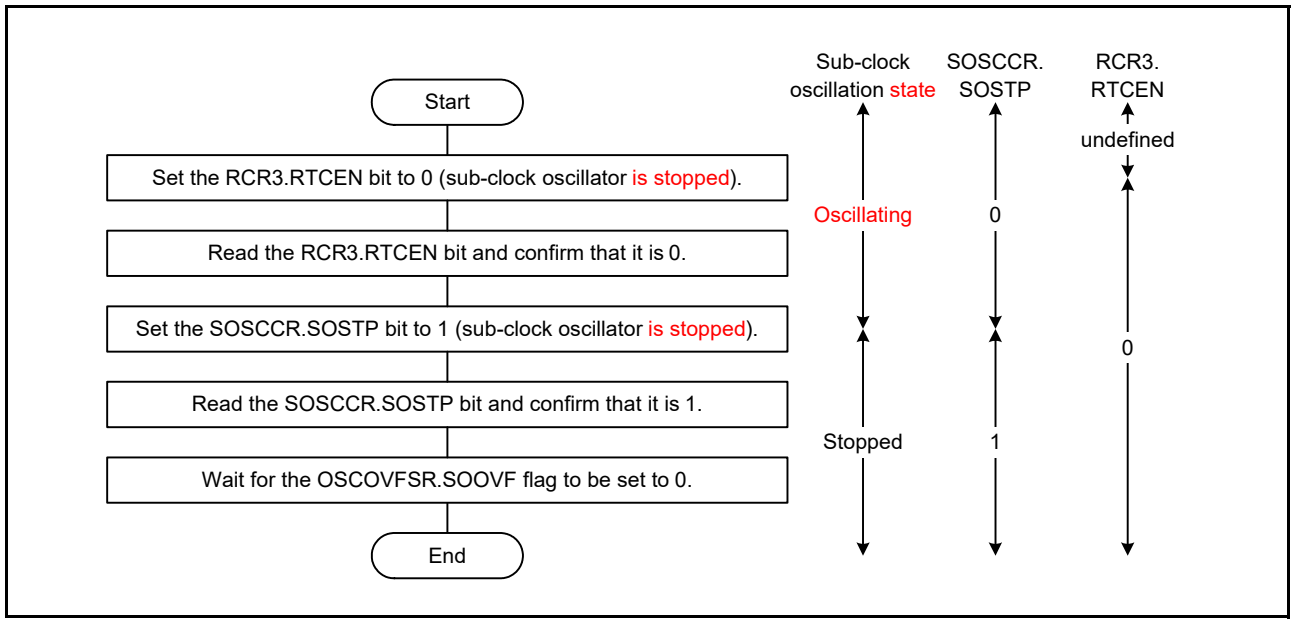

Figure 9.13 Example of Initialization Flowchart When the Sub-Clock Is Not to Be Used

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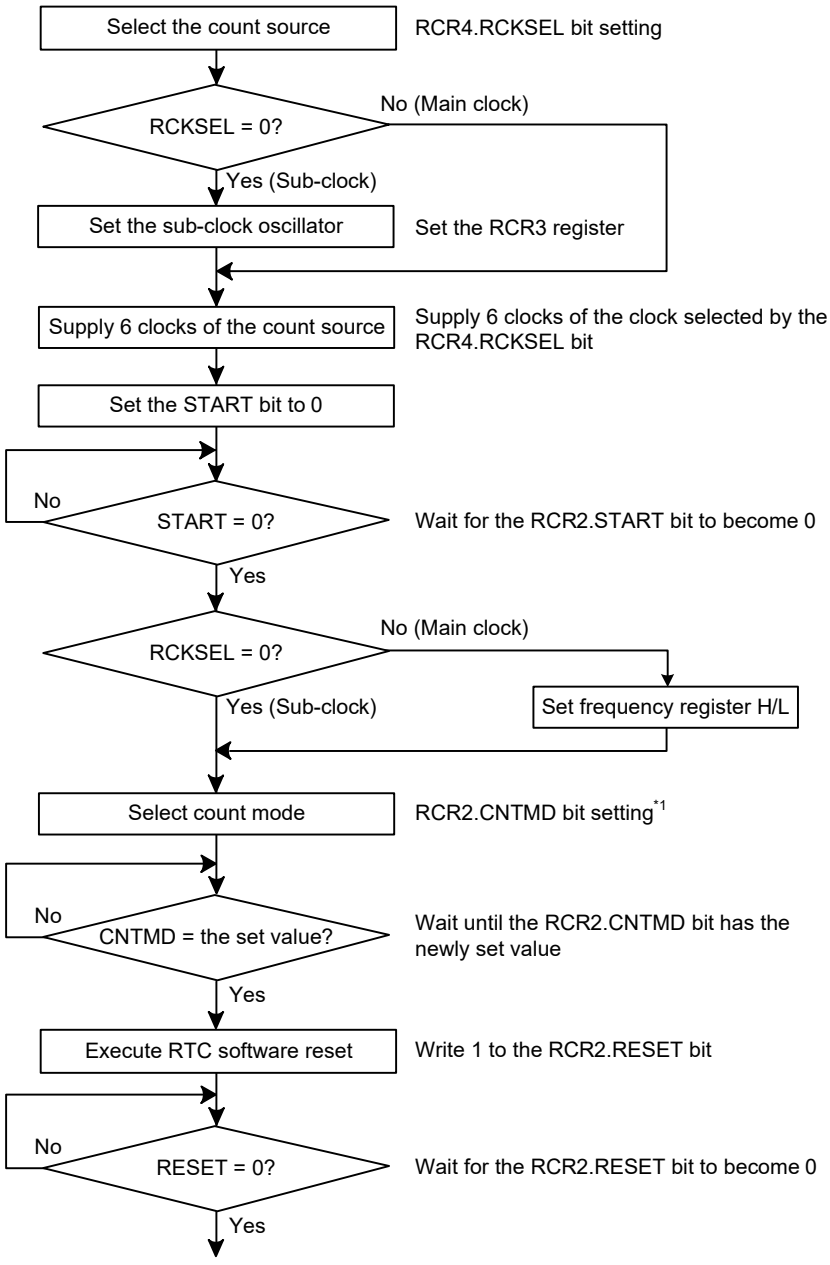
Figure 32.3, Clock and Count Mode Setting Procedure, in section 32.3.2, Clock and Count Mode Setting Procedure, is separated into two flowcharts as follows to suit the clock that is in use.

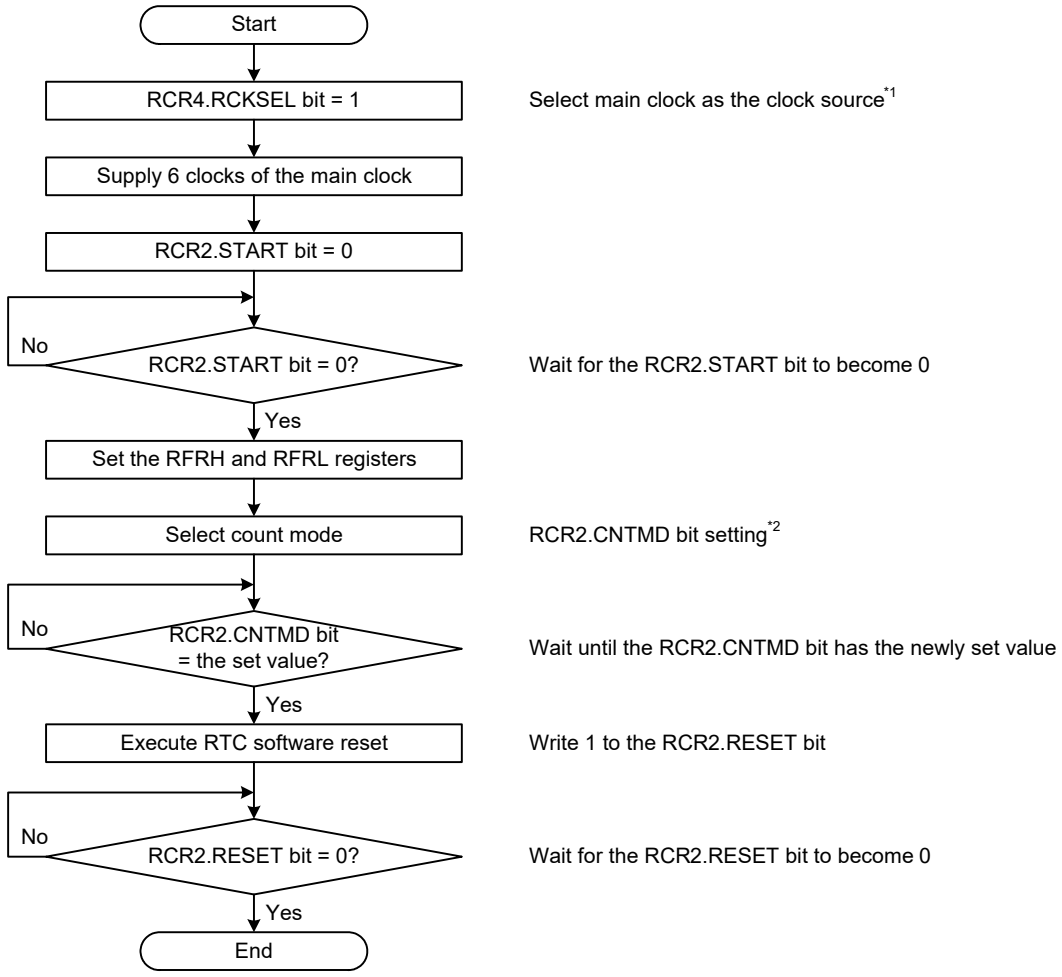
Before correction



Note 1. This step is not necessary if the count mode has been set concurrently with setting the START bit to 0. A value corresponding to the count mode setting must be written to the RCR2.CNTMD bit.

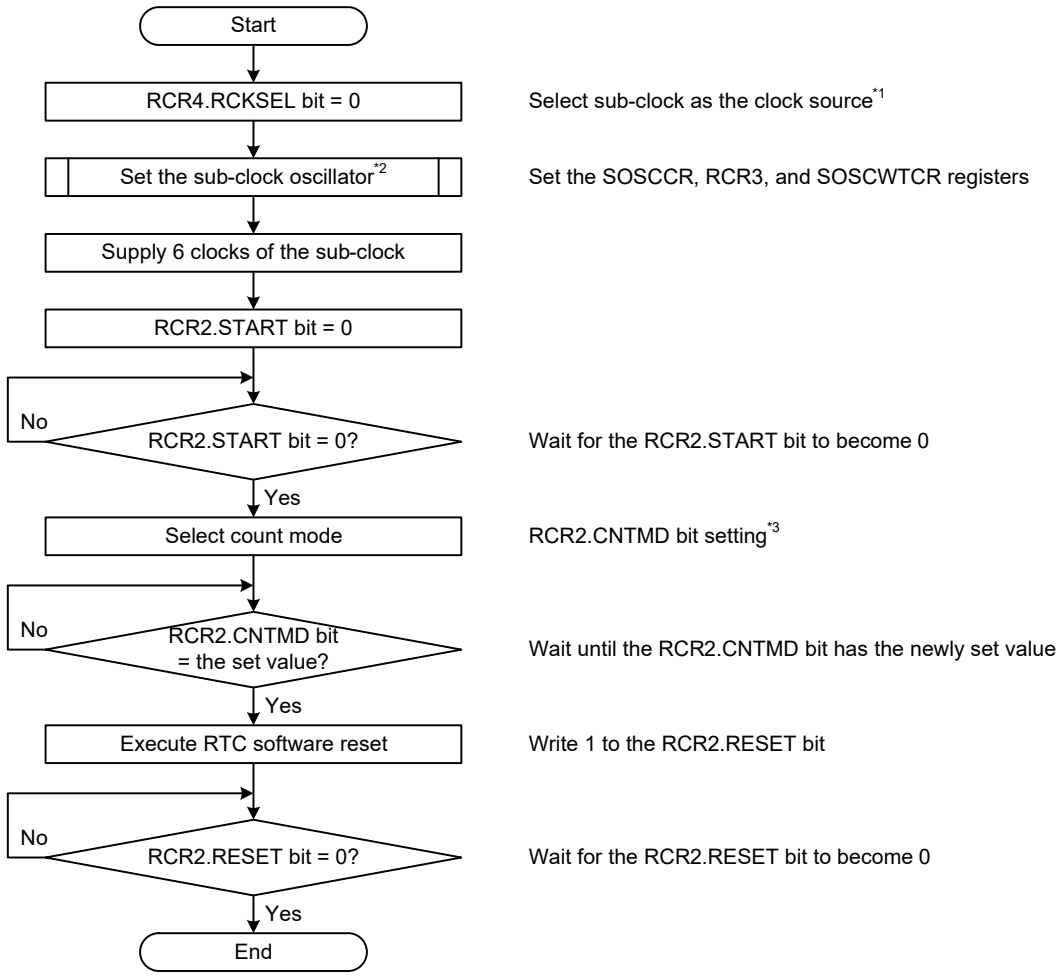
Figure 32.3 Clock and Count Mode Setting Procedure

After correction



Note 1. Only write to the RCR4.RCKSEL bit at this point in the flow.
Note 2. This step is not necessary if the count mode has been set concurrently with setting the RCR2.START bit to 0. A value corresponding to the count mode setting must be written to the RCR2.CNTMD bit.

Figure 32.3 Clock and Count Mode Setting Procedure (When Using Main Clock)



Note 1. Only write to the RCR4.RCKSEL bit at this point in the flow.
Note 2. For the procedure for setting up a sub-clock oscillator, refer to section 9, Clock Generation Circuit.
Note 3. This step is not necessary if the count mode has been set concurrently with setting the RCR2.START bit to 0. A value corresponding to the count mode setting must be written to the RCR2.CNTMD bit.

Figure 32.4 Clock and Count Mode Setting Procedure (When Using Sub-Clock)

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Figure 32.14, Initialization Procedure, in section 32.6.7, Initialization Procedure When the Realtime Clock is Not to be Used, is separated into two flowcharts as follows to suit the clock that is in use. A step of clearing the interrupt status flags is also added to both flowcharts.

Before correction

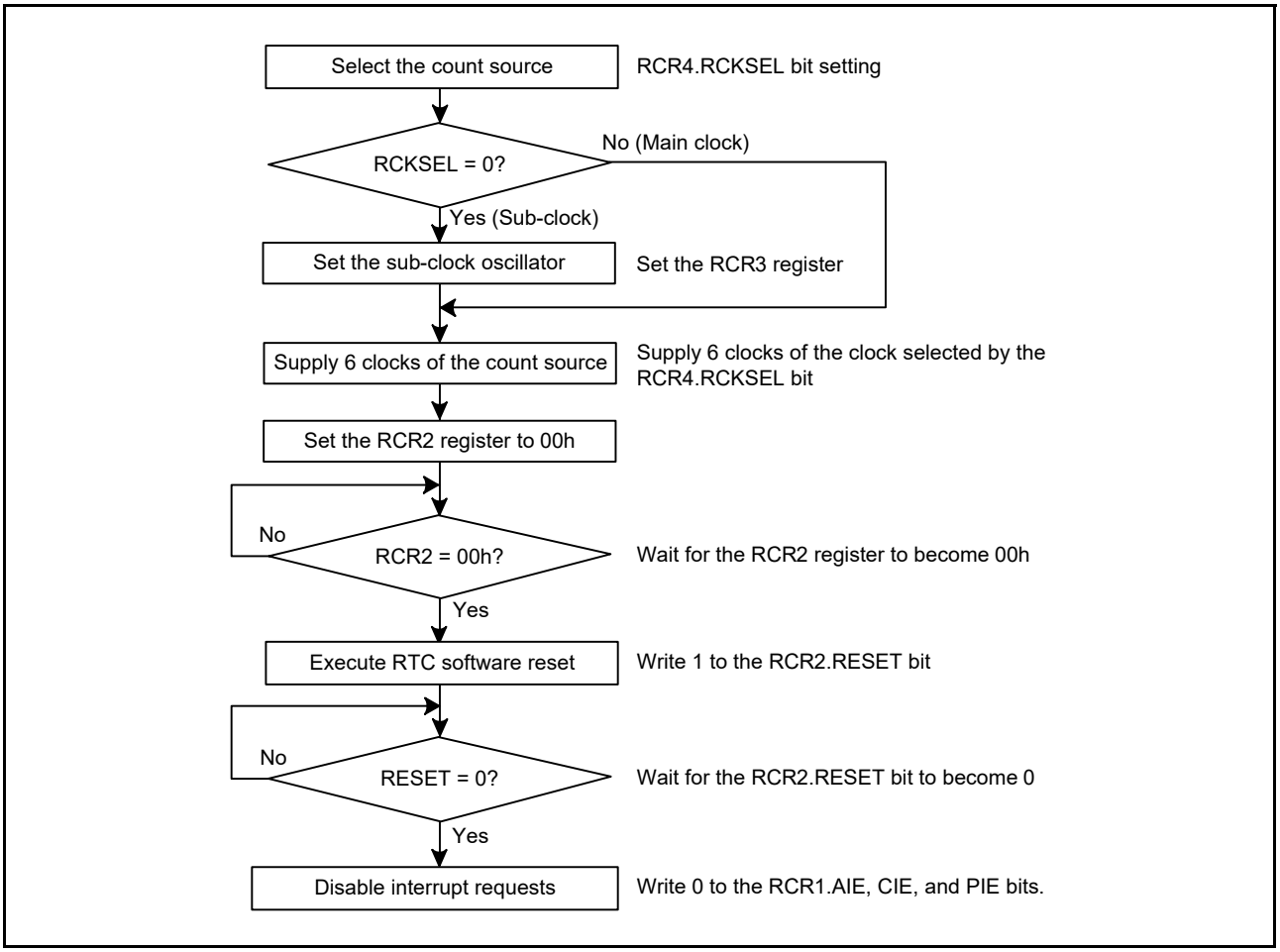


Figure 32.14 Initialization Procedure

After correction

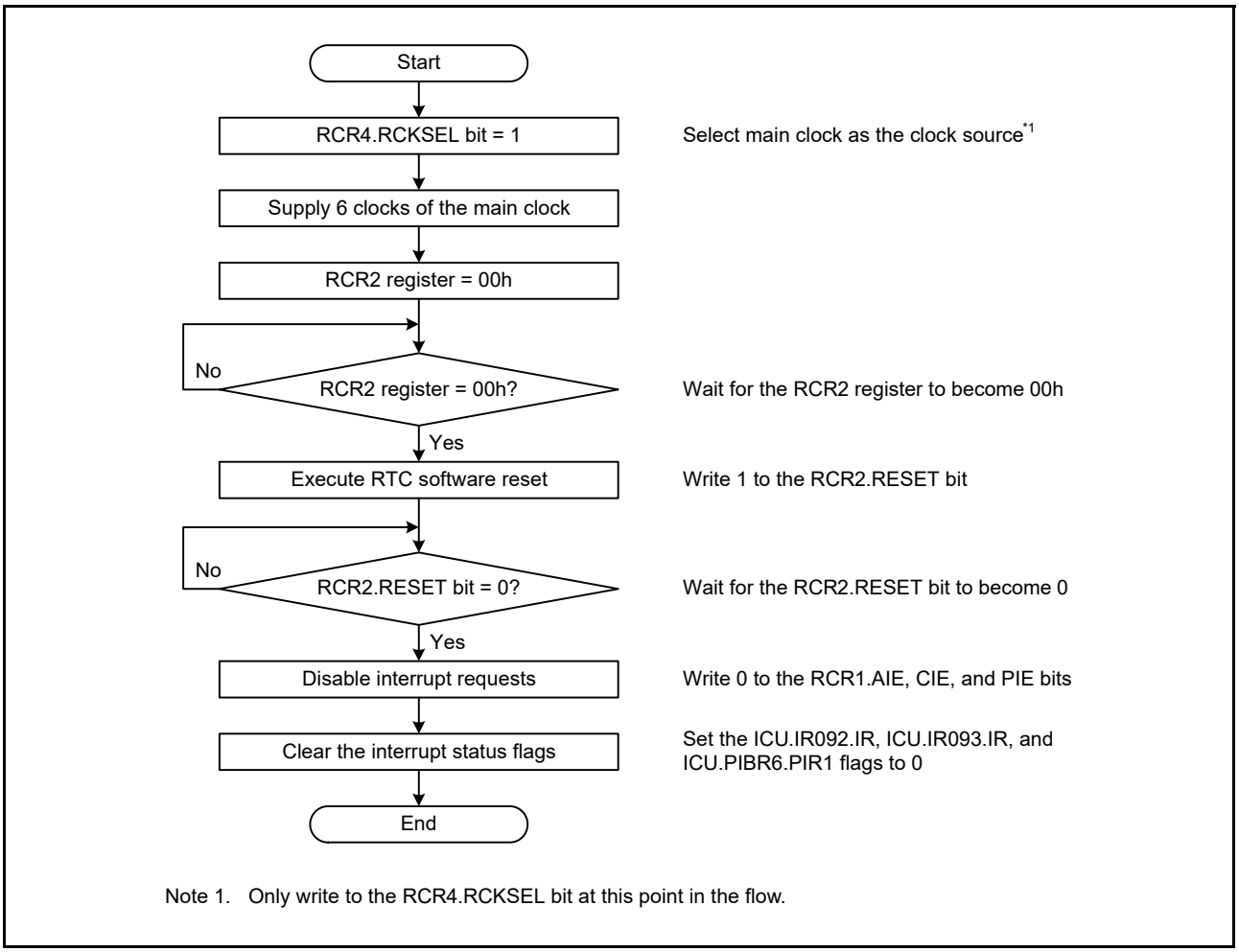
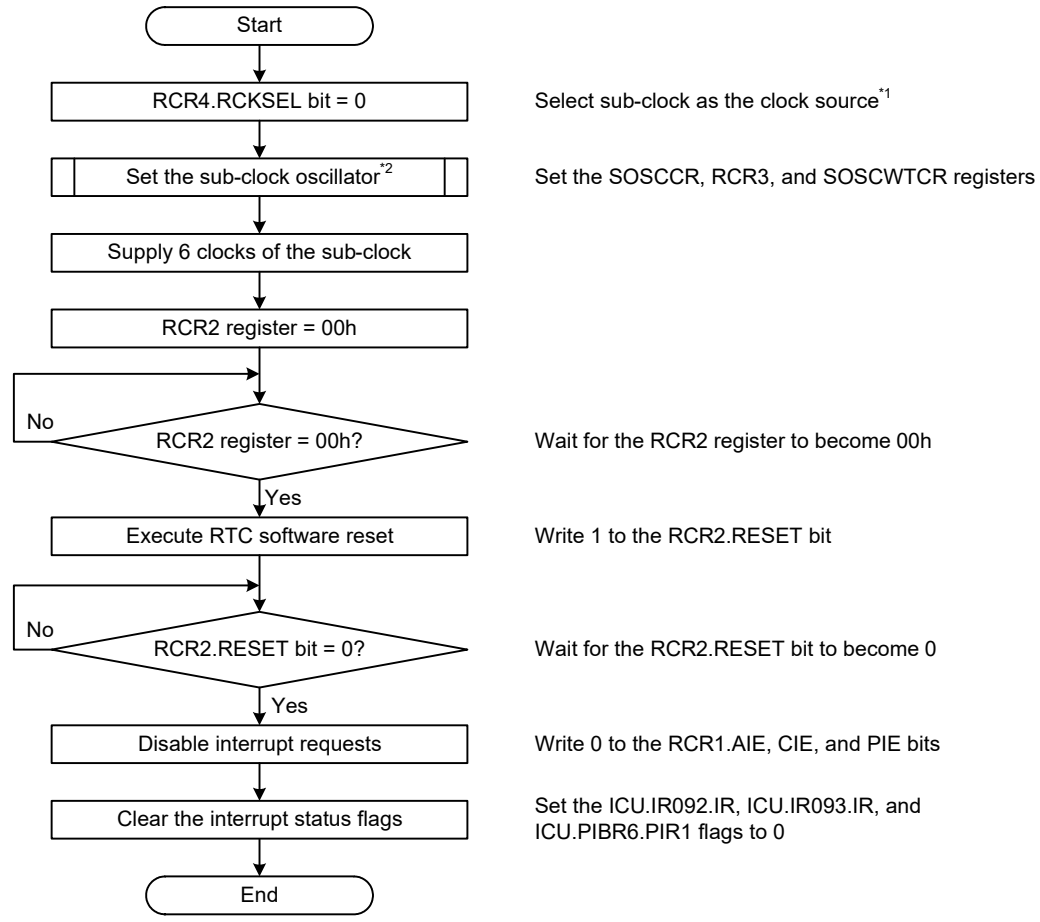


Figure 32.14 Initialization Procedure (When Using Main Clock)



Note 1. Only write to the RCR4.RCKSEL bit at this point in the flow.
Note 2. For the procedure for setting up a sub-clock oscillator, refer to section 9, Clock Generation Circuit.

Figure 32.15 Initialization Procedure (When Using Sub-Clock)

Reference Documents

Applicable Products	Manual Title (Document Number)	Page Number	Figure Number
RX64M Group	RX64M Group User's Manual: Hardware Rev.1.20 (R01UH0377EJ0120)	Pages 333 to 335 of 2963	Figures 9.11 to 9.13
		Page 1475 of 2963	Figure 32.3
		Page 1489 of 2963	Figure 32.14
RX71M Group	RX71M Group User's Manual: Hardware Rev.1.20 (R01UH0493EJ0120)	Pages 338 to 340 of 2975	Figures 9.13 to 9.15
		Page 1482 of 2975	Figure 32.3
		Page 1496 of 2975	Figure 32.14