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RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU		Document No.	TN-RX*-A114A/E	Rev.	1.00
Title	Corrections to User's Manual regarding the FASR.EXS bit for the Flash Memory in the RX110 Group		Information Category	Technical Notification		
Applicable Product	RX110 Group	Lot No.	Reference Document	RX110 Group User's Manual: Hardware Rev.1.00 (R01UH0421EJ0100) Specification Changes to the RX110 Group (TN-RX*-A112A/E) Corrections to Descriptions for the Flash Memory in the RX110 Group User's Manual (TN-RX*-A113A/E)		
		All				

This document describes corrections to the description for the FASR.EXS bit in section 31. Flash Memory of RX110 Group User's Manual: Hardware Rev.1.00.

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Description for the EXS bit of 31.3.7 Flash Area Select Register (FASR) is corrected as follows:

Before correction

Set this bit to 1 when programming the extra area using the FEXCR register.
Set this bit to 0 when not programming the extra area.

After correction

Set this bit to 1 before issuing a software command (unique ID read, start-up area information program, or access window information program) for the extra area. Set this bit to 0 before issuing a software command (program, block erase, or blank check) for the user area.
After issuing a software command, do not change the value until changing it for issuing the next software command.

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Figure 31.7 in (3) Programming and Erasure Procedures of 31.6.3 Software Command Usage is corrected as follows:

Before correction

Figure 31.7   **ROM Programming Procedure**

After correction

```
                    ┌──────────────────────────┐
                    │   Start in ROM P/E mode   │
                    └──────────────────────────┘
                                 │
                    ┌──────────────────────────┐
                    │     FASR.EXS bit = 0      │
                    └──────────────────────────┘
                                 │
                    ┌──────────────────────────┐
                    │  Set programming address  │
                    │ in registers FSARH and FSARL │
                    └──────────────────────────┘
                                 │
                    ┌──────────────────────────┐
                    │   Set programming data    │
                    │ in registers FWBH and FWBL │
                    └──────────────────────────┘
                                 │
                    ┌──────────────────────────┐
                    │     FCR register = 81h    │
                    └──────────────────────────┘
                                 │
                    ┌──────────────────────────┐    No
                    │  FSTATR1.FRDY flag = 1?   │───────►
                    └──────────────────────────┘
                                 │ Yes
                    ┌──────────────────────────┐
                    │     FCR register = 00h    │
                    └──────────────────────────┘
                                 │
                    ┌──────────────────────────┐    No
                    │  FSTATR1.FRDY flag = 0?   │───────►
                    └──────────────────────────┘
                                 │ Yes
                    ┌──────────────────────────┐    No
                    │ FSTATR0.ILGLERR flag = 1 or │──────────────┐
                    │ FSTATR0.PRGERR flag = 1?   │              │
                    └──────────────────────────┘              │
                                 │ Yes                         ▼
                    ┌──────────────────────────┐   ┌──────────────────────────┐  Yes
                    │ FRESETR.FRESET bit = 1    │   │  Continue ROM programming? │─────►
                    └──────────────────────────┘   └──────────────────────────┘
                                 │                          │ No
                    ┌──────────────────────────┐
                    │ FRESETR.FRESET bit = 0    │
                    └──────────────────────────┘
                                 │
                    ┌──────────────────────────┐
                    │    End in ROM P/E mode    │
                    └──────────────────────────┘
```

Sequencer initialization

Figure 31.7   Procedure to Issue the Program Command for the ROM

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Figure 31.8 in (3) Programming and Erasure Procedures of 31.6.3 Software Command Usage is corrected as follows:
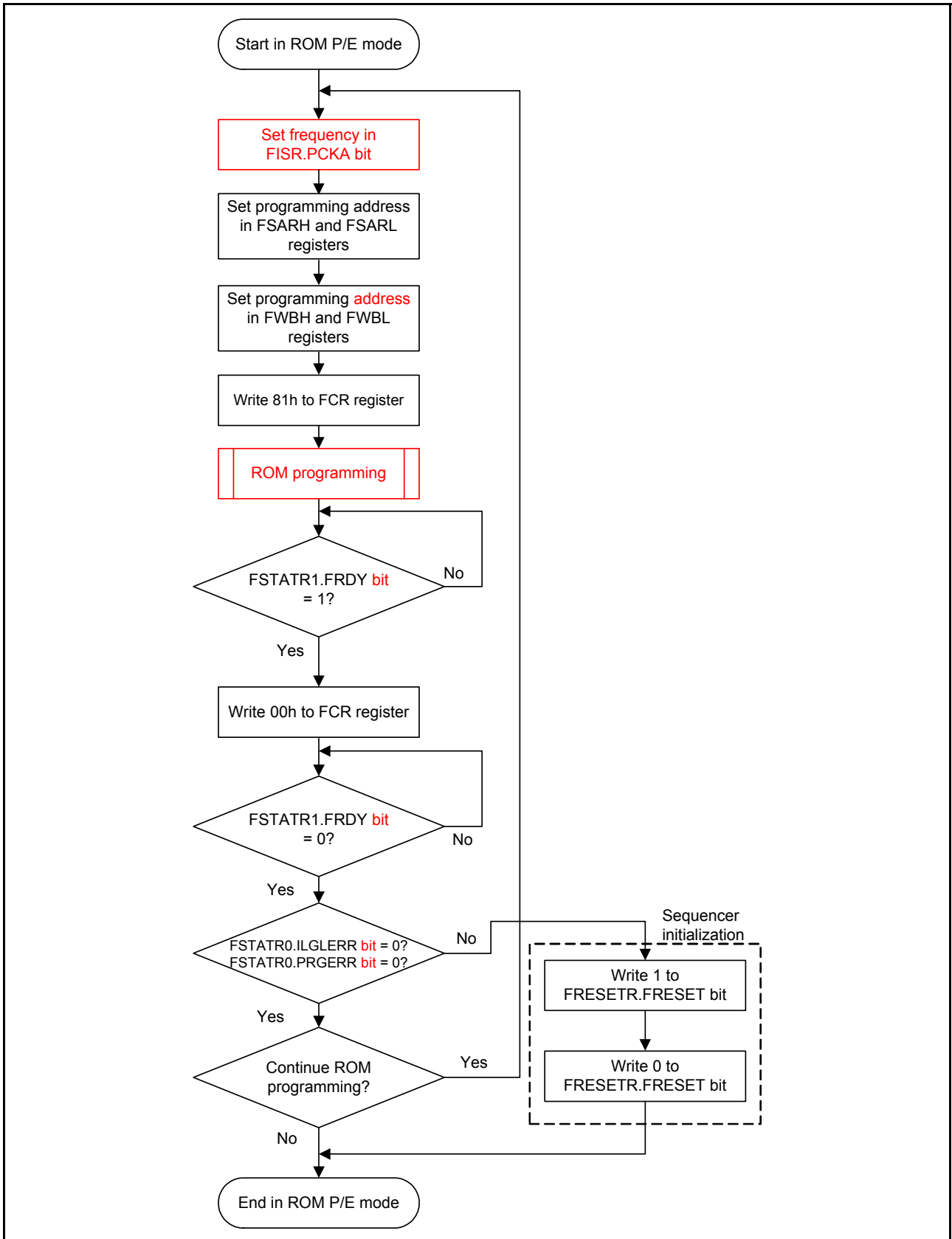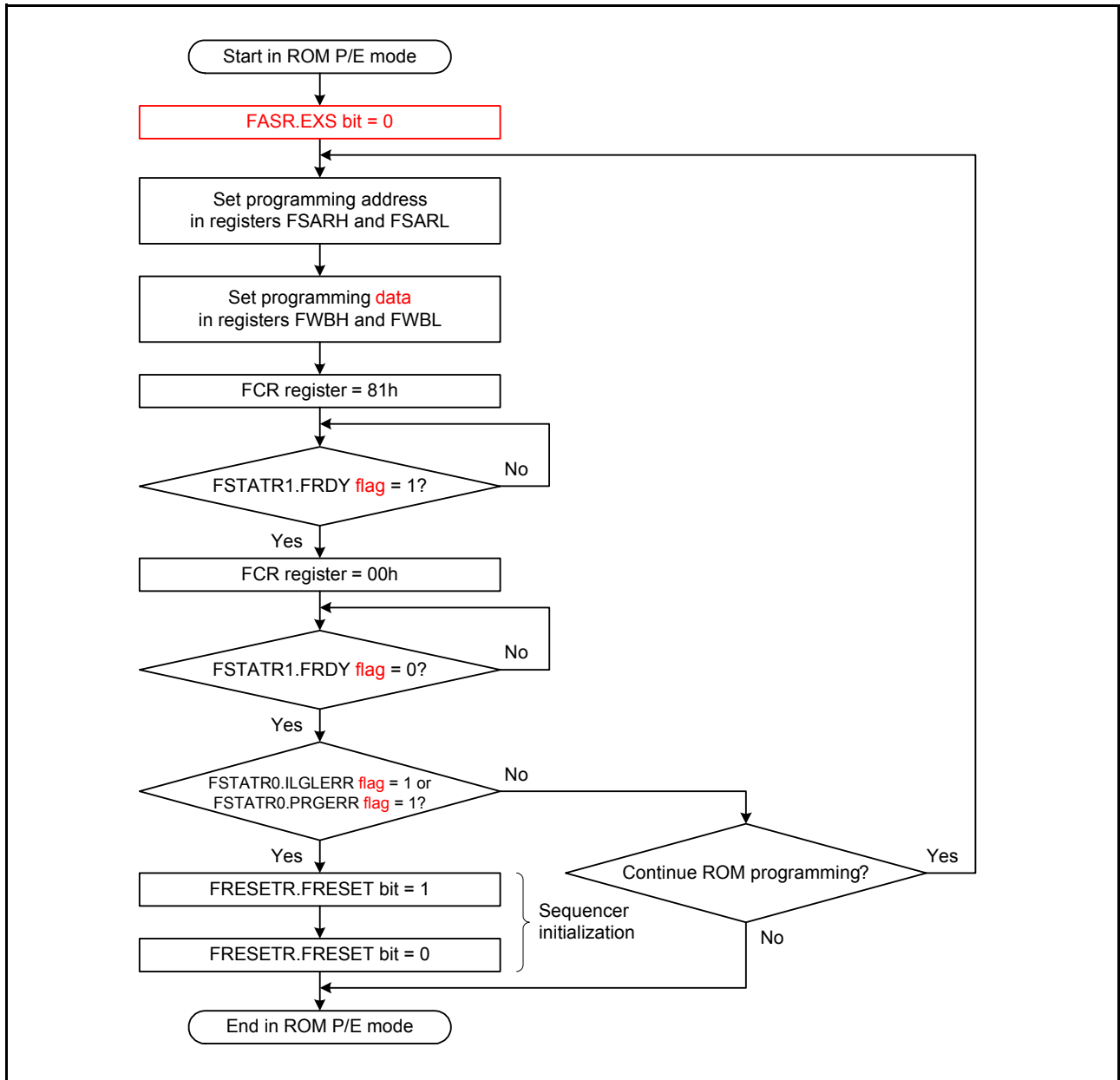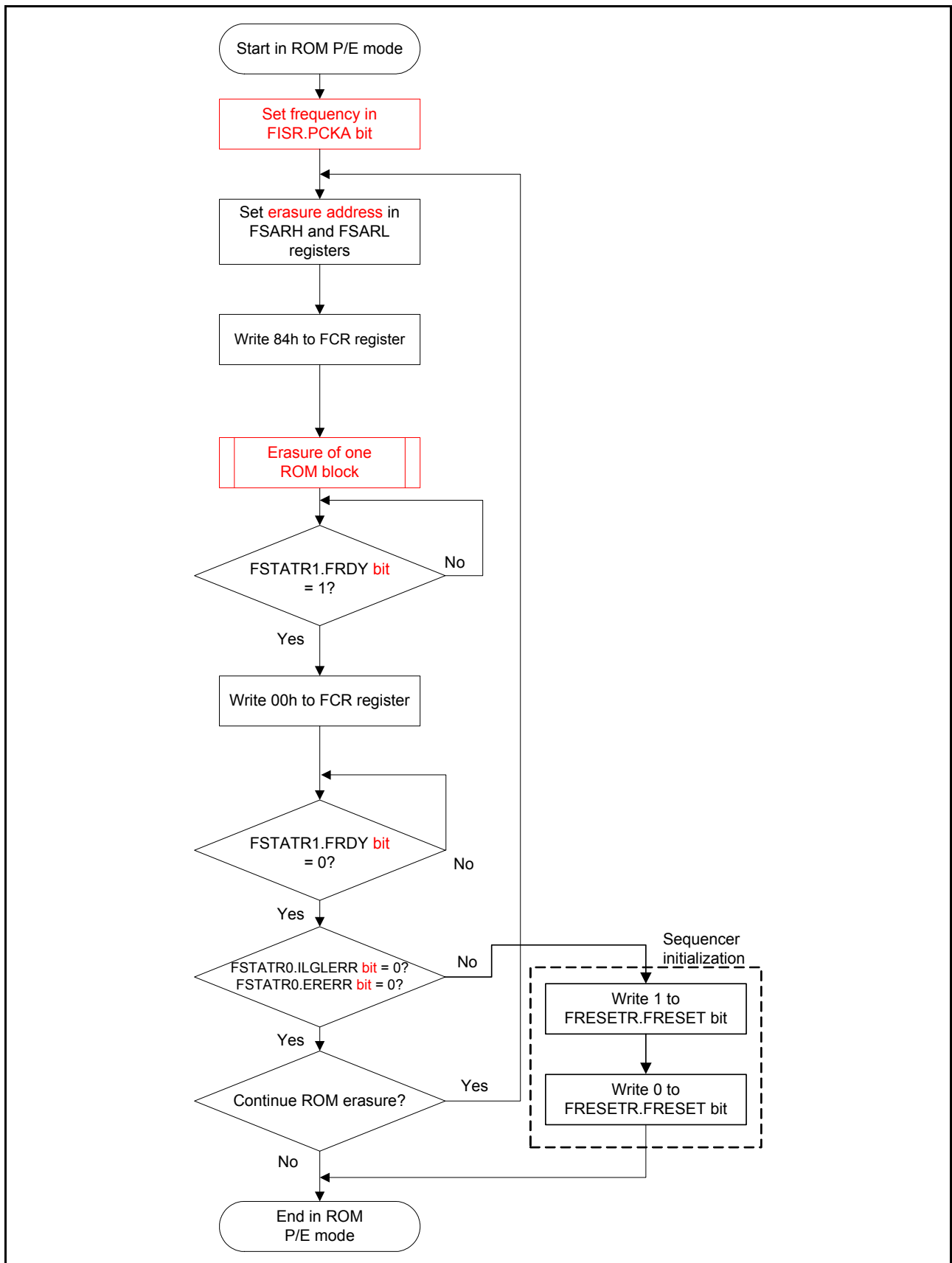
Before correction

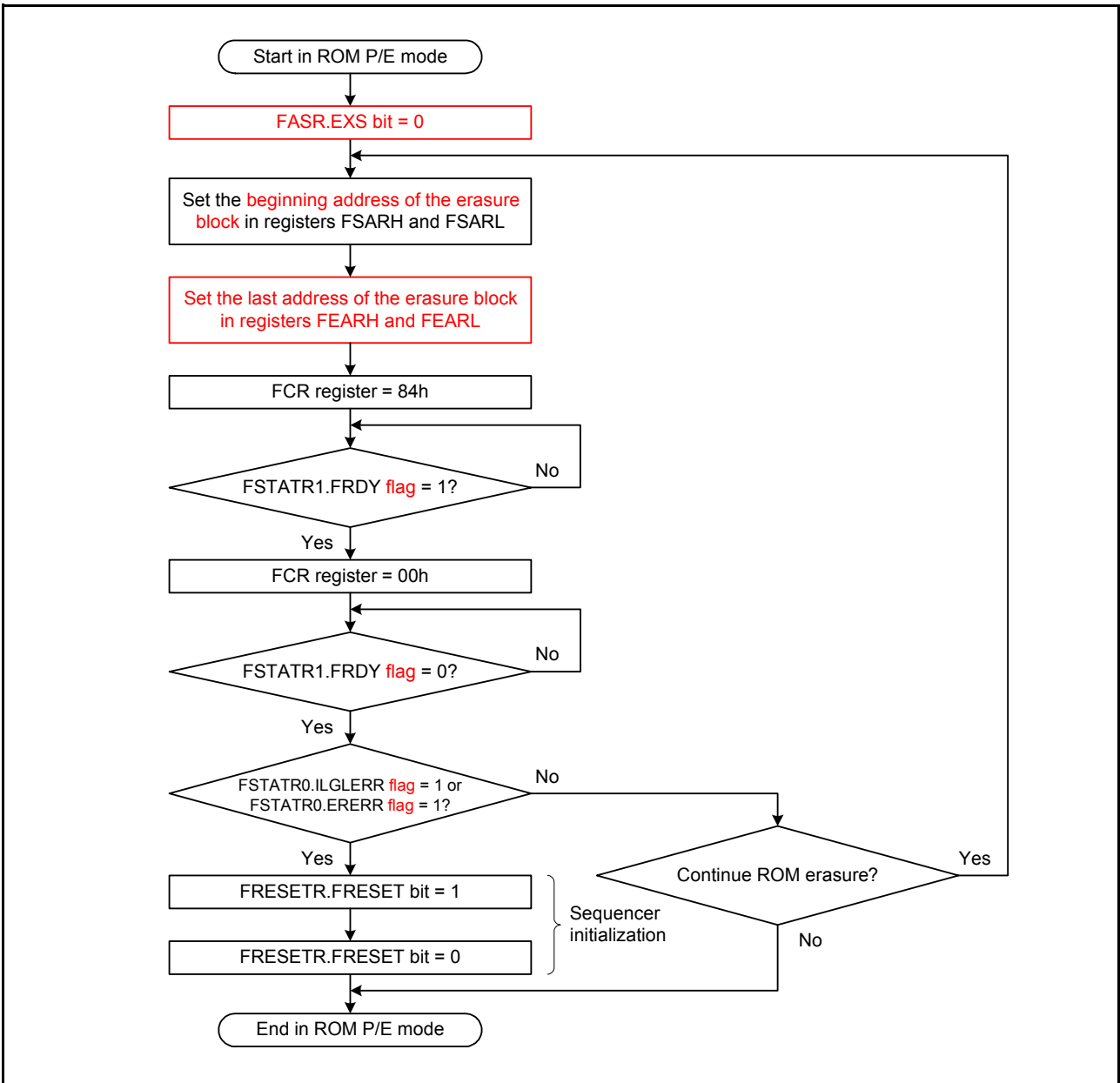**Figure 31.8   ROM Block Erase Procedure**

After correction

Figure 31.8   **Procedure to Issue the Block Erase Command for the ROM**

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 Figure 31.9 in (3) Programming and Erasure Procedures of 31.6.3 Software Command Usage is corrected as follows:
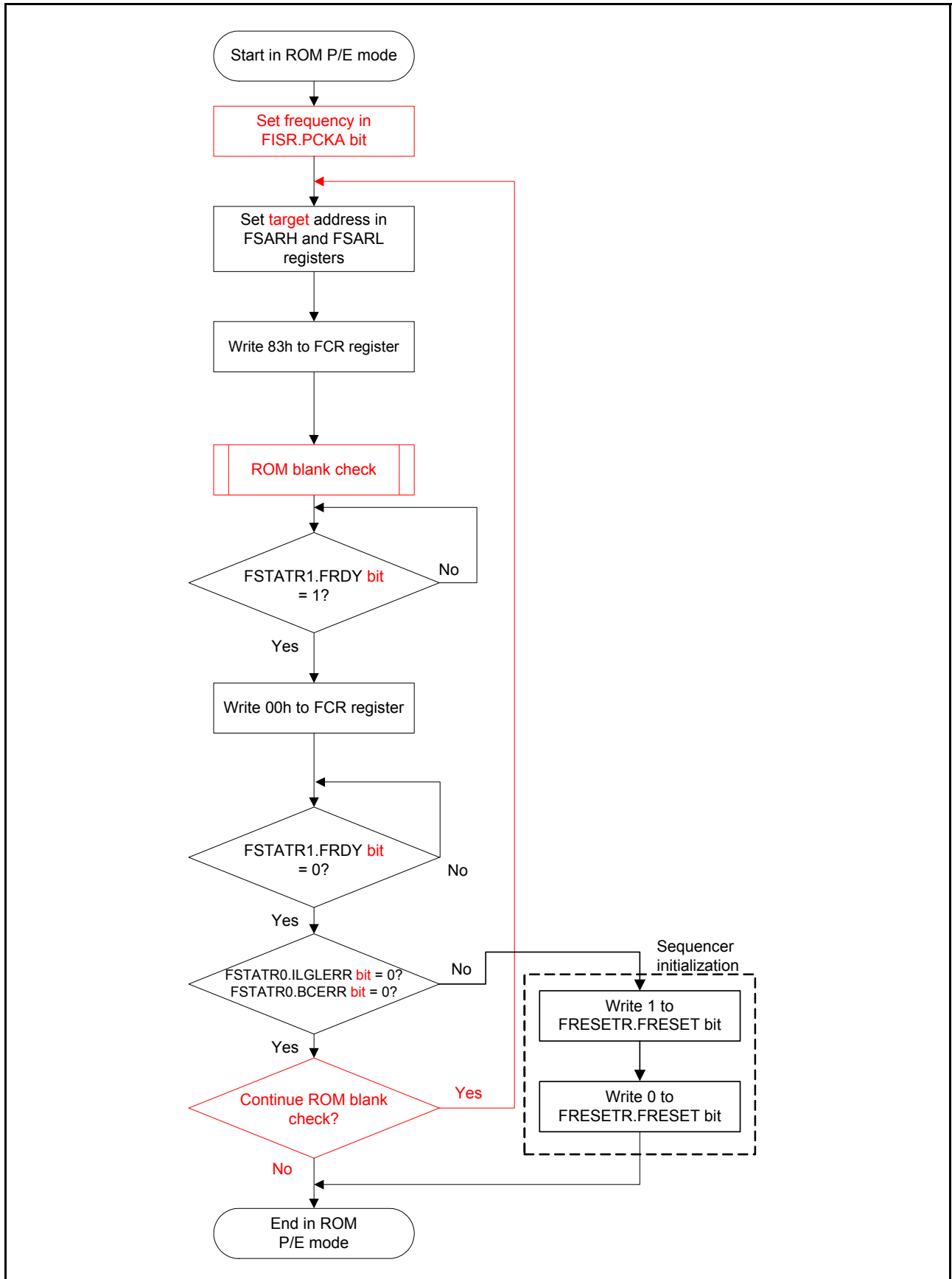
Before correction

Figure 31.9   ROM Blank Check Procedure

After correction


```
                    ( Start in ROM P/E mode )
                              │
                    ┌─────────────────────┐
                    │   FASR.EXS bit = 0   │
                    └─────────────────────┘
                              │
                    ┌─────────────────────┐
                    │ Set the blank check  │
                    │  start address in    │
                    │ registers FSARH and  │
                    │       FSARL          │
                    └─────────────────────┘
                              │
                    ┌─────────────────────┐
                    │ Set the blank check  │
                    │   end address in     │
                    │ registers FEARH and  │
                    │       FEARL          │
                    └─────────────────────┘
                              │
                    ┌─────────────────────┐
                    │  FCR register = 83h  │
                    └─────────────────────┘
                              │
                    ◇ FSTATR1.FRDY flag = 1? ◇──No──┐
                              │ Yes                  │
                              │←─────────────────────┘
                    ┌─────────────────────┐
                    │  FCR register = 00h  │
                    └─────────────────────┘
                              │
                    ◇ FSTATR1.FRDY flag = 0? ◇──No──┐
                              │ Yes                  │
                              │←─────────────────────┘
                    ◇ FSTATR0.ILGLERR flag = 1 or
                      FSTATR0.BCERR flag = 1? ◇──No──────────┐
                              │ Yes                          │
                    ┌─────────────────────┐                  │
                    │ FRESETR.FRESET bit=1 │  Sequencer       │
                    └─────────────────────┘  initialization   │
                    ┌─────────────────────┐                  │
                    │ FRESETR.FRESET bit=0 │                  │
                    └─────────────────────┘                  │
                              │←──────────────────────────────┘
                    ( End in ROM P/E mode )
```
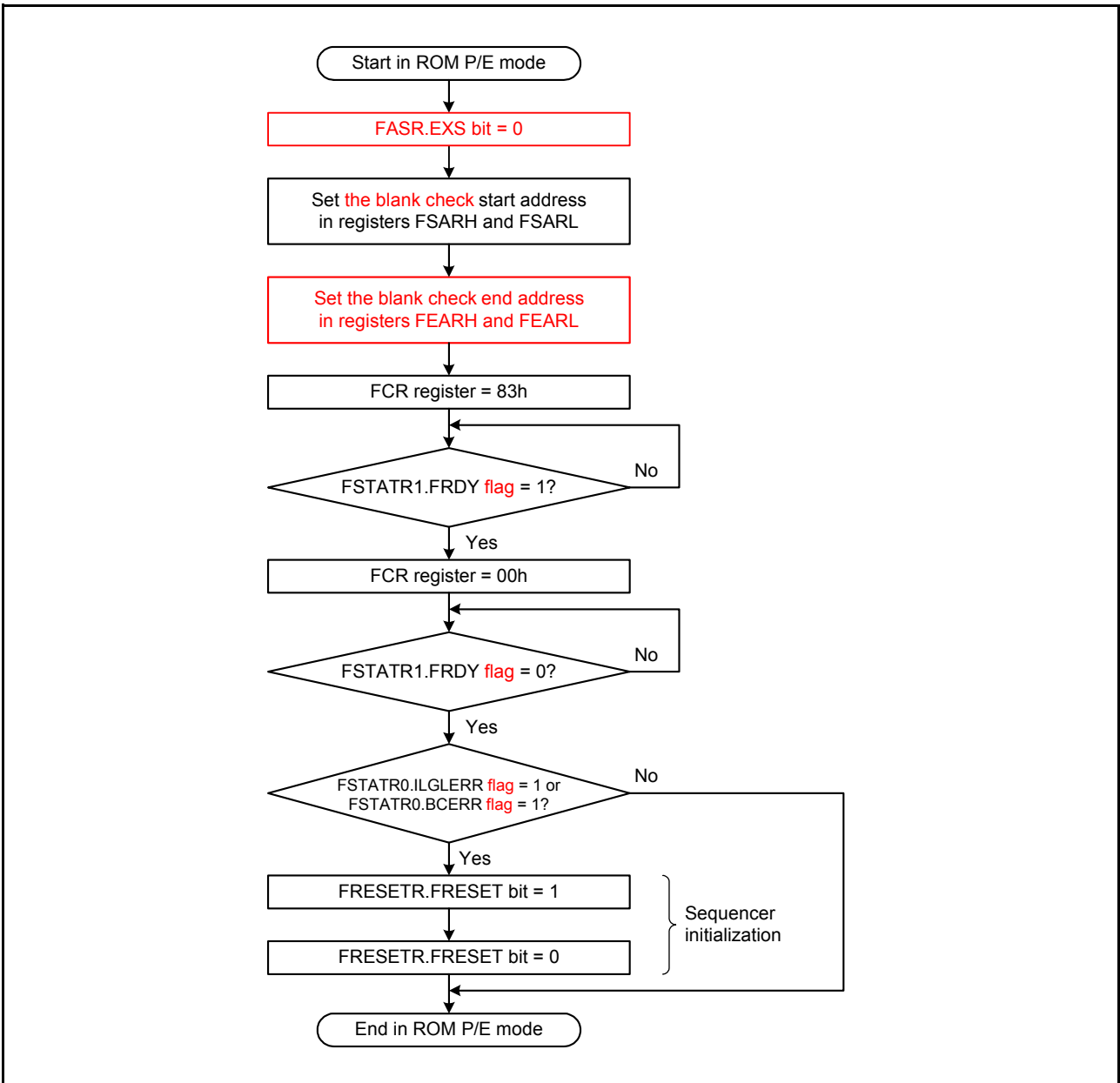
Figure 31.9   Procedure to Issue the Blank Check Command for the ROM

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Figure 31.10 in (4) Start-Up Area Information Program/Access Window Information Program of 31.6.3 Software Command Usage is corrected as follows:
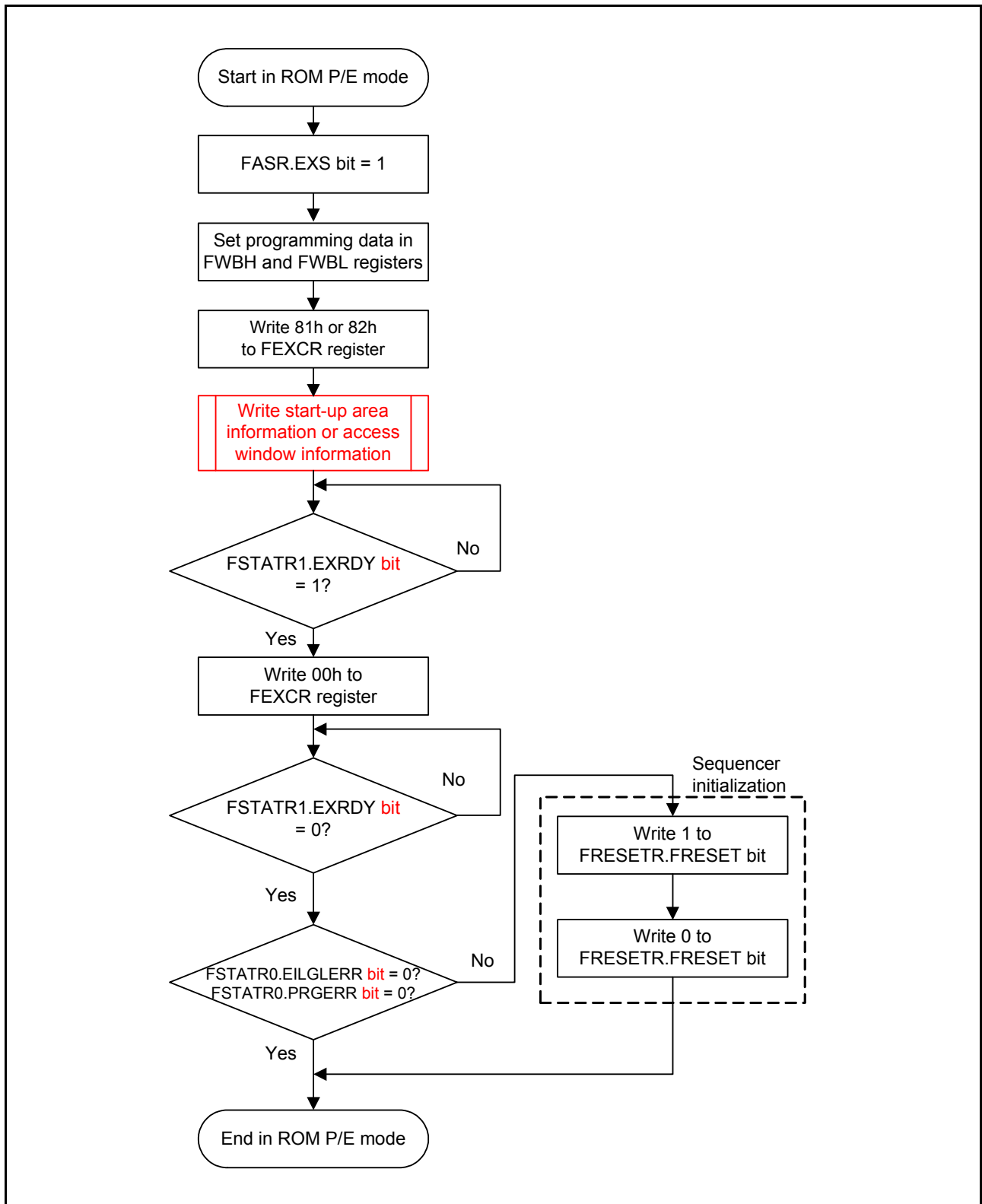
Before correction

Figure 31.10   Simple Flowchart of the Procedure for the Start-Up Area Information Program/Access Window Information Program
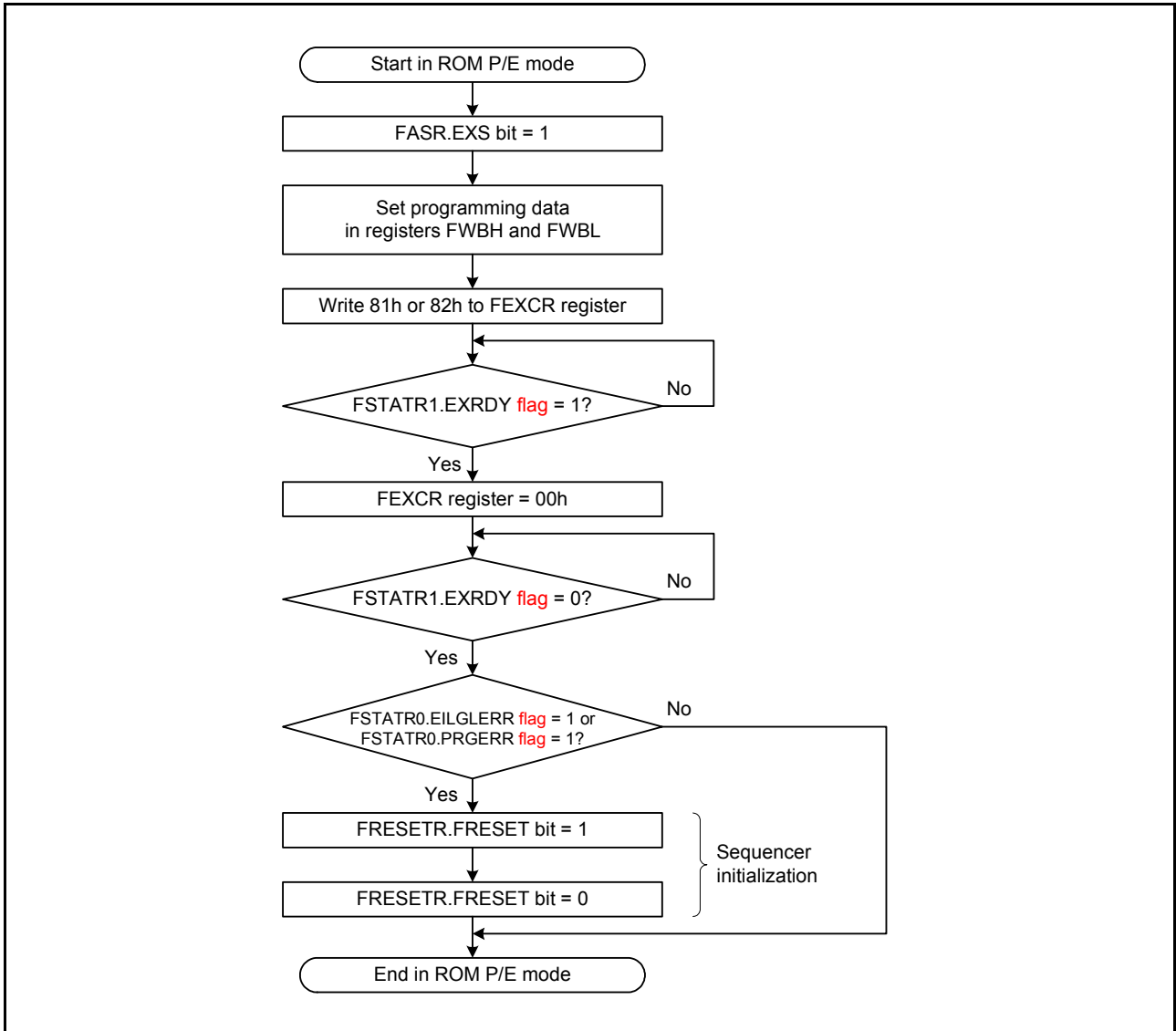
After correction

Figure 31.10   Procedure to Issue the Start-Up Area Information Program Command/Access Window Information Program Command