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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A0154A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice Descriptions of errors in the RL78/D1A User's Manual: Hardware Rev.1.10		Information Category	Technical Notification		
Applicable Product	RL78/D1A Group	Lot No. All lots	Reference Document	RL78/D1A User's Manual: Hardware Rev.1.10 (R01UH0317EJ0110)		

This document describes misstatements found in RL78/D1A User's Manual: Hardware Rev.1.10 (R01UH0317EJ0110).

Related documents:

- Published technical updates [TN-RL*-A058A/E, TN-RL*-A068A/E, TN-RL*-A0096A/E, TN-RL*-A0123A/E]
- PCN "Supplier addition on Cu wire for LQFP products" [EPPO2-EX-25-0026]

Corrections:

(1/3)

No	Corrections	R01UH0317EJ0110	Pages in this document
1	Update "1.3 Ordering Information".	P.3	P.4
2	Correct typo in the Function Table (3/4) of "1.7 Outline of Functions".	P.25	P.5
3	Correct typo in the Function Table (4/4) of "1.7 Outline of Functions".	P.26	P.5
4	Correct typo in the CAN control pin in "2.2.14 P130 to P137 (port13)".	P.62	P.5
5	Add a description of 128-pin product to "Chapter 2.2.18".	P.64	P.6
6	Add the target product to the "Table 2-7 (10/15) to (12/15)".	P.74 to P.76	P.6
7	Correct the typo in the applicable products in the "Table 3-3".	P.99, P.100	P.6
8	Correct the typo in the applicable product in the "Table 3-11".	P.106	P.6
9	Correct the typo in the applicable product in the "Table 3-19".	P.114	P.7
10	Add a description of target registers to the "(e) ISP1, ISP0".	P.116	P.7
11	Correct the typo in the "After reset" value of PM13 register in the "Table 3-5".	P.121	P.7
12	Update the "Table 3-6". (Access bit range, Typos, Add register, Reset value)	P.126, P.127, P.142	P.7
13	Add descriptions for product groups A and B.	P.164	P.7
14	Add TxD0, RxD0 pins to "Figures 4-3, 4-4, 4-8, 4-9, 4-15, 4-16, 4-43".	P.169, P.170, P.175, P.176, P.184, P.185, P.221	P.8
15	Add a description of RTC1HZ output function in the Caution to "Figure 4-11".	P.178	P.12
16	Correct a typo in the pin name of ANIxx in "Figure 4-12".	P.180	P.12
17	Correct the typo in the LCDPF4 section in "Table 4-6".	P.186	P.12
18	Correct a typo in the Caution at the bottom of "Figure 4-33".	P.207	P.12
19	Correct a typo in the SEG27 pin in "Figure 4-35".	P.209	P.13
20	Correct a typo in the Caution at the bottom of "Figure 4-37".	P.212	P.13
21	Correct a typo in the Caution at the bottom of "Figure 4-52".	P.231	P.13
22	Correct a typo in the PM15 register in "Table 4-18".	P.237	P.13
23	Update the information about Port 11 and 12 to "Table 4-19".	P.241	P.14
24	Delete the unnecessary registers PM13, PU13, PIM13, LCDPF13 from "Figures 4-58, 4-60, 4-61, 63".	P.243, P254, P.259, P.265	P.14
25	Correct a typo in the "After reset" value of PM10 register in "Figure 4-58".	P.247	P.15

(2/3)

No	Corrections	R01UH0317EJ0110	Pages in this document
26	Correct a typo in the “R/W” access of P12 register in “Figure 4-59”.	P.253	P.16
27	Update the “Figure 4-66”. (Add a description for TIS001 bit.)	P.273	P.16
28	Update the “Figure 4-67”. (Add a description for SAU0.)	P.276	P.16
29	Correct a description for TISxx and TOSxx registers in “Figure 4-68 to 4-73”.	P.278 to P.289	P.17
30	Correct a description for TISELSE register in “Figure 4-74”.	P.289	P.23
31	Correct a description for STSEL0 register in “Figure 4-75”.	P.291	P.23
32	Correct the “Table 4-23”.	P.295 to P.310	P.24
33	Correct a typo in the PLL clock description in “Chapter 5.1”.	P.312	P.30
34	Correct the description of the CMC register in “Chapter 5.3, (1)”.	P.317, P.318	P.30
35	Correct the description of the OSTC register in “Chapter 5.3, (4)”.	P.323	P.30
36	Correct the “Figure 5-19”.	P.347	P.31
37	Delete the incorrect description in “Table 5-5, (3)”.	P.348	P.31
38	Correct the incorrect “Remark” at the bottom of “Table 5-5”.	P.348 to P.352	P.31
39	Add PLL clock explanation to “Table 5-5”.	P.351, P.352	P.32
40	Add PLL clock explanation to “Table 5-6”.	P.353, P.354	P.32
41	Add PLL clock explanation to “Table 5-10”.	P.356	P.33
42	Update the “Figures 6-2, 6-4, 6-6”. (same as Figure 4-66)	P.364, P.366, P.368	P.33
43	Correct incorrect description of CKSmn[1:0] and MDmn0 bits in “Figure 6-11”.	P.376, P.378	P.36
44	Update the “Figures 6-30 to 6-35”. (same as Figures 4-68 to 4-73)	P.399 to P.410	P.37
45	Correct a description for TISELSE register in “Figure 6-36”.	P.411	P.43
46	Correct a description of SCSI00[1:0] bit in “Figure 6-37”.	P.412	P.43
47	Correct the “Table 6-5”.	P.414 to P.426	P.44
48	Add a description of combination operation in “Chapter 6.6.2”.	P.444	P.51
49	Correct the typo in CKSmn[1:0] bit of TMRmn register in “Figures 6-53, 6-57, 6-61, 6-65, 6-69, 6-73, 6-74, 6-78, 6-79, 6-83, 6-84”.	P.448, P.452, P.456, P.461, P.465, P.470, P.471, P.477, P.478, P.484, P.485	P.52
50	Correct the description of RWAIT bit of RTCC1 register in “Figure 7-7”.	P.497	P.52
51	Correct the typo in the bit diagram in “Figure 7-19”.	P.507	P.53
52	Correct the typo in the Notes at the bottom of “Figure 7-20”.	P.508	P.53
53	Add explanations for the Cautions at the bottom of “Figures 7-22 and 7-23”.	P.510, P.511	P.53
54	Correct the “Tables 9-2, 9-3”.	P.525, P.526	P.54
55	Correct the typo in the bit diagram in “Figure 9-5”.	P.527	P.54
56	Add a Note to Table 10-4 when setting WINDOW[1:0] = 10B (75%).	P.534	P.55
57	Correct the typo for A/D channel number in “Chapters 11.1, 11.2, 11.3, 11.5, 11.7, 11.10”.	P.536, P.538, P.539, P.563, P.564, P.567, P.581 to P.584, P.590, P.591, P.593	P.55
58	Update the “Figure 11-1”. (add channels ANI9 and ANI10)	P.537	P.58
59	Correct the typo in the bit diagram in “Figures 11-2, 11-3, 11-11, 11-13”.	P.541, P.542, P.558, P.560	P.58
60	Correct the item name in the table in Note 2 of the “Figure 11-4”.	P.544	P.59
61	Update the “Table 12-1”.	P.597	P.59
62	Update block diagram of serial array unit.	P.598 to P.600	P.60
63	Correct the typo for SAU channel number in “Chapters 12.2, 12.3, 12.7”.	P.602, P.609, P.720, P.724, P.728, P.734	P.63
64	Correct the description of Caution 1 in “Figure 12-6”.	P.605	P.63
65	Correct the typo in SDRmn[15:9] bit in “Figure 12-10”.	P.612	P.63
66	Correct the description of SIRmn, SSRmn registers in “Figures 12-11, 12-13”.	P.613, P.615	P.64
67	Correct the typo in after reset value of SOm register.	P.620	P.64
68	Correct the description of STSEL0 register in “Figure 12-19”.	P.622	P.64
69	Add a description of SNFEN0 register.	- (P.623)	P.65
70	Add a description of PIM11, PM11 registers.	P.624, P.625, P.627, P.628	P.65
71	Correct the typo of Note in “Tables 12-2, 12-4”.	P.692, P.735	P.66
72	Correct the port settings in the flowchart in “Figure 12-75, 12-92”.	P.698, P.721	P.67

(3/3)

No	Corrections	R01UH0317EJ0110	Pages in this document
73	Update the register conditions table for SAU.	P.738, P.740, P.743, P.744, P.748	P.67
74	Correct the “Figure 13-1”.	P.751	P.70
75	Correct the typo in after reset value of UFnOPT0 register.	P.756	P.70
76	Correct a description of UFnRX register.	P.775	P.70
77	Update the “Figures 13-30, 13-31”.	P.795, P.796	P.71
78	Correct the typo in the UFnRRQ bit name at the bottom of Figure 13-49.	P.817	P.72
79	Correct the “Figures 13-70, 13-71”.	P.838	P.72
80	Correct the typo of the PER0 register name in “Chapter 13.11”.	P.846	P.72
81	Correct the typo of the product name in “Chapter 14”.	P.847	P.73
82	Correct a typo in the C0MDB502 register address in “Table 14-16”.	P.877	P.73
83	Correct the typo in the bit diagram in “Figure 14-25”.	P.902	P.73
84	Update the “Figure 14-62”.	P.969	P.73
85	Correct the bit diagram of the PER1 register in “Figure 15-8”.	P.1016	P.74
86	Correct a typo of the pixel number for R5F10DSx product in “Table 16-1”.	P.1024	P.74
87	Update a description of the LCDPFn register in “Chapter 16.3”.	P.1031, P.1034	P.74
88	Correct a description of memory address in “Chapter 16.5”.	P.1036, P.1038	P.75
89	Correct a typo in the table in “Figure 16-27”.	P.1053	P.76
90	Correct a typo of LBCYC, LBWST registers in “Chapter 17.3”.	P.1061	P.76
91	Correct the bit diagram of the PER1 register in “Chapter 18.2”.	P.1084	P.76
92	Correct the description of interrupt related registers in “Chapter 20.6”.	P.1132	P.77
93	Correct a typo of the product information in “Chapter 21”.	P.1134	P.77
94	Correct a typo in the product name in “Table 21-1”.	P.1135, P.1136	P.77
95	Add the SRPR00 and STPR00 flags in “Figure 21-4”.	P.1144	P.77
96	Correct figure and table reference numbers in “Chapter 21”.	P.1146, P.1147, P.1149, P.1152, P.1156	P.78
97	Correct the description of interrupt related registers in “Table 21-5 and Chapter 21.4.4”.	P.1153, P.1156	P.78
98	Correct the table reference number in “Chapter 23”.	P.1177	P.79
99	Add the target registers to Table 23-2.	P.1182 to P.1188	P.79
100	Add a description of RESOC register to Chapter 23.	- (P.1190)	P.80
101	Delete the description of IEC61508 in “Chapter 26”.	P.1215, P.1220, P.1223, P.1224	P.81
102	Correct a typo of register name in “Chapter 26.2”.	P.1216, P.1230	P.81
103	Correct the typo in the access size of GUARD register in “Chapter 26.3.5.2”.	P.1225	P.82
104	Correct a typo in the memory size in “Chapter 29.4.1”.	P.1249	P.82
105	Correct the description of data flash accessing in “Chapter 29.4.3”.	P.1251	P.82
106	Correct a typo in the memory address in “Figure 30-2”.	P.1266	P.83
107	Update the product group table in “Chapters 33, 34”.	P.1292, P.1334	P.84
108	Change the chapter number in "LCD Bus Interface Characteristics".	P.1324, P.1366	P.85
109	Correct the “A/D converter characteristics”.	P.1329, P.1371	P.85
110	Correct the typo of $I_{OLTOTAL}$ for Group 3E products.	P.1350	P.85
111	Correct a typo of the condition in “Chapter 34.5.2”.	P.1359	P.85
112	Correct the max. value of the LVD detection delay time in “Chapter 34.7.4”.	P.1373	P.86
113	Update the Table of registers access wait cycles in “APPENDIX.A”.	P.1380 to P.1427	P.86

No.1: Update “1.3 Ordering Information”

[PCN: EPPO2-EX-25-0026]

Add the order name to the table. The type name to be added is shown in red characters.

[List of Part Number]

Pin count	Package	Part Number	
		Operating ambient temperature J grade (T_A = -40 to +85 °C)	Operating ambient temperature L grade (T_A = -40 to +105 °C)
48-pin	48-pin plastic LFQFP (fine pitch) (7 × 7)	R5F10CGBCJFB R5F10CGCCJFB R5F10CGDCJFB R5F10DGCCJFB R5F10DGDCJFB R5F10DGECJFB R5F10CGBJFB R5F10CGCJFB R5F10CGDJFB R5F10DGCJFB R5F10DGDJFB R5F10DGEJFB	R5F10CGBCLFB R5F10CGCCLFB R5F10CGDCLFB R5F10DGCCLFB R5F10DGDCLFB R5F10DGECLFB R5F10CGBLFB R5F10CGCLFB R5F10CGDLFB R5F10DGCLFB R5F10DGDLFB R5F10DGELFB
64-pin	64-pin plastic LFQFP (fine pitch) (10 × 10)	R5F10CLDCJFB R5F10DLDCJFB R5F10DLECJFB R5F10CLDJFB R5F10DLDJFB R5F10DLEJFB	R5F10CLDCLFB R5F10DLDCLFB R5F10DLECLFB R5F10CLDLFB R5F10DLDLFB R5F10DLELFB
80-pin	80-pin plastic LFQFP (fine pitch) (12 × 12)	R5F10CMDCJFB R5F10CMECJFB R5F10DMDCJFB R5F10DMECJFB R5F10DMFCJFB R5F10DMGCJFB R5F10DMJCJFB R5F10CMDJFB R5F10CMEJFB R5F10DMDJFB R5F10DMEJFB R5F10DMFJFB R5F10DMGJFB R5F10DMJJFB	R5F10CMDCLFB R5F10CMECLFB R5F10DMDCLFB R5F10DMECLFB R5F10DMFCLFB R5F10DMGCLFB R5F10DMJCLFB R5F10CMDLFB R5F10CMELFB R5F10DMDLFB R5F10DMELFB R5F10DMFLFB R5F10DMGLFB R5F10DMJLFB
100-pin	100-pin plastic LFQFP (fine pitch) (14 × 14)	R5F10DPECJFB R5F10DPFCJFB R5F10DPGCJFB R5F10DPJCJFB R5F10TPJCJFB R5F10DPKJFB R5F10DPLJFB R5F10DPEJFB R5F10DPFJFB R5F10DPGJFB R5F10DPJJFB R5F10TPJJFB	R5F10DPECLFB R5F10DPFCLFB R5F10DPGCLFB R5F10DPJCLFB R5F10TPJCLFB R5F10DPKLFB R5F10DPLLFB R5F10DPELFB R5F10DPFLFB R5F10DPGLFB R5F10DPJLFB R5F10TPJLFB
128-pin	128-pin plastic LFQFP (fine pitch) (14 × 20)	R5F10DSJJFB R5F10DSKJFB R5F10DSLJFB	R5F10DSJLFB R5F10DSKLFB R5F10DSLLFB

No.2: Correct typo in the Function Table (3/4) of “1.7 Outline of Functions”

Correct the typos in items “Reset output” and “STOP status output” of function table. These features are only available in 128-pin product.

(3/4)

Item			100-pin							128-pin		
	ROM	RAM	R5F10DPE	R5F10DPF	R5F10DPG	R5F10TPJ	R5F10DPJ	R5F10DPK	R5F10DPL	R5F10DSJ	R5F10DSK	R5F10DSL
Reset output			—							Can be output from P130		
STOP status output			—							Can be output from P41		

No.3: Correct typo in the Function Table (4/4) of “1.7 Outline of Functions”

Correct the typo in item “Vectored interrupt sources: Internal” of function table. The number of interrupt sources for R5F10DPE, R5F10DPF, R5F10DPG, and R5F10TPJ products is 49, not 53.

(4/4)

Item		100-pin							128-pin		
		R5F10DPE	R5F10DPF	R5F10DPG	R5F10TPJ	R5F10DPJ	R5F10DPK	R5F10DPL	R5F10DSJ	R5F10DSK	R5F10DSL
Vectored interrupt sources	Internal	~~53~~ 49				53					
	External	8									
	Software	1									
	Debugger	1									

No.4: Correct typo in the CAN control pin in “2.2.14 P130 to P137 (port13)”

There is an error in the corresponding product. The error is shown in red characters.

2.2.14 P130 to P137 (port13)

(2) Control mode

(m) CTxD1 (P134) (~~R5F10DPJxFB and R5F10DSJxFB only~~ R5F10DPJ, R5F10DPK, R5F10DPL, R5F10DSJ, R5F10DSK and R5F10DSL only)

This is a CAN serial transmit data output pin of aFCAN1.

(n) CRxD1 (P135) (~~R5F10DPJxFB and R5F10DSJxFB only~~ R5F10DPJ, R5F10DPK, R5F10DPL, R5F10DSJ, R5F10DSK and R5F10DSL only)

This is a CAN serial receive data input pin of aFCAN1.

No.5: Add a description of 128-pin product to “Chapter 2.2.18”

Add a description in red characters.

2.2.14 V_{DD}, EV_{DD0}, EV_{DD1}, SMV_{DD0}, SMV_{DD1}, V_{SS}, EV_{SS0}, EV_{SS1}, SMV_{SS0}, SMV_{SS1}

(1) V_{DD}, EV_{DD}, EV_{DD0}, EV_{DD1}

When using the 48-pin products, V_{DD} is the positive power supply pin for P20 to P23, P27, P121 to P122, P137, $\overline{\text{RESET}}$. When using the 64-pin products, V_{DD} is the positive power supply pin for P20 to P23, P27, P121 to P124, P137, $\overline{\text{RESET}}$. When using the 80-pin products, V_{DD} is the positive power supply pin for P20 to P27, P121 to P124, P137, $\overline{\text{RESET}}$. When using the 100-pin products, V_{DD} is the positive power supply pin for P20 to P27, P121 to P124, P137, P150, $\overline{\text{RESET}}$. When using the 128-pin products, V_{DD} is the positive power supply pin for P20 to P27, P121 to P124, P137, P150 to P152, $\overline{\text{RESET}}$.

EV_{DD}, EV_{DD0}, EV_{DD1} are the positive power supply pins for the other than V_{DD}, SMV_{DD}, SMV_{DD0}, SMV_{DD1}.

(2) SMV_{DD}, SMV_{DD0}, SMV_{DD1}

When using the 48-pin products, SMV_{DD} is the positive power supply pin for P80 to P83, P90 to P94. When using the 64-pin products, SMV_{DD} is the positive power supply pin for P80 to P87, P90 to P94. When using the 80-pin, 100-pin and 128-pin products, SMV_{DD0}, SMV_{DD1} are the positive power supply pins for P80 to P87, P90 to P97.

(3) V_{SS}, EV_{SS}, EV_{SS0}, EV_{SS1}

When using the 48-pin products, V_{SS} is the ground potential pin for P20 to P23, P27, P121 to P122, P137, $\overline{\text{RESET}}$. When using the 64-pin products, V_{SS} is the ground potential pin for P20 to P23, P27, P121 to P124, P137, $\overline{\text{RESET}}$. When using the 80-pin products, V_{SS} is the ground potential pin for P20 to P27, P121 to P124, P137, $\overline{\text{RESET}}$. When using the 100-pin products, V_{SS} is the ground potential pin for P20 to P27, P121 to P124, P137, P150, $\overline{\text{RESET}}$. When using the 128-pin products, V_{SS} is the ground potential pin for P20 to P27, P121 to P124, P137, P150 to P152, $\overline{\text{RESET}}$.

EV_{SS}, EV_{SS0}, EMV_{SS1} are the ground potential pins for the other than V_{SS}, SMV_{SS}, SMV_{SS0}, SMV_{SS1}.

(4) SMV_{SS}, SMV_{SS0}, SMV_{SS1}

When using the 48-pin products, SMV_{SS} is the ground potential pin for P80 to P83, P90 to P94. When using the 64-pin products, SMV_{SS} is the ground potential pin for P80 to P87, P90 to P94. When using the 80-pin, 100-pin, and 128-pin products, SMV_{SS0}, SMV_{SS1} are the ground potential pins for P80 to P87, P90 to P97.

No.6: Add the target product to the “Table 2-7”

Add the product name for the target product (Table title). Changes are shown in red characters.

Table 2-7. Connection of Unused Pins (10/15), (11/15), (12/15)
(e) ~~R5F10DPJxFB~~ R5F10DPJ, R5F10DPK, R5F10DPL (1/3), (2/3), (3/3)

No.7: Correct the typo in the applicable products in the “Table 3-3”

Changes are shown in red characters.

Table 3-3. Vector Table (1/2), (2/2)

Vector Table Address	Interrupt Source	48-pin		64-pin		80-pin		100-pin			128-pin
		R5F10CGx	R5F10DGx	R5F10CLx	R5F10DLx	~~R5F10DSx~~	R5F10CMx	R5F10DMx	~~R5F10TPx/~~ ~~R5F10DPx~~ R5F10TPJ/ R5F10DPG/ R5F10DPF/ R5F10DPE	~~R5F10DPJ~~	R5F10DPL/ R5F10DPK/ R5F10DPJ	R5F10DSx

No.8: Correct the typo in the applicable product in the “Table 3-11”

Correct the product name for the target product (Table title). Changes are shown in red characters.

Figure 3-11. Correspondence Between Data Memory and Addressing
(~~R5F10CGD~~ R5F10CGB)

No.9: Correct the typo in the applicable product in the “Table 3-19”.

Correct the product name for the target product (Table title). Changes are shown in red characters.

Figure 3-19. Correspondence Between Data Memory and Addressing
(~~R5F10DSL, R5F10DP~~ R5F10DPL, R5F10DSL)

No.10: Add a description of target registers to the “(e) ISP1, ISP0”

Add a description in red characters.

3.2.1 Control registers

(e) In-service priority flags (ISP1, ISP0)

This flag manages the priority of acknowledgeable maskable vectored interrupts. Vectored interrupt requests specified lower than the value of ISP0 and ISP1 flags by the priority specification flag registers (PRn0L, PRn0H, PRn1L, PRn1H, PRn2L, PRn2H, PRn3L, PRn3H) (see **21.3 (3)**) cannot be acknowledged. Actual request acknowledgment is controlled by the interrupt enable flag (IE).

No.11: Correct the typo in the “After reset” value of PM13 register in the “Table 3-5”.

Changes are shown in red characters.

Table 3-5. SFR List (2/5)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset
				1-bit	8-bit	16-bit	
FFF2DH	Port mode register 13	PM13	R/W	√	√	–	~~FFH~~ FEH

No.12: Update the “Table 3-6” (Access bit range, Typos, Add register, Reset value)

Changes are shown in red characters.

Table 3-6. Extended SFR (2nd SFR) List (1/21), (2/21), (17/21)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset
				1-bit	8-bit	16-bit	
F0019H	~~LCB~~ LCD Bus Interface cycle control register Note	LBCYC	R/W	~~√~~ –	√	–	02H
F001AH	~~LCB~~ LCD Bus Interface wait control register Note	LBWST	R/W	~~√~~ –	√	–	00H
F006DH	Noise filter enable register for SAU Note 2	SNFEN0	R/W	√	√	–	00H
F05F4H	CAN0 module transmit history list register	C0TGPT	R/W	–	–	√	~~xx2H~~ xx02H

Note 2. 128-pin products only.

No.13: Add descriptions for product groups A and B

4.1 Port Functions

Definition of Product Groups

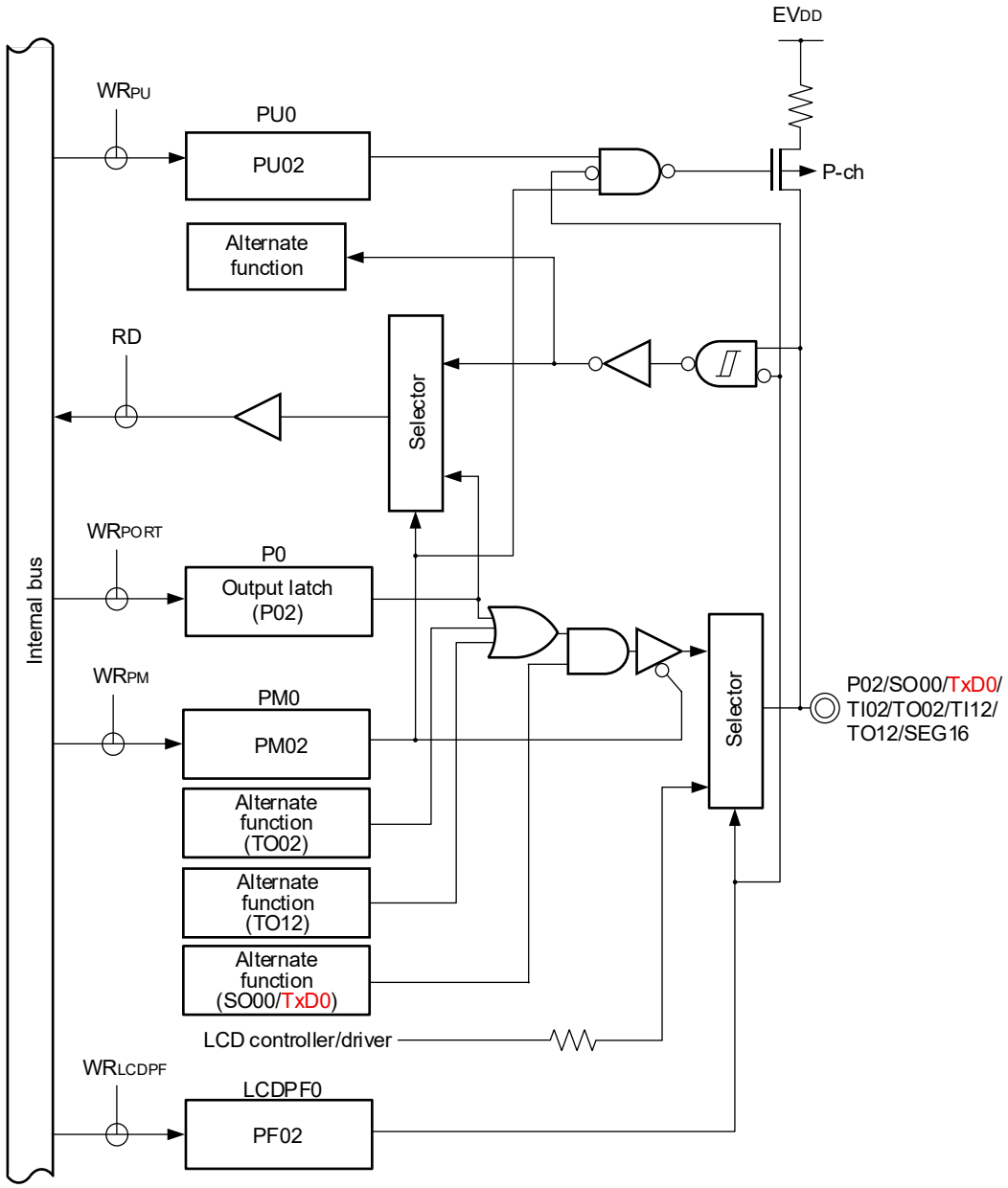
Definition of product groups described in this chapter is shown in the following table.

Product groups	Product names				
	48-pin products	64-pin products	80-pin products	100-pin products	128-pin products
Product Group A	R5F10CGB R5F10CGC R5F10CGD R5F10DGC R5F10DGD R5F10DGE	R5F10CLD R5F10DLD R5F10DLE	R5F10CMD R5F10CME R5F10DMD R5F10DME R5F10DMF R5F10DMG R5F10DMJ	R5F10DPE R5F10DPF R5F10DPG R5F10DPJ R5F10TPJ	–
Product Group B	–	–	–	R5F10DPK R5F10DPL	R5F10DSJ R5F10DSK R5F10DSL

No.14: Add TxD0, RxD0 pins to “Figures 4-3, 4-4, 4-8, 4-9, 4-15, 4-16, 4-43”

Add TxD0, RxD0 (UART0 transmission/reception pin) to the port block diagram. Also, add a description of TxD0 function to the “Caution” at the bottom of the figure. Changes are shown in red characters.

Figure 4-3. Block Diagram of P02



Caution When using the alternate function TO02 or TO12, set the port latch to 0.
When using the alternate function SO00/TxD0, set the port latch to 1.
When using P02 as a general-purpose port, specify the port settings so that the alternate function outputs are fixed (Timer to 0 and Serial to 1).

Figure 4-4. Block Diagram of P03

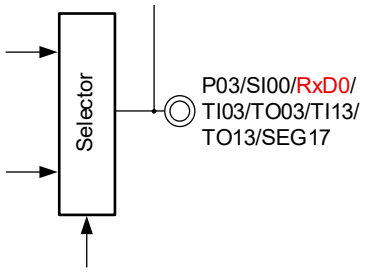


Figure 4-8. Block Diagram of P11, P17

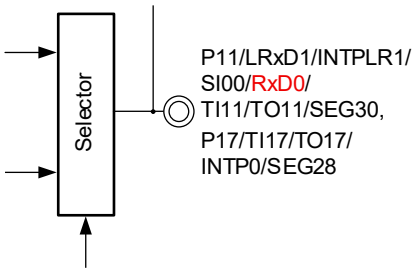
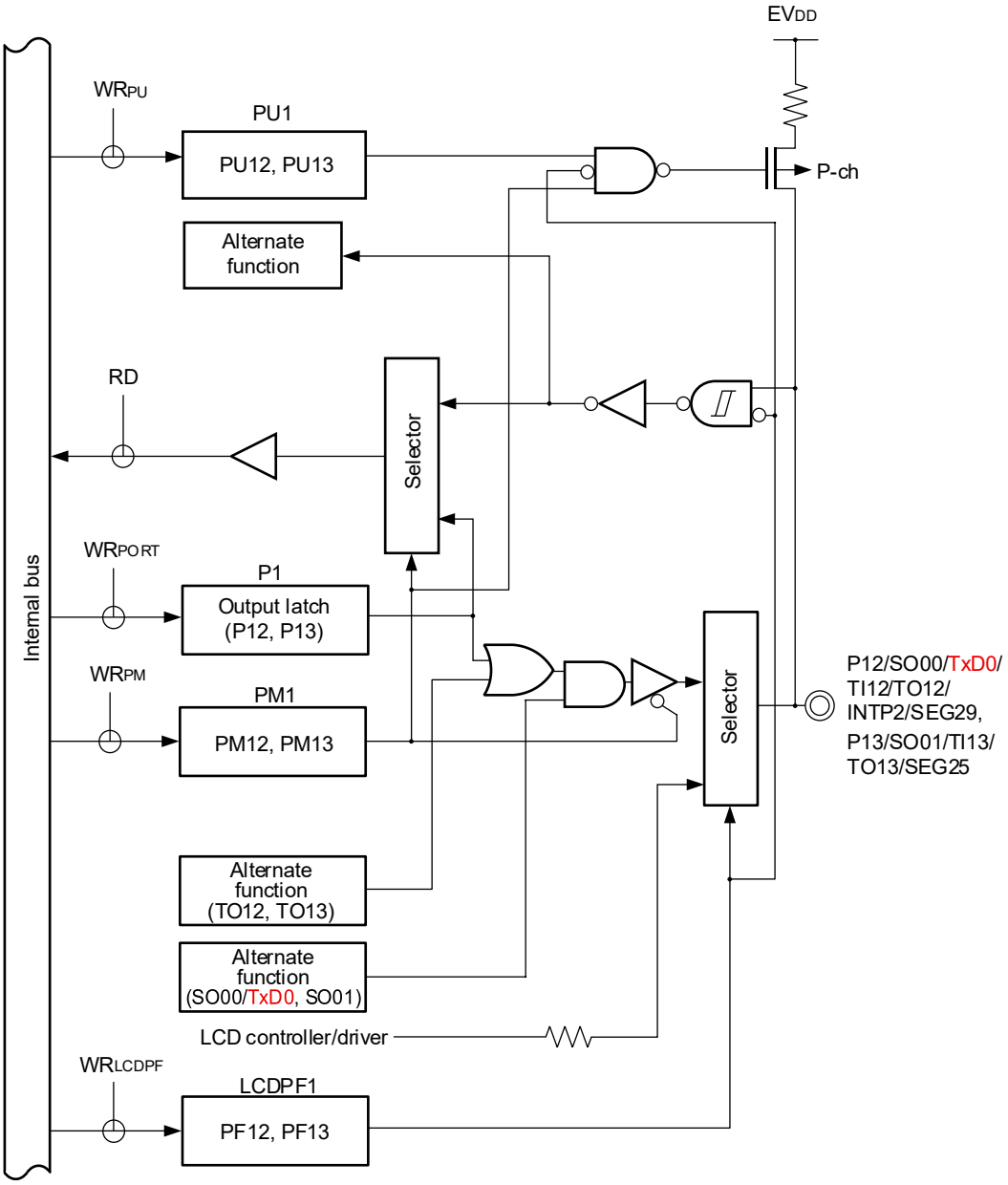
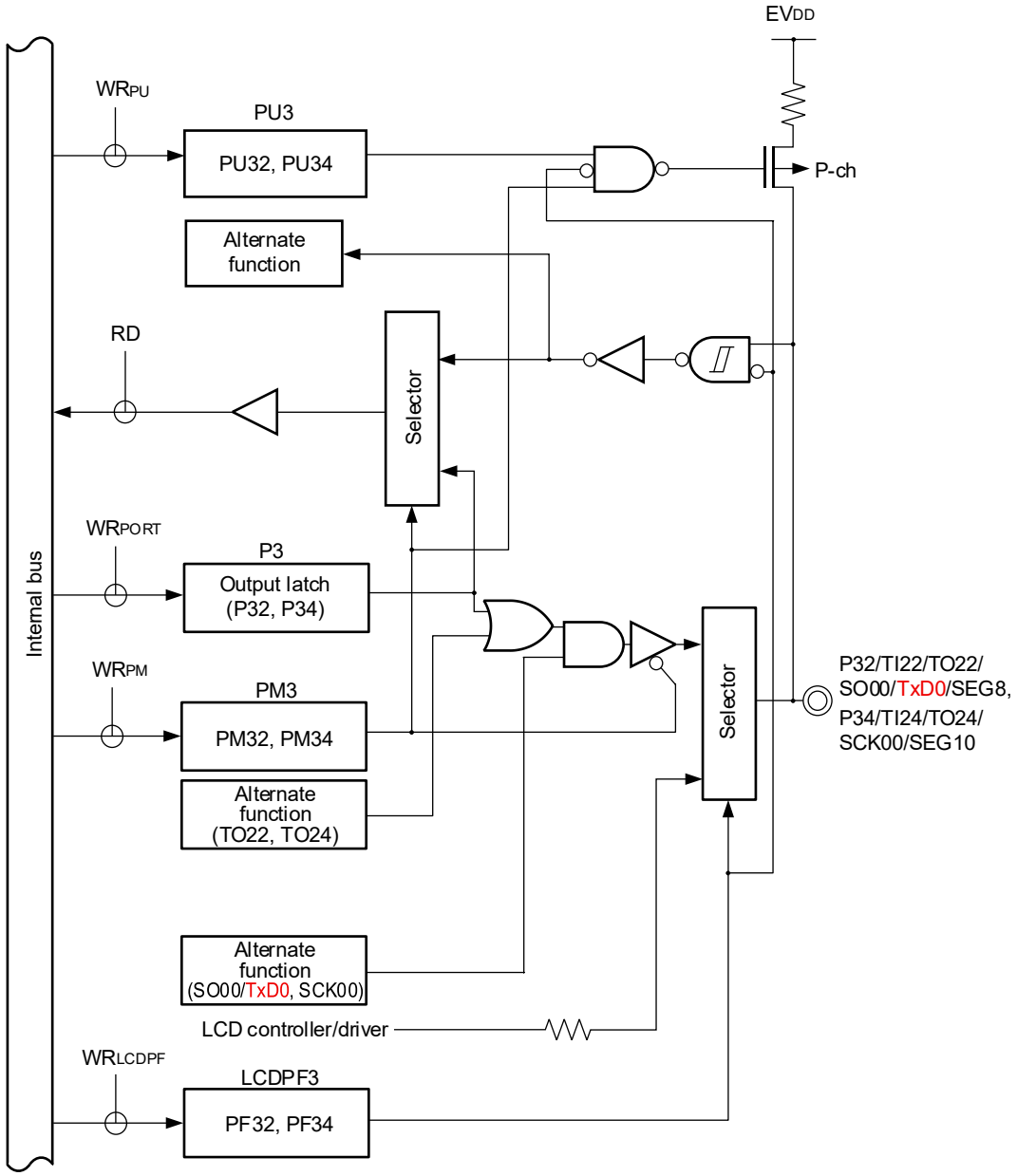


Figure 4-9. Block Diagram of P12, P13



Caution When using the alternate function TO12 or TO13, set the port latch to 0.
When using the alternate function SO00/TxD0 or SO01, set the port latch to 1.
When using P12 or P13 as a general-purpose port, specify the port settings so that the alternate function outputs are fixed (Timer to 0 and Serial to 1).

Figure 4-15. Block Diagram of P32, P34



Caution When using the alternate function TO22 or TO24, set the port latch to 0.
When using the alternate function SO00/TxD0 or SCK00, set the port latch to 1.
When using P32 or P34 as a general-purpose port, specify the port settings so that the alternate function outputs are fixed (Timer to 0 and Serial to 1).

Figure 4-16. Block Diagram of P33, P35 to P37

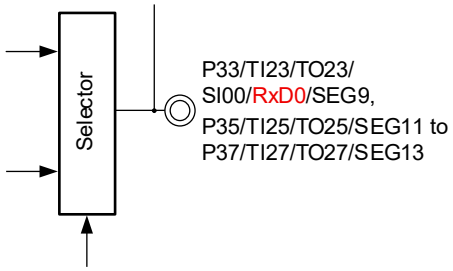
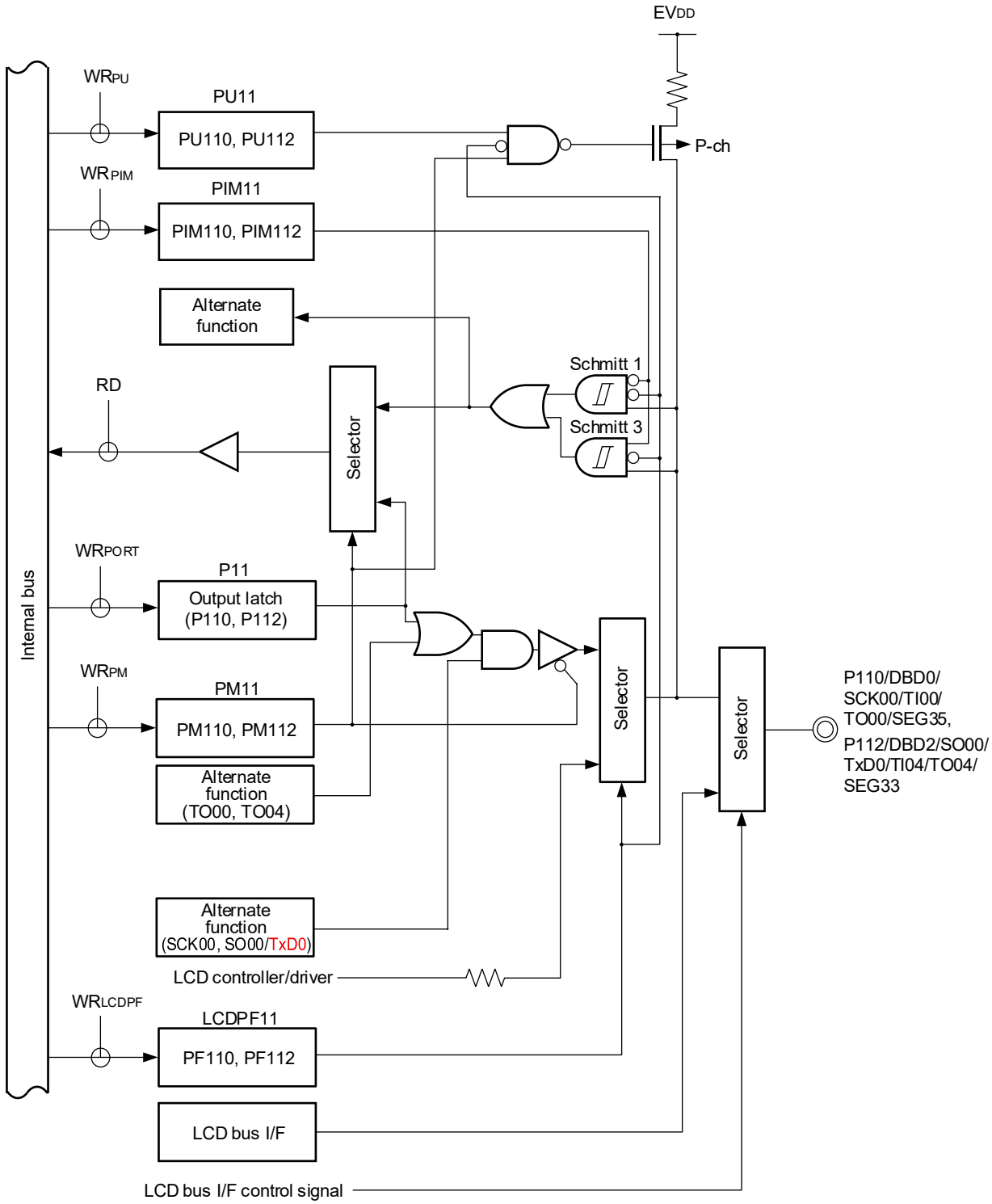


Figure 4-43. Block Diagram of P110, P112



No.15: Add a description of RTC1HZ output function in the Caution to “Figure 4-11”

Add a description of RTC1HZ output function to the “Caution” at the bottom of the figure. Changes are shown in red characters.

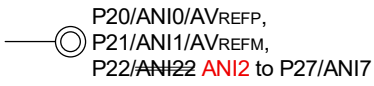
Figure 4-11. Block Diagram of P15

Caution When using the alternate function TO15 or RTC1HZ, set the port latch to 0.
When using the alternate function LTxD0, set the port latch to 1.
When using P15 as a general-purpose port, specify the port settings so that the alternate function outputs are fixed (Timer to 0 and Serial to 1).

No.16: Correct a typo in the pin name of ANIxx in “Figure 4-12”

Changes are shown in red characters.

Figure 4-20. Block Diagram of P20 to P27



No.17: Correct the typo in the LCDPF4 section in “Table 4-6”

Changes are shown in red characters.

Table 4-6. Setting of P40 to P47 Pins to port function

P40 to P47 Pins		LCDPF4	Alternate function		PM4	PIM4	POM	Remarks
port	function	Register	Timer	Serial	Register	Register	Register	
P40	Input port	~~Digital I/O selection~~ N/A	N/A	N/A	Input mode	N/A	N/A	
	Output port				Output mode			
P41	Input port	~~Digital I/O selection~~ N/A	-	N/A	Input mode	N/A	N/A	
	Output port		0		Output mode			

Reset signal generation sets ~~port 0~~ port 4 to input mode.
Figures 4-17 to 4-20 show block diagrams of port 4.

No.18: Correct a typo in the Caution at the bottom of “Figure 4-33”

Changes are shown in red characters.

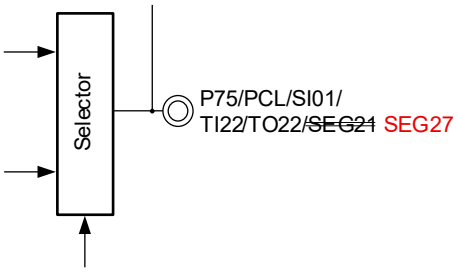
Figure 4-33. Block Diagram of P72, P73

Caution When using the alternate function ~~SGOA, SGO/SGOF, or TO22~~ SGOA or SGO/SGOF, set the port latch to 0.
When using P72 or P73 as a general-purpose port, specify the port settings so that the alternate function output is fixed to 0.

No.19: Correct a typo in the SEG27 pin in “Figure 4-35”

Changes are shown in red characters.

Figure 4-35. Block Diagram of P75



No.20: Correct a typo in the Caution at the bottom of “Figure 4-37”

Changes are shown in red characters.

Figure 4-37. Block Diagram of P83, P87

Caution When using the alternate function SM14, ~~SM18~~ SM24, TO07, or TO17 set the port latch to 0.
When using P83 or P87 as a general-purpose port, specify the port settings so that the alternate function outputs are fixed 0.

No.21: Correct a typo in the Caution at the bottom of “Figure 4-52”

Changes are shown in red characters.

Figure 4-52. Block Diagram of P134

Caution When using the alternate function TO24 or SGOA, set the port latch to 0.
When using the alternate function CTxD1, set the port latch to 1.
When using P134 as a general-purpose port, specify the port settings so that the alternate function outputs are fixed (Timer to 0 and Serial to 1).

No.22: Correct a typo in the PM15 register in “Table 4-18”.

Changes are shown in red characters.

Table 4-18. Setting of P150 to P152 Pins

P150 Pin		ADPC Register	~~PM2~~ PM15 Register	Remarks
port	function			
P150	Input port	0001 to 1001	Input mode	
	Output port		Output mode	
P151	Input port	0001 to 1010	Input mode	
	Output port		Output mode	
P152	Input port	0001 to 1011	Input mode	
	Output port		Output mode	

No.23: Update the information about Port 11 and 12 to "Table 4-19"

Change the “PIMxx register” for Port 11 from “N/A” to “PIM11x”. Also, add the information for P125, P126, and P127 to the table. Changes are shown in red characters.

Table 4-19. Pxx, PMxx, PUxx, PIMxx, POM, LCDPFxx registers and the bits mounted on each products (3/4)

Port		Bit name						128-pin	100-pin	80-pin	64-pin	48-pin
		Pxx register	PMxx register	PUxx register	PIMxx register	POM register	LCDPFxx register					
Port 11	0	P110	PM110	PU110	~~N/A~~ PIM110	N/A	LCDPF110	√	N/A	N/A	N/A	N/A
	1	P111	PM111	PU111	~~N/A~~ PIM111		LCDPF111	√	N/A	N/A	N/A	N/A
	2	P112	PM112	PU112	~~N/A~~ PIM112		LCDPF112	√	N/A	N/A	N/A	N/A
	3	P113	PM113	PU113	~~N/A~~ PIM113		LCDPF113	√	N/A	N/A	N/A	N/A
	4	P114	PM114	PU114	~~N/A~~ PIM114		LCDPF114	√	N/A	N/A	N/A	N/A
	5	P115	PM115	PU115	~~N/A~~ PIM115		LCDPF115	√	N/A	N/A	N/A	N/A
	6	P116	PM116	PU116	~~N/A~~ PIM116		LCDPF116	√	N/A	N/A	N/A	N/A
	7	P117	PM117	PU117	~~N/A~~ PIM117		LCDPF117	√	N/A	N/A	N/A	N/A
Port 12	1	P121	N/A	N/A	N/A	N/A	N/A	√	√	√	√	√
	2	P122						√	√	√	√	√
	3	P123						√	√	√	√	N/A
	4	P124						√	√	√	√	N/A
	5	P125	PM125	PU125			LCDPF125	√	N/A	N/A	N/A	N/A
	6	P126	PM126	PU126			LCDPF126	√	N/A	N/A	N/A	N/A
	7	P127	PM127	PU127			LCDPF127	√	N/A	N/A	N/A	N/A

No.24: Delete the unnecessary registers PM13, PU13, PIM13, LCDPF13

Changes are shown in red characters.

Figure 4-58. Format of Port Mode Register (1/5)
(48-pin products)

PM9	1	1	1	PM94	PM93	PM92	PM91	PM90	FFF29	FFH	R/W
~~PM13~~	~~1~~	~~1~~	~~1~~	~~1~~	~~1~~	~~1~~	~~1~~	~~1~~	~~FFF2D~~	~~FEH~~	~~R/W~~

PMmn	Pmn pin I/O mode selection (~~m = 0 to 9 and 13~~ m = 0 to 9 ; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Caution Be sure to set bits 2 to 7 of the PM0 register, bits 5 to 7 of the PM1 register, bits 4 to 6 of the PM2 register, bits 2 and 4 to 7 of the PM3 register, bits 1 to 7 of the PM4 register, bits 0 to 3 of the PM5 register, bits 2 to 7 of the PM6 register, bits 0 to 1 and 6 to 7 of the PM7 register, bits 4 to 7 of the PM8 register, ~~bits 5 to 7 of the PM9 register and bits 0 to 7 of the PM13 register to “1”~~ and bits 5 to 7 of the PM9 register to “1”.

Figure 4-60. Format of Pull-up resistor option Register (1/5)
(48-pin products)

PU9	0	0	0	PU94	PU93	PU92	PU91	PU90	F0039	00H	R/W
~~PU13~~	~~0~~	~~0~~	~~0~~	~~0~~	~~0~~	~~0~~	~~0~~	~~0~~	~~FFF2D~~	~~FEH~~	~~R/W~~

PUmn	Pmn pin on-chip pull-up resistor selection (~~m = 0 to 9 and 13~~ m = 0 to 9 ; n = 0 to 7)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Figure 4-61. Format of Port input mode Register (1/5)
(48-pin products)

PIM7	0	0	0	0	0	0	0	0	F0047	00H	R/W
~~PIM13~~	~~0~~	~~0~~	~~0~~	~~0~~	~~0~~	~~0~~	~~0~~	~~0~~	~~F004D~~	~~00H~~	~~R/W~~

PMmn	PIMmn pin input threshold selection (~~m = 0, 1, 3, 5 to 7, and 13~~ m = 0, 1, 3, 5 to 7 ; n = 0 to 7)
0	Schmit1 input mode
1	Schmit3 input mode

Figure 4-63. Format of LCD port function Register (1/5)
(48-pin products)

LCDPF9	0	0	0	LCDPF94	LCDPF93	LCDPF92	LCDPF91	LCDPF90	F0059	00H	R/W
~~LCDPF13~~	~~0~~	~~0~~	~~0~~	~~0~~	~~0~~	~~0~~	~~0~~	~~0~~	~~F005D~~	~~00H~~	~~R/W~~

LCDPFmn	LCDPFmn register function (~~m = 0, 1, 3, 5, 7 to 9, 13~~ m = 0, 1, 3, 5, 7 to 9, 13 ; n = 0 to 7)
0	Used as port or alternate function other than segment output
1	Used as LCD segment signal output

No.25: Correct a typo in the after reset value of PM10 register in “Figure 4-58”

Changes are shown in red characters.

Figure 4-58. Format of Port Mode Register (5/5)
(128-pin products)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM9	PM97	PM96	PM95	PM94	PM93	PM92	PM91	PM90	FFF29	FFH	R/W
PM10	PM107	PM106	PM105	PM104	PM103	PM102	PM101	PM100	FFF2A	~~FEH~~ FFH	R/W

No.26: Correct a typo in the “R/W” access of P12 register in “Figure 4-59”

Changes are shown in red characters.

Figure 4-59. Format of Port Mode Register (5/5)

(128-pin products)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
P12	P127	P126	P125	P124	P123	P122	P121	0	FFF0C	00H	~~Read only~~ R/W Note 2
P13	P137	P136	P135	P134	P133	P132	P131	P130	FFF0D	00H	R/W ~~Note~~ Note 1

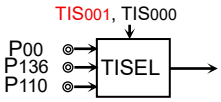
Notes 1. P137 is read only.

2. P121 to P124 are read only.

No.27: Update the “Figure 4-66”

Changes are shown in red characters.

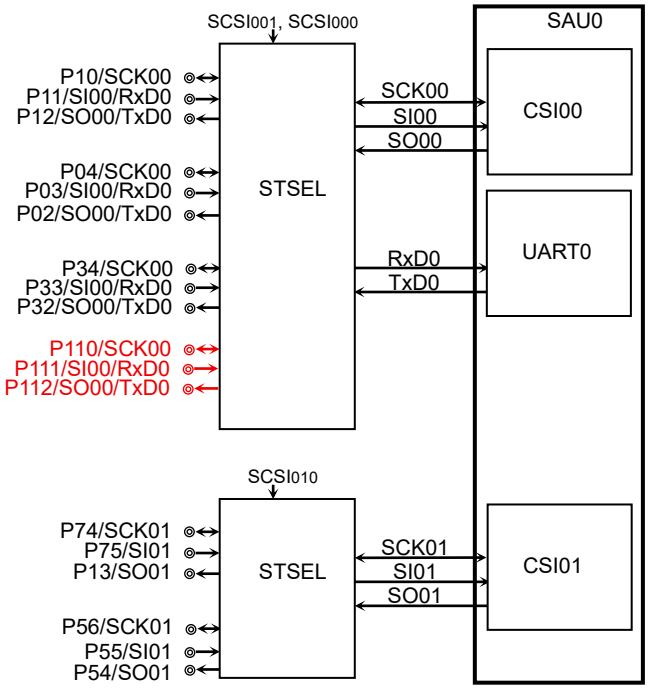
Figure 4-66. Timer Array unit and RTC I/O connection (128-pin products) (1/3)



No.28: Update the “Figure 4-67”

Changes are shown in red characters.

Figure 4-67. Serial unit, SG, and PCL connection (128-pin products) (1/2)



No.29: Correct a description for TISxx and TOSxx registers in “Figure 4-68 to 4-73”

Changes are shown in red characters.

Figure 4-68. Format of TIS00 and TIS01 Registers ~~(128-pin products)~~

TIS001	TIS000	TI00 (TAU unit0 CH0) alternate pin selection
0	0	P00
0	1	P136
1	0	P110 Note 1
~~Other than the above~~		~~Setting prohibited (same as “00” setting)~~
1	1	Setting prohibited (same as “10” setting) Note 1

TIS011	TIS010	TI01 (TAU unit0 CH1) alternate pin selection
0	0	P01
0	1	P80
1	0	P94
1	1	P104 Note 2

TIS021	TIS020	TI02 (TAU unit0 CH2) alternate pin selection
0	0	P02
0	1	P50
1	0	P105 Note 1
1	1	P111 Note 1

TIS041	TIS040	TI04 (TAU unit0 CH4) alternate pin selection
0	0	P04
0	1	P51
1	0	P112 Note 1
1	1	P41 Note 1

TIS051	TIS050	TI05 (TAU unit0 CH5) alternate pin selection
0	0	P05
0	1	P82
1	0	P96
1	1	P106 Note 2

TIS061	TIS060	TI06 (TAU unit0 CH6) alternate pin selection
0	0	P06
0	1	P52
1	0	P107 Note 1
1	1	P113 Note 1

TIS071	TIS070	TI07 (TAU unit0 CH7) alternate pin selection
0	0	P07
0	1	P83
1	0	P97
1	1	P114 Note 2

Notes 1. This bit is only available for Group B products.

2. "Setting prohibited (same as “00” setting)" for Group A products.

Remark For Groups A and B products, see "**Definition of Product Groups**" in Chapter 4.1.

Figure 4-69. Format of TIS10 and TIS11 Registers ~~(128-pin products)~~

TIS101	TIS100	TI10 (TAU unit1 CH0) alternate pin selection
0	0	P10 Note 1
0	1	P115 Note 1
1	0	P42 Note 1
1	1	Setting prohibited (same as “10” setting) Note 1

TIS121	TIS120	TI12 (TAU unit1 CH2) alternate pin selection
0	0	P12
0	1	P02
1	0	P125 Note 1
1	1	P116 Note 1

TIS141	TIS140	TI14 (TAU unit1 CH4) alternate pin selection
0	0	P14
0	1	P04
1	0	P54
1	1	P126 Note 2

TIS161	TIS160	TI16 (TAU unit1 CH6) alternate pin selection
0	0	P16
0	1	P06
1	0	P56
1	1	P127 Note 2

Notes 1. This bit is only available for Group B products.

2. "Setting prohibited (same as “00” setting)" for Group A products.

Remark For Groups A and B products, see "**Definition of Product Groups**" in Chapter 4.1.

Figure 4-70. Format of TIS20 and TIS21 Registers ~~(128-pin products)~~

TIS201	TIS200	~~TI21 (TAU unit2 CH1)~~ TI20 (TAU unit2 CH0) alternate pin selection
0	0	P60
0	1	P30
1	0	P132
1	1	P117 Note

TIS221	TIS220	TI22 (TAU unit2 CH2) alternate pin selection
0	0	P75
0	1	P32
1	0	P133
1	1	P43 Note

TIS231	TIS230	TI23 (TAU unit2 CH3) alternate pin selection
0	0	P74
0	1	P33
1	0	P91
1	1	P44 Note

TIS241	TIS240	TI24 (TAU unit2 CH4) alternate pin selection
0	0	P66
0	1	P34
1	0	P134
1	1	P100 Note

TIS251	TIS250	TI25 (TAU unit2 CH5) alternate pin selection
0	0	P65
0	1	P92
1	0	P35
1	1	P101 Note

TIS261	TIS260	TI26 (TAU unit2 CH6) alternate pin selection
0	0	P63
0	1	P36
1	0	P135
1	1	P102 Note

TIS271	TIS270	TI27 (TAU unit2 CH7) alternate pin selection
0	0	P93
0	1	P62
1	0	P37
1	1	P103 Note

Note "Setting prohibited (same as “00” setting)" for Group A products.

Remark For Groups A products, see "**Definition of Product Groups**" in Chapter 4.1.

Figure 4-71. Format of TOS00 and TOS01 Registers ~~(128-pin products)~~

TOS001	~~TIS000~~ TOS000	TO00 (TAU unit0 CH0) alternate pin selection
0	0	P00
0	1	P136
1	0	P110 Note 1
~~Other than the above~~		~~Setting prohibited (same as "00" setting)~~
1	1	Setting prohibited (same as "10" setting) Note 1

TOS011	TOS010	TO01 (TAU unit0 CH1) alternate pin selection
0	0	P01
0	1	P80
1	0	P94
1	1	P104 Note 2

TOS021	TOS020	TO02 (TAU unit0 CH2) alternate pin selection
0	0	P02
0	1	P50
1	0	P105 Note 1
1	1	P111 Note 1

TOS041	TOS040	TO04 (TAU unit0 CH4) alternate pin selection
0	0	P04
0	1	P51
1	0	P112 Note 1
1	1	P41 Note 1

TIS051	TIS050	TI05 (TAU unit0 CH5) alternate pin selection
0	0	P05
0	1	P82
1	0	P96
1	1	P106 Note 2

TOS061	TOS060	TO06 (TAU unit0 CH6) alternate pin selection
0	0	P06
0	1	P52
1	0	P107 Note 1
1	1	P113 Note 1

TOS071	TOS070	TO07 (TAU unit0 CH7) alternate pin selection
0	0	P07
0	1	P83
1	0	P97
1	1	P114 Note 2

Notes 1. This bit is only available for Group B products.

2. "Setting prohibited (same as "00" setting)" for Group A products.

Remark For Groups A and B products, see "**Definition of Product Groups**" in Chapter 4.1.

Figure 4-72. Format of TOS10 and TOS11 Registers ~~(128-pin products)~~

TOS101	TOS100	TI10 (TAU unit1 CH0) alternate pin selection
0	0	P10 Note 1
0	1	P115 Note 1
1	0	P42 Note 1
~~Other than the above~~		~~Setting prohibited (same as “00” setting)~~
1	1	Setting prohibited (same as “10” setting) Note 1

TOS121	TOS120	TO12 (TAU unit1 CH2) alternate pin selection
0	0	P12
0	1	P02
1	0	P125 Note 1
1	1	P116 Note 1

TOS141	TOS140	TO14 (TAU unit1 CH4) alternate pin selection
0	0	P14
0	1	P04
1	0	P54
1	1	P126 Note 2

TOS161	TOS160	TO16 (TAU unit1 CH6) alternate pin selection
0	0	P16
0	1	P06
1	0	P56
1	1	P127 Note 2

Notes 1. This bit is only available for Group B products.

2. "Setting prohibited (same as “00” setting)" for Group A products.

Remark For Groups A and B products, see "**Definition of Product Groups**" in Chapter 4.1.

Figure 4-73. Format of TOS20 and TOS21 Registers ~~(128-pin products)~~

TOS201	TOS200	TO20 (TAU unit2 CH0) alternate pin selection
0	0	P60
0	1	P30
1	0	P132
1	1	P117 Note

TOS221	TOS220	TO22 (TAU unit2 CH2) alternate pin selection
0	0	P75
0	1	P32
1	0	P133
1	1	P43 Note

TOS231	TOS230	TO23 (TAU unit2 CH3) alternate pin selection
0	0	P74
0	1	P33
1	0	P91
1	1	P44 Note

TOS241	TOS240	TO24 (TAU unit2 CH4) alternate pin selection
0	0	P66
0	1	P34
1	0	P134
1	1	P100 Note

TOS251	TOS250	TO25 (TAU unit2 CH5) alternate pin selection
0	0	P65
0	1	P92
1	0	P35
1	1	P101 Note

TOS261	TOS260	TO26 (TAU unit2 CH6) alternate pin selection
0	0	P63
0	1	P36
1	0	P135
1	1	P102 Note

TOS271	TOS270	TO27 (TAU unit2 CH7) alternate pin selection
0	0	P93
0	1	P62
1	0	P37
1	1	P103 Note

Note "Setting prohibited (same as “00” setting)" for Group A products.

Remark For Groups A products, see "**Definition of Product Groups**" in Chapter 4.1.

No.30: Correct a description for TISELSE register in “Figure 4-74”

Changes are shown in red characters.

Figure 4-74. Format of TISELSE Registers

TI05SEL1	TI05SEL0	TIS051	TIS050	TAU unit0 CH5 input alternate selection
0	0	0	0	P05
0	0	0	1	P82
0	0	1	0	P96
0	0	1	1	P106 Note
0	1	x	x	Low-speed on-chip clock (f_{IL})
1	0	x	x	Sub system clock (f_{SUB})
1	1	x	x	Main external clock (f_{EX})
Other than the above				Setting prohibited (same as “0000” setting)

Note "Setting prohibited (same as “0000” setting)" for Group A products.

Remark For Groups A and B products, see "**Definition of Product Groups**" in Chapter 4.1.

No.31: Correct a description for STSEL0 register in “Figure 4-75”

Changes are shown in red characters.

Figure 4-75. Format of STSEL0 Register

SUARTF0	Communication pin selection of UARTF0	
	LTxD0	LRxD0/INTPLR0
0	P71	P70
1	P15	P14

SUARTF1	Communication pin selection of UARTF1	
	LTxD1	LRxD1/INTPLR1
0	P10	P11
1	P131	P132

SCSI001	SCSI000	CSI00 communication pin selection			UART0 pin selection	
		SCK00	SI00	SO00	RxD0	TxD0
0	0	P10	P11	P12	P11 Note1	P12 Note1
0	1	P04	P03	P02	P03 Note1	P02 Note1
1	0	P34	P33	P32	P33 Notie1	P32 Note1
1	~~0~~ 1	P110 Notes1,2	P111 Notes1,2	P112 Notes1,2	P111 Note1	P112 Note1

Notes 1. 128-pin products only ~~(same as “00” setting for other products)~~.

2. "Setting prohibited (same as “00” setting)" for Group A products.

Remark For Group A products, see "**Definition of Product Groups**" in Chapter 4.1.

No.32: Correct the “Table 4-23”

Changes are shown in red characters.

Table 4-23. Settings of Register, and Output Latch When Using Alternate Function

(a) Alternate function of P0

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P00	TI00	Input	1	x	0	~~TIS00.0 = 0~~ TIS00.[1:0] = 00 TISELSE.6 = 0	-
	TO00	Output	0	0	0	TOS00.[1:0] = 00	STSEL1.2 = 0
	CTxD0	Output	0	1	0	STSEL1.2 = 1	TOS00.[1:0] = 01/10
	SEG14	Output	x	x	1	-	-
P02	TI02	Input	1	x	0	~~TIS00.4 = 0~~ TIS00.[5:4] = 00	-
	TO02	Output	0	0	0	~~TOS00.4 = 0~~ TOS00.[5:4] = 00	STSEL0.[3:2] = 00/10/11 ~~TOS10.4 = 0~~ TOS10.[5:4] = 00/10/11
	TI12	Input	1	x	0	~~TIS10.4 = 1~~ TIS10.[5:4] = 01	-
	TO12	Output	0	0	0	~~TOS10.4 = 1~~ TOS10.[5:4] = 01	STSEL0.[3:2] = 00/10/11 ~~TOS00.4 = 0~~ TOS00.[5:4] = 01/10/11
	SO00	Output	0	1	0	STSEL0.[3:2] = 01	TOS00.[5:4] = 01/10/11 TOS10.[5:4] = 00/10/11
	TxD0	Output					
P03	SI00	Input	1	x	0	STSEL0.[3:2] = 01	-
	RxD0	Input					
P04	TI04	Input	1	x	0	~~TIS01.0 = 0~~ TIS01.[1:0] = 00	
	TO04	Output	0	0	0	~~TOS01.0 = 0~~ TOS01.[1:0] = 00	STSEL0.[3:2] = 00/10/11 TOS11.[1:0] = 00/10/11
	TO14	Output	0	0	0	TOS11.[1:0] = 01	STSEL0.[3:2] = 00/10/11 ~~TOS01.0 = 1~~ TOS01.[1:0] = 01/10/11
	SCK00	Output	0	1	0	STSEL0.[3:2] = 01	TOS01.[1:0] = 01/10/11 TOS11.[1:0] = 00/10/11
		Input	1	x			-
P05	TO15	Output	0	0	0	TOS11.[3:2] = 01	TOS01.[3:2] = 01/10/11
P06	TI06	Input	1	x	0	~~TIS01.4 = 0~~ TIS01.[5:4] = 00 RTCSEL.0 = 0	-
	TO06	Output	0	0	0	~~TOS01.4 = 0~~ TOS01.[5:4] = 00	TOS11.[5:4] = 00/10/11
	TO16	Output	0	0	0	TOS11.[5:4] = 01	~~TOS01.4 = 1~~ TOS01.[5:4] = 01/10/11
P07	TO17	Output	0	0	0	TOS11.[7:6] = 01	TOS01.[7:6] = 01/10/11

Table 4-23. Settings of Register, and Output Latch When Using Alternate Function

(b) Alternate function of P1

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P10	TI10	Input	1	x	0	TIS10.[1:0] = 00	-
	TO10	Output	0	0	0	TOS10.[1:0] = 00	STSEL0.1 = 1 STSEL0.[3:2] = 01/10/11
	LTxD1	Output	0	1	0	STSEL0.1 = 0	TOS10.[1:0] = 01/10 STSEL0.[3:2] = 01/10/11
	SCK00	Output	0	1	0	STSEL0.[3:2] = 00	TOS10.[1:0] = 01/10 STSEL0.1 = 1
		Input	1	x			-
P11	SI00	Input	1	x	0	STSEL0.[3:2] = 00	-
	RxD0	Input					
P12	TI12	Input	1	x	0	~~TIS10.4 = 0~~ TIS10.[5:4] = 00	-
	TO12	Output	0	0	0	~~TOS10.4 = 0~~ TOS10.[5:4] = 00	STSEL0.[3:2] = 01/10/11
	SO00	Output	0	1	0	STSEL0.[3:2] = 00	~~TOS10.4 = 1~~ TOS10.[5:4] = 01/10/11
	TxD0	Output					
P17	TO17	Output	0	0	0	TOS11.[7:6] = 00	~~STSEL0.3,2 = 01/10~~ -

(c) Alternate function of P2

port	Alternate function		PMxx	Pxx	ADPC (bit 3 to 0)
	Function name	I/O			
P20	AVREFP	Input	— 1	— x	0000/0010 to ~~1001~~ 1011
	ANI0	Input	— 1	— x	
P21	AVREFM	Input	— 1	— x	0000/0011 to ~~1001~~ 1011
	ANI1	Input	— 1	— x	
P22	ANI2	Input	— 1	— x	0000/0100 to ~~1001~~ 1011
P23	ANI3	Input	— 1	— x	0000/0101 to ~~1001~~ 1011
P24	ANI4	Input	— 1	— x	0000/0110 to ~~1001~~ 1011
P25	ANI5	Input	— 1	— x	0000/0111 to ~~1001~~ 1011
P26	ANI6	Input	— 1	— x	~~0000/1000/1001~~ 0000/1000 to 1011
P27	ANI7	Input	— 1	— x	~~0000/1001~~ 0000/1001 to 1011

Table 4-23. Settings of Register, and Output Latch When Using Alternate Function

(d) Alternate function of P3

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P30	SCL11	Output	0	1	0	STSEL1.[7:6] = 01	TOS20.[1:0] = 00/10/11
P32	TO22	Output	0	0	0	TOS20.[5:4] = 01	STSEL0.[3:2] = 00/01/11
	SO00	Output	0	1	0	STSEL0.[3:2] = 10	TOS20.[5:4] = 00/10/11
	TxD0	Output					
P33	TO23	Output	0	0	0	TOS20.[7:6] = 01	~~STSEL0.3,2 = 00/01~~ -
	SI00	Input	1	x	0	STSEL0.[3:2] = 10	~~TOS20.7,6 = 00/10~~ -
	RxD0	Input					
P34	TO24	Output	0	0	0	TOS21.[1:0] = 01	STSEL0.[3:2] = 00/01/11
	SCK00	Output	0	1	0	STSEL0.[3:2] = 10	TOS21.[1:0] = 00/10/11
		Input	1	x			-
P35	TO25	Output	0	0	0	TOS21.[3:2] = 10	~~STSEL0.3,2 = 00/01~~ -

(e) Alternate function of P4

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P41	TI04	Input	1	x	~~0~~ N/A	TIS01.[1:0] = 11	-
	TO04	Output	0	0		TOS01.[1:0] = 11	~~-~~ STPSTC.STPOEN = 0
	STOPST	Output	0	0		-	~~-~~ TOS01.[1:0] = 00/01/10
P47	$\overline{\text{DBRD}}$	~~Input~~ Output	0	1	0	-	-

(f) Alternate function of P5

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P50	TI02	Input	1	x	0	~~TIS00.4 = 1~~ TIS00.[5:4] = 01	-
	TO02	Output	0	0	0	~~TOS00.4 = 1~~ TOS00.[5:4] = 01	STSEL1.[7:6] = 00/01
	SDA11	I/O	0	1	0	STSEL1.[7:6] = 10	~~TOS00.4 = 0~~ TOS00.[5:4] = 00/10/11
P51	TI04	Input	1	x	0	~~TIS01.0 = 1~~ TIS01.[1:0] = 01	-
	TO04	Output	0	0	0	~~TOS01.0 = 1~~ TOS01.[1:0] = 01	STSEL0.6 = 0
	SCK10	Output	0	1	0	STSEL0.6 = 1	~~TOS01.0 = 0~~ TOS01.[1:0] = 00/10/11
		Input	1	x			-
P52	TI06	Input	1	x	0	~~TIS01.4 = 1~~ TIS01.[5:4] = 01 RTCSEL.0 = 0	-
	TO06	Output	0	0	0	~~TOS01.4 = 1~~ TOS01.[5:4] = 01	-
P54	TO14	Output	0	0	0	TOS11.[1:0] = 10	STSEL0.4 = 0
	SO01	Output	0	1	0	STSEL0.4 = 1	TOS11.[1:0] = 00/01/11
P56	SCK01	Output	0	1	0	STSEL0.4 = 1	TOS11.[5:4] = 00/01/11
		Input	1	x			-

Table 4-23. Settings of Register, and Output Latch When Using Alternate Function

(g) Alternate function of P6

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P60	SCL11	Output	0	1	N/A	STSEL1.[7:6] = 00	TOS20.[1:0] = 01/10/11
P62	CTxD1	Output	0	1	N/A	STSEL1.3 = 0	TOS21.[7:6] = 00/01/11
P66	PCL	Output	0	0	N/A	SGSEL.3 = 1	TOS21.[1:0] = 01/10/11

(h) Alternate function of P7

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P71	LTxD0	Output	0	1	N/A	STSEL0.0 = 0	~~STSEL1.3 = 1~~ STSEL1.2 = 1
P73	SGO/SGOF	Output	0	0	0	SGSEL.[2:0] = 000/100	-
P74	SCK01	Output	0	1	0	STSEL0.4 = 0	TOS20.[7:6] = 01/10/11
		Input	1	x			-
P75	PCL	Output	0	0	0	SGSEL.3 = 0	TOS20.[5:4] = 01/10/11

(i) Alternate function of P8

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P80	SM11	Output	0	0	0	SMPC.0 = 1	TOS00.[3:2] = 00/10/11
P82	SM13	Output	0	0	0	SMPC.0 = 1	TOS01.[3:2] = 00/10/11
P83	SM14	Output	0	0	0	SMPC.0 = 1	TOS01.[7:6] = 00/10/11

(j) Alternate function of P9

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P91	SM32	Output	0	0	0	SMPC.2 = 1	TOS20.[7:6] = 00/01/11
P92	SM33	Output	0	0	0	SMPC.2 = 1	TOS21.[3:2] = 00/10/11 SGSEL.[2:0] = 000/010/100/ 101/110
	SGOA	Output	0	0	0	SGSEL.[2:0] = 001	SMPC.2 = 0 TOS21.[3:2] = 00/10/11
P93	TO27	Output	0	0	0	TOS21.[7:6] = 00	SMPC.2 = 0 ~~SGSEL.1,0 = 00/10~~ SGSEL.[2:0] = 000/010/100/110
	SM34	Output	0	0	0	SMPC.2 = 1	TOS21.[7:6] = 01/10/ ~~SGSEL.1,0 = 00/10~~ SGSEL.[2:0] = 000/010/100/110
	SGO/SGOF	Output	0	0	0	~~SGSEL.1,0 = 01~~ SGSEL.[2:0] = 001/101	TOS21.[7:6] = 01/10/11 SMPC.2 = 0
P94	TO01	Output	0	0	0	TOS00.[3:2] = 10	SMPC.3 = 0 RTCSEL.[7:6] = 00/01/11
	RTC1HZ	Output	0	0	0	RTCSEL.[7:6] = 10	TOS00.[3:2] = 00/01/11 SMPC.3 = 0
	SM41	Output	0	0	0	SMPC.3 = 1	TOS00.[3:2] = 00/01/11 RTCSEL.[7:6] = 00/01/11
P96	SM43	Output	0	0	0	SMPC.3 = 1	TOS01.[3:2] = 00/01/11
P97	SM44	Output	0	0	0	SMPC.3 = 1	TOS01.[7:6] = 00/01/11

Table 4-23. Settings of Register, and Output Latch When Using Alternate Function

(k) Alternate function of P10

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P105	TI02	Input	1	x	0	~~TIS00.[5:4] = 11~~ TIS00.[5:4] = 10	-
	TO02	Output	0	0	0	~~TOS00.[5:4] = 11~~ TOS00.[5:4] = 10	-
P106	TI05	Input	1	x	0	TIS01.[3:2] = 11 TISELSE.[1:0] = 00	-
P107	TI06	Input	1	x	0	TIS01.[5:4] = 10 RTCSEL.0 = 0	-

(l) Alternate function of P11

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P110	TI00	Input	1	x	0	TIS00.[1:0] = ~~00~~ 10 TISELSE.6 = 0	-
	TO00	Output	0	0	0	TOS00.[1:0] = ~~00~~ 10	STSEL0.[3:2] = 00/01/10 PER1.LBEN = 0
	SCK00	Output	0	1	0	STSEL0.[3:2] = 11	TOS00.[1:0] = ~~01/10~~ 00/01 PER1.LBEN = 0
		Input	1	x			-
	DBD0	I/O	1	0	0	-	TOS00.[1:0] = 00/01 STSEL0.[3:2] = 00/01/10
P111	TO02	Output	0	0	0	TOS00.[5:4] = 11	PER1.LBEN = 0
	DBD1	I/O	1	0	0	-	TOS00.[5:4] = 00/01/10
P112	TO04	Output	0	0	0	TOS01.[1:0] = 10	STSEL0.[3:2] = 00/01/10 PER1.LBEN = 0
	SO00	Output	0	1	0	STSEL0.[3:2] = 11	TOS01.[1:0] = 00/01/11 PER1.LBEN = 0
	TxD0	Output					
	DBD2	I/O	1	0	0	-	TOS01.[1:0] = 00/01/11 STSEL0.[3:2] = 00/01/10
P113	TI06	Input	1	x	0	TIS01.[5:4] = 11 RTCSEL.0 = 0	-
	TO06	Output	0	0	0	TOS01.[5:4] = 11	PER1.LBEN = 0
	DBD3	I/O	1	0	0	-	TOS01.[5:4] = 00/01/10
P114	TI07	Input	1	x	0	TIS01.[7:6] = 11 RTCSEL.1 = 0	-
	TO07	Output	0	0	0	TOS01.[7:6] = 11	PER1.LBEN = 0
	DBD4	I/O	1	0	0	-	TOS01.[7:6] = 00/01/10
P115	TO10	Output	0	0	0	TOS10.[1:0] = 01	PER1.LBEN = 0
	DBD5	I/O	1	0	0	-	TOS10.[1:0] = 00/10
P116	TO12	Output	0	0	0	TOS10.[5:4] = 11	PER1.LBEN = 0
	DBD6	I/O	1	0	0	-	TOS10.[5:4] = 00/01/10
P117	TI20	Input	1	x	0	TIS20.[1:0] = 11 TISELSE.7 = 0	-
	TO20	Output	0	0	0	TOS20.[1:0] = 11	PER1.LBEN = 0
	DBD7	I/O	1	0	0	-	TOS20.[1:0] = 00/01/10

Table 4-23. Settings of Register, and Output Latch When Using Alternate Function

(n) Alternate function of P12

Port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P126	TI14	Input	1	x	0	TIS11.[1:0] = 11 STSEL1.0 = 0	-
P127	TI16	Input	1	x	0	TIS11.[5:4] = 11 RTCSEL.2 = 0	-

(o) Alternate function of P13

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P133	SCK10	Output	0	1	N/A	STSEL0.6 = 0	TOS20.[5:4] = 00/01/11
		Input	1	x			-
P134	SGOA	Output	0	0	N/A	SGSEL.[2:0] = 010	TOS21.[1:0] = 00/01/11 STSEL1.3 = 0
	CTxD1	Output	0	1		STSEL1.3 = 1	TOS21.[1:0] = 00/01/11 SGSEL.[2:0] = 000/001/100/101/110
P135	TO26	Output	0	0	N/A	TOS21.[5:4] = 10	~~SGSEL.1,0 = 00/01~~ SGSEL.[2:0] = 000/001/100/101
	SGO/SGOF	Output	0	0		~~SGSEL.1,0 = 10~~ SGSEL.[2:0] = 010/110	TOS21.[5:4] = 00/01/11
P136	TI00	Input	1	x	0	~~TIS00.0 = 1~~ TIS00.[1:0] = 01 TISELSE.6 = 0	-
	TO00	Output	0	0	0	~~TOS00.0 = 1~~ TOS00.[1:0] = 01	STSEL1.[7:6] = 00/01
	SCL11	Output	0	1	0	STSEL1.[7:6] = 10	~~TOS00.0 = 0~~ TOS00.[1:0] = 00/10

(p) Alternate function of P14

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
~~P14~~ P140	TI11	Input	1	x	N/A	TIS10.[3:2] = 10	-
	TO11	Output	0	0		TOS10.[3:2] = 10	-

(q) Alternate function of P15

port	Alternate function		PMxx	Pxx	ADPC (bit 3 to 0)
	Function name	I/O			
P150	ANI8	Input	~~x~~ 1	x	0000/1010/1011
P151	ANI9	Input	~~x~~ 1	x	0000/1011
P152	ANI10	Input	~~x~~ 1	x	0000

No.33: Correct a typo in the PLL clock description in “Chapter 5.1”

Changes are shown in red characters.

5.1 Functions of Clock Generator

(2) PLL clock

A clock that is the main system clock multiplied by ~~4, 6 or 8~~ 3, 4, 6 or 8 can be oscillated. Oscillation can be stopped by executing a STOP instruction or by setting PLLON (bit 0 of PLLCTL) to 0.

No.34: Correct the description of the CMC register in “Chapter 5.3, (1)”

Changes are shown in red characters.

(1) Clock operation mode control register (CMC)

This register is used to set the operation mode of the X1/P121, X2/EXCLK/P122, XT1/P123, and XT2/P124 pins, and to select a gain of the oscillator.

The CMC register can be written only once by an 8-bit memory manipulation instruction after reset release. This register can be read by ~~a 1-bit or 8-bit~~ an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 5-3. Format of Clock Operation Mode Control Register (CMC)

Caution 3. Be sure to set the AMPH bit to 1 if the X1 clock oscillation frequency exceeds 10 MHz. When the X1 clock oscillation frequency is in the range from 1 to 10 MHz, setting the AMPH bit to 1 improves the oscillation margin.

No.35: Correct the description of the OSTC register in “Chapter 5.3, (4)”

Changes are shown in red characters.

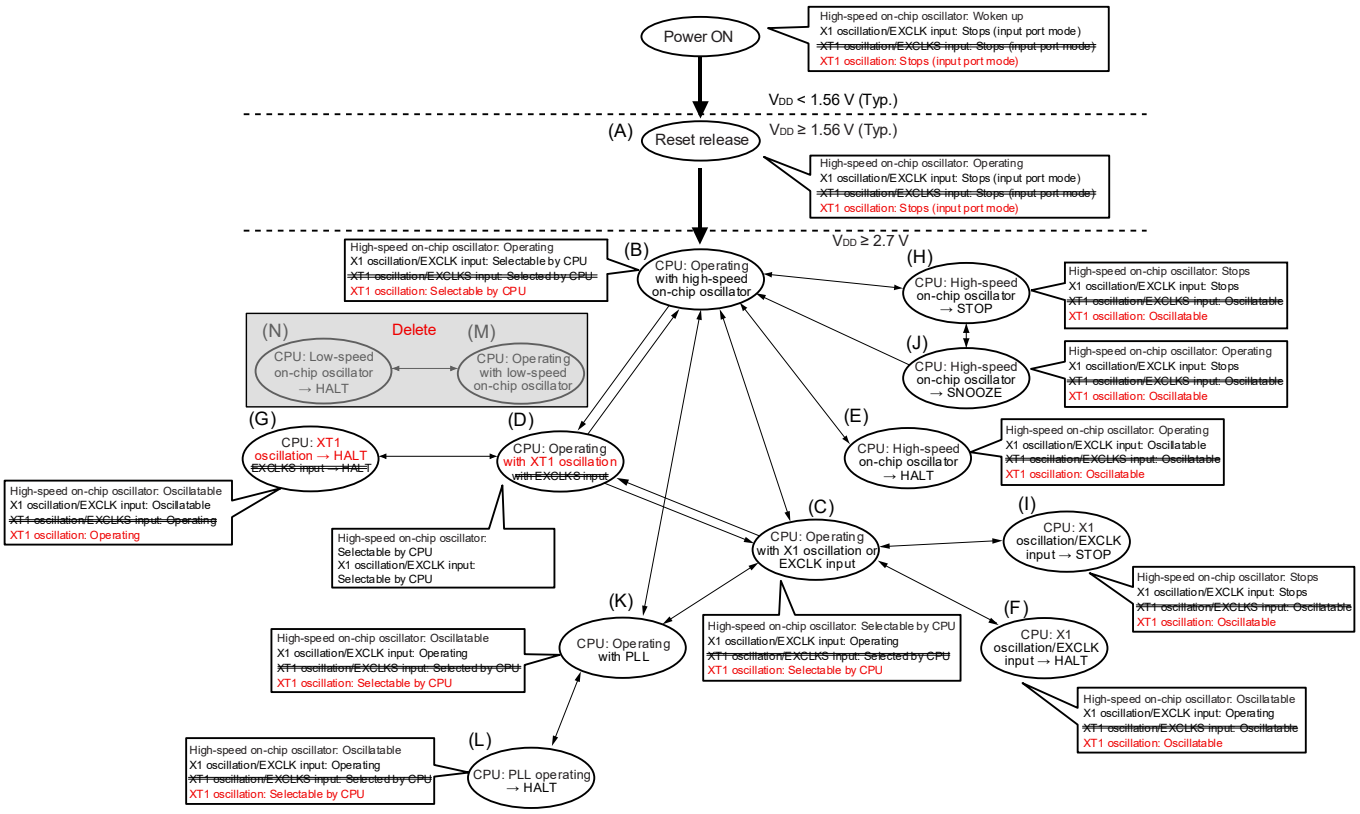
(4) Oscillation stabilization time counter status register (OSTC)

Caution 2. The oscillation stabilization time counter counts up to the oscillation stabilization time set by the oscillation stabilization time select register (OSTS). In the following cases, set the oscillation stabilization time of the OSTS register to the value equal to or greater than the count value which is to be checked by the OSTC register.

No.36: Correct the “Figure 5-19”

Changes are shown in red characters.

Figure 5-19. CPU Clock Status Transition Diagram



No.37: Delete the incorrect description in “Table 5-5, (3)”

Changes are shown in red characters.

(3) CPU operating with subsystem clock (D) after reset release (A)

(The CPU operates with the high-speed on-chip oscillator clock immediately after a reset release (B).)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CMC Register[Note]			CSC Register	Waiting for Oscillation Stabilization	CKC Register
	OSCSELS	AMPHS1	AMPHS0	XTSTOP		CSS
(A) → (B) → (D) (XT1 clock)	1	0/1	0/1	0	Necessary	1
~~(A) → (B) → (D)~~ ~~(external sub clock)~~	~~1~~	~~×~~	~~×~~	~~0~~	~~Necessary~~	~~1~~

No.38: Correct the incorrect “Remark” at the bottom of “Table 5-5”

Changes are shown in red characters.

Remark ~~(A) to (J)~~ (A) to (L) in Table 5-5 correspond to (A) to (L) in ~~Figure 5-20~~ Figure 5-19.

No.39: Add PLL clock explanation to “Table 5-5”

Changes are shown in red characters.

Table 5-5. CPU Clock Transition and SFR Register Setting Examples

(10)
- **HALT mode (E) set while CPU is operating with high-speed on-chip oscillator clock (B)**
- **HALT mode (F) set while CPU is operating with high-speed system clock (C)**
- **HALT mode (G) set while CPU is operating with subsystem clock (D)**
- **HALT mode (L) set while CPU is operating with PLL clock (K)**

Status Transition	Setting
(B) → (E) (C) → (F) (D) → (G) (K) → (L)	Executing HALT instruction

(13) CPU clock changing from high-speed on-chip oscillator clock (B) or high-speed system clock (C) to operating with the PLL clock (K)

- Set the PLLCTL register (LCKSEL[1:0] = xx, PLLDIV0 = x).
- Set the PLLON bit in the PLLCTL register to 1.
- Confirm that the LOCK bit in the PLLSTS register is set to 1 (checking PLL locked state).
- Set the SELPLL bit in the PLLCTL register to 1.
- Confirm that the SELPLLS bit in the PLLSTS register is set to 1.

No.40: Add PLL clock explanation to “Table 5-6”

Changes are shown in red characters.

Table 5-6. Changing CPU Clock

CPU Clock		Condition Before Change	Processing After Change
Before Change	After Change		
High-speed on-chip oscillator clock	PLL clock	PLL oscillation is stable. • LOCK = 1, PLLON = 1	The high-speed on-chip oscillator cannot be stopped because it is the PLL input clock.
X1 clock	PLL clock	PLL oscillation is stable. • LOCK = 1, PLLON = 1	The X1 clock cannot be stopped because it is the PLL input clock.
External main system clock	PLL clock	PLL oscillation is stable. • LOCK = 1, PLLON = 1	The external main system clock cannot be stopped because it is the PLL input clock.
PLL clock	High-speed on-chip oscillator clock	The high-speed on-chip oscillator starts oscillation, and the high-speed on-chip oscillator clock is selected as the main system clock. • HIOSTOP = 0, MCS = 0	The PLL clock can be stopped (PLLON = 0) after checking that the CPU clock is changed.
	X1 clock	X1 clock is stable, and the high-speed system clock is selected as the main system clock • OSCSEL = 1, EXCLK = 0, MSTOP = 0 • After elapse of oscillation stabilization time • MCS = 1	
	External main system clock	External clock input from the EXCLK pin is enabled, and the high-speed system clock is selected as the main system clock • OSCSEL = 1, EXCLK = 1, MSTOP = 0 • MCS = 1	

No.41: Add PLL clock explanation to “Table 5-10”

Changes are shown in red characters.

Table 5-10. Conditions Before the Clock Oscillation Is Stopped and Flag Settings

Clock	Conditions Before Clock Oscillation Is Stopped (External Clock Input Disabled)	Flag Settings of SFR Register
High-speed on-chip oscillator clock	MCS = 1 or CLS = 1 (The CPU is operating on a clock other than the high-speed on-chip oscillator clock.)	HIOSTOP = 1
X1 clock External main system clock	MCS = 0 or CLS = 1 (The CPU is operating on a clock other than the high-speed system clock.)	MSTOP = 1
XT1 clock	CLS = 0 (The CPU is operating on a clock other than the subsystem clock.)	XTSTOP = 1
PLL clock	SELPLLS = 0 (The CPU is operating on a clock other than the PLL clock)	PLLON = 0

No.42: Update the “Figures 6-2, 6-4, 6-6”

Changes are shown in red characters.

Figure 6-2. Port Configuration Diagram of Timer Array Unit 0

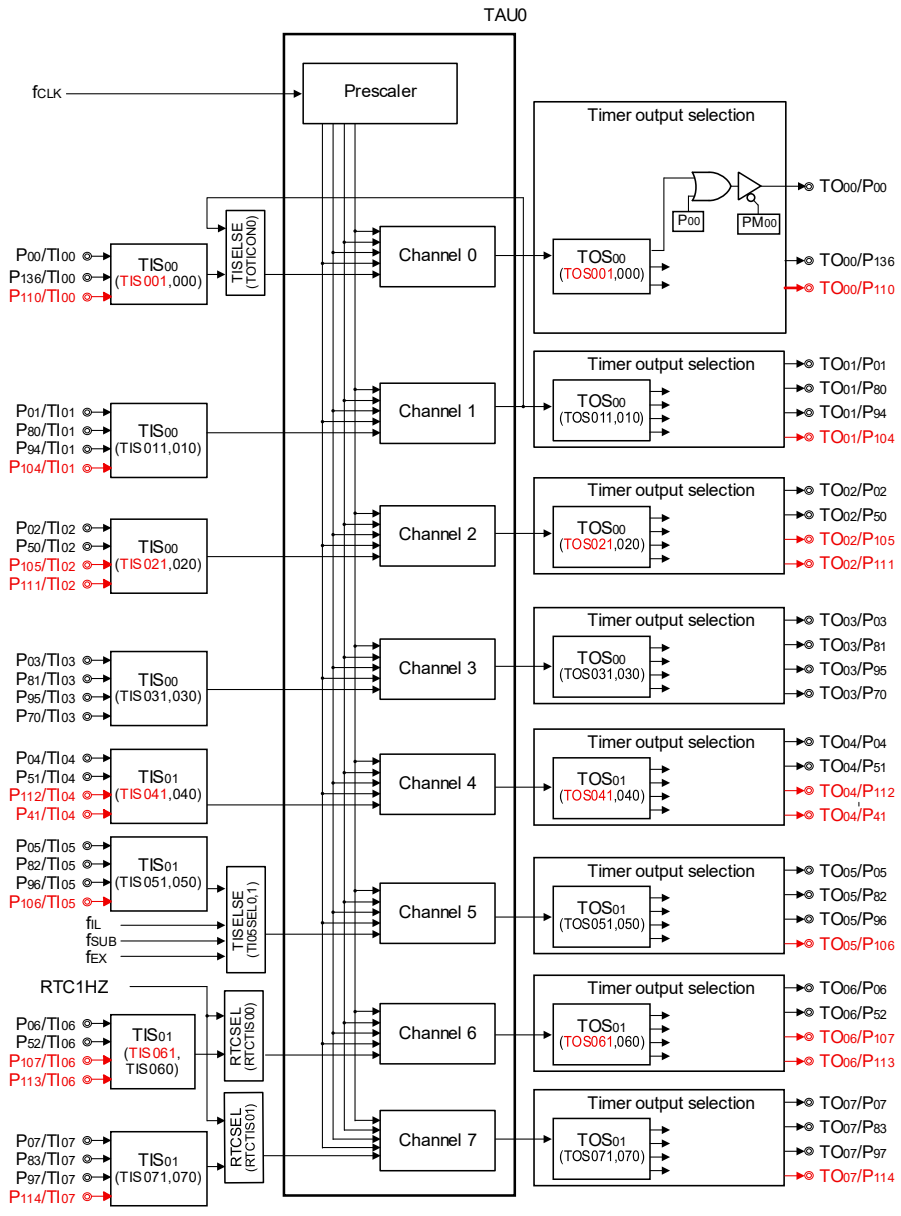


Figure 6-4. Port Configuration Diagram of Timer Array Unit 1

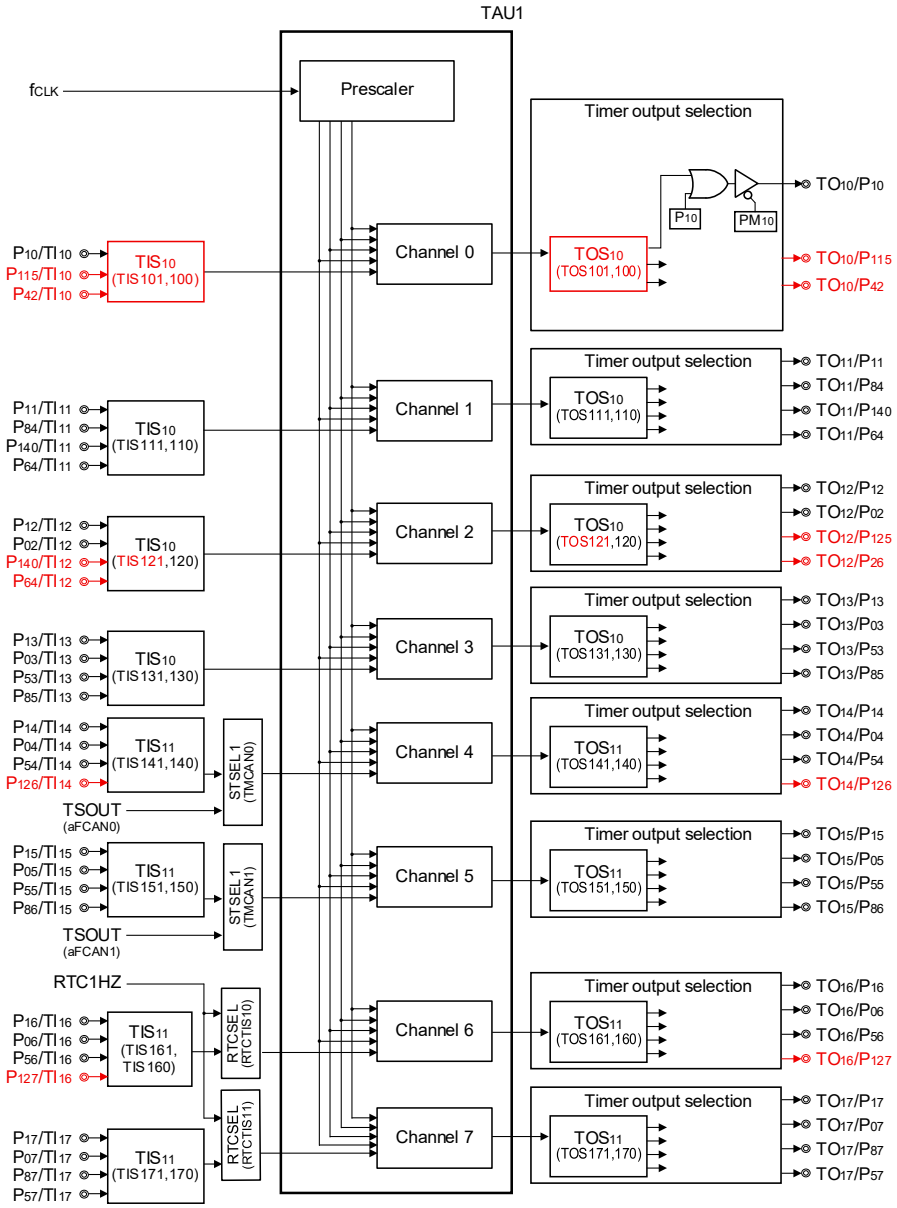
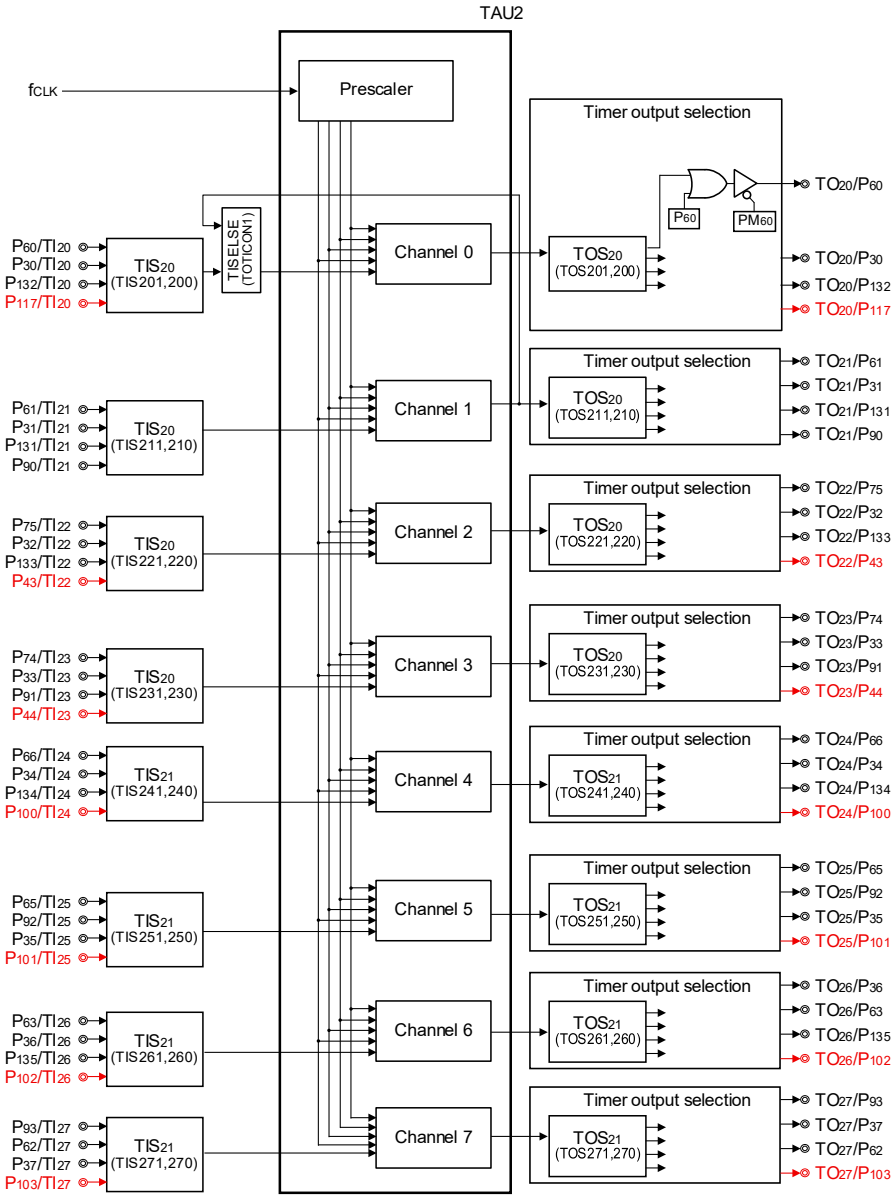


Figure 6-6. Port Configuration Diagram of Timer Array Unit 2



No.43: Correct incorrect description of CKSmn[1:0] and MDmn0 bits in “Figure 6-11”

Changes are shown in red characters.

Figure 6-11. Format of Timer Mode Register mn (TMRmn)

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07), F01D0H, F01D1H (TMR10) to F01DEH, F01DFH (TMR17), F0210H, F0211H (TMR20) to F021EH, F021FH (TMR27) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn	CKS mn1	CKS mn0	0	CCS mn	MAST ERmn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

CKS mn1	CKS mn0	Selection of operation clock (f_{MCK}) of channel n
0	0	Operation clock CKm0 set byTPSm register
0	1	Operation clock ~~CKm1~~ CKm2 set by TPSm register
1	0	Operation clock ~~CKm2~~ CKm1 set by TPSm register
1	1	Operation clock CKm3 set by TPSm register
Operation clock (f_{MCK}) is used by the edge detector. A count clock (f_{TCLK}) is generated depending on the setting of the CCSmn bit.		

Operation mode (Value set by the MDmn3 to MDmn1 bits (see table above))	MD mn0	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• Capture mode (0, 1, 0)	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode Note 1 (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation Note 2. ~~At that time, interrupt is also generated.~~ At that time, interrupt is not generated, either.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
Other than the above		Setting prohibited

~~**Note** If the start trigger (TSmn = 1) is issued during operation, the counter is cleared, an interrupt is generated, and recounting is started.~~

Notes 1. In one-count mode, interrupt output (INTTMmn) when starting a count operation and TOmn output are not controlled.

2. If the start trigger (TSmn = 1) is issued during operation, the counter is cleared, an interrupt is generated, and recounting is started (no interrupt request is generated).

No.44: Update the “Figures 6-30 to 6-35”

Changes are shown in red characters.

Figure 6-30. Format of Timer Input Select Register 0 (TIS00, TIS01)

Address: F0070H After reset: 00H R/W ~~(Note: Bits 1 and 5 are read only bit.)~~

Symbol	7	6	5	4	3	2	1	0
TIS00	TIS031	TIS030	~~0~~ TIS021	TIS020	TIS011	TIS010	~~0~~ TIS001	TIS000

Address: F0071H After reset: 00H R/W ~~(Note: Bits 1 and 5 are read only bit.)~~

Symbol	7	6	5	4	3	2	1	0
TIS01	TIS071	TIS070	~~0~~ TIS061	TIS060	TIS051	TIS050	~~0~~ TIS041	TIS040

TIS001	TIS000	TI00 (TAU unit0 CH0) alternate pin selection
0	0	P00
0	1	P136
1	0	P110 Note 1
1	1	Setting prohibited (same as “10” setting) Note 1

TIS011	TIS010	TI01 (TAU unit0 CH1) alternate pin selection
0	0	P01
0	1	P80
1	0	P94
~~Other than the above~~		~~Setting prohibited (same as “00” setting)~~
1	1	P104 Note 2

TIS021	TIS020	TI02 (TAU unit0 CH2) alternate pin selection
0	0	P02
0	1	P50
1	0	P105 Note 1
1	1	P111 Note 1

TIS041	TIS040	TI04 (TAU unit0 CH4) alternate pin selection
0	0	P04
0	1	P51
1	0	P112 Note 1
1	1	P41 Note 1

TIS051	TIS050	TI05 (TAU unit0 CH5) alternate pin selection
0	0	P05
0	1	P82
1	0	P96
~~Other than the above~~		~~Setting prohibited (same as “00” setting)~~
1	1	P106 Note 2

TIS061	TIS060	TI06 (TAU unit0 CH6) alternate pin selection
0	0	P06
0	1	P52
1	0	P107 Note 1
1	1	P113 Note 1

TIS071	TIS070	TI07 (TAU unit0 CH7) alternate pin selection
0	0	P07
0	1	P83
1	0	P97
~~Other than the above~~		~~Setting prohibited (same as “00” setting)~~
1	1	P114 Note 2

Notes 1. This bit is only available for Group B products.

2. "Setting prohibited (same as “00” setting)" for Group A products.

Remark For Groups A and B products, see "**Definition of Product Groups**" in Chapter 4.1.

Figure 6-31. Format of TIS10 and TIS11 Registers

Address: F0072H After reset: 00H R/W ~~(Note: Bits 0, 1 and 5 are read only bit.)~~

Symbol	7	6	5	4	3	2	1	0
TIS10	TIS131	TIS130	~~0~~ TIS121	TIS120	TIS111	TIS110	~~0~~ TIS101	~~0~~ TIS100

Address: F0073H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TIS11	TIS171	TIS170	TIS161	TIS160	TIS151	TIS150	TIS141	TIS140

TIS101	TIS100	TI10 (TAU unit1 CH0) alternate pin selection
0	0	P10 Note 1
0	1	P115 Note 1
1	0	P42 Note 1
1	1	Setting prohibited (same as “10” setting) Note 1

TIS121	TIS120	TI12 (TAU unit1 CH2) alternate pin selection
0	0	P12
0	1	P02
1	0	P125 Note 1
1	1	P116 Note 1

TIS141	TIS140	TI14 (TAU unit1 CH4) alternate pin selection
0	0	P14
0	1	P04
1	0	P54
~~Other than the above~~		~~Setting prohibited (same as “00” setting)~~
1	1	P126 Note 2

TIS161	TIS160	TI16 (TAU unit1 CH6) alternate pin selection
0	0	P16
0	1	P06
1	0	P56
~~Other than the above~~		~~Setting prohibited (same as “00” setting)~~
1	1	P127 Note 2

Notes 1. This bit is only available for Group B products.

2. "Setting prohibited (same as “00” setting)" for Group A products.

Remark For Groups A and B products, see "**Definition of Product Groups**" in Chapter 4.1.

Figure 6-32. Format of TIS20 and TIS21 Registers

Address: F0074H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TIS20	TIS231	TIS230	TIS221	TIS220	TIS211	TIS210	TIS201	TIS200

Address: F0075H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TIS21	TIS271	TIS270	TIS261	TIS260	TIS251	TIS250	TIS241	TIS240

TIS201	TIS200	TI20 (TAU unit2 CH0) alternate pin selection
0	0	P60
0	1	P30
1	0	P132
~~Other than the above~~		~~Setting prohibited (same as “00” setting)~~
1	1	P117 Note

TIS221	TIS220	TI22 (TAU unit2 CH2) alternate pin selection
0	0	P75
0	1	P32
1	0	P133
~~Other than the above~~		~~Setting prohibited (same as “00” setting)~~
1	1	P43 Note

TIS231	TIS230	TI23 (TAU unit2 CH3) alternate pin selection
0	0	P74
0	1	P33
1	0	P91
~~Other than the above~~		~~Setting prohibited (same as “00” setting)~~
1	1	P44 Note

TIS241	TIS240	TI24 (TAU unit2 CH4) alternate pin selection
0	0	P66
0	1	P34
1	0	P134
~~Other than the above~~		~~Setting prohibited (same as “00” setting)~~
1	1	P100 Note

TIS251	TIS250	TI25 (TAU unit2 CH5) alternate pin selection
0	0	P65
0	1	P92
1	0	P35
~~Other than the above~~		~~Setting prohibited (same as “00” setting)~~
1	1	P101 Note

TIS261	TIS260	TI26 (TAU unit2 CH6) alternate pin selection
0	0	P63
0	1	P36
1	0	P135
~~Other than the above~~		~~Setting prohibited (same as “00” setting)~~
1	1	P102 Note

TIS271	TIS270	TI27 (TAU unit2 CH7) alternate pin selection
0	0	P93
0	1	P62
1	0	P37
~~Other than the above~~		~~Setting prohibited (same as “00” setting)~~
1	1	P103 Note

Note "Setting prohibited (same as “00” setting)" for Group A products.

Remark For Group A products, see "**Definition of Product Groups**" in Chapter 4.1.

Figure 6-33. Format of Timer Output Select Registers (TOS00, TOS01)

Address: F0076H After reset: 00H R/W ~~(Note: Bits 1 and 5 are read only bit.)~~

Symbol	7	6	5	4	3	2	1	0
TOS00	TOS031	TOS030	~~0~~ TOS021	TOS020	TOS011	TOS010	~~0~~ TOS001	TOS000

Address: F0077H After reset: 00H R/W ~~(Note: Bits 1 and 5 are read only bit.)~~

Symbol	7	6	5	4	3	2	1	0
TOS01	TOS071	TOS070	~~0~~ TOS061	TOS060	TOS051	TOS050	~~0~~ TOS041	TOS040

TOS001	TOS000	TO00 (TAU unit0 CH0) alternate pin selection
0	0	P00
0	1	P136
1	0	P110 Note 1
1	1	Setting prohibited (same as “10” setting) Note 1

TOS011	TOS010	TO01 (TAU unit0 CH1) alternate pin selection
0	0	P01
0	1	P80
1	0	P94
~~Other than the above~~		~~Setting prohibited (same as “00” setting)~~
1	1	P104 Note 2

TOS021	TOS020	TO02 (TAU unit0 CH2) alternate pin selection
0	0	P02
0	1	P50
1	0	P105 Note 1
1	1	P111 Note 1

TOS041	TOS040	TO04 (TAU unit0 CH4) alternate pin selection
0	0	P04
0	1	P51
1	0	P112 Note 1
1	1	P41 Note 1

TOS051	TOS050	TO05 (TAU unit0 CH5) alternate pin selection
0	0	P05
0	1	P82
1	0	P96
~~Other than the above~~		~~Setting prohibited (same as “00” setting)~~
1	1	P106 Note 2

TOS061	TOS060	TO06 (TAU unit0 CH6) alternate pin selection
0	0	P06
0	1	P52
1	0	P107 Note 1
1	1	P113 Note 1

TOS071	TOS070	TO07 (TAU unit0 CH7) alternate pin selection
0	0	P07
0	1	P83
1	0	P97
~~Other than the above~~		~~Setting prohibited (same as “00” setting)~~
1	1	P114 Note 2

Notes 1. This bit is only available for Group B products.

2. "Setting prohibited (same as “00” setting)" for Group A products.

Remark For Groups A and B products, see "**Definition of Product Groups**" in Chapter 4.1.

Figure 6-34. Format of TOS10 and TOS11 Registers

Address: F0079H After reset: 00H R/W ~~(Note: Bits 0, 1 and 5 are read only bit.)~~

Symbol	7	6	5	4	3	2	1	0
TOS10	TOS131	TOS130	~~0~~ TOS121	TOS120	TOS111	TOS110	~~0~~ TSO101	~~0~~ TOS100

Address: F007AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TOS11	TOS171	TOS170	TOS161	TOS160	TOS151	TOS150	TOS141	TOS140

TOS101	TOS100	TO10 (TAU unit1 CH0) alternate pin selection
0	0	P10 Note 1
0	1	P115 Note 1
1	0	P42 Note 1
1	1	Setting prohibited (same as “10” setting) Note 1

TOS121	TOS120	TO12 (TAU unit1 CH2) alternate pin selection
0	0	P12
0	1	P02
1	0	P125 Note 1
1	1	P116 Note 1

TOS141	TOS140	TO14 (TAU unit1 CH4) alternate pin selection
0	0	P14
0	1	P04
1	0	P54
~~Other than the above~~		~~Setting prohibited (same as “00” setting)~~
1	1	P126 Note 2

TOS161	TOS160	TO16 (TAU unit1 CH6) alternate pin selection
0	0	P16
0	1	P06
1	0	P56
~~Other than the above~~		~~Setting prohibited (same as “00” setting)~~
1	1	P127 Note 2

Notes 1. This bit is only available for Group B products.

2. "Setting prohibited (same as “00” setting)" for Group A products.

Remark For Groups A and B products, see "**Definition of Product Groups**" in Chapter 4.1.

Figure 6-35. Format of TOS20 and TOS21 Registers

Address: F007BH After reset: 00H R/W ~~(Note: Bits 0, 1 and 5 are read only bit.)~~

Symbol	7	6	5	4	3	2	1	0
TOS20	TOS231	TOS230	TOS221	TOS220	TOS211	TOS210	TOS201	TOS200

Address: F007CH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TOS21	TOS271	TOS270	TOS261	TOS260	TOS251	TOS250	TOS241	TOS240

TOS201	TOS200	TO20 (TAU unit2 CH0) alternate pin selection
0	0	P60
0	1	P30
1	0	P132
~~Other than the above~~		~~Setting prohibited (same as "00" setting)~~
1	1	P117 Note

TOS221	TOS220	TO22 (TAU unit2 CH2) alternate pin selection
0	0	P75
0	1	P32
1	0	P133
~~Other than the above~~		~~Setting prohibited (same as "00" setting)~~
1	1	P43 Note

TOS231	TOS230	TO23 (TAU unit2 CH3) alternate pin selection
0	0	P74
0	1	P33
1	0	P91
~~Other than the above~~		~~Setting prohibited (same as "00" setting)~~
1	1	P44 Note

TOS241	TOS240	TO24 (TAU unit2 CH4) alternate pin selection
0	0	P66
0	1	P34
1	0	P134
~~Other than the above~~		~~Setting prohibited (same as "00" setting)~~
1	1	P100 Note

TOS251	TOS250	TO25 (TAU unit2 CH5) alternate pin selection
0	0	P65
0	1	P92
1	0	P35
~~Other than the above~~		~~Setting prohibited (same as "00" setting)~~
1	1	P101 Note

TOS261	TOS260	TO26 (TAU unit2 CH6) alternate pin selection
0	0	P36
0	1	P63
1	0	P135
~~Other than the above~~		~~Setting prohibited (same as "00" setting)~~
1	1	P102 Note

~~TIS271~~ TOS271	~~TIS270~~ TOS270	~~TI27~~ TO27 (TAU unit2 CH7) alternate pin selection
0	0	P93
0	1	P37
1	0	P62
~~Other than the above~~		~~Setting prohibited (same as "00" setting)~~
1	1	P103 Note

Note "Setting prohibited (same as "00" setting)" for Group A products.

Remark For Group A products, see "**Definition of Product Groups**" in Chapter 4.1.

No.45: Correct a description for TISELSE register in “Figure 6-36”

Changes are shown in red characters.

Figure 6-36. Format of TISELSE Registers

Address: FFF3E After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TISELSE	TOTICON1	TOTICON0	0	0	0	0	TI05SEL1	TI05SEL0

TI05SEL1	TI05SEL0	TIS051	TIS050	TAU unit0 CH5 input alternate selection
0	0	0	0	P05
0	0	0	1	P82
0	0	1	0	P96
0	0	1	1	P106 Note
0	1	x	x	Low-speed on-chip clock (f_{IL})
1	0	x	x	Sub system clock (f_{SUB})
1	1	x	x	Main external clock (f_{EX})
Other than the above				Setting prohibited (same as “0000” setting)

Note "Setting prohibited (same as “0000” setting)" for Group A products.

Remark For Group A products, see "**Definition of Product Groups**" in Chapter 4.1.

No.46: Correct a description of SCSI00[1:0] bit in “Figure 6-37”

Changes are shown in red characters.

Figure 6-37. Format of STSEL0 Register

Address: FFF3CH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
STSEL0	0	SCSI100	0	SCSI010	SCSI001	SCSI000	SUARTF1	SUARTF0

SyCSI001	SCSI000	CSI00 communication pin selection			UART0 pin selection	
		$\overline{\text{SCK00}}$	SI00	SO00	RxD0	TxD0
0	0	P10	P11	P12	P11 Note1	P12 Note1
0	1	P04	P03	P02	P03 Note1	P02 Note1
1	0	P34	P33	P32	P33 Notie1	P32 Note1
~~Other than the above~~		~~Setting prohibited (same as “00” setting)~~				
1	1	P110 Notes1,2	P111 Notes1,2	P112 Notes1,2	P111 Notes1,2	P112 Notes1,2

Notes 1. 128-pin products only.

2. "Setting prohibited (same as “00” setting)" for Group A products.

Remark For Group A products, see "**Definition of Product Groups**" in Chapter 4.1.

No.47: Correct the “Table 6-5”

Remove irrelevant feature descriptions that do not contain TIxx or TOxx. Changes are shown in red characters.

Table 6-5. Settings of Register, and Output Latch When Using Alternate Function

(a) Alternate function of P0

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P00	TI00	Input	1	x	0	~~TIS00.0 = 0~~ TIS00.[1:0] = 00 TISELSE.6 = 0	-
	TO00	Output	0	0	0	TOS00.[1:0] = 00	STSEL1.2 = 0
P01	TI01	Input	1	x	0	TIS00.[3:2] = 00	-
	TO01	Output	0	0	0	TOS00.[3:2] = 00	-
P02	TI02	Input	1	x	0	~~TIS00.4 = 0~~ TIS00.[5:4] = 00	-
	TO02	Output	0	0	0	~~TOS00.4 = 0~~ TOS00.[5:4] = 00	STSEL0.[3:2] = 00/10/11 ~~TOS10.4 = 0~~ TOS10.[5:4] = 00/10/11
	TI12	Input	1	x	0	~~TIS10.4 = 1~~ TIS10.[5:4] = 01	-
	TO12	Output	0	0	0	~~TOS10.4 = 1~~ TOS10.[5:4] = 01	STSEL0.[3:2] = 00/10/11 ~~TOS00.4 = 0~~ TOS00.[5:4] = 01/10/11
P03	TI03	Input	1	x	0	TIS00.[7:6] = 00	-
	TO03	Output	0	0	0	TOS00.[7:6] = 00	TOS10.[7:6] = 00/10/11
	TI13	Input	1	x	0	TIS10.[7:6] = 01	-
	TO13	Output	0	0	0	TOS10.[7:6] = 01	TOS00.[7:6] = 01/10/11
P04	TI04	Input	1	x	0	~~TIS01.0 = 0~~ TIS01.[1:0] = 00	-
	TO04	Output	0	0	0	~~TOS01.0 = 0~~ TOS01.[1:0] = 00	STSEL0.[3:2] = 00/10/11 TOS11.[1:0] = 00/10/11
	TI14	Input	1	x	0	TIS11.[1:0] = 01 STSEL1.0 = 0	-
	TO14	Output	0	0	0	TOS11.[1:0] = 01	STSEL0.[3:2] = 00/10/11 ~~TOS01.0 = 1~~ TOS01.[1:0] = 01/10/11
P05	TI05	Input	1	x	0	TIS01.[3:2] = 00 TISELSE.[1:0] = 00	-
	TO05	Output	0	0	0	TOS01.[3:2] = 00	TOS11.[3:2] = 00/10/11
	TI15	Input	1	x	0	TIS11.[3:2] = 01 STSEL1.1 = 0	-
	TO15	Output	0	0	0	TOS11.[3:2] = 01	TOS01.[3:2] = 01/10/11
P06	TI06	Input	1	x	0	~~TIS01.4 = 0~~ TIS01.[5:4] = 00 RTCSEL.0 = 0	-
	TO06	Output	0	0	0	~~TOS01.4 = 0~~ TOS01.[5:4] = 00	TOS11.[5:4] = 00/10/11
	TI16	Input	1	x	0	TIS11.[5:4] = 01 RTCSEL.2 = 0	-
	TO16	Output	0	0	0	TOS11.[5:4] = 01	~~TOS01.4 = 1~~ TOS01.[5:4] = 01/10/11
P07	TI07	Input	1	x	0	TIS01.[7:6] = 00 RTCSEL.1 = 0	-
	TO07	Output	0	0	0	TOS01.[7:6] = 00	TOS11.[7:6] = 00/10/11
	TI17	Input	1	x	0	TIS11.[7:6] = 01 RTCSEL.3 = 0	-
	TO17	Output	0	0	0	TOS11.[7:6] = 01	TOS01.[7:6] = 01/10/11

(b) Alternate function of P1

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P10	TI10	Input	1	x	0	~~—~~ TIS10.[1:0] = 00	-
	TO10	Output	0	0	0	~~—~~ TOS10.[1:0] = 00	STSEL0.1 = 1 STSEL0.[3:2] = 01/10/11
P11	TI11	Input	1	x	0	TIS10.[3:2] = 00	-
	TO11	Output	0	0	0	TOS10.[3:2] = 00	-
P12	TI12	Input	1	x	0	~~TIS10.4 = 0~~ TIS10.[5:4] = 00	-
	TO12	Output	0	0	0	~~TOS10.4 = 0~~ TOS10.[5:4] = 00	STSEL0.[3:2] = 01/10/11
P13	TI13	Input	1	x	0	TIS10.[7:6] = 00	-
	TO13	Output	0	0	0	TOS10.[7:6] = 00	STSEL0.4 = 1
P14	TI14	Input	1	x	0	TIS11.[1:0] = 00 STSEL1.0 = 0	-
	TO14	Output	0	0	0	TOS11.[1:0] = 00	-
P15	TI15	Input	1	x	0	TIS11.[3:2] = 00 STSEL1.1 = 0	-
	TO15	Output	0	0	0	TOS11.[3:2] = 00	RTCSEL.[7:6] = 00/10/11 STSEL0.0 = 0
P16	TI16	Input	1	x	0	TIS11.[5:4] = 00 RTCSEL.2 = 0	-
	TO16	Output	0	0	0	TOS11.[5:4] = 00	-
P17	TI17	Input	1	x	0	TIS11.[7:6] = 00 RTCSEL.3 = 0	-
	TO17	Output	0	0	0	TOS11.[7:6] = 00	-

(C) Alternate function of P2

port	Alternate function		PMxx	Pxx	Expanded control setting (Register.bit)
	Function name	I/O			
P20	These pins are not assigned to the Timer Array Unit function.				
P21					
P22					
P23					
P24					
P25					
P26					
P27					

(d) Alternate function of P3

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P30	TI20	Input	1	x	0	TIS20.[1:0] = 01 TISELSE.7 = 0	-
	TO20	Output	0	0	0	TOS20.[1:0] = 01	STSEL1.[7:6] = 00/10
P31	TI21	Input	1	x	0	TIS20.[3:2] = 01	-
	TO21	Output	0	0	0	TOS20.[3:2] = 01	STSEL1.[7:6] = 00/10
P32	TI22	Input	1	x	0	TIS20.[5:4] = 01	-
	TO22	Output	0	0	0	TOS20.[5:4] = 01	STSEL0.[3:2] = 00/01/11
P33	TI23	Input	1	x	0	TIS20.[7:6] = 01	-
	TO23	Output	0	0	0	TOS20.[7:6] = 01	~~STSEL0.3,2 = 00/01~~ -
P34	TI24	Input	1	x	0	TIS21.[1:0] = 01	-
	TO24	Output	0	0	0	TOS21.[1:0] = 01	STSEL0.[3:2] = 00/01/11
P35	TI25	Input	1	x	0	TIS21.[3:2] = 10	-
	TO25	Output	0	0	0	TOS21.[3:2] = 10	~~STSEL0.3,2 = 00/01~~ -
P36	TI26	Input	1	x	0	TIS21.[5:4] = 01	-
	TO26	Output	0	0	0	TOS21.[5:4] = 00	-
P37	TI27	Input	1	x	0	TIS21.[7:6] = 10	-
	TO27	Output	0	0	0	TOS21.[7:6] = 01	-

(e) Alternate function of P4

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P40	This pin is not assigned to the Timer Array Unit function.						
P41	TI04	Input	1	x	N/A	TIS01.[1:0] = 11	-
	TO04	Output	0	0		TOS01.[1:0] = 11	STPSTC.STPOEN = 0
P42	TI10	Input	1	x	0	TIS10.[1:0] = 10	-
	TO10	Output	0	0	0	TOS10.[1:0] = 10	-
P43	TI22	Input	1	x	0	TIS20.[5:4] = 11	-
	TO22	Output	0	0	0	TOS20.[5:4] = 11	-
P44	TI23	Input	1	x	0	TIS20.[7:6] = 11	-
	TO23	Output	0	0	0	TOS20.[7:6] = 11	-
P45	These pins are not assigned to the Timer Array Unit function.						
P46							
P47							

(f) Alternate function of P5

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P50	TI02	Input	1	x	0	~~TIS00.4 = 1~~ TIS00.[5:4] = 01	-
	TO02	Output	0	0	0	~~TOS00.4 = 1~~ TOS00.[5:4] = 01	STSEL1.[7:6] = 00/01
P51	TI04	Input	1	x	0	~~TIS01.0 = 1~~ TIS01.[1:0] = 01	-
	TO04	Output	0	0	0	~~TOS01.0 = 1~~ TOS01.[1:0] = 01	STSEL0.6 = 0
P52	TI06	Input	1	x	0	~~TIS01.4 = 1~~ TIS01.[5:4] = 01 RTCSEL.0 = 0	-
	TO06	Output	0	0	0	~~TOS01.4 = 1~~ TOS01.[5:4] = 01	-
P53	TI13	Input	1	x	0	TIS10.[7:6] = 10	-
	TO13	Output	0	0	0	TOS10.[7:6] = 10	STSEL0.6 = 0
P54	TI14	Input	1	x	0	TIS11.[1:0] = 10 STSEL1.0 = 0	-
	TO14	Output	0	0	0	TOS11.[1:0] = 10	~~STSEL0.4 = 0~~
P55	TI15	Input	1	x	0	TIS11.[3:2] = 10 STSEL1.1 = 0	-
	TO15	Output	0	0	0	TOS11.[3:2] = 10	-
P56	TI16	Input	1	x	0	TIS11.[5:4] = 10 RTCSEL.2 = 0	-
	TO16	Output	0	0	0	TOS11.[5:4] = 10	STSEL0.4 = 0
P57	TI17	Input	1	x	0	TIS11.[7:6] = 11 RTCSEL.3 = 0	-
	TO17	Output	0	0	0	TOS11.[7:6] = 11	-

(g) Alternate function of P6

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P60	TI20	Input	1	x	N/A	TIS20.[1:0] = 00 TISELSE.7 = 0	-
	TO20	Output	0	0		TOS20.[1:0] = 00	STSEL1.[7:6] = 01/10
P61	TI21	Input	1	x	N/A	TIS20.[3:2] = 00	-
	TO21	Output	0	0		TOS20.[3:2] = 00	STSEL1.[7:6] = 01/10
P62	TI27	Input	1	x	N/A	TIS21.[7:6] = 01	-
	TO27	Output	1	0		TOS21.[7:6] = 10	STSEL1.3 = 1
P63	TI26	Input	1	x	N/A	TIS21.[5:4] = 00	-
	TO26	Output	0	0		TOS21.[5:4] = 01	-
P64	TI11	Input	1	x	N/A	TIS10.[3:2] = 11	-
	TO11	Output	0	0		TOS10.[3:2] = 11	RTCSEL.[7:6] = 01/10/11
P65	TI25	Input	1	x	N/A	TIS21.[3:2] = 00	-
	TO25	Output	0	0		TOS21.[3:2] = 00	-
P66	TI24	Input	1	x	N/A	TIS21.[1:0] = 00	-
	TO24	Output	0	0		TOS21.[1:0] = 00	SGSEL.3 = 0

(h) Alternate function of P7

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P70	TI03	Input	1	x	N/A	TIS00.[7:6] = 11	-
	TO03	Output	0	0		TOS00.[7:6] = 11	-
P71	These pins are not assigned to the Timer Array Unit function.						
P72							
P73							
P74	TI23	Input	1	x	0	TIS20.[7:6] = 00	-
	TO23	Output	0	0	0	TOS20.[7:6] = 00	STSEL0.4 = 1
P75	TI22	Input	1	x	0	TIS20.[5:4] = 00	-
	TO22	Output	0	0	0	TOS20.[5:4] = 00	SGSEL.3 = 1

(i) Alternate function of P8

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P80	TI01	Input	1	x	0	TIS00.[3:2] = 01	-
	TO01	Output	0	0	0	TOS00.[3:2] = 01	SMPC.0 = 0
P81	TI03	Input	1	x	0	TIS00.[7:6] = 01	-
	TO03	Output	0	0	0	TOS00.[7:6] = 01	SMPC.0 = 0
P82	TI05	Input	1	x	0	TIS01.[3:2] = 01 TISELSE.[1:0] = 00	-
	TO05	Output	0	0	0	TOS01.[3:2] = 01	SMPC.0 = 0
P83	TI07	Input	1	x	0	TIS01.[7:6] = 01 RTCSEL.1 = 0	-
	TO07	Output	0	0	0	TOS01.[7:6] = 01	SMPC.0 = 0
P84	TI11	Input	1	x	0	TIS10.[3:2] = 01	-
	TO11	Output	0	0	0	TOS10.[3:2] = 01	SMPC.1 = 0
P85	TI13	Input	1	x	0	TIS10.[7:6] = 11	-
	TO13	Output	0	0	0	TOS10.[7:6] = 11	SMPC.1 = 0
P86	TI15	Input	1	x	0	TIS11.[3:2] = 11 STSEL1.1 = 0	-
	TO15	Output	0	0	0	TOS11.[3:2] = 11	SMPC.1 = 0
P87	TI17	Input	1	x	0	TIS11.[7:6] = 10 RTCSEL.3 = 0	-
	TO17	Output	0	0	0	TOS11.[7:6] = 10	SMPC.1 = 0

(j) Alternate function of P9

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P90	TI21	Input	1	x	0	TIS20.[3:2] = 11	-
	TO21	Output	0	0	0	TOS20.[3:2] = 11	SMPC.2 = 0
P91	TI23	Input	1	x	0	TIS20.[7:6] = 10	-
	TO23	Output	0	0	0	TOS20.[7:6] = 10	SMPC.2 = 0
P92	TI25	Input	1	x	0	TIS21.[3:2] = 01	-
	TO25	Output	0	0	0	TOS21.[3:2] = 01	SMPC.2 = 0 SGSEL.[2:0] = 000/010/100/ 101/110
P93	TI27	Input	1	x	0	TIS21.[7:6] = 00	-
	TO27	Output	0	0	0	TOS21.[7:6] = 00	SMPC.2 = 0 ~~SGSEL.1,0 = 00/10~~ SGSEL.[2:0] = 000/010/100/110
P94	TI01	Input	1	x	0	TIS00.[3:2] = 10	-
	TO01	Output	0	0	0	TOS00.[3:2] = 10	SMPC.3 = 0 RTCSEL.[7:6] = 00/01/11
P95	TI03	Input	1	x	0	TIS00.[7:6] = 10	-
	TO03	Output	0	0	0	TOS00.[7:6] = 10	SMPC.3 = 0
P96	TI05	Input	1	x	0	TIS01.[3:2] = 10 TISELSE.[1:0] = 00	-
	TO05	Output	0	0	0	TOS01.[3:2] = 10	SMPC.3 = 0
P97	TI07	Input	1	x	0	TIS01.[7:6] = 10 RTCSEL.1 = 0	-
	TO07	Output	0	0	0	TOS01.[7:6] = 10	SMPC.3 = 0

(k) Alternate function of P10

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P100	TI24	Input	1	x	0	TIS21.[1:0] = 11	-
	TO24	Output	0	0	0	TOS21.[1:0] = 11	-
P101	TI25	Input	1	x	0	TIS21.[3:2] = 11	-
	TO25	Output	0	0	0	TOS21.[3:2] = 11	-
P102	TI26	Input	1	x	0	TIS21.[5:4] = 11	-
	TO26	Output	0	0	0	TOS21.[5:4] = 11	-
P103	TI27	Input	1	x	0	TIS21.[7:6] = 11	-
	TO27	Output	0	0	0	TOS21.[7:6] = 11	-
P104	TI01	Input	1	x	0	TIS00.[3:2] = 11	-
	TO01	Output	0	0	0	TOS00.[3:2] = 11	-
P105	TI02	Input	1	x	0	TIS00.[5:4] = 10	-
	TO02	Output	0	0	0	TOS00.[5:4] = 10	-
P106	TI05	Input	1	x	0	TIS01.[3:2] = 11 TISELSE.[1:0] = 00	-
	TO05	Output	0	0	0	TIS01.[3:2] = 11	-
P107	TI06	Input	1	x	0	TIS01.[5:4] = 10 RTCSEL.0 = 0	-
	TO06	Output	0	0	0	TIS01.[5:4] = 10	-

(l) Alternate function of P11

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P110	TI00	Input	1	x	0	TIS00.[1:0] = 10 TISELSE.6 = 0	-
	TO00	Output	0	0	0	TOS00.[1:0] = 10	STSEL0.[3:2] = 00/01/10 PER1.LBEN = 0
P111	TI02	Input	1	x	0	TIS00.[5:4] = 11	-
	TO02	Output	0	0	0	TOS00.[5:4] = 11	PER1.LBEN = 0
P112	TI04	Input	1	x	0	TIS01.[1:0] = 10	-
	TO04	Output	0	0	0	TOS01.[1:0] = 10	STSEL0.[3:2] = 00/01/10 PER1.LBEN = 0
P113	TI06	Input	1	x	0	TIS01.[5:4] = 11 RTCSEL.0 = 0	-
	TO06	Output	0	0	0	TOS01.[5:4] = 11	PER1.LBEN = 0
P114	TI07	Input	1	x	0	TIS01.[7:6] = 11 RTCSEL.1 = 0	-
	TO07	Output	0	0	0	TOS01.[7:6] = 11	PER1.LBEN = 0
P115	TI10	Input	1	x	0	TIS10.[1:0] = 01	-
	TO10	Output	0	0	0	TOS10.[1:0] = 01	PER1.LBEN = 0
P116	TI12	Input	1	x	0	TIS10.[5:4] = 11	-
	TO12	Output	0	0	0	TOS10.[5:4] = 11	PER1.LBEN = 0
P117	TI20	Input	1	x	0	TIS20.[1:0] = 11 TISELSE.7 = 0	-
	TO20	Output	0	0	0	TOS20.[1:0] = 11	PER1.LBEN = 0

(m) Alternate function of P12

Port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P121	These pins are not assigned to the Timer Array Unit function.						
P122							
P123							
P124							
P125	TI12	Input	1	x	0	TIS10.[5:4] = 10	-
	TO12	Output	0	0	0	TOS10.[5:4] = 10	-
P126	TI14	Input	1	x	0	TIS11.[1:0] = 11 STSEL1.0 = 0	-
	TO14	Output	0	0	0	TOS11.[1:0] = 11	-
P127	TI16	Input	1	x	0	TIS11.[5:4] = 11 RTCSEL.2 = 0	-
	TO16	Output	0	0	0	TOS11.[5:4] = 11	-

(n) Alternate function of P13

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P130	This pin is not assigned to the Timer Array Unit function.						
P131	TI21	Input	1	x	N/A	TIS20.[3:2] = 10	-
	TO21	Output	0	0		TOS20.[3:2] = 10	STSEL0.6 = 1 STSEL0.1 = 0
P132	TI20	Input	1	x	N/A	TIS20.[1:0] = 10 TISELSE.7 = 0	-
	TO20	Output	0	0		TOS20.[1:0] = 10	-
P133	TI22	Input	1	x	N/A	TIS20.[5:4] = 10	-
	TO22	Output	0	0		TOS20.[5:4] = 10	STSEL0.6 = 1
P134	TI24	Input	1	x	N/A	TIS21.[1:0] = 10	-
	TO24	Output	0	0		TOS21.[1:0] = 10	SGSEL.[2:0] = 000/001/100/ 101/110 STSEL1.3 = 0
P135	TI26	Input	1	x	N/A	TIS21.[5:4] = 10	-
	TO26	Output	0	0		TOS21.[5:4] = 10	~~SGSEL.1,0 = 00/01~~ SGSEL.[2:0] = 000/001/100/101
P136	TI00	Input	1	x	0	~~TIS00.0 = 1~~ TIS00.[1:0] = 01 TISELSE.6 = 0	-
	TO00	Output	0	0	0	~~TOS00.0 = 1~~ TOS00.[1:0] = 01	STSEL1.[7:6] = 00/01
P137	This pin is not assigned to the Timer Array Unit function.						

(o) Alternate function of P14

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
~~P14~~ P140	TI11	Input	1	x	N/A	TIS10.[3:2] = 10	-
	TO11	Output	0	0		TOS10.[3:2] = 10	-

(p) Alternate function of P15

port	Alternate function		PMxx	Pxx	Expanded control setting (Register.bit)
	Function name	I/O			
P150	These pins are not assigned to the Timer Array Unit function.				
P151					
P152					

No.48: Add a description of combination operation in “Chapter 6.6.2”

Changes are shown in red characters.

6.6.2 Basic rules of combination operation function

The basic rules of using the combination operation function are as follows.

(1) Only an even channel (channel 0, 2, 4, etc.) can be set as a master channel.

(2) Any channel, except channel 0, can be set as a slave channel.

(3) The slave channel must be lower than the master channel. (Slave channel number: Master channel number + 1, or more.)

Example: If channel 2 of the TAU0 is set as a master channel, channel 3 or those that follow (channels 3, 4, 5, etc.) can be set as a slave channel.

No.49: Correct the typo in CKSmn[1:0] bit of TMRmn register

The description of CKSmn[1:0] bit of TMRmn register is incorrect.

Target figure: Figure 6-53, Figure 6-57, Figure 6-61, Figure 6-65, Figure 6-69, Figure 6-73, Figure 6-74, Figure 6-78, Figure 6-79, Figure6-83, Figure 6-84

Figure 6-53 is shown below for reference. (Changes are shown in red characters.)

Figure 6-53. Example of Set Contents of Registers During Operation as Interval Timer/Square Wave Output

(a) Timer mode register mn (TMRmn)

TMRmn	CKSmn1 1/0	CKSmn0 1/0	0	CCSmn	MAS TERmn	STSmn2	STSmn1	STSmn0	0	0	MDmn3	MDmn2	MDmn1	MDmn0

Operation clock selection
00B: Selects CKm0 as operation clock of channel n.
~~01B~~ 10B: Selects CKm1 as operation clock of channel n.
~~10B~~ 01B: Selects CKm2 as operation clock of channel n.
11B: Selects CKm3 as operation clock of channel n.

No.50: Correct the description of RWAIT bit of RTCC1 register in “Figure 7-7”

[TU: TN-RL*-A058A/E, TN-RL*-A0123A/E]

Changes are shown in red characters.

Figure 7-7. Format of Real-time Clock Control Register 1 (RTCC1) (2/2)

RWAIT	Wait control of real-time clock
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value

This bit controls the operation of the counter.
Be sure to write “1” to it to read or write the counter value.
As the sub-count register is continuing to run, complete reading or writing within one second and turn back to 0.
When RWAIT = 1, it takes up to 1 clock (fRTC) until the counter value can be read or written (RWST = 1). Notes 1, 2
When reading or writing to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second).
Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant period interrupt.
When the sub-count register overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up.
However, when it wrote a value to second count register, it will not keep the overflow event.

Notes 1. When setting RWAIT=1 during 1 operating clock (f_{RTC}), after setting RTCE=1, it may take two clock time of the operation clock (f_{RTC}), until RWST bit is set to "1".
2. When setting RWAIT=1 during 1 operating clock (f_{RTC}), after returning from a stand-by (HALT mode, STOP mode and SNOOZE mode), it may take two clock time of the operation clock (f_{RTC}), until RWST bit is set to "1".

No.51: Correct the typo in the bit diagram in “Figure 7-19”

Add bit access definitions (“<n>”). Changes are shown in red characters.

Figure 7-19. Format of RTC1HZ pin Select Register (RTCSEL)

Address: FFFF36 After reset: 00H R/W

Symbol	~~7~~ <7>	~~6~~ <6>	5	4	~~3~~ <3>	~~2~~ <2>	~~1~~ <1>	~~0~~ <0>
RTCSEL	RTCOSEL1	RTCOSEL0	0	0	RTCTIS11	RTCTIS10	RTCTIS01	RTCTIS00

No.52: Correct the typo in the Notes at the bottom of “Figure 7-20”

Changes are shown in red characters.

Figure 7-20. Procedure for Starting Operation of Real-time Clock

Notes 1. First set the RTCEN bit to 1, while oscillation of the input clock (f_{RTC}) is stable.

2. Set up the SUBCUD register only if the watch error must be corrected. For details about how to calculate the correction value, see **7.4.6 Example of watch error correction of real-time clock**.

3. Confirm the procedure described in ~~**7.4.2 Shifting to STOP mode after starting operation**~~ **7.4.2 Shifting to HALT/STOP mode after starting operation** when shifting to ~~STOP mode~~ HALT/STOP mode without waiting for INTRTC = 1 after RTCE = 1.

No.53: Add explanations for the Cautions at the bottom of “Figures 7-22 and 7-23”

[TU: TN-RL*-A0123A/E]

Changes are shown in red characters.

Figure 7-22. Procedure for Reading Real-time Clock

Caution Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second. When reading to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.

Figure 7-23. Procedure for Writing Real-time Clock

Caution 1. Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second. When reading to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.

2. When changing the values of the SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR register while the counter operates (RTCE = 1), rewrite the values of the MIN register after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG, RIFG and RTCIF flags after rewriting the MIN register.

No.54: Correct the “Tables 9-2, 9-3”

Changes are shown in red characters.

Table 9-2. Settings of Register, and Output Latch When Using Alternate Function

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P75	TI22	Input	1	x	0	TIS20.[5:4] = 00	-
	TO22	Output	0	0	0	TOS20.[5:4] = 00	SGSEL.3 = 1
	PCL	Output	0	0	0	SGSEL.3 = 0	~~TOS20.[5:4] = 01/10~~ TOS20.[5:4] = 01/10/11
	SI01	Input	1	x	0	STSEL0.4 = 0	-
	SEG27	Output	x	x	1	-	-

Table 9-3. Settings of Register, and Output Latch When Using Alternate Function

port	Alternate function		PMxx	Pxx	LCDPFxx	Expanded control setting (Register.bit)	
	Function name	I/O				Enable function	Disable other function
P66	TI24	Input	1	x	N/A	TIS21.[1:0] = 00	-
	TO24	Output	0	0		TOS21.[1:0] = 00	SGSEL.3 = 0
	PCL	Output	0	0		SGSEL.3 = 1	~~TOS21.[1:0] = 01/10~~ TOS21.[1:0] = 01/10/11

No.55: Correct the typo in the bit diagram in “Figure 9-5”

Add bit access definitions (“<n>”). Changes are shown in red characters.

Figure 9-5. Format of sound generator and PCL pin select register (SGSEL)

Address: FFF3FH After reset: 00H R/W

Symbol	7	6	5	4	~~3~~ <3>	2	1	0
SGSEL	0	0	0	0	PCLSEL	SGSEL2	SGSEL1	SGSEL0

No.56: Add a Note to Table 10-4 when setting WINDOW[1:0] = 10B (75%)

[TU: TN-RL*-A068A/E]

Changes are shown in red characters.

Table 10-4. Setting Window Open Period of Watchdog Timer

WINDOW1	WINDOW0	Window Open Period of Watchdog Timer
0	0	Setting prohibited
0	1	50%
1	0	75% Note
1	1	100%

Note When the window open period is set to 75%, clearing the counter of the watchdog timer (writing ACH to WDTE) must proceed outside the corresponding period from among those listed below, over which clearing of the counter is prohibited (for example, confirming that the interval timer interrupt request flag (WDTIIF) of the watchdog timer is set).

WDCS2	WDCS1	WDCS0	Watchdog timer overflow time (f_{WDT} = 17.25 kHz (MAX.))	Period over which clearing the counter is prohibited when the window open period is set to 75%
0	0	0	$2^6/f_{WDT}$ (3.71 ms)	1.85 ms to 2.51 ms
0	0	1	$2^7/f_{WDT}$ (7.42 ms)	3.71 ms to 5.02 ms
0	1	0	$2^8/f_{WDT}$ (14.84 ms)	7.42 ms to 10.04 ms
0	1	1	$2^9/f_{WDT}$ (29.68 ms)	14.84 ms to 20.08 ms
1	0	0	$2^{11}/f_{WDT}$ (118.72 ms)	59.36 ms to 80.32 ms
1	0	1	$2^{13}/f_{WDT}$ (474.89 ms)	237.44 ms to 321.26 ms
1	1	0	$2^{14}/f_{WDT}$ (949.79 ms)	474.89 ms to 642.51 ms
1	1	1	$2^{16}/f_{WDT}$ (3799.18 ms)	1899.59 ms to 2570.04 ms

No.57: Correct the typo for A/D channel number

Changes are shown in red characters.

11.1 Function of A/D Converter

The A/D converter is a 10-bit resolution[Note] converter that converts analog input signals into digital values, and is configured to control analog inputs, including up to nine channels of A/D converter analog inputs (ANI0 to ~~ANI8~~ ANI10).

The A/D converter has the following function.

- **10-bit resolution A/D conversion[Note]**

  10-bit resolution A/D conversion is carried out repeatedly for one analog input channel selected from ANI0 to ~~ANI8~~ ANI10. Each time an A/D conversion operation ends, an interrupt request (INTAD) is generated (when in the select mode).

Note 8-bit resolution can also be selected by using the ADTYP bit of A/D converter mode register 2 (ADM2).

11.2 Configuration of A/D Converter

(1) ANI0 to ~~ANI8~~ ANI10 pins

These are the analog input pins of the up to ~~9 channels~~ 11 channels of the A/D converter. They input analog signals to be converted into digital signals. Pins other than the one selected as the analog input pin can be used as I/O port pins.

(9) AV_{REFP} pin

This pin inputs an external reference voltage (AV_{REFP}).

If using AV_{REFP} as the + side reference voltage of the A/D converter, set the ADREFP1 and ADREFP0 bits of A/D converter mode register 2 (ADM2) to 0 and 1, respectively.

The analog signals input to ANI0 to ~~ANI8~~ ANI10 are converted to digital signals based on the voltage applied between AV_{REFP} and the – side reference voltage (AV_{REFM}/V_{SS}).

In addition to AV_{REFP}, it is possible to select V_{DD} or the internal reference voltage (1.45 V) as the + side reference voltage of the A/D converter.

11.3 Registers Used in A/D Converter

(12) Port mode registers (PM0 to PM15)

When using the ANI0 to ~~ANI8~~ ANI10 pin for an analog input port, set the PMmn bit to 1. The output latches of Pnm at this time may be 0 or 1.

If the PMmn bits are set to 0, they cannot be used as analog input port pins.

The PMmn registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Remark For details of the port mode register other than ~~100-pin products~~ 128-pin products, see **4. 3 Registers Controlling Port Function**.

The ~~ANI8/P150 pin~~ ANI8/P150 to ANI10/P152 pins are as shown below depending on the settings of the A/D port configuration register (ADPC), analog input channel specification register (ADS), and PM15 registers.

Table 11-5. Setting Functions of ~~ANI8/P150 Pins~~ ANI8/P150 to ANI10/P152 Pins

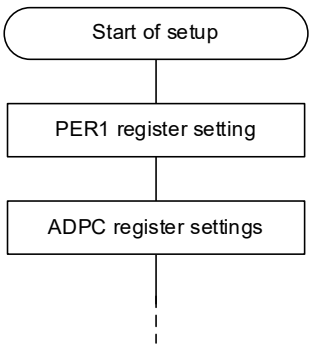
ADPC	PM15	ADS	ANI8/P150 to ANI10/P152 Pins
Digital I/O selection	Input mode	–	Digital input
	Output mode	–	Digital output
Analog input selection	Input mode	Selects ANI.	Analog input (to be converted)
		Does not select ANI.	Analog input (not to be converted)
	Output mode	Selects ANI.	Setting prohibited
		Does not select ANI.	

11.5 Input Voltage and Conversion Results

The relationship between the analog input voltage input to the analog input pins (ANI0 to ~~ANI8~~ ANI10) and the theoretical A/D conversion result (stored in the 10-bit A/D conversion result register (ADCR)) is shown by the following expression.

11.7 A/D Converter Setup Flowchart

Target figure: Figure 11-31, Figure 11-32, Figure 11-33, Figure 11-34



The ADCEN bit of the PER1 register is set (1), and supplying the clock starts.

The ports are set to analog input.
ANI0 to ~~ANI8~~ ANI10 pins: Set using the ADPC register

11.10 Cautions for A/D Converter

(2) Input range of ANI0 to ANI10 pins

Observe the rated range of the ANI0 to ~~ANI8~~ ANI10 pins input voltage. If a voltage of V_{DD} and AV_{REFP} or higher and V_{SS} and AV_{REFM} or lower (even in the range of absolute maximum ratings) is input to an analog input channel, the converted value of that channel becomes undefined. In addition, the converted values of the other channels may also be affected.

(4) Noise countermeasures

To maintain the 10-bit resolution, attention must be paid to noise input to the AV_{REFP}, V_{DD}, ANI0 to ~~ANI8~~ ANI10 pins.

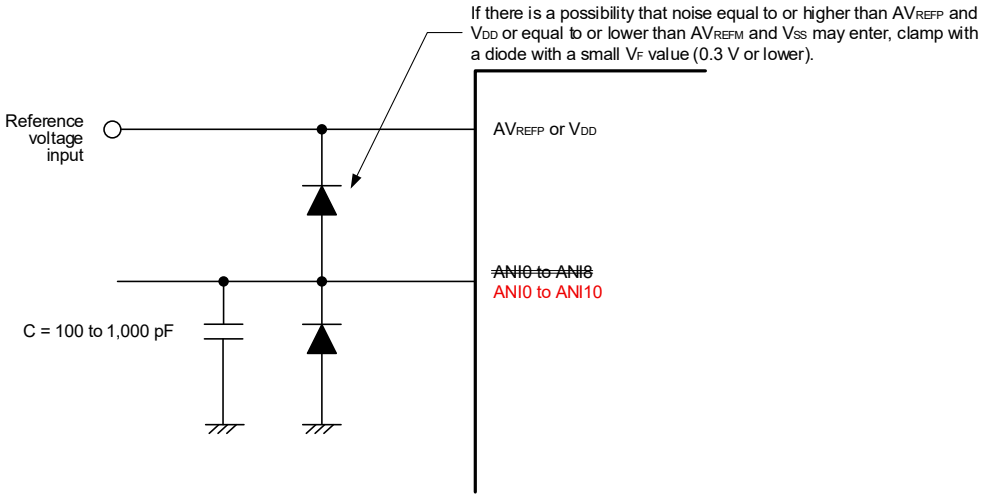
<1> Connect a capacitor with a low equivalent resistance and a good frequency response to the power supply.

<2> The higher the output impedance of the analog input source, the greater the influence. To reduce the noise, connecting external C as shown in Figure 11-44 is recommended.

<3> Do not switch these pins with other pins during conversion.

<4> The accuracy is improved if the HALT mode is set immediately after the start of conversion.

Figure 11-44. Analog Input Pin Connection



(5) Analog input (ANIn) pins

<1> The analog input pins (ANI0 to ~~ANI8~~ ANI10) are also used as input port pins (P20 to P27, ~~P150~~ P150 to P152). When A/D conversion is performed with any of the ANI0 to ~~ANI8~~ ANI10 pins selected, do not change the output value to P20 to P27 and ~~P150~~ P150 to P152 while conversion is in progress; otherwise the conversion accuracy may be degraded.

<2> If the pins adjacent to the pins currently used for A/D conversion is used as digital I/O ports, the expected value of the A/D conversion may not be obtained due to coupling noise. Take care not to input or output such a pulse to these pins.

(6) Input impedance of analog input (ANIn) pins

This A/D converter charges a sampling capacitor for sampling during sampling time.

Therefore, only a leakage current flows when sampling is not in progress, and a current that charges the capacitor flows during sampling. Consequently, the input impedance fluctuates depending on whether sampling is in progress, and on the other states.

To make sure that sampling is effective, however, it is recommended to keep the output impedance of the analog input source to within 1 kΩ, and to connect a capacitor of about 100 pF to the ~~ANI0 to ANI8 pins~~ ANI0 to ANI10 pins (see **Figure 11-44**).

(10) Internal equivalent circuit

Delete any unnecessary descriptions in the “Table 11-6”.

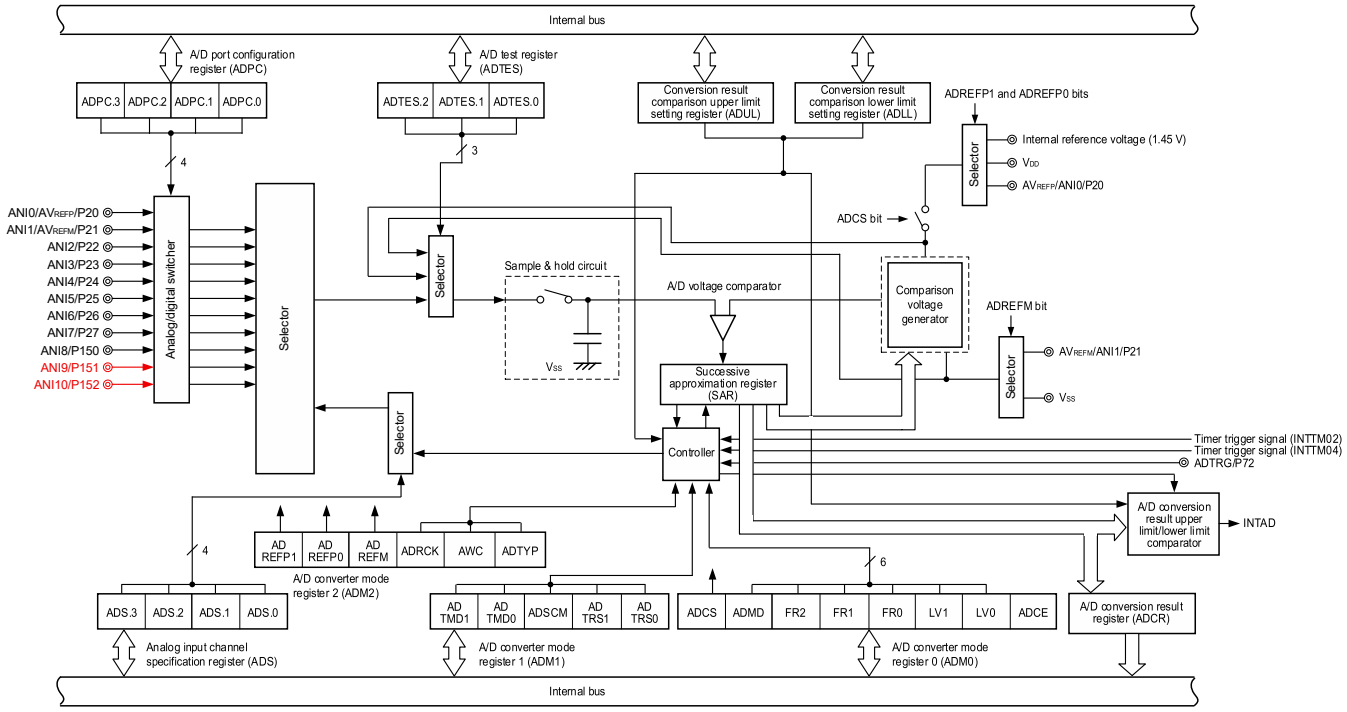
Table 11-6. Resistance and Capacitance Values of Equivalent Circuit (Reference Values)

AVREFP, VDD	ANIn pin	R1 [kΩ]	C1 [pF]	C2 [pF]
4.0 ≤ VDD ≤ 5.5	ANI0 to ANI7	14	8	2.5
	~~ANI8~~ ANI8 to ANI10	18	8	7.0
2.7 ≤ VDD ≤ 4.0	ANI0 to ANI7	39	8	2.5
	~~ANI8~~ ANI8 to ANI10	53	8	7.0
~~1.8 ≤ VDD ≤ 2.7~~	~~ANI0 to ANI7~~	~~231~~	~~8~~	~~2.5~~
	~~ANI8~~	~~321~~	~~8~~	~~7.0~~

No.58: Update the “Figure 11-1”

Changes are shown in red characters.

Figure 11-1. Block Diagram of A/D Converter



No.59: Correct the typos in the bit diagram in “Figures 11-2, 11-13, 11-11, 11-13”

Changes are shown in red characters.

Figure 11-2. Format of Peripheral Enable Register 1 (PER1)

Address: F00F1H After reset: 00H R/W

Symbol	<7>	~~<6>~~ 6	<5>	<4>	<3>	~~<2>~~ 2	~~<1>~~ 1	~~<0>~~ 0
PER1	ADCEN	0	MTRCEN	SGEN	~~0~~ LBEN	0	0	0

Figure 11-3. Format of A/D Converter Mode Register 0 (ADM0)

Address: FFF30H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	<0>
ADM0	ADCS	ADMD	FR2Note 1	FR1Note 1	FR0Note 1	~~DV1~~ LV1Note 1	~~DV0~~ LV0Note 1	ADCE

Figure 11-11. Format of Analog Input Channel Specification Register (ADS)

Address: FFF31H After reset: 00H R/W

Symbol	7	6	5	4	~~<3>~~ 3	~~<2>~~ 2	~~<1>~~ 1	~~<0>~~ 0
ADS	0	0	0	0	ADS.3	ADS.2	ADS.1	ADS.0

Figure 11-13. Format of Conversion Result Comparison Lower Limit Setting Register (ADLL)

Address: F0012H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADLL	ADLL.7	ADLL.6	ADLL.5	ADLL.4	ADLL.3	~~0~~ ADLL.2	ADLL.1	ADLL.0

No.60: Correct the item name in the table in Note 2 of the “Figure 11-4”

Changes are shown in red characters.

Figure 11-4. Timing Chart When A/D Voltage Comparator Is Used

Note 2. In starting conversion, the longer will take up to following time.

ADM0			Conversion clock (f_{AD})	~~Conversion Operation Time (f_{CLK} clock)~~ Conversion Start Time (f_{CLK} clock)	
FR2	FR1	FR0		Software trigger mode / Hardware trigger no-wait mode	Hardware trigger wait mode
0	0	0	f_{CLK}/64	63	1
0	0	1	f_{CLK}/32	31	
0	1	0	f_{CLK}/16	15	
0	1	1	f_{CLK}/8	7	
1	0	0	f_{CLK}/6	5	
1	0	1	f_{CLK}/5	4	
1	1	0	f_{CLK}/4	3	
1	1	1	f_{CLK}/2	1	

No.61: Update the “Table 12-1”

Add SNFEN0 register and add Port 11 to the target pins. Changes are shown in red characters.

Table 12-1. Configuration of Serial Array Unit

Item	Configuration
Shift register	16 bits
Buffer register	Serial data register mn (SDRmn)[Note]
Serial clock I/O	SCK00, SCK01, SCK10 pins (for 3-wire serial I/O), SCL11 pins (for simplified I^2C)
Serial data input	SI00, SI01, SI10 pins (for 3-wire serial I/O) , RxD0 pin (for UART)
Serial data output	SO00, SO01, SO10 pins (for 3-wire serial I/O) , TxD0 pin (for UART)
Serial data I/O	SDA11 pins (for simplified I^2C)
Control registers	<Registers of unit setting block> • Peripheral enable registers 0 (PER0) • Serial clock select register m (SPSm) • Serial channel enable status register m (SEm) • Serial channel start register m (SSm) • Serial channel stop register m (STm) • Serial output enable register m (SOEm) • Serial output register m (SOm) • Serial output level register m (SOLm) • Noise filter enable register for SAU (SNFEN0)
	<Registers of each channel> • Serial data register mn (SDRmn) • Serial mode register mn (SMRmn) • Serial communication operation setting register mn (SCRmn) • Serial status register mn (SSRmn) • Serial flag clear trigger register mn (SIRmn) • Serial communication pin select register (~~STSEL~~ STSEL0, STSEL1)
	• Port input mode registers 0, 1, 3, 5 to 7, 11, 13 (PIM0, PIM1, PIM3, PIM5 to PIM7, PIM11, PIM13) • Port output mode register (POM) • Port mode registers 0, 1, 3, 5 to 7, 11, 13 (PM0, PM1, PM3, PM5 to PM7, PM11, PM13) • Port registers 0, 1, 3, 5 to 7, 11, 13 (P0, P1, P3, P5 to P7, P11, P13)

No.62: Update block diagram of serial array unit

Changes are shown in red characters.

Figure 12-1. Block Diagram of Serial Array Unit 0

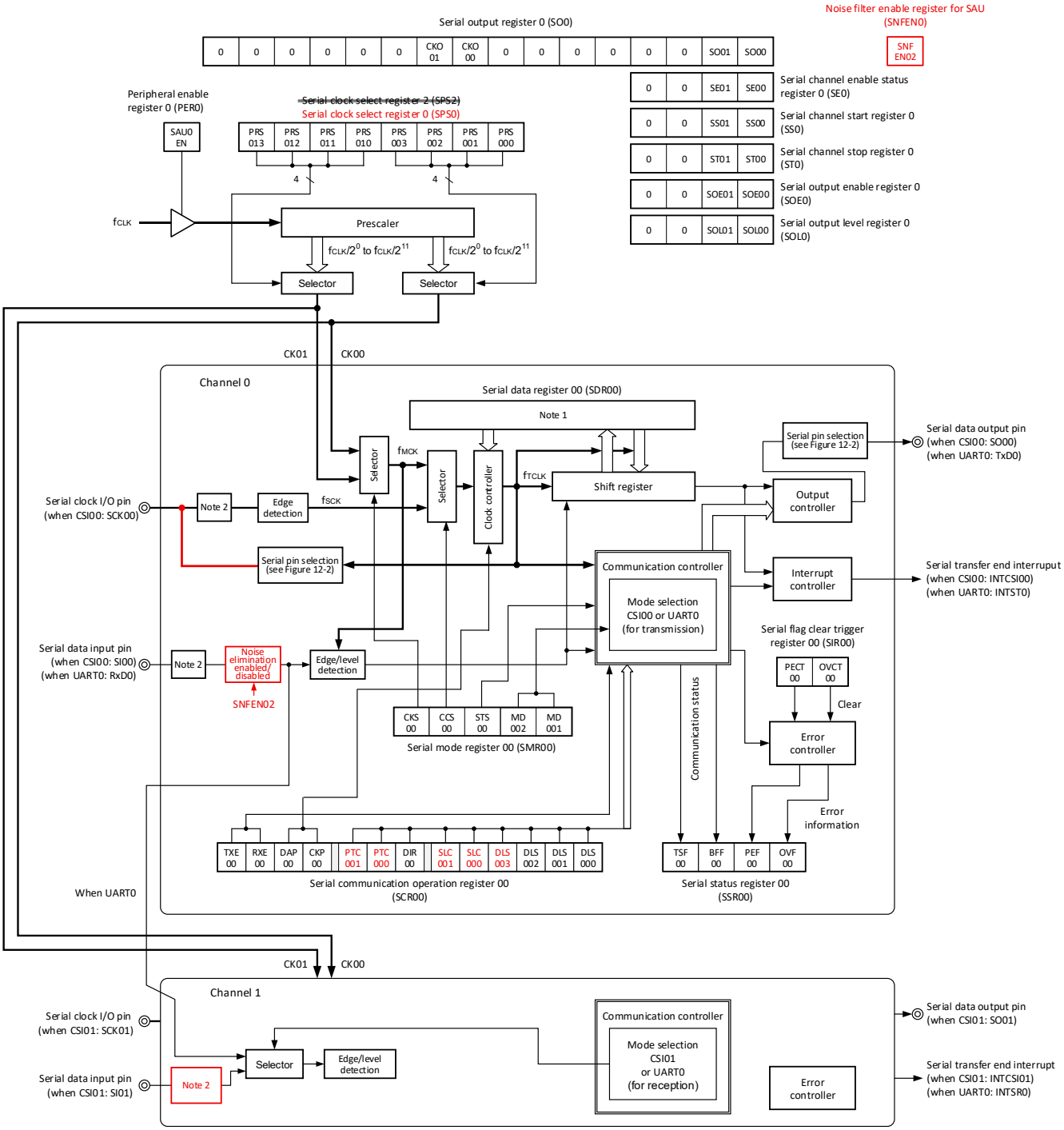


Figure 12-2. Port Configuration Diagram of Serial Array Unit 0

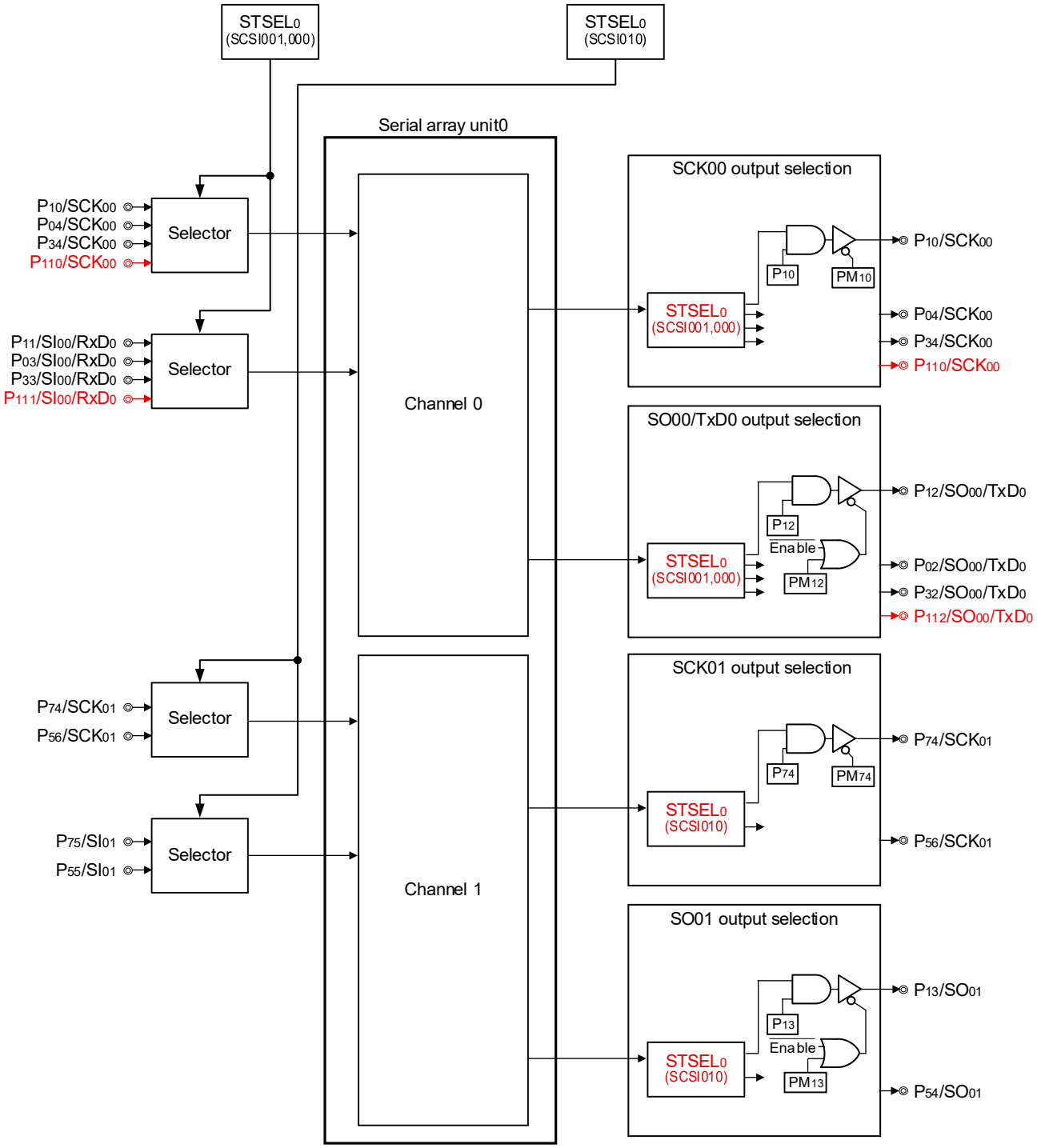
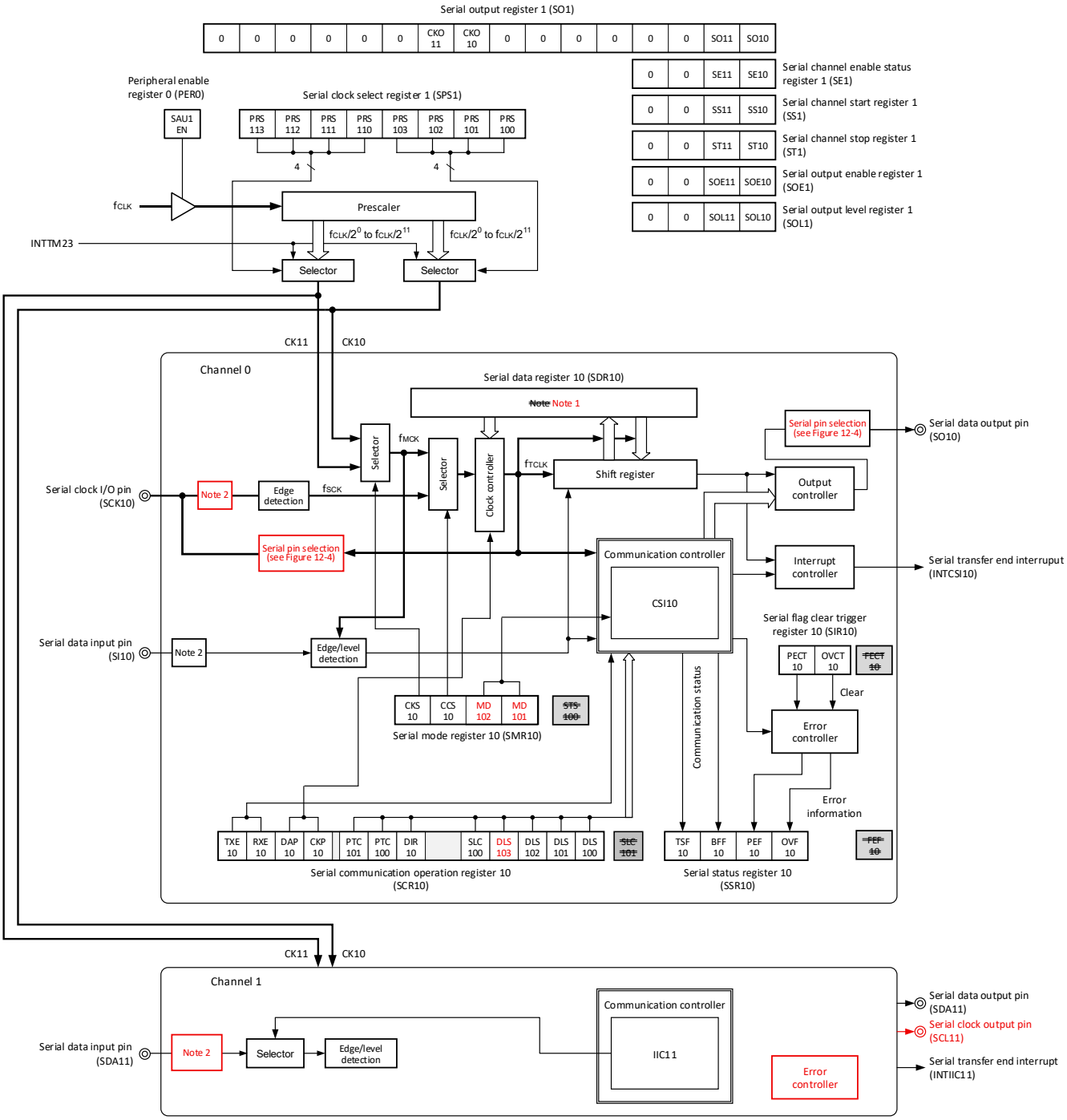


Figure 12-3. Block Diagram of Serial Array Unit 1



Notes 1. When operation is stopped (SEmn = 0), the higher 7 bits become the clock division setting section and the lower bits are fixed to 0.
During operation (SEmn = 1), it becomes a buffer register.

2. Serial pin selection (see ~~Figure 12-2~~ Figure 12-4)

No.63: Correct the typo for SAU channel number in “Chapters 12.2, 12.3”

Changes are shown in red characters.

12.2 Configuration of Serial Array Unit

(2) Serial data register mn (SDRmn)

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 1),
p: CSI number (p = 00, 01, 10), q: UART number (~~q = 0 to 2~~ q = 0), r: IIC number (r = 11)

12.3 Registers Controlling Serial Array Unit

(4) Serial communication operation setting register mn (SCRmn)

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 1), p: CSI number (p = ~~00, 01, 10, 11~~ 00, 01, 10)

12.7 Operation of Simplified I²C (IIC11) Communication

Figure 12-91. Example of Contents of Registers for Address Field Transmission of Simplified I²C (~~IIC00, IIC01, IIC11, IIC20, IIC21~~ IIC11) (2/2)

12.7.2 Data transmission

12.7.3 Data reception

Simplified I²C	IIC11
Target channel	~~Channel 3 of SAU0~~ Channel 1 of SAU1
Pins used	SCL11, SDA11 Note
:	:

No.64: Correct the description of Caution 1 in “Figure 12-6”

Changes are shown in red characters.

Figure 12-6. Format of Peripheral Enable Register 0 (PER0)

Cautions 1. When setting serial array unit m, be sure to set the SAUmEN bit to 1 first. If SAUmEN = 0, writing to a control register of serial array unit m is ignored, and, even if the register is read, only the default value is read (except for Serial communication pin select register (~~STSEL~~ STSEL0, STSEL1), noise filter enable register (SNFEN0), port input mode register (PIM0, PIM1, PIM3, PIM5 to PIM7, PIM11, PIM13), port output mode register (POM), port mode registers (PM0, PM1, PM3, PM5 to PM7, PM11, PM13), and port registers (P0, P1, P3, P5 to P7, P11, P13)).

No.65: Correct the typo in SDRmn[15:9] bit in “Figure 12-10”

Changes are shown in red characters.

Figure 12-10. Format of Serial Data Register mn (SDRmn)

SDRmn[15:9]							Setting of division ratio of operation clock (fMCK)
0	0	0	0	0	0	0	~~fMCK~~ fMCK/2
0	0	0	0	0	0	1	~~fMCK/2~~ fMCK/4
0	0	0	0	0	1	0	~~fMCK/3~~ fMCK/6
0	0	0	0	0	1	1	~~fMCK/4~~ fMCK/8
• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •
1	1	1	1	1	1	0	~~fMCK/127~~ fMCK/254
1	1	1	1	1	1	1	~~fMCK/128~~ fMCK/256

No.66: Correct the description of SIRmn, SSRmn registers in “Figures 12-11, 12-12”

Changes are shown in red characters.

Figure 12-11. Format of Serial Flag Clear Trigger Register mn (SIRmn)

Address: F0104H, F0105H (SIR00), F0106H, F0107H (SIR01), F0134H, F0135H (SIR10), F0136H, F0137H (SIR11) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIRmn	0	0	0	0	0	0	0	0	0	0	0	0	0	FECTmn[Note]	PECTmn	OVCTmn

PECT~~11~~mn	~~Clear trigger of parity error of SCL11~~ Clear trigger of parity error of channel n
0	No trigger operation
1	~~Clears PEF11 bit of SSR11 register to 0.~~ Clears PEFmn bit of SSRmn register to 0.

Note The SIR01 register only.

Figure 12-12. Format of Serial Status Register mn (SSRmn)

PEFmn	~~Parity error detection flag of channel 11~~ Parity error detection flag of channel n
0	No error occurs.
1	An error occurs (during UART reception) or ACK is not detected (during I^2C transmission).
<Clear condition> • 1 is written to the PECTmn bit of the SIRmn register. <Set condition> • No ACK signal is returned from the slave channel at the ACK reception timing during I^2C transmission (ACK is not detected). • The parity of the transmit data and the parity bit do not match when UART reception ends (parity error).	

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 1), ~~PEF bit is SSR11 only~~

No.67: Correct the typo in after reset value of SOm register

Changes are shown in red characters.

12.3 Registers Controlling Serial Array Unit

(12) Serial output register m (SOm)

Reset signal generation clears the SOm register to ~~0F0FH~~ 0303H.

No.68: Correct the description of STSEL0 register in “Figure 12-19”

Changes are shown in red characters.

Figure 12-19. Serial communication pin select register 0 (STSEL0)

~~STSCSI00~~ SCSI001	SCSI000	CSI00/UART0 communication pin selection		
		SCK00	SI00/RxD0	SO00/TxD0
0	0	P10	P11	P12
0	1	P04	P03	P02
1	0	P34	P33	P32
~~Other than the above~~		~~Setting prohibited (same as “00” setting)~~		
1	1	P110	P111	P112

No.69: Add a description of SNFEN0 register

The SNFEN0 register description was omitted.

12.3 Registers Controlling Serial Array Unit

(15) Noise filter enable register for SAU (SNFEN0)

The SNFEN0 register is used to set whether the noise filter can be used for the input signal from the RxD0 pin.

When the noise filter is enabled, CPU/peripheral hardware clock (f_{CLK}) is synchronized with 2-clock match detection.

When the noise filter is OFF, only synchronization is performed with the CPU/peripheral hardware clock (f_{MCK}).

Set the SNFEN0 register by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears the SNFEN0 register to 00H.

Figure 12-21. Format of Noise filter enable register for SAU (SNFEN0)

Address: F006DH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SNFEN0	0	0	0	0	0	SNFEN02	0	0

SNFEN02	Use of noise filter of RxD0 pin
0	Noise filter OFF
1	Noise filter ON

No.70: Add a description of PIM11, PM11 registers

Changes are shown in red characters.

12.3 Registers Controlling Serial Array Unit

(16) Port input mode registers 0, 1, 3, 5 to 7, 11, and 13 (PIM0, PIM1, PIM3, PIM5 to PIM7, PIM11, PIM13)

These registers set the input buffer of ports 0, 1, 3, 5 to 7, 11, and 13 in 1-bit units.

The PIM0, PIM1, PIM3, PIM5 to PIM7, PIM11, and PIM13 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears the PIM0, PIM1, PIM3, PIM5 to PIM7, PIM11, and PIM13 registers to 00H.

Figure 12-22. Format of Port Input Mode Registers 0, 1, 3, 5 to 7, 11, and 13 (PIM0, PIM1, PIM3, PIM5 to PIM7, PIM11, PIM13)

Address: F004BH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIM11	PIM11.7	PIM11.6	PIM11.5	PIM11.4	PIM11.3	PIM11.2	PIM11.1	PIM11.0

Bit name	PIM5.2	PIM5.1	PIM5.0	PIM3.1	PIM1.7	PIM1.1	PIM1.0	PIM0.1
Port input function	P52/SI10	P51/SCK10	P50/SDA11	P31/SDA11	P17	P11/LRxD1/ SI00	P10/SCK00	P01/CRxD0
Bit name	-	PIM13.5	PIM7.0	PIM6.3	PIM6.1	PIM5.7	PIM5.6	PIM5.5
Port input function	-	P135/CRxD1	P70/CRxD0/ LRxD0	P63/CRxD1	P61/SDA11	P57	P56/SCK01	P55/SI01
Bit name	PIM11.7	PIM11.6	PIM11.5	PIM11.4	PIM11.3	PIM11.2	PIM11.1	PIM11.0
Port input function	P117/DBD7	P116/DBD6	P115/DBD5	P114/DBD4	P113/DBD3	P112/DBD2	P111/DBD1	P112/DBD0

(18) Port mode registers 0, 1, 3, 5 to 7, 11, 13 (PM0, PM1, PM3, PM5 to PM7, PM11, PM13)

These registers set input/output of ports 0, 1, 3, 5 to 7, 11, 13 in 1-bit units.

When using the ports (such as P02/ SO00/TxD0/TI02/TO02/ TI12/TO12) to be shared with the serial data output pin for serial data output, set the port mode register (PMxx) bit corresponding to each port to 0. And set the port register (Pxx) bit corresponding to each port to 1.

Example: When using P02/SO00/TxD0/TI02/TO02/TI12/TO12 for serial data output or serial clock output

Set the PM0.2 bit of the port mode register 0 to 0.

Set the P0.2 bit of the port register 0 to 1.

When using the ports (such as P03/SI00/RxD0/TI03/TO03/TI13/TO13) to be shared with the serial data input pin for serial data input, set the port mode register (PMxx) bit corresponding to each port to 1. At this time, the port register (Pxx) bit may be 0 or 1.

Example: When using P03/SI00/RxD0/TI03/TO03/TI13/TO13 for serial data input

Set the PM0.3 bit of port mode register 0 to 1.

Set the P0.3 bit of port register 0 to 0 or 1.

The PM0, PM1, PM3, PM5 to PM7, PM11, PM13 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets the PM0, PM1, PM3, PM5 to PM7, PM11, PM13 registers to FFH.

Figure 12-24. Format of Port Mode Registers 0, 1, 3, 5 to 7, 11, 13 (PM0, PM1, PM3, PM5 to PM7, PM11, PM13)

Address: FFF26H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM6	~~PM6.7~~ 1	PM6.6	PM6.5	PM6.4	PM6.3	PM6.2	PM6.1	PM6.0

Address: FFF27H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM7	~~PM7.7~~ 1	~~PM7.6~~ 1	PM7.5	PM7.4	PM7.3	PM7.2	PM7.1	PM7.0

Address: FFF2BH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM11	PM11.7	PM11.6	PM11.5	PM11.4	PM11.3	PM11.2	PM11.1	PM11.0

No.71: Correct the typo of Note in “Tables 12-2, 12-4”

Changes are shown in red characters.

Table 12-2. Selection of Operation Clock For 3-Wire Serial I/O

Table 12-4. Selection of Operation Clock For Simplified I^2C

Note Stop the operation of the serial array unit (SAU) (by setting ~~bits 3 to 0~~ bits 1 and 0 of ST0 register and bits 1 and 0 of ~~ST1 and STS register~~ ST1 register to 1) before changing operation clock (f_{CLK}) selection (by changing the system clock control register (CKC) value).

No.72: Correct the port settings in the flowchart in “Figure 12-75”

Changes are shown in red characters.

Figure 12-75. Initial Setting Procedure for UART Transmission

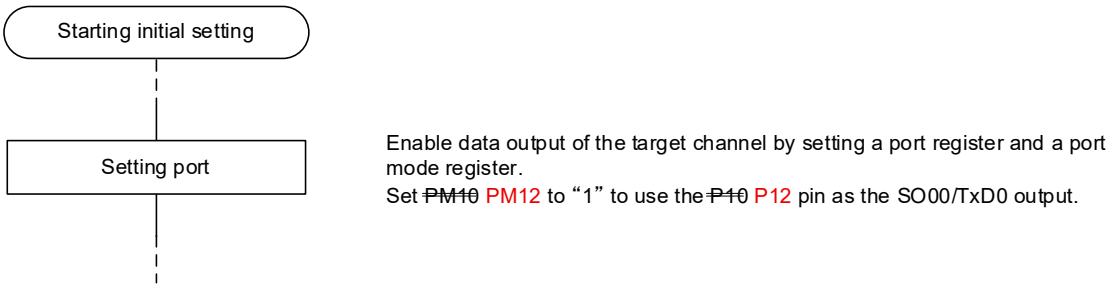
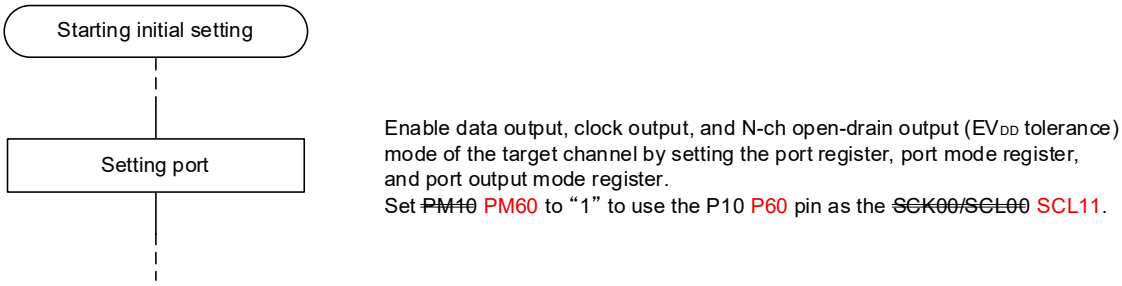


Figure 12-92. Initial Setting Procedure for Address Field Transmission



No.73: Update the register conditions table for SAU

Add Tables 12-8 (CSI00, SCSI00[1:0] = 11B). Correct Tables 12-5 (CSI00, SCSI00[1:0] = 00B), 12-11 (CSI10, SCSI100 = 0), 12-12 (CSI10, SCSI100 = 1), and 12-16 (UART0). Changes are shown in red characters.

Table 12-5. Relationship between register settings and pins (Channel 0 of unit 0: CSI00, SCSI001 = 0, SCSI000 = 0)

SE 00 Note1	MD 002	MD 001	SOE 00	SO 00	CKO 00	TXE 00	RXE 00	PM10	P10	PM11	P11	PM12	P12	Operation mode	Pin Function		
															P10/LTxD1/ SCK00/TI10/ TO10/INTP4	P11/LRxD1/ INTPLR1/ SI00/RxD0/ TI11/TO11	P12/SO00/ TxD0/TI12/ TO12/INTP2
0	0	0	0	1	1	0	0	× Note2	× Note2	× Note2	× Note2	× Note2	× Note2	Operation stop mode	P10/LTxD1/ TI10/TO10/ INTP4	P11/LRxD1/ INTPLR1/ TI11/TO11	P12/TI12/ TO12/INTP2
1	0	0	0	1	1	0	1	1	×	1	×	× Note2	× Note2	Slave CSI00 reception	SCK00 (input)	SI00	P12/TI12/ TO12/INTP2
			1	0/1 Note3	1	1	0	1	×	× Note2	× Note2	0	1	Slave CSI00 transmission	SCK00 (input)	P11/LRxD1/ INTPLR1/ TI11/TO11	SO00
			1	0/1 Note3	1	1	1	1	×	1	×	0	1	Slave CSI00 transmission/ reception	SCK00 (input)	SI00	SO00
			0	1	0/1	0	1	0	1	1	×	× Note2	× Note2	Master CSI00 reception	SCK00 (output)	SI00	P12/~~SO00~~/ TI12/TO12/ INTP2
			1	0/1 Note3	0/1 Note3	1	0	0	1	× Note2	× Note2	0	1	Master CSI00 transmission	SCK00 (output)	P11/LRxD1/ INTPLR1/ TI11/TO11	SO00
			1	0/1 Note3	0/1 Note3	1	1	0	1	1	×	0	1	Master CSI00 transmission/ reception	SCK00 (output)	SI00	SO00

Notes 1. The SE0 register is a read-only status register which is set using the SS0 and ST0 registers.

2. This pin can be set as a port function pin or other alternate function pin.

3. This is 0 or 1, depending on the communication operation. For details, refer to **12.3 (12) Serial output register m (SOm)**.

Table 12-8. Relationship between register settings and pins (Channel 0 of unit 0: CSI00, SCSI001 = 1, SCSI000 = 1)

SE 00 Note1	MD 002	MD 001	SOE 00	SO 00	CKO 00	TXE 00	RXE 00	PM 110	P110	PM 111	P111	PM 112	P112	Operation mode	Pin Function		
															P110/SCK00/ TI00/TO00	P111/SI00/ RxD0/TI02/ TO02	P112/SO00/ TxD0/TI04/ TO04
0	0	0	0	1	1	0	0	× Note2	× Note2	× Note2	× Note2	× Note2	× Note2	Operation stop mode	P110/TI00/ TO00	P111/TI02/ TO02	P112/TI04/ TO04
1	0	0	0	1	1	0	1	1	×	1	×	× Note2	× Note2	Slave CSI00 reception	SCK00 (input)	SI00	P112/TI04/ TO04
			1	0/1 Note3	1	1	0	1	×	× Note2	× Note2	0	1	Slave CSI00 transmission	SCK00 (input)	P111/TI02/ TO02	SO00
			1	0/1 Note3	1	1	1	1	×	1	×	0	1	Slave CSI00 transmission/ reception	SCK00 (input)	SI00	SO00
			0	1	0/1	0	1	0	1	1	×	× Note2	× Note2	Master CSI00 reception	SCK00 (output)	SI00	P112/TI04/ TO04
			1	0/1 Note3	0/1 Note3	1	0	0	1	× Note2	× Note2	0	1	Master CSI00 transmission	SCK00 (output)	P111/TI02/ TO02	SO00
			1	0/1 Note3	0/1 Note3	1	1	0	1	1	×	0	1	Master CSI00 transmission/ reception	SCK00 (output)	SI00	SO00

Notes 1. The SE0 register is a read-only status register which is set using the SS0 and ST0 registers.

2. This pin can be set as a port function pin or other alternate function pin.

3. This is 0 or 1, depending on the communication operation. For details, refer to **12.3 (12) Serial output register m (SOm)**.

Table ~~12-10~~ 12-11. Relationship between register settings and pins (Channel 0 of unit 1: CSI10, SCSI100 = 0)

SE 10 Note 1	MD 102	MD 101	SOE 10	SO 10	CKO 10	TXE 10	RXE 10	~~PM10~~ PM 133	P133	PM 132	P132	PM 131	P131	Operation mode	Pin Function		
															~~P133/SCK10/ TI22/TO22~~ P133/SCK10/ TI22/TO22	~~P132/SI00/ LRxD1/INTPLR1/ TI20/TO20~~ P132/SI10/ LRxD1/INTPLR1/ TI20/TO20	~~P131/SO10/ LTxD1/TI21/ TO21~~ P131/SO10/ LTxD1/TI21/ TO21
0	0	0	0	1	1	0	0	× Note2	× Note2	× Note2	× Note2	× Note2	× Note2	Slave CSI10 reception	~~P132/INTP4/ CRxD/LTxD1/ TI00/P133/ TI22/TO22~~ P133/ TI22/TO22	~~P132/INTP5/ LRxD1/INTPLR1/ TI20/TO20~~ P132/LRxD1/ INTPLR1/ TI20/TO20	~~P131/TI21/ TO21~~ P131/LTxD1/ TI21/TO21
1	0	0	0	1	1	0	1	1	×	1	×	× Note2	× Note2	Slave CSI10 transmission	SCK10 (input)	SI10	~~P131/TI21/ TO21~~ P131/LTxD1/ TI21/TO21
			1	0/1 Note3	1	1	1	1	×	× Note2	× Note2	0	1	Slave CSI10 transmission/ reception	SCK10 (input)	~~P132/INTP5/ TI20/TO20~~ P132/LRxD1/ INTPLR1/ TI20/TO20	SO10
			1	0/1 Note3	1	1	1	1	×	1	×	0	1	Master CSI10 reception	SCK10 (input)	SI10	SO10
			0	1	0/1	0	1	0	1	1	×	× Note2	× Note2	Master CSI10 transmission	SCK10 (output)	SI10	~~P131/TI21/ TO21~~ P131/LTxD1/ TI21/TO21
			1	0/1 Note3	0/1 Note3	1	0	0	1	× Note2	× Note2	0	1	Master CSI10 transmission/ reception	SCK10 (output)	~~P132/INTP5/ TI20/TO20~~ P132/LRxD1/ INTPLR1/ TI20/TO20	SO10
			1	0/1 Note3	0/1 Note3	1	1	0	1	1	×	0	1	Slave CSI10 reception	SCK10 (output)	SI10	SO10

Notes 1. The SE1 register is a read-only status register which is set using the SS1 and ST1 registers.

2. This pin can be set as a port function pin or other alternate function pin.

3. This is 0 or 1, depending on the communication operation. For details, refer to **12.3 (12) Serial output register m (SOm)**.

Table ~~12-11~~ 12-12. Relationship between register settings and pins (Channel 0 of unit 1: CSI10, SCSI100 = 1)

SE 10 Note 1	MD 102	MD 101	SOE 10	SO 10	CKO 10	TXE 10	RXE 10	~~PM10~~ PM 51	P51	PM 52	P52	PM 53	P53	Operation mode	Pin Function		
															P51/TI04/ TO04/SCK10	P52/TI06/ TO06/SI10	P53/TI13/ TO13/SO10
0	0	0	0	1	1	0	0	× Note2	× Note2	× Note2	× Note2	× Note2	× Note2	Slave CSI10 reception	P51/TI04/ TO04	P52/TI06/ TO06	P53/TI13/ TO13
1	0	0	0	1	1	0	1	1	×	1	×	× Note2	× Note2	Slave CSI10 transmission	SCK10 (input)	SI10	P53/TI13/ TO13
			1	0/1 Note3	1	1	1	1	×	× Note2	× Note2	0	1	Slave CSI10 transmission/ reception	SCK10 (input)	P52/TI06/ TO06	SO10
			1	0/1 Note3	1	1	1	1	×	1	×	0	1	Master CSI10 reception	SCK10 (input)	SI10	SO10
			0	1	0/1	0	1	0	1	1	×	× Note2	× Note2	Master CSI10 transmission	SCK10 (output)	SI10	P53/TI13/ TO13
			1	0/1 Note3	0/1 Note3	1	0	0	1	× Note2	× Note2	0	1	Master CSI10 transmission/ reception	SCK10 (output)	P52/TI06/ TO06	SO10
			1	0/1 Note3	0/1 Note3	1	1	0	1	1	×	0	1	Slave CSI10 reception	SCK10 (output)	SI10	SO10

Notes 1. The SE1 register is a read-only status register which is set using the SS1 and ST1 registers.

2. This pin can be set as a port function pin or other alternate function pin.

3. This is 0 or 1, depending on the communication operation. For details, refer to **12.3 (12) Serial output register m (SOm)**.

Table ~~12-15~~ 12-16. Relationship between register settings and pins (Channel 0 and 1 of unit 0: UART0, SCSI001 = 0/1, SCSI000 = 0/1)

SE 00 Note 1	SE 01 Note 1	MD 002	MD 001	MD 012	MD 011	SOE 00	SO 00	TXE 00	RXE 01	Port-related register (bit)				Operation mode	Pin Function	
										PM11	P11	PM12	P12		P11/LRxD1/INTPLR1/ SI00/RxD0/TI11/TO11	P12/SO00/TxD0/TI12/ TO12/INTP2
										PM03	P03	PM02	P02		P03/SI00/RxD0/TI03/TO03/ TI13/TO13	P02/SO00/TxD0/TI02/TO02/ TI12/TO12
										PM33	P33	PM32	P32		P33/TI23/TO23/SI00/RxD0	P32/TI22/TO22/SO00/TxD0
										PM111	P111	PM112	P112		P111/DBD1/SI00/RxD0/ TI02/TO02	P112/DBD2/SO00/TxD0/ TI04/TO04/
0	0	×	×	×	×	0	1	0	0	× Note2	× Note2	× Note2	× Note2	Operation stop mode	~~P11/LRxD1/INTPLR1/ SI00/RxD0/TI11/TO11~~ P11/LRxD1/INTPLR1/ TI11/TO11	~~P12/SO00/TxD0/TI12/ TO12/INTP2~~ P12/TI12/TO12/INTP2
															P03/TI03/TO03/TI13/TO13	P02/TI02/TO02/TI12/TO12
															P33/TI23/TO23	P32/TI22/TO22
															P111/DBD1/TI02/TO02	P112/DBD2/TI04/TO04/
0	1	×	×	0	1	0	1	0	1	1	×	× Note2	× Note2	UART0 reception	RxD0 (SCSI00[1:0] = 00B)	P12/TI12/TO12/INTP2
															RxD0 (SCSI00[1:0] = 01B)	P02/TI02/TO02/TI12/TO12
															RxD0 (SCSI00[1:0] = 10B)	P32/TI22/TO22
															RxD0 (SCSI00[1:0] = 11B)	P112/DBD2/TI04/TO04/
1	0	0	1	×	×	1	0/1 Note3	1	0	×	×	0	1	UART0 transmission	P11/LRxD1/INTPLR1/ TI11/TO11	TxD0 (SCSI00[1:0] = 00B)
															P03/TI03/TO03/TI13/TO13	TxD0 (SCSI00[1:0] = 01B)
															P33/TI23/TO23	TxD0 (SCSI00[1:0] = 10B)
															P111/DBD1/TI02/TO02	TxD0 (SCSI00[1:0] = 11B)
1	1	0	1	0	1	1	0/1 Note3	1	1	1	×	0	1	UART0 transmission/ reception	RxD0 (SCSI00[1:0] = 00B)	TxD0 (SCSI00[1:0] = 00B)
															RxD0 (SCSI00[1:0] = 01B)	TxD0 (SCSI00[1:0] = 01B)
															RxD0 (SCSI00[1:0] = 10B)	TxD0 (SCSI00[1:0] = 10B)
															RxD0 (SCSI00[1:0] = 11B)	TxD0 (SCSI00[1:0] = 11B)

Notes 1. The SE0 register is a read-only status register which is set using the SS0 and ST0 registers.

2. This pin can be set as a port function pin or other alternate function pin.

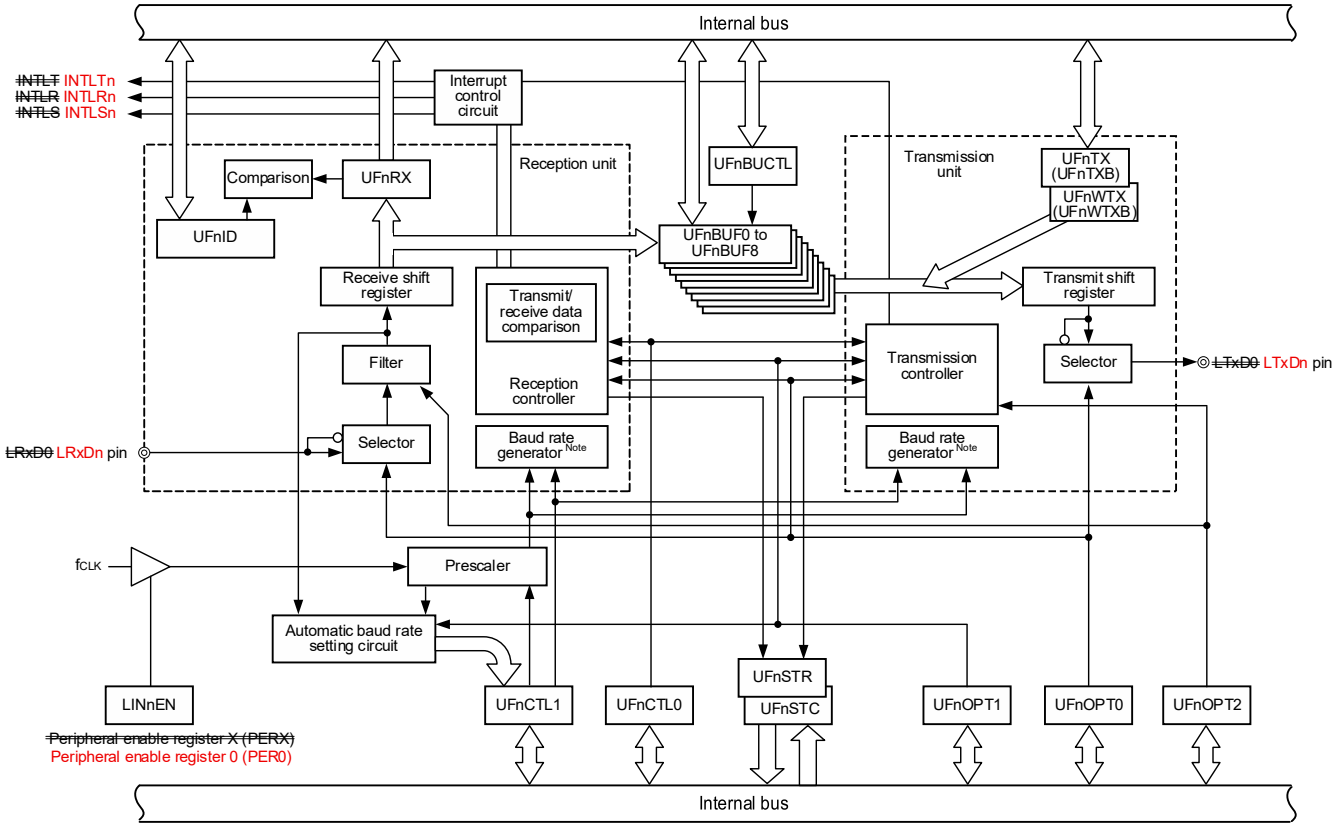
3. This is 0 or 1, depending on the communication operation. For details, refer to **12.3 (12) Serial output register m (SOm)**.

Caution The shaded pins are provided at some ports. Select either port by using the corresponding register.

No.74: Correct the “Figure 13-1”

Changes are shown in red characters.

Figure 13-1. Block Diagram of Asynchronous Serial Interface LIN-UART



No.75: Correct the typo in after reset value of UFnOPT0 register

Changes are shown in red characters.

13.3 Control Registers

(4) LIN-UARTn option register 0 (UFnOPT0)

The UFnOPT0 register is an 8-bit register that controls serial communication operation of LIN-UARTn.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to ~~13H~~ 14H.

No.76: Correct a description of UFnRX register”

Changes are shown in red characters.

13.3 Control Registers

(13) LIN-UARTn receive data register (UFnRX)

The UFnRX register is a 16-bit register that is used to store receive data.

Receive data of a character length specified by the UFnCL bit after reception completion will be stored into the UFnRX register when not in automatic baud rate mode (UFnMD1, UFnMD0 = 00B/10B) and when UFnEBE is “0”. When UFnEBE = UFnCL = 1, receive data of 9-bit length will be stored.

This register is read-only, in 16-bit units. When the UFnRX register is read in 8-bit units, it can be accessed as the ~~UFnRX~~ UFnRXB register.

Reset input sets this register to 0000H.

No.77: Update the “Figures 13-30, 13-31”

Changes are shown in red characters.

Figure 13-30. Port Configuration of LIN Reception Manipulation

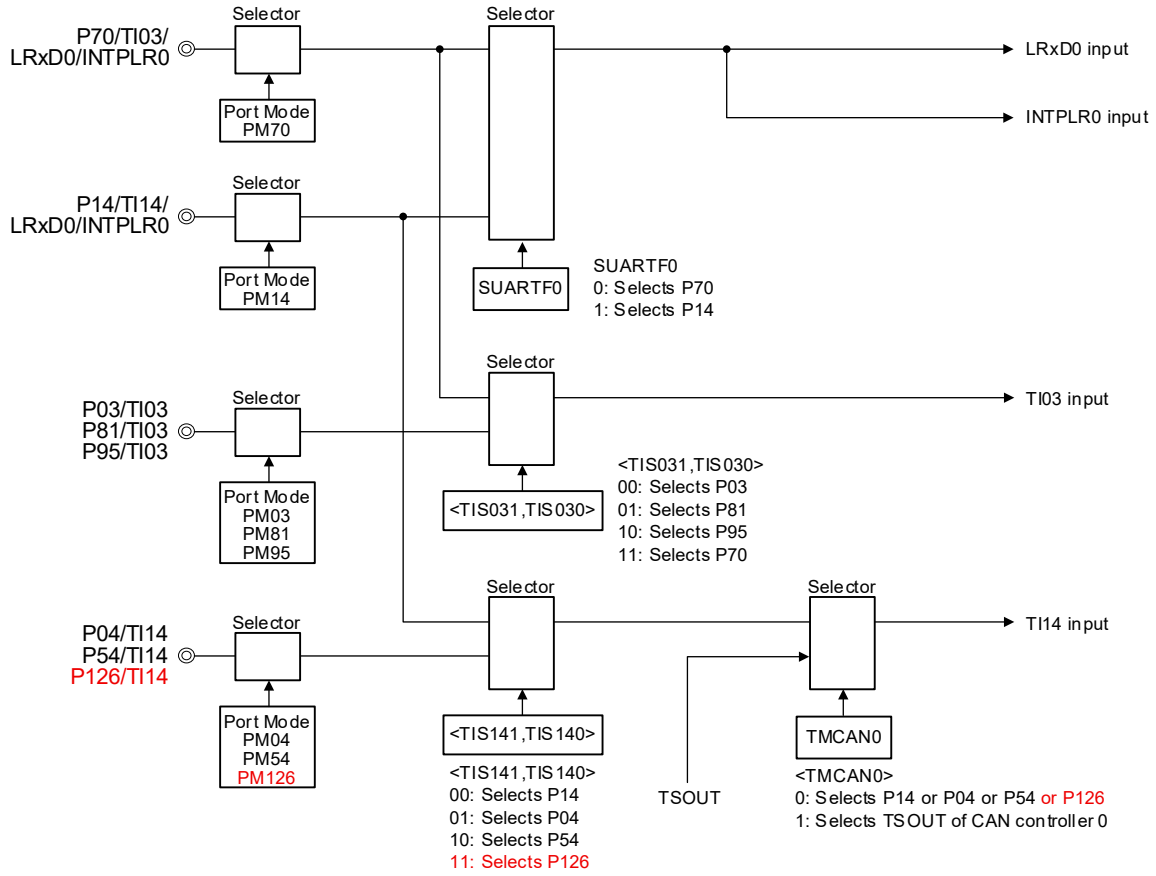
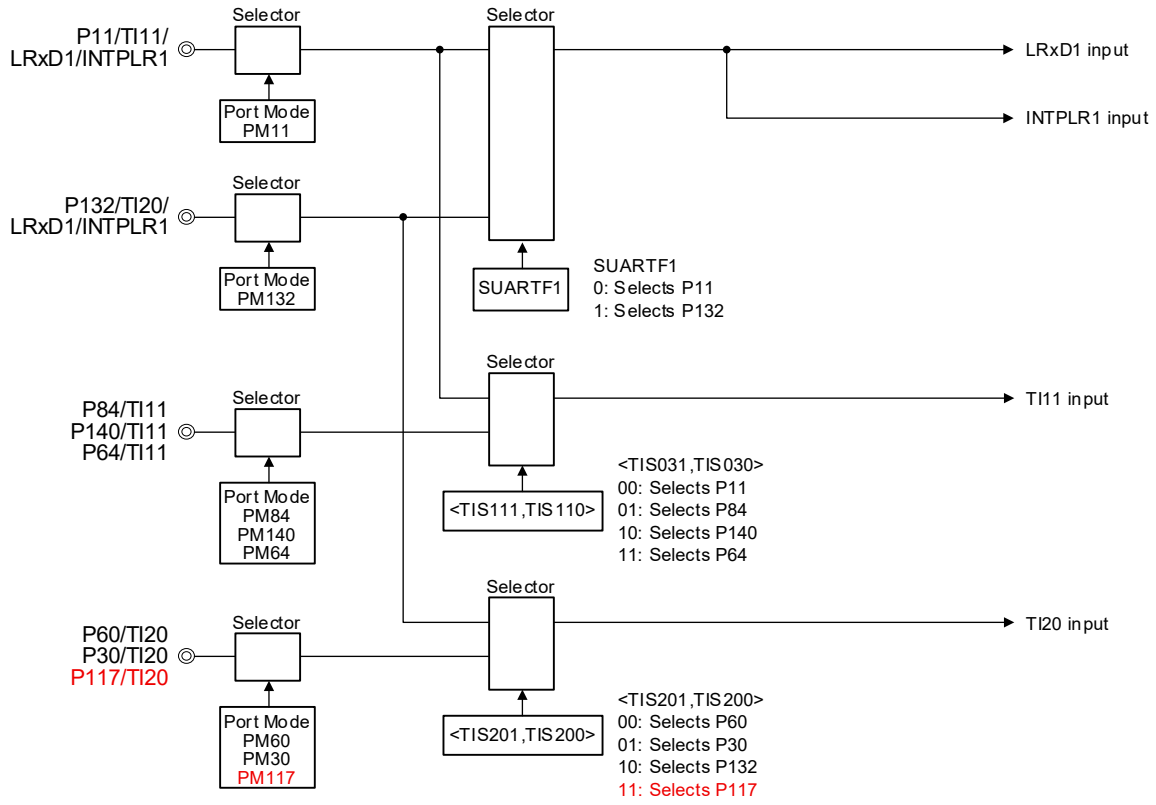


Figure 13-31. Port Configuration of LIN Reception Manipulation



No.78: Correct the typo in the UFnRRQ bit name at the bottom of Figure 13-49

Changes are shown in red characters.

Figure 13-49. UART Buffer Mode Transmission Processing Flow

Caution 2. ~~UFnPRQ~~ UFnRRQ must not be set to 1 before completion of receive data reading.

No.79: Correct the “Figures 13-70, 13-71”

Changes are shown in red lines.

Figure 13-70. Noise Filter Circuit Example

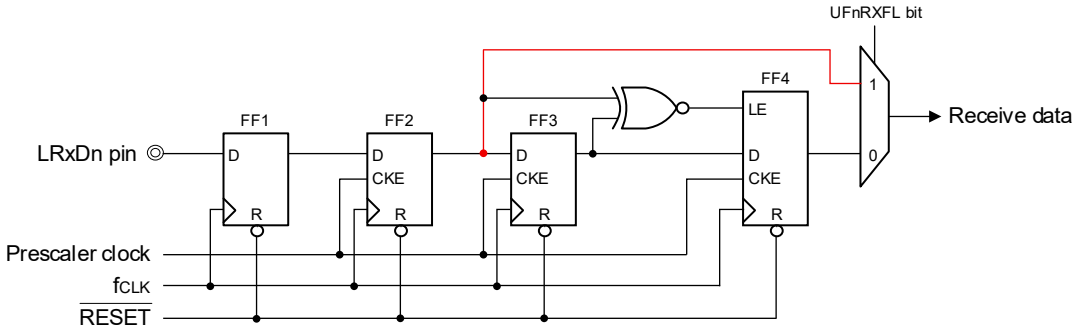
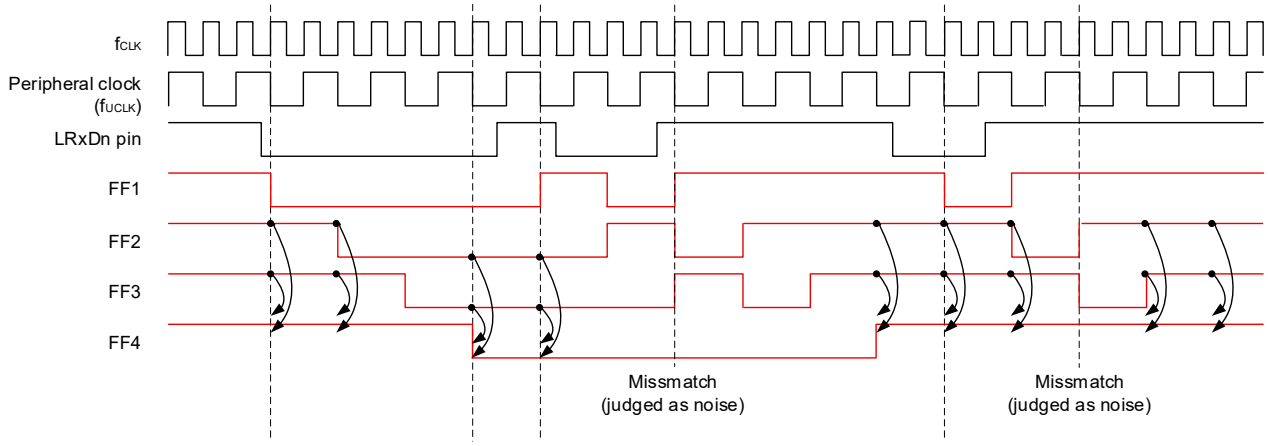


Figure 13-71. Noise Filter Timing Chart Example (UFnPRS = 1)



No.80: Correct the typo of the PER0 register name in “Chapter 13.11”

Changes are shown in red characters.

13.11 Cautions for Use

(3) Stop the LIN-UARTn in the following sequence.

<1> Set UFnCTL0.UFnTXE to 0, and UFnCTL0.UFnRXE to 0.

<2> Set ~~PER1.LINnEN~~ PER0.LINnEN to 0.

<3> Set the ports. (It is not a problem if port setting is not changed.)

No.81: Correct the typo of the product name in “Chapter 14”

Changes are shown in red characters.

CHAPTER 14 CAN CONTROLLER

	R5F10CGx	R5F10DGx	R5F10CLx	R5F10DLx	R5F10CMx	R5F10DMx	R5F10TPJ/ R5F10DPE/F/G	R5F10DPJ/K/L ~~E5F10DSx~~ R5F10DSx
aFCAN	0 channel	1 channel	0 channel	1 channel	0 channel	1 channel	1 channel	2 channels

No.82: Correct a typo in the C0MDB502 register address in “Table 14-16”

Changes are shown in red characters.

Table 14-16. Register Access Types (3/18)

Address	Register Name	Symbol	R/W	Bit Manipulation Units			Default Value
				1	8	16	
F0624H	CAN0 message data byte 45 register 02	C0MDB4502	R/W	–	–	√	Undefined
F0624H	CAN0 message data byte 4 register 02	C0MDB402		–	√	–	Undefined
~~000F625H~~ F0625H	CAN0 message data byte 5 register 02	C0MDB502		–	√	–	Undefined

No.83: Correct the typo in the bit diagram in “Figure 14-25”

Add bit access definitions (“<n>”). Changes are shown in red characters.

Figure 14-25. Format of Peripheral Clock Select Register (PCKSEL)

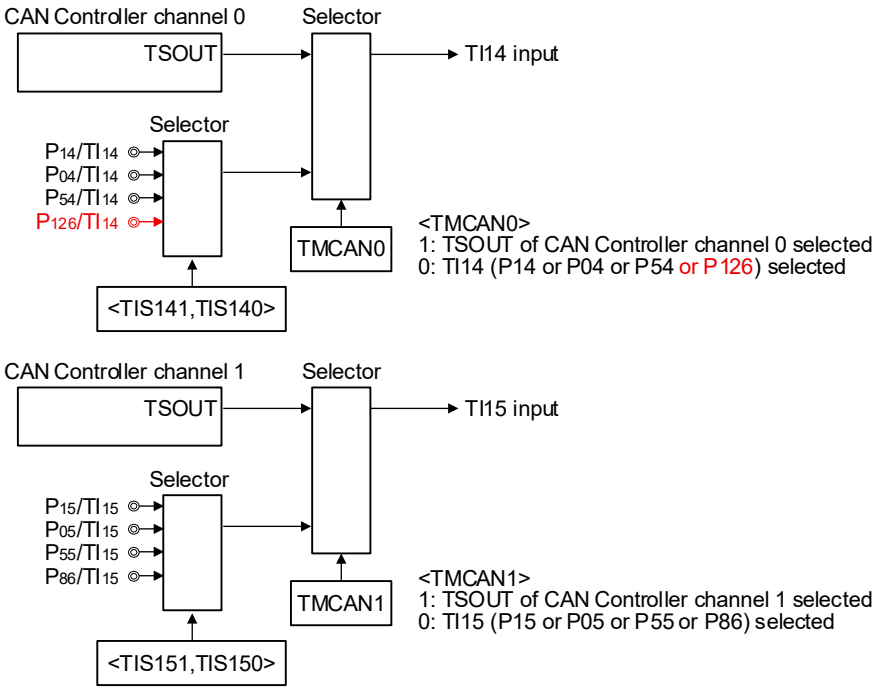
Address: F00F2H After reset: 00H R/W

Symbol	7	~~6~~ <6>	~~5~~ <5>	~~4~~ <4>	~~3~~ <3>	2	1	~~0~~ <0>
PCKSEL	0	CAN MCKE1	CAN MCK1	CAN MCKE0	CAN MCK0	0	0	SGCLK SEL

No.84: Update the “Figure 14-62”

Changes are shown in red characters.

Figure 14-62. Switching source of input



No.85: Correct the bit diagram of the PER1 register in “Figure 15-8”

Changes are shown in red characters.

Figure 15-8. Format of Peripheral Enable Registers 1 (PER1)

Address: F00F1H After reset: 00H R/W (Note: Bits 0 to 3 and 6 are Read Only)

Symbol	~~7~~ <7>	6	~~5~~ <5>	~~4~~ <4>	~~3~~ <3>	2	1	0
PER1	ADCEN	0	MTRCEN	SGEN	~~0~~ LBEN	0	0	0

No.86: Correct a typo of the pixel number for R5F10DSx product in “Table 16-1”

Changes are shown in red characters.

Table 16-1. Maximum Number of Pixels

(e) R5F10DSx

LCD Driver Voltage Generator	Bias Mode	Number of Time Slices	Common Signals Used	Number of Segments	Maximum Number of Pixels
• Internal resistance division	–	Static	COM0 (COM1 to COM3)	54	54 (54 segment signals, 1 common signal)Note 1
	1/3	3	COM0 to COM2		162 (54 segment signals, 3 common signals)Note 2
		4	COM0 to COM3		~~212~~ 216 (54 segment signals, 4 common signals)Note 3

Notes 1. 6-digit LCD panel, each digit having an 8-segment 8. configuration.
2. 17-digit LCD panel, each digit having a 3-segment 8. configuration.
3. 26-digit LCD panel, each digit having a 2-segment 8. configuration.

No.87: Update a description of the LCDPFn register in “Chapter 16.3”

Add the description of LCDPF10, LCDPF11, LCDPF12 registers. Changes are shown in red characters.

16.3 Registers Controlling LCD Controller/Driver

(7) LCD port function register 4 (LCDPF4)

This register sets whether to use pins P42 to P47 of 128-pin products as port pins (other than segment output pins) or segment output pins.

~~LCDPF3~~ LCDPF4 is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets ~~LCDPF3~~ LCDPF4 to 00H.

Figure 16-8. Format of LCD Port Function ~~Register 3~~ Register 4

Address: F0054H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
LCDPF4	LCDPF47	LCDPF46	LCDPF45	LCDPF44	LCDPF43	~~LCDPF2~~ LCDPF42	0	0

(13) LCD port function register 10, 11, 12 (LCDPF10, LCDPF11, LCDPF12) (128-pin only)

These registers set whether to use pins P10n, P11n, and P125 to P127 as port pins (other than segment output pins) or segment output pins.

LCDPF10, 11, 12 are set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets LCDPF10, 11, 12 to 00H.

Figure 16-14. Format of LCD Port Function Register 10, 11, 12

Address: F005AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
LCDPF10	LCDPF107	LCDPF106	LCDPF105	LCDPF104	LCDPF103	LCDPF102	LCDPF101	LCDPF100

Address: F005BH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
LCDPF11	LCDPF117	LCDPF116	LCDPF115	LCDPF114	LCDPF113	LCDPF112	LCDPF111	LCDPF110

Address: F005CH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
LCDPF12	LCDPF127	LCDPF126	LCDPF125	0	0	0	0	0

LCDPFmn	Port/segment output specification
0	Used as port or alternate function other than segment output
1	Used as segment output

Remark m = 10, 11, 12, n = 0 to 7

No.88: Correct a description of memory address in “Chapter 16.5”

Changes are shown in red characters. (The reference figure number will be revised due to the addition of Figure 16-14.)

16.5 LCD Display Data Memory

The LCD display data memory is mapped at the following addresses:

~~F0300H to F0334H for R5F10TPx, R5F10DPx, and R5F10DSx~~

F0300H to F0335H for R5F10DSx

F0300H to F0334H for R5F10TPx and R5F10DPx

F0300H to F032FH for R5F10CMx and R5F10DMx

F0300H to F032CH for R5F10CLx, R5F10DLx, R5F10CGx and R5F10DGx

Figure 16-15. Relationship between LCD Display Data Memory Contents and Segment/Common Outputs (2/3)

(e) R5F10DSx

	b7	b6	b5	b4	b3	b2	b1	b0	
~~F0334H~~ F0335H	0	0	0	0					SEG53
~~F0333H~~ F0334H	0	0	0	0					SEG52
~~F0332H~~ F0333H	0	0	0	0					SEG51
⋮									
F0305H	0	0	0	0					SEG5
F0304H	0	0	0	0					SEG4
F0303H	0	0	0	0					SEG3
F0302H	0	0	0	0					SEG2
F0301H	0	0	0	0					SEG1
F0300H	0	0	0	0					SEG0
					COM3	COM2	COM1	COM0	

Note ~~R5F10TPx/R5F10DPx has 53 segment signals (SEG0 to SEG52)~~

R5F10DSx has 54 segment signals (SEG0 to SEG53).

No.89: Correct a typo in the table in “Figure 16-27”

Changes are shown in red characters.

Figure 16-27. LCD Drive Power Block Diagram

mode		LCDR0	LCDR1	LCDR2	LCDR3	LCDR4
Static or or 1/3 bias mode	no step-down transforming	~~R~~ 0	R	R	R	0**
	step-down transforming	2R	R	R	R*	0**

No.90: Correct a typo of LBCYC, LBWST registers in “Chapter 17.3”

Changes are shown in red characters.

17.3 Registers Controlling LCD Bus Interface

(3) ~~LCB~~ LCD Bus Interface cycle control register (LBCYC)

LBCYC register determines the cycle time of the LCD Bus Interface.

The cycle time is the duration of one bus access for transferring one 8-bit data.

LBCYC is set using ~~a 1-bit or 8-bit~~ an 8-bit memory manipulation instruction.

Reset signal generation sets LBCYC to ~~00H~~ 02H.

Figure 17-6. Format of ~~LCB~~ LCD Bus Interface cycle control register (LBCYC)

(4) ~~LCB~~ LCD Bus Interface wait control register (LBWST)

LBWST determines the number of wait states of the LCD Bus Interface. The number of wait states defines the duration of the $\overline{\text{DBWR}}$ and $\overline{\text{DBRD}}$ signals. This duration must remain below the cycle time.

LBWST is set using ~~a 1-bit or 8-bit~~ an 8-bit memory manipulation instruction.

Reset signal generation sets LBWST to 00H.

Figure 17-7. Format of ~~LCB~~ LCD Bus Interface wait control register (LBWST)

No.91: Correct the bit diagram of the PER1 register in “Chapter 18.2”

Changes are shown in red characters.

18.2 Sound Generator Registers

(1) Peripheral enable register (PER1) and peripheral clock select register (PCKSEL)

Peripheral enable register (PER1)

Address: F00F1H After reset: 00H R/W

Symbol	~~7~~ <7>	6	~~5~~ <5>	~~4~~ <4>	~~3~~ <3>	2	1	0
PER1	ADCEN	0	MTRCEN	SGEN	~~0~~ LBEN	0	0	0

No.92: Correct the description of interrupt related registers in “Chapter 20.6”

Changes are shown in red characters.

20.6 Cautions on Using DMA Controller

(4) DMA pending instruction

- Write instructions for registers IF0L, IF0H, IF1L, IF1H, IF2L, IF2H, IF3L, IF3H, MK0L, MK0H, MK1L, MK1H, MK2L,MK2H, MK3L, MK3H, PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR03L, PR03H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H, PR13L and PR13H each.

No.93: Correct a typo of the product information in “Chapter 21”

Changes are shown in red characters.

CHAPTER 21 INTERRUPT FUNCTIONS

		R5F10CGx	R5F10DGx	R5F10CLx	R5F10DLx	R5F10CMx	~~R5F10CMx~~ R5F10DMx	R5F10TPx ~~R5F10DPx~~ R5F10DP [E/F/G]	~~R5F10DPJ~~ R5F10DP [J/K/L]	R5F10DSx
Maskable interrupts	External	6		8						
	Internal	39	43	~~53~~ 42	~~26~~ 46	42	~~26~~ 46	49	53	53

No.94: Correct a typo in the product name in “Table 21-1”

Changes are shown in red characters.

Table 21-1. Interrupt Source List

Type	Default priority Note1	Interrupt Source		Internal/ External	Vector table address	Basic Configuration type	R5F10CGx	R5F10DGx	R5F10CLx	R5F10DLx	R5F10CMx	R5F10DMx	~~R5F10DPx, R5F10TPJ~~ R5F10TPJ/R5F10DP[E/F/G]	~~R5F10DPJ~~ R5F10DP[J/K/L]	R5F10DSx
		Name	Trigger												

Changes are shown in red characters.

No.95: Add the SRPR00 and STPR00 flags in “Figure 21-4”

Figure 21-4. Format of Priority Specification Flag Registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR03L, PR03H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H, PR13L, PR13H) (R5F10DSx) (1/3)

Address: FFFE9H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR00H	LTPR00	ITPR0	RTCPR0	DMAPR01	DMAPR00	CSIPR001 SRPR00	CSIPR000 STPR00	CLMPR0

No.96: Correct figure and table reference numbers in “Chapter 21”

Changes are shown in red characters.

Figure 21-4. Format of Priority Specification Flag Registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR03L, PR03H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H, PR13L, PR13H) (R5F10DSx) (3/3)

Caution The above is the bit layout for the R5F10DSx. The available bits differ depending on the product. For details about the bits available for each product, see ~~Table 20-1 and 20-2~~ Table 21-1 and 21-2. Be sure to set bits that are not available to 1.

Figure 21-5. Format of External Interrupt Rising Edge Enable Register 0 (EGP0) and External Interrupt Falling Edge Enable Register 0 (EGN0)

~~Table 20-3~~ Table 21-3 shows the ports corresponding to the EGPn and EGNn bits.

21.4.1 Maskable interrupt request acknowledgement

The times from generation of a maskable interrupt request until vectored interrupt servicing is performed are listed in ~~Table 20-4~~ Table 21-4 below.

~~Figure 20-7~~ Figure 21-7 shows the interrupt request acknowledgment algorithm.

21.4.3 Multiple interrupt servicing

~~Table 20-5~~ Table 21-5 shows relationship between interrupt requests enabled for multiple interrupt servicing and ~~Figure 20-10~~ Figure 21-10 shows multiple interrupt servicing examples.

21.4.4 Interrupt request hold

~~Figure 20-11~~ Figure 21-11 shows the timing at which interrupt requests are held pending.

No.97: Correct the description of interrupt related registers in “Table 21-5 and Chapter 21.4.4”

Changes are shown in red characters.

Table 21-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing

Remark 4. PR is a flag contained in the PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR03L, PR03H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H, PR13L and PR13H registers.

PR = 00: Specify level 0 with ××PR1× = 0, ××PR0× = 0 (higher priority level)

PR = 01: Specify level 1 with ××PR1× = 0, ××PR0× = 1

PR = 10: Specify level 2 with ××PR1× = 1, ××PR0× = 0

PR = 11: Specify level 3 with ××PR1× = 1, ××PR0× = 1 (lower priority level)

21.4.4 Interrupt request hold

- Write instructions for the IF0L, IF0H, IF1L, IF1H, IF2L, IF2H, IF3L, IF3H, MK0L, MK0H, MK1L, MK1H, MK2L, MK2H, MK3L, MK3H, PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR03L, PR03H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H, PR13L and PR13H registers

No.98: Correct the table reference numbers in “Chapter 23”

Changes are shown in red characters.

CHAPTER 23 RESET FUNCTION

A reset is effected when a low level is input to the $\overline{\text{RESET}}$ pin, the watchdog timer overflows, or by POR and LVD circuit voltage detection, execution of illegal instruction[Note], RAM parity error, detection of main clock oscillation stop via clock monitoring, or illegal-memory access, and each item of hardware is set to the status shown in ~~Table 22-1~~ Table 23-1.

No.99: Add the target registers to Table 23-2

Changes are shown in red characters.

Table 23-2. Hardware Statuses After Reset Acknowledgment (1/7)

Hardware		After Reset Acknowledgment[Note 1]
Port registers (~~P0 to P9, P13 to P15~~ P0 to P15) (output latches)		00H
Port mode registers ~~0 to 9, 13 to 15 (PM0 to PM9, PM13 to PM15)~~ 0 to 15 (PM0 to PM15)		FFH [Note3]
Port input mode registers 0, 1, 3, 5 to 7, 11, 13 (PIM0, PIM1, PIM3, PIM5 to PIM7, PIM11, PIM13)		00H
~~Pull-up resistor option registers 0, 1, 3 to 9, 13, 14 (PU0, PU1, PU3 to PU9, PU13, PU14)~~ Pull-up resistor option registers 0, 1, 3 to 14 (PU0, PU1, PU3 to PU14)		00H (PU4 is 01H)
RESET output control register (RESOC)		00H
Processor mode control register (PMC)		00H
Operation speed mode control register (OSMC)		00H
Timer array unit	Timer status registers 00 to 07, 10 to 17, 20 to 27 (TSR00 to TSR07, TSR10 to TSR17, TSR20 to TSR27)	0000H
	Timer channel enable status register 0, 1, 2 (TE0, TE1, TE2)	0000H
	Timer channel start register 0, 1, 2 (TS0, TS1, TS2)	0000H
	Timer channel stop register 0, 1, 2 (TT0, TT1, TT2)	0000H
	Timer output register 0, 1, 2 (TO0, TO1, TO2)	0000H
	Timer output enable register 0, 1, 2 (TOE0, TOE1, TOE2)	0000H
	Timer output level register 0, 1, 2 (TOL0, TOL1, TOL2)	0000H

Notes 3. Value after reset is FEH only for ~~PM3~~ PM13.

Table 23-2. Hardware Statuses After Reset Acknowledgment (2/7)

Hardware		Status After Reset Acknowledgment[Note 1]
Timer array unit	~~Noise filter enable register for each channel of TAU unit0 to 2 BCD correction result register (TNFEN0BCDADJ to TNFEN2)~~ Noise filter enable register for each channel of TAU unit0 to 2 (TNFEN0 to TNFEN2)	00H

Table 23-2. Hardware Statuses After Reset Acknowledgment (3/7)

Hardware		Status After Reset Acknowledgment[Note 1]
Serial array unit (SAU)	Noise filter enable register for SAU (SNFEN0)	00H
DMA controller	DMA RAM address registers 0 to 3 (DRA0 to DRA3)	~~00H~~ 0000H
	DMA byte count registers 0 to 3 (DBC0 to DBC3)	~~00H~~ 0000H
	DMA trigger selection register (DMATSEL)	00H
	DMA all-channel forced wait register (DWAITALL)	00H

Table 23-2. Hardware Statuses After Reset Acknowledgment (4/7)

Hardware		Status After Reset Acknowledgment[Note 1]
UART	LIN-UART0 option control registers 0, to 2 (UF0OPT0 to UF0OPT2)	14H, 00H, 00H
	LIN-UART1 option control registers 0 to 2 (UF1OPT0 to UF1OPT2)	14H, 00H, 00H
	LIN-UART1 status clear register (UF1STC)	0000H

Table 23-2. Hardware Statuses After Reset Acknowledgment (6/7)

Hardware		Status After Reset Acknowledgment[Note 1]
LCD controller	LCD display data memory ~~0 to 52 (SEG0 to SEG52)~~ 0 to 53 (SEG0 to SEG53)	00H
	~~LCD port function registers 0, 1, 3, 5, 7 to 9, 13 (LCDPF0, LCDPF1, LCDPF3, LCDPF5, LCDPF7 to LCDPF9, LCDPF13)~~ LCD port function registers 0, 1, 3 to 5, 7 to 13 (LCDPF0, LCDPF1, LCDPF3 to LCDPF5, LCDPF7 to LCDPF13)	00H
LCD bus interface	LCD bus interface mode register (LBCTL)	00H
	LCD bus interface cycle control register (LBCYC)	02H
	LCD bus interface wait control register (LBWST)	00H
	LCD bus interface data register (LBDATA)	0000H
	LCD bus interface read data register (LBDATAR)	0000H

Table 23-2. Hardware Statuses After Reset Acknowledgment (7/7)

Hardware		Status After Reset Acknowledgment[Note 1]
Multiplier & divider, multiply-accumulator	Multiplication/division data register A (MDAL/MULA, MDAH/MULB)	0000H
	Multiplication/division data register B (MDBL/MULOL, MDBH/MULOH)	0000H

No.100: Add a description of RESOC register to Chapter 23

23.4 RESET Output Control Register

Output only port (P130) is added RESET output function. The RESET signal is not output directory from P130, it is controlled it by software. RESO bit and P130 bit together control the output of P130/RESOUT.

This register is only 128-pin products.

Figure 23-8. Format of RESET Output Control Register (RESOC)

Address: F0014H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
RESOC	0	0	0	0	0	0	0	RESO

RESO	P130/RESOUT output control [Note]
0	“Low” level output
1	“High” level output

Note RESO can only be written “1” after reset, “0” cannot be written by software. It can be cleared to “0” by all reset sources.

P130	RESO	P130/RESOUT pin output
0	0	“Low” level output
1	0	“High” level output
0	1	
1	1	

No.101: Delete the description of IEC61508 in “Chapter 26”

26.1 Overview of Safety Functions

The RL78/D1A is provided with the following safety functions to meet the IEC 60730 ~~and IEC 61508~~ safety standards. The functions are intended to detect failures through microcomputer’s self-diagnosis and to stop the system safely.

26.3.2 CRC Operation Function (General-Purpose CRC)

~~The IEC 61508 standard requires safety to be guaranteed during operation and thus the means for data verification during CPU operation is necessary.~~

With the general-purpose CRC operation function, the CRC operation is possible as a peripheral function during CPU operation. The general-purpose CRC operation function can be used for not only check of code flash memory area but versatile check. Data to be checked is specified with the user program. In HALT mode, the CRC operation function is available only during DMA transfer.

26.3.4 RAM Guard Function

~~The IEC 61508 standard requires safety to be guaranteed during operation and thus it is necessary to protect significant data stored in RAM when the CPU freezes.~~

The RAM guard function protects data in the specified space.

Setting this function disables writing to RAM in the specified space but enables reading normally.

26.3.5 SFR Guard Function

~~The IEC 61508 standard requires safety to be guaranteed during operation and thus it is necessary to prevent significant SFRs from being erroneously rewritten when the CPU freezes.~~

The SFR guard function protects data in the registers used to control the port function, interrupt function, clock control function, voltage detection circuits, and RAM parity error detection function.

Setting this function disables writing to guarded SFRs but enables reading normally.

No.102: Correct a typo of register name in “Chapter 26.2”

Changes are shown in red characters.

26.2 Registers Used by Safety Functions

Register Name	Safety Functions
• Flash memory CRC control register (CRC0CTL) • Flash memory CRC operation result register (PGCRCL)	Flash memory CRC operation function (high-speed CRC)
• CRC input register (CRCIN) • CRC data register (CRCD)	CRC operation function (general-purpose CRC)
• RAM parity error control register (RPECTL)	RAM parity error detection function
• Invalid memory access detection control register (IAWCTL)	RAM guard function SFR guard function Invalid memory access detection function
• ~~Timer input select register 0 (TIS0)~~ • Timer input select else register (TISELSE)	Frequency detection function
• A/D test register (ADTES)	A/D test function
• Analog input channel specification register (ADS)	Specification of the analog voltage input channel

26.3.7.1 ~~Timer input select register 0~~ Timer input select else register (TISELSE)

This register is used to select the timer input of channel 5.

By selecting the internal low-speed oscillation clock for the timer input, its pulse width can be measured to determine whether the proportional relationship between the internal low-speed oscillation clock and the timer operation clock is correct.

The TISELSE register can be set by ~~an 8-bit~~ a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

No.103: Correct the typo in the access size of GUARD register in “Chapter 26.3.5.2”

Changes are shown in red characters.

26.3.5.2 Specific register manipulation protect register (GUARD)

This register is used to control the guard function.

GDRTC and GDPLL bits are used in SFR guard function.

The GUARD register can be set by ~~an 8-bit~~ a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

No.104: Correct a typo in the memory size in “Chapter 29.4.1”

Changes are shown in red characters.

29.4.1 Data flash overview

In addition to ~~24 to 256 KB~~ 24 to 512 KB of code flash memory, the RL78/D1A includes 8 KB of data flash memory for storing data.

No.105: Correct the description of data flash accessing in “Chapter 29.4.3”

[TU: TN-RL*-A0096A/E]

Changes are shown in red characters.

29.4.3 Procedure for accessing data flash memory

The data flash memory is initially stopped after a reset ends and cannot be accessed (read or programmed). To access the memory, perform the following procedure:

<1> Write 1 to bit 0 (DFLEN) of the data flash control register (DFLCTL).

<2> Wait for the setup to finish.

The time setup takes differs for each main clock mode.

<Setup time for each main clock mode>

- HS (high-speed main) mode: 5 μs
- LS (low-speed main) mode: ~~720 ns~~ 1 μs

<3> After the wait, the data flash memory can be accessed.

Cautions 4. The data flash should be read in either of following ways.

• Use the flash library provided by Renesas (EEL (Pack01) version V1.13 or later).

• Stop the DMA transfer before reading.

5. If accessing data flash memory when the f_{SUB} (subsystem clock) is selected as f_{CLK} (CPU/peripheral hardware clock), take one of the following procedures.:

i) To switch f_{CLK} from f_{SUB} to the main system clock, follow these steps (1) to (3).

(1) Confirming the complete switching to main system clock (CLS* = 0).

(2) Read any data flash memory address as a dummy read (don't use the read value).

(3) Waiting until the following time has passed:

HS (high-speed main) mode: 5 μs

LS (low-speed main) mode: 1 μs

***: Bit of the system clock control register (CKC)**

ii) Do not read data flash memory when f_{SUB} is selected as f_{CLK}.

If data flash content needs to be accessed during f_{SUB} is selected as f_{CLK}, store the required data flash content to RAM before setting f_{SUB} to f_{CLK}. And read copied content from RAM.

No.106: Correct a typo in the memory address in “Figure 30-2”

Changes are shown in red characters.

Figure 30-2. Memory Spaces Where Debug Monitor Programs Are Allocated

Notes 1. Address differs depending on products as follows.

Products (code flash memory capacity)	Address of **Note 1**
R5F10CGB	~~05C00H to 05FFFH~~ 05FFFH
R5F10CGC, R5F10DGC	~~07C00H to 07FFFH~~ 07FFFH
R5F10CxD, R5F10DxD (x = G, L, M)	~~0BC00H to 0BFFFH~~ 0BFFFH
R5F10CME, R5F10DxE (x = G, L, M, P)	~~0FC00H to 0FFFFH~~ 0FFFFH
R5F10DxF (x = M, P)	~~17C00H to 17FFFH~~ 17FFFH
R5F10DxG (x = M, P)	~~1FC00H to 1FFFFH~~ 1FFFFH
R5F10DxJ, R5F10TPJ (x = ~~M, P~~ M, P, S)	~~3FC00H to 3FFFFH~~ 3FFFFH
R5F10DPK, R5F10DSK	~~5FC00H to 5FFFFH~~ 5FFFFH
R5F10DPL, ~~R5F10DSx (x = L, K, J)~~ R5F10DSL	~~7FC00H to 7FFFFH~~ 7FFFFH

No.107: Update the product group table in “Chapters 33, 34”

Changes are shown in red characters.

[Chapter 33]

Definition of Product Groups

Definition of product groups described in this chapter is shown in the following table.

Product groups	Product names				
	48-pin products	64-pin products	80-pin products	100-pin products	128-pin products
Product Group A	R5F10CGBCJFB R5F10CGCCJFB R5F10CGDCJFB R5F10DGCCJFB R5F10DGDCJFB R5F10DGECJFB R5F10CGBJFB R5F10CGCJFB R5F10CGDJFB R5F10DGCJFB R5F10DGDJFB R5F10DGEJFB	R5F10CLDCJFB R5F10DLDCJFB R5F10DLECJFB R5F10CLDJFB R5F10DLDJFB R5F10DLEJFB	R5F10CMDCJFB R5F10CMECJFB R5F10DMDCJFB R5F10DMECJFB R5F10DMFCJFB R5F10DMGCJFB R5F10DMJCJFB R5F10CMDJFB R5F10CMEJFB R5F10DMDJFB R5F10DMEJFB R5F10DMFJFB R5F10DMGJFB R5F10DMJJFB	R5F10DPECJFB R5F10DPFCJFB R5F10DPGCJFB R5F10DPJCJFB R5F10TPJCJFB R5F10DPEJFB R5F10DPFJFB R5F10DPGJFB R5F10DPJJFB R5F10TPJJFB	-
Product Group B	-	-	-	R5F10DPKJFB R5F10DPLJFB	R5F10DSJJFB R5F10DSKJFB R5F10DSLJFB

[Chapter 34]

Definition of Product Groups

Definition of product groups described in this chapter is shown in the following table.

Product groups	Product names				
	48-pin products	64-pin products	80-pin products	100-pin products	128-pin products
Product Group A	R5F10CGBCLFB R5F10CGCCLFB R5F10CGDCLFB R5F10DGCCLFB R5F10DGDCLFB R5F10DGECLFB R5F10CGBLFB R5F10CGCLFB R5F10CGDLFB R5F10DGCLFB R5F10DGDLFB R5F10DGELFB	R5F10CLDCLFB R5F10DLDCLFB R5F10DLECLFB R5F10CLDLFB R5F10DLDLFB R5F10DLELFB	R5F10CMDCLFB R5F10CMECLFB R5F10DMDCLFB R5F10DMECLFB R5F10DMFCLFB R5F10DMGCLFB R5F10DMJCLFB R5F10CMDLFB R5F10CMELFB R5F10DMDLFB R5F10DMELFB R5F10DMFLFB R5F10DMGLFB R5F10DMJLFB	R5F10DPECLFB R5F10DPFCLFB R5F10DPGCLFB R5F10DPJCLFB R5F10TPJCLFB R5F10DPELFB R5F10DPFLFB R5F10DPGLFB R5F10DPJLFB R5F10TPJLFB	-
Product Group B	-	-	-	R5F10DPKLFB R5F10DPLLFB	R5F10DSJLFB R5F10DSKLFB R5F10DSLLFB

No.108: Change the chapter number in "LCD Bus Interface Characteristics"

Changes are shown in red characters.

[Chapter 33]

~~**33.6 LCD Bus Interface Characteristics (128-pin products only)**~~

33.5.9 LCD Bus Interface Characteristics (128-pin products only)

[Chapter 34]

~~**34.6 LCD Bus Interface Characteristics (128-pin products only)**~~

34.5.9 LCD Bus Interface Characteristics (128-pin products only)

No.109: Correct the “A/D converter characteristics”

Changes are shown in red characters.

[Chapters 33, 34]

33.7.1 A/D converter characteristics

34.7.1 A/D converter characteristics

Items	Symbols	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	Bit
Overall error Note 1,2	AINL	10 bit Resolution $AV_{REFP} = V_{DD}$ Note 3 $AV_{REFM} = 0$ V		~~1.2~~ ±1.2	±3.5	LSB

No.110: Correct the typo of $I_{OLTOTAL}$ for Group 3E products

Changes are shown in red characters.

T_A = -40 to +105 °C, 4.0 V ≤ V_{DD} = SMV_{DD0} = SMV_{DD1} ≤ 5.5 V, V_{SS} = SMV_{SS0} = SMV_{SS1} = 0 V (2/3)

Parameter	Symbols	Conditions			Min.	Typ.	Max.	Unit
Output current, low	$I_{OLTOTAL}$	Total (for duty factors ≤ 70%Note)	Group 3E (64-pin, 48-pin)	T_A = -40 °C			~~148~~ 148	mA
				T_A = +25 °C			~~118~~ 118	mA
				T_A = +85 °C			~~96~~ 96	mA
				T_A = +105 °C			96	mA

No.111: Correct a typo of the condition in “Chapter 34.5.2”

Changes are shown in red characters.

34.5.2 Stepper motor controller/driver

T_A = -40 to +105 °C,

2.7 V ≤ = SMV_{DD0} = SMV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = SMV_{SS0} = SMV_{SS1} = 0 V

Items	Symbols	Conditions		MIN.	TYP.	MAX.	Unit
PWM output rise time	t_R	10%-90% Note 2	4.0 V ≤ SMV_{DD} ≤ 5.5 V	15	60	100	ns
			2.7 V ≤ SMV_{DD} ≤ 4.0 V	20		500	ns
PWM output fall time	t_F	10%-90% Note 2	~~4.0 V ≤ SMV_{DD} 5.5 V~~ 4.0 V ≤ SMV_{DD} ≤ 5.5 V	15	60	100	ns
			2.7 V ≤ SMV_{DD} ≤ 4.0 V	20		500	ns

No.112: Correct the max. value of the LVD detection delay time in “Chapter 34.7.4”

Changes are shown in red characters.

34.7.4 LVD characteristics

T_A = -40 to +105 °C, $V_{PDR} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5$ V, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V

Items	Symbols	Conditions	MIN.	TYP.	MAX.	Unit
Detection Delay time	T_{LD}				~~200~~ 300	μs
Minimum pulse width	T_{LW}	Necessary width of V_{DD} drop down below selected V_{LVIx} (x = 0, 3 to 5)	300			μs

No.113: Update the Table of registers access wait cycles in “APPENDIX.A”

Changes are shown in red characters.

Necessary WAIT				Address	I/O register (SFR) Name								R/W		
READ (Min.)	READ (Max.)	WEITE (Min.)	WRITE (MAX.)		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	1	8	16
-	-	-	-	F0014	RESOC (RESET output control register)								E	E	-
												RESO			
-	-	-	-	F0016	STPSTC (STOP status output control register)								E	E	-
					STOPEN			STPLV							
-	-	-	-	F0018	LBCTL (LCD bus interface mode register)								E	E	-
					EL	IMD	LBC1	LBC0	TCIS		TPF	BYF			
-	-	-	-	F0019	LBCYC (LCD bus interface cycle control register)								-	E	-
-	-	-	-	F001A	LBWST (LCD bus interface wait control register)								-	E	-
-	-	-	-	F001F	DMATSEL (DMA trigger selection register)								E	E	-
											DMATSL23	DMATSL01			
-	-	-	-	F003A	PU10 (Pull-up resistor option register 10)								E	E	-
					PU107	PU106	PU105	PU104	PU103	PU102	PU101	PU100			
-	-	-	-	F003B	PU11 (Pull-up resistor option register 11)								E	E	-
					PU117	PU116	PU115	PU114	PU113	PU112	PU111	PU110			
-	-	-	-	F003C	PU12 (Pull-up resistor option register 12)								E	E	-
					PU127	PU126	PU125								
-	-	-	-	F004B	PIM11 (Port input mode register 11)								E	E	-
					PIM117	PIM116	PIM115	PIM114	PIM113	PIM112	PIM111	PIM110			
-	-	-	-	F0054	LCDPF4 (LCD port function register 4)								E	E	-
					LCDPF47	LCDPF46	LCDPF45	LCDPF44	LCDPF43	LCDPF42					
-	-	-	-	F005A	LCDPF10 (LCD port function register 10)								E	E	-
					LCDPF107	LCDPF106	LCDPF105	LCDPF104	LCDPF103	LCDPF102	LCDPF101	LCDPF100			
-	-	-	-	F005B	LCDPF11 (LCD port function register 11)								E	E	-
					LCDPF117	LCDPF116	LCDPF115	LCDPF114	LCDPF113	LCDPF112	LCDPF111	LCDPF110			
-	-	-	-	F005C	LCDPF12 (LCD port function register 12)								E	E	-
					LCDPF127	LCDPF126	LCDPF125								
-	-	-	-	F006D	SNFEN0 (Noise filter enable register for SAU)								E	E	-
										SNFEN02					
1	1	1	1	F0335	SEG53 (LCD display data memory 53)								-	E	-

Necessary WAIT				Address	I/O register (SFR) Name								R/W		
READ (Min.)	READ (Max.)	WEITE (Min.)	WRITE (MAX.)		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	1	8	16
-	-	-	-	FFF0A	P10 (Port register 10)								E	E	-
					P107	P106	P105	P104	P103	P102	P101	P100			
-	-	-	-	FFF0B	P11 (Port register 11)								E	E	-
					P117	P116	P115	P114	P113	P112	P111	P110			
-	-	-	-	FFF2A	PM10 (Port mode register 10)								E	E	-
					PM107	PM106	PM105	PM104	PM103	PM102	PM101	PM100			
-	-	-	-	FFF2B	PM11 (Port mode register 11)								E	E	-
					PM117	PM116	PM115	PM114	PM113	PM112	PM111	PM110			
-	-	-	-	FFF2C	PM12 (Port mode register 12)								E	E	-
					PM127	PM126	PM125								
-	-	-	-	FFF44	LBDATA (LCD bus interface data register)								-	-	E
					LBDATAL								-	E	-
-	-	-	-	FFF46	LBDATAR (LCD bus interface read data register)								-	-	E
					LBDATARL								-	E	-