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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A857A/E	Rev.	1.00
Title	Correct SH7734 User's Manual:Hardware(HSPI)		Information Category	Technical Notification		
Applicable Product	SH7734	Lot No. All lots	Reference Document	SH7734 User's Manual: Hardware Rev.1.00 (R01UH0233EJ0100)		

There is correction and addition to explanation of "18.Serial Peripheral Interface (HSPI)" in SH7734 User's Manual.

The correction is shown by shading.

1. Correct to "18.1.1 Features" in page 1567

<Wrong>

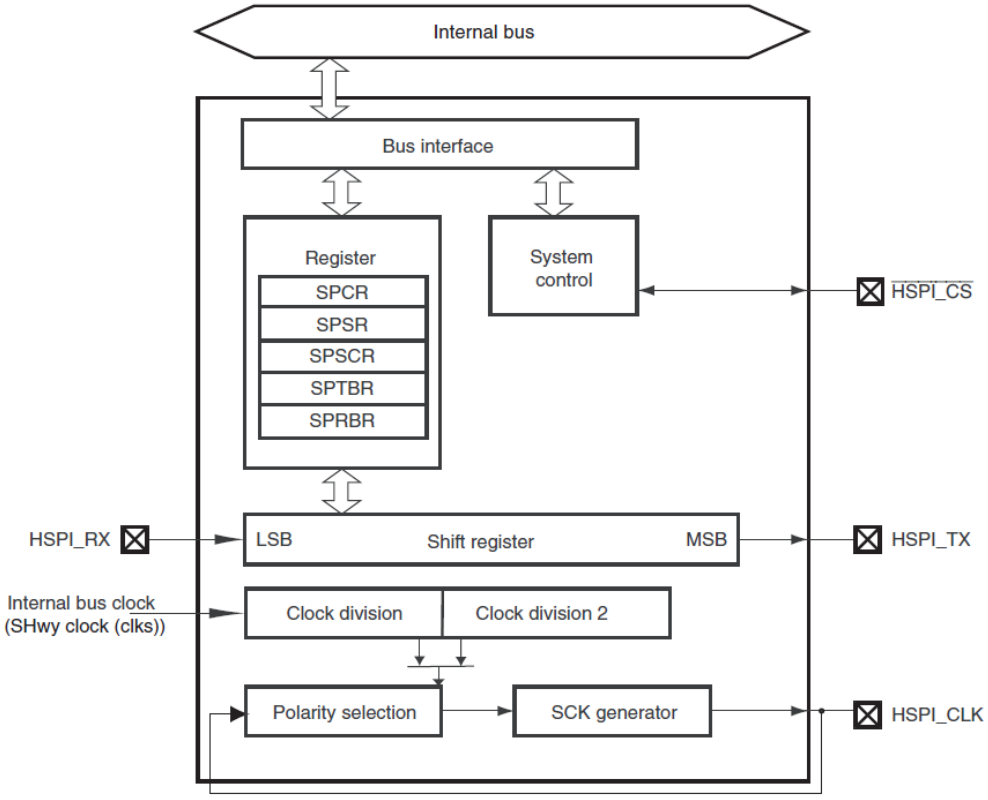
Independent DMA transfer of data for transmission and received data is possible through two DMA channels.

<Correct>

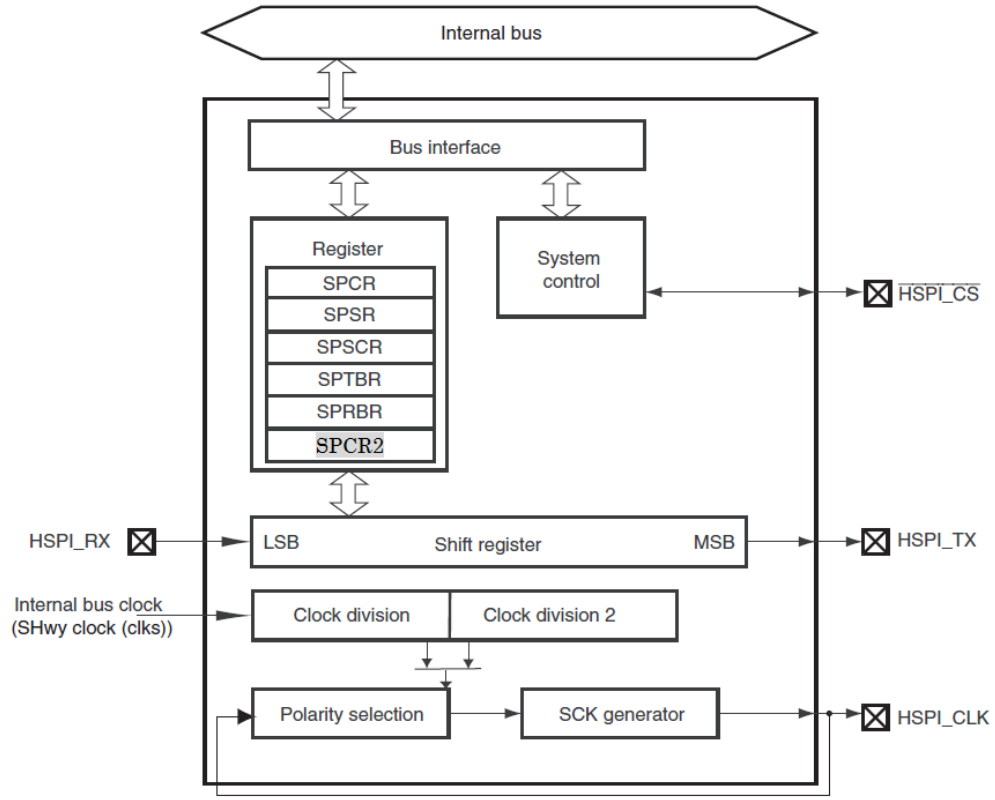
Independent DMA transfer of dat a for trans mission and received data is possible through two DMA channels. Transmission and reception in master mode are supported as high-speed modes for use with DMA transfer.

2. Correct to “Figure 18.1 Block Diagram of HSPI” in page 1568

<Wrong>



<Correct>



3. Correct to “Table 18.2(1) Register Configuration” in page 1569

<Wrong>

Receive buffer register	SPRBR	R	H'10	32

<Correct>

Receive buffer register	SPRBR	R	H'10	32
Control register 2	SPCR2	R/W	H'14	32

4. Correct to “Table 18.2(2) Register State in Each Operating Mode” in page 1570

<Wrong>

SPRBR	Initialized	Initialized	Retained	Retained	Retained	Initialized

<Correct>

SPRBR	Initialized	Initialized	Retained	Retained	Retained	Initialized
SPCR2	Initialized	Initialized	Retained	Retained	Retained	Initialized

5. Add “18.2.6 Control register 2” to page 1582 as explanation SPCR2

<Wrong>

This explanation is nothing.

<Correct>

18.2.6 Control Register 2 (SPCR2)

SPCR2 is a 32-bit readable and writable register that is used to set the clock frequency for data transfer when transfer is to be at a higher rate than that set in the SPCR.

Transmission and reception in master mode are supported as high-speed modes for use with DMA transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HFE	—	—	—	—	CKHP4	CKHP3	CKHP2	CKHP1	CKHP0	CKCYC5	CKCYC4	CKCYC3	CKCYC2	CKCYC1	CKCYC0
Initial value:	0	—	—	—	—	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	—	R	Reserved These bits are always read as an undefined value. The write value should always be 0.
15	HFE	0	R/W	High-speed transfer enable Enables or disables generation of a serial clock signal with the division ratio set in SPCR2. 0: The clock setting in SPCR2 is disabled. 1: The clock setting in SPCR2 is enabled.
14 to 11	—	—	R	Reserved These bits are always read as an undefined value. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
10 to 6	CKHP[4:0]	0	R/W	Serial clock high period The width at high level of the serial bit clock is set to (this setting) cycles of the SuperHyway clock (clks). If the width at high level is not set to half of the period setting in CKCYC, the duty cycle will greatly diverge from 50:50.
5 to 0	CKCYS[5:0]	0	R/W	Serial clock period The period of the serial bit clock is set to (this setting - 1) cycles of the SuperHyway clock (clks). The maximum frequency of the serial bit clock is 20 MHz. In accord with the formula for calculation given below, the CKCYC value should be no less than 9.

The serial bit clock frequency can be computed using the following formula:

$$\text{Serial bit clock frequency} = \frac{\text{SuperHyway (Internal bus) clock frequency}}{\text{CKCYC} + 1}$$

If any bit (FBS, CLKP, IDIV or CLKC) of SPCR is changed or any bit of SPCR2 is changed, the HSPI is soft reset.

Register settings and serial bit-clock frequencies are indicated below.

CKCYC[5:0]	CKHP[4:0]	Serial bit clock frequency	Duty
D'9	D'5	SuperHyway clock frequency/10	50%
D'11	D'6	SuperHyway clock frequency/12	50%
D'13	D'7	SuperHyway clock frequency/14	50%
D'15	D'8	SuperHyway clock frequency/16	50%
D'17	D'9	SuperHyway clock frequency/18	50%
D'63	D'32	SuperHyway clock frequency/64	50%

6. Correct “18.3.5 HSPI Software Reset” to page 1587

<Wrong>

The HSPI software reset is generated when the control bits except SPCR, the interrupt/DMA enable bits and the chip select value bit (CSV) of SPSCR are modified.

<Correct>

The HSPI software reset is generated when the control bits except SPCR/SPCR2, the interrupt/DMA enable bits and the chip select value bit (CSV) of SPSCR are modified.

- End of report -