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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A856A/E	Rev.	1.00
Title	The error correction about target memory devices connected to memory controller(DBSC3).		Information Category	Technical Notification		
Applicable Product	SH7734	Lot No. ALL	Reference Document	SH7734 User's Manual : Hardware Rev.1.00 (R01UH0233EJ0100)		

We would like to inform you of the following error correction about target memory devices connected to the memory controller(DBSC3).

[Error] Table 4.1 DBSC3 Functions (common to all the SDRAM types)

Memory to be connected	DDR3-SDRAM compliant with JEDEC. (The controller supports the connection of memory devices having capacities from 512 Mbits to 2 Gbits, with two devices connectable if the data bus width is 8 bits and one device connectable if the data bus width is 16 bits. SDRAM with a data bus width of 4 bits is not supported. The controller does not support write leveling.) DDR2-SDRAM compliant with JEDEC. (The controller supports the connection of memory devices having capacities from 256 Mbits to 2 Gbits, with two devices connectable if the data bus width is 8 bits and one device connectable if the data bus width is 16 bits. SDRAM with a data bus width of 4 bits is not supported.)

[Correction] Table 4.1 DBSC3 Functions (common to all the SDRAM types)

Memory to be connected	DDR3-SDRAM compliant with JEDEC. (The controller supports the connection of memory devices having capacities from 512 Mbits to 1 Gbits, with two devices connectable if the data bus width is 8 bits, memory devices having capacities from 512 Mbits to 2 Gbits, with one device connectable if the data bus width is 16 bits. SDRAM with a data bus width of 4 bits is not supported. The controller does not support write leveling.) DDR2-SDRAM compliant with JEDEC. (The controller supports the connection of memory devices having capacities from 256 Mbits to 1 Gbits, with two devices connectable if the data bus width is 8 bits, memory devices having capacities from 256 Mbits to 2 Gbits, with one device connectable if the data bus width is 16 bits. SDRAM with a data bus width of 4 bits is not supported.)