

Packaging Information

PCB Thermal Land Design for Ceramic Packages with Bottom Metal or Heat Sinks

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Introduction

Certain Intersil ceramic packages include bottom metal or bottom heat sinks (also called heat slugs). When present, these features will be noted on Intersil’s product datasheet Package Outline Drawings (POD). The POD includes the bottom metal or bottom heat sinks features and their dimensions. The bottom metal or heat sink provide for a direct thermal path out of the bottom of the package, which can significantly improve thermal performance.

Packages with such built-in thermal enhancements are generally based on styles such as ceramic quad flat-packs and ceramic dual flat-packs (see [Figures 1](#) and [2](#)). This tech brief provides guidance to help optimize the board design to take full advantage of such a package’s built-in thermal enhancements.

It should be emphasized that these guidelines are general in nature and should only be considered a starting point in this effort. The user must apply their actual experiences and development efforts to optimize designs and processes for their manufacturing practices and the needs of varying end-use applications.

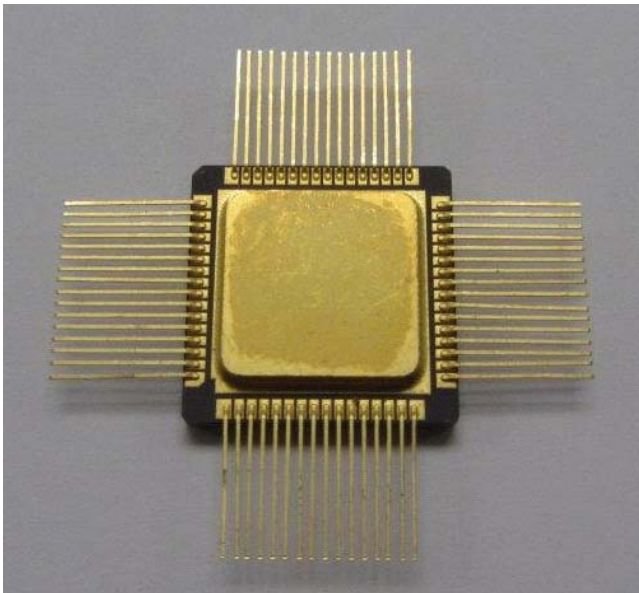


FIGURE 1. ISL70003SEHFE CERAMIC QUAD FLAT-PACK PACKAGE WITH HEAT SINK

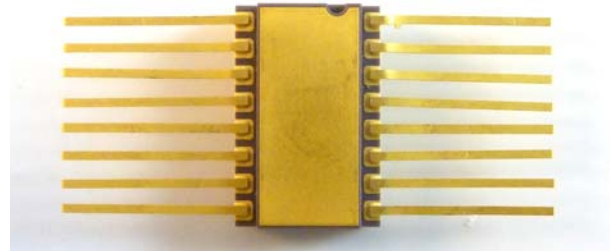


FIGURE 2. ISL75052SEHF CERAMIC DUAL FLAT-PACK PACKAGE WITH BOTTOM METAL

General Design Guidelines for Thermally Enhanced Packages

The bottom metal or heat sink features are intended to be mounted directly to a matching “thermal land” pad pattern on the printed circuit board (PCB). The mounting should be accomplished using materials such as solder, thermal and or electrically conductive or non-conductive epoxy. Choice of mounting material may be affected by whether or not electrical connection between the package bottom and PCB is needed, by board assembly facility capabilities or various application requirements (temperature extremes involved, low out-gassing properties, etc.).

To take full advantage of the bottom heat-escape path, the board design should include thermal vias dropped down beneath the “thermal land” to one or more buried or back-side planes. This helps overcome the PCB’s base material’s relatively poor thermal conductivity.

The closer thermal coupling of the device to the buried planes results in more efficient heat spreading and more uniform temperature distribution across the board. This combination of vias for vertical heat escape and planes (and/or higher conductivity board material) for heat spreading, helps enable the IC device to achieve its full performance potential.

Land Pattern Guidelines

Peripheral I/O Lands

Packages with such built-in thermal enhancements are generally based on styles such as ceramic dual flat-packs and ceramic quad flat-packs and typically use the same peripheral I/O lead designs. These leads are generally formed with gull-wing shapes prior to soldering to the board.

For the peripheral I/O lands on the board, the standard design methodology (for packages without bottom metal or heat sinks) can be used. Note that the vertical level of the bottom of formed lead feet should:

In the case of solder-mounting of the base: Peripheral I/O leads should be formed to coincide with the package bottom plane.

In the case of “thick” epoxy, etc. mounting of the base: Peripheral I/O leads should be formed lower than the package bottom plane by an amount coinciding with the thickness of the base mounting material (i.e. so that the peripheral I/O leads will be allowed to sit fully down on their board I/O lands during solder reflow).

Board Thermal Land

The board thermal land (beneath the package's bottom metal or heat sink), should have an X-Y size approximately the “same-size-as” to 0.2mm larger than the nominal bottom metal or heat sink size. If the base will be solder mounted, an overly large thermal land (and solder mask opening) should be avoided since this could adversely affect the “self-alignment” tendency of the package during solder reflow. See [Figures 3](#) and [4](#) for examples of thermal land patterns with and without plugged vias.

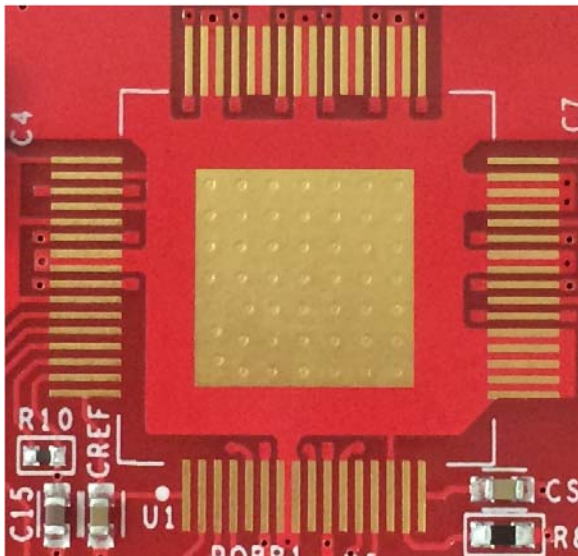


FIGURE 3. ISL70003SEH EVALUATION BOARD THERMAL LAND WITH PLUGGED VIAS TO ELIMINATE SOLDER WICKING

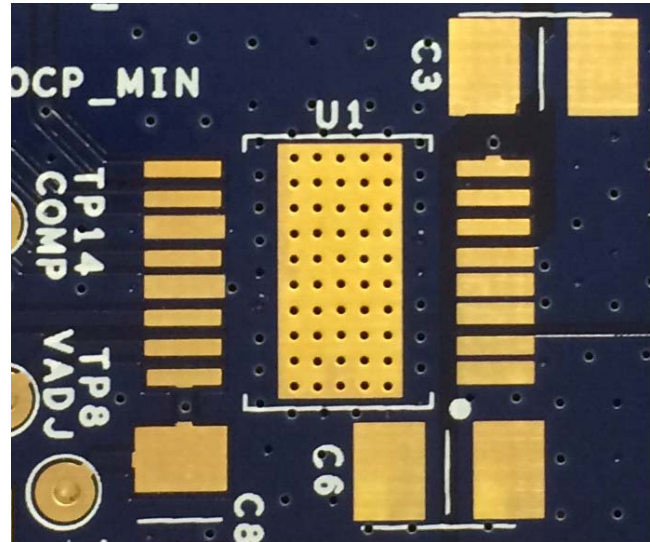


FIGURE 4. ISL75052SEH EVALUATION BOARD THERMAL LAND WITH VIAS TO DISSIPATE HEAT

Thermal Vias

A grid of 1.0mm to 1.2mm pitch thermal vias, which drop down and connect to the buried copper plane(s), should be placed under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter, with the barrel plated to about 1.0 ounce copper. Use this type of via scheme, or similar designs as appropriate based on manufacturing capabilities or preferences.

Although adding more vias (such as by decreasing via pitch) will improve thermal performance, diminishing returns will be seen as more and more vias are added. Therefore, simply use as many vias as practical for the thermal land size and your board design ground rules.

Solder Mask Design

Two types of land patterns are used for surface mount packages:

- Solder Mask Defined (SMD): Solder mask openings smaller than metal pads.
- Non-Solder Mask Defined (NSMD): Solder mask openings larger than metal pads.

Better control of the copper etching process as compared to the solder masking process makes NSMD preferable. Also, the SMD pad definition can introduce stress concentrations near the solder mask overlap region that can result in solder joints cracking under extreme fatigue conditions. Using NSMD instead improves the reliability of solder joints as solder is allowed to “wrap around” the sides of the metal pads on the board.

For these reasons, NSMD is recommended for the perimeter I/O lands and generally for the thermal land as well.

Solder Masking of I/O Lands

For NSMD lands, the solder mask opening should be about 120µm to 150µm+ larger than the I/O land size, providing a 60µm to 75µm+ design clearance between the copper land and solder mask.

Typically each I/O land on the PCB should have its own solder mask opening with a web of solder mask between adjacent pads. The lead pitch of ceramic/metal packages is generally large enough to accomplish this. A less-preferred alternate method is to use one big opening, designed around a whole strip of I/O lands (for instance all the lands on one side of a package) with no solder mask in between them.

Solder Masking of the Thermal Land (for the case of solder mounting the package base)

For NSMD lands, the solder mask opening should be about 120µm to 150µm+ larger than the thermal land size, providing a 60µm to 75µm+ design clearance between the copper land and solder mask.

When the package bottom metal or heat sink is solder mounted, solder masking is also required for thermal vias to prevent solder wicking inside the vias, drawing solder away from the thermal land interface. The solder mask diameter should be about 100µm larger than the via diameter. The vias can be plugged or tented with solder mask, either from the bottom or top surface of the PCB (see [Figure 3](#)). Tenting from the top is considered a better option as it results in smaller voids under the die pad. Solder masking of vias from the bottom side can result in increased outgassing during reflow, creating bigger voids around vias. Note that small voids in this area are not unusual and will have little effect on thermal or electrical performance.

Stencil Guidelines

Stencil Design for I/O Lands

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2mil to 3mil) standoff height. The solder paste stencil design is the first step in developing such optimized, reliable joints.

Stencil aperture size-to-land size should typically be a 1:1 ratio. For finer pitch parts, the aperture width may be reduced slightly if desired to help prevent solder bridging between adjacent I/O lands.

Stencil Design for Thermal Land (for the case of solder mounting the package base)

To reduce solder paste volume on the thermal land, it is recommended that an array of small paste dispensing apertures be used instead of one large aperture. The smaller apertures can be circular or square and of various dimensions and array sizes; but the main goal should be a dimensional combination that results in 50% to 80% solder paste coverage across the thermal land.

The thermal land's solder paste coverage should not be reduced too low since this could potentially affect "self-alignment" of the package during solder reflow and could contribute to increased solder voiding.

Stencil Type and Thickness

A laser-cut, stainless steel stencil with electro-polished trapezoidal walls is recommended. Electropolishing "smooths" aperture walls, resulting in reduced surface friction, good paste release and void reduction. Using a trapezoidal section aperture (TSA) promotes paste release and also forms "brick-like" paste deposits that assist in firm component placement.

A 0.15mm to 0.2mm stencil thickness is generally recommended for typical ceramic/metal packages.

Solder Paste and Reflow Profile

A system board reflow profile depends on the thermal mass of the entire populated board, so it's not practical to define a specific soldering profile just for a specific package/product.

Consult with paste manufacturers to choose a suitable solder paste type, and use a reflow profile appropriate for the specifics of the particular board design. Use the lowest practical peak reflow temperature which still provides for thorough solder reflow and good solder joint quality across the entire populated board.

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