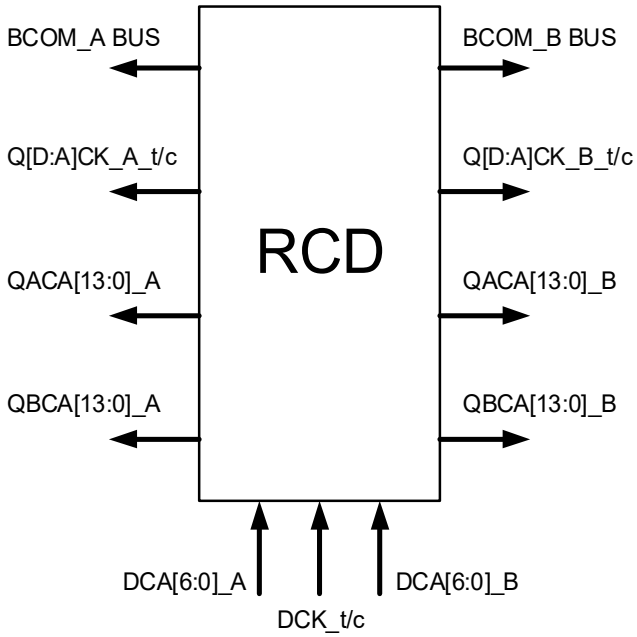
RG5R364A0C0GBY

DDR5 Registering Clock Driver

The RG5R364A0C0GBY is a registering clock driver used on DDR5 RDIMMs, LRDIMMs, and NVDIMMs. Its primary function is to buffer the Command/Address (CA) bus, chip selects, and clock between the host controller and the DRAMs. It also creates a BCOM bus which controls the data buffers for LRDIMMs.

It contains two separate channels which have some common logic such as clocking, but otherwise operate independently of each other. Each channel has a 7-bit double data rate CA bus input, a single parity input, two chip select inputs, and produces two copies of 14-bit single data rate CA bus outputs, and two copies of the chip select outputs. The RCD has a common clock input and PLL, but produces four separate clock pairs to the DRAM channels.

Block Diagram



Features

- Pinout optimized DDR5 RDIMM and LRDIMM PCB layout
- DDR5 server speeds up to 6400MT/s
- Supports power-down modes to conserve server power
- Supports 1-rank/2-rank DIMM configurations
- Supports SDP, DDP, 3DS DRAM types
- Provides access to internal control words for configuring device features and adapting to different RDIMM and LRDIMM system applications
- I^2C and I3C sideband access for asynchronous register access control
- BCOM for LRDIMM data buffer control
- Loopback and pass-through modes
- Package: 8.7 × 13.5 mm, 240-FCBGA

Applications

- RDIMM, LRDIMM, NVDIMM modules for Enterprise Servers
- Memory down server motherboards

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