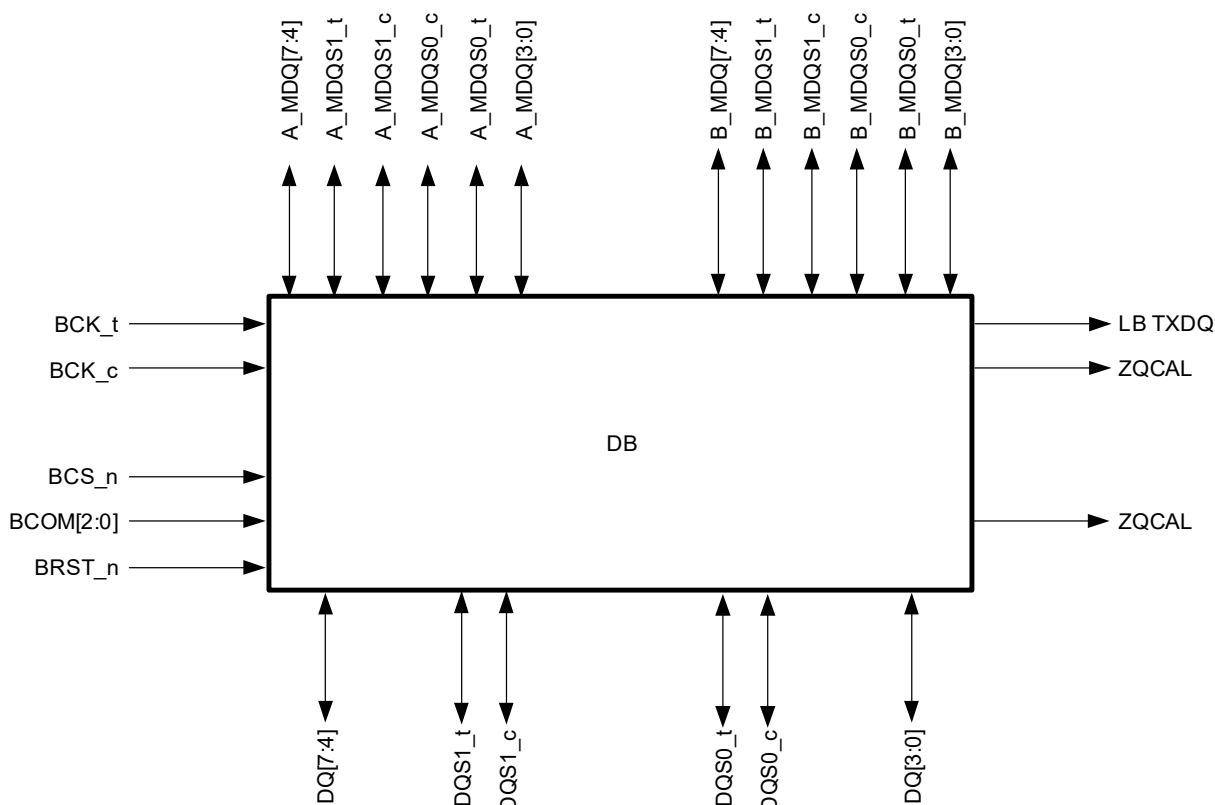# RG5D188C1AIGBX

DDR5 Multiplexing Data Buffer

The RG5D188C1AIGBX (MDB) is a DDR5 Multiplexing Data Buffer. Its primary function is to demultiplex and buffer data from the Host CPU to DRAMs. It has two 4-bit data interfaces to the Host, running at twice the speed of the DRAM interfaces. Each Host interface multiplexes two pseudo-channels, both of which have a separate 4-bit DRAM interface. The RG5D188C1AIGBX supports x4 or x8 DRAMs. It also has an input-only control bus interface that is connected to an DDR5 MRCD, as well as a dedicated pin for ZQ Calibration and loopback outputs for test purposes.

Applications

MRDIMM modules for Enterprise Servers.

Block Diagram

Features

- Pinout optimized MRDIMM PCB layout
- DDR5 Server speeds up to 8800MT/s
- Supports power-down modes to conserve server power
- Supports up to 2 ranks per pseudo-channel in both x4 and x8 configurations.
- Supports SDP, DDP, and 3DS DRAM types
- Provides access to internal control words for configuring device features and adapting to different MRDIMM and system applications
- Loopback and pass-through modes
- Training support features for DQ and MDQ interfaces
- ZQ calibration

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