4RCD0124KC0

DDR4 Register Command Address Buffer with Parity

Description

The 4RCD0124KC0 is a 32-bit 1:2 register command, address buffer with parity, and is designed for 1.2V VDD operation.

All inputs are pseudo-differential with an external or internal voltage reference. All outputs are full-swing CMOS drivers optimized to drive single-terminated 25Ω to 50Ω traces in DDR4 RDIMM and LRDIMM applications. The clock outputs Yn_t and Yn_c and control net outputs QxCKEn, QxCSn, and QxODTn can be driven with a different strength to compensate for different DIMM net topologies. By disabling unused outputs the power consumption is reduced.

The 4RCD0124KC0 operates from a differential clock (CK_t and CK_c). Inputs are registered at the crossing of CK_t going HIGH, and CK_c going LOW. The input signals can be either re-driven to the outputs or can be used to access device internal control registers when certain input conditions are met.

Features

- Pinout optimized DDR4 RDIMM PCB layout
- DDR4-1600/1866/2133/2400
- Supports CKE Power Down operation modes
- Support Quad Chip Select Operation
  - Direct Dual CS Mode
  - Direct QuadCS Mode
  - Encoded QuadCS Mode
- Provides access to internal control words for configuring the device features and adapting in different RDIMM and system applications
- Compliant to *JEDEC DDR4RCD01 Spec* rev 1.0
- Available in 253-ball Dual-Pitch (0.50mm/0.65mm), 15 x 20 grid, Rectangular Ball Grid Array Package

Applications

- Servers with DIMM data rates up to 2400

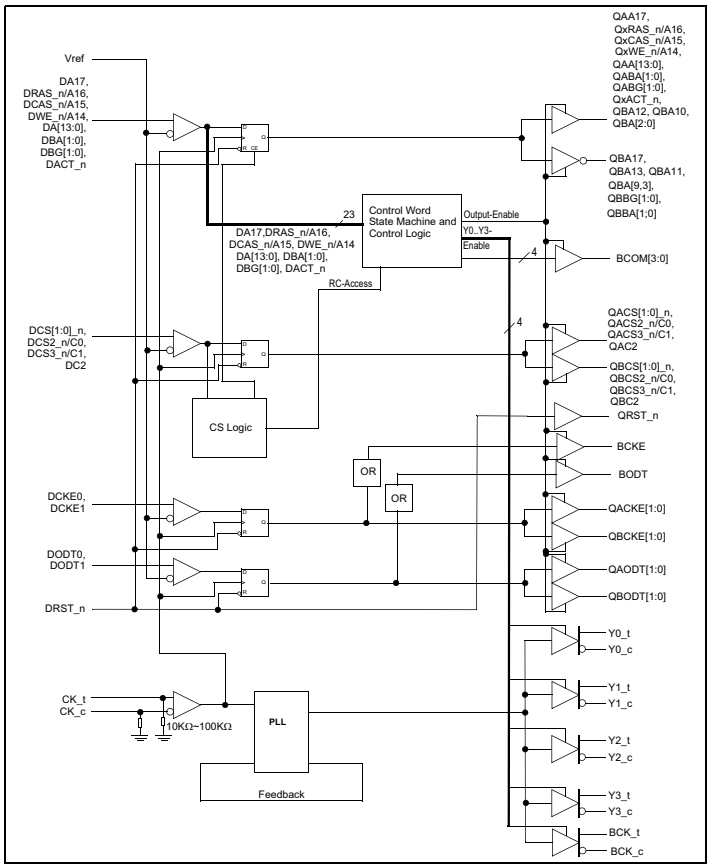

Figure 1. Block Diagram

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