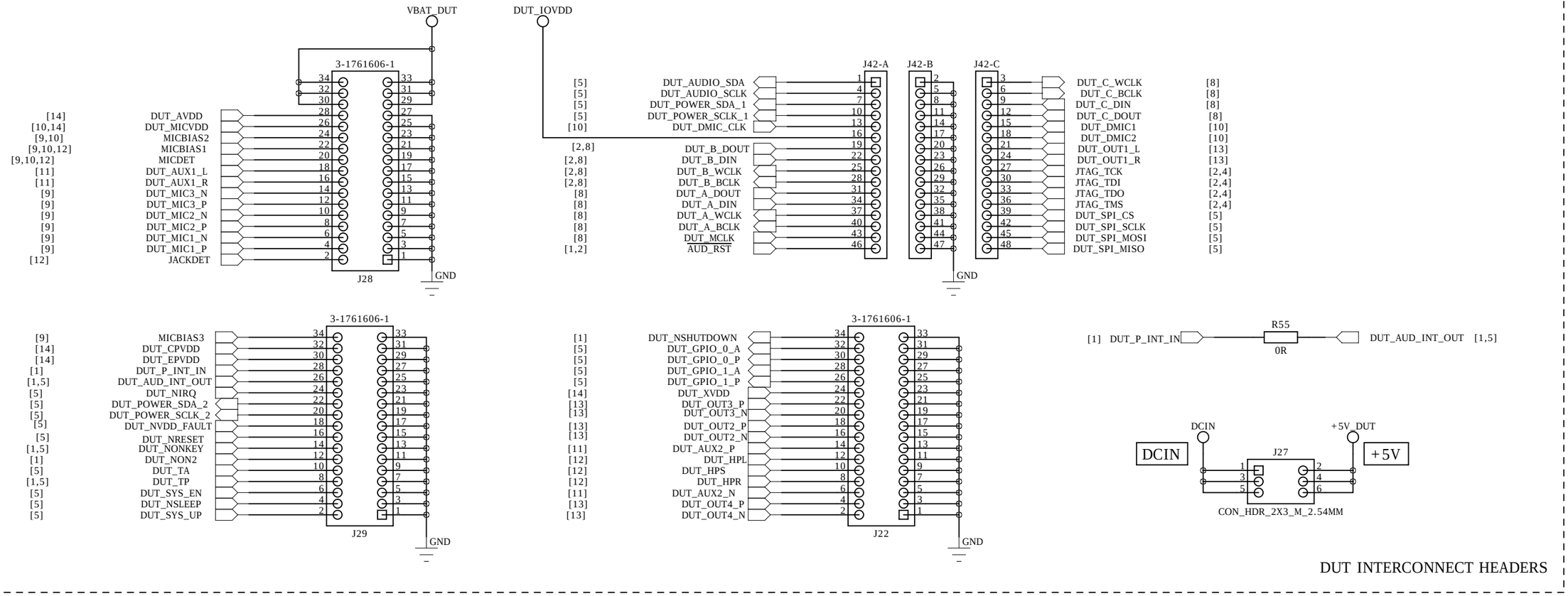
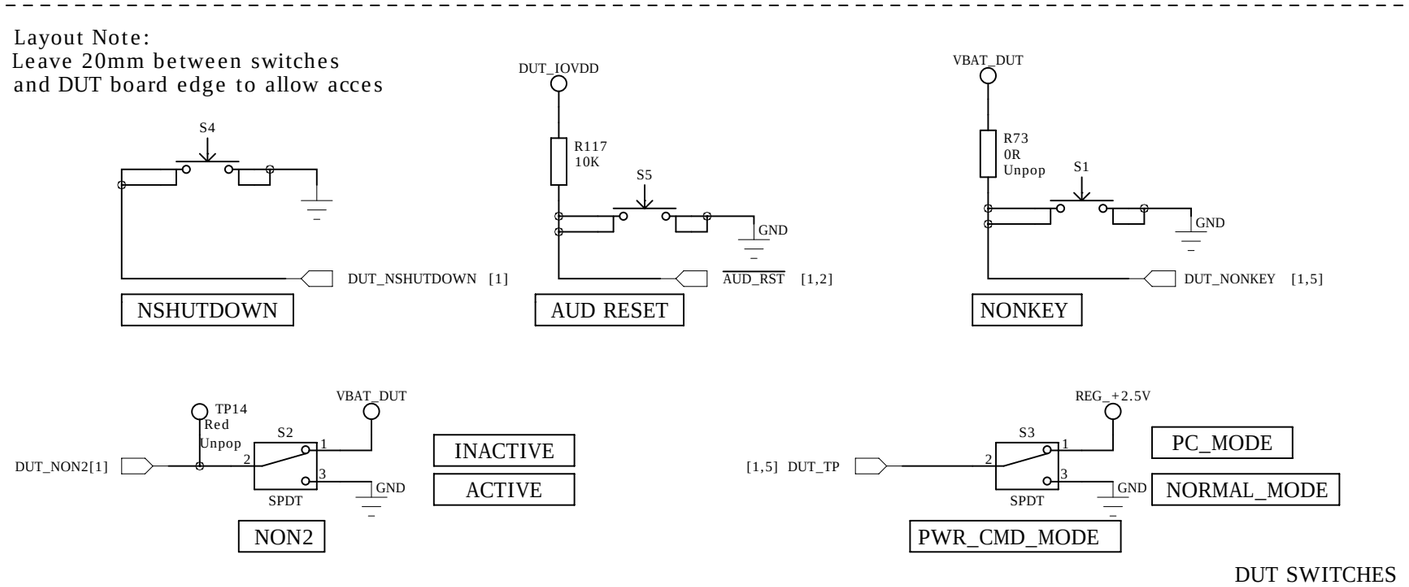
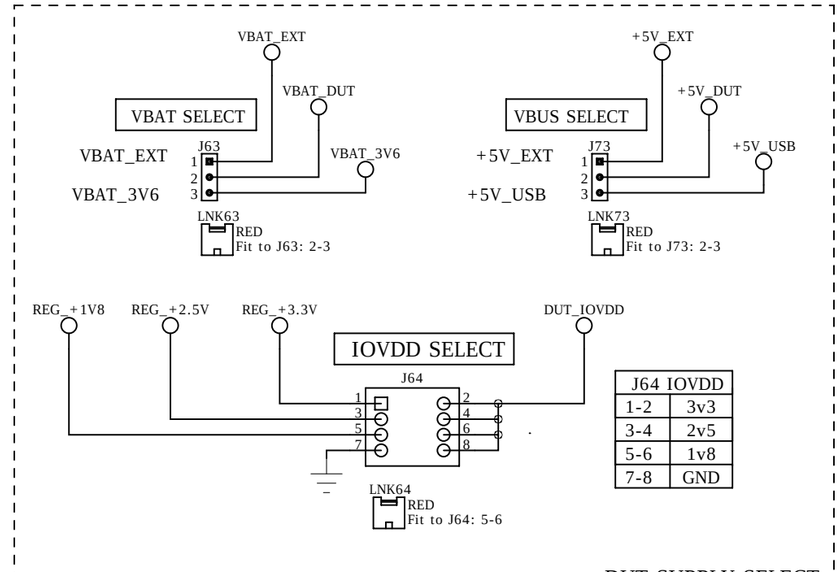




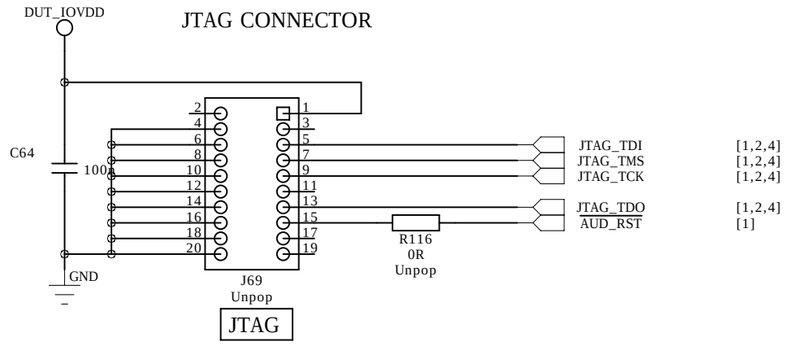


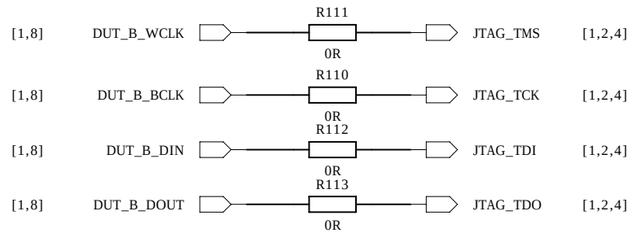
SCHEMATIC TEMPLATE REV PA2 (November 30, 2011) DIALOG DOCUMENT NUMBER 31-902-03

CONFIDENTIAL INFORMATION

TITLE: AUDIO DSP PMIC CUSTOMER EVAL BOARD			
PREPARED: BL/BT	DATED: 23/04/2013	DRAWING NO: 44-179-170-01-B	REV: C
RESPONSIBLE: BT	DATED: 23/04/2013	SHEET NAME: DUT_HEADERS	PAGE: 1 OF 16

dialog SEMICONDUCTOR





SCHEMATIC TEMPLATE REV PA2 (November 30, 2011) DIALOG DOCUMENT NUMBER 31-902-03

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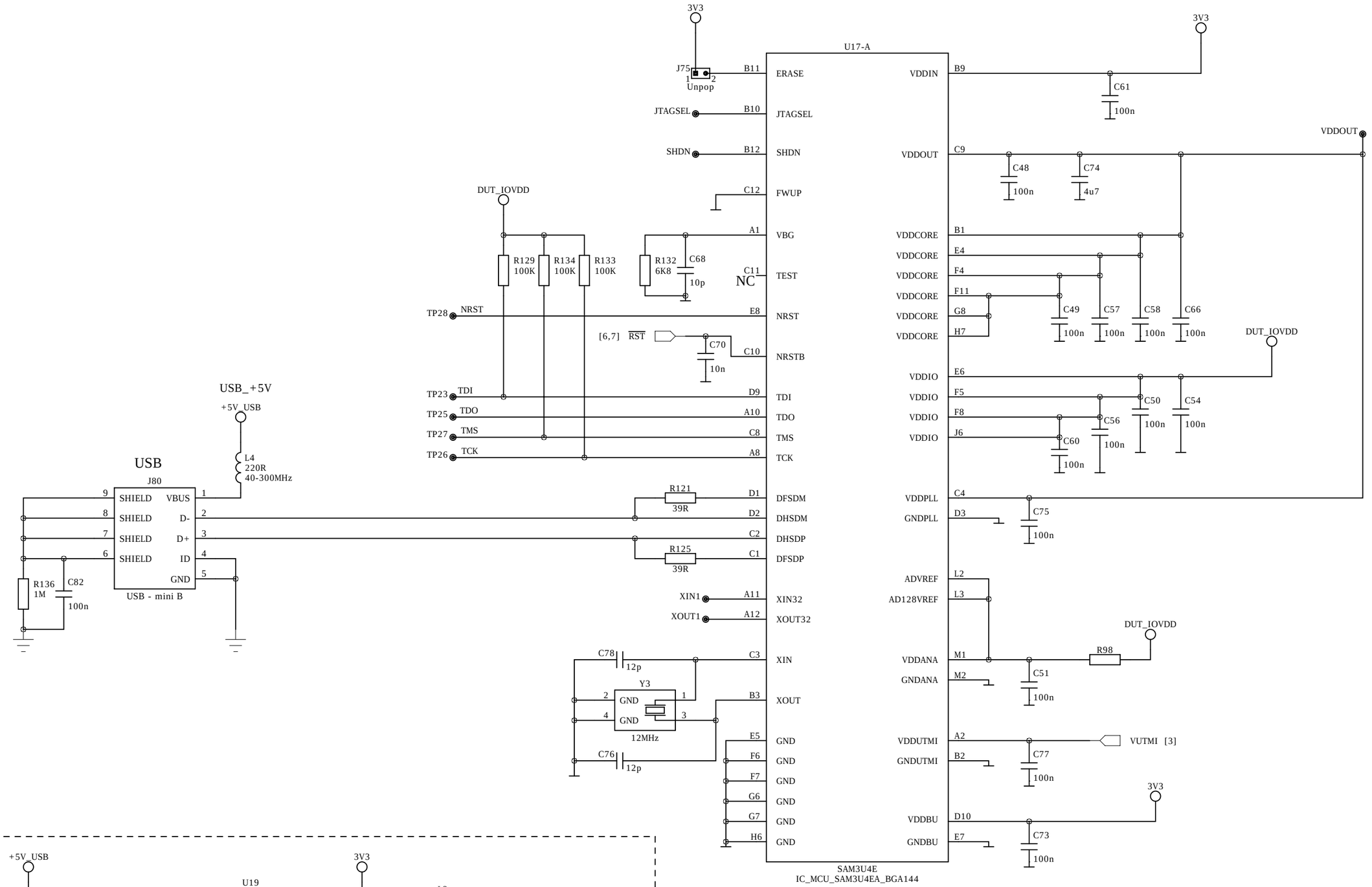
PREPARED: BL/BT	DATED: 23/04/2013	DRAWING NO: 44-179-170-01-B	REV: C
RESPONSIBLE: BT	DATED: 23/04/2013	SHEET NAME: JTAG	PAGE: 2 OF 16



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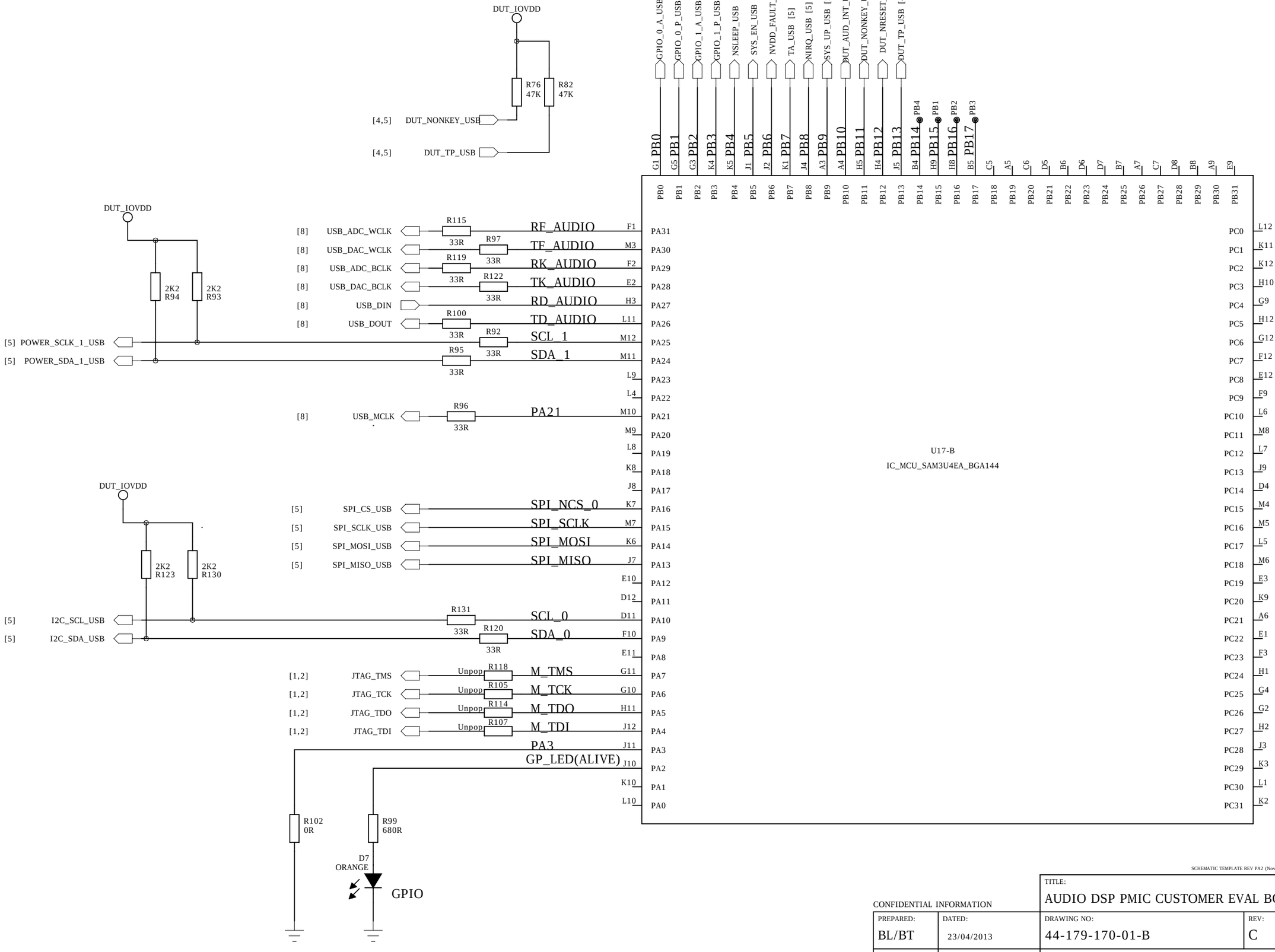
TITLE: AUDIO DSP PMIC CUSTOMER EVAL BOARD			
PREPARED: BL/BT	DATED: 23/04/2013	DRAWING NO: 44-179-170-01-B	REV: C
RESPONSIBLE: BT	DATED: 23/04/2013	SHEET NAME: USB_IF	PAGE: 3 OF 16



SCHEMATIC TEMPLATE REV PA2 (November 30, 2011) DIALOG DOCUMENT NUMBER 31-902-03

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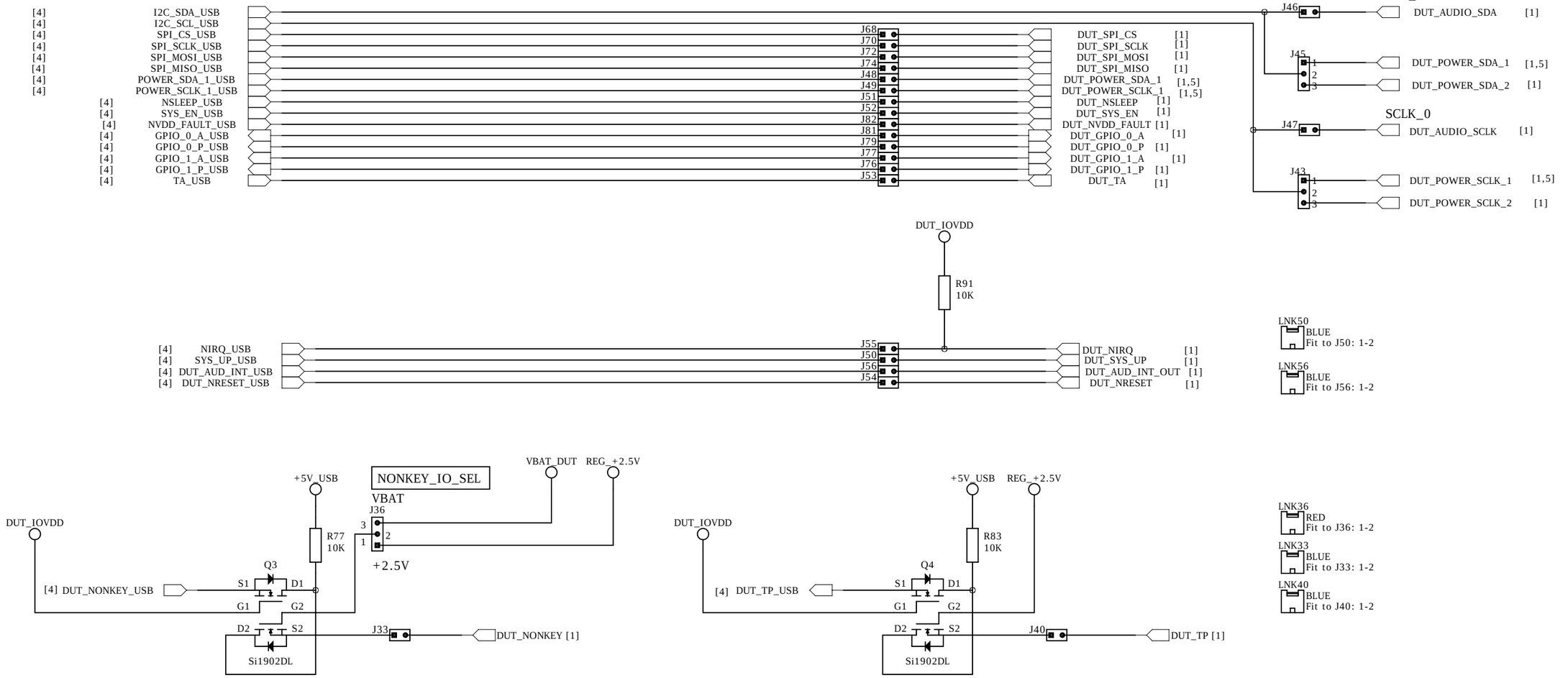
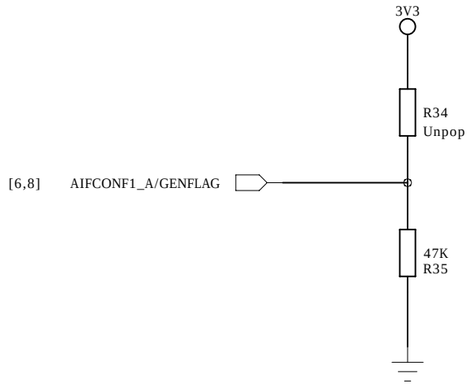
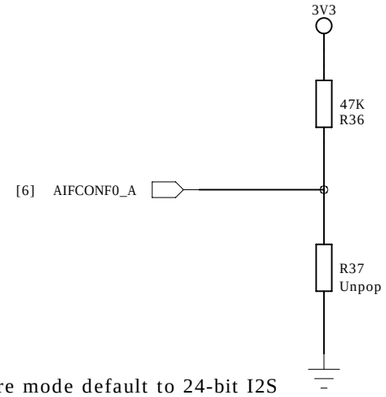
TITLE: AUDIO DSP PMIC CUSTOMER EVAL BOARD			
PREPARED: BL/BT	DATED: 23/04/2013	DRAWING NO: 44-179-170-01-B	REV: C
RESPONSIBLE: BT	DATED: 23/04/2013	SHEET NAME: USB_LEVEL_SHIFTER	PAGE: 4 OF 16

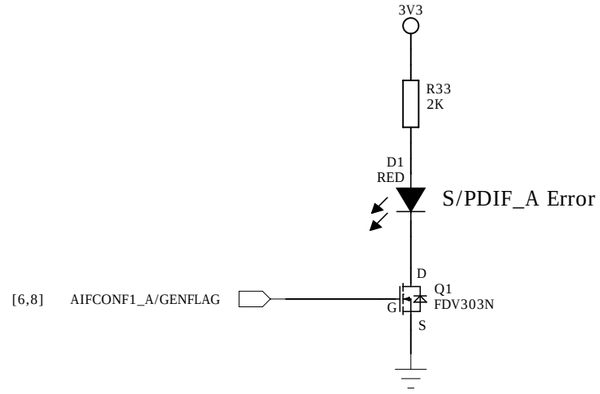
SAM3U - DUT I/F

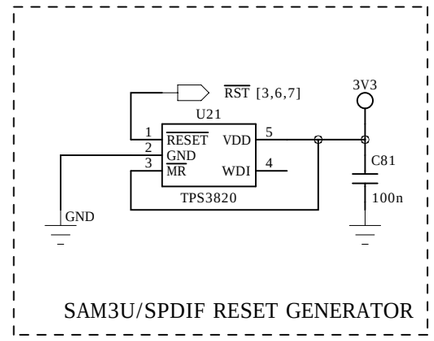

[4] I2C_SDA_USB
[4] I2C_SCL_USB
[4] SPI_CS_USB
[4] SPI_SCLK_USB
[4] SPI_MOSI_USB
[4] SPI_MISO_USB
[4] POWER_SDA_1_USB
[4] POWER_SCLK_1_USB
[4] NSLEEP_USB
[4] SYS_EN_USB
[4] NVDD_FAULT_USB
[4] GPIO_0_A_USB
[4] GPIO_0_P_USB
[4] GPIO_1_A_USB
[4] GPIO_1_P_USB
[4] TA_USB
J68 J70 J72 J74 J48 J49 J51 J52 J82 J81 J79 J77 J76 J53
DUT_SPI_CS [1]
DUT_SPI_SCLK [1]
DUT_SPI_MOSI [1]
DUT_SPI_MISO [1]
DUT_POWER_SDA_1 [1,5]
DUT_POWER_SCLK_1 [1,5]
DUT_NSLEEP [1]
DUT_SYS_EN [1]
DUT_NVDD_FAULT [1]
DUT_GPIO_0_A [1]
DUT_GPIO_0_P [1]
DUT_GPIO_1_A [1]
DUT_GPIO_1_P [1]
DUT_TA [1]
J46
SDA_0
DUT_AUDIO_SDA [1]
J45
DUT_POWER_SDA_1 [1,5]
DUT_POWER_SDA_2 [1]
J47
SCLK_0
DUT_AUDIO_SCLK [1]
J43
DUT_POWER_SCLK_1 [1,5]
DUT_POWER_SCLK_2 [1]
DUT_IOVDD
R91
10K
[4] NIRQ_USB
[4] SYS_UP_USB
[4] DUT_AUD_INT_USB
[4] DUT_NRESET_USB
J55 J50 J56 J54
DUT_NIRQ [1]
DUT_SYS_UP [1]
DUT_AUD_INT_OUT [1]
DUT_NRESET [1]
LNK50 BLUE Fit to J50: 1-2
LNK56 BLUE Fit to J56: 1-2
LNK46 BLUE Fit to J46: 1-2
LNK45 BLUE Fit to J45: 2-3
LNK47 BLUE Fit to J47: 1-2
LNK43 BLUE Fit to J43: 2-3
LNK68 BLUE Fit to J68: 1-2
LNK70 BLUE Fit to J70: 1-2
LNK72 BLUE Fit to J72: 1-2
LNK74 BLUE Fit to J74: 1-2
LNK48 BLUE Fit to J48: 1-2
LNK49 BLUE Fit to J49: 1-2
LNK51 BLUE Fit to J51: 1-2
LNK52 BLUE Fit to J52: 1-2
LNK82 BLUE Fit to J82: 1-2
LNK81 BLUE Fit to J81: 1-2
LNK79 BLUE Fit to J79: 1-2
LNK77 BLUE Fit to J77: 1-2
LNK76 BLUE Fit to J76: 1-2
LNK53 BLUE Fit to J53: 1-2
+5V_USB
NONKEY_IO_SEL
VBAT
VBAT_DUT
REG_+2.5V
J36
3
2
1
+2.5V
R77
10K
DUT_IOVDD
Q3
[4] DUT_NONKEY_USB
S1 D1 G1 G2 D2 S2
Si1902DL
J33
DUT_NONKEY [1]
+5V_USB
REG_+2.5V
R83
10K
DUT_IOVDD
Q4
[4] DUT_TP_USB
S1 D1 G1 G2 D2 S2
Si1902DL
J40
DUT_TP [1]
LNK36 RED Fit to J36: 1-2
LNK33 BLUE Fit to J33: 1-2
LNK40 BLUE Fit to J40: 1-2



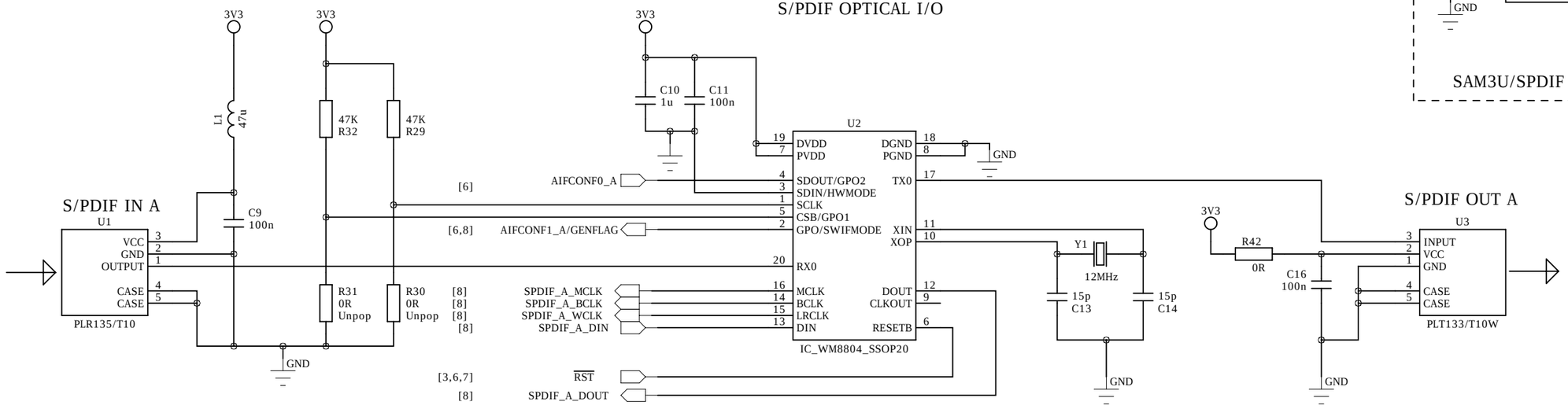


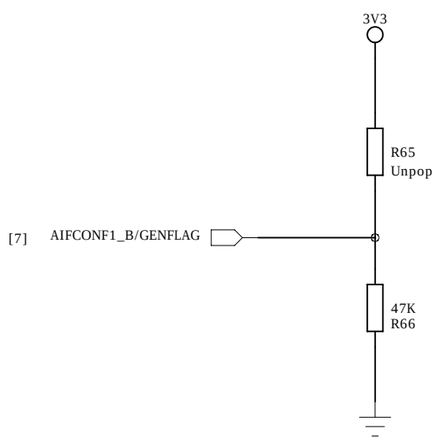
Hardware mode default to 24-bit I2S

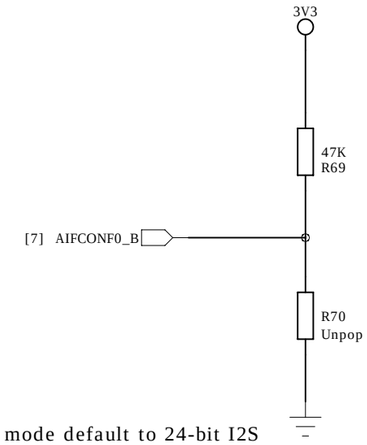




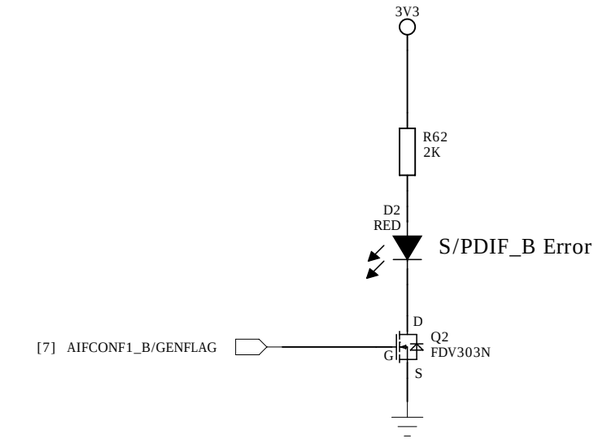
S/PDIF OPTICAL I/O







Hardware mode default to 24-bit I2S



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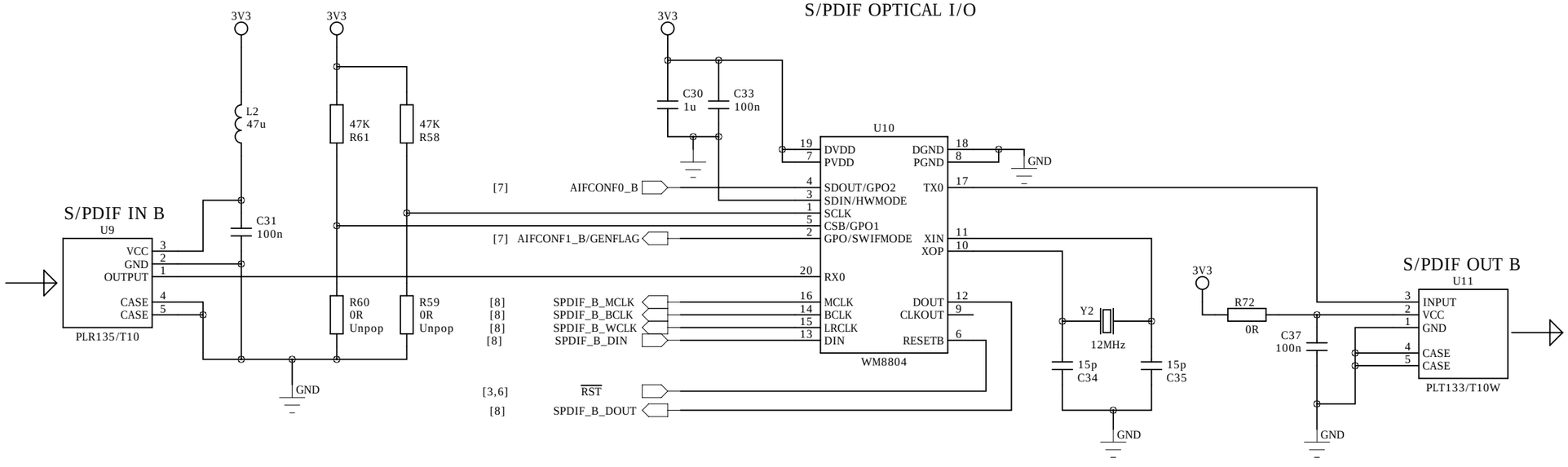

AIF2 SOURCE SELECT

SCHEMATIC TEMPLATE REV PA2 (November 30, 2011) DIALOG DOCUMENT NUMBER 31-902-03

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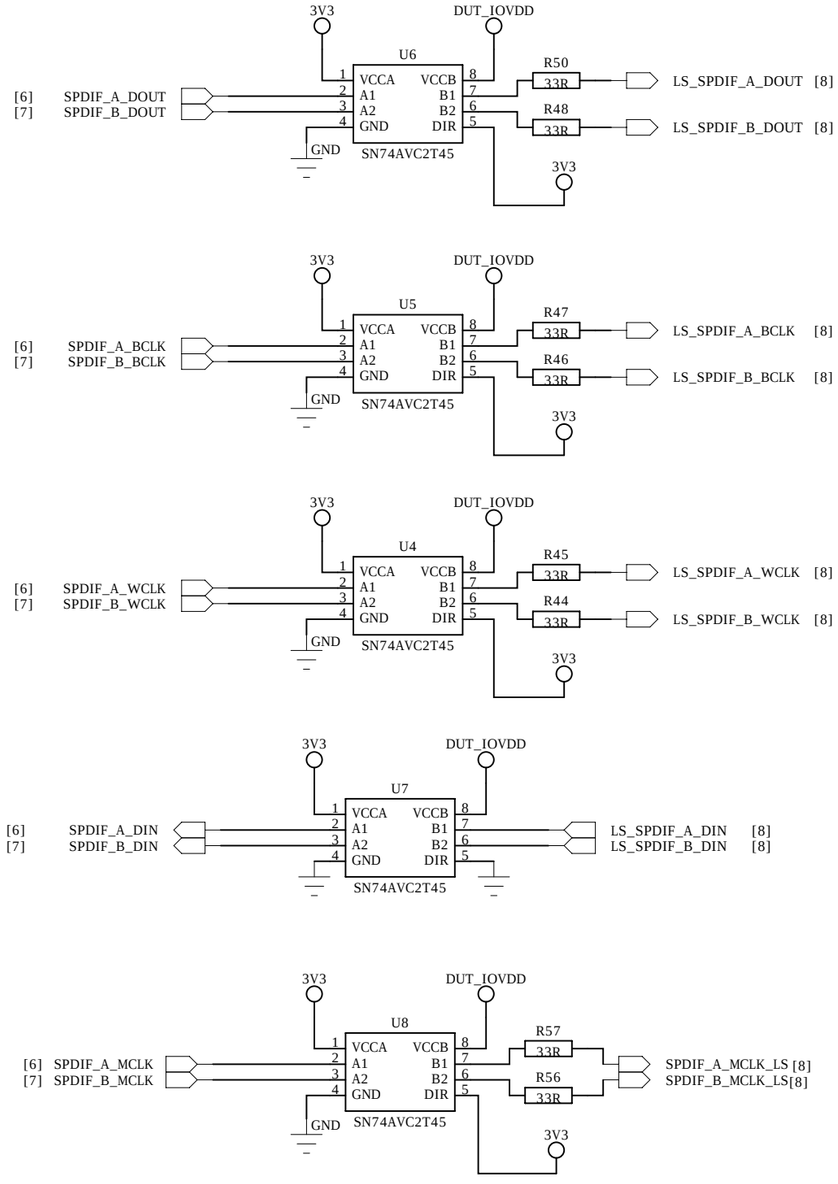
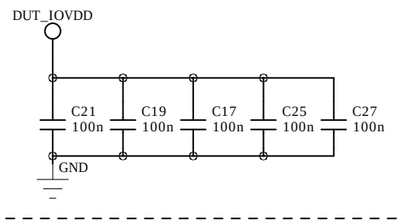
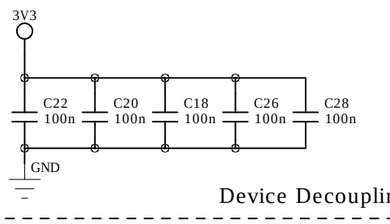
PREPARED: BL/BT	DATED: 23/04/2013	DRAWING NO: 44-179-170-01-B	REV: C
RESPONSIBLE: BT	DATED: 23/04/2013	SHEET NAME: S/PDIF_B	PAGE: 7 OF 16

dialog SEMICONDUCTOR

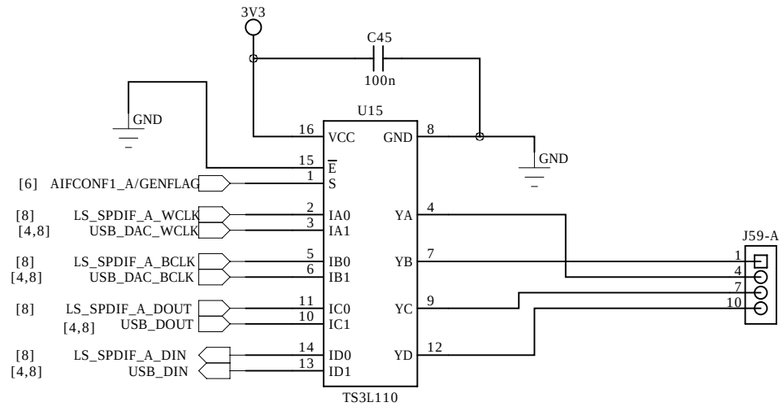


I2S VOLTAGE LEVEL TRANSLATION

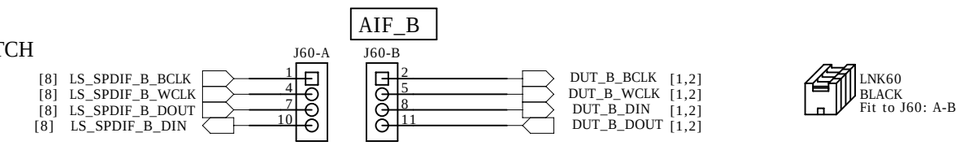


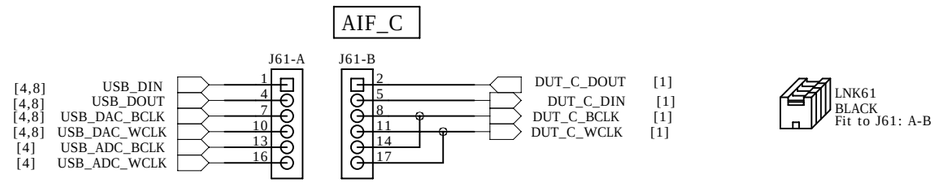


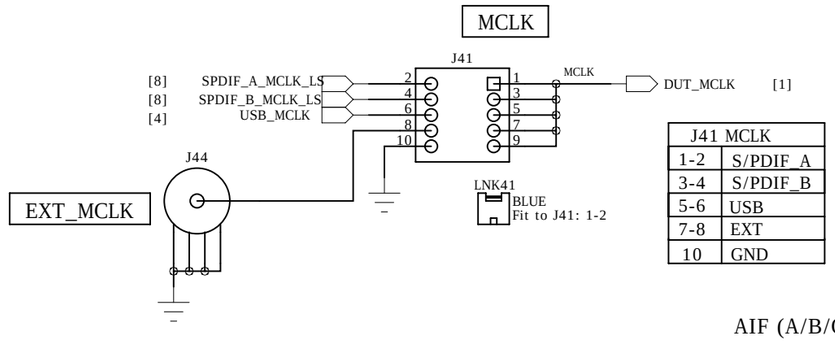
Device Decoupling



AIF_A SELECT SWITCH

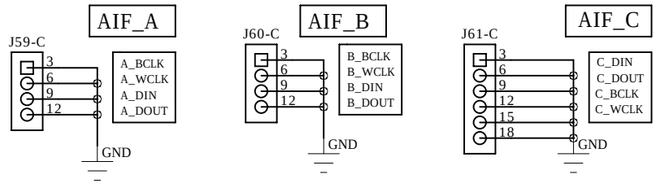






J41 MCLK	
1-2	S/PDIF_A
3-4	S/PDIF_B
5-6	USB
7-8	EXT
10	GND

AIF (A/B/C) / MCLK HEADERS



AIF Header GND Connections

SCHEMATIC TEMPLATE REV PA2 (November 30, 2011) DIALOG DOCUMENT NUMBER 31-902-03

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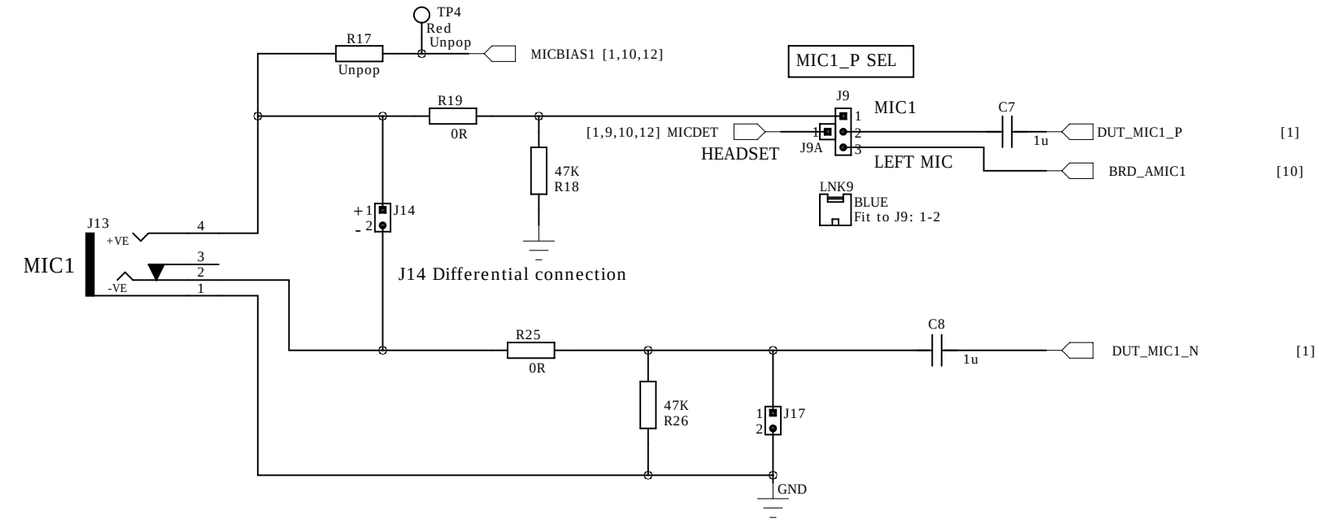
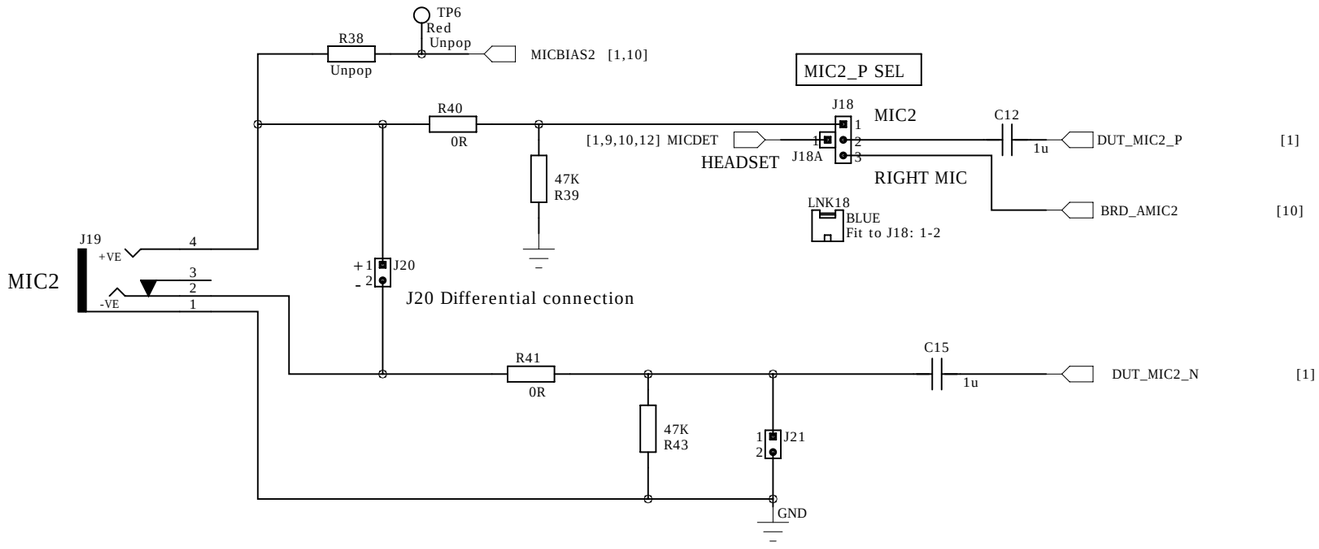
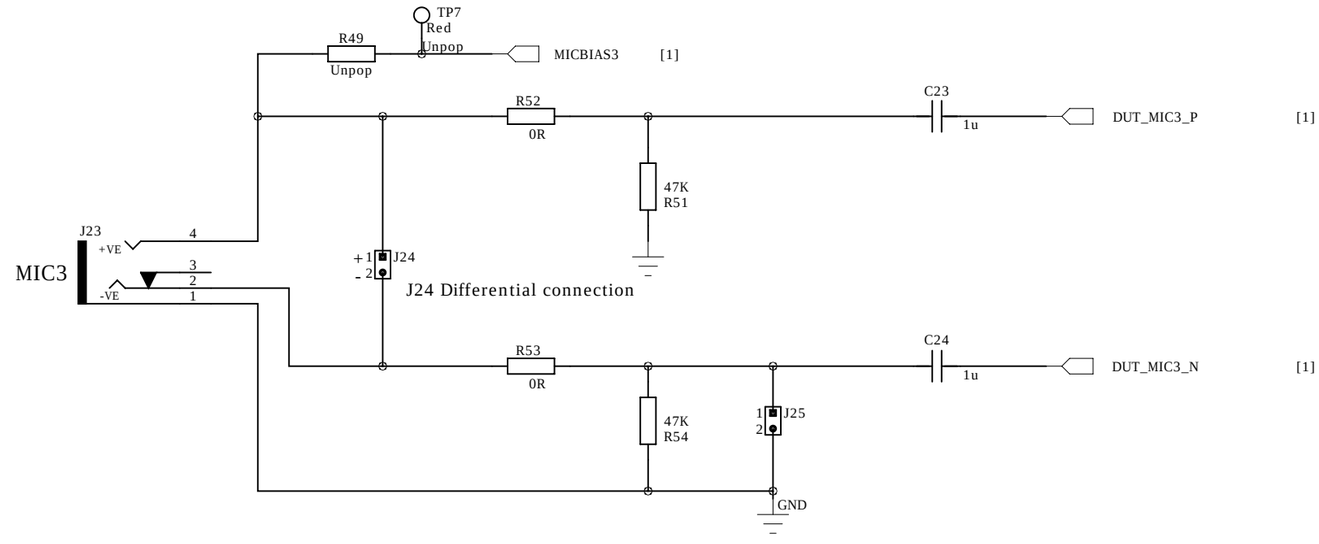
PREPARED: BL/BT	DATED: 23/04/2013	DRAWING NO: 44-179-170-01-B	REV: C
RESPONSIBLE: BT	DATED: 23/04/2013	SHEET NAME: I2S_LEVEL_SHIFT	PAGE: 8 OF 16







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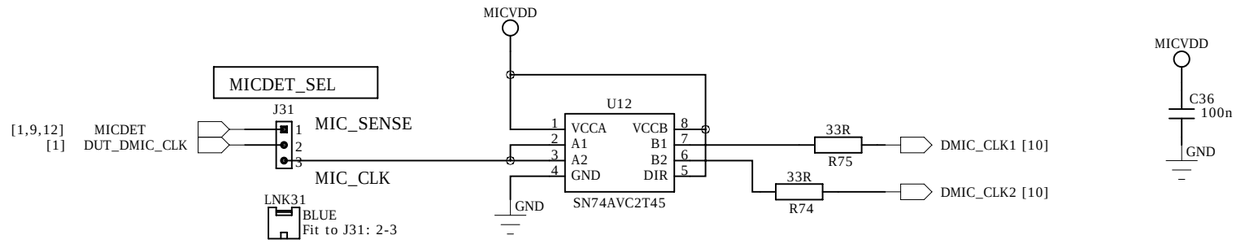
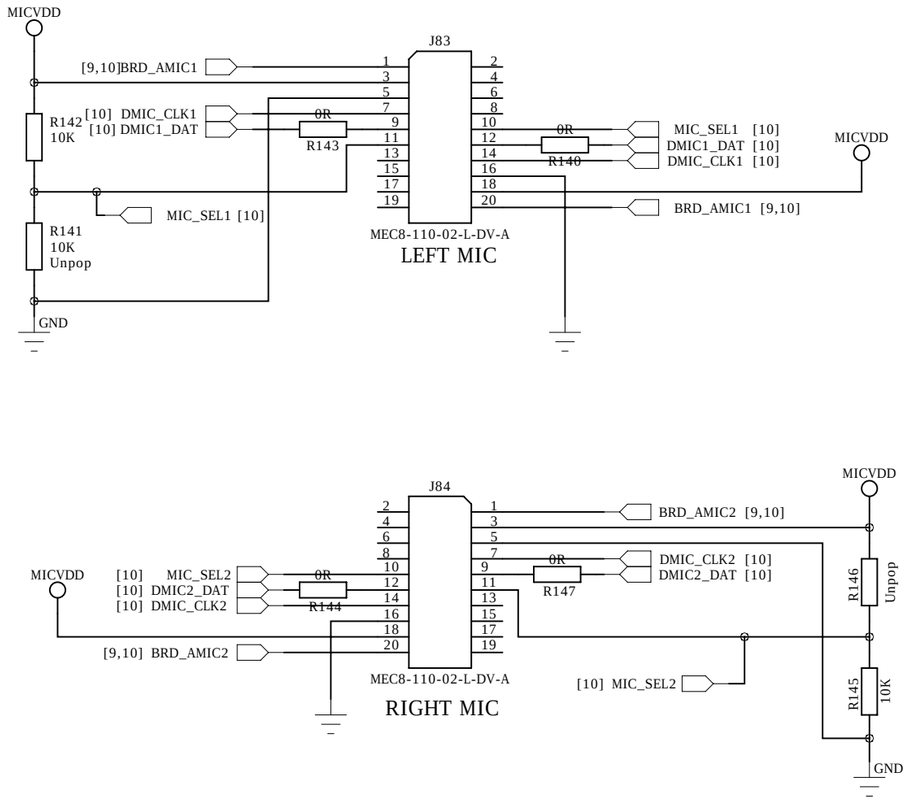
TITLE: AUDIO DSP PMIC CUSTOMER EVAL BOARD			
PREPARED: BL/BT	DATED: 23/04/2013	DRAWING NO: 44-179-170-01-B	REV: C
RESPONSIBLE: BT	DATED: 23/04/2013	SHEET NAME: MIC_INPUT	PAGE: 9 OF 16



J34	1-2	2-3
MICDET_SEL	ANALOGUE MIC SENSE	DIGI MIC CLK

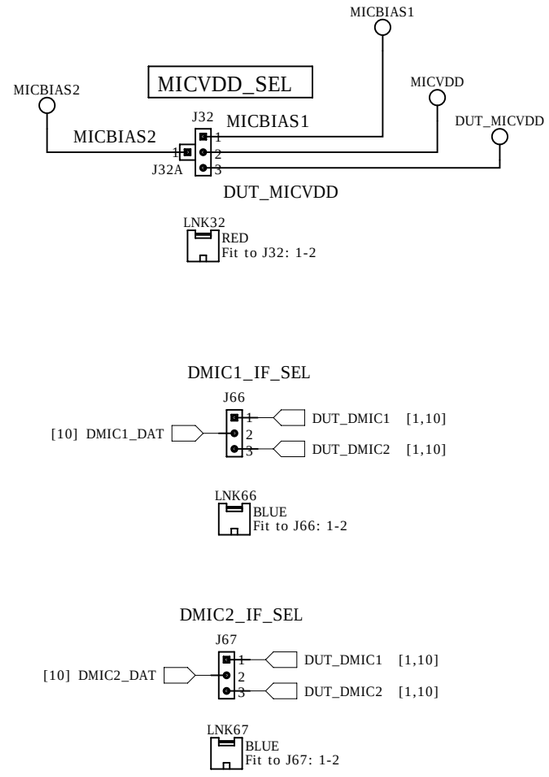
LAYOUT NOTE: PLACE BUFFER AS
CLOSE TO DUT HEADER AS POSSIBLE

MICDET FUNCTIONALITY SELECT



LAYOUT NOTES: PLACE AT CORNERS ON LONG EDGE OF BOARD
: LEAVE SPACE AROUND

ANALOGUE/DIGITAL MICROPHONE CONNECTORS



LAYOUT NOTE: PLACE JUMPER HEADERS AS
CLOSE TO DUT HEADER AS POSSIBLE

MIC CONNECTOR SELECT JUMPERS

SCHEMATIC TEMPLATE REV PA2 (November 30, 2011) DIALOG DOCUMENT NUMBER 31-902-03

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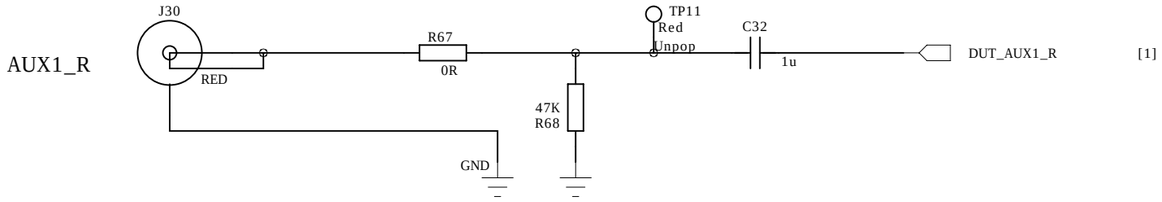
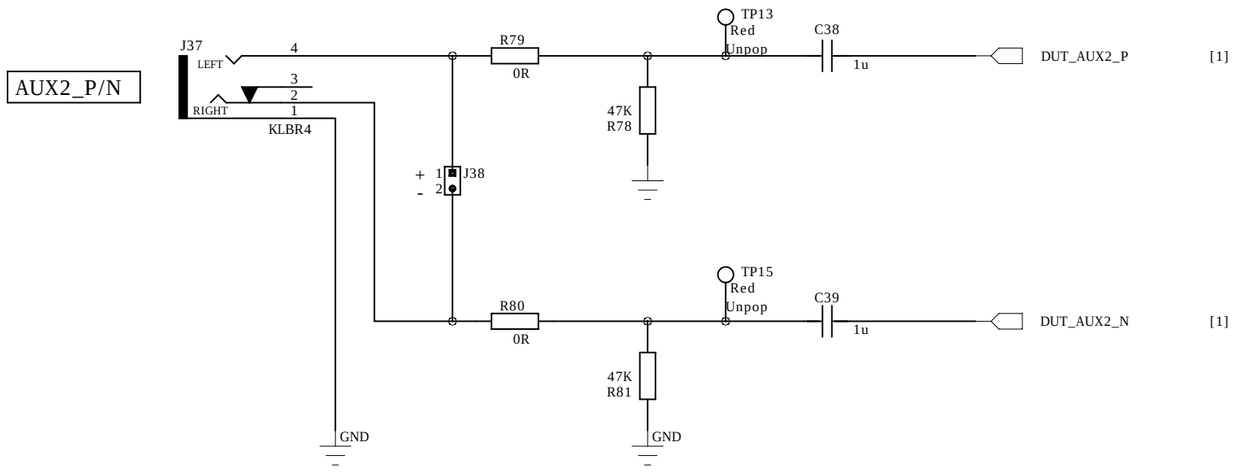
PREPARED:	DATED:	TITLE: AUDIO DSP PMIC CUSTOMER EVAL BOARD		
BL/BT	23/04/2013	DRAWING NO: 44-179-170-01-B	REV: C	dialog SEMICONDUCTOR
RESPONSIBLE: BT	DATED: 23/04/2013	SHEET NAME: MIC_CONNECTORS		PAGE: 10OF 16





SCHEMATIC TEMPLATE REV PA2 (November 30, 2011) DIALOG DOCUMENT NUMBER 31-902-03

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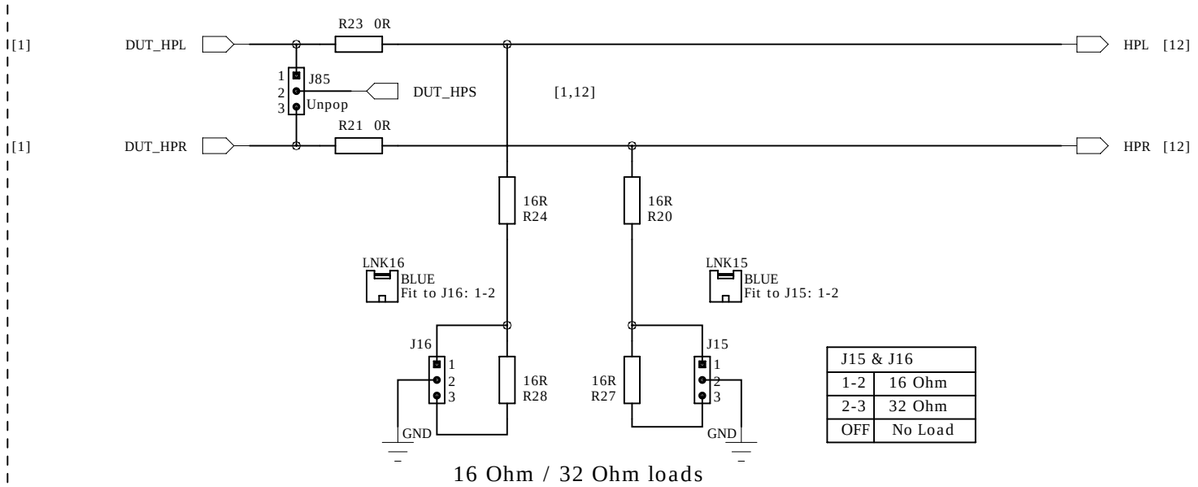
RESPONSIBLE: BT	DATED: 23/04/2013	SHEET NAME: AUX_INPUT	PAGE: 11OF 16



J15 & J16	
1-2	16 Ohm
2-3	32 Ohm
OFF	No Load

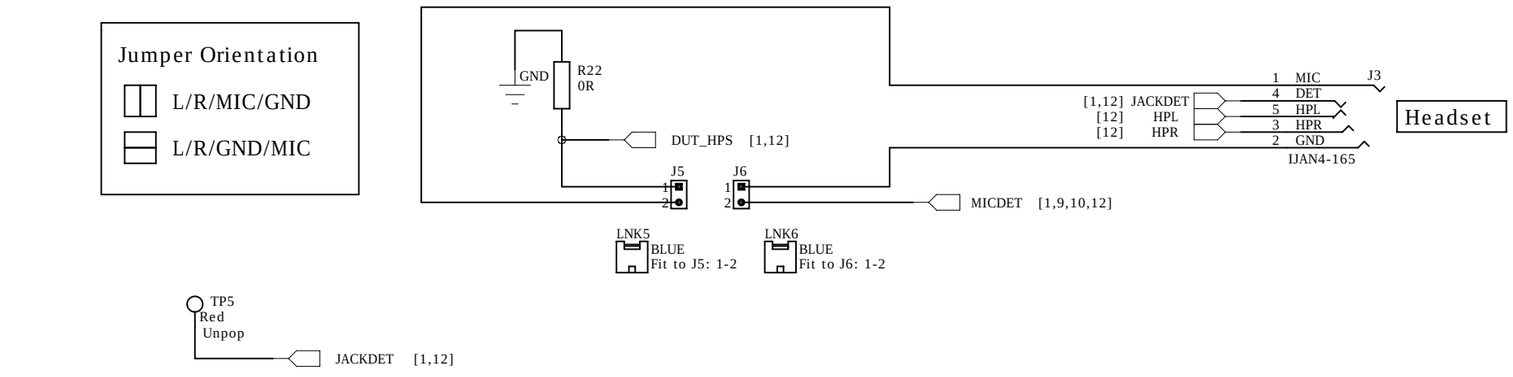
16 Ohm / 32 Ohm loads

HEADPHONE LOAD SELECT

Jumper Orientation

L/R/MIC/GND

L/R/GND/MIC



Layout Note:
Place J3 and J4 Adjacent

HEADSET OUTPUT / GND_MIC SELECT

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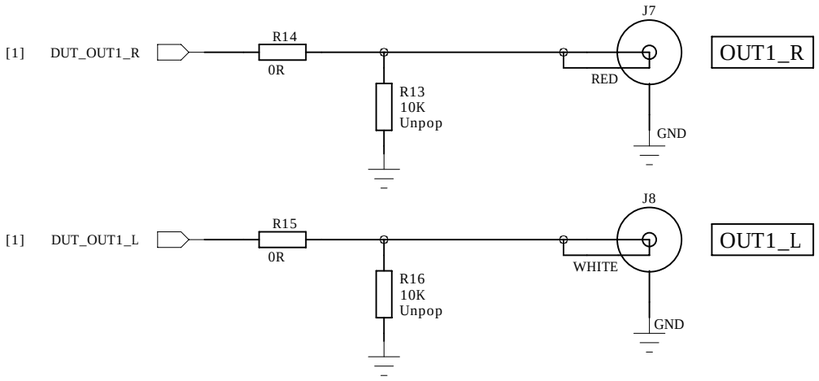
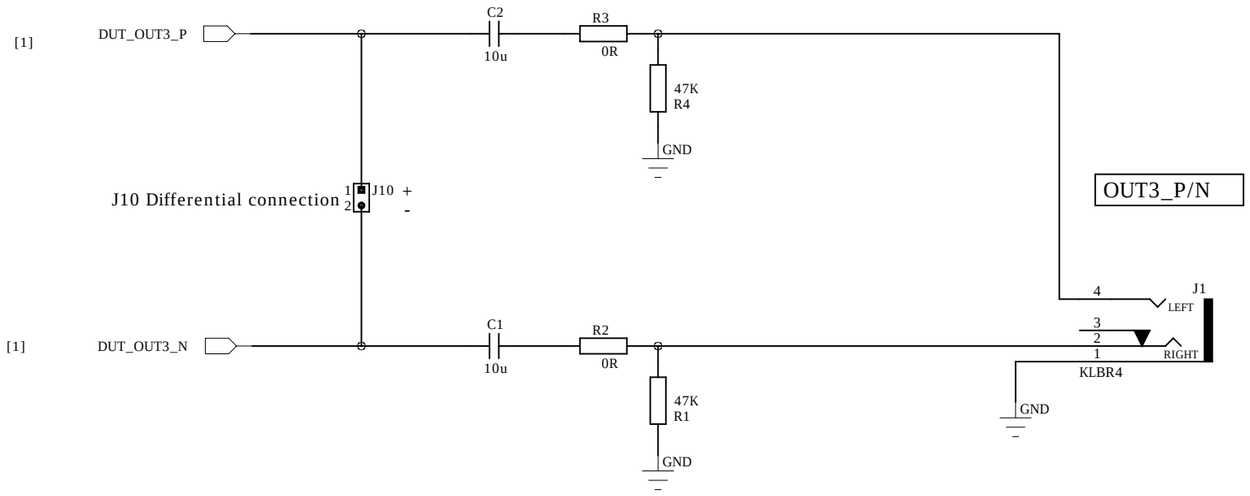
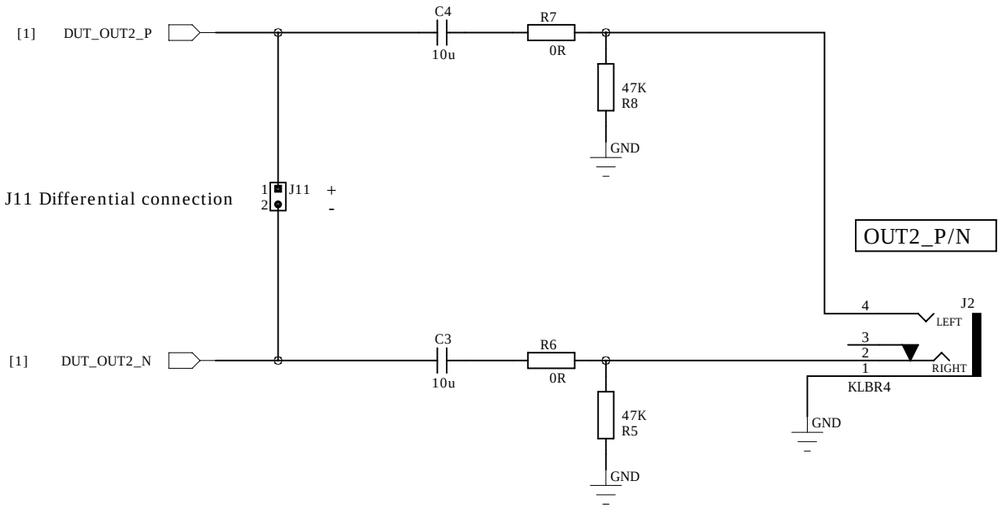
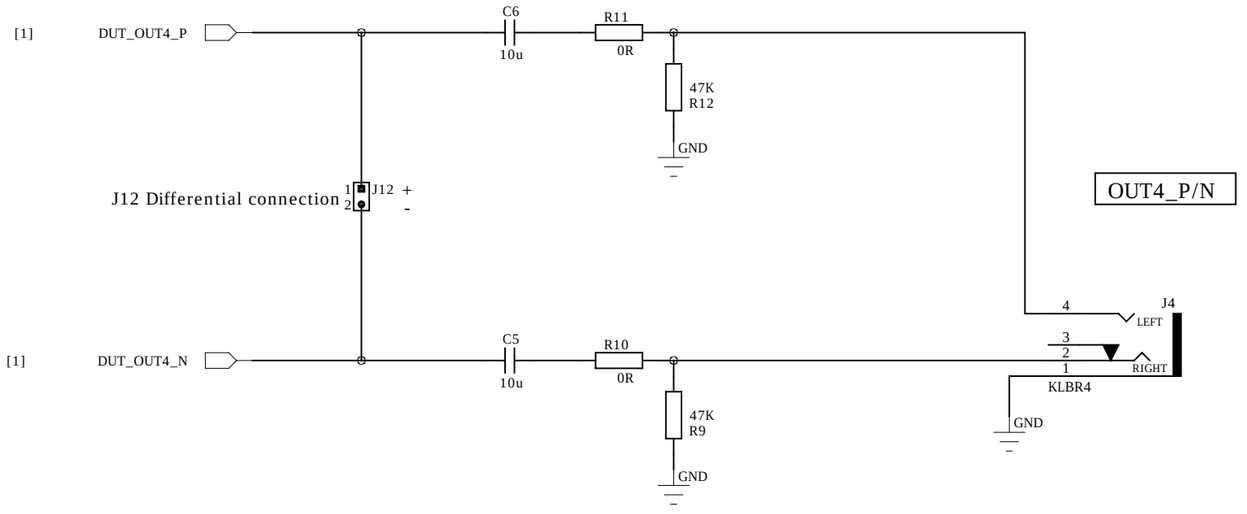
RESPONSIBLE: BT	DATED: 23/04/2013	SHEET NAME: HEADPHONE_HS	PAGE: 12OF 16









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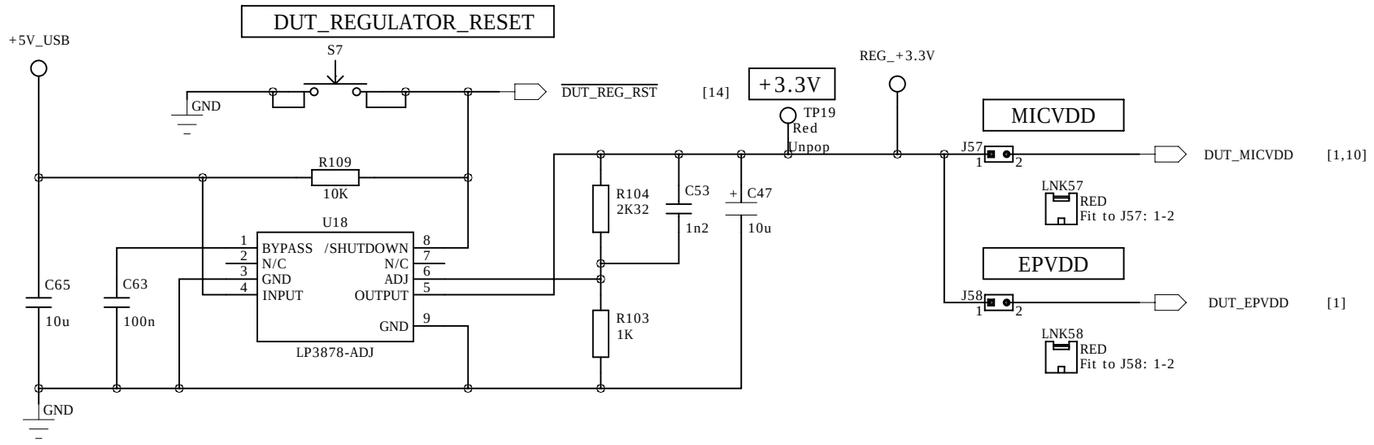
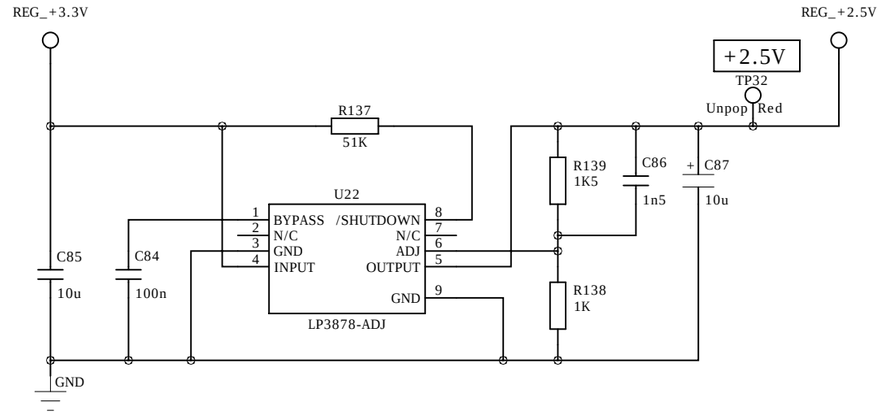
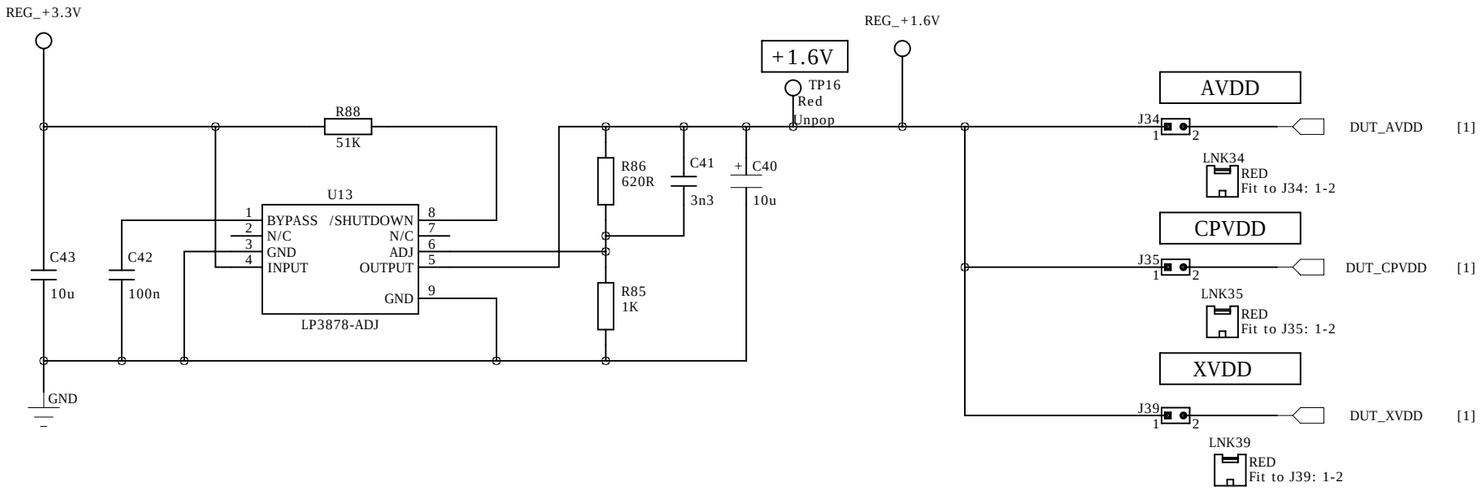
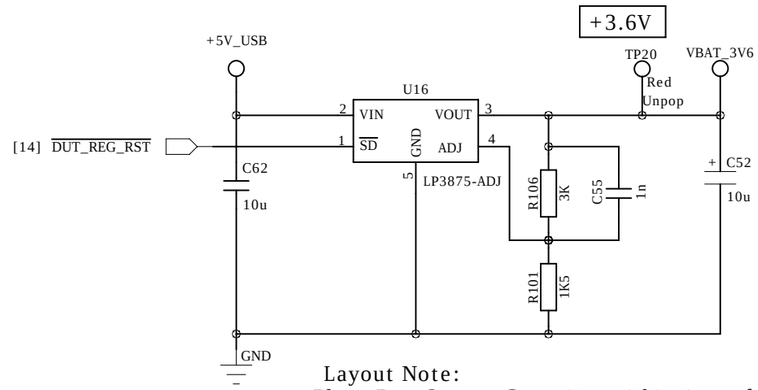
RESPONSIBLE: BT	DATED: 23/04/2013	SHEET NAME: LINE_OUTPUT	PAGE: 13 OF 16

dialog SEMICONDUCTOR



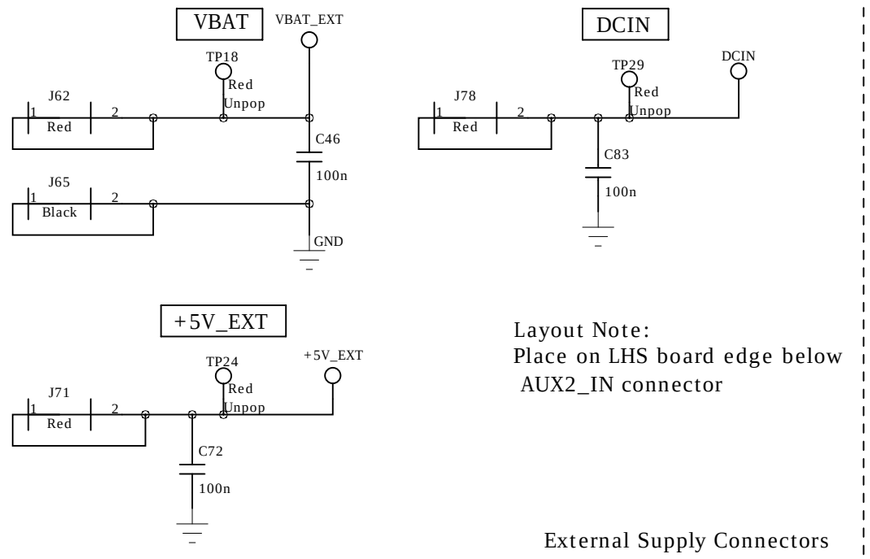






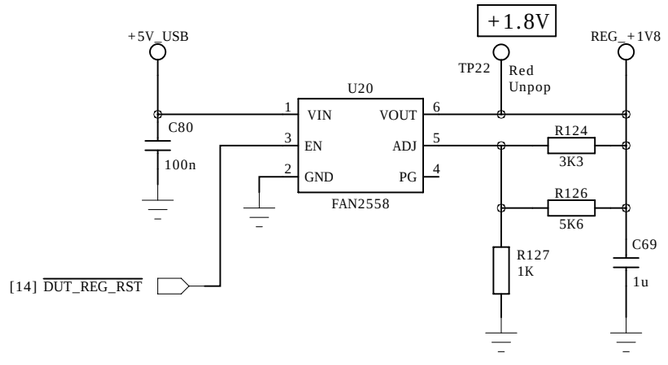
Layout Note:
Place Reg Output Capacitor within 1cm of Reg on traces directly to output and GND pins.

Design Note:
Output Cap (including any p//l connected caps) ESR must be between 0.1 and 10 Ohms



Layout Note:
Place on LHS board edge below AUX2_IN connector

External Supply Connectors

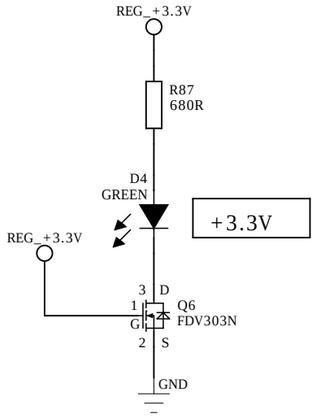


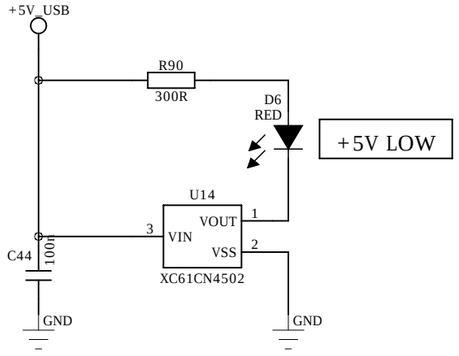
SCHEMATIC TEMPLATE REV PA2 (November 30, 2011) DIALOG DOCUMENT NUMBER 31-902-03

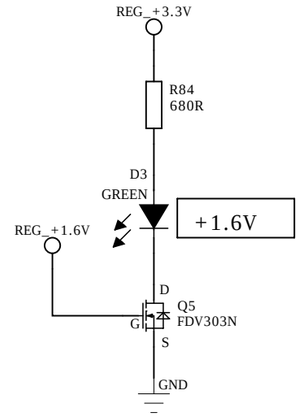
CONFIDENTIAL INFORMATION

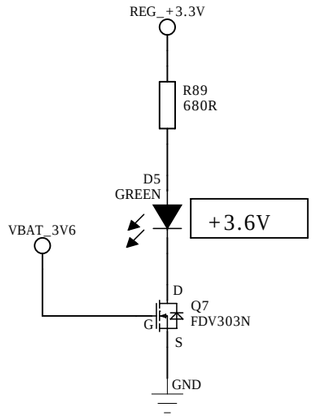
TITLE: AUDIO DSP PMIC CUSTOMER EVAL BOARD			
PREPARED: BL/BT	DATED: 23/04/2013	DRAWING NO: 44-179-170-01-B	REV: C
RESPONSIBLE: BT	DATED: 23/04/2013	SHEET NAME: POWER_SUPPLY	PAGE: 14OF 16

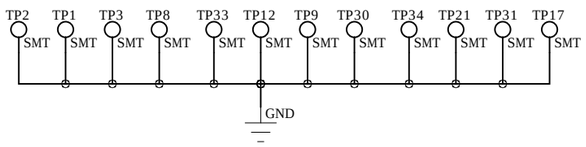
LAYOUT NOTE: ALIGN LEDS IN ROW











LAYOUT NOTE: SPREAD GND CONNECTORS EVENLY THROUGHOUT BOARD

SCHEMATIC TEMPLATE REV PA2 (November 30, 2011) DIALOG DOCUMENT NUMBER 31-902-03

CONFIDENTIAL INFORMATION

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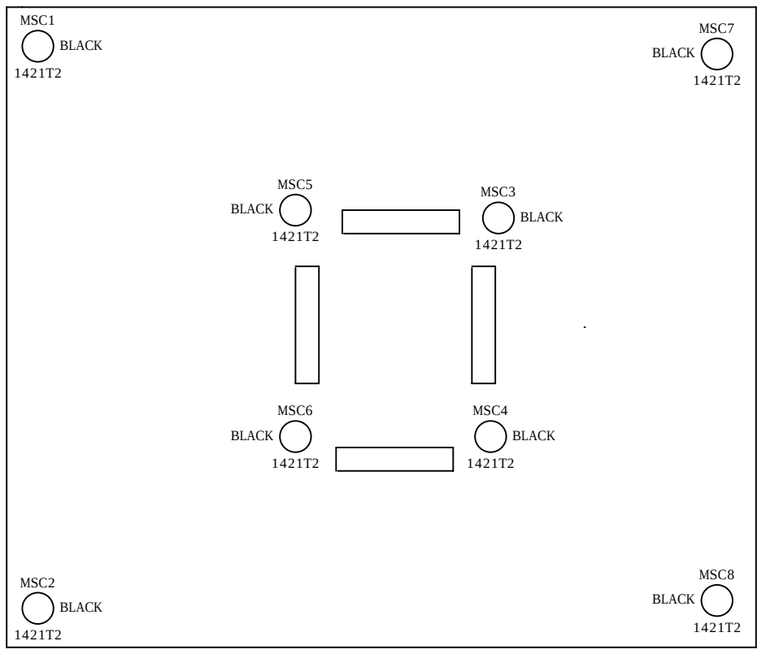
PREPARED: BL/BT	DATED: 23/04/2013	DRAWING NO: 44-179-170-01-B	REV: C
RESPONSIBLE: BT	DATED: 23/04/2013	SHEET NAME: POWER_LEDS	PAGE: 15OF 16

REV	DATE	ENGINEER	NOTES
C	28/03/2013	BL/BT	J85 (unpop 1x3 header) added.



Leave at least 20mm spacing around daughter-board header connectors
Rubber Feet in corners, four close to centre of the board
The diagram shows a suggested placement of the interfaces to this evaluation board

CONFIDENTIAL INFORMATION

		TITLE: AUDIO DSP PMIC CUSTOMER EVAL BOARD		dialog SEMICONDUCTOR
PREPARED: BL/BT	DATED: 23/04/2013	DRAWING NO: 44-179-170-01-B	REV: C	
RESPONSIBLE: BT	DATED: 23/04/2013	SHEET NAME: REVISION		PAGE: 16 OF 16