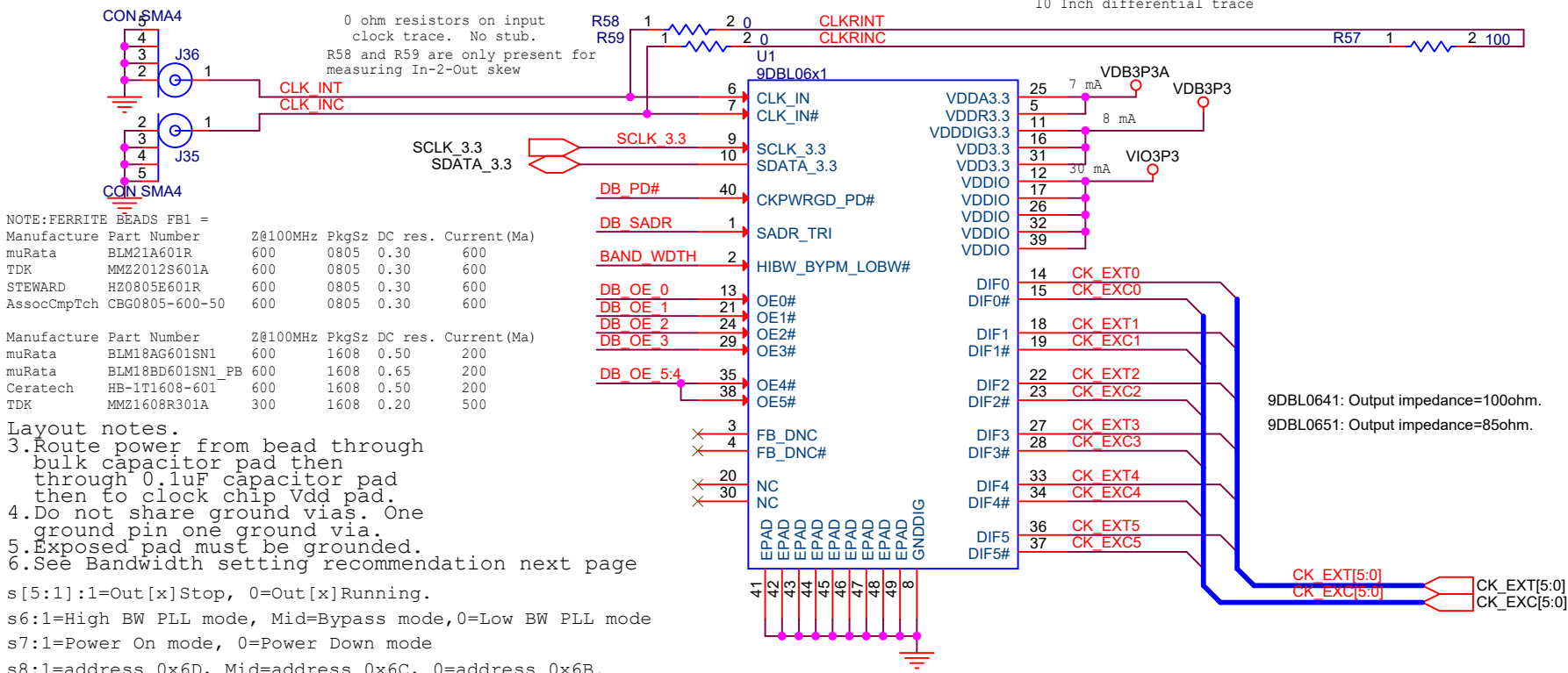




NOTE:FERRITE BEADS FB1 =

Manufacture	Part Number	Z@100MHz	PkgSz	DC res.	Current (Ma)
muRata	BLM21A601R	600	0805	0.30	600
TDK	MMZ2012S601A	600	0805	0.30	600
STEWART	HZ0805E601R	600	0805	0.30	600
AssocCmpTch	CBG0805-600-50	600	0805	0.30	600

Manufacture	Part Number	Z@100MHz	PkgSz	DC res.	Current (Ma)
muRata	BLM18AG601SN1	600	1608	0.50	200
muRata	BLM18BD601SN1_PB	600	1608	0.65	200
Ceratech	HB-1T1608-601	600	1608	0.50	200
TDK	MMZ1608R301A	300	1608	0.20	500

Layout notes.

3.Route power from bead through bulk capacitor pad then through 0.1uF capacitor pad then to clock chip Vdd pad.

4.Do not share ground vias. One ground pin one ground via.

5.Exposed pad must be grounded.

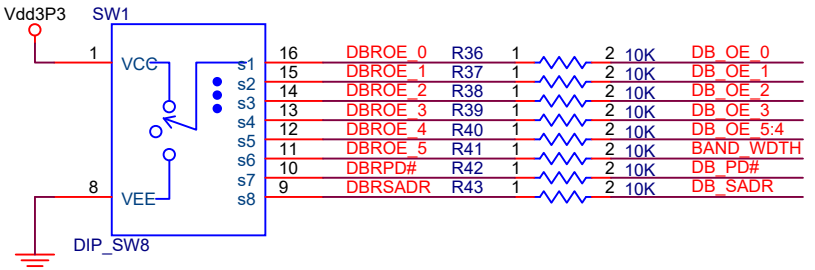
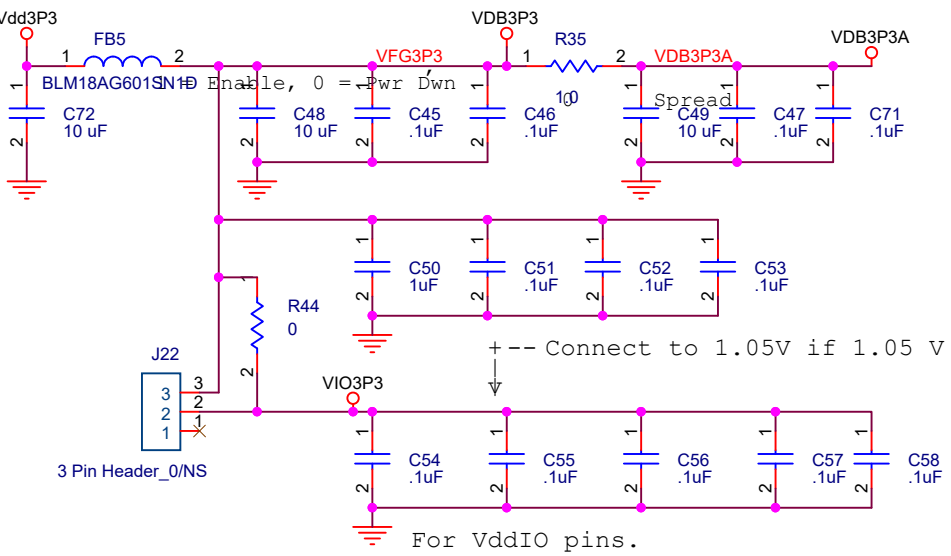
6.See Bandwidth setting recommendation next page

s[5:1]:1=Out[x]Stop, 0=Out[x]Running.

s6:1=High BW PLL mode, Mid=Bypass mode,0=Low BW PLL mode

s7:1=Power On mode, 0=Power Down mode

s8:1=address 0x6D, Mid=address 0x6C, 0=address 0x6B.



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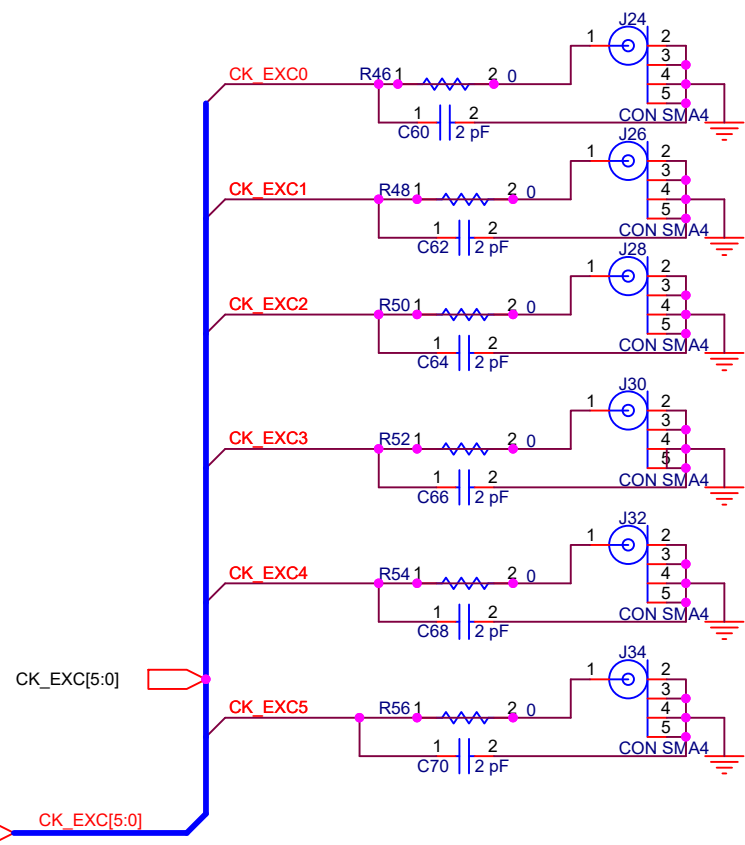
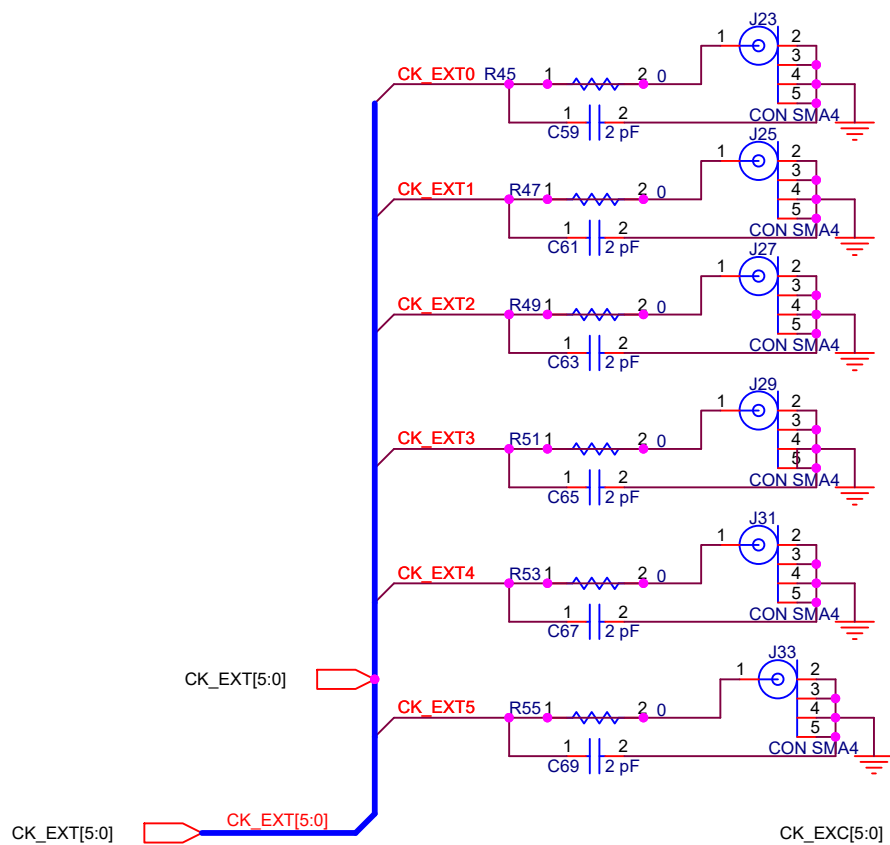
Title

9DBL0641 Reference Schematic.

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Bandwidth setting

1. If the ZDB is on an Add-In-Card (AIC) use PLL bypass mode.
2. If it is motherboard down and it is providing clocks to all PCIe devices including the Root Complex use High Bandwidth.

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