Smart Configurator for RZ V1.19.0

Release Note

Introduction

Thank you for using the Smart Configurator for RZ.

This document describes the restrictions and points for caution. Read this document before using the product.

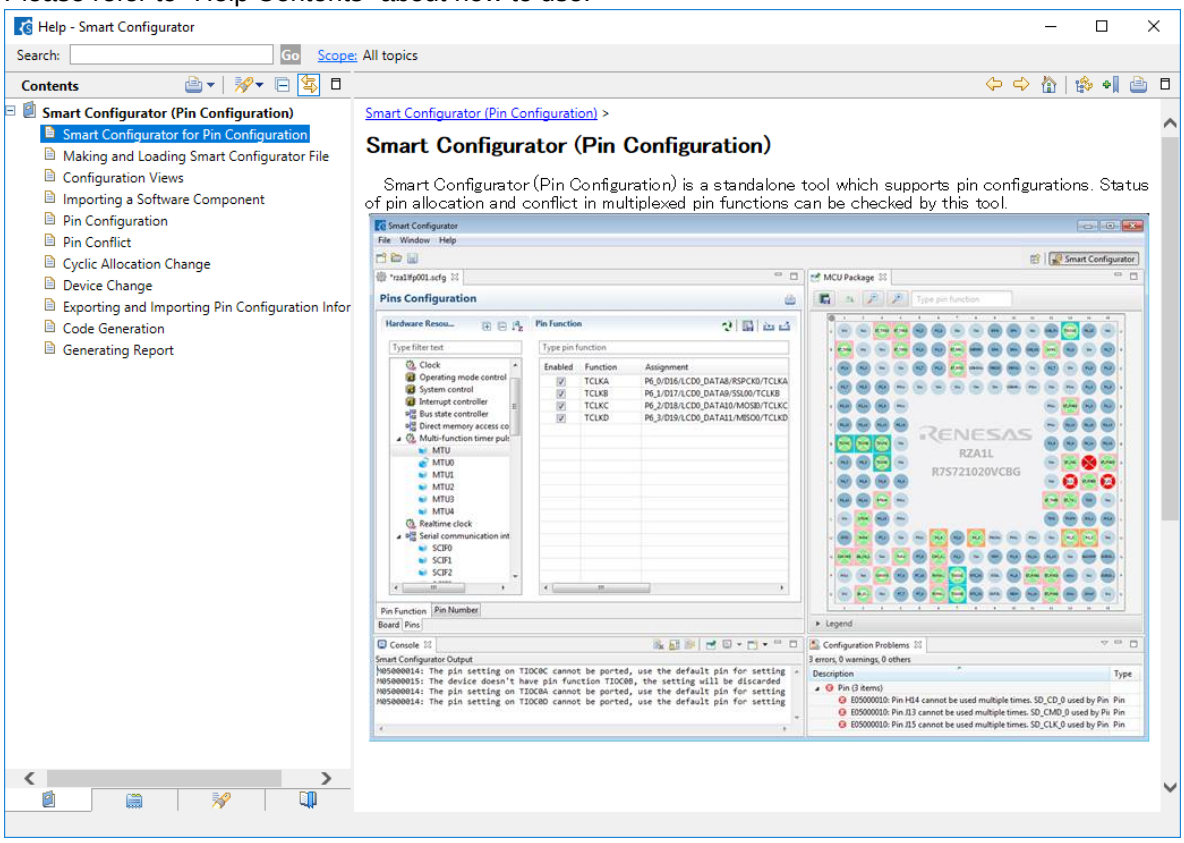
Contents

1. Introduction 2
1.1 System Requirements 2
1.1.1 PC 2
2. Support List 3
2.1 Supported Devices List 3
2.2 New Support 8
2.2.1 Add support for new device package RZ/V2N 8
3. Changes 9
3.1.1 Correction of name of macro in RZ/T2H and RZ/N2H 9
4. List of [Notes] RENESAS TOOL NEWS 10
5. Points for Limitation 11
6. Point for Caution 12
6.1 List of Caution 12
6.2 Details of Caution 12
6.2.1 Functions not supported by RZ/A1 package 12
6.2.2 Projects created using Smart Configurator for RZ V1.3.0 and before 12
Revision History 13

1. Introduction

The Smart Configurator for RZ is a standalone GUI-based tool for setting the assignments of pin functions to pins in the design of hardware specifications. The assignments of pins can be set up from a GUI, which also checks and offers solutions for cases of contention for the same pins by multiplexed functions.

Please refer to "Help Contents" about how to use.



1.1 System Requirements

The operating environment is as follows:

1.1.1 PC

- IBM PC/AT compatibles (Windows® 11, Windows® 10 64-bit)
- Processor: 1 GHz or higher (must support hyper-threading, multi-core CPUs)
- Memory capacity: 2 GB or more recommended.
- Hard disk capacity: 300 MB or more spare capacity
- Display: 1024 x 768 or higher resolution, 65,536 or more colors
- All other necessary software environments in addition to Windows OS
  - Java Runtime Environment

Please note that from V1.11.0, Smart Configurator for RZ will be released as a 64-bit product build. The switch to 64-bit means that it is no longer possible to run this version of the tool on Windows 10 32-bit versions.

2. Support List

2.1 Supported Devices List

Below is a list of devices supported by the Smart Configurator for RZ V1.19.0.

Table 1. Supported Devices

RZ/A1L group	
PIN	Device name
176pin	R7S721020VCBG, R7S721020VCFP, R7S721020VLFP
208pin	R7S721021VCFP, R7S721021VLFP
RZ/A1LU group	
PIN	Device name
176pin	R7S721030VCBG, R7S721030VCFP, R7S721030VLFP
208pin	R7S721031VCFP, R7S721031VLFP
233pin	R7S721031VCBG, R7S722031VLBG
RZ/A1LC group	
PIN	Device name
176pin	R7S721034VCBG
Following documents.	
Manual Name	Document Number
RZ/A1L, RZ/A1LU, RZ/A1LC Group User's Manual: Hardware	R01UH0437EJ0300

RZ/A1H group	
PIN	Device name
256pin	R7S721000VCBG, R7S721000VCFP, R7S721000VLFP
324pin	R7S721001VCBG, R7S721001VLBG
RZ/A1M group	
PIN	Device name
256pin	R7S721010VCBG, R7S721010VCFP, R7S721010VLFP
324pin	R7S721011VCBG, R7S721011VLBG
Following documents.	
Manual Name	Document Number
RZ/A1H, RZ/A1M Group User's Manual: Hardware	R01UH0403EJ0200

RZ/G1M group	
PIN	Device name
831pin	R8A77430
Following documents	
Manual name	Document Number
RZ/G1M User's Manual: Hardware	R01UH0626EJ0100

RZ/G1E group	
PIN	Device name
501pin	R8A77450
Following documents	
Manual name	Document Number
RZ/G1E User's Manual: Hardware	R01UH0544EJ0100

RZ/G1H group	
PIN	Device name
831pin	R8A77420
Following documents	
Manual name	Document Number
RZ/G1H User's Manual: Hardware	R01UH0627EJ0100

RZ/G1N group	
PIN	Device name
831pin	R8A77440
Following documents	
Manual name	Document Number
RZ/G1N User's Manual: Hardware	R01UH0628EJ0100

RZ/G2E group	
PIN	Device name
552pin	R8A774C0
Following documents	
Manual name	Document Number
RZ/G2E User's Manual: Hardware	R01UH0848EJ0080

RZ/G2M group	
PIN	Device name
1022pin	R8A774A0
Following documents	
Manual name	Document Number
RZ/G2M User's Manual: Hardware	R01UH0846EJ0080

RZ/G2N group	
PIN	Device name
1022pin	R8A774B0
Following documents	
Manual name	Document Number
RZ/G2N User's Manual: Hardware	R01UH0847EJ0080

RZ/G2H group	
PIN	Device name
1022pin	R8A774E0
Following documents	
Manual name	Document Number
RZ/G Series, 2nd Generation User's Manual: Hardware	R01UH0808EJ0100

RZ/G2L, G2LC group	
PIN	Device name
456pin 551pin 361pin	R9A07G044L (15mm) R9A07G044L (21mm) R9A07G044LC
Following documents	
Manual name	Document Number
RZ/G Series, 2nd Generation User's Manual: Hardware	R01UH0914EJ0041

RZ/V2L group	
PIN	Device name
456pin 551pin	R9A07G054L (15mm) R9A07G054L (21mm)
Following documents	
Manual name	Document Number
RZ/V2L Group User's Manual: Hardware	R01UH0914EJ0041 R01UH0936EJ0040

RZ/G2UL group	
PIN	Device name
361pin	R9A07G043U
Following documents	
Manual name	Document Number
RZ/G2UL Group User's Manual: Hardware	R01UH0968EJ0050

RZ/Five group	
PIN	Device name
266pin 361pin	R9A07G043F00GBG R9A07G043F01GBG
Following documents	
Manual name	Document Number
RZ/Five Group User's Manual: Hardware	R01UH0986EJ0050

RZ/G3S group	
PIN	Device name
359pin 361pin	R9A08G045S (14mm) R9A08G045S (13mm)
Following documents	
Manual name	Document Number
RZ/G3S Group User's Manual: Hardware	R01UH1014EJ0100

RZ/V2H group	
PIN	Device name
1369pin	R9A09G057H
Following documents	
Manual name	Document Number
RZ/V2H Group User's Manual: Hardware	R01UH1015EJ0050

RZ/T2H and RZ/N2H group	
PIN	Device name
576pin	R9A09G087M (RZ/N2H)
729pin	R9A09G077M (RZ/T2H)
Following documents	
Manual name	Document Number
RZ/T2H and RZ/N2H Group User's Manual: Hardware	R01UH1039EJ0041

RZ/V2N group	
PIN	Device name
1368pin	R9A09G056N (RZ/V2N)
Following documents	
Manual name	Document Number
RZ/V2N Group User's Manual: Hardware	R01UH1072EJ0050

2.2 New Support

2.2.1 Add support for new device package RZ/V2N

Smart Configurator for RZ now supports new device package R9A09G056N from the RZ/V2N device group.

3. Changes

3.1.1 Correction of name of macro in RZ/T2H and RZ/N2H

In the generated DTSI file “r9a09g0_pinconf.dtsi” of RZ/T2H and RZ/N2H, the macro **RZG2L**_PORT_PINMUX has been renamed to **RZT2H**_PORT_PINMUX.

This change was made to ensure the macro definition matches the definition in the Verified Linux Package (VLP) supporting RZ/T2H and RZ/N2H.

4. List of [Notes] RENESAS TOOL NEWS

[Notes] Below is a list of notifications delivered by RENESAS TOOL NEWS.

Issue date	Document No.	Description	Applicable MCUs	Fixed version
2019/12/16	R20TS0520	Incorrect display of peripheral function names "Camera Serial Interface" and "SPI Multi I/O Bus Controller" on pin function tab	RZ/G2E	V1.8.0
2021/7/16	R20TS0739	Missing pins for I2C0, I2C3 and I2C5 of RZ/G2M	RZ/G2M	V1.10.1

5. Points for Limitation

There are no limitations for Smart Configurator for RZ V1.19.0.

6. Point for Caution

This chapter describes the cautions for Smart Configurator for RZ V1.19.0.

6.1 List of Caution

No.	Descriptions	RZ/A1	RZ/G1	RZ/G2	RZ/V2
1	Functions not supported by RZ/A1 package	✓	-	-	-
2	Projects created using Smart Configurator for RZ V1.3.0 and before	-	✓	-	-

✓:Applicable, -:Not Applicable

6.2 Details of Caution

6.2.1 Functions not supported by RZ/A1 package

RZ/A1 package does not support code generation and board configuration.

[Target]

RZ/A1H, A1L, A1LC, A1LU, A1M

6.2.2 Projects created using Smart Configurator for RZ V1.3.0 and before

Projects created using Smart Configurator for RZ V1.3.0 and before do not have [Group] information. Please confirm [Group] after opening those projects.

[Workaround]

None.

[Target]

RZ/G1C, G1E, G1H, G1M, G1N

Revision History

Rev.	Section	Description
1.00	-	First edition issued
		-

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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