CS+ Cycle Accurate Simulator for RH850/C1x V1.04.00

Release Note

R20UT4949EJ0100
Rev.1.00
Dec 02, 2020

Thank you for using the CS+ cycle-accurate simulator for RH850/C1x devices.

This document describes restrictions on and points for caution regarding the simulator.

Read this document before using the product.

Contents

1. Introduction

This chapter describes the devices supported by this product and the related user's manuals.

1.1 Supported Devices

- RH850/C1H (R7F701270)
- RH850/C1M-A2 (R7F701275)
- RH850/C1M-A1 (R7F701278)

1.2 Provided Materials

We provide the following executable file and license key to enable use of the CS+ cycle-accurate simulators for RH850/C1x V1.04.00.

- **CSPlus_Cycle_accurate_simulator_for_RH850_C1x__V10400.exe**

  This is an executable file to install information for cycle accuracy when running the instruction simulators of the RH850/C1H (R7F701270), RH850/C1M-A2 (R7F701275), and RH850/C1M-A1 (R7F701278) as cycle-accurate simulators within CS+ V8.05.00.

- **License Key for Evaluation**

  This license key is node-locked and has an expiry period of one year or three-month.

1.3 User's Manuals

Refer to the following user's manuals for details on the operation of CS+, including the cycle-accurate simulators.

Manual Name	Document Number
CS+ V8.02.00 Integrated Development Environment User's Manual: Installer	R20UT4525EJ0100
CS+ V8.05.00 Integrated Development Environment User's Manual: Message	R20UT4855EJ0100
CS+ V8.05.00 Integrated Development Environment User's Manual: Project Operation	R20UT4856EJ0100
CS+ Integrated Development Environment User's Manual: CC-RH Build Tool Operation	R20UT3283EJ0108
CS+ V8.05.00 Integrated Development Environment User's Manual: GHS CCRH850 Build Tool Operation	R20UT4853EJ0100
CS+ V8.05.00 Integrated Development Environment User's Manual: RH850 Debug Tool	R20UT4858EJ0100
CS+ V8.05.00 Integrated Development Environment User's Manual: Python Console	R20UT4854EJ0100
License Manager V2.04.00 User's Manual	R20UT4888EJ0100

* GHS: Green Hills Software, LLC

2. Features of the Cycle-Accurate Simulators

This chapter describes the major features and specifications of the cycle-accurate simulators for RH850/C1x products.

2.1 Access Latency

Since the operation of the CPU is simulated in consideration of the latencies of the RH850/C1H (R7F701270), RH850/C1M-A2 (R7F701275), and RH850/C1M-A1 (R7F701278) during access to various types of memory, the results of measuring the following items differ according to whether a cycle-accurate simulator or an instruction simulator is in use.

- The results of measurement by the Run-Break timer
- The results of measurement of Timer Result events
- The [Pipeline] area of the Trace panel
- The [Time (clock)] area of the Trace panel
- Result of tracing when the trace target is selected as [All core] (timing between processor elements).
- Timestamps of the software trace data.

2.2 Peripheral Functions

You can simulate the basic operations of the following peripheral functions.

- Interrupt controller (INTC1/INTC2)
- Inter-processor interrupt (IPIR)
- Exclusive Control Register (MEV)
- OS timer (Interval timer mode)

The value of [Main clock frequency [MHz]] on the [Connect Settings] tabbed page in the Property of the simulator is used as the clock frequency for the OS timer when an OS timer function (interval timer mode) is to be simulated.

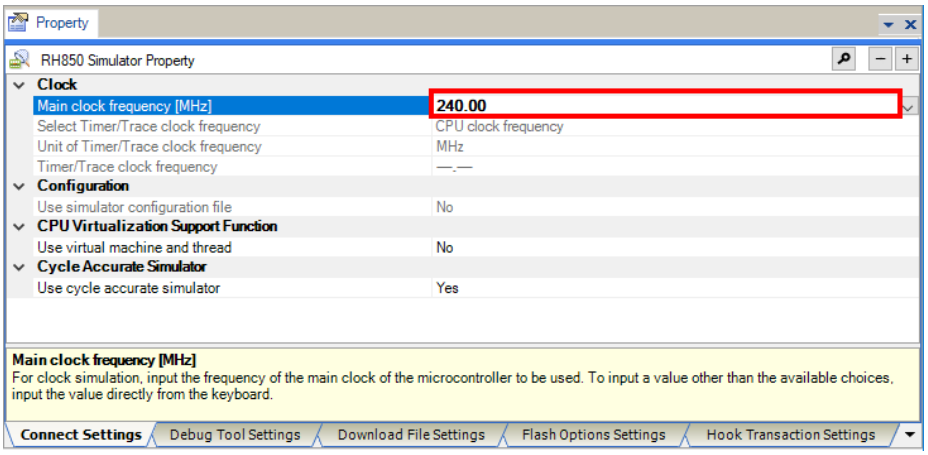


Figure 2-1 Setting the Main Clock Frequency

2.3 Pseudo-Interrupts

You can generate pseudo-interrupts with the following Python functions. For details, refer to the CS+ V8.05.00 Integrated Development Environment User's Manual: Python Console.

- debugger.Interrupt.OccurEI
- debugger.Interrupt.OccurFE

2.4 CPU Operating Clock

RH850/C1H (R7F701270):

The CPU operating clock runs at 240 MHz.

RH850/C1M-A2 (R7F701275):

The CPU operating clock runs at 320 MHz.

RH850/C1M-A1 (R7F701278):

The CPU operating clock runs at 240 MHz.

2.5 Supported Compilers

Files in executable form from the following compilers can be simulated.

- RH850 compilers from Renesas
- RH850 compilers from GHS

CS+ V8.05.00 supports the following versions of the GHS compiler.
2020.5.5, 2020.1.5, 2019.5.5, 2019.1.5, 2018.5.5, 2018.1.5, 2017.5.5, 2017.1.5, 2016.5.5, 2015.1.7, 2015.1.5, 2014.1.7, 2013.5.5, 2013.1.5, and 2012.5.5

3. Installing the Simulators

This chapter describes how to install the cycle-accurate simulators for RH850/C1x products.
Install the CS+ V8.05.00 and the cycle-accuracy information files for RH850/C1x products respectively as described below.

3.1 Installing CS+ V8.05.00

From our web site, download and install CS+ for CC V8.05.00 [Evaluation Software].

https://www.renesas.com/support/document-search?title=CS+%20for%20CC&doc_file_all_types%5BEvaluation+Software%5D=Evaluation+Software

3.2 Installing the Information Files for Cycle Accuracy

Activate the provided “CSPlus_Cycle_accurate_simulator_for_RH850_C1x__V10400.exe” to install the information files for cycle accuracy of RH850/C1x products.

After installation, the [Use cycle accurate simulator] property can be displayed from the [Cycle Accurate Simulator] category of the [Connect Settings] tabbed page under the properties of the RH850 simulator, when the RH850/C1H (R7F701270), RH850/C1M-A2 (R7F701275) or RH850/C1M-A1 (R7F701278) is selected as the target device for creating a project with CS+ V8.05.00.

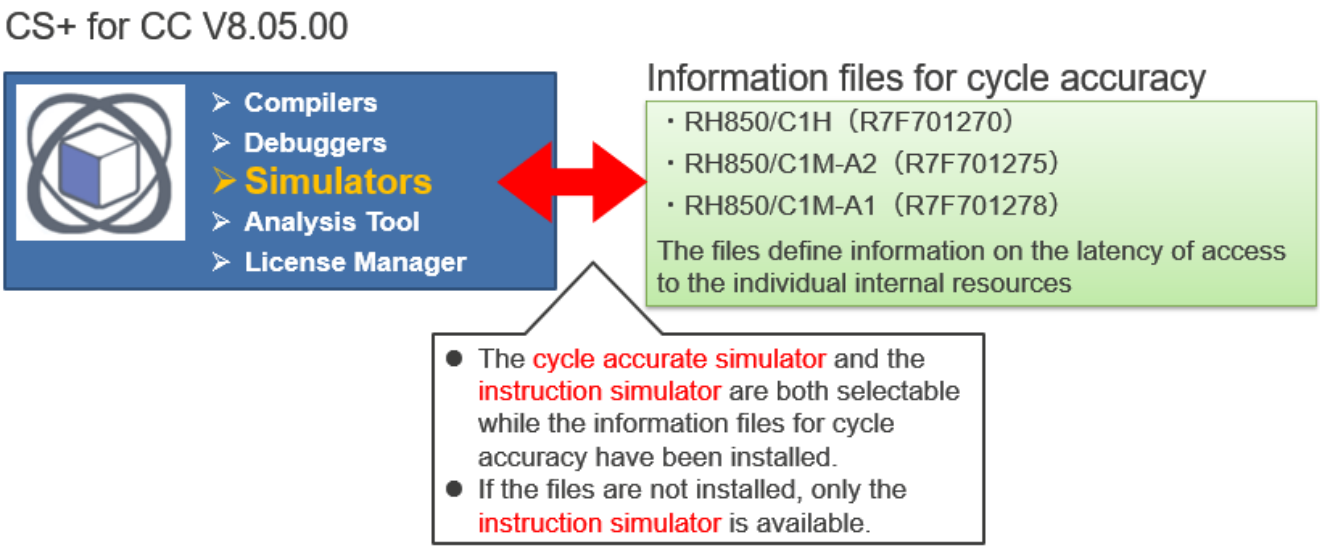


Figure 3-1 Relation between CS+ and the Information Files for Cycle Accuracy

3.3 Registering the License Key

After installing CS+ V8.05.00, activate the License Manager from [Renesas License Manager] of [Renesas Electronics Utilities] from the start menu of Windows.

Click on the [Add license] button of the License Manager and register your provided license key in the [Add License] dialog box.

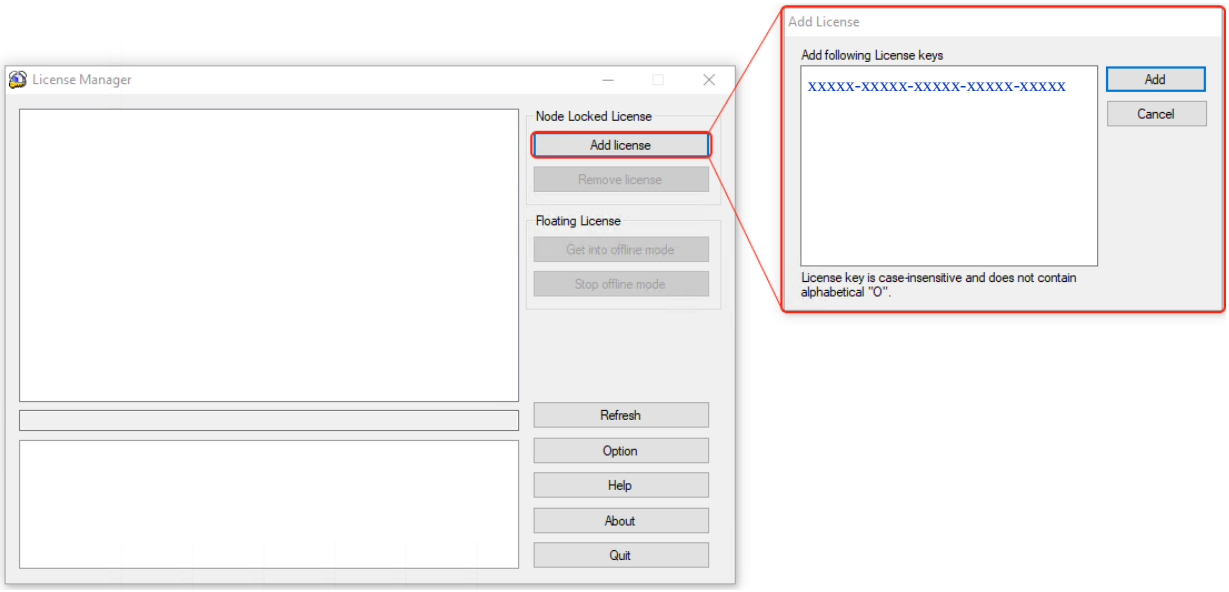


Figure 3-2 License Manager

The software license agreement is displayed when you register a license key for the first time.

Select “Accept” and click on [OK] if you accept the agreement after having read it.

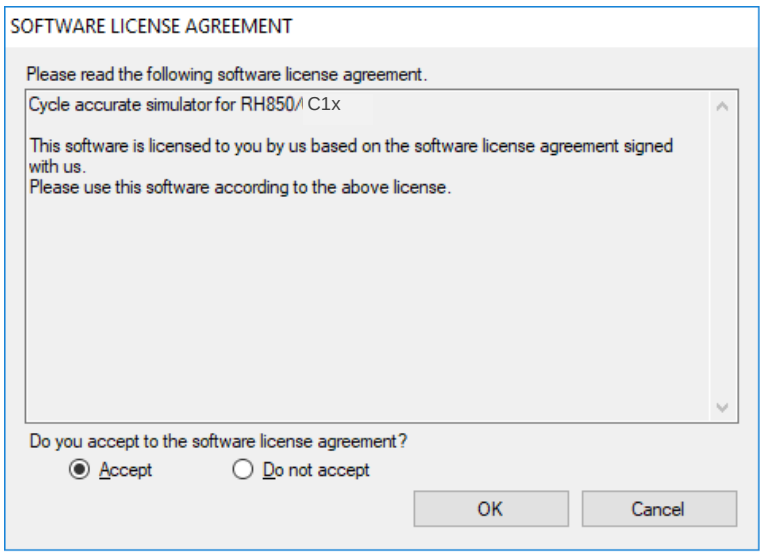


Figure 3-3 Software License Agreement Dialog Box

Check that “Cycle accurate simulator for RH850/C1x” is registered in the list of licenses. This license is valid until the date and time indicated against [Expiration Date].

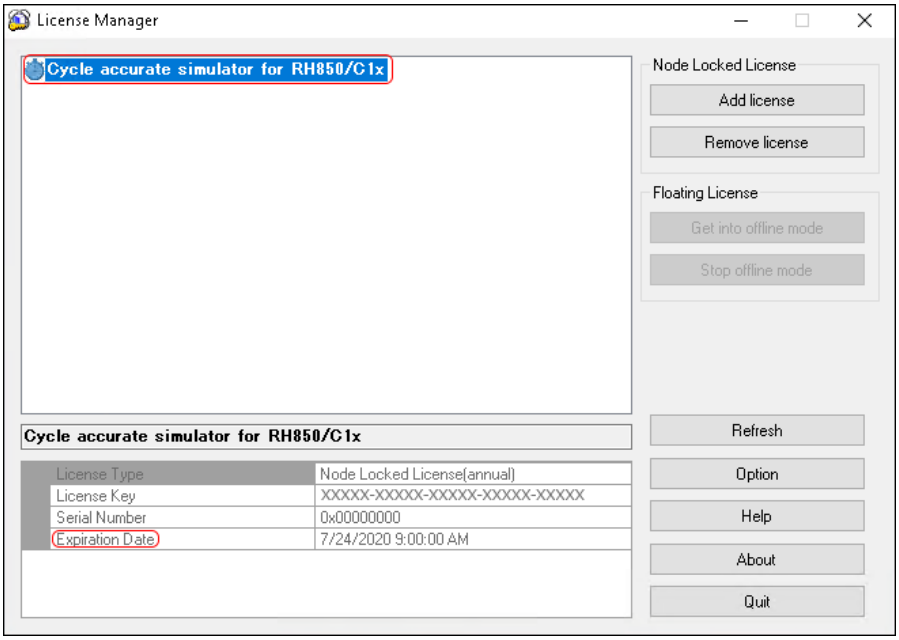


Figure3-4 License Manager with a Registered License
for the Cycle-Accurate Simulators

4. Activating a Simulator

This chapter describes how to activate the cycle-accurate simulators for RH850/C1x devices.

For details on the usage of the simulators, refer to the CS+ V8.05.00 Integrated Development Environment User's Manual: RH850 Debug Tool.

4.1 Specifying a Device

Click on the [Start] button after activating CS+. Then click [GO] on [Create New Project] or [Create New Multi-core Project] in the start panel. When the Create Project dialog box appears, enter “RH850” against [Microcontroller:]. Select [R7F701270] under [RH850/C1H], [R7F701275] under [RH850/C1M-A2], or [R7F701278] under [RH850/C1M-A1] from the list as shown below.

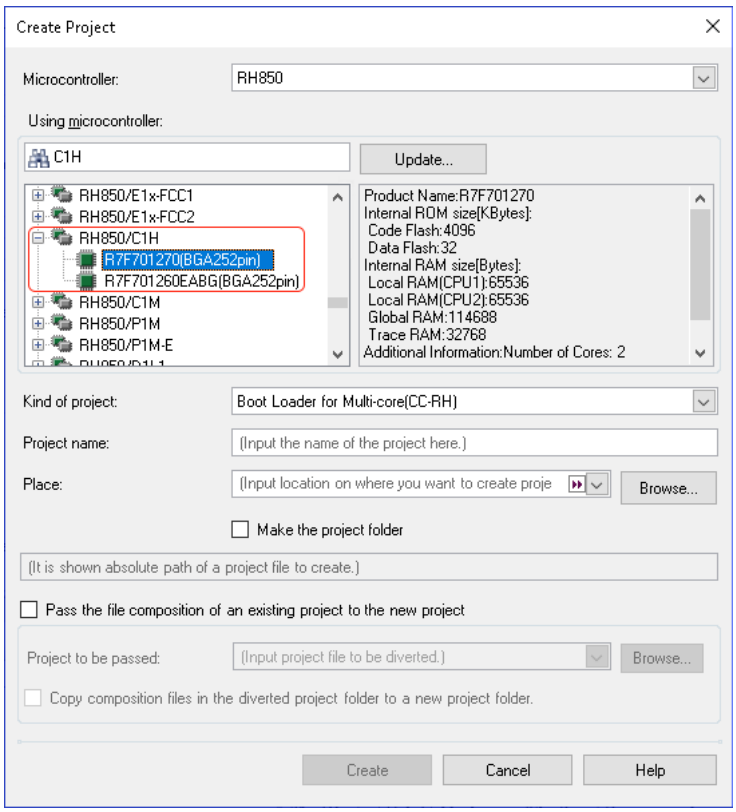


Figure 4-1 Create Project Dialog Box

4.2 Specifying a Debug Tool

In the Project Tree of CS+, right click on [*****(Debug Tool)] and select the debug tool to be specified from [Using Debug Tool]. [RH850 Simulator] is configured as a default. (***** indicates any from among RH850 E2, RH850 E1 (LPD), RH850 E20 (LPD), or RH850 Simulator).

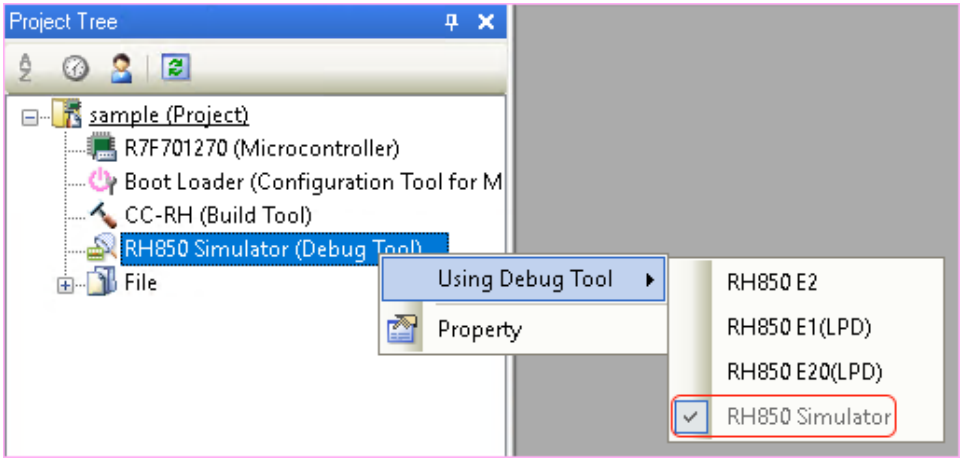


Figure 4-2 Specifying a Debug Tool

4.3 Specifying a Cycle-Accurate Simulator

From the [Connect Settings] tabbed page in the properties of the RH850 Simulator, select [Yes] for [Use cycle accurate simulator] under [Cycle Accurate Simulator]. Selecting [No] activates the instruction simulator. [Yes] is selected by default.

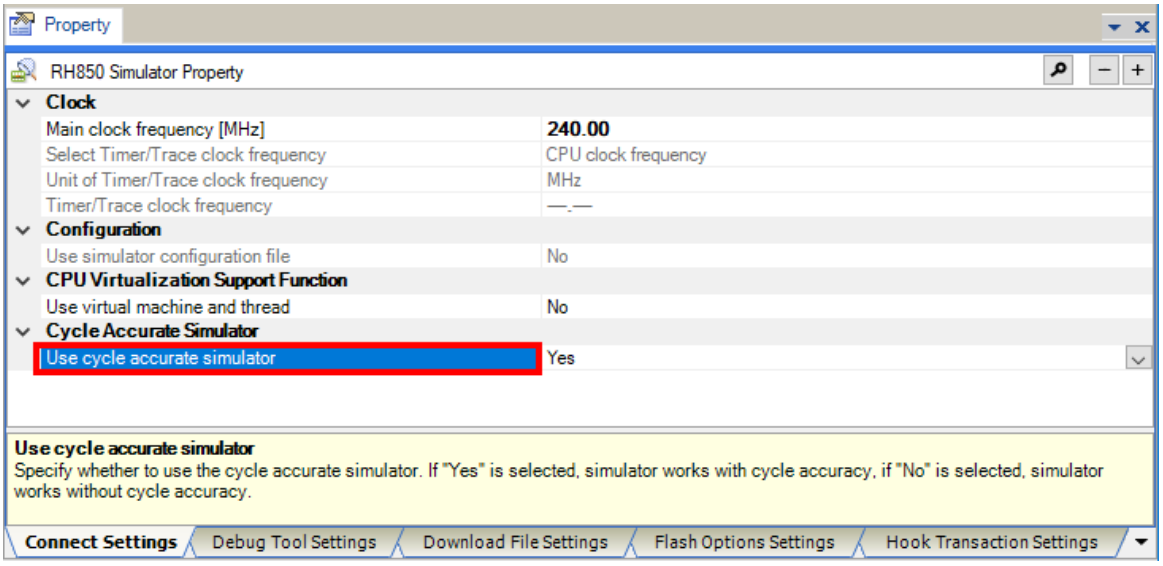


Figure 4-3 Specifying the Cycle-Accurate Simulators

4.4 Selecting a Target for Debugging

Select a file for debugging as follows. In the Project Tree of CS+, right-click on [CC-RH (Build Tool)] then select [Property]. From [Output file type] under [Output File Type and Path] on the [Common Options] tabbed page, you can select a file in either of the following executable forms.

- Load Module File
- Hex File

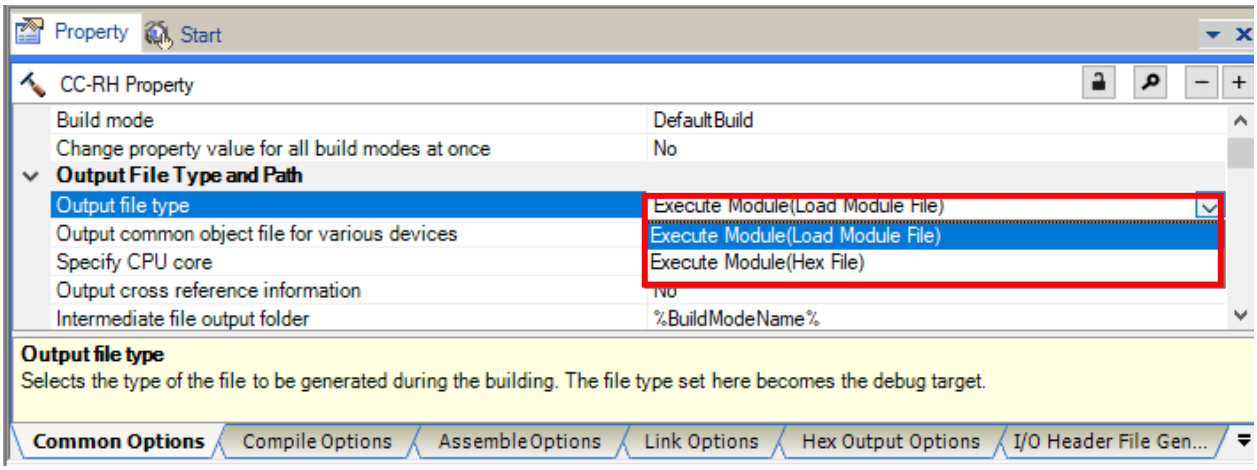


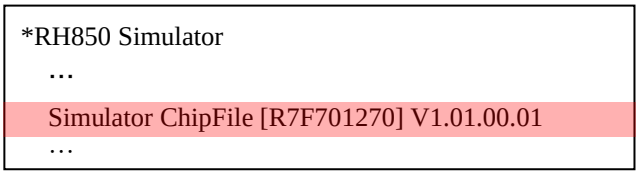
Figure 4-4 Specifying a Target for Debugging

4.5 Activating a Cycle-Accurate Simulator

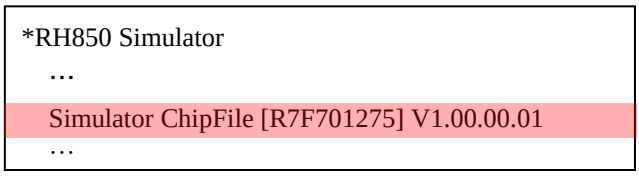
Activate the debug tool as follows. After generating a file in an executable form by rebuilding a project, select [Connect to Debut Tool] from the [Debug] menu of CS+. This activates the debug tool which was specified in chapter 4.2.

Check the version number of the cycle-accurate simulators for RH850/C1x. The number is indicated after “Simulator ChipFile [R7F70****]” of Debug Tool Information, in the information shown in [Detail Version Information] from the [Help] menu of the CS+.

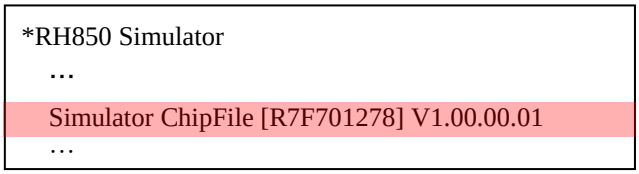
- Select the file indicated below for the RH850/C1H (R7F701270) simulator.



- Select the file indicated below for the RH850/C1M-A2 (R7F701275) simulator.



- Select the file indicated below for the RH850/C1M-A1 (R7F701278) simulator.



5. Points for Caution

This section describes points for caution you will need to note when you use CS+ V8.05.00 with a cycle-accurate simulator for RH850/C1x V1.04.00.

5.1 Executing Programs in Steps

A break occurs when any of the following occurs while a program is being executed. These errors are not detected if the program is in stepwise execution.

- Access to a non-mapped area
- Writing to a write-protected area
- Fetching from a fetch-protected area

5.2 Tracing

- Do not have a point-trace event at the same time as a trace-start event or a trace-end event, otherwise the time will be indicated wrongly in the trace data.
- When a breakpoint is configured at the address of a trace-start event, trace data are not collected in response to the trace-start and trace-end events.
- When a program is executed from the address of a trace-start event, the collection of trace data does not start from the trace-start address.
- When a program is executed in steps at the assembly instruction level, the time tag of the trace data is always displayed as “0”.

5.3 Cache Rate

The cache-hit rate (the ratio of the number of cache hits to the number of times the cache is accessed) is displayed on the [Cache Rate] tabbed page when a break occurs; however, this may be different from the result for the actual device.

5.4 Fetching from the Global RAM Area [Only Applicable to the RH850/C1H (R7F701275)]

On the target device of RH850/C1H (R7F701275), instructions can be fetched from the Global RAM area. However, the simulator cannot fetch instructions from the Global RAM area.

5.5 Option Bytes

The cycle-accurate simulator does not support option bytes.

5.6 Cycle Accuracy

The cycle-accurate simulator simulates the CPU operation in consideration of the latencies of access to various types of memory. However, inaccuracies may become relatively large depending on the program in use.

5.7 Booting up of Individual CPUs and the State of the Sub-CPU (PE3) [Only Applicable to the RH850/C1M-A2 (R7F701275) and the RH850/C1M-A1 (R7F701278)]

The RH850/C1M-A2 (R7F701275) device and the RH850/C1M-A1 (R7F701278) device have a specific option byte for selecting the boot mode for the CPUs and an IO register for selecting which CPUs should be booted up when the MCU is reset.

The cycle-accurate simulator, on the other hand, does not support these facilities, so both CPU1 (PE1) and CPU2 (PE2) [Note] are booted up in response to the MCU having been reset. However, the sub-CPU (PE3) is stopped at this time. If you have selected PE3 as the target of debugging in CS+, “Stop” is indicated on the status bar.

Note: RH850/C1M-A2(R7F701275) only

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 2, 2020	-	First edition issued.

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(Rev.4.0-1 November 2017)

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