ISL74420SLH

Low Dose Rate Total Ionizing Dose Testing of the ISL74420SLH Radiation Hardened Quad Clock Fanout IC

Introduction

This report summarizes the results of low dose rate (LDR) total ionizing dose (TID) testing of the ISL74420SLH Radiation Hardened Quad Clock Fanout IC. The test was conducted to provide an assessment of the total dose hardness of the part and to provide an estimate of the bias sensitivity. Parts were irradiated either under bias or with all pins grounded at a LDR (0.01rad(Si)/s) to 100krad(Si). The ISL74420SLH is rated to 75krad(Si) at LDR and is acceptance tested on a wafer-by-wafer basis to the datasheet limits.

Product Description

The ISL74420SLH is a radiation hardened quad output clock fanout buffer with an optional internal oscillator. It provides synchronization clocks for any application and are particularly useful in multiphase power converters. Each of the four outputs can be set to a different frequency division and phase delay.

Using the CLKIN pin, multiple ISL74420SLH can be connected together to create more than four synchronized clocks.

The division and delay options can be set through selection pins or over an I^2C interface.

In addition to the external CLKIN capability, an internal oscillator operates at 48MHz and is tunable ±10% with an external resistor.

The ISL74420SLHMF is offered in a 48 Lead Ceramic Quad Flat Pack (CQFP) and operates across the full-range military temperature of -55°C to +125°C. The pin assignments are shown in Figure 1 and the pin descriptions are shown in Table 1.

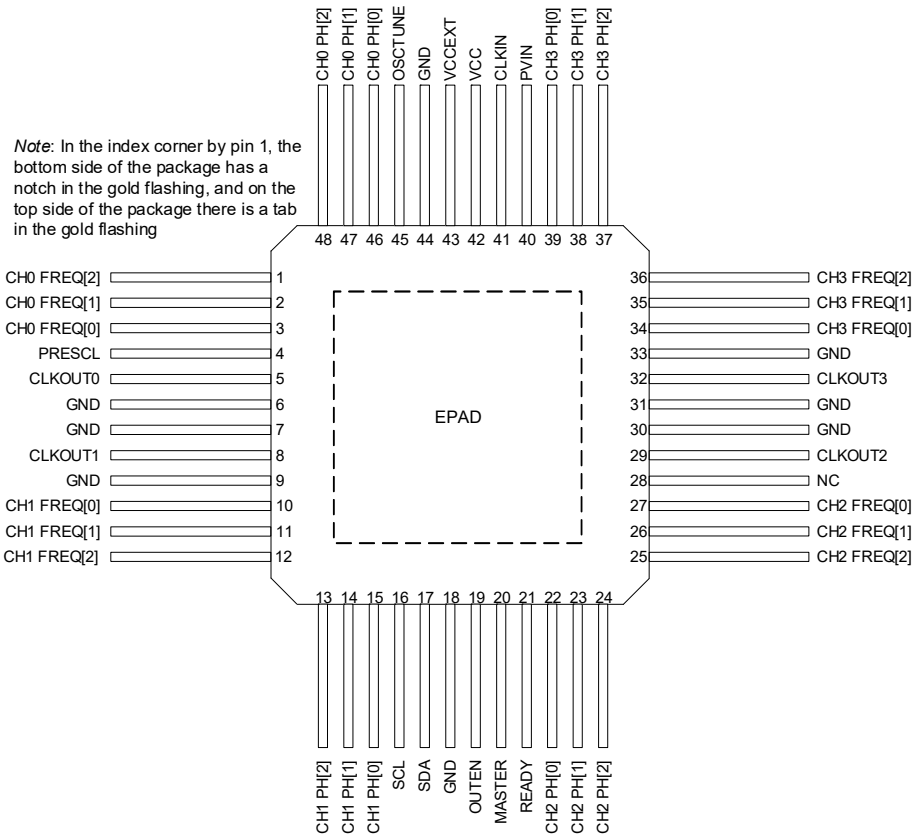

Figure 1. ISL74420SLH Pin Assignments

Table 1. ISL74420SLH Pin Descriptions

Pin Number	Pin Name	Description
1	CH0 FREQ[2]	3 level (tri-level) logic with a 3-bit setting for frequency division selection on Channel 0.
2	CH0 FREQ[1]	
3	CH0 FREQ[0]	
4	PRESCL	3 level (tri-level) logic pre-scaler selection for all channels.
5	CLKOUT0	Clock output pin for Channel 0.
6	GND	Connect this pin to the PCB ground.
7	GND	Connect this pin to the PCB ground.
8	CLKOUT1	Clock output pin for Channel 1
9	GND	Connect this pin to the PCB ground.
10	CH1 FREQ[0]	3 level (tri-level) logic with a 3-bit setting for frequency division selection on Channel 1
11	CH1 FREQ[1]	
12	CH1 FREQ[2]	
13	CH1 PH[2]	3 level (tri-level) logic with a 3-bit setting for phase delay selection for Channel 1
14	CH1 PH[1]	
15	CH1 PH[0]	
16	SCL	I^2C clock input. SCL requires an external pull-up resistor for proper operation. Tie to VCC through a 4.7kΩ to 100kΩ resistor even if I^2C is not going to be used.
17	SDA	I^2C data input/output. SDA requires an external pull-up resistor for proper operation. Tie to VCC through a 4.7kΩ-100kΩ resistor even if I^2C is not going to be used.
18	GND	Connect this pin to the PCB ground.
19	OUTEN	Logic level input to enable the CLKOUTx pins.
20	MASTER	Logic level input to select if the part should use its internal oscillator when no external clock is present. A logic high enables “Leader Mode” and the internal 48MHz oscillator if no CLKIN signal is present. A logic low enables “Follower Mode” and internal oscillator is disabled.
21	READY	Open-drain output to indicate if the part is ready to enable the CLKOUTx pins
22	CH2 PH[0]	3 level (tri-level) logic with a 3-bit setting for phase delay selection for Channel 2
23	CH2 PH[1]	
24	CH2 PH[2]	
25	CH2 FREQ[2]	3 level (tri-level) logic with a 3-bit settling for frequency division selection on Channel 2.
26	CH2 FREQ[1]	
27	CH2 FREQ[0]	
28	NC	No internal connection. Renesas recommends connecting this pin to GND.
29	CLKOUT2	Clock output pin for Channel 2.
30	GND	Connect this pin to the PCB ground.
31	GND	Connect this pin to the PCB ground.
32	CLKOUT3	Clock output pin for Channel 3.
33	GND	Connect this pin to the PCB ground.

Table 1. ISL74420SLH Pin Descriptions (Cont.)

Pin Number	Pin Name	Description
34	CH3 FREQ[0]	3 level (tri-level) logic with a 3-bit setting for frequency division selection on Channel 3.
35	CH3 FREQ[1]	
36	CH3 FREQ[2]	
37	CH3 PH[2]	3 level (tri-level) logic with a 3-bit setting for phase delay selection for Channel 3.
38	CH3 PH[1]	
39	CH3 PH[0]	
40	PVIN	The power supply input to the IC. This supplies power to the internal linear regulator. Locally bypass PVIN to GND with a 0.1µF or larger capacitor.
41	CLKIN	External clock input. Tie this pin to the ISL74420SLHMNF GND with a short trace if not using CLKIN.
42	VCC	Output of the 3.3V internal linear regulator. The regulator can be bypassed by providing a 3.0V-3.6V supply to both PVIN and VCC. Locally bypass VCC to GND with a 1µF capacitor.
43	VCCEXT	The power supply input for all the CLKOUTx pins. This can be connected to VCC or supplied externally to level shift them to a different voltage. If supplied externally, locally bypass VCCEXT to GND with a 1µF or larger capacitor.
44	GND	Connect this pin to the PCB ground.
45	OSCTUNE	Connect a resistor between this pin and GND to adjust the internal oscillator.
46	CH0 PH[0]	3 level (tri-level) logic with a 3-bit setting for phase delay selection for Channel 0.
47	CH0 PH[1]	
48	CH0 PH[2]	
-	EPAD	Connect to the PCB ground.

Contents

1. Test Description

1.1 Irradiation Facility

LDR testing was performed at 0.01rad(Si)/s using a Hopewell Designs N40 vault-type LDR irradiator located in the Palm Bay, Florida Renesas facility. A PbAl box was used to shield the test fixture and devices under test against low energy, secondary gamma radiation.

1.2 Test Fixturing

Figure 2 shows the configuration used for the biased LDR testing and the high temperature anneal.

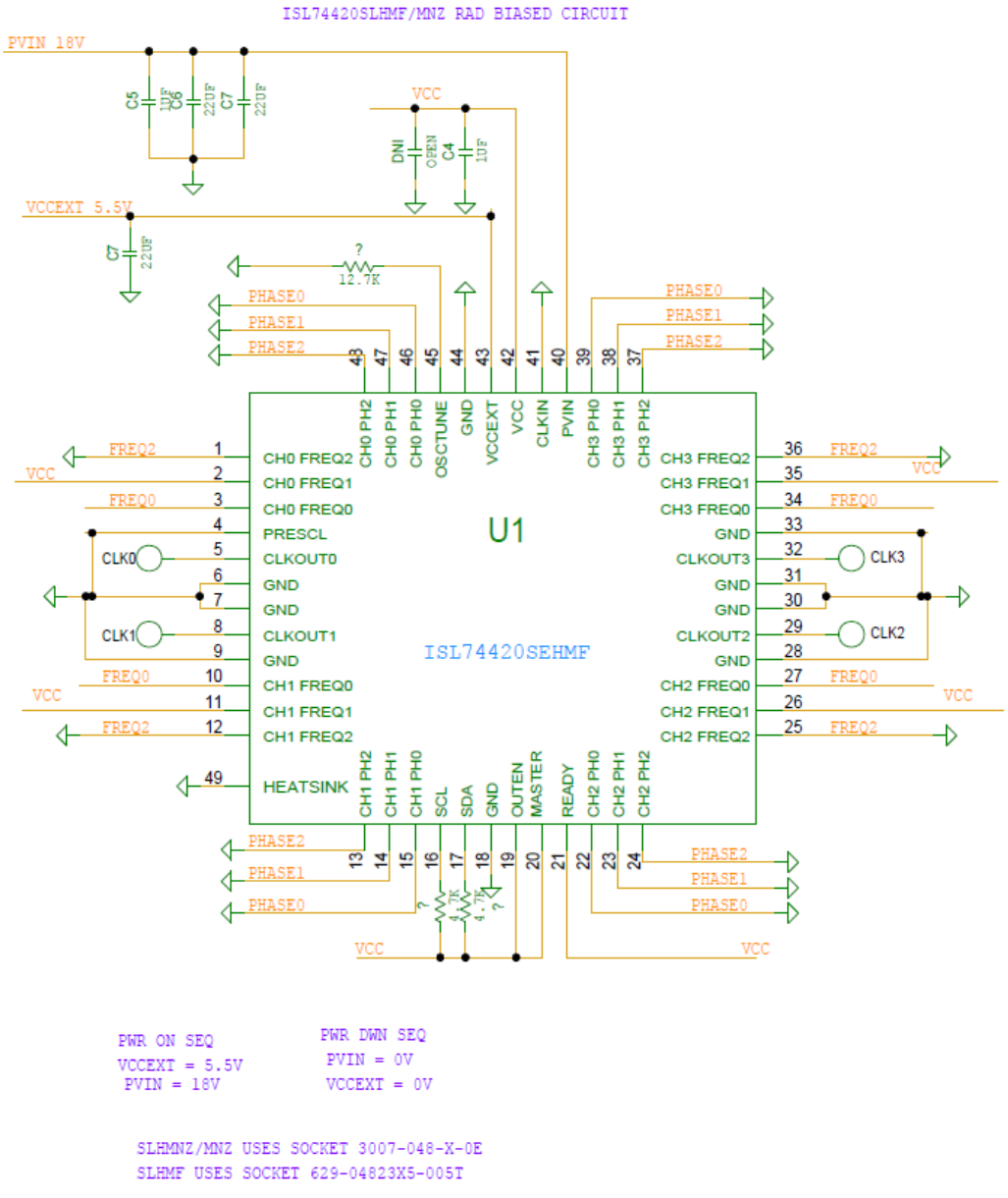

Figure 2. ISL74420SLH LDR Bias Configuration

1.3 Characterization Equipment and Procedures

All electrical testing was performed outside the irradiator using the production Automated Test Equipment (ATE) with data logging at each downpoint. Downpoint electrical testing was performed at room temperature.

1.4 Experimental Matrix

Irradiation was performed in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of thirteen samples irradiated at LDR under bias and nine samples irradiated at LDR with all pins grounded. Three control units were used.

The ISL74420SLH samples were drawn from wafer lots F6X588.1, F6X589.1, and F6X590.1. All samples were packaged in the standard 48 Ld hermetically sealed CQFP package.

1.5 Downpoints

Planned irradiation downpoints for the LDR test were 0krad(Si), 10krad(Si), 30krad(Si), 50krad(Si), 75krad(Si), and 100krad(Si). The LDR irradiations were followed by a 168-hour high temperature anneal at 100ºC under bias.

2. Results

LDR TID testing of the ISL74420SLH is completed. All tested parameters passed the datasheet limits. Table 2 summarizes the preliminary results.

2.1 Attributes Data

Table 2. ISL74420SLH Attributes Data

Dose Rate (rad(Si)/s)	Condition	Sample Size	Downpoint	Pass[1]	Fail
0.01	Biased (Figure 2)	13	Pre-irradiation	13	0
			10krad(Si)	13	0
			30krad(Si)	13	0
			50krad(Si)	13	0
			75krad(Si)	13	0
			100krad(Si)	13	0
			Anneal	13	0
0.01	Grounded	9	Pre-irradiation	9	0
			10krad(Si)	9	0
			30krad(Si)	9	0
			50krad(Si)	9	0
			75krad(Si)	9	0
			100krad(Si)	9	0
			Anneal	9	0

1. A Pass indicates a sample that passes all datasheet limits.

2.2 Variables Data

The plots in Figure 3 through Figure 47 illustrate the LDR response of the selected parameters shown in Table 3 in the Appendix. The plots show the average tested values of the parameters as a function of total dose for each of the irradiation conditions, biased and grounded. The plots also include error bars at each down-point, representing the minimum and maximum measured values of the samples, although in some plots the error bars might not be visible due to their values compared to the scale of the graph.

Some plots denote that the parameter depicted is the average. This indicates that the plotted parameter is the average over all clocks.

All samples passed the datasheet limits after irradiation to each level up to 100krad(Si) and the subsequent anneal.

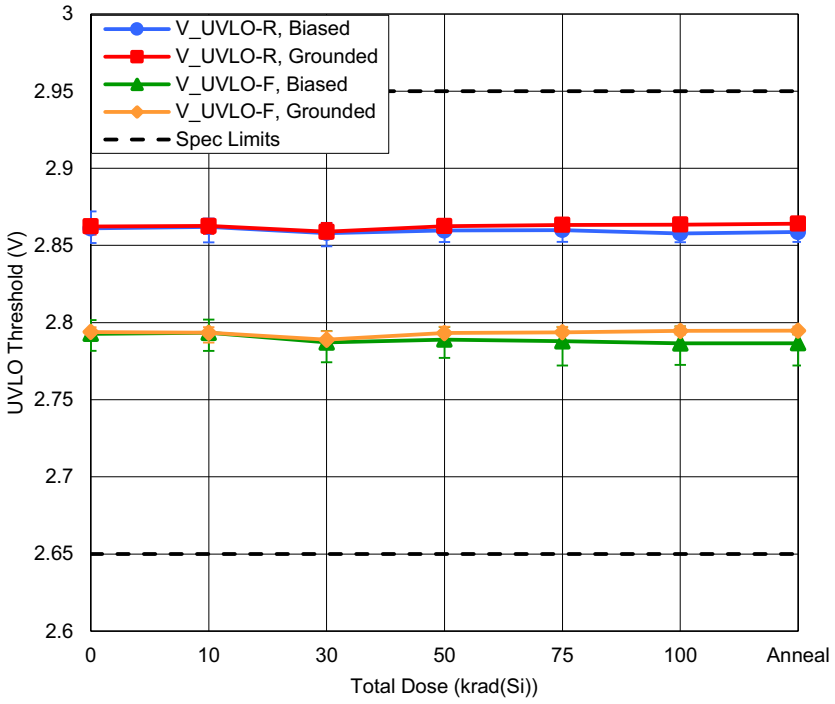

Figure 3. ISL74420SLH UVLO Rising and Falling Threshold (V_{UVLO-R}, V_{UVLO-F}) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a maximum of 2.95V for the rising threshold and a minimum of 2.65V for the falling threshold.

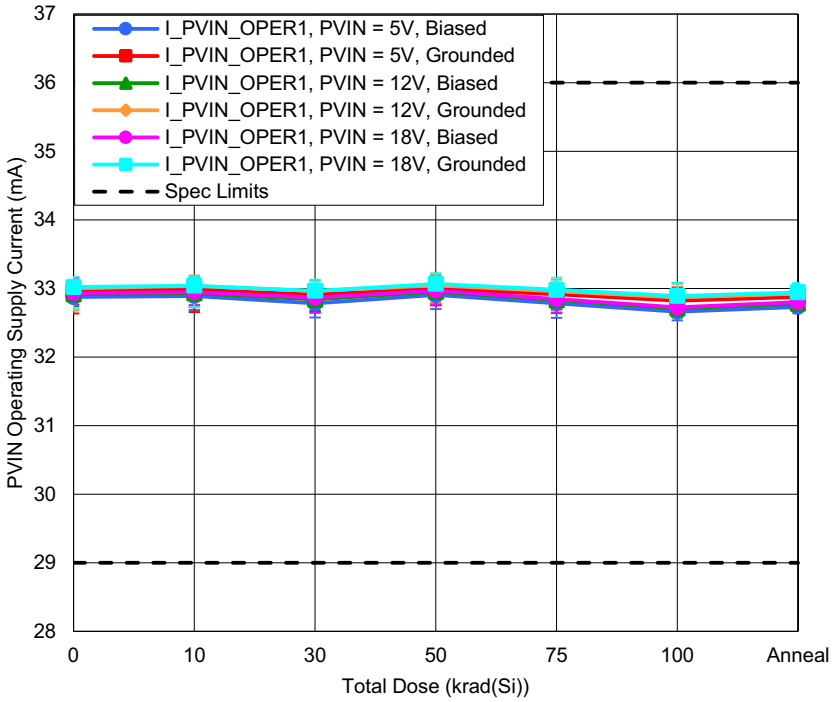

Figure 4. ISL74420SLH PVIN Operating Supply Current - Leader Mode 48MHz out (I_{PVIN_OPER1}) with PVIN = 5V, 12V, or 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 29mA and a maximum of 36mA.

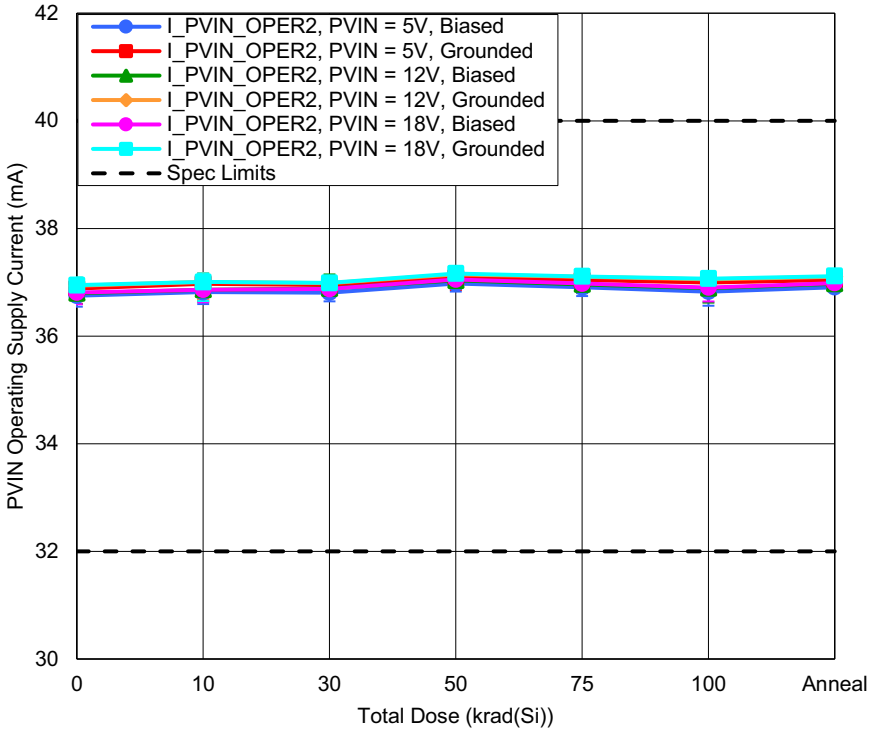

Figure 5. ISL74420SLH PVIN Operating Supply Current - Leader Mode 48MHz out with CLKIN (I_{PVIN_OPER2}) with PVIN = 5V, 12V, or 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 32mA and a maximum of 40mA.

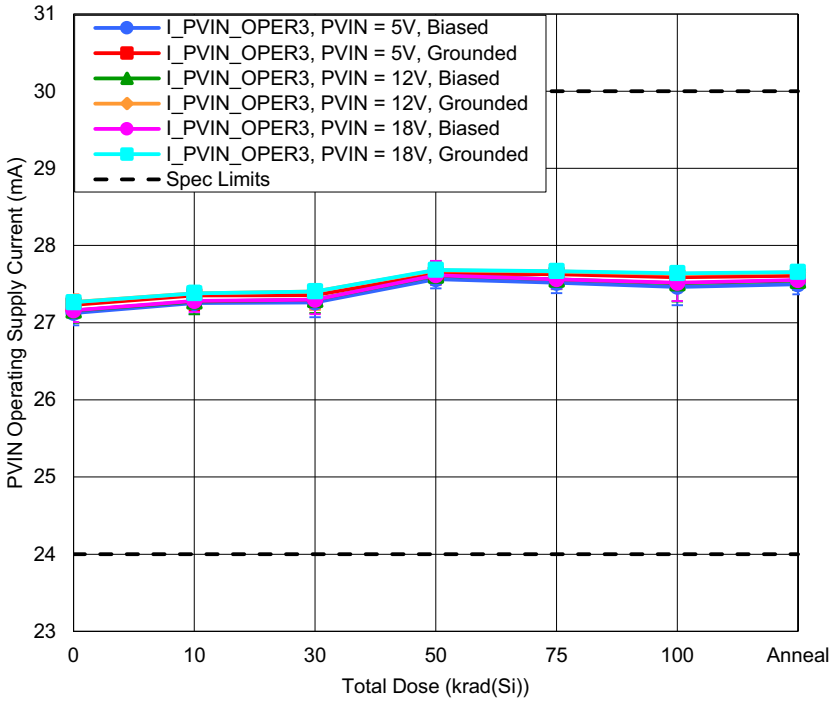

Figure 6. ISL74420SLH PVIN Operating Supply Current - Follower Mode (I_{PVIN_OPER3}) with PVIN = 5V, 12V, or 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 24mA and a maximum of 30mA.

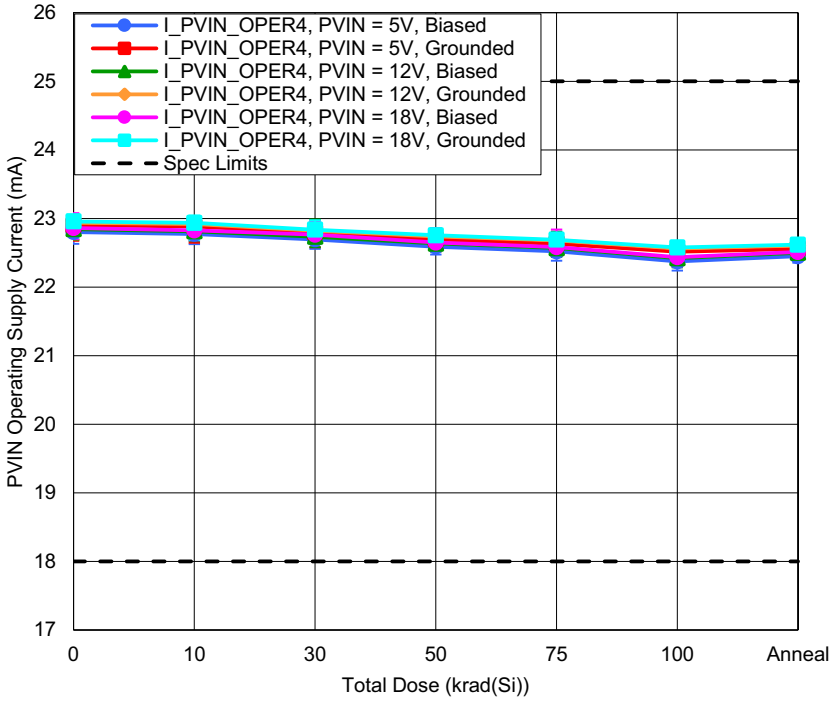

Figure 7. ISL74420SLH PVIN Operating Supply Current - Leader Mode 1MHz out (I_{PVIN_OPER4}) with PVIN = 5V, 12V, or 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 18mA and a maximum of 25mA.

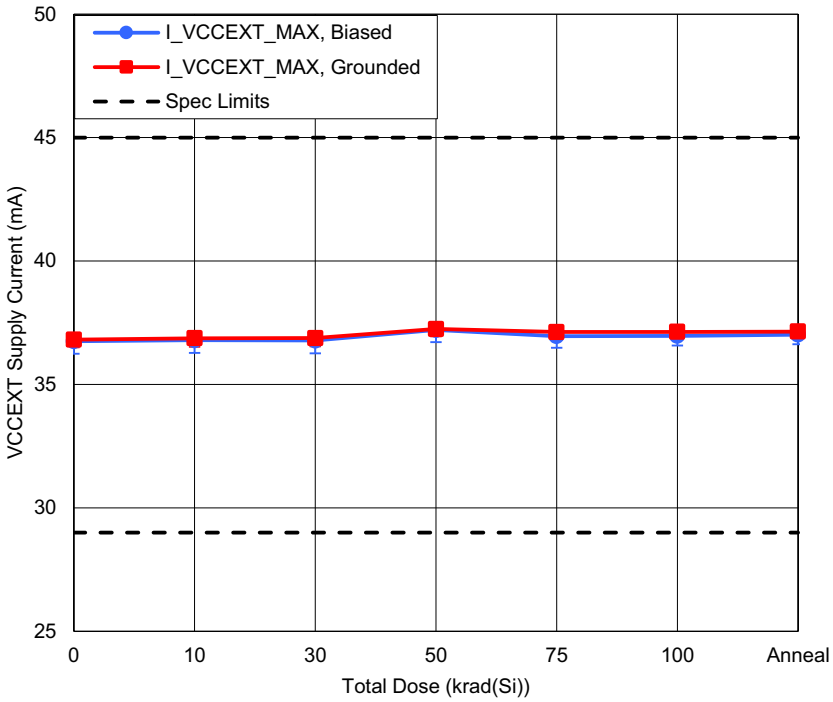

Figure 8. ISL74420SLH VCCEXT Supply Current (I_{VCCEXT_MAX}) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 29mA and a maximum of 45mA.

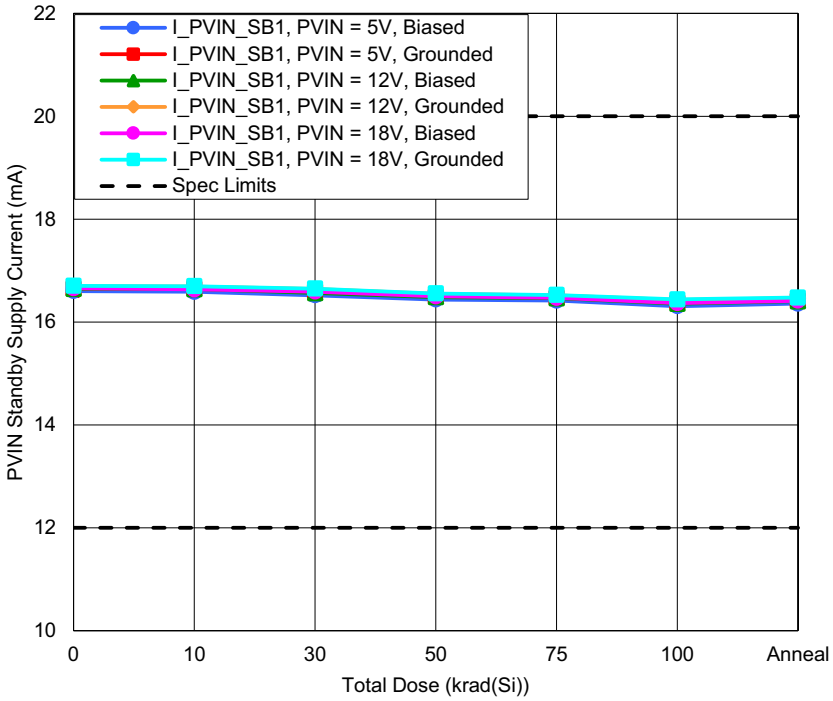

Figure 9. ISL74420SLH PVIN Standby Leader Moder Supply Current (I_{PVIN_SB1}) with PVIN = 5V, 12V, or 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 12mA and a maximum of 20mA.

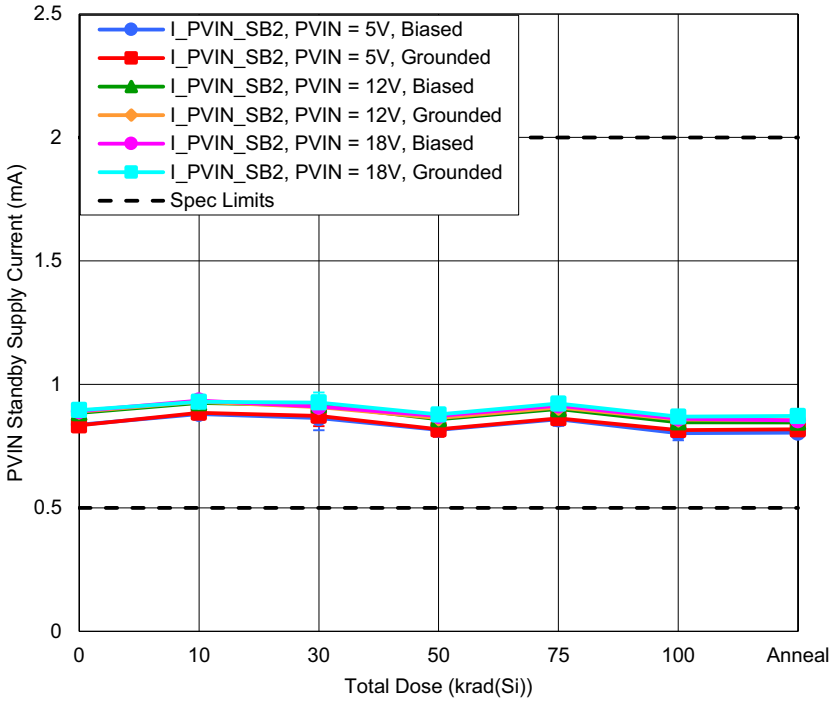

Figure 10. ISL74420SLH PVIN Standby Follower Mode Supply Current (I_{PVIN_SB2}) with PVIN = 5V, 12V, or 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0.5mA and a maximum of 2mA.

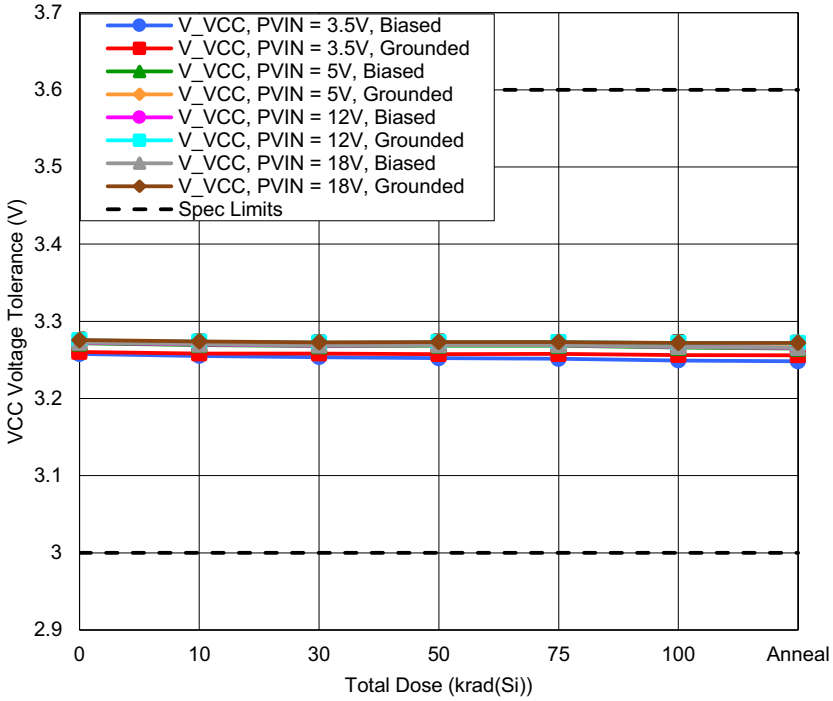

Figure 11. ISL74420SLH VCC Voltage Tolerance (V_{VCC}) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 3V and a maximum of 3.6V.

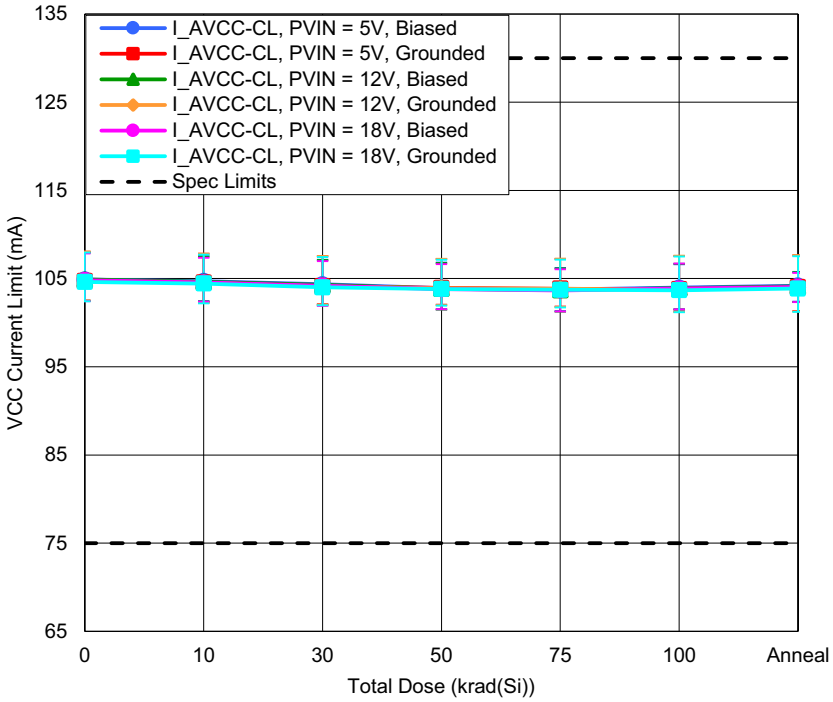

Figure 12. ISL74420SLH VCC Current Limit ($I_{AVCC-CL}$) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 75mA and a maximum of 130mA.

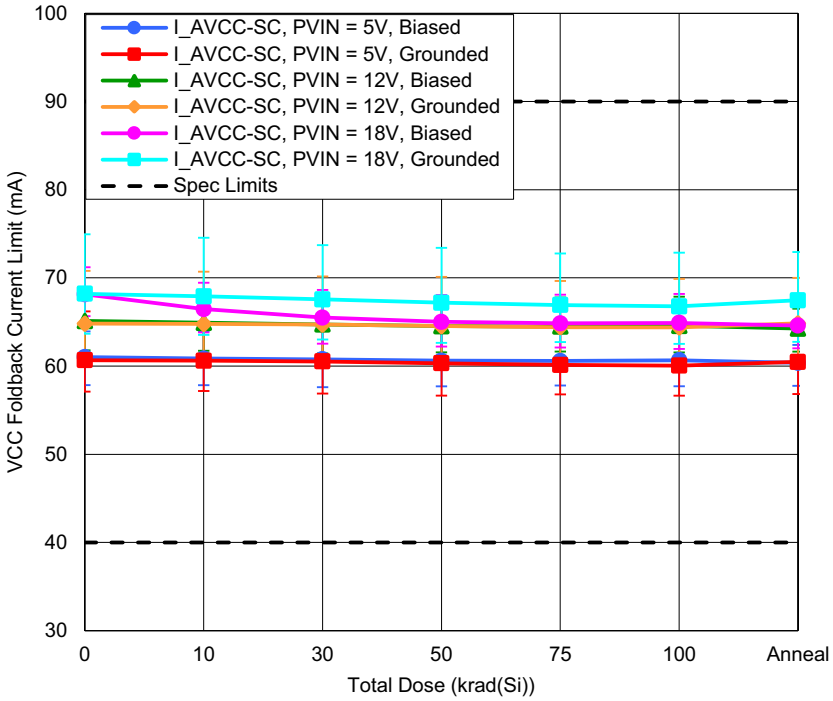

Figure 13. ISL74420SLH VCC Foldback Current Limit ($I_{AVCC-SC}$) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 40mA and a maximum of 90mA.

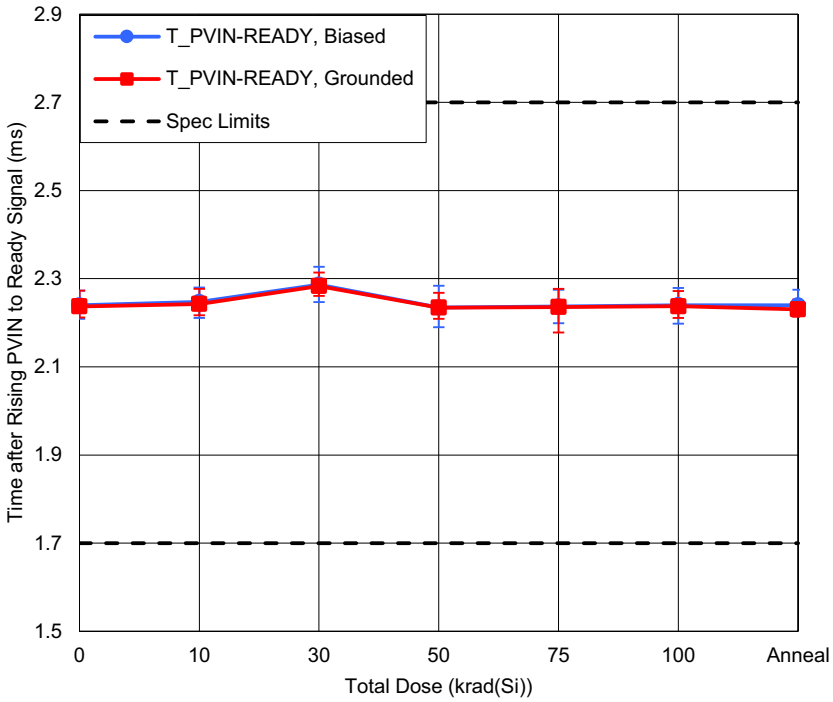

Figure 14. ISL74420SLH Time after Rising PVIN to READY Signal ($T_{PVIN-READY}$) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 1.7ms and a maximum of 2.7ms.

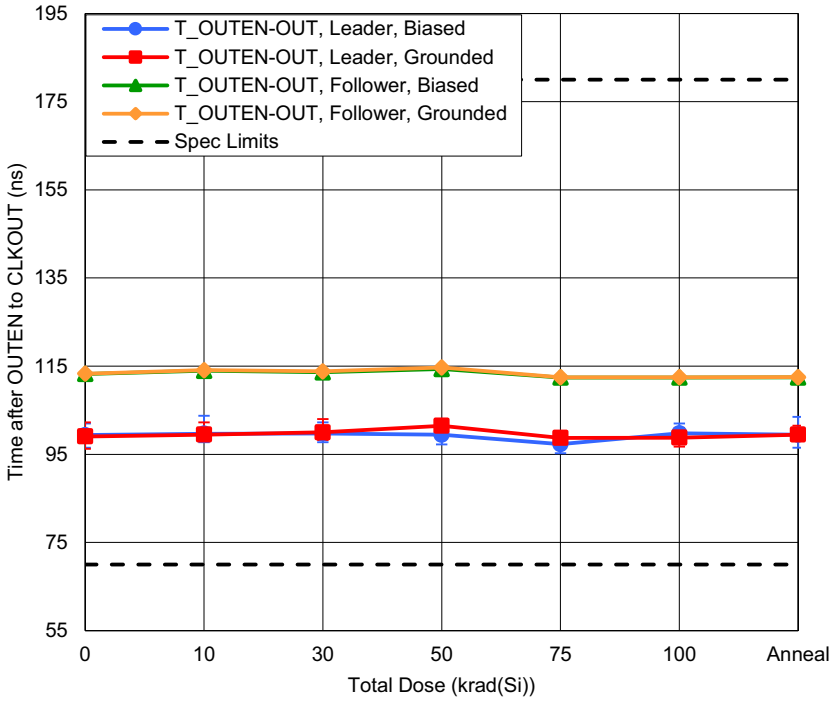

Figure 15. ISL74420SLH Time after OUTEN to CLKOUT with Phase = 0° ($T_{OUTEN-OUT}$) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 70ns and a maximum of 180ns.

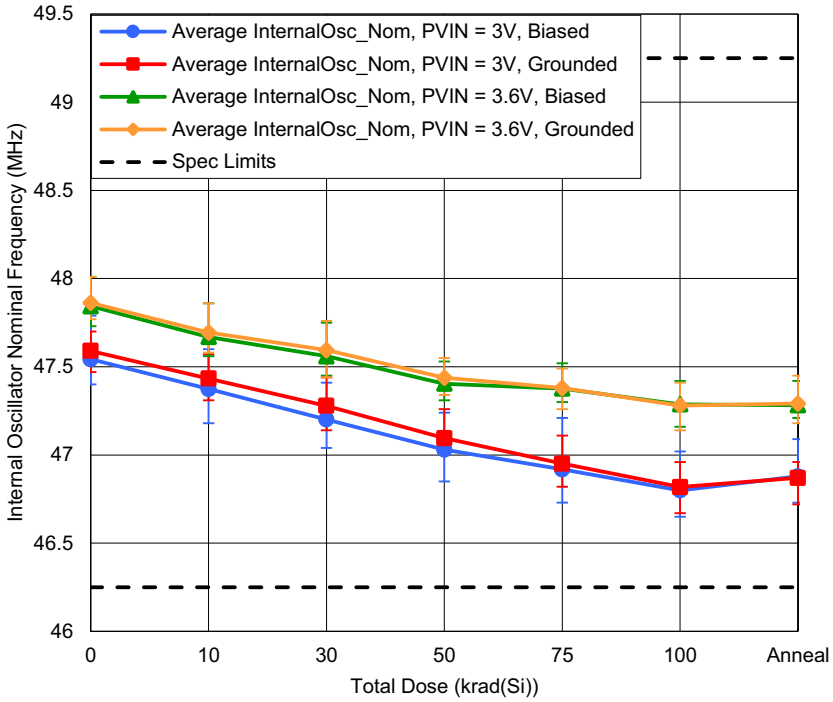

Figure 16. ISL74420SLH average Internal Oscillator Nominal Frequency (InternalOsc_Nom) with PVIN = VCC = 3V or 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all clocks. The datasheet limits are a minimum of 46.25MHz and a maximum of 49.25MHz.

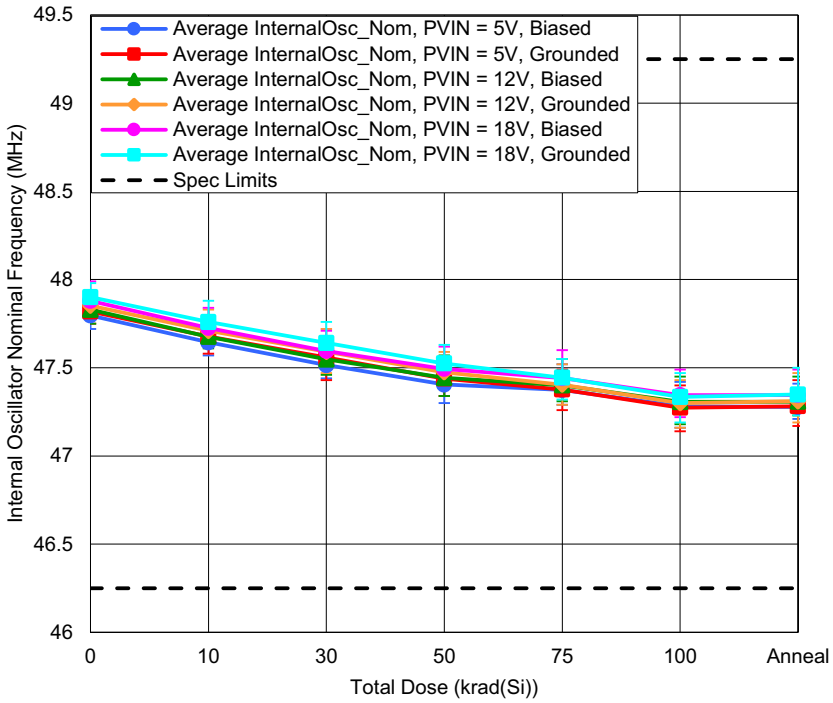

Figure 17. ISL74420SLH average Internal Oscillator Nominal Frequency (InternalOsc_Nom) with VCC regulating and with PVIN = 5V, 12V, or 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all clocks. The datasheet limits are a minimum of 46.25MHz and a maximum of 49.25MHz.

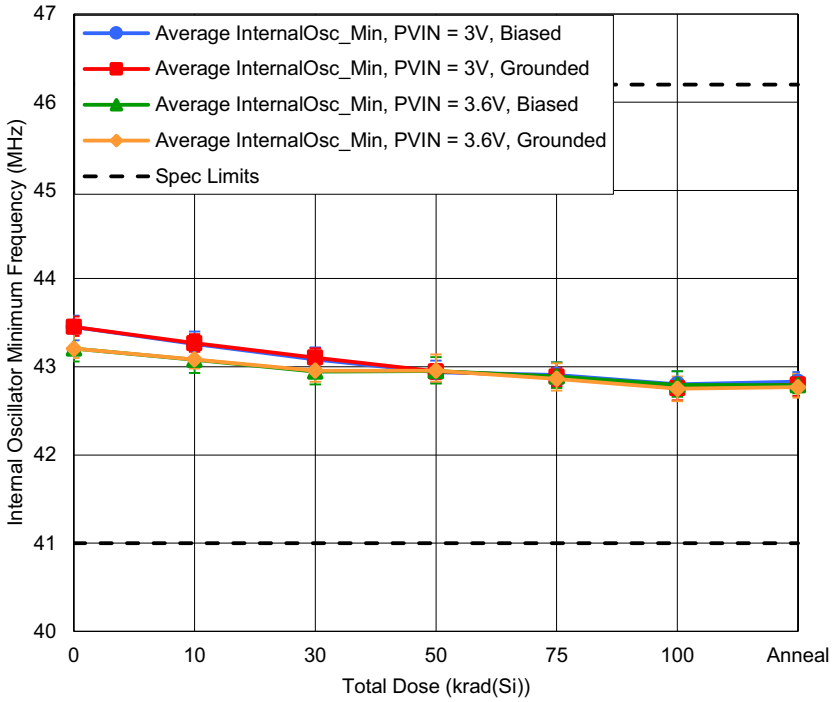

Figure 18. ISL74420SLH average Internal Oscillator Minimum Frequency (InternalOsc_Min) with PVIN = VCC = 3V or 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all clocks. The datasheet limits are a minimum of 41MHz and a maximum of 46.2MHz.

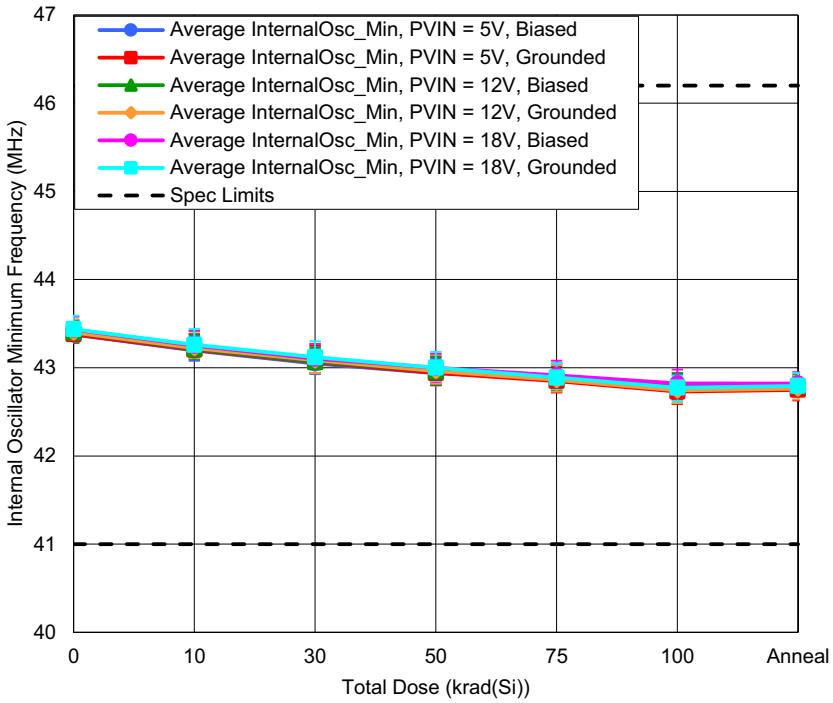

Figure 19. ISL74420SLH average Internal Oscillator Minimum Frequency (InternalOsc_Min) with VCC = PVIN = 5V, 12V, or 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all clocks. The datasheet limits are a minimum of 41MHz and a maximum of 46.2MHz.

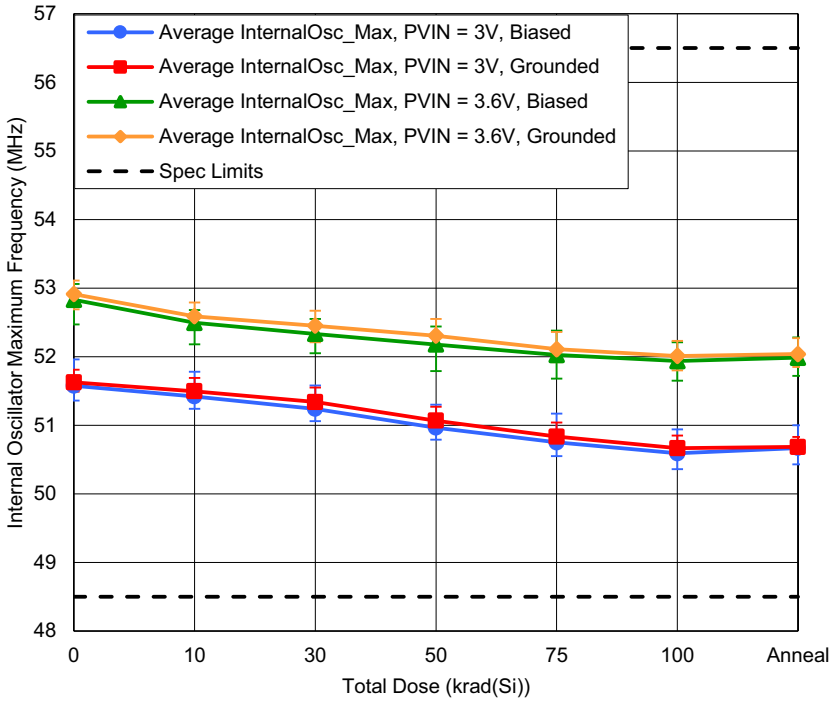

Figure 20. ISL74420SLH average Internal Oscillator Maximum Frequency (InternalOsc_Max) with PVIN = VCC = 3V or 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all clocks. The datasheet limits are a minimum of 48.5MHz and a maximum of 56.5MHz.

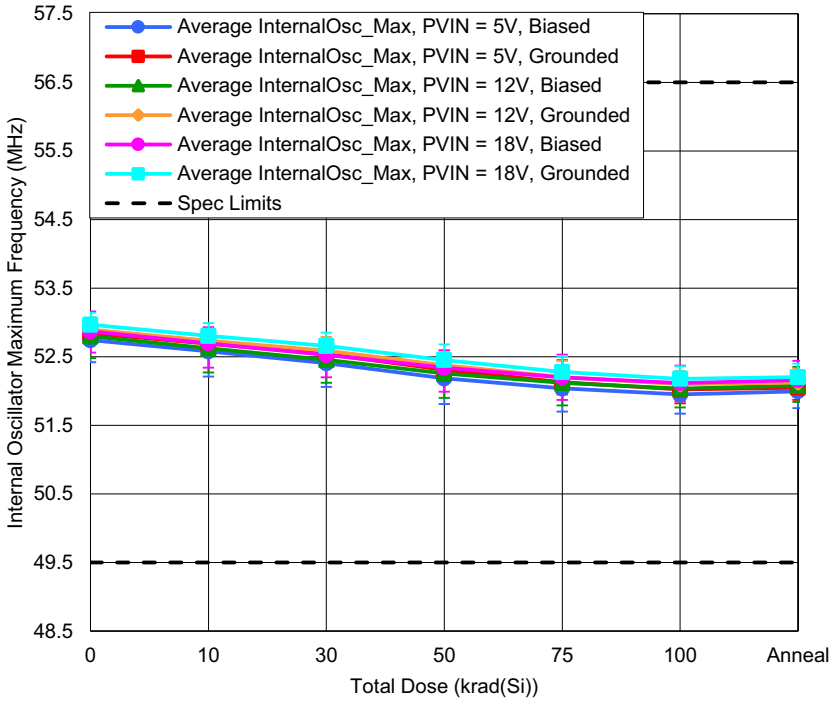

Figure 21. ISL74420SLH average Internal Oscillator Maximum Frequency (InternalOsc_Max) with VCC = PVIN = 5V, 12V, or 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all clocks. The datasheet limits are a minimum of 49.5MHz and a maximum of 56.5MHz

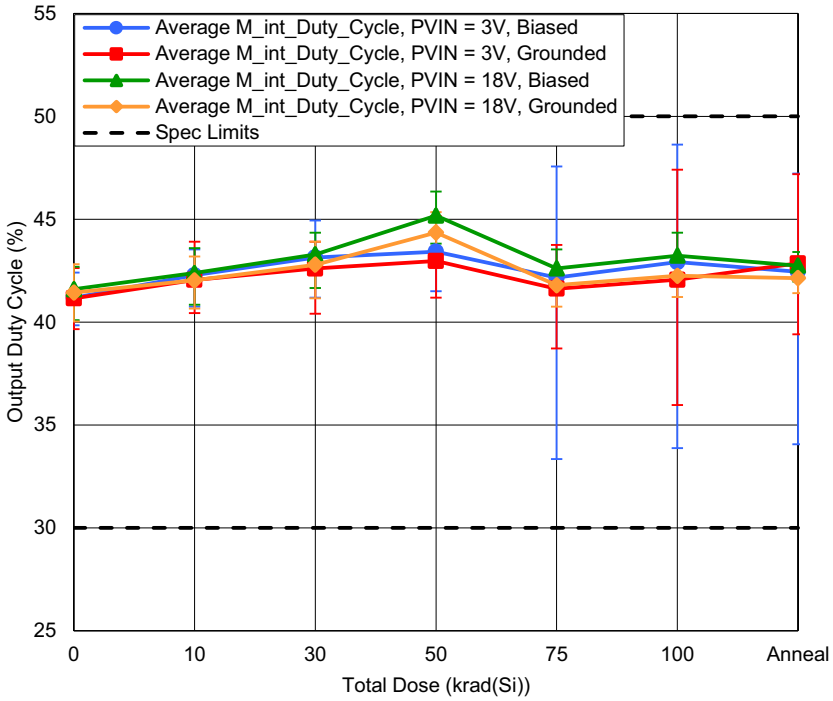

Figure 22. ISL74420SLH average Output Duty Cycle in Leader Mode with Internal Oscillator (M_int_Duty_Cycle) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all clocks. The datasheet limits are a minimum of 30% and a maximum of 50%.

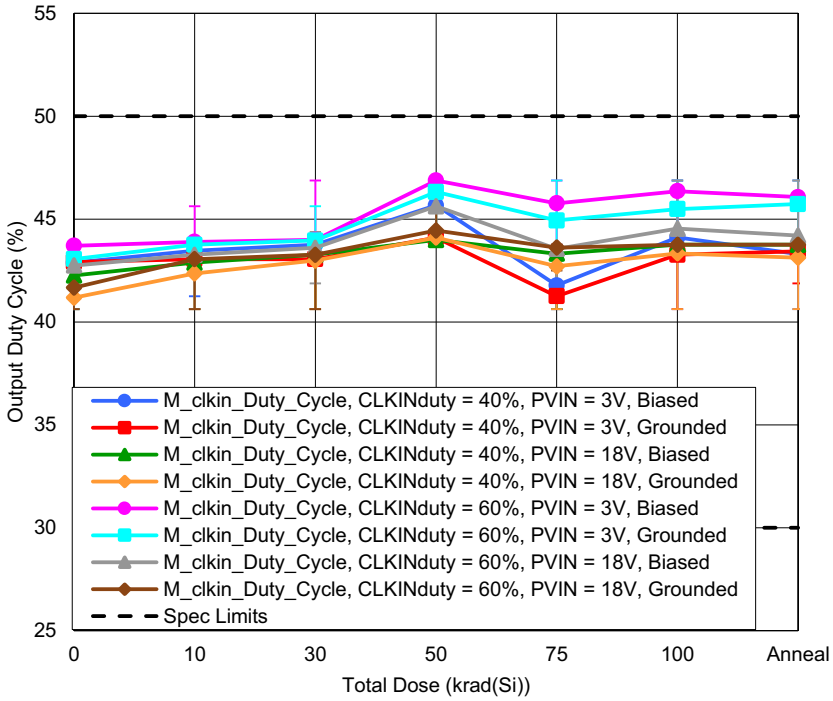

Figure 23. ISL74420SLH Output Duty Cycle in Leader Mode with CLKIN (M_clkin_Duty_Cycle) with CLKINduty = 40% or 60% and with PVIN = 3V or 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 30% and a maximum of 50%.

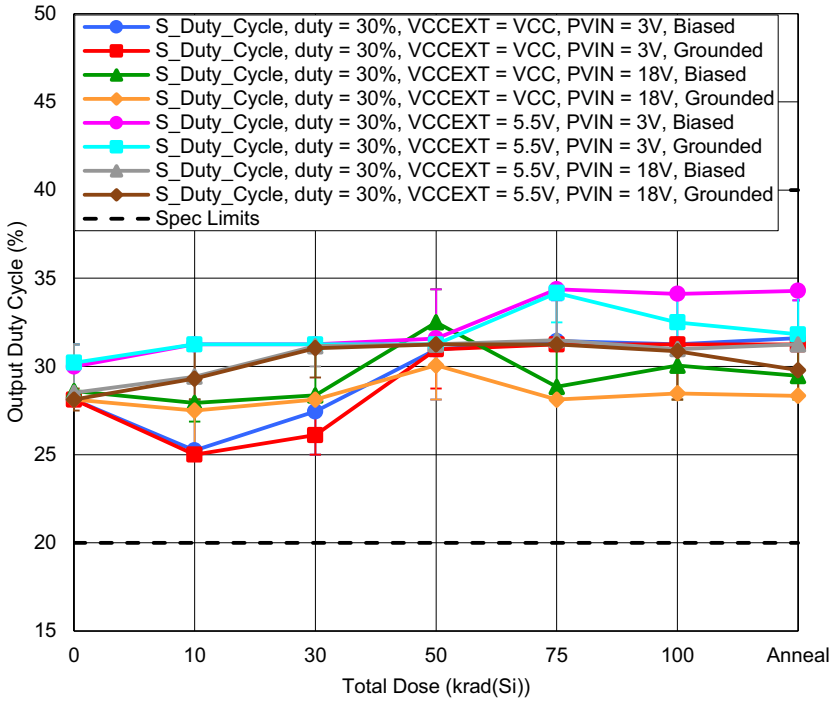

Figure 24. ISL74420SLH Output Duty Cycle in Follower Mode (S_Duty_Cycle) with VCCEXT = VCC or 5.5V, PVIN = 3V or 18V, CLKINfreq = 30MHz, and with CLKINduty = 30% duty cycle as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 20% and a maximum of 40%.

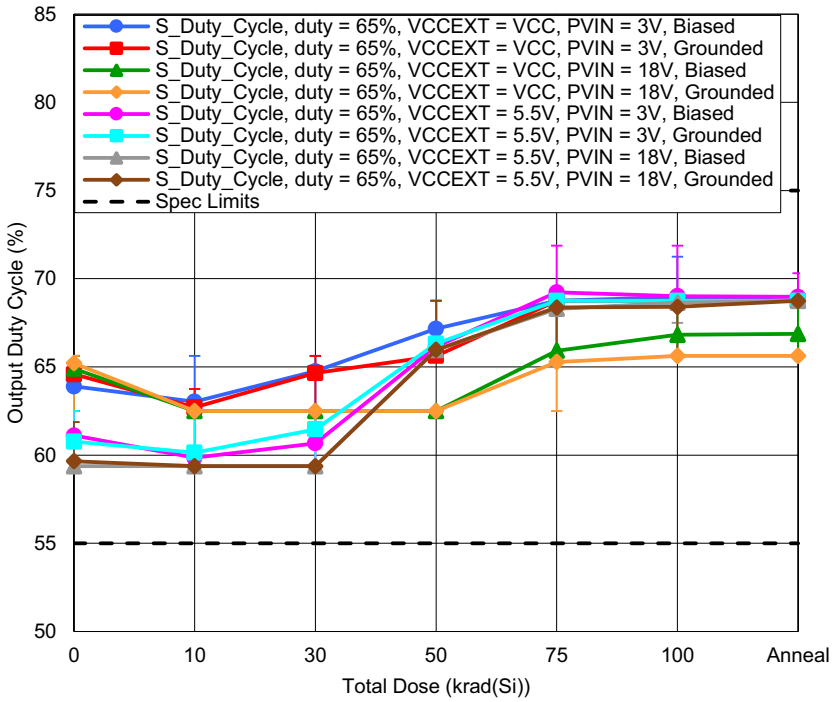

Figure 25. ISL74420SLH Output Duty Cycle in Follower Mode (S_Duty_Cycle) with VCCEXT = VCC or 5.5V, PVIN = 3V or 18V, CLKINfreq = 30MHz, and with CLKINduty = 65% duty cycle as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 55% and a maximum of 75%.

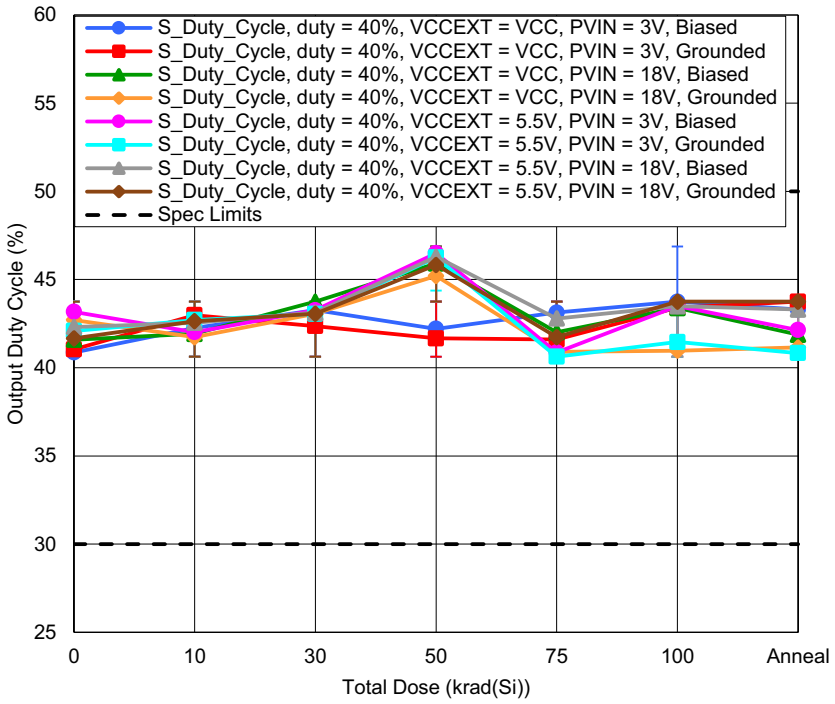

Figure 26. ISL74420SLH Output Duty Cycle in Follower Mode (S_Duty_Cycle) with VCCEXT = VCC or 5.5V, PVIN = 3V or 18V, CLKINfreq = 50MHz, and with CLKINduty = 40% duty cycle as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 30% and a maximum of 50%.

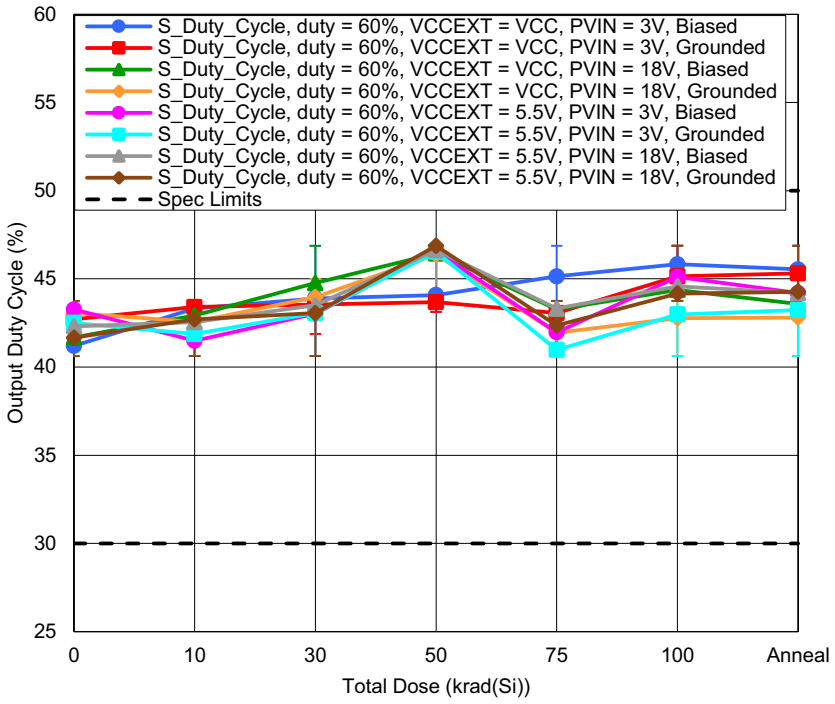

Figure 27. ISL74420SLH Output Duty Cycle in Follower Mode (S_Duty_Cycle) with VCCEXT = VCC or 5.5V, PVIN = 3V or 18V, CLKINfreq = 50MHz, and with CLKINduty = 60% duty cycle as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 30% and a maximum of 50%.

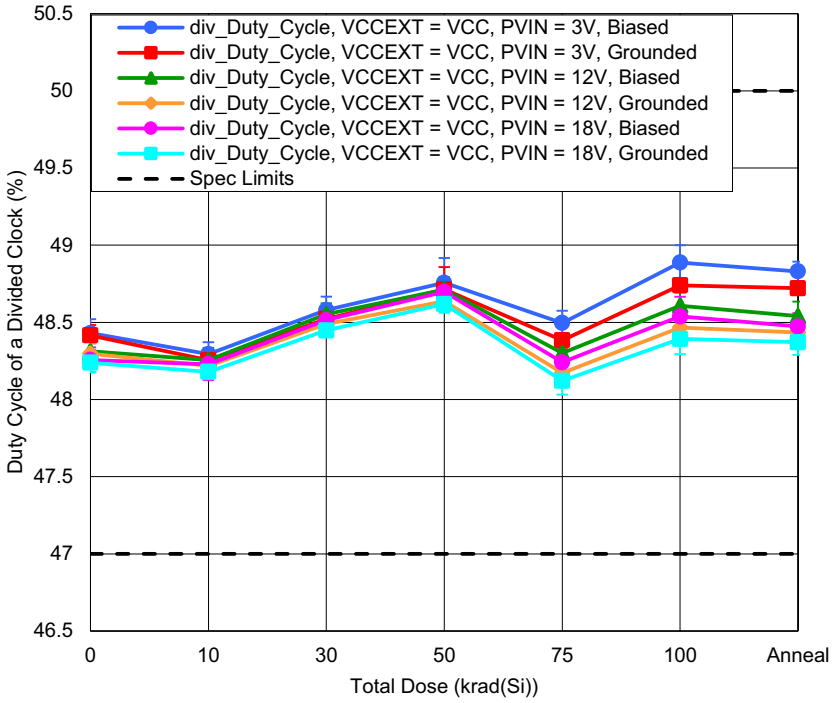

Figure 28. ISL74420SLH Duty Cycle of a Divided Clock (div_Duty_Cycle) with VCCEXT = VCC and PVIN = 3V, 12V, or 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 47% and a maximum of 50%.

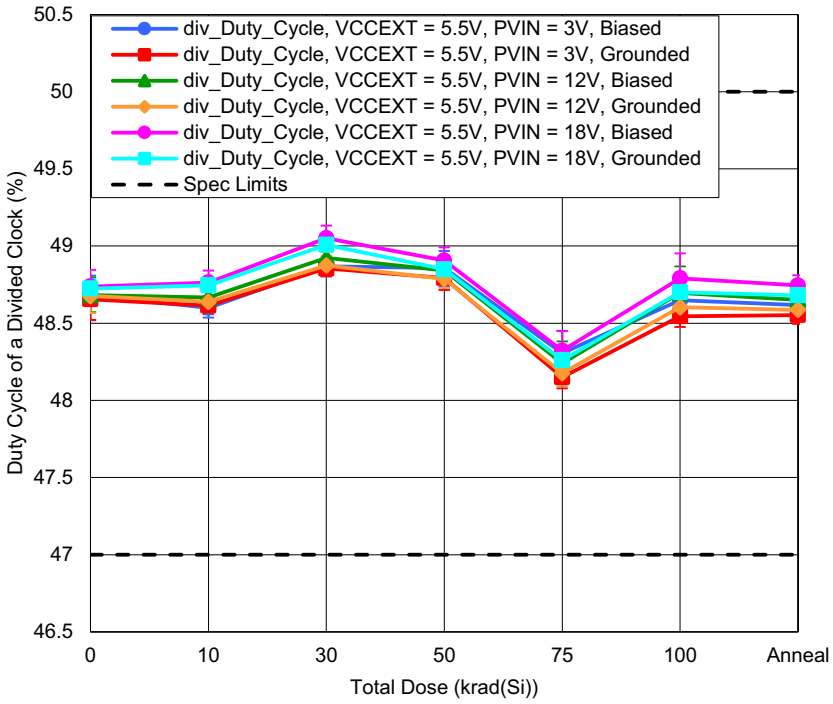

Figure 29. ISL74420SLH Duty Cycle of a Divided Clock (div_Duty_Cycle) with VCCEXT = 5.5V and PVIN = 3V, 12V, or 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 47% and a maximum of 50%.

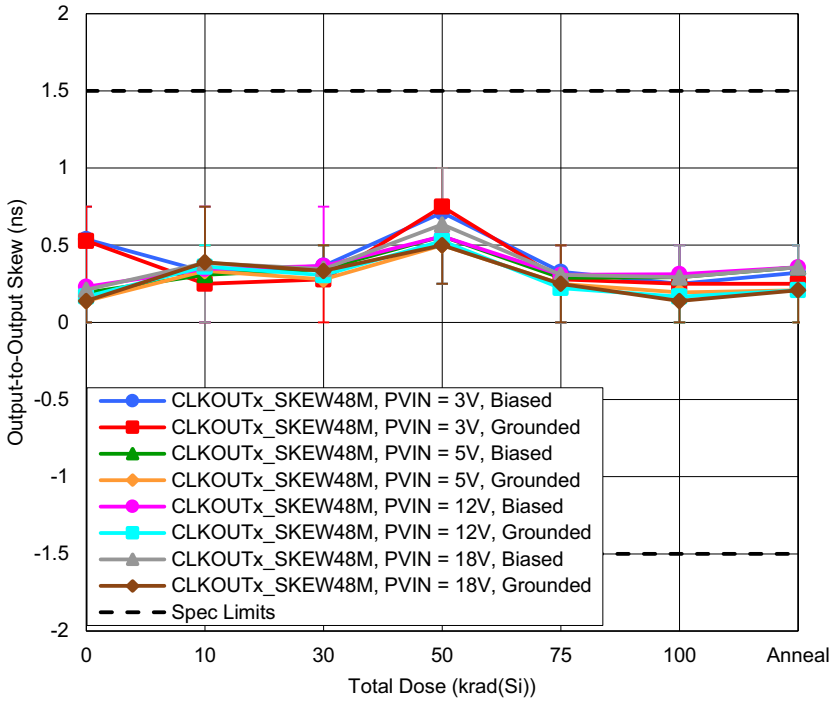

Figure 30. ISL74420SLH Output-to-Output Skew between CLKOUTx's with Equal Frequency and Phase ($CLKOUTx_{SKEW48M}$) with CH[0:3]FREQ = Option 0 and PVIN = 3V, 5V, 12V, or 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -1.5ns and a maximum of 1.5ns.

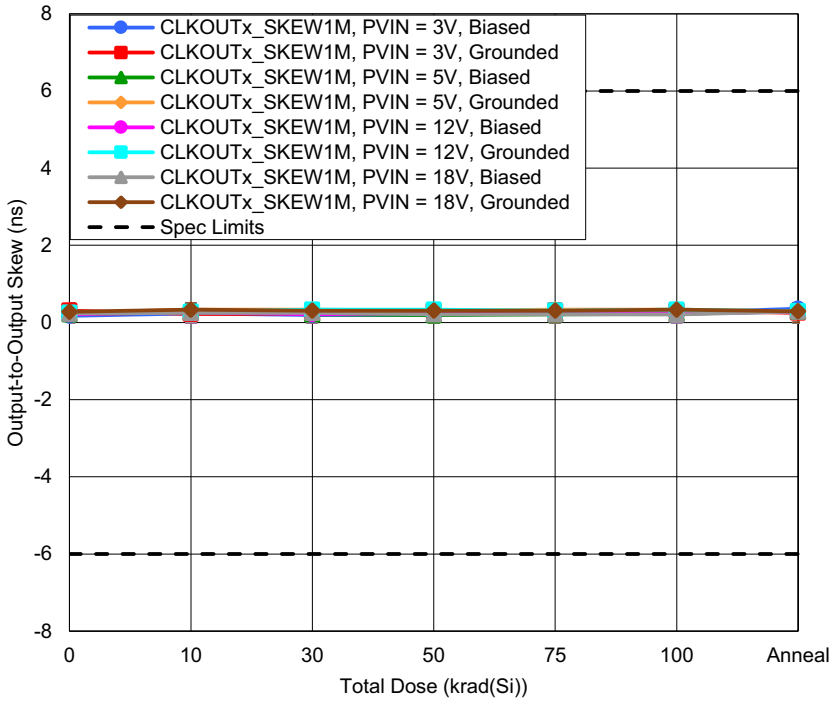

Figure 31. ISL74420SLH Output-to-Output Skew between CLKOUTx's with Equal Frequency and Phase ($CLKOUTx_{SKEW1M}$) with CH[0:3]FREQ = Option 5 and PVIN = 3V, 5V, 12V, or 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -6ns and a maximum of 6ns.

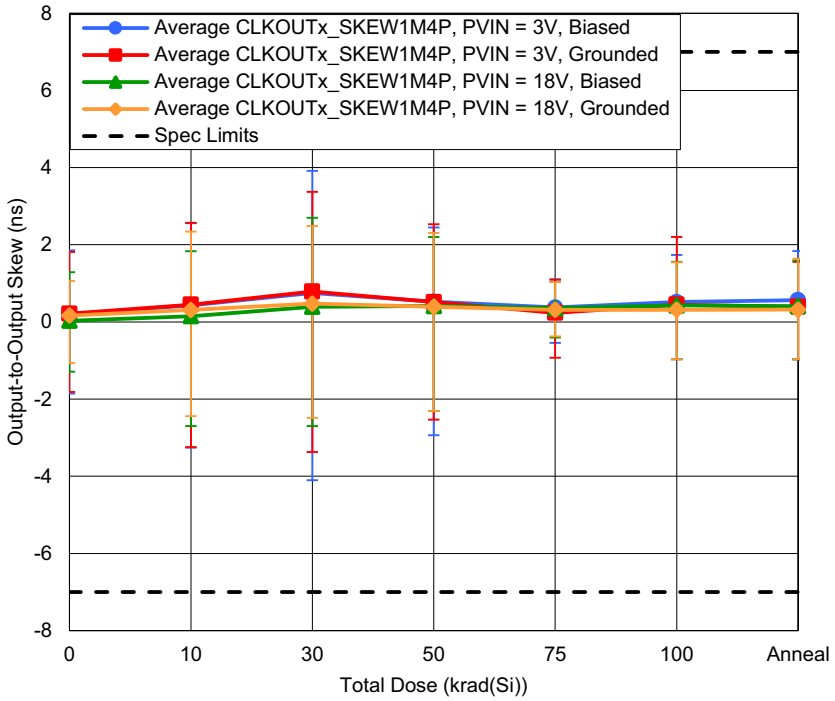

Figure 32. ISL74420SLH average Output-to-Output Skew Between CLKOUTx's with Equal Frequency and Different Phase ($CLKOUTx_{SKEW1M4P}$) with PVIN = 3V or 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all clocks. The datasheet limits are a minimum of -7ns and a maximum of 7ns.

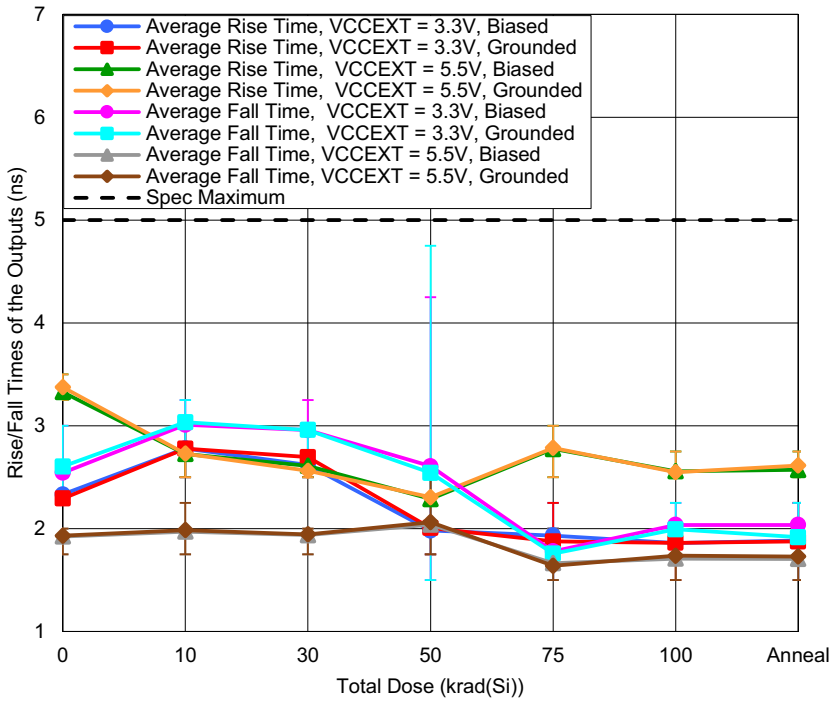

Figure 33. ISL74420SLH average CLKIN-to-CLKOUT Follower Mode Propagation Delay ($CLK_{PROPDELAY}$) with PVIN = 3V or 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all clocks. The datasheet limits are a minimum of 20ns and a maximum of 40ns.

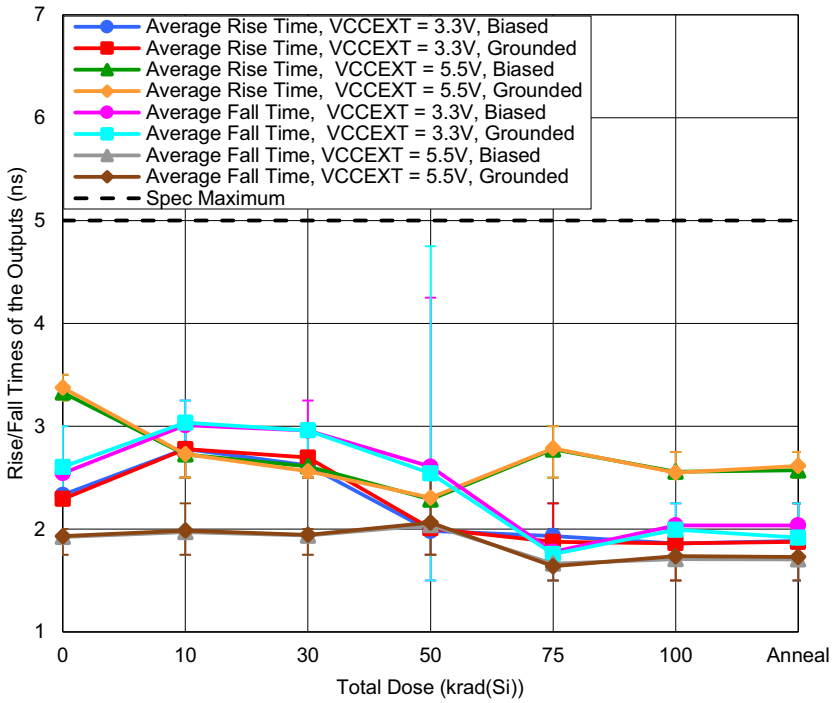

Figure 34. ISL74420SLH average Rise/Fall Times of Outputs (T_{OUT_RF3p3}, T_{OUT_RF5}) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all clocks. The datasheet limit is a maximum of 5ns.

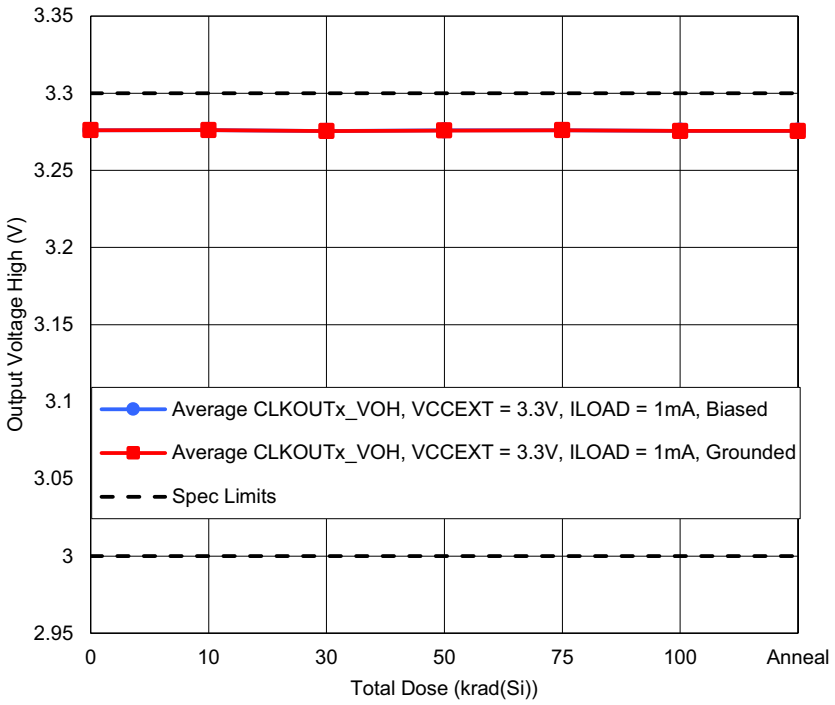

Figure 35. ISL74420SLH average Output Voltage High ($CLKOUTx_{VOH}$) with VCCEXT = 3.3V and I_{LOAD} = 1mA as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all clocks. The datasheet limits are a minimum of 3V and a maximum of 3.3V.

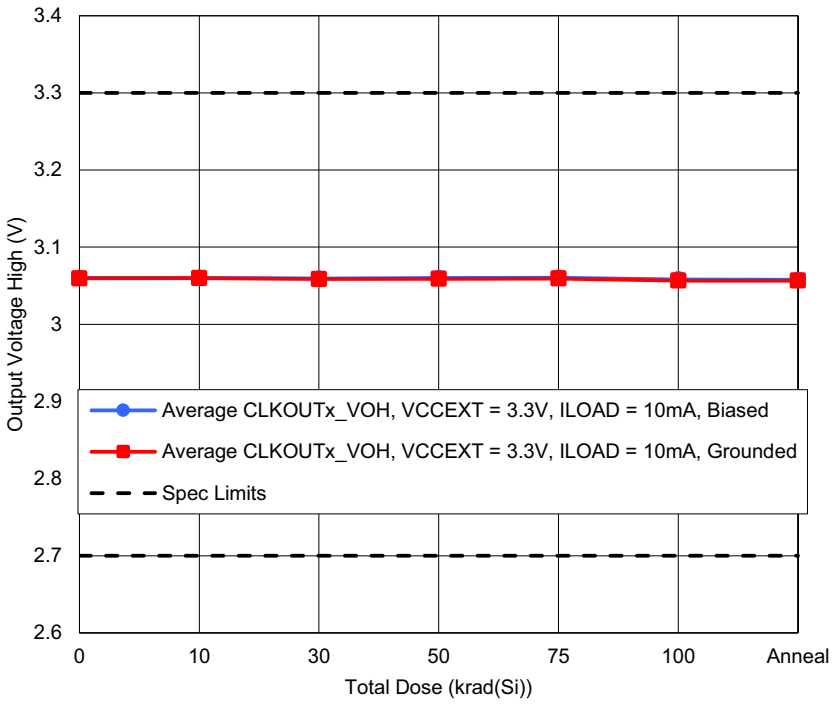

Figure 36. ISL74420SLH average Output Voltage High ($CLKOUTx_{VOH}$) with VCCEXT = 3.3V and I_{LOAD} = 10mA as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all clocks. The datasheet limits are a minimum of 2.7V and a maximum of 3.3V.

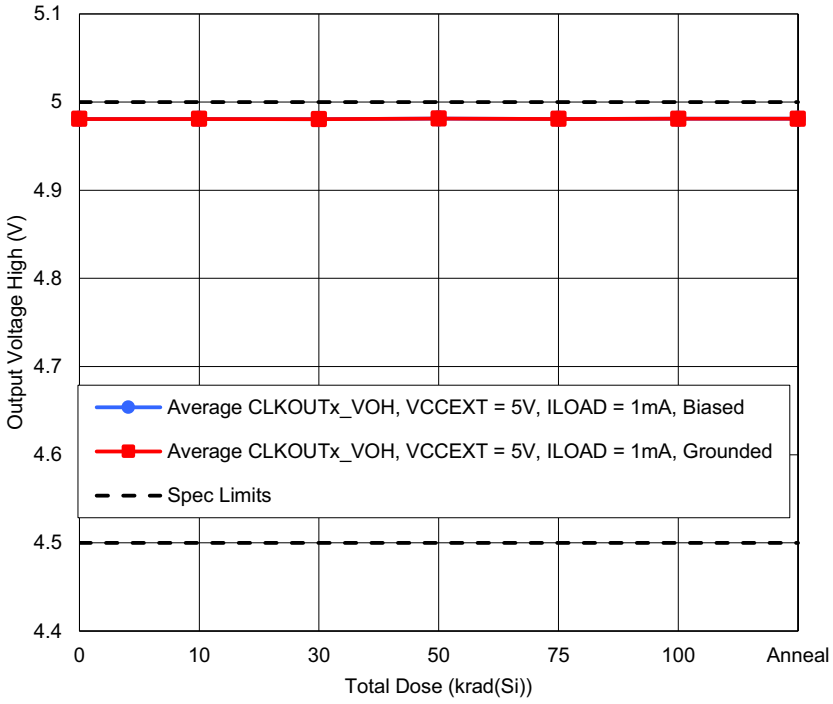

Figure 37. ISL74420SLH average Output Voltage High ($CLKOUTx_{VOH}$) with VCCEXT = 5V and I_{LOAD} = 1mA as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all clocks. The datasheet limits are a minimum of 4.5V and a maximum of 5V.

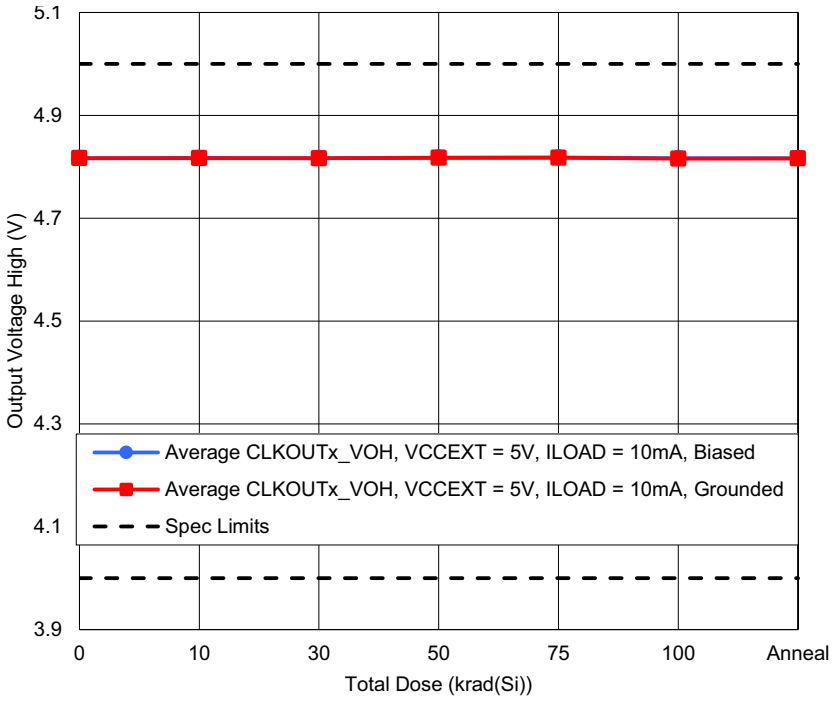

Figure 38. ISL74420SLH average Output Voltage High ($CLKOUTx_{VOH}$) with VCCEXT = 5V and I_{LOAD} = 10mA as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all clocks. The datasheet limits are a minimum of 4V and a maximum of 5V.

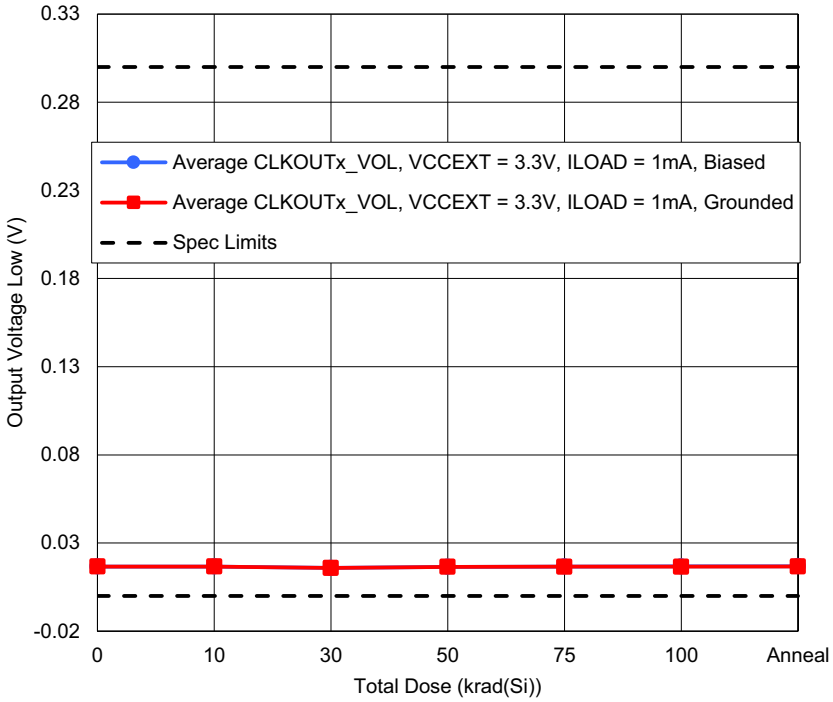

Figure 39. ISL74420SLH average Output Voltage Low ($CLKOUTx_{VOL}$) with VCCEXT = 3.3V and I_{LOAD} = 1mA as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all clocks. The datasheet limits are a minimum of 0V and a maximum of 0.3V.

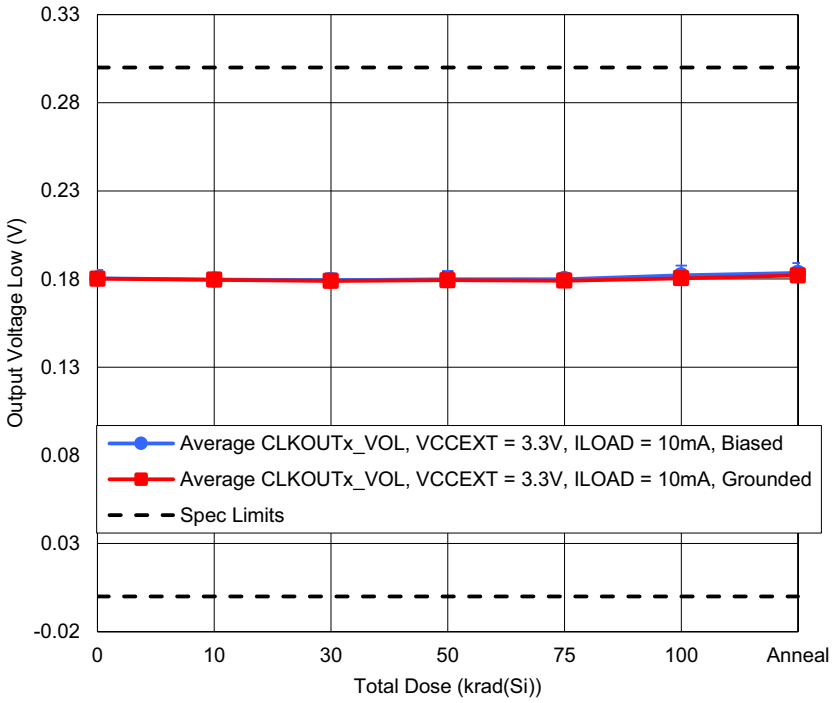

Figure 40. ISL74420SLH average Output Voltage Low ($CLKOUTx_{VOL}$) with VCCEXT = 3.3V and I_{LOAD} = 10mA as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all clocks. The datasheet limits are a minimum of 0V and a maximum of 0.3V.

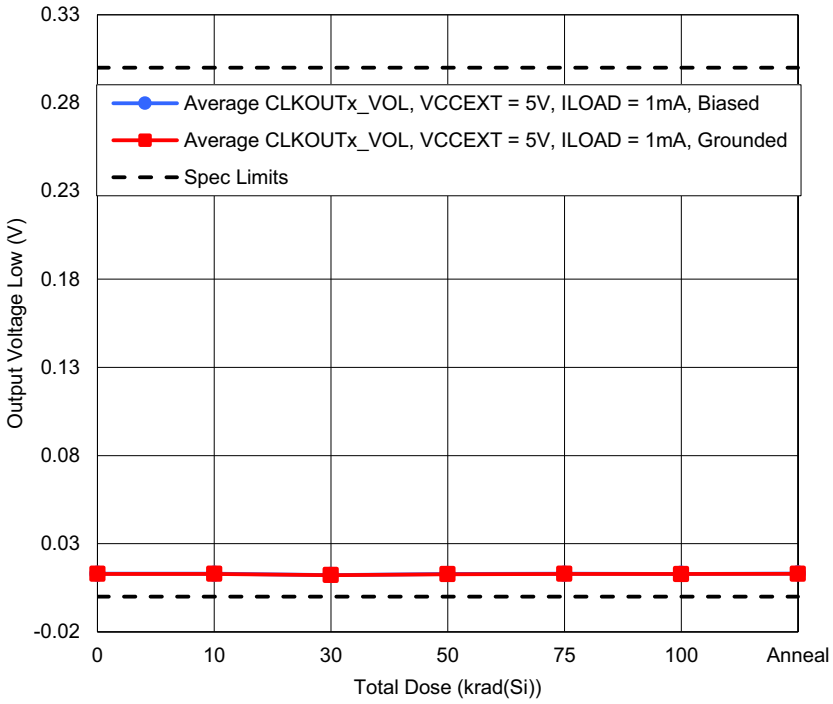

Figure 41. ISL74420SLH average Output Voltage Low ($CLKOUTx_{VOL}$) with VCCEXT = 5V and I_{LOAD} = 1mA as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all clocks. The datasheet limits are a minimum of 0V and a maximum of 0.3V.

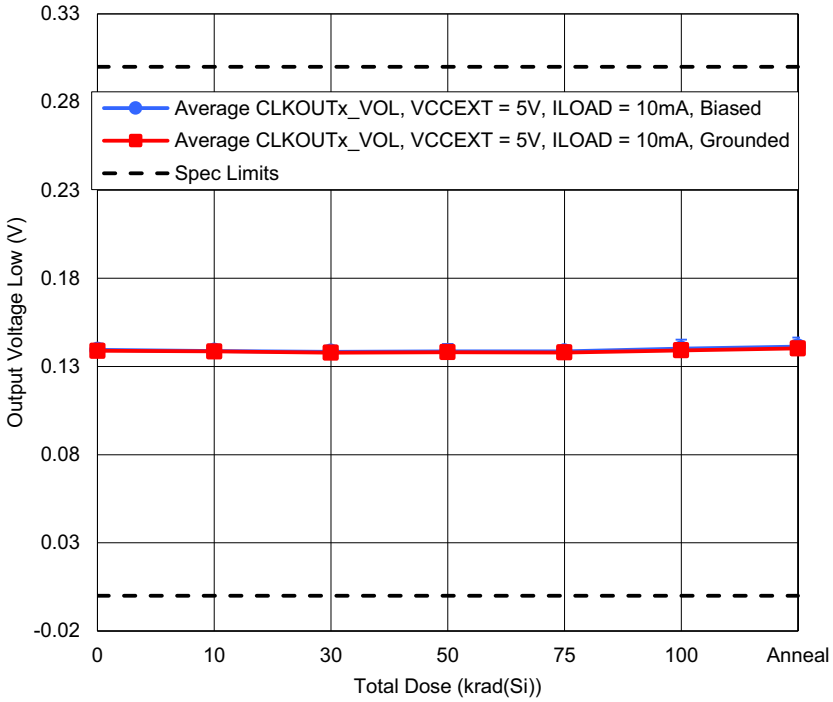

Figure 42. ISL74420SLH average Output Voltage Low ($CLKOUTx_{VOL}$) with VCCEXT = 5V and I_{LOAD} = 10mA as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all clocks. The datasheet limits are a minimum of 0V and a maximum of 0.3V.

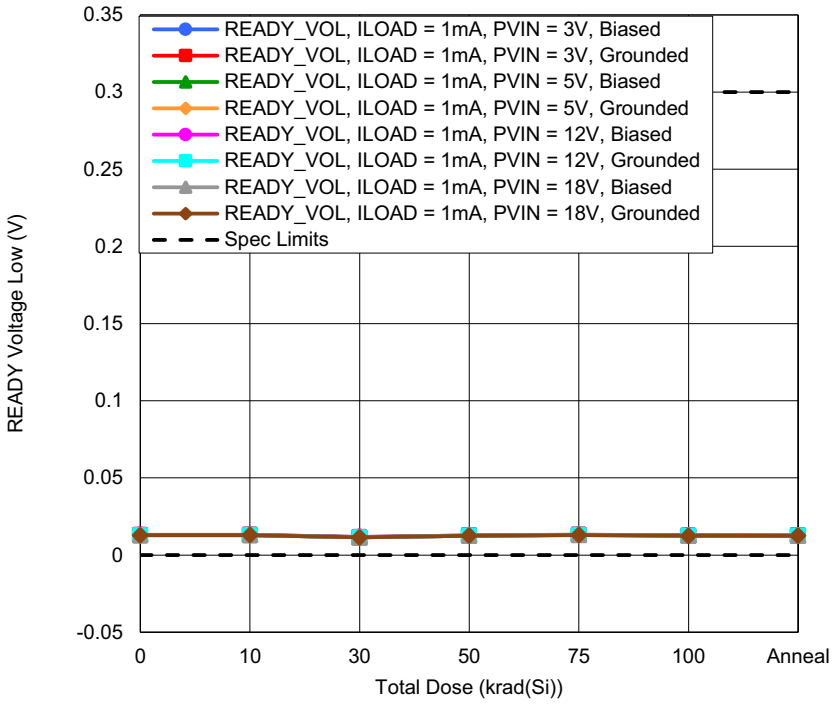

Figure 43. ISL74420SLH READY Voltage Low ($READY_{VOL}$) with I_{LOAD} = 1mA and PVIN = 3V, 5V, 12V, or 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0V and a maximum of 0.3V.

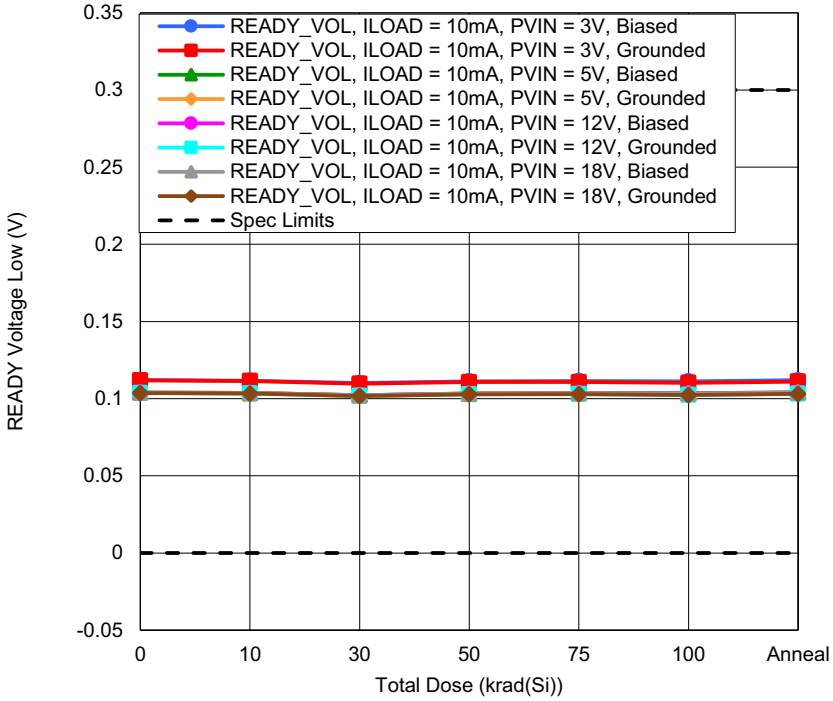

Figure 44. ISL74420SLH READY Voltage Low ($READY_{VOL}$) with I_{LOAD} = 10mA and PVIN = 3V, 5V, 12V, or 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0V and a maximum of 0.3V.

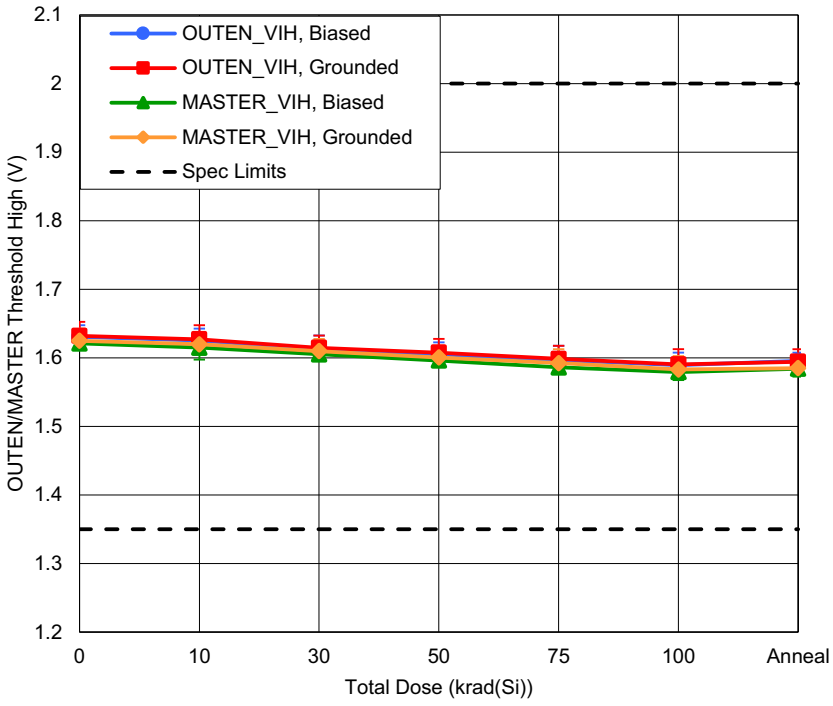

Figure 45. ISL74420SLH OUTEN/MASTER Threshold High ($OUTEN/MASTER_{VIH}$) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 1.35V and a maximum of 2V.

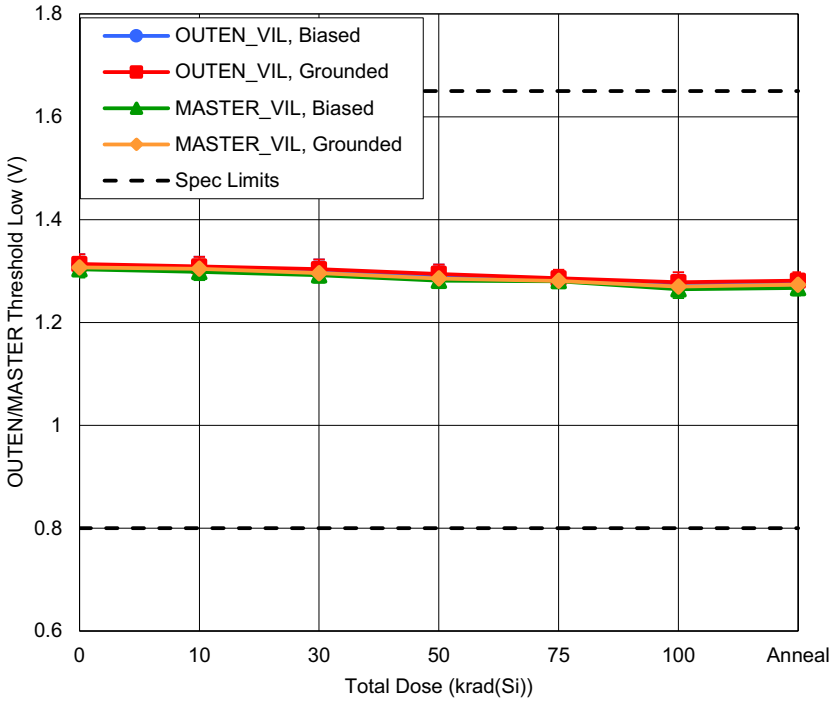

Figure 46. ISL74420SLH OUTEN/MASTER Threshold Low (OUTEN/MASTER$_{VIL}$) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0.8V and a maximum of 1.65V.

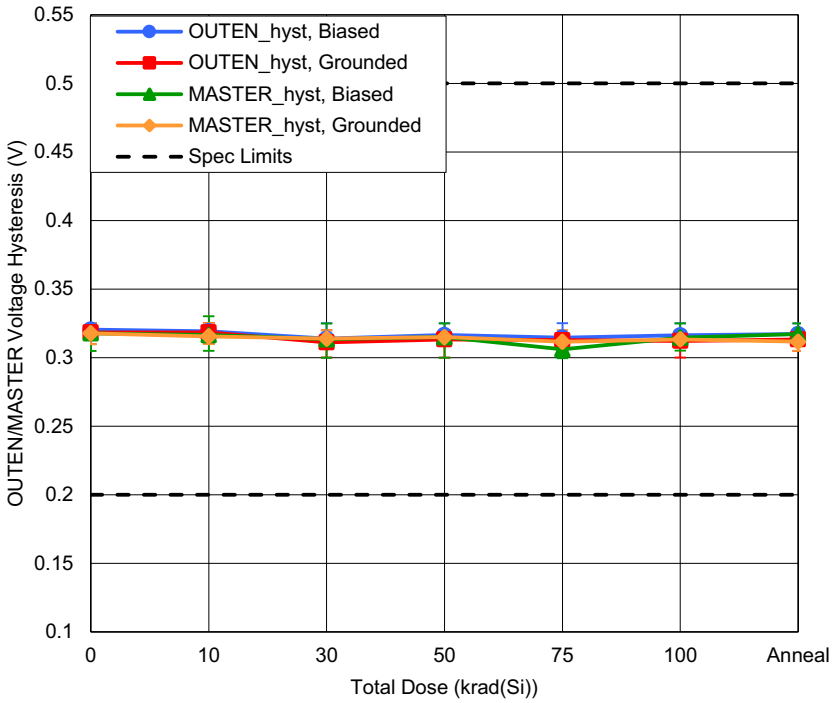

Figure 47. ISL74420SLH OUTEN/MASTER Threshold Hysteresis (OUTEN/MASTER$_{hys}$) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0.2V and a maximum of 0.5V.

3. Discussion and Conclusion

This document reports the results of the LDR TID test of the ISL74420SLH radiation hardened quad clock fanout IC. The irradiation of biased and grounded samples to 100krad(Si) at a LDR of 0.01rad(Si)/s was followed by a 168-hour anneal at 100ºC under bias. All datasheet parameters passed at all downpoints. No evidence of bias dependence was observed.

4. Revision History

Revision	Date	Description
1.00	Jun 20, 2025	Initial release.

Appendix

Table 3 lists the datasheet parameters that are considered indicative of part performance. These parameters are plotted in Figure 3 through Figure 47. All limits are taken from the ISL74420SLH datasheet, which may also have more details on test conditions.

Table 3. ISL74420SLH Datasheet Total Dose Parameters (TA = 25ºC)

Fig.	Parameter	Symbol	Test Conditions	Min	Max	Unit
3	UVLO Rising Threshold	V_{UVLO-R}	PVIN = VCC = VCCEXT	-	2.95	V
	UVLO Falling Threshold	V_{UVLO-F}	PVIN = VCC = VCCEXT	2.65	-	V
4	PVIN Operating Supply Current - Leader Mode 48MHz out	I_{PVIN_OPER1}	CH[0:3]FREQ = Option 0	29	36	mA
5	PVIN Operating Supply Current - Leader Mode 48MHz out with CLKIN	I_{PVIN_OPER2}	CH[0:3]FREQ = Option 0, MASTER = VCC, CLKIN = 48MHz	32	40	mA
6	PVIN Operating Supply Current - Follower Mode	I_{PVIN_OPER3}	CH[0:3] = Option 0, MASTER = GND, CLKIN = 48MHz	24	30	mA
7	PVIN Operating Supply Current - Leader Mode 1MHz out	I_{PVIN_OPER4}	CH[0:3]FREQ = Option 5 (1MHz), CH[0:3]PH = 0°, 90°, 180°, 270°	18	25	mA
8	VCCEXT Supply Current	I_{VCCEXT_MAX}	PVIN = 12V, VCCEXT = 5.5V, CH[0:3]FREQ = Option 0	29	45	mA
9	PVIN Standby Leader Mode Supply Current	I_{PVIN_SB1}	OUTEN = GND, VCCEXT tied to VCC	12	20	mA
10	PVIN Standby Follower Mode Supply Current	I_{PVIN_SB2}	OUTEN = GND, MASTER = GND, CLKIN = GND, VCCEXT tied to VCC	0.5	2	mA
11	VCC Voltage Tolerance (Accuracy)	V_{VCC}	I_{LOAD} = 50mA	3	3.6	V
12	VCC Current Limit	$I_{AVCC-CL}$	VCC = 2.9V, VCCEXT = 3.3V, OUTEN = GND, MASTER = GND, CLKIN = GND	75	130	mA
13	VCC Foldback Current Limit	$I_{AVCC-SC}$	VCC = GND, VCCEXT = 3.3V	40	90	mA
14	Time after Rising PVIN to READY Signal	$T_{PVIN-READY}$	PVIN = step 2V to 4V, CH3FREQ = non-I^2C/SMBus Mode	1.7	2.7	ms
15	Time after OUTEN to CLKOUT with Phase = 0°	$T_{OUTEN-OUT}$	PVIN = 5V, CH[0:3]PH = 0°, OUTEN rising	70	180	ns
			PVIN = 5V, MASTER = GND, CLKIN = 48MHz, CH[0:3]PH = 0°, OUTEN rising	70	180	ns
16	Internal Oscillator Nominal Frequency	InternalOsc_Nom	OSCTUNE = 12.7kΩ, PVIN = VCC = [3V, 3.6V]	46.25	49.25	MHz
17			OSCTUNE = 12.7kΩ, VCC regulating and PVIN = [5V, 12V, 18V]	46.25	49.25	MHz

Table 3. ISL74420SLH Datasheet Total Dose Parameters (TA = 25ºC) (Cont.)

Fig.	Parameter	Symbol	Test Conditions	Min	Max	Unit
18	Internal Oscillator Minimum Frequency	InternalOsc_Min	PVIN = VCC = [3V, 3.6V], OSCTUNE = 26.7kΩ	41.0	46.2	MHz
19			PVIN = VCC = [5V, 12V, 18V], OSCTUNE = 26.7kΩ	41.0	46.2	MHz
20	Internal Oscillator Maximum Frequnecy	InternalOsc_Max	PVIN = VCC = [3V, 3.6V], OSCTUNE = 8.2kΩ	48.5	56.5	MHz
21			PVIN = VCC = [5V, 12V, 18V], OSCTUNE = 8.2kΩ	49.5	56.5	MHz
22	Output Duty Cycle in Leader Mode with Internal Oscillator	M_int_Duty_Cycle	OSCTUNE = 8.2kΩ, CH[0:3]FREQ = Option 1	30	50	%
23	Output Duty Cycle in Leader Mode with CLKIN	M_clkin_Duty_Cycle	OSCTUNE = 12.7kΩ, MASTER = VCC, CLKINfreq = 50MHz, CLKINduty = [40%, 60%] duty cycle, CH[0:3]FREQ = Option 1	30	50	%
24	Output Duty Cycle in Follower Mode	S_Duty_Cycle	VCCEXT = [VCC, 5.5V] MASTER = GND, CLKINfreq = 30MHz, CLKIN duty = 30% duty cycle, CH[0:3]FREQ = Option 0	20	40	%
25			VCCEXT = [VCC, 5.5V] MASTER = GND, CLKINfreq = 30MHz, CLKIN duty = 65% duty cycle, CH[0:3]FREQ = Option 0	55	75	%
26			VCCEXT = [VCC, 5.5V] MASTER = GND, CLKINfreq = 50MHz, CLKIN duty = 40% duty cycle, CH[0:3]FREQ = Option 1	30	50	%
27			VCCEXT = [VCC, 5.5V] MASTER = GND, CLKINfreq = 50MHz, CLKIN duty = 60% duty cycle, CH[0:3]FREQ = Option 1	30	50	%
28	Duty Cycle of a Divided Clock	div_Duty_Cycle	VCCEXT = VCC CH[0:3]FREQ = Option 3 (4MHz)	47	50	%
29			VCCEXT = 5.5V CH[0:3]FREQ = Option 3 (4MHz)	47	50	%
30	Output-to-Output Skew between CLKOUTx's with Equal Frequency and Phase	$CLKOUTx_{SKEW48M}$	MASTER = GND, CLKIN = 48MHz, CH[0:3]FREQ = Option 0	-1.5	1.5	ns

Table 3. ISL74420SLH Datasheet Total Dose Parameters (TA = 25ºC) (Cont.)

Fig.	Parameter	Symbol	Test Conditions	Min	Max	Unit
31	Output-to-Output Skew between CLKOUTx's with Equal Frequency and Phase	$CLKOUTx_{SKEW1M}$	MASTER = GND, CLKIN = 48MHz, CH[0:3]FREQ = Option 5 (1MHz), equal phase	-6	6	ns
32	Output-to-Output Skew Between CLKOUTx's with Equal Frequency and Different Phase	$CLKOUTx_{SKEW1M4P}$	MASTER = GND, CLKIN = 48MHz, CH[0:3]FREQ = Option 5 (1MHz), CH[0:3]PH = 0°, 90°, 180°, 270°	-7	7	ns
33	CLKIN-to-CLKOUT Follower Mode Propagation Delay	$CLK_{PROPDELAY}$	MASTER = GND, CH[0:3] FREQ = Option 0, CLKIN = 1MHz	20	40	ns
34	Rise /Fall Times of Outputs	T_{OUT_RF3p3}	PVIN = 12V, MASTER = GND, CLKIN = 1MHz, CH[0:3]FREQ = Option 0, VCCEXT = 3.3V, Measured 80%/20%	-	5	ns
		T_{OUT_RF5}	PVIN = 12V, MASTER = GND, CLKIN = 1MHz, CH[0:3]FREQ = Option 0, VCCEXT = 5.5V, Measured 80%/20%	-	5	ns
35	Output Voltage High	$CLKOUTx_{VOH}$	PVIN = 12V, MASTER = GND, CLKIN = 3.3V, CH[0:3]FREQ = Option 0 VCCEXT = 3.3V, I_{LOAD} = 1mA	3	3.3	V
36			PVIN = 12V, MASTER = GND, CLKIN = 3.3V, CH[0:3]FREQ = Option 0 VCCEXT = 3.3V, I_{LOAD} = 10mA	2.7	3.3	V
37			PVIN = 12V, MASTER = GND, CLKIN = 3.3V, CH[0:3]FREQ = Option 0 VCCEXT = 5V, I_{LOAD} = 1mA	4.5	5	V
38			PVIN = 12V, MASTER = GND, CLKIN = 3.3V, CH[0:3]FREQ = Option 0 VCCEXT = 5V, I_{LOAD} = 10mA	4	5	V

Table 3. ISL74420SLH Datasheet Total Dose Parameters (TA = 25ºC) (Cont.)

Fig.	Parameter	Symbol	Test Conditions	Min	Max	Unit
39	Output Voltage Low	$CLKOUTx_{VOL}$	PVIN = 12V, MASTER = GND, CLKIN = GND, CH[0:3]FREQ = Option 0 VCCEXT = 3.3V, I_{LOAD} = 1mA	0	0.3	V
40			PVIN = 12V, MASTER = GND, CLKIN = GND, CH[0:3]FREQ = Option 0 VCCEXT = 3.3V, I_{LOAD} = 10mA	0	0.3	V
41			PVIN = 12V, MASTER = GND, CLKIN = GND, CH[0:3]FREQ = Option 0 VCCEXT = 5V, I_{LOAD} = 1mA	0	0.3	V
42			PVIN = 12V, MASTER = GND, CLKIN = GND, CH[0:3]FREQ = Option 0 VCCEXT = 5V, I_{LOAD} = 10mA	0	0.3	V
43	READY Voltage Low	$READY_{VOL}$	I_{LOAD} = 1mA	0	0.3	V
44			I_{LOAD} = 10mA	0	0.3	V
45	OUTEN/MASTER Threshold High	$OUTEN/MASTER_{VIH}$	-	1.35	2	V
46	OUTEN/MASTER Threshold Low	$OUTEN/MASTER_{VIL}$	-	0.8	1.65	V
47	OUTEN/MASTER Voltage Hysteresis	$OUTEN/MASTER_{hys}$	-	0.2	0.5	V

Related Literature

For a full list of related documents, visit our website:

- ISL74420SLH device page
- MIL-STD-883 test method 1019

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