ISL73849SLH

Single Event Effects (SEE) Testing of the ISL73849SLH Single/Dual Phase Current Mode PWM Controller

Introduction

The intense proton and heavy-ion environment encountered in space applications can cause a variety of Single Event Effects (SEE) in electronic circuitry, including Single Event Upset (SEU), Single Event Transient (SET), Single Event Functional Interrupt (SEFI), Single Event Latch-Up (SEL), Single Event Gate Rupture (SEGR), and Single Event Burnout (SEB). SEE can lead to system-level performance issues including disruption, degradation, and destruction. For predictable and reliable space system operation, individual electronic components should be characterized to determine their SEE response. This report discusses the results of the SEE testing performed on the ISL73849SLH product. The ISL73849SLH is offered with radiation assurance screening to 75krad(Si) at 10mrad(Si)/s.

SEE Summary

SEE testing was performed with normal incidence gold and silver for a LETs of 86.3MeV·cm^2/mg and 45.8MeV·cm^2/mg at the surface of the device. The LET of the gold ions in the active silicon layer of the device ranged from 88.4MeV·cm^2/mg to 90.2MeV·cm^2/mg. The LET of the silver ions in the active silicon layer of the device ranged from 47.9MeV·cm^2/mg to 49.8MeV·cm^2/mg.

The ISL73849SLH proved to be free of Destructive Single Event Effects (DSEE) at 125°C under the following maximum parameter set: V_{DD} = 23V, V_{CC} = 6.3V, and V_{ISEN} = 13.5V at 86MeV·cm^2/mg and V_{DD} = 25V, V_{CC} = 6.7V, and V_{ISEN} = 13.5V at 46MeV·cm^2/mg.

The regulator exhibited SET events where V_{OUT} deviated beyond ±2.5% of its nominal value with a worst-case cross-section of 920µm^2 at 86MeV·cm^2/mg. The maximum deviation in V_{OUT} at 86MeV·cm^2/mg was 3.55%. The maximum amount of time until V_{OUT} returned to within ±2.5% of its nominal value at 86MeV·cm^2/mg was 16ns.

A V_{OUT} SEFI was defined as an event in which FLTb pulled low and there was a loss of regulation in V_{OUT}. During a SEFI, V_{OUT} regulation is restored with a spontaneous soft start. A total of 4 SEFIs were observed during SET testing for an average cross-section of 2.5µm^2 per test condition at 86MeV·cm^2/mg. FLTb was low for approximately 10ms during SEFIs. SALERT recovered with the CLEAR_FAULT PMBus command.

The on-chip analog to digital converter (ADC) exhibited SETs during telemetry readings. The SETs in the readings were up to full scale; however, they only lasted a single sample. Therefore, these SETs can be mitigated by averaging multiple samples.

The ADC also exhibited one SEFI event during a total fluence of 6.4E8ions/cm^2 at 86MeV·cm^2/mg for a total cross-section of 0.16µm^2. During this event, the ADC remained in a busy state and could not sample. The event lasted for 39 consecutive samples on each recorded parameter, and the ADC read 8191 decimal for each telemetry parameter. The device did not exhibit ADC SEFIs at 46MeV·cm^2/mg. If an ADC SEFI occurs, a power cycle is recommended to restore telemetry functionality.

The PMBus configuration registers did not exhibit any SEUs during testing at 86MeV·cm^2/mg.

Product Description

The ISL73849SLH is a PMBUS based synchronous buck controller that can operate as a single or dual-phase controller. The device works with the ISL73041SEH (half bridge GaN FET driver) to generate point-of-load voltage rails for commercial space applications.

It accepts an input voltage range of 4.5V to 19V with a programmable output switching frequency between 250kHz and 1.5MHz with a single resistor. The output can regulate a voltage downwards of 200mV and is limited on the top end by the minimum off-time and selected switching frequency.

The wide input voltage range makes it a suitable power supply option for a high current FPGA core and other general purpose power solutions. The ISL73849SLH uses current mode modulation, which simplifies loop compensation and provides excellent power supply rejection. Additionally, the output is remotely sensed to compensate for any voltage drop in the load conditions. All of this put together results in a robust power supply solution that requires minimal components while achieving high current density.

The ISL73849SLH also features a tri-level output, which provides excellent protection against faults by driving a mid-scale voltage to signal the power stage to enter a Hi-Z condition. Control, Telemetry, and Fault Reporting through PMBUS provides for an easy interface with an MCU.

The ISL73849SLH operates across the military temperature range from -55°C to +125°C and is available in a 24-pin hermetically sealed Ceramic Dual Flatpack (CDFP) package or in die form. Figure 1 shows the pin assignments of the ISL73849SLH and Table 1 displays the pin descriptions.

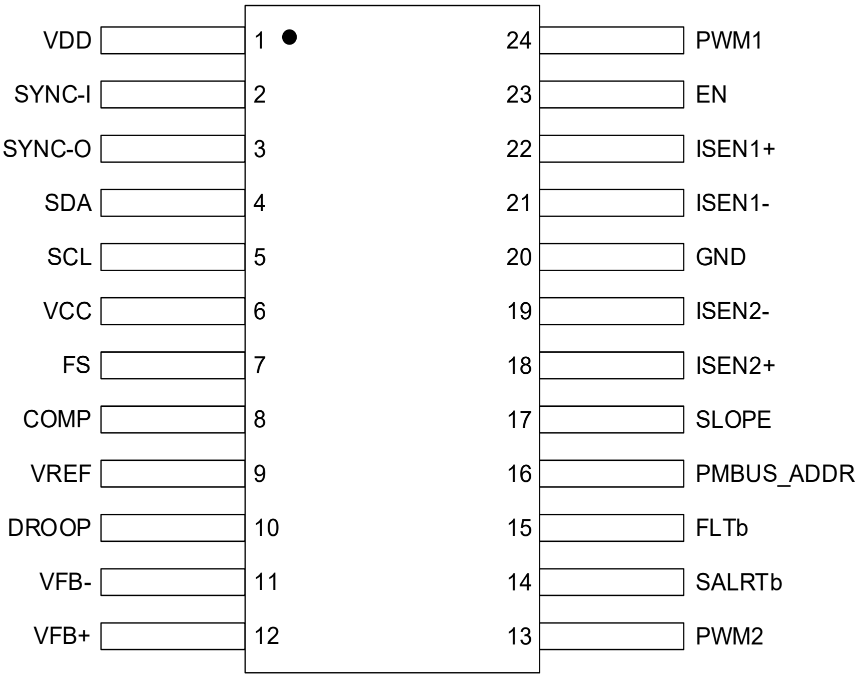

Figure 1. ISL73849SLH Pin Assignments

Table 1. ISL73849SLH Pin Descriptions

Pin Number	Pin Name	Description
1	VDD	The power supply input to the IC. The voltage range on this pin is 4.5V to 19V. Connect 2.2µF and 0.1µF ceramic capacitors from this pin to GND.
2	SYNC-I	This pin is an input that accepts 2x the required output switching frequency (regardless of single or dual phase). Internally the IC divides the clock down to get 2 clocks 180º from each other for each phase.
3	SYNC-O	This pin can output either 1x or 2x the output switching frequency depending on the loading present on the pin during power up (before soft start). When outputting 1x, the SYNC-O is 180º out of phase with phase 1 clock. The 2x SYNC-O output is in phase with the SYNC-I.
4	SDA	PMBus Serial Data Bus
5	SCA	PMBus Serial Data Clock
6	VCC	5V Output of internal LDO for analog circuitry. Connect a 1µF ceramic capacitor from this pin to GND.
7	FS	This pin sets the frequency for the internal oscillator between 0.5MHz and 3MHz. This sets the PWM outputs between 0.25MHz and 1.5MHz for each phase. When FS is tied to VCC the oscillator switching frequency (f_{OSC}) is 1MHz. To adjust the PWM outputs between 0.25MHz and 1.5MHz, use a 13.7kΩ to 205kΩ resistor between FS and GND. If SYNC-I is being used to sync to an external clock, FS needs to be set to frequency 15% less than the external clock.

Table 1. ISL73849SLH Pin Descriptions (Cont.)

Pin Number	Pin Name	Description
8	COMP	The output of the error amplifier. Connect a resistor and capacitor in series to ground for type-2 compensation adjustment. For type-3 compensation add an additional capacitor in parallel with the type-2 series RC component.
9	VREF	Output for the internal voltage reference. Connect a resistor between VREF and DROOP to enable droop regulation. Otherwise to disable droop regulation, short the VREF and DROOP pins together. Connect a 47nF ceramic capacitor from this pin to GND.
10	DROOP	This pin is a current mirrored version of the output of the current-sense amplifier output (sum of both phases). This output can be tied to the VREF pin through a resistor to enable droop regulation. The voltage created by the mirrored current and the resistor between VREF and DROOP sets the droop level.
11	VFB-	This pin is the negative input for differential voltage feedback.
12	VFB+	This pin is the positive input for differential voltage feedback.
13	PWM2	This pin is the PWM output for the secondary phase. Place100kΩ to GND on this pin.
14	SALRTb	This pin serves as the SALRTb pin for the PMBus. Pull up this pin to a maximum of 5.5V via 10kΩ.
15	FLTb	This pin is used to sequence the startup between the ISL73849SLH and compatible drivers. On the ISL73849SLH, this pin operates as a bi-directional I/O during power up (before soft start) and as an input while switching (during and after soft start). A logic LOW on this pin indicates that either the ISL73849SLH or driver has encountered a fault or is not ready to start switching. A logic HIGH indicates that there are no faults for either device. Because FLTb is an open-drain output, use a 4.99kΩ typical pull-up resistor to VCC for a proper HIGH level.
16	PMBUS_ADDR	This pin sets six unique PMBus addresses. When the PMBUS_ADDR pin is tied to GND, it is 0x11. The remaining addresses are set by using a resistor to GND: 0x12 (37.5kΩ), 0x13 (112.5kΩ), 0x14 (62.5kΩ), 0x16 (150kΩ) or 0x18 (87.5kΩ).
17	SLOPE	This pin is used to adjust the slope compensation of the ISL73849SLH. Place a resistor in the range of 25kΩ to 100kΩ to adjust slope compensation.
18	ISEN2+	This pin is the positive input for the secondary phase current-sense amplifier.
19	ISEN2-	This pin is the negative input for the secondary phase current-sense amplifier.
20	GND	This is the ground reference for the ISL73849SLH. This pin is tied to the package seal ring (lid).
21	ISEN1-	This pin is the negative input for the primary phase current-sense amplifier.
22	ISEN1+	This pin is the positive input for the primary phase current-sense amplifier.
23	EN	This pin is the chip enable for the ISL73849SLH.
24	PWM1	This pin is the PWM output for the primary phase. Place 100kΩ to GND on this pin.
-	Lid	The lid is electrically connected to pin 20 (GND).

Contents

1. SEE Testing

1.1 Objective

The testing was intended to find the limits of the power input (V_{DD}), linear regulator output (V_{CC}), and the common-mode voltage on the ISEN pins (V_{ISEN}) set by the onset of Destructive Single Event Effects (DSEE) at a LET of 86.3MeV·cm^2/mg (normal incidence gold) and 45.8MeV·cm^2/mg (normal incidence silver). Additional testing was intended to identify and quantify SETs in the output voltage, SETs in the ADC, SEUs in the PMBus configuration registers, and SEFIs. The SET and SEFI studies also consisted of irradiation with normal incidence gold (86.3MeV·cm^2/mg) and normal incidence silver (45.8MeV·cm^2/mg).

1.2 Facility

SEE testing was done at the Texas A&M University (TAMU) Radiation Effects Facility of the Cyclotron Institute in College Station, Texas. This facility is coupled to a K500 superconducting cyclotron that can supply a wide range of ion species and flux. The SEE testing in this report was conducted in April 2025.

2. Results

2.1 DSEE Results

DSEE testing consisted of three components: VDD DSEE testing, VCC DSEE testing, and ISEN DSEE testing. For all three components, a 22nF soft-start capacitor was used and the switching frequency was 500kHz.

The schematic for the schematic for the SEE board is shown in Figure 2.

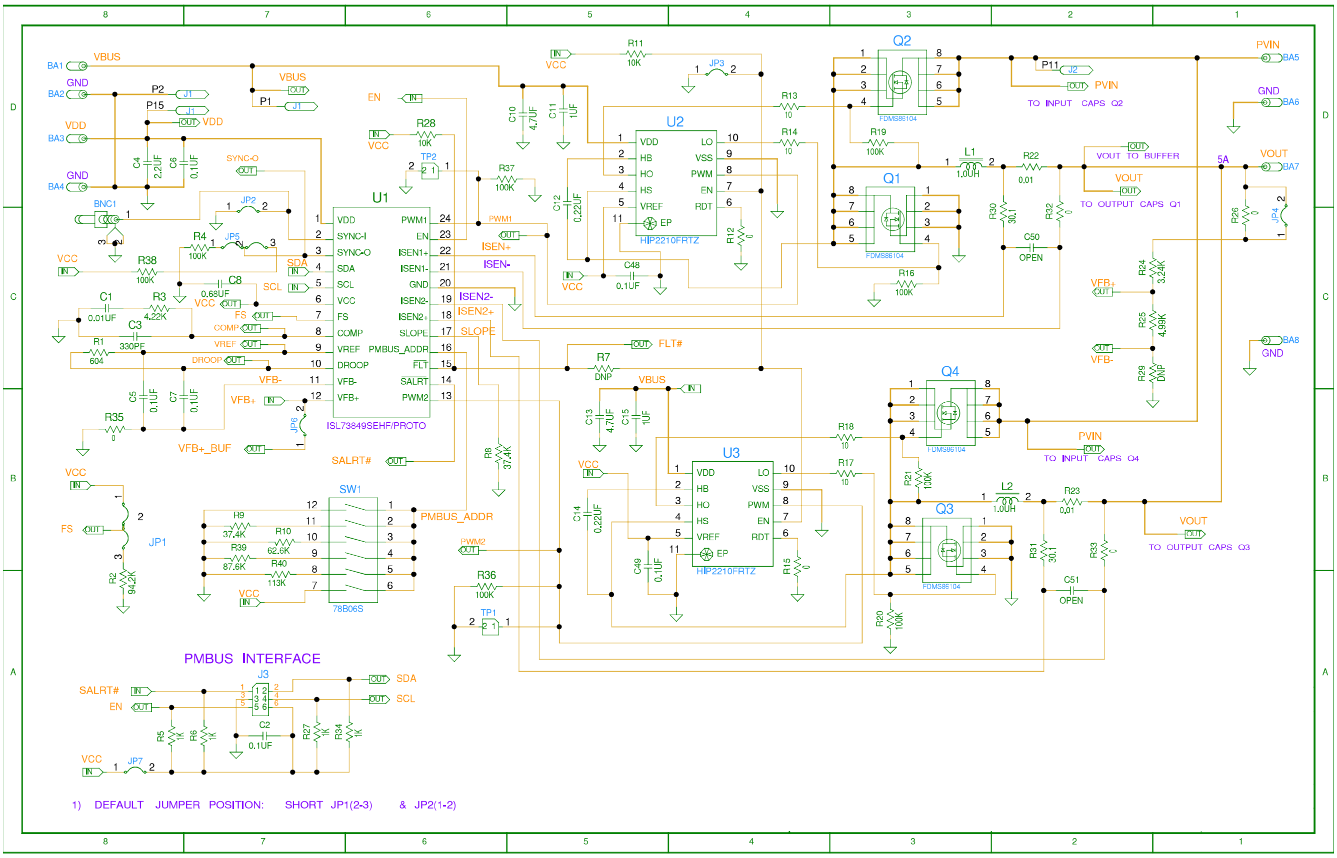

Figure 2. SEE Schematic

The purpose of the first component of DSEE testing was to find the maximum value of the power input voltage (V_{DD}) set by the onset of DSEEs at a die temperature of 125°C. For VDD DSEE testing, the DUT was operated in dual phase with a 5A load. VBUS was set to 6V. PVIN was set to 5V. VCC was bypassed to the PCB ground plane with a 0.68µF capacitor. The SLOPE resistor was 37.4kΩ. The RC COMP network consisted of a 4.22kΩ resistor and a 10nF capacitor. A 1µH output inductor and 440µF of output capacitance were used. VOUT was set to 1V. VDD was initially set to 23V and was incremented by 1V after each run up to a maximum voltage of 25V. Testing ended when the device exhibited a DSEE or when VDD reached 25V. The device was considered to have exhibited a DSEE if V_{OUT} changed by ±1% or the VDD current changed by ±2%.

The purpose of the second component of DSEE testing was to find the maximum value of the linear regulator output (V_{CC}) set by the onset of DSEEs at a die temperature of 125°C. For VCC DSEE testing, the VCC supply was overdriven so that the internal regulator from VDD was inactive, and the VCC current could be monitored directly. The DUT was operated in dual phase with a 5A with an electronic load in constant resistance mode. VBUS was set to 12V. PVIN was set to 5V. VDD was tied to VCC. The SLOPE resistor was 37.4kΩ. The RC COMP network consisted of a 4.22kΩ resistor and a 10nF capacitor. A 1.5µH output inductor and 220µF of output capacitance were used. VOUT was set to 1V. VCC was initially set 6.1V and was incremented by 0.2V after each run to a maximum voltage of 6.5V. Testing ended when the device exhibited a DSEE or when VCC reached 6.5V. The device was considered to have exhibited a DSEE if VOUT changed by ±2% or the VCC current changed by ±5%.

The purpose of the third component of DSEE testing was to find the maximum common-mode value of the input to the current-sense amplifier (ISEN) set by the onset of DSEEs at a die temperature of 125°C. The DUT was operated in dual phase with a 5A with an electronic load in constant resistance mode. VBUS was set to 6V. PVIN was set to 25V. VDD was tied to VCC, and VCC was set to 5V. The SLOPE resistor was 76.8kΩ. The RC COMP network consisted of a 4.22kΩ resistor and a 47nF capacitor. A 10µH output inductor and 100µF of output capacitance were used. The common-mode voltage on ISEN was adjusted by changing VOUT. Initially, VOUT was set to 12V and was incremented by 0.5V after each run to a maximum voltage of 13.5V. Testing ended when the device exhibited a DSEE or when VCC reached 13.5V. The device was considered to have exhibited a DSEE if VOUT changed by ±2% or the VDD current changed by ±5%.

2.1.1 VDD DSEE Results at 86MeV·cm^2/mg

The results of PVIN DSEE testing are displayed in Table 2. Two devices exhibited DSEEs with V_{DD} = 24V, therefore, the device should be operated with a maximum value of V_{DD} = 23V to be robust against DSEE at 86MeV·cm^2/mg.

Table 2. ISL73849SLH VDD DSEE Test Results at 86MeV·cm^2/mg

V_{DD} (V)	DUT #	Result	V_{OUT} (±1%)			I_{VDD} (±2%)		
			Pre (V)	Post (V)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)
23	1	Pass	0.957	0.955	-0.21	20.10	20.10	0.00
	2	Pass	0.957	0.954	-0.31	20.20	20.20	0.00
	3	Pass	0.960	0.961	0.10	20.04	20.05	0.05
	4	Pass	0.957	0.955	-0.21	20.50	20.55	0.24
24	1	Fail	0.957	0.954	-0.31	20.10	0.02	-99.9
	2	Pass	0.954	0.953	-0.11	20.20	19.90	-1.49
	3	Pass	0.961	0.955	-0.62	20.05	20.30	1.25
	4	Fail	0.956	0.00	-100	20.56	0.02	-99.9
25	1	-	-	-	-	-	-	-
	2	Pass	0.953	0.954	0.11	20.03	20.10	0.35
	3	Pass	0.956	0.955	-0.11	20.30	20.40	0.49
	4	-	-	-	-	-	-	-

2.1.2 VCC DSEE Results at 86MeV·cm^2/mg

The results of VCC DSEE testing are displayed in Table 3. All four devices exhibited DSEEs with V_{CC} = 6.5V; therefore, the device should be operated with a maximum value of V_{CC} = 6.3V to be robust against DSEE at 86MeV·cm^2/mg.

Table 3. ISL73849SLH VCC DSEE Test Results at 86MeV·cm^2/mg

VCC (V)	DUT #	Result	V_{OUT} (±1%)			I_{VCC} (±5%)		
			Pre (V)	Post (V)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)
6.1	5	Pass	0.960	0.960	0.00	25.27	25.30	0.12
	6	Pass	0.959	0.959	0.00	24.98	25.10	0.48
	7	Pass	0.966	0.963	-0.31	25.23	25.16	-0.28
	8	Pass	0.960	0.958	-0.21	25.64	25.80	0.62
6.3	5	Pass	0.959	0.963	0.42	26.77	26.86	0.32
	6	Pass	0.958	0.959	0.10	26.56	26.46	-0.38
	7	Pass	0.962	0.963	0.10	26.66	26.91	0.92
	8	Pass	0.956	0.962	0.63	27.40	27.41	0.04
6.5	5	Fail	0.962	0.978	1.67	28.57	64.89	127.1
	6	Fail	0.957	1.014	5.96	28.14	57.60	104.7
	7	Fail	0.961	0.962	0.10	28.63	38.42	34.20
	8	Fail	0.962	0.977	1.56	29.20	56.10	92.12

2.1.3 ISEN DSEE Results at 86MeV·cm^2/mg

The results of ISEN DSEE testing are displayed in Table 4. All four DUTs passed at all voltages, therefore, the device should be operated with a maximum value of V_{ISEN} = 13.5V to be robust against DSEE at 86MeV·cm^2/mg.

Table 4. ISL73849SLH VCC DSEE Test Results at 86MeV·cm^2/mg

VOUT/ V_{ISEN} (V)	DUT #	Result	V_{OUT} (±1%)			I_{VDD}(±5%)		
			Pre (V)	Post (V)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)
12.0	9	Pass	12.016	12.054	0.32	18.57	18.62	0.27
	10	Pass	12.017	12.067	0.42	18.64	18.63	-0.05
	11	Pass	12.050	12.015	-0.29	18.59	18.69	0.57
	12	Pass	12.022	11.920	-0.85	18.62	18.65	0.16
12.5	9	Pass	12.500	12.404	-0.77	18.64	18.53	-0.59
	10	Pass	12.519	12.504	-0.12	18.66	18.65	-0.05
	11	Pass	12.553	12.594	0.33	18.71	18.77	0.35
	12	Pass	12.527	12.502	-0.20	18.68	18.16	-2.78
13.0	9	Pass	13.033	13.066	0.25	18.55	18.45	-0.54
	10	Pass	13.047	13.032	-0.12	18.71	18.69	-0.12
	11	Pass	13.063	13.025	-0.29	18.79	18.70	-0.46
	12	Pass	13.050	13.006	-0.34	18.64	18.60	-0.22
13.5	9	Pass	13.542	13.459	-0.61	18.33	18.35	0.11
	10	Pass	13.508	13.480	-0.21	18.57	18.70	0.70
	11	Pass	13.501	13.507	0.04	18.57	18.64	0.39
	12	Pass	13.522	13.600	0.58	18.50	18.48	-0.11

DSEE testing indicates that the device should be operated with the following maximum parameter set to be robust against DSEE: V_{DD} = 23V, V_{CC} = 6.3V, and V_{ISEN} = 13.5V at 86MeV·cm^2/mg.

2.1.4 VDD DSEE Results at 46MeV·cm^2/mg

The results of VDD DSEE testing are displayed in Table 5. None of the devices exhibited DSEEs; therefore, the device should be operated with a maximum value of V_{DD} = 25V to be robust against DSEE at 46MeV·cm^2/mg.

Table 5. ISL73849SLH VDD DSEE Test Results at 46MeV·cm^2/mg

VDD (V)	DUT #	Result	V_{OUT} (±1%)			I_{VDD} (±2%)		
			Pre (V)	Post (V)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)
23	31	Pass	0.967	0.968	0.10	23.00	23.00	0.00
	32	Pass	0.963	0.964	0.10	22.00	22.00	0.00
	33	Pass	0.965	0.967	0.21	24.00	24.00	0.00
	34	Pass	-	-	-	-	-	-
24	31	Pass	0.968	0.968	0.00	23.00	24.00	4.35
	32	Pass	0.963	0.963	0.00	22.00	23.00	4.55
	33	Pass	0.967	0.967	0.00	24.00	24.00	0.00
	34	Pass	-	-	-	-	-	-
25	31	Pass	0.968	0.965	-0.31	24.00	24.00	0.00
	32	Pass	0.963	0.963	0.00	23.00	23.00	0.00
	33	Pass	0.967	0.968	0.10	24.00	24.00	0.00
	34	Pass	0.968	0.968	0.00	23.00	23.00	0.00

2.1.5 VCC DSEE Results at 46MeV·cm^2/mg

The results of VCC DSEE testing are displayed in Table 6. None of the devices exhibited DSEEs, therefore, the device should be operated with a maximum value of V_{CC} = 6.7V to be robust against DSEE at 46MeV·cm^2/mg.

Table 6. ISL73849SLH VCC DSEE Test Results at 46MeV·cm^2/mg

VCC (V)	DUT #	Result	V_{OUT} (±1%)			I_{VCC} (±5%)		
			Pre (V)	Post (V)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)
6.1	35	Pass	0.971	0.969	-0.21	26.41	25.52	-3.37
	36	Pass	-	-	-	-	-	-
	37	Pass	-	-	-	-	-	-
	38	Pass	-	-	-	-	-	-
6.3	35	Pass	0.967	0.968	0.10	27.04	27.07	0.07
	36	Pass	0.973	0.972	-0.10	26.98	26.90	-0.30
	37	Pass	0.967	0.965	-0.21	27.51	27.46	-0.18
	38	Pass	0.971	0.973	0.21	27.16	27.07	-0.33
6.5	35	Pass	0.965	0.967	0.21	28.82	28.82	0.00
	36	Pass	0.969	0.969	0.00	28.66	28.61	-0.17
	37	Pass	0.962	0.961	-0.10	29.26	29.20	-0.21
	38	Pass	0.970	0.970	0.00	28.85	28.84	-0.04

Table 6. ISL73849SLH VCC DSEE Test Results at 46MeV·cm²/mg (Cont.)

VCC (V)	DUT #	Result	V_{OUT} (±1%)			I_{VCC} (±5%)		
			Pre (V)	Post (V)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)
6.7	35	Pass	0.963	0.961	-0.21	30.80	30.80	0.00
	36	Pass	0.966	0.966	0.00	30.65	30.62	-0.10
	37	Pass	0.957	0.958	0.10	31.28	31.18	-0.32
	38	Pass	0.965	0.966	0.10	30.90	30.85	-0.16

2.1.6 ISEN DSEE Results at 46MeV·cm²/mg

Since the ISL73849SLH passed ISEN DSEE testing at the highest testing voltage at 86MeV·cm²/mg, the testing was not repeated at 46MeV·cm²/mg. The device should be operated with a maximum value of V_{ISEN} = 13.5V to be robust against DSEE at 46MeV·cm²/mg.

DSEE testing indicates that the device should be operated with the following maximum parameter set to be robust against DSEE: V_{DD} = 25V, V_{CC} = 6.7V, and V_{ISEN} = 13.5V at 46MeV·cm²/mg.

2.2 SET and SEFI Results

For SET testing, devices were tested under eight different test conditions (TCs) as given in Table 7. The ISL73849SLH was operated at 500kHz for four of the configurations and was operated at 1MHz for the other four configurations. The output inductor was 1µH for 500kHz operation and it was 0.56µH for 1MHz operation. Additionally, slope was tied to ground using a 37.4kΩ resistor for 500kHz operation and it was tied to ground using a 26.1kΩ resistor for 1MHz operation. For all configurations, VBUS was set to 6V. SS had a 22nF bypass capacitor. VCC had a 0.68µF bypass capacitor. COMP had a 4.22kΩ and 10nF RC filter. The ISL73849SLH was operated in dual phase with a 5A load. The output voltage was 1V. The ambient temperature was 25°C. A device exhibited a SET when VOUT deviated beyond ±2.5% (±25mV) of its nominal value of 1V. Triggers were set to capture events in which SALERT dropped below 2.25V or V_{OUT} deviated beyond ±2.5% of its nominal value to capture SEFIs and SETs, respectively. Additionally, the PMBus registers were continuously read during the run to monitor for SEUs or SETs in the internal analog to digital converter (ADC). The device was exposed to a fluence of 1E7ions/cm² during each test run.

Table 7. ISL73849SLH SET Test Conditions

Test Condition	Number of Devices Tested	Frequency (kHz)	V_{DD} (V)	PVIN (V)
#1	4	500	4.5	5.0
#2	4			13.2
#3	4		13.2	13.2
#4	4			5.0
#5	4	1000	4.5	5.0
#6	4			13.2
#7	4		13.2	13.2
#8	4			5.0

2.2.1 VOUT SETs and SEFIs at 86MeV·cm²/mg

The results of VOUT SET and SEFI testing for the ISL73849SLH at 86MeV·cm²/mg are displayed in Table 8. The results are summarized in Table 9.

Table 8. ISL73849SLH SET Test Results at LET = 86MeV·cm²/mg

Test Condition	Run #	DUT #	# of SETs	# of SEFIs
#1	440	13	4	0
	444	14	0	0
	460	15	5	0
	504	16	0	0
#2	441	13	2	0
	445	14	0	0
	501	15	0	0
	505	16	0	0
#3	442	13	4	0
	446	14	0	0
	502	15	0	0
	506	16	1	1
#4	443	13	13	0
	447	14	0	0
	503	15	0	1
	507	16	1	0
#5	448	17	36	0
	452	18	3	0
	456	19	10	0
	508	20	0	0
#6	449	17	36	0
	453	18	1	0
	457	19	0	0
	509	20	0	1
#7	450	17	3	0
	454	18	90	1
	458	19	98	0
	510	20	177	0
#8	451	17	16	0
	455	18	32	0
	459	18	33	0
	511	20	17	0

Table 9. ISL73849SLH SET Test Results Summary at LET = 86MeV·cm²/mg

Test Condition	# of DUTs	Total Fluence (ions/cm²)	# of SETs	SET σ (µm²)	# of SEFIs	SEFI σ (µm²)
#1	4	4.0E7	9	22.5	0	2.5
#2	4	4.0E7	2	5	0	2.5
#3	4	4.0E7	5	12.5	1	2.5

Table 9. ISL73849SLH SET Test Results Summary at LET = 86MeV·cm^2/mg

Test Condition	# of DUTs	Total Fluence (ions/cm^2)	# of SETs	SET σ (μm^2)	# of SEFIs	SEFI σ (μm^2)
#4	4	4.0E7	14	35	1	2.5
#5	4	4.0E7	49	122.5	0	2.5
#6	4	4.0E7	37	92.5	1	2.5
#7	4	4.0E7	368	920	1	2.5
#8	4	4.0E7	98	245	0	2.5

Figure 3 show scatter plots of the maximum V_{OUT} deviation in percentage of the measured operating VOUT voltage vs the SET recovery time in nanoseconds for all test conditions. The recovery time was defined as the duration for which V_{OUT} deviated beyond 2.5% of its measured operating voltage. Some events had maximum V_{OUT} deviations less than 2.5%, so their SET recovery time is reported as 0ns. The timing resolution of the oscilloscope was 2ns, so the scatter plots of these test conditions appear columnar due to the discrete time. The dashed red lines indicate the 2.5% V_{OUT} deviation criteria. The maximum positive V_{OUT} deviation was by 3.55%. The maximum negative deviation was by -2.72%. The maximum recovery time was 16ns.

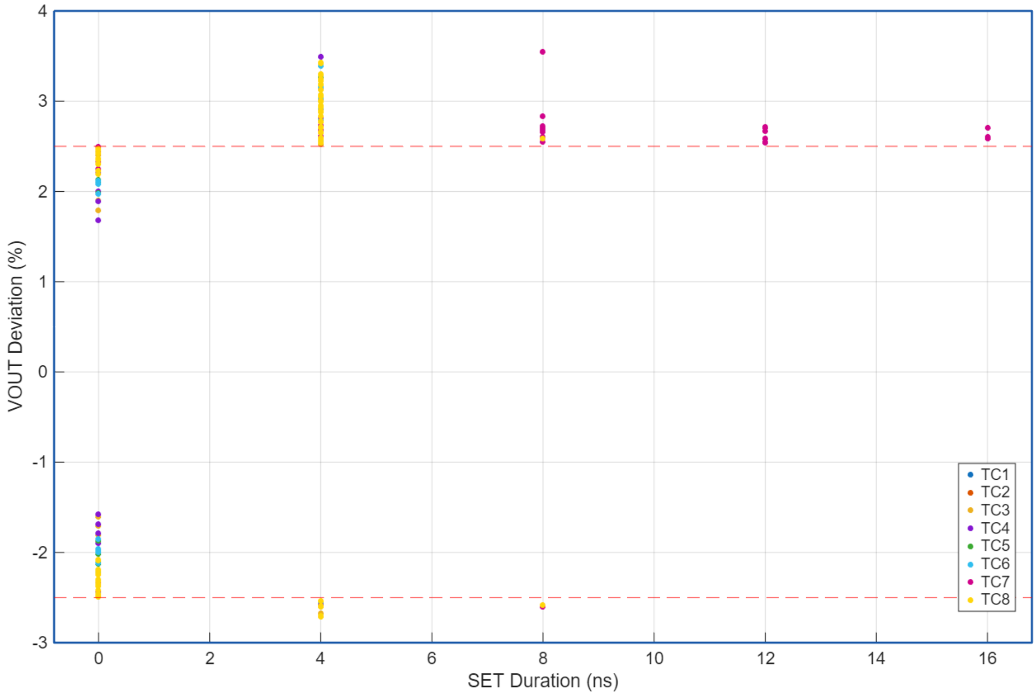

Figure 3. ISL73849SLH VOUT SET Size vs Recovery Time at 86MeV*cm2/mg

Figure 4 shows the waveforms of a typical SET capture. This SET occurred while the device was in TC #1; it had a V_{OUT} deviation of 2.68% and a recovery of time of 4ns. During the SET, the positive pulse widths of the preceding PWM1 and PWM2 pulses were increased. The elongated pulses were followed by three shortened pulses before normal operation resumed. COMP rose by approximately 150mV. The deviation in V_{OUT} was a short duration spike with a 26mV magnitude.

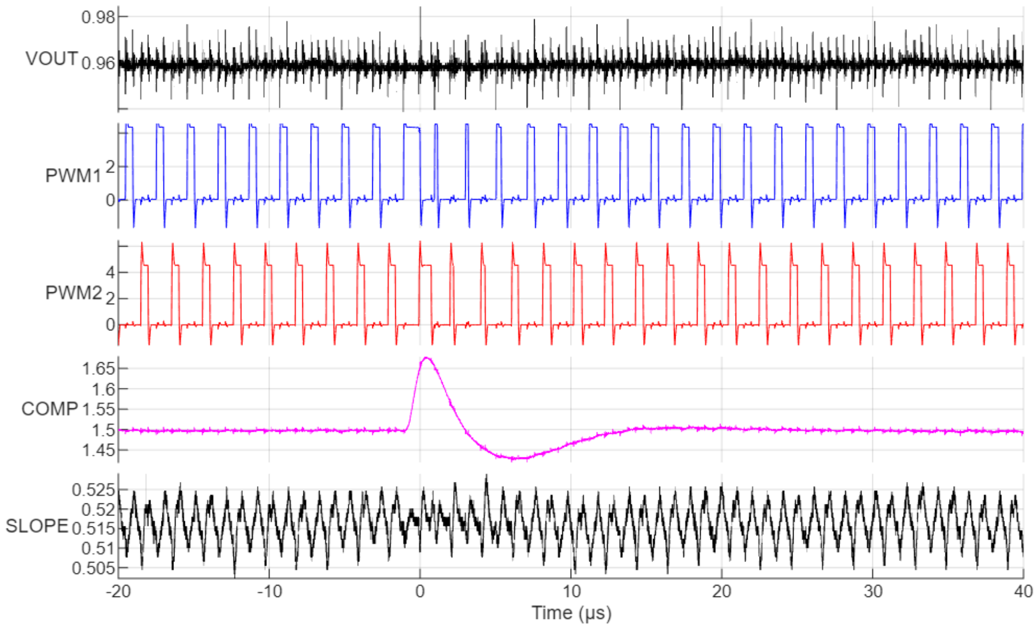

Figure 4. Typical SET Capture

The ISL73849SLH also exhibited SEFIs. A typical SEFI capture is displayed in Figure 5. During the SEFI, FLTb and SALERT pull low. FLTb is low for approximately 10ms until it spontaneously recovers, while SALERT is low until the CLEAR_FAULT PMBus command is issued. PWM2 stops switching for approximately 12ms, and VOUT loses regulation. When PWM2 resumes switching, VOUT charges back up until regulation is restored approximately 18ms following the onset of the SEFI.

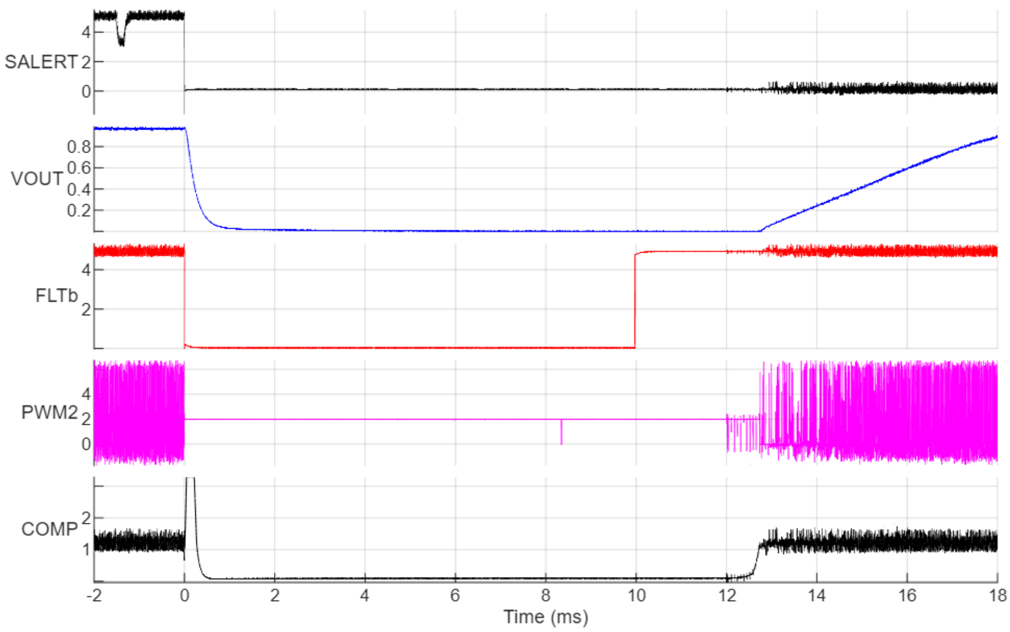

Figure 5. Typical SEFI Capture

2.2.2 VOUT SETs and SEFIs at 46MeV·cm^2/mg

The results of VOUT SET and SEFI testing at 46MeV·cm2/mg are shown in Table 10 and summarized in Table 11.

Table 10. ISL73849SLH SET Test Results at LET = 46MeV·cm^2/mg

Test Condition	Run #	DUT #	# of SETs	# of SEFIs
#1	339	43	3	0
	343	44	0	0
	347	45	0	0
	351	46	0	0
#2	340	43	0	0
	344	44	0	0
	348	45	0	0
	352	46	0	0
#3	341	43	0	0
	345	44	0	0
	349	45	0	0
	353	46	1	0
#4	342	43	2	0
	346	44	0	0
	350	45	2	0
	354	46	1	0
#5	355	47	0	0
	359	48	0	0
	363	49	0	0
	367	50	0	0
#6	356	47	3	0
	360	48	0	0
	364	49	2	1
	368	50	0	0
#7	357	47	1	0
	361	48	39	1
	365	49	76	4
	369	50	0	0
#8	358	47	1	0
	362	48	0	0
	366	49	1	0
	370	50	0	0

Table 11. ISL73849SLH SET Test Results Summary at LET = 46MeV·cm^2/mg

Test Condition	# of DUTs	Total Fluence (ions/cm^2)	# of SETs	SET σ (µm^2)	# of SEFIs	SEFI σ (µm^2)
#1	4	4.0E7	3	7.5	0	2.5
#2	4	4.0E7	0	2.5	0	2.5
#3	4	4.0E7	1	2.5	0	2.5
#4	4	4.0E7	5	12.5	0	2.5
#5	4	4.0E7	0	2.5	0	2.5
#6	4	4.0E7	5	12.5	1	2.5

Table 11. ISL73849SLH SET Test Results Summary at LET = 46MeV·cm^2/mg (Cont.)

Test Condition	# of DUTs	Total Fluence (ions/cm^2)	# of SETs	SET σ (µm^2)	# of SEFIs	SEFI σ (µm^2)
#7	4	4.0E7	116	290	5	12.5
#8	4	4.0E7	2	5	0	2.5

Figure 6 show scatter plots of the maximum V_{OUT} deviation in percentage of the measured operating V_{OUT} voltage vs the SET recovery time in nanoseconds for all test conditions. The recovery time was defined as the duration for which V_{OUT} deviated beyond 2.5% of its measured operating voltage. Some events had maximum V_{OUT} deviations less than 2.5%, so their SET recovery time is reported as 0ns. The timing resolution of the oscilloscope was 2ns, so the scatter plots of these test conditions appear columnar due to the discrete time. The dashed, red lines indicate the 2.5% V_{OUT} deviation criteria. The maximum positive V_{OUT} deviation was by 3.91%. The maximum negative deviation was by -2.70%. The maximum recovery time was 24ns.

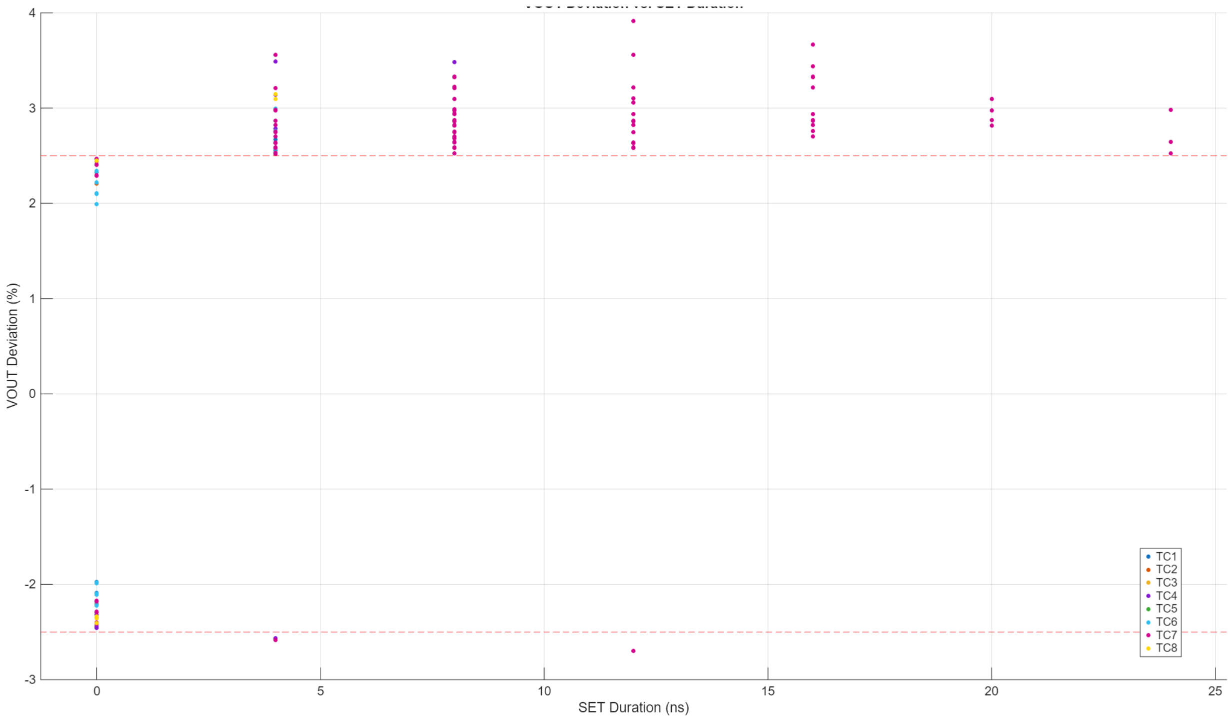

Figure 6. ISL73849SLH VOUT SET Size vs Recovery Time at 46MeV·cm^2/mg

The waveforms for the V_{OUT} SETs and SEFIs were similar to those captured at 86MeV·cm^2/mg.

2.2.3 ADC SETs

On power-up, the ISL73849SLH turns on with the PMBus registers in a default state. For PMBus testing, each PMBus register was read out sequentially in a continuous loop while the beam was on. The SALERTb pin was also read back as high or low. Before each read of the telemetry registers, the register was overwritten with data from the internal ADC. At the end of each loop, the FAULT_STATUS register is cleared with CLEAR_FAULT PMBus command regardless of whether a fault was detected or not. Approximately 93ms to 96ms transpired between consecutive samples on an individual register. After the beam, a single read of all the registers was taken, followed by a power cycle and an additional read of all the registers to determine if there were any hard-error SEUs.

A DUT was considered to have exhibited a SEU if one of the PMBus configuration registers transitioned from its default setting.

Before each run, the PMBus registers were read out following the above protocol for approximately one minute to establish a baseline estimate of the noise margin for each measurement. A DUT was considered to exhibit a telemetry SET if a telemetry measurement exceeded the 31-point moving median of the measurement by greater than the noise floor plus one ADC code. The moving median was used to account for drift in the measurements over the course of the run.

The results of the testing are shown in Table 12 and Table 13. The data for several runs was corrupted, and that data was omitted. The results are summarized in Table 14.

Table 12. ISL73849SLH SET Test Results at LET = 86MeV·cm^2/mg

TC	Run #	DUT #	VDD SET	VOUT SET	VREF SET	VDROOP SET	VFBP SET	VFBN SET	ISEN1 SET	ISEN2 SET	IOUT SET	FREQ SET
#1	440	13	66	204	260	165	218	199	87	69	121	0
	444	14	24	94	125	70	52	79	89	107	82	0
	460	15	51	93	206	202	266	96	149	136	110	0
	504	16	2	1	0	1	0	0	25	17	35	0
#2	441	13	1	1	3	1	3	10	10	119	48	0
	445	14	9	151	221	212	130	144	86	85	167	0
	501	15	2	3	1	1	0	7	72	84	3	0
	505	16	4	9	2	11	1	22	60	36	30	0
#3	442	13	3	2	1	1	5	0	38	47	4	0
	446	14	29	79	221	254	193	136	133	63	63	0
	502	15	-	-	-	-	-	-	-	-	-	-
	506	16	24	44	48	69	122	59	45	235	216	0
#4	443	13	35	140	165	179	352	118	81	6	43	0
	447	14	0	4	2	1	2	5	7	5	7	0
	503	15	5	1	5	4	2	2	111	83	82	0
	507	16	16	77	12	32	205	45	82	69	17	0
#5	448	17	85	235	328	445	21	248	76	78	43	0
	452	18	7	3	1	3	1	8	6	18	2	0
	456	19	3	0	3	1	10	5	37	120	17	0
	508	20	-	-	-	-	-	-	-	-	-	-
#6	449	17	2	4	3	0	1	9	15	13	19	0
	453	18	4	2	1	10	8	7	109	9	39	0
	457	19	0	5	3	0	17	5	20	32	36	0
	509	20	5	2	3	9	8	3	32	24	8	0
#7	450	17	0	0	3	3	0	26	44	26	18	0
	454	18	11	26	63	28	53	97	30	20	150	0
	458	19	11	2	5	4	6	227	87	85	19	0
	510	20	-	-	-	-	-	-	-	-	-	-
#8	451	17	5	1	6	0	1	0	37	39	17	0
	455	18	118	107	121	127	609	169	96	141	61	0
	459	18	2	99	35	31	28	187	36	18	91	0
	511	20	-	-	-	-	-	-	-	-	-	-

Table 13. ISL73849SLH SET Test Results at LET = 46MeV·cm²/mg

TC	Run #	DUT#	VDD SET	VOUT SET	VREF SET	VDROOP SET	VFBP SET	VFBN SET	ISEN1 SET	ISEN2 SET	IOUT SET	FREQ SET
#1	339	43	14	124	177	188	174	92	9	26	7	0
	343	44	0	0	0	0	2	1	0	1	0	0
	347	45	4	2	3	3	3	9	8	2	3	0
	351	46	1	6	2	5	3	7	23	3	2	0
#2	340	43	3	0	1	2	0	1	2	2	5	0
	344	44	0	0	2	2	0	3	1	0	1	0
	348	45	6	1	12	1	2	6	1	3	5	0
	352	46	8	3	3	16	3	39	19	7	3	0
#3	341	43	18	2	0	1	9	11	3	4	2	0
	345	44	0	0	0	0	0	4	3	4	5	0
	349	45	5	0	3	5	0	7	9	0	1	0
	353	46	14	0	6	4	2	7	17	5	10	0
#4	342	43	11	11	6	3	1	9	1	8	0	0
	346	44	5	6	3	0	0	6	3	0	4	0
	350	45	6	2	2	1	2	6	3	0	2	0
	354	46	2	8	3	5	3	8	0	13	7	0
#5	355	47	1	1	5	1	4	10	3	0	3	0
	359	48	2	1	1	1	3	0	7	6	12	0
	363	49	0	0	1	2	6	6	2	2	4	0
	367	50	2	4	4	0	7	13	11	2	1	0
#6	356	47	0	1	0	0	1	0	3	17	4	0
	360	48	1	0	0	0	1	6	2	3	0	0
	364	49	0	8	2	0	4	3	4	20	0	0
	368	50	1	0	7	6	5	17	22	15	38	0
#7	357	47	4	0	1	0	9	2	8	0	1	0
	361	48	1	0	4	1	8	0	0	0	9	0
	365	49	9	5	0	4	7	4	2	0	1	0
	369	50	13	4	1	2	8	6	0	1	12	0
#8	358	47	2	0	2	3	0	2	1	1	0	0
	362	48	2	0	4	1	2	2	4	15	0	0
	366	49	3	1	1	1	6	9	0	1	0	0
	370	50	2	0	0	14	0	12	1	2	1	0

Table 14. ISL73849SLH SET Test Results at LET = 86MeV·cm²/mg

TC	LET (MeV·cm²/mg)	VDD SET σ (μm²)	VOUT SET σ (μm²)	VREF SET σ (μm²)	VDROOP SET σ (μm²)	VFBP SET σ (μm²)	VFBN SET σ (μm²)	ISEN1 SET σ (μm²)	ISEN2 SET σ (μm²)	IOUT SET σ (μm²)	FREQ SET σ (μm²)
#1	86	357.5	980	1477.5	1095	1340	935	875	822.5	870	2.5
	46	47.5	330	455	490	455	272.5	100	80	30	2.5
#2	86	40	410	567.5	562.5	335	457.5	570	810	620	2.5
	46	42.5	10	45	52.5	12.5	122.5	57.5	30	35	2.5
#3	86	186.67	416.67	900	1080	1066.67	650	720	1150	943.33	3.33
	46	92.5	5	22.5	25	27.5	72.5	80	32.5	45	2.5

Table 14. ISL73849SLH SET Test Results at LET = 86MeV·cm²/mg (Cont.)

TC	LET (MeV·cm²/mg)	VDD SET σ (μm²)	VOUT SET σ (μm²)	VREF SET σ (μm²)	VDROOP SET σ (μm²)	VFBP SET σ (μm²)	VFBN SET σ (μm²)	ISEN1 SET σ (μm²)	ISEN2 SET σ (μm²)	IOUT SET σ (μm²)	FREQ SET σ (μm²)
#4	86	140	555	460	540	1402.5	425	702.5	407.5	372.5	2.5
	46	60	67.5	35	22.5	15	72.5	17.5	52.5	32.5	2.5
#5	86	316.67	793.33	1106.67	1496.67	106.6	870	396.67	720	206.67	3.33
	46	12.5	15	27.5	10	50	72.5	57.5	25	50	2.5
#6	86	36.67	32.5	25	47.5	85	60	440	195	255	2.5
	46	5	22.5	22.5	15	27.5	65	77.5	137.5	105	2.5
#7	86	73.33	93.33	236.67	116.67	196.67	1166.67	536.67	436.67	623.33	3.33
	46	67.5	22.5	15	17.5	80	30	25	2.5	57.5	2.5
#8	86	416.67	690	540	526.67	2126.67	1186.67	563.33	660	563.33	3.33
	46	22.5	2.5	17.5	47.5	20	62.5	15	47.5	2.5	2.5

Figure 7 shows a typical telemetry run while under beam. The ADC showed transients up to full scale, however, the transients only lasted a single reading. Therefore, averaging can be used as a mitigation technique for the ADC SETs.

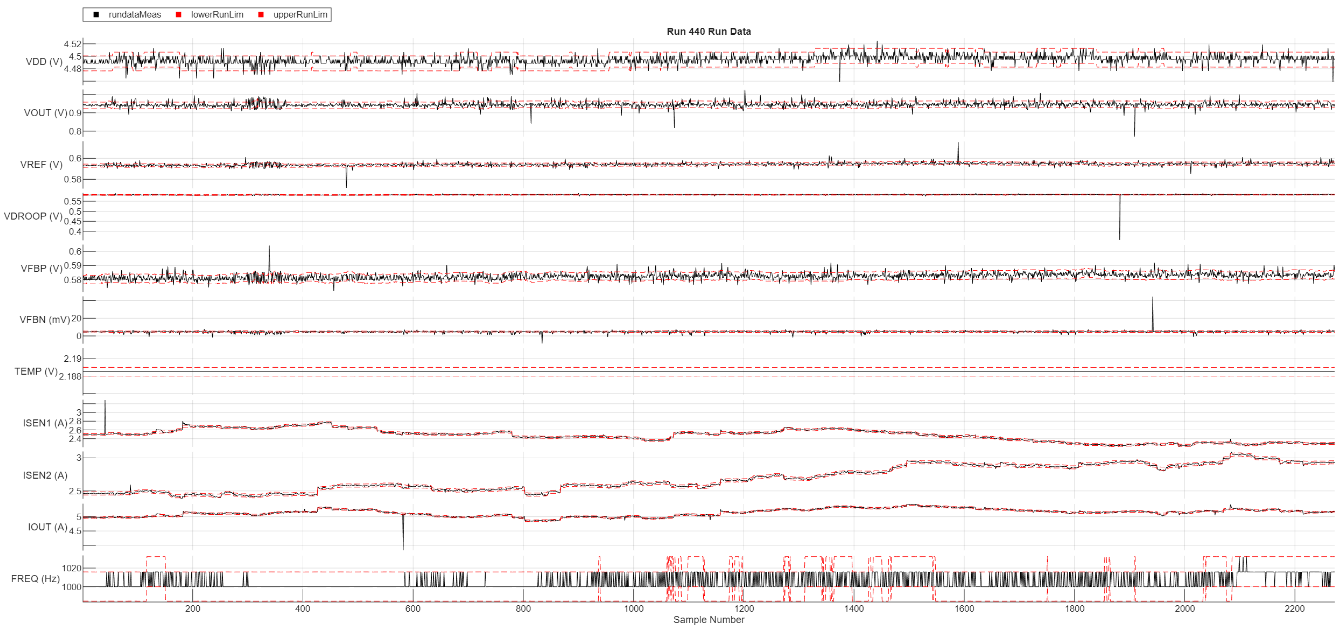

Figure 7. Typical Telemetry Run: Run 440

The PMBus configuration registers did not exhibit any SEUs during any of the testing.

2.2.4 ADC SEFIs

During one run on a prior test trip while testing at 86MeV·cm²/mg, the ADC exhibited a SEFI during which the ADC remained in a busy state and could not sample. The event lasted for 39 consecutive samples on each parameter, and the ADC read 8191 decimal for each telemetry parameter. The event is shown in Figure 8. The y-axis for each parameter in Figure 8 is in units of ADC codes in decimal. A power cycle might be required to restore telemetry operation. Since the event was only observed once and the total fluence between the two trip was 6.4E8ions/cm², the cross-section for this event at 86MeV·cm²/mg is 0.16μm². The DUT did not exhibit the event at 45.8MeV·cm²/mg. By approximating the cross-section versus LET curve as a step function with a saturation cross-section of 0.16µm^2 and an onset LET of 45.8MeV·cm^2/mg, an ADC SEFI error rate calculation can be made using CREME96. The ADC SEFI error rate in GEO during solar minimum and behind 100mils of aluminum is 3.27E-13 events per year. The mean time between ADC SEFIs is three trillion years.

The PMBus configuration registers were not upset during the event.

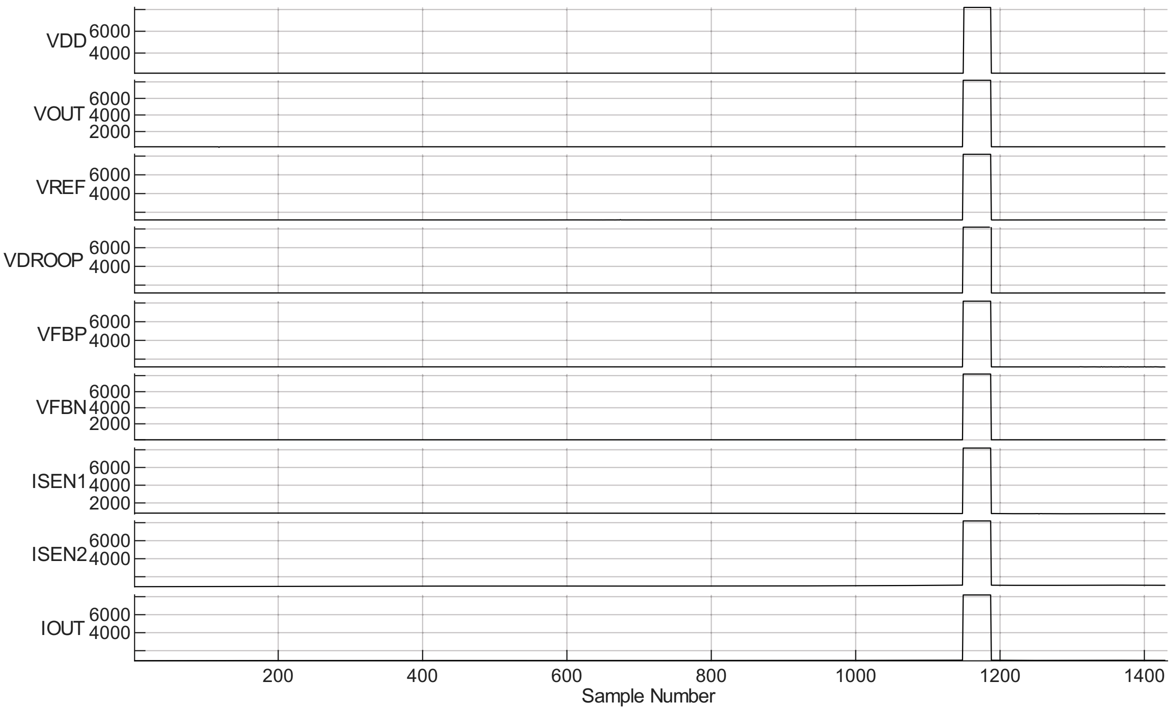

Figure 8. ADC SEFI

3. Discussion and Conclusion

SEE testing was performed with normal incidence gold and silver for a LETs of 86.3MeV·cm^2/mg and 45.8MeV·cm^2/mg at the surface of the device. The LET of the gold ions in the active silicon layer of the device ranged from 88.4MeV·cm^2/mg to 90.2MeV·cm^2/mg. The LET of the silver ions in the active silicon layer of the device ranged from 47.9MeV·cm^2/mg to 49.8MeV·cm^2/mg.

The ISL73849SLH proved to be free of Destructive Single Event Effects (DSEE) at 125°C under the following maximum parameter set: V_{DD} = 23V, V_{CC} = 6.3V, and V_{ISEN} = 13.5V at 86MeV·cm^2/mg and V_{DD} = 25V, V_{CC} = 6.7V, and V_{ISEN} = 13.5V at 46MeV·cm^2/mg.

The regulator exhibited SET events where V_{OUT} deviated beyond ±2.5% of its nominal value with a worst-case cross-section of 920µm^2 at 86MeV·cm^2/mg. The maximum deviation in V_{OUT} at 86MeV·cm^2/mg was 3.55%. The maximum amount of time until V_{OU}T returned to within ±2.5% of its nominal value at 86MeV·cm^2/mg was 16ns.

A VOUT SEFI was defined as an event in which FLTb pulled low and there was a loss of regulation in V_{OUT}. During a SEFI, V_{OUT} regulation is restored with a spontaneous soft start. A total of four SEFIs were observed during SET testing for an average cross-section of 2.5µm^2 per test condition at 86MeV·cm^2/mg. FLTb was low for approximately 10ms during SEFIs. SALERT recovered with the CLEAR_STATUS PMBus command.

The on-chip analog to digital converter (ADC) exhibited SETs during telemetry readings. The SETs in the readings were up to full scale; however, they only lasted a single sample. Therefore, these SETs can be mitigated by averaging multiple samples.

The ADC also exhibited one SEFI event during a total fluence of 6.4E8ions/cm^2 at 86MeV·cm^2/mg for a total cross-section of 0.16µm^2. During this event, the ADC remained in a busy state and could not sample. The event lasted for 39 consecutive samples on each recorded parameter, and the ADC read 8191 decimal for each telemetry parameter. The device did not exhibit ADC SEFIs at 46MeV·cm^2/mg. If an ADC SEFI occurs, a power cycle is recommended to restore telemetry functionality. An ADC SEFI error rate calculation can be made using CREME96. The ADC SEFI error rate in GEO during solar minimum and behind 100 mils of aluminum is 3.27E-13 events per year. The mean time between ADC SEFIs is three trillion years.

The PMBus configuration registers did not exhibit any SEUs during testing at 86MeV·cm^2/mg.

4. Revision History

Revision	Date	Description
1.00	Dec 12, 2025	Initial release.

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