ISL73148SEH

Low Dose Rate Total Ionizing Dose Testing of the ISL73148SEH 8-Channel 14-Bit 900/480ksps SAR ADC

Introduction

This report summarizes the results of low dose rate (LDR) total ionizing dose (TID) testing of the ISL73148SEH, a radiation hardened 8-channel 14-Bit 900/480ksps successive approximation register (SAR) analog-to-digital converter (ADC). The test was conducted to provide an assessment of the total dose hardness of the part and to provide an estimate of the bias sensitivity. Parts were irradiated either under bias or with all pins grounded at a LDR (0.01rad(Si)/s) to 100krad(Si) followed by a 168-hour biased anneal at 100ºC. The ISL73148SEH is rated to 75krad(Si) at LDR and is acceptance tested on a wafer-by-wafer basis to the datasheet limits.

Product Description

The ISL73148SEH is a radiation hardened 8-channel high precision 14-bit, 900/480ksps SAR ADC. The ADC core is preceded by eight analog input channels followed by a buffered 8-to-1 multiplexer and a PGA (Programmable Gain Amplifier). The device features a peak SNR of 82dBFS when operating at 900ksps. With the PGA enabled, sampling rates up to 480ksps are supported. The PGA can be bypassed so that the sample rate increases to 900ksps.

The product features 900/480ksps throughput with no data latency. The device also features excellent linearity and dynamic accuracy. The ISL73148SEH offers a high-speed SPI-compatible serial interface that supports logic ranging from 2.2V to 3.6V using a separate digital I/O supply pin.

The ISL73148SEH offers a separate low power mode (LPM) pin that reduces power dissipation at lower sample rates. The analog input signal range is determined by an external reference with a supported input range of 2.4V to 2.6V.

The ISL73148SEH operates across the military temperature range from -55ºC to +125ºC and is available in a 28 Ld hermetically sealed Ceramic Dual Flat-Pack (CDFP) package. The pin assignments for the ISL73148SEH are shown in Figure 1 and the pin descriptions are shown in Table 1.
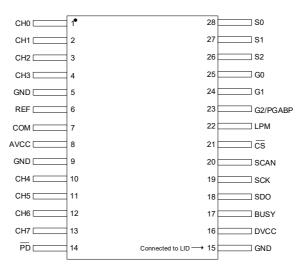

Figure 1. ISL73148SEH Pin Assignments

Table 1. ISL73148SEH Pin Descriptions

Pin Number	Pin Name	Description
5, 9, 15	GND	Analog and digital supply ground. Tie directly to the PCB ground plane (GND). Pin 15 is electrically tied to the package lid.
8	AVCC	Analog supply. The supply range is 4.5V to 5.5V. Bypass this pin to GND with a 10µF ceramic capacitor.
6	REF	Reference Input. The input range of REF is 2.4V to 2.6V. The voltage at the REF pin (VREF) defines the input range of each Analog Input Channel as 0V to VREF. Bypass REF to GND with a 10µF ceramic capacitor.
1, 2, 3, 4, 10, 11, 12, 13	CH0, CH1, CH2, CH3, CH4, CH5, CH6, CH7	Analog input channels. CH0 to CH7 are eight single-ended analog input channels. Each input channel pin may be driven within the voltage range from 0V to VREF.
7	COM	Common input. This is the reference voltage for all single-ended analog input channels. Connect to GND for unipolar (unsigned) conversions. For bipolar (signed) conversions, the COM pin outputs a voltage equal to VREF/2 and requires bypassing to GND with a 0.1µF ceramic capacitor. This pin is referenced to VREF. This pin is a device configuration pin and should not be switched dynamically during operation.
14	$\overline{PD}$	Power-down low input. When this pin is a logic low, the ADC enters power-down mode. If this occurs during a conversion, the conversion is halted, and the SDO pin is placed in Hi-Z. Logic levels are determined by DVCC. This pin has an internal 500kΩ pull-up resistor to DVCC.
16	DVCC	Digital I/O supply. The voltage range on this pin is 2.2V to 3.6V. DVCC is nominally set to the same supply voltage as the host interface (2.5V or 3.3V). Bypass DVCC to GND with 0.1µF capacitor.
17	BUSY	Busy output. A logic high indicates a conversion is in progress. The BUSY indicator returns low following the completion of a conversion. Logic levels are determined by DVCC.
18	SDO	Serial data output. The current conversion result is serially shifted out on this pin on the rising edges of SCK, MSB first to LSB last. The data stream is composed of 14 bits of conversion data followed by the channel select and gain select bits corresponding to the conversion result. When the COM pin is floated and bypassed to ground with a 0.1µF ceramic capacitor, the data format is in bipolar (signed) format. When the COM pin is grounded, the data format is unipolar (unsigned). Logic Levels are determined by DVCC.
19	SCK	Serial data clock input. When $\overline{CS}$ is low and the BUSY indicator is low, the conversion result is shifted out on SDO on the rising edges of SCK, Most Significant Bit (MSB) first to Least Significant Bit (LSB) last. Logic levels are determined by DVCC. SCK should be held low when it is not being asserted.
20	SCAN	Channel scan input. When this input is logic high, the internal sequencer controls the channel selected. CH0 is the first channel selected following the rising edge of SCAN. Each subsequent channel is selected on each new rising edge of $\overline{CS}$. Logic levels are determined by DVCC.
21	$\overline{CS}$	Convert Start Low input. A falling edge on this input completes the sampling process and starts a new conversion. The conversion is timed using an internal oscillator. The device automatically powers down following the conversion process. The logic state of the $\overline{CS}$ pin controls the state of the SDO pin. A logic high on the $\overline{CS}$ pin disables the SDO pin driver and the SDO pin impedance is Hi-Z. A logic low on the $\overline{CS}$ pin enables the SDO driver (unless $\overline{PD}$ is low) and allows data to be read out following a conversion. This pin should be held low at power-up and when in power-down or when the device is inactive.
22	LPM	Low power mode input. When this input is logic high, the acquisition time is directly controlled by the $\overline{CS}$ pin logic state held high. The ADC is automatically powered down between conversions to reduce power consumption for lower sample rates. This pin is a device configuration pin and should not be switched dynamically during operation.

Table 1. ISL73148SEH Pin Descriptions (Cont.)

Pin Number	Pin Name	Description
23, 24, 25	G2/PGABP, G1, G0	Gain selection logic inputs. These three pins program the gain of the PGA. The G2, G1, and G0 logic inputs are latched internally on the rising edge of $\overline{CS}$. The G2/PGABP pin should be left floating and bypassed to GND with a 100pF capacitor to bypass the PGA. When the PGA is bypassed, the maximum throughput rate is increased to approximately 900ksps. When using the G2/PGABP pin to bypass the PGA, the pin should not be switched dynamically during operation and should be driven to a static value to set the configuration of the PGA. When using the G2/PGABP pin to configure gain settings, it is safe to switch the pin dynamically during operation as long as timing requirements are met. Logic levels are determined by DVCC.
26, 27, 28	S2, S1, S0	Channel selection logic inputs. These three pins select the input channel passed through the input multiplexer to the PGA (or ADC if the PGA is bypassed). The S2, S1, and S0 logic inputs are latched internally on the rising edge of CS. Logic levels are determined by DVCC.
LID	N/A	Package Lid is internally connected to GND through Pin 15.

Contents

1. Test Description

1.1 Irradiation Facility

LDR testing was performed at 0.01rad(Si)/s using a Hopewell Designs N40 vault-type LDR irradiator located in the Palm Bay, Florida Rensas facility. A PbAl box was used to shield the test fixture and devices under test against low energy, secondary gamma radiation. Post-irradiation anneals were performed under bias in a small temperature chamber.

1.2 Test Fixturing

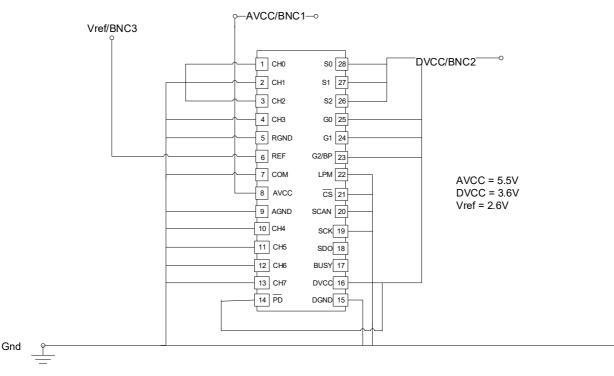Figure 2 shows the configuration used for the biased LDR testing and for the anneals.

Figure 2. ISL73148SEH LDR Bias Configuration

1.3 Characterization Equipment and Procedures

All electrical testing was performed outside the irradiator using the production Automated Test Equipment (ATE) with datalogging at each downpoint. Downpoint electrical testing was performed at room temperature.

1.4 Experimental Matrix

Irradiation was performed in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of nine samples irradiated at LDR under bias and nine samples irradiated at LDR with all pins grounded. All parts were also subject to a 168-hour, 100ºC biased anneal. Three control units were used.

The ISL73148SEH samples were drawn from wafer lots V6C750, V6C751, and V6C752. All samples were package in the standard 28 Ld hermetically sealed CDFP.

1.5 Downpoints

Planned irradiation downpoints for the LDR test were 0krad(Si), 10krad(Si), 30krad(Si), 50krad(Si), 75krad(Si), and 100krad(Si). The LDR irradiations were followed by a 168-hour high temperature anneal at 100ºC under bias.

2. Results

LDR TID testing of the ISL73148SEH is complete. All tested parameters passed the datasheet limits. Table 2 summarizes the results.

2.1 Attributes Data

Table 2. ISL73148SEH Attributes Data

Dose Rate (rad(Si)/s)	Condition	Sample Size	Downpoint	Pass[1]	Fail
0.01	Biased (Figure 2)	9	Pre-irradiation	9	0
			10krad(Si)	9	0
			30krad(Si)	9	0
			50krad(Si)	9	0
			75krad(Si)	9	0
			100krad(Si)	9	0
			Anneal	9	0
0.01	Grounded	9	Pre-irradiation	9	0
			10krad(Si)	9	0
			30krad(Si)	9	0
			50krad(Si)	9	0
			75krad(Si)	9	0
			100krad(Si)	9	0
			Anneal	9	0

1. A Pass indicates a sample that passes all datasheet limits.

2.2 Variables Data

The plots in Figure 3 through Figure 80 illustrate the LDR response of the selected parameters shown in Table 3 in the Appendix. The plots show the average tested values of the parameters as a function of total dose for each of the irradiation conditions, biased and grounded, plus a 168-hour, 100ºC biased anneal. The plots also include error bars at each down-point, representing the minimum and maximum measured values of the samples, although in some plots the error bars might not be visible due to their values compared to the scale of the graph.

Some graphs and captions state that they are the average; this denotes that the average of the measurements of multiple channels or pins was plotted. The error bars on these graphs represent the maximum and minimum measured values across all the channels or pins. Additionally, some parameters were only tested on CH0, as per the datasheet, and their graphs and captions state that they are CH0.

All samples passed the datasheet limits after irradiation to each level up to 100krad(Si) and the subsequent anneal.

Figure 3. ISL73148SEH CH0 minimum and maximum integral non-linearity (INL) in normal operating mode with AV$_{CC}$ = 5V and PGA Gain = 2 as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -1.2LSB and a maximum of 2LSB.
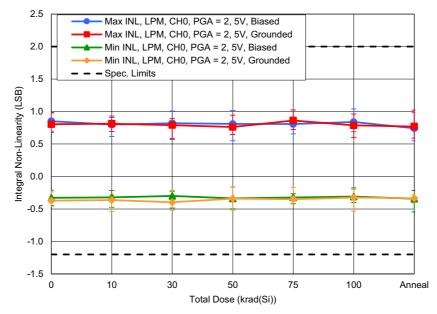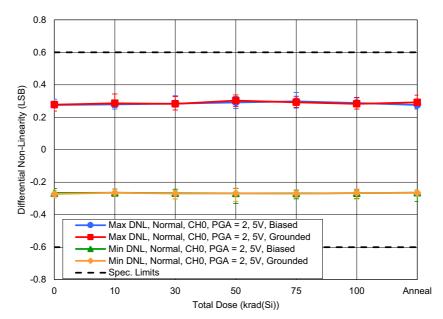
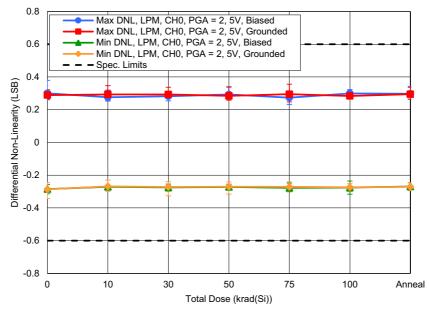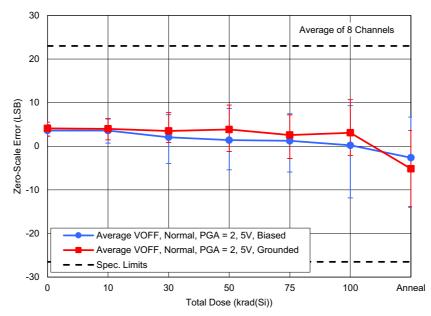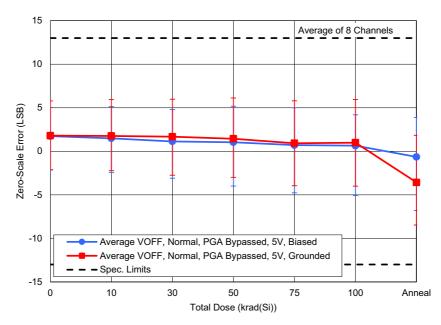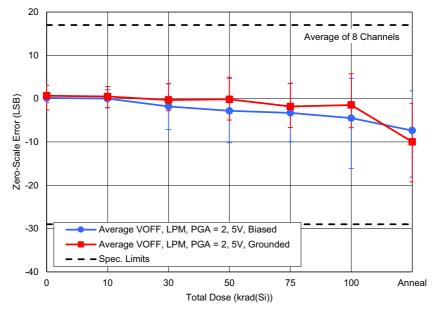

Figure 4. ISL73148SEH CH0 minimum and maximum integral non-linearity (INL) in low power mode with AV$_{CC}$ = 5V and PGA Gain = 2 as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -1.2LSB and a maximum of 2LSB.
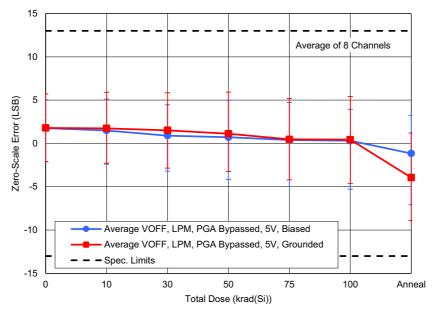
Figure 5. ISL73148SEH CH0 minimum and maximum differential non-linearity (DNL) in normal operating mode with AV$_{CC}$ = 5V and PGA Gain = 2 as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -0.6LSB and a maximum of 0.6LSB.

Figure 6. ISL73148SEH CH0 minimum and maximum differential non-linearity (DNL) in low power mode with AV$_{CC}$ = 5V and PGA Gain = 2 as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -0.6LSB and a maximum of 0.6LSB.

Figure 7. ISL73148SEH average zero-scale error (V_{OFF}) in normal operating mode with AV_{CC} = 5V and PGA Gain = 2 as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limits are a minimum of -26.5LSB and a maximum of 23LSB.
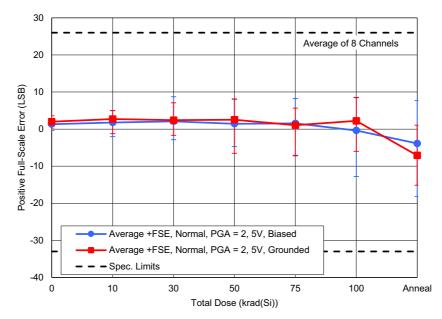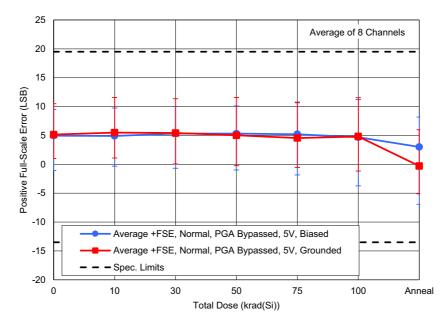

Figure 8. ISL73148SEH average zero-scale error (V_{OFF}) in normal operating mode with AV_{CC} = 5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limits are a minimum of -13LSB and a maximum of 13LSB.
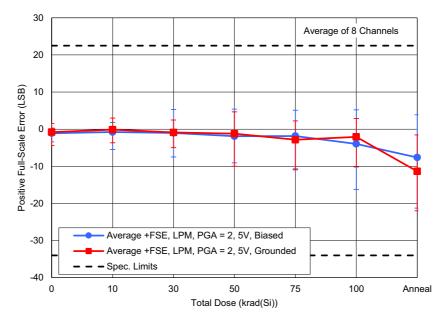
Figure 9. ISL73148SEH average zero-scale error (V$_{OFF}$) in low power mode with AV$_{CC}$ = 5V and PGA Gain = 2 as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limits are a minimum of -29LSB and a maximum of 17LSB.
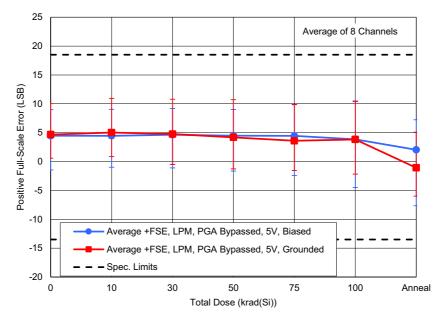

Figure 10. ISL73148SEH average zero-scale error (V$_{OFF}$) in low power mode with AV$_{CC}$ = 5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limits are a minimum of -13LSB and a maximum of 13LSB.

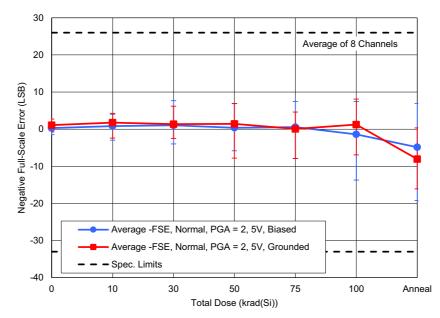**Figure 11. ISL73148SEH average positive full-scale error (+FSE) in normal operating mode with AV$_{CC}$ = 5V and PGA Gain = 2 as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limits are a minimum of -33LSB and a maximum of 26LSB.**
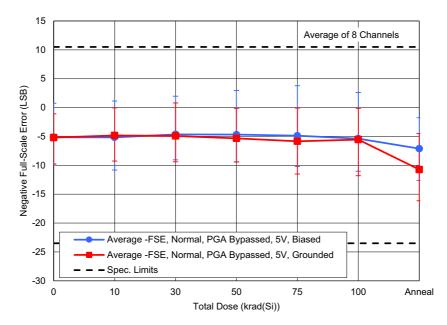

Figure 12. ISL73148SEH average positive full-scale error (+FSE) in normal operating mode with AV$_{CC}$ = 5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limits are a minimum of -13.5LSB and a maximum of 19.5LSB.
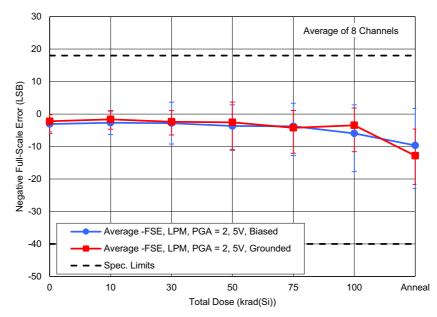
Figure 13. ISL73148SEH average positive full-scale error (+FSE) in low power mode with AV$_{CC}$ = 5V and PGA Gain = 2 as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limits are a minimum of -34LSB and a maximum of 22.5LSB.
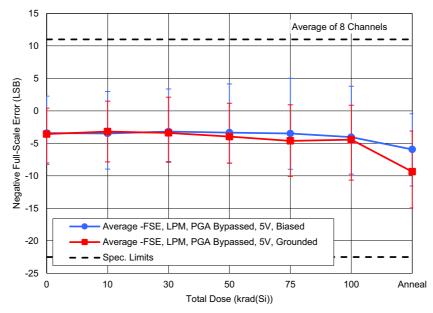

Figure 14. ISL73148SEH average positive full-scale error (+FSE) in low power mode with AV$_{CC}$ = 5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limits are a minimum of -13.5LSB and a maximum of 18.5LSB.
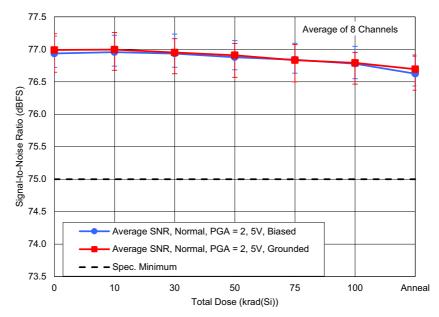
Figure 15. ISL73148SEH average negative full-scale error (-FSE) in normal operating mode with AV$_{CC}$ = 5V and PGA Gain = 2 as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limits are a minimum of -33LSB and a maximum of 26LSB.
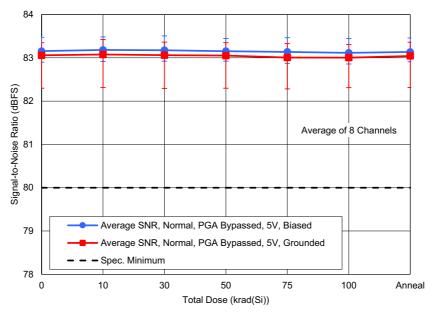

Figure 16. ISL73148SEH average negative full-scale error (-FSE) in normal operating mode with AV$_{CC}$ = 5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limits are a minimum of -23.5LSB and a maximum of 10.5LSB.

Figure 17. ISL73148SEH average negative full-scale error (-FSE) in low power mode with AV$_{CC}$ = 5V and PGA Gain = 2 as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limits are a minimum of -40LSB and a maximum of 18LSB.
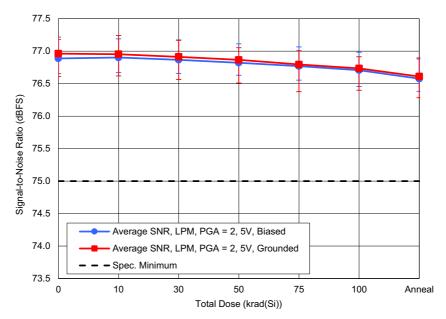

Figure 18. ISL73148SEH average negative full-scale error (-FSE) in low power mode with AV$_{CC}$ = 5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limits are a minimum of -22.5LSB and a maximum of 11LSB.

Figure 19. ISL73148SEH average signal-to-noise ratio (SNR) in normal operating mode with AV_{CC} = 5V and PGA Gain = 2 as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limit is a minimum of 75dBFS.
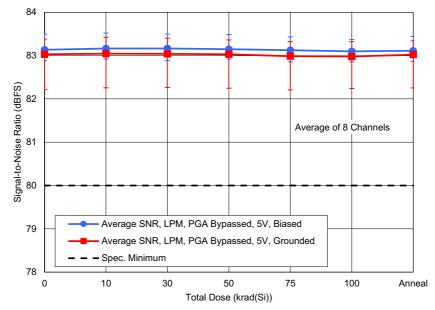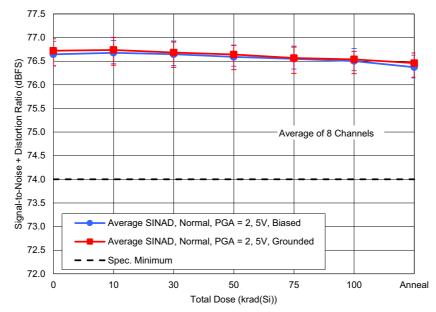

Figure 20. ISL73148SEH average signal-to-noise ratio (SNR) in normal operating mode with AV_{CC} = 5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limit is a minimum of 80dBFS.
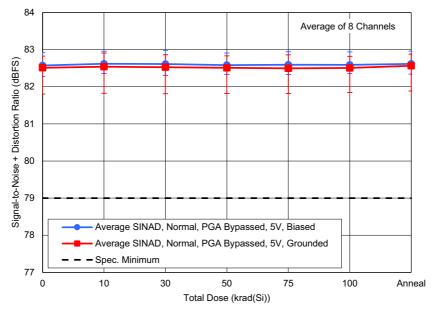
Figure 21. ISL73148SEH average signal-to-noise ratio (SNR) in low power mode with AV_{CC} = 5V and PGA Gain = 2 as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limit is a minimum of 75dBFS.
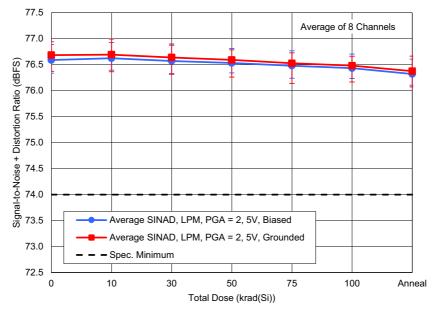

Figure 22. ISL73148SEH average signal-to-noise ratio (SNR) in low power mode with AV_{CC} = 5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limit is a minimum of 80dBFS.
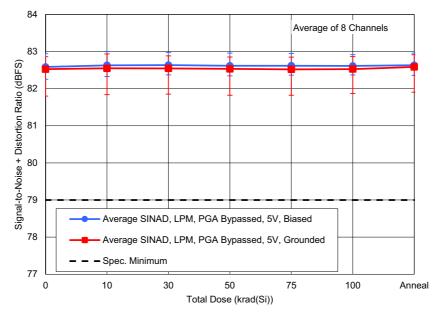
Figure 23. ISL73148SEH average signal to noise + distortion ratio (SINAD) in normal operating mode with AV$_{CC}$ = 5V and PGA Gain = 2 as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limit is a minimum of 74dBFS.
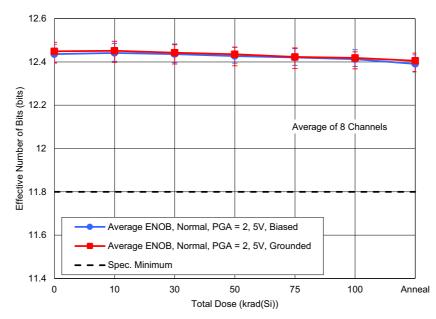

Figure 24. ISL73148SEH average signal to noise + distortion ratio (SINAD) in normal operating mode with AV$_{CC}$ = 5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limit is a minimum of 79dBFS.
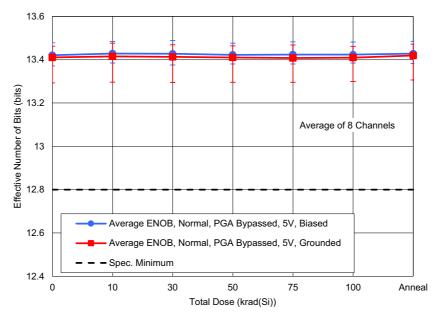
Figure 25. ISL73148SEH average signal to noise + distortion ratio (SINAD) in low power mode with AV$_{CC}$ = 5V and PGA Gain = 2 as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limit is a minimum of 74dBFS.
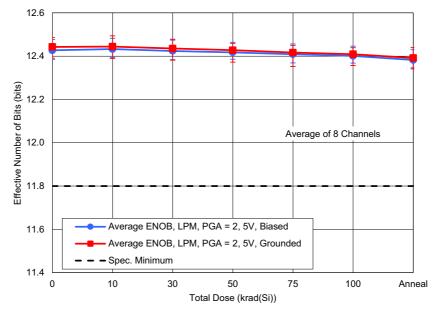

Figure 26. ISL73148SEH average signal to noise + distortion ratio (SINAD) in low power mode with AV$_{CC}$ = 5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limit is a minimum of 79dBFS.
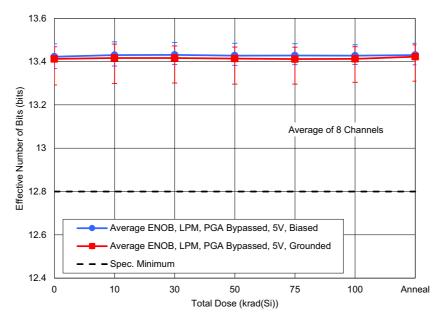
Figure 27. ISL73148SEH average effective number of bits (ENOB) in normal operating mode with AV$_{CC}$ = 5V and PGA Gain = 2 as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limit is a minimum of 11.8bits.

Figure 28. ISL73148SEH average effective number of bits (ENOB) in normal operating mode with AV$_{CC}$ = 5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limit is a minimum of 12.8bits.
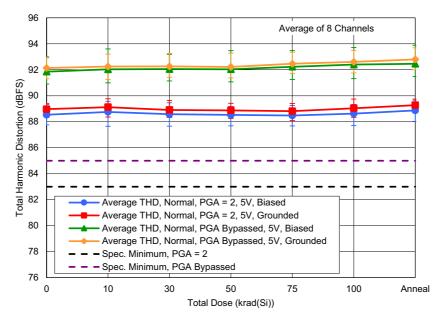
Figure 29. ISL73148SEH average effective number of bits (ENOB) in low power mode with AV$_{CC}$ = 5V and PGA Gain = 2 as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limit is a minimum of 11.8bits.

Figure 30. ISL73148SEH average effective number of bits (ENOB) in low power mode with AV$_{CC}$ = 5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limit is a minimum of 12.8bits.

Figure 31. ISL73148SEH average total harmonic distortion (THD) in normal operating mode with AV$_{CC}$ = 5V and PGA Gain = 2 or bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limits are minimums of 83dBFS when PGA Gain = 2 and 85dBFS when PGA is bypassed.
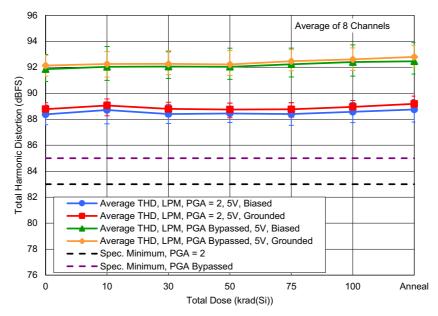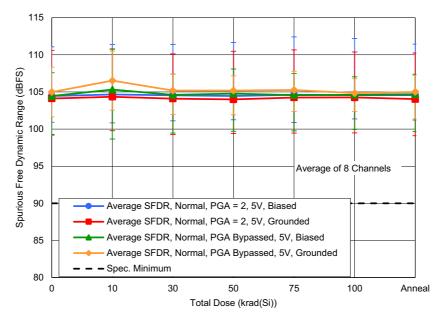

Figure 32. ISL73148SEH average total harmonic distortion (THD) in low power mode with AV$_{CC}$ = 5V and PGA Gain = 2 or bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limits are minimums of 83dBFS when PGA Gain = 2 and 85dBFS when PGA is bypassed.

Figure 33. ISL73148SEH average spurious free dynamic range (SFDR) in normal operating mode with AV$_{CC}$ = 5V and PGA Gain = 2 or bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limit is a minimum of 90dBFS for both conditions.
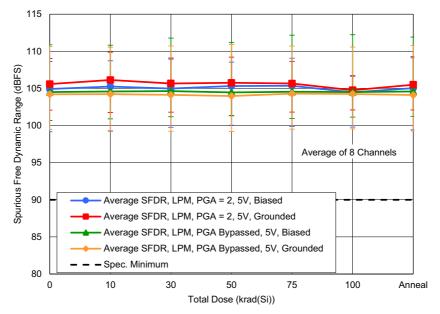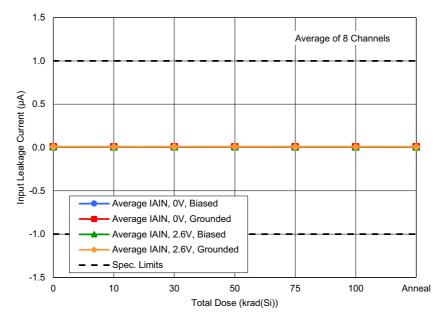

Figure 34. ISL73148SEH average spurious free dynamic range (SFDR) in low power mode with AV$_{CC}$ = 5V and PGA Gain = 2 or bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limit is a minimum of 90dBFS for both conditions.

Figure 35. ISL73148SEH average input leakage current (IA$_{IN}$) with A$_{IN}$ = 0V or 2.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limits are a minimum of -1µA and a maximum of 1µA.
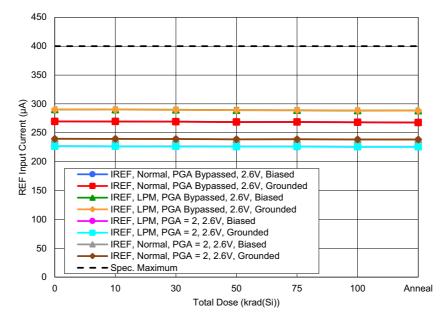

Figure 36. ISL73148SEH REF input current (I$_{REF}$) in normal operating mode or low power mode with PGA Gain = 2 or bypassed, and with V$_{REF}$ = 2.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 400µA for all conditions.

Figure 37. ISL73148SEH analog supply current – active (I_{AVCC}) in normal operating mode with AV_{CC} = 5V and PGA Gain = 2 or bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are maximums of 20.5mA when PGA Gain = 2 and 23mA when PGA is bypassed.
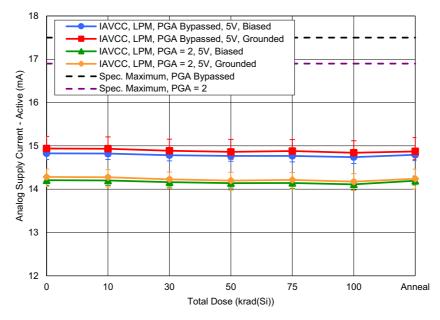

Figure 38. ISL73148SEH analog supply current – active (I_{AVCC}) in low power mode with AV_{CC} = 5V and PGA Gain = 2 or bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are maximums of 16.9mA when PGA Gain = 2 and 17.5mA when PGA is bypassed.
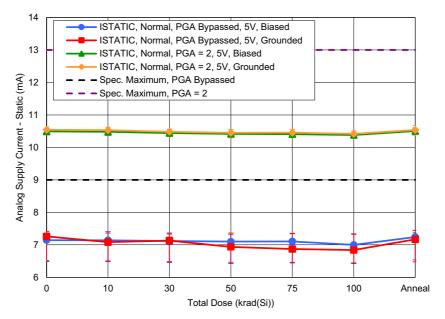
Figure 39. ISL73148SEH analog supply current – static (I_{STATIC}) in normal operating mode with AV_{CC} = 5V and PGA Gain = 2 or bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are maximums of 13mA when PGA Gain = 2 and 9mA when the PGA is bypassed.
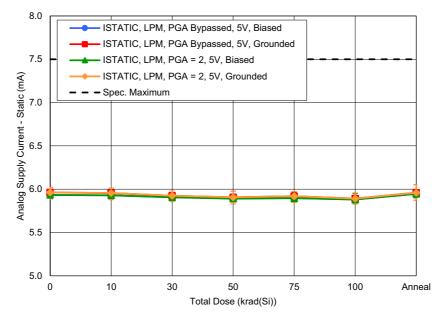

Figure 40. ISL73148SEH analog supply current – static (I_{STATIC}) in low power mode with AV_{CC} = 5V and PGA Gain = 2 or bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 7.5mA for both conditions.
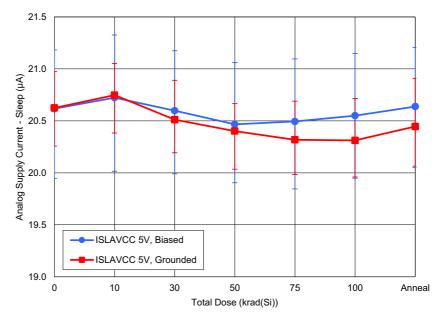
Figure 41. ISL73148SEH analog supply current – sleep (I_SLAVCC) in normal operating mode with AV_CC = 5V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. There are no datasheet limits for this parameter, but the typical value is 20µA.
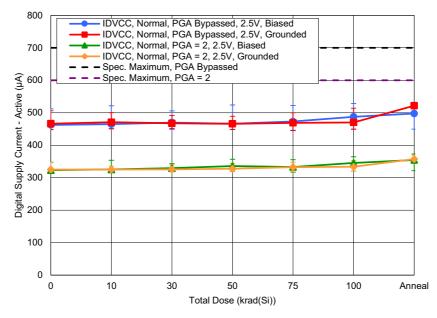

Figure 42. ISL73148SEH digital supply current – active (I_DVCC) in normal operating mode with DV_CC = 2.5V and PGA Gain = 2 or bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are maximums of 600µA when PGA Gain = 2 and 700µA when PGA is bypassed.
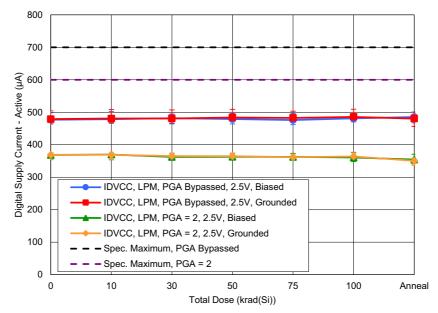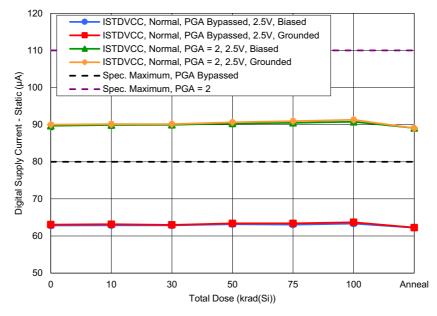
Figure 43. ISL73148SEH digital supply current – active (I_{DVCC}) in low power mode with DV_{CC} = 2.5V and PGA Gain = 2 or bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are maximums of 600μA when PGA Gain = 2 and 700μA when PGA is bypassed.
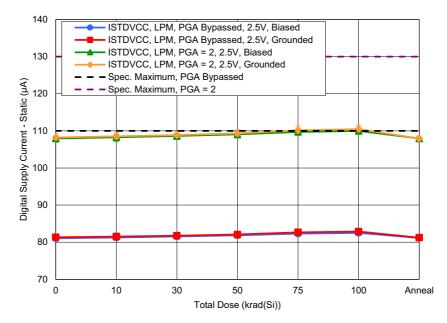

Figure 44. ISL73148SEH digital supply current – static (I_{STDVCC}) in normal operating mode with DV_{CC} = 2.5V and PGA Gain = 2 or bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are maximums of 110μA when PGA Gain = 2 and 80μA when PGA is bypassed.
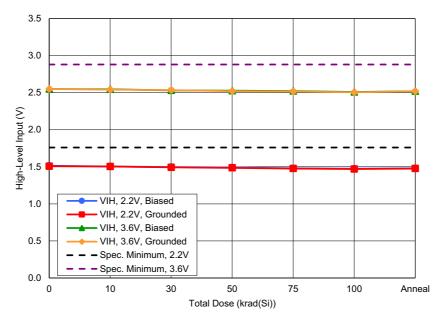
Figure 45. ISL73148SEH digital supply current – static (I$_{STDVCC}$) in low power mode with DV$_{CC}$ = 2.5V and PGA Gain = 2 or bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are maximums of 130µA when PGA Gain = 2 and 110µA when PGA is bypassed.

Figure 46. ISL73148SEH high-level input (V$_{IH}$) with DV$_{CC}$ = 2.2V or 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are minimums of 1.76V when DV$_{CC}$ = 2.2V and 2.88V when DV$_{CC}$ = 3.6V. *Note:* The datasheet reports the minimum voltages that are assured to be registered as logic high inputs. The measured values are the actual maximum voltages required to be registered as logic high inputs, so the datasheet limits are the maximums of the measured values.
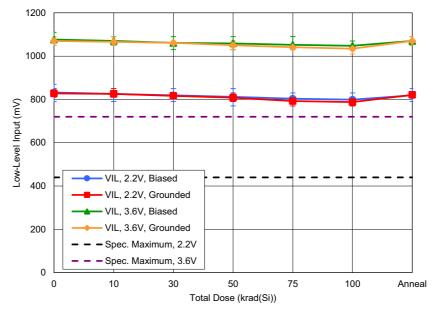
Figure 47. ISL73148SEH low-level input (V_{IL}) with DV_{CC} = 2.2V or 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are maximums of 440mV when DV_{CC} = 2.2V and 720mV when DV_{CC} = 3.6V. *Note:* The datasheet reports the maximum voltages that are assured to be registered as logic low inputs. The measured values are the actual minimum voltages required to be registered as logic low inputs, so the datasheet limits are the minimums of the measured values.
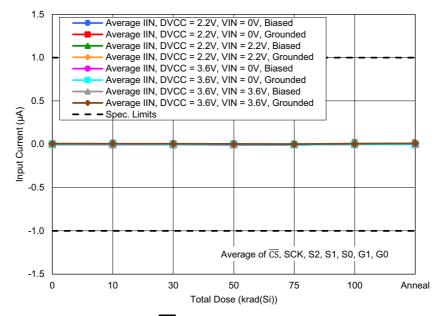

Figure 48. ISL73148SEH average input current ($\overline{CS}$, SCK, S2, S1, S0, G1, G0) (I_{IN}) with DV_{CC} = 2.2V and V_{IN} = 2.2V and 0V or DV_{CC} = 3.6V and V_{IN} = 3.6V and 0V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all pins. The datasheet limits are a minimum of -1µA and a maximum of 1µA for all conditions.
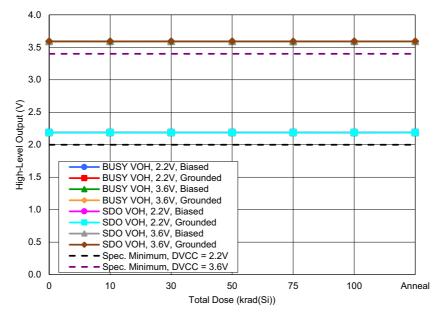
Figure 49. ISL73148SEH high-level output (V$_{OH}$) with DV$_{CC}$ = 2.2V or 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are minimums of 2V when DV$_{CC}$ = 2.2V and 3.4V when DV$_{CC}$ = 3.6V.
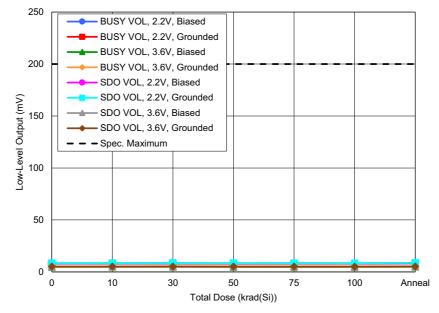

Figure 50. ISL73148SEH low-level output (V$_{OL}$) with DV$_{CC}$ = 2.2V or 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 200mV for all conditions.
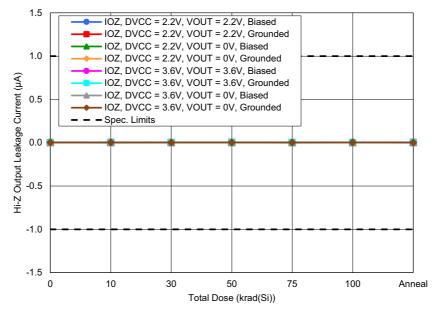
Figure 51. ISL73148SEH Hi-Z output leakage current (I_{OZ}) with DV_{CC} = 2.2V and V_{OUT} = 2.2V and 0V or DV_{CC} = 3.6V and V_{OUT} = 3.6V and 0V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -1µA and a maximum of 1µA for all conditions.
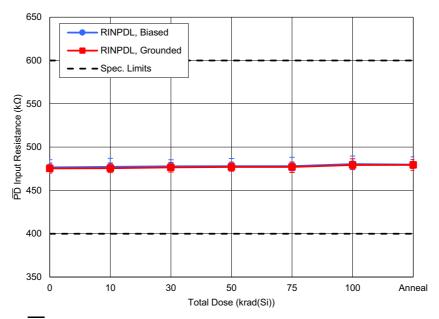

Figure 52. ISL73148SEH PD input resistance (R_{INPDL}) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 400kΩ and a maximum of 600kΩ.
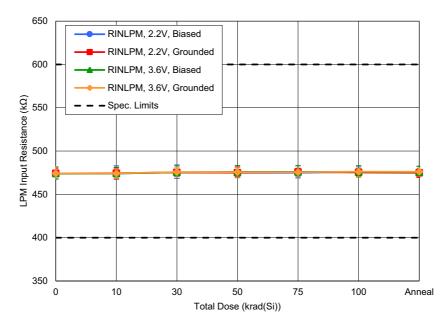
Figure 53. ISL73148SEH LPM input resistance (R$_{INLPM}$) with DV$_{CC}$ = 2.2V or 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 400kΩ and a maximum of 600kΩ.
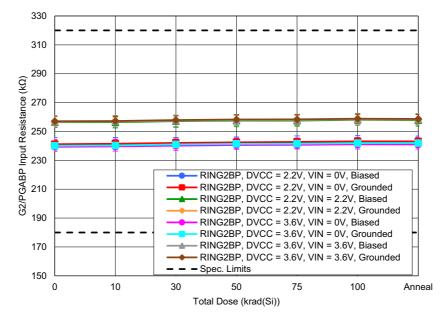

Figure 54. ISL73148SEH G2/PGABP input resistance (R$_{ING2BP}$) with DV$_{CC}$ = 2.2V and V$_{IN}$ = 2.2V and 0V or DV$_{CC}$ = 3.6V and V$_{IN}$ = 3.6V and 0V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 180kΩ and a maximum of 320kΩ.
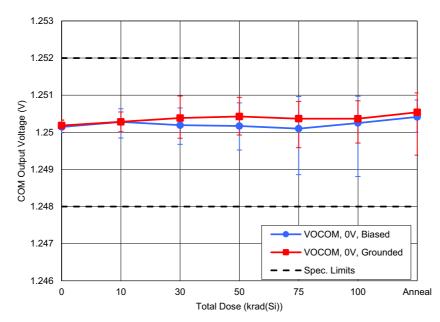
Figure 55. ISL73148SEH COM output voltage (V$_{OCOM}$) with COM pin bypassed to ground with a 0.1µF ceramic capacitor and with V$_{REF}$ = 2.5V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 1.248V and a maximum of 1.252V.
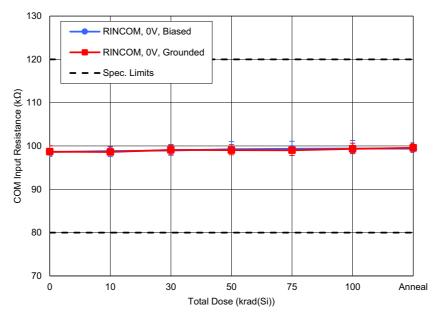

Figure 56. ISL73148SEH COM input resistance (R$_{INCOM}$) with COM pin driven to GND as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 80kΩ and a maximum of 120kΩ.
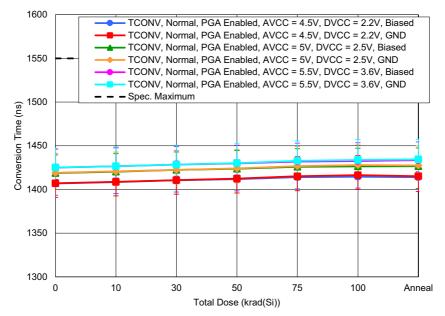
Figure 57. ISL73148SEH conversion time (t$_{CONV}$) in normal operating mode with PGA enabled and with AV$_{CC}$ = 4.5V and DV$_{CC}$ = 2.2V or AV$_{CC}$ = 5V and DV$_{CC}$ = 2.5V or AV$_{CC}$ = 5.5V and DV$_{CC}$ = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 1550ns.
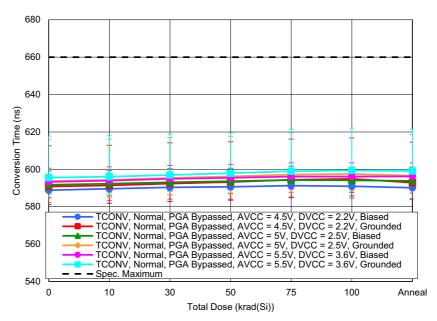

Figure 58. ISL73148SEH conversion time (t$_{CONV}$) in normal operating mode with PGA bypassed and with AV$_{CC}$ = 4.5V and DV$_{CC}$ = 2.2V or AV$_{CC}$ = 5V and DV$_{CC}$ = 2.5V or AV$_{CC}$ = 5.5V and DV$_{CC}$ = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 660ns.

Figure 59. ISL73148SEH conversion time (t$_{CONV}$) in low power mode with PGA enabled and with AV$_{CC}$ = 4.5V and DV$_{CC}$ = 2.2V or AV$_{CC}$ = 5V and DV$_{CC}$ = 2.5V or AV$_{CC}$ = 5.5V and DV$_{CC}$ = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 1550ns.
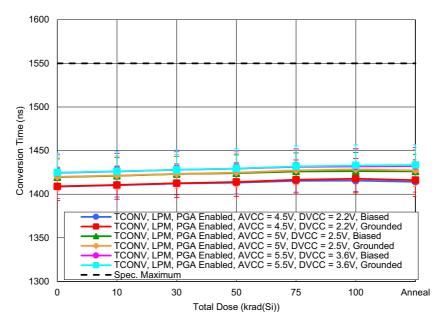

Figure 60. ISL73148SEH conversion time (t$_{CONV}$) in low power mode with PGA bypassed and with AV$_{CC}$ = 4.5V and DV$_{CC}$ = 2.2V or AV$_{CC}$ = 5V and DV$_{CC}$ = 2.5V or AV$_{CC}$ = 5.5V and DV$_{CC}$ = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 660ns.
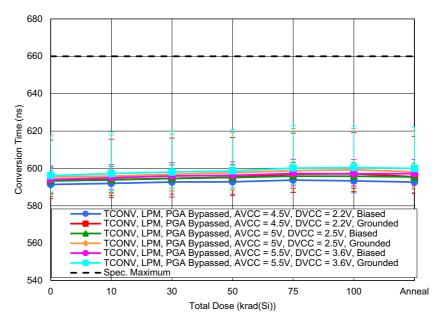
Figure 61. ISL73148SEH $\overline{CS}\downarrow$ to BUSY $\uparrow$ (t_{BUSYLH}) in normal operating mode with PGA Gain = 2, C_L = 10pF, and with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5V and DV_{CC} = 2.5V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 100ns.
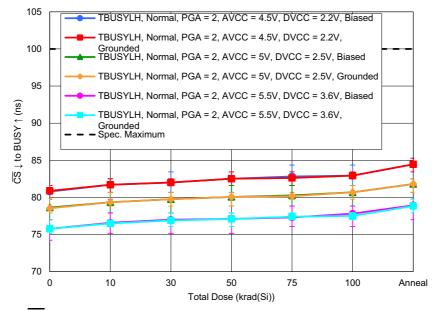

Figure 62. ISL73148SEH $\overline{CS}\downarrow$ to BUSY $\uparrow$ (t_{BUSYLH}) in normal operating mode with PGA bypassed, C_L = 10pF and with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5V and DV_{CC} = 2.5V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 30ns.
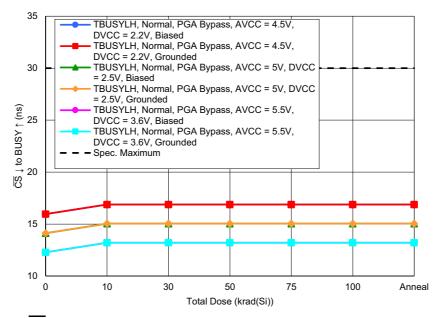
Figure 63. ISL73148SEH $\overline{CS}\downarrow$ to BUSY $\uparrow$ (t_{BUSYLH}) in low power mode with PGA Gain = 2, C_L = 10pF, and with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5V and DV_{CC} = 2.5V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 100ns.
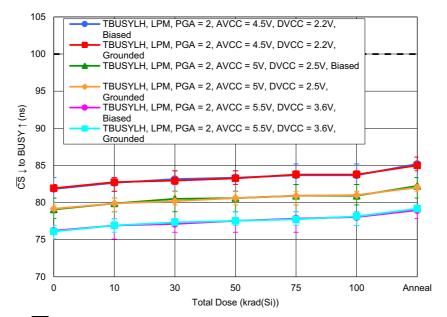

Figure 64. ISL73148SEH $\overline{CS}\downarrow$ to BUSY $\uparrow$ (t_{BUSYLH}) in low power mode with PGA bypassed, C_L = 10pF and with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5V and DV_{CC} = 2.5V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 30ns.
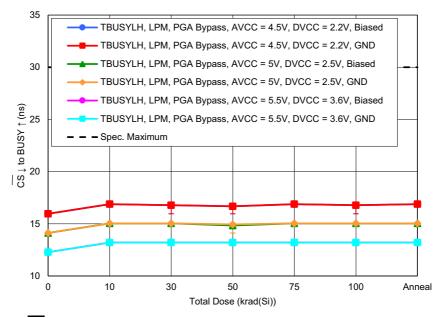
Figure 65. ISL73148SEH SDO Data Valid Delay from BUSY ↓ (t$_{DBUSYLSDOV}$) in normal operating mode with C$_L$ = 10pF and with AV$_{CC}$ = 4.5V and DV$_{CC}$ = 2.2V or AV$_{CC}$ = 5V and DV$_{CC}$ = 2.5V or AV$_{CC}$ = 5.5V and DV$_{CC}$ = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 0ns.
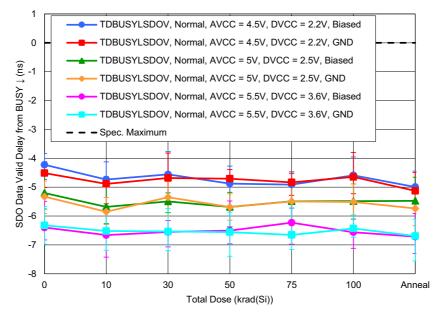

Figure 66. ISL73148SEH SDO Data Valid Delay from BUSY ↓ (t$_{DBUSYLSDOV}$) in low power mode with C$_L$ = 10pF and with AV$_{CC}$ = 4.5V and DV$_{CC}$ = 2.2V or AV$_{CC}$ = 5V and DV$_{CC}$ = 2.5V or AV$_{CC}$ = 5.5V and DV$_{CC}$ = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 0ns.
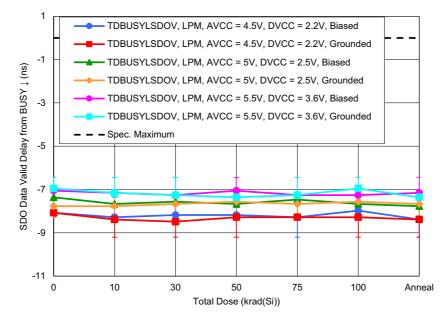
Figure 67. ISL73148SEH SDO Data Valid Delay from SCK ↑ ($t_{DSCKSDOV}$) in normal operating mode with C_L = 10pF, and with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5V and DV_{CC} = 2.5V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 20ns.

Figure 68. ISL73148SEH SDO Data Valid Delay from SCK ↑ ($t_{DSCKSDOV}$) in low power mode with C_L = 10pF, and with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5V and DV_{CC} = 2.5V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 20ns.
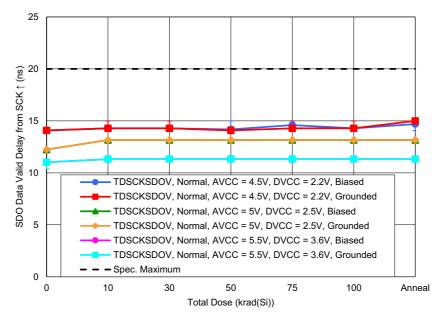
Figure 69. ISL73148SEH SDO Data Valid Hold Time from SCK ↑ (t$_{HSDOV}$) in normal operating mode with C$_L$ = 10pF and with AV$_{CC}$ = 4.5V and DV$_{CC}$ = 2.2V or AV$_{CC}$ = 5V and DV$_{CC}$ = 2.5V or AV$_{CC}$ = 5.5V and DV$_{CC}$ = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a minimum of 7ns.
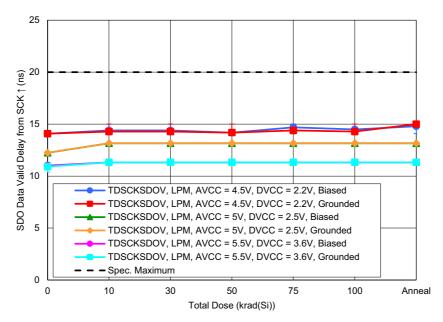

Figure 70. ISL73148SEH SDO Data Valid Hold Time from SCK ↑ (t$_{HSDOV}$) in low power mode with C$_L$ = 10pF and with AV$_{CC}$ = 4.5V and DV$_{CC}$ = 2.2V or AV$_{CC}$ = 5V and DV$_{CC}$ = 2.5V or AV$_{CC}$ = 5.5V and DV$_{CC}$ = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a minimum of 7ns.
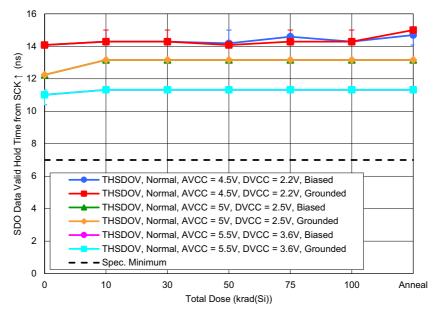
Figure 71. ISL73148SEH SDO Bus Acquisition Time from $\overline{CS}\downarrow$ ($t_{DCSLSDOL}$) in normal operating mode with C_L = 10pF and with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5V and DV_{CC} = 2.5V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 25ns.
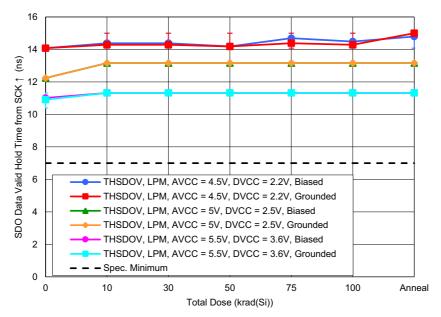

Figure 72. ISL73148SEH SDO Bus Acquisition Time from $\overline{CS}\downarrow$ ($t_{DCSLSDOL}$) in low power mode with C_L = 10pF and with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5V and DV_{CC} = 2.5V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 25ns.
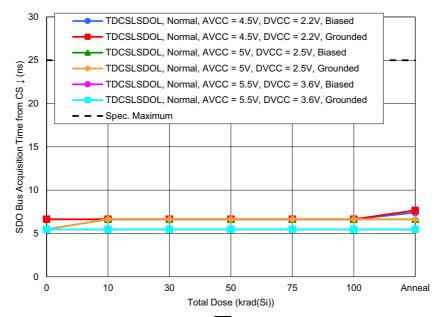
Figure 73. ISL73148SEH SDO Bus Relinquish Time after $\overline{CS}$ ↑ ($t_{DCSHSDOZ}$) in normal operating mode with C_L = 10pF and with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5V and DV_{CC} = 2.5V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 25ns.
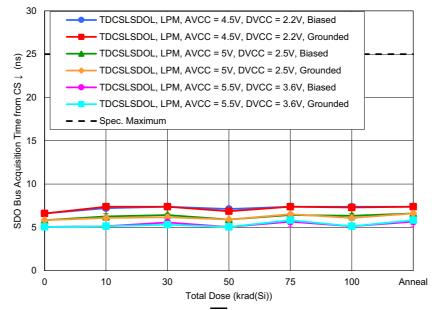

Figure 74. ISL73148SEH SDO Bus Relinquish Time after $\overline{CS}$↑ ($t_{DCSHSDOZ}$) in low power mode with C_L = 10pF and with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5V and DV_{CC} = 2.5V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 25ns.
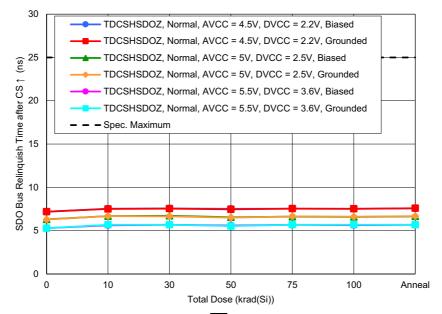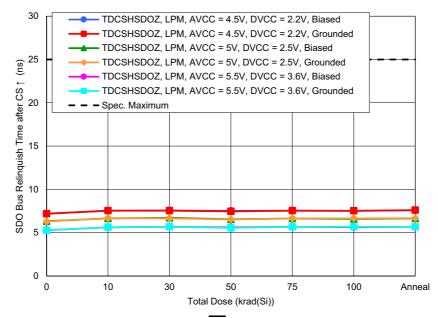
Figure 75. ISL73148SEH average G2:0, S2:0 to $\overline{CS}$↑ ($t_{SUDIGCSH}$) in normal operating mode with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5V and DV_{CC} = 2.5V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all pins. The datasheet limit is a minimum of 5ns.

Figure 76. ISL73148SEH average G2:0, S2:0 to $\overline{CS}$↑ ($t_{SUDIGCSH}$) in low power mode with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5V and DV_{CC} = 2.5V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all pins. The datasheet limit is a minimum of 15ns.

Figure 77. ISL73148SEH average G2:0, S2:0 from $\overline{CS}\uparrow$ ($t_{HDIGCSH}$) in normal operating mode with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5V and DV_{CC} = 2.5V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all pins. The datasheet limit is a minimum of 25ns. *Note:* the measured values are the actual maximum required hold times, so the datasheet limits are the maximums of the measured values.

Figure 78. ISL73148SEH average G2:0, S2:0 from $\overline{CS}\uparrow$ ($t_{HDIGCSH}$) in low power mode with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5V and DV_{CC} = 2.5V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all pins. The datasheet limit is a minimum of 10ns. *Note:* The measured values are the actual maximum required hold times, so the datasheet limits are the maximums of the measured values.

Figure 79. ISL73148SEH SCAN to $\overline{CS}$↑ ($t_{SCANCSH}$) in low power mode with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5V and DV_{CC} = 2.5V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a minimum of 20ns.
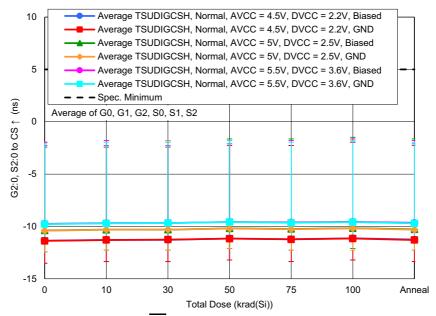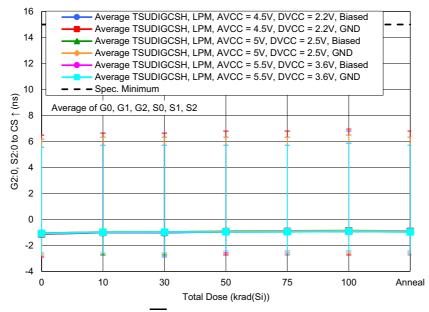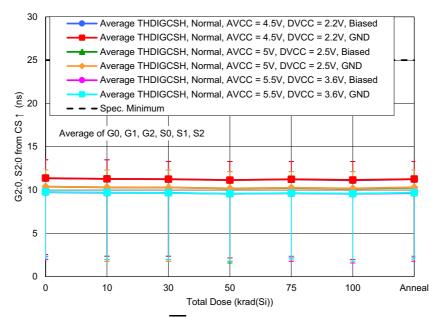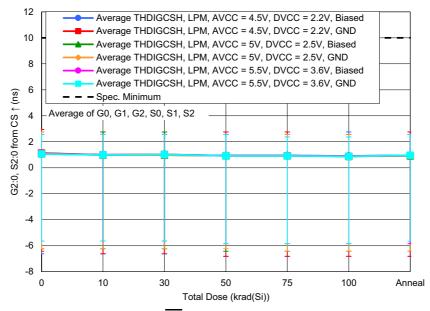

Figure 80. ISL73148SEH wake-up time from power-down mode (t_{WAKE}) in normal operating mode (but results also apply to LPM) with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5V and DV_{CC} = 2.5V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 25ns.

3. Discussion and Conclusion

This document reports the results of the LDR TID test of the ISL73148SEH radiation hardened 8-channel 14-Bit 900/480ksps SAR ADC. The irradiation of biased and grounded samples to 100krad(Si) at a LDR of 0.01rad(Si)/s was followed by a 168-hour anneal at 100ºC under bias. All datasheet parameters passed at all downpoints. No evidence of bias dependence was observed.

4. Revision History

Revision	Date	Description
1.00	Sep 28, 2022	Initial release.

Appendix

Table 3 lists the datasheet parameters that are considered indicative of part performance. These parameters are plotted in Figure 3 through Figure 80. All limits are taken from the ISL73148SEH datasheet, which may also have more details on test conditions.

Table 3. ISL73148SEH Datasheet Total Dose Parameters (TA = 25ºC)

Fig.	Parameter	Symbol	Test Conditions	Low Limit	High Limit	Unit
3	Integral Non-Linearity	INL	Normal Mode; PGA Gain = 2; AV_{CC} = 5V	-1.2	2	LSB
4			LPM; PGA Gain = 2; AV_{CC} = 5V			
5	Differential Non-Linearity	DNL	Normal Mode; PGA Gain = 2; AV_{CC} = 5V	-0.6	0.6	LSB
6			LPM; PGA Gain = 2; AV_{CC} = 5V			
7	Zero-Scale Error	V_{OFF}	Normal Mode; PGA Gain = 2; AV_{CC} = 5V	-26.5	23	LSB
8			Normal Mode; PGA Bypassed; AV_{CC} = 5V	-13	13	
9			LPM; PGA Gain = 2; AV_{CC} = 5V	-29	17	
10			LPM; PGA Bypassed; AV_{CC} = 5V	-13	13	
11	Positive Full-Scale Error	+FSE	Normal Mode; PGA Gain = 2; AV_{CC} = 5V	-33	26	LSB
12			Normal Mode; PGA Bypassed; AV_{CC} = 5V	-13.5	19.5	
13			LPM; PGA Gain = 2; AV_{CC} = 5V	-34	22.5	
14			LPM; PGA Bypassed; AV_{CC} = 5V	-13.5	18.5	
15	Negative Full-Scale Error	-FSE	Normal Mode; PGA Gain = 2; AV_{CC} = 5V	-33	26	LSB
16			Normal Mode; PGA Bypassed; AV_{CC} = 5V	-23.5	10.5	
17			LPM; PGA Gain = 2; AV_{CC} = 5V	-40	18	
18			LPM; PGA Bypassed; AV_{CC} = 5V	-22.5	11	
19	Signal-to-Noise Ratio	SNR	Normal Mode; PGA Gain = 2; AV_{CC} = 5V	75	-	dBFS
20			Normal Mode; PGA Bypassed; AV_{CC} = 5V	80	-	
21			LPM; PGA Gain = 2; AV_{CC} = 5V	75	-	
22			LPM; PGA Bypassed; AV_{CC} = 5V	80	-	
23	Signal-to-Noise + Distortion Ratio	SINAD	Normal Mode; PGA Gain = 2; AV_{CC} = 5V	74	-	dBFS
24			Normal Mode; PGA Bypassed; AV_{CC} = 5V	79	-	
25			LPM; PGA Gain = 2; AV_{CC} = 5V	74	-	
26			LPM; PGA Bypassed; AV_{CC} = 5V	79	-	
27	Effective Number of Bits	ENOB	Normal Mode; PGA Gain = 2; AV_{CC} = 5V	11.8	-	bits
28			Normal Mode; PGA Bypassed; AV_{CC} = 5V	12.8	-	
29			LPM; PGA Gain = 2; AV_{CC} = 5V	11.8	-	
30			LPM; PGA Bypassed; AV_{CC} = 5V	12.8	-	

Table 3. ISL73148SEH Datasheet Total Dose Parameters (TA = 25ºC)

Fig.	Parameter	Symbol	Test Conditions	Low Limit	High Limit	Unit
31	Total Harmonic Distortion	THD	Normal Mode; PGA Gain = 2; AV_{CC} = 5V	83	-	dBFS
			Normal Mode; PGA Bypassed; AV_{CC} = 5V	85	-	
32			LPM; PGA Gain = 2; AV_{CC} = 5V	83	-	
			LPM; PGA Bypassed; AV_{CC} = 5V	85	-	
33	Spurious Free Dynamic Range	SFDR	Normal Mode; PGA Gain = 2; AV_{CC} = 5V	90	-	dBFS
			Normal Mode; PGA Bypassed; AV_{CC} = 5V			
34			LPM; PGA Gain = 2; AV_{CC} = 5V	90	-	
			LPM; PGA Bypassed; AV_{CC} = 5V			
35	Input Leakage Current	IA_{IN}	A_{IN} = 0V, 2.6V	-1	1	µA
36	REF Input Current	I_{REF}	Normal Mode, LPM; PGA Gain = 2, bypassed; V_{REF} = 2.6V	-	400	µA
37	Analog Supply Current – Active	I_{AVCC}	Normal Mode; PGA Gain = 2; AV_{CC} = 5V	-	20.5	mA
			Normal Mode; PGA Bypassed; AV_{CC} = 5V	-	23	
38			LPM; PGA Gain = 2; AV_{CC} = 5V	-	16.9	
			LPM; PGA Bypassed; AV_{CC} = 5V	-	17.5	
39	Analog Supply Current – Static	I_{STATIC}	Normal Mode; PGA Gain = 2; AV_{CC} = 5V	-	13	mA
			Normal Mode; PGA Bypassed; AV_{CC} = 5V	-	9	
40			LPM; PGA Gain = 2; AV_{CC} = 5V	-	7.5	
			LPM; PGA Bypassed; AV_{CC} = 5V	-	7.5	
41	Analog Supply Current – Sleep	I_{SLAVCC}	Normal Mode; AV_{CC} = 5V	-	-	µA
42	Digital Supply Current – Active	I_{DVCC}	Normal Mode; PGA Gain = 2; DV_{CC} = 2.5V	-	600	µA
			Normal Mode; PGA Bypassed; DV_{CC} = 2.5V	-	700	
43			LPM; PGA Gain = 2; DV_{CC} = 2.5V	-	600	
			LPM; PGA Bypassed; DV_{CC} = 2.5V	-	700	
44	Digital Supply Current – Static	I_{STDVCC}	Normal Mode; PGA Gain = 2; DV_{CC} = 2.5V	-	110	µA
			Normal Mode; PGA Bypassed; DV_{CC} = 2.5V	-	80	
45			LPM; PGA Gain = 2; DV_{CC} = 2.5V	-	130	
			LPM; PGA Bypassed; DV_{CC} = 2.5V	-	110	
46	High-Level Input	V_{IH}	DV_{CC} = 2.2V, 3.6V	$0.8 \times DV_{CC}$	-	V
47	Low-Level Input	V_{IL}	DV_{CC} = 2.2V, 3.6V	-	$0.2 \times DV_{CC}$	mV

Table 3. ISL73148SEH Datasheet Total Dose Parameters (TA = 25ºC)

Fig.	Parameter	Symbol	Test Conditions	Low Limit	High Limit	Unit
48	Input Current ($\overline{CS}$, SCK, S2, S1, S0, G1, G0)	I_{IN}	DV_{CC} = 2.2V; V_{IN} = 0V, 2.2V	-1	1	µA
			DV_{CC} = 3.6V; V_{IN} = 0V, 3.6V			
49	High-Level Output	V_{OH}	DV_{CC} – Output; I_O = -500µA	DV_{CC} - 0.2	-	V
50	Low-Level Output	V_{OL}	I_O = 500µA	-	0.2	V
51	Hi-Z Output Leakage Current	I_{OZ}	DV_{CC} = 3.6V, 2.2V; V_{OUT} = 0V to DV_{CC}	-1	1	µA
52	$\overline{PD}$ Input Resistance	R_{INPDL}	Internal pull-up resistance to DV_{CC}	400	600	kΩ
53	LPM Input Resistance	R_{INLPM}	Internal pull-down resistance to GND; DV_{CC} = 2.2V, 3.6V	400	600	kΩ
54	G2/PGABP Input Resistance	R_{ING2BP}	DV_{CC} = 2.2V; V_{IN} = 0V, 2.2V	180	320	kΩ
			DV_{CC} = 3.6V; V_{IN} = 0V, 3.6V			
55	COM Output Voltage	V_{OCOM}	COM pin bypassed to ground with 0.1µF ceramic capacitor	$V_{REF}/2$ - 0.002	$V_{REF}/2$ + 0.002	V
56	COM Input Resistance	R_{INCOM}	COM pin driven to GND	80	120	kΩ
57	Conversion Time	t_{CONV}	Normal Mode; PGA enabled; AV_{CC} = 4.5V, 5V, 5.5V; DV_{CC} = 2.2V, 2.5V, 3.6V	-	1550	ns
58			Normal Mode; PGA bypassed; AV_{CC} = 4.5V, 5V, 5.5V; DV_{CC} = 2.2V, 2.5V, 3.6V	-	660	
59			LPM; PGA enabled; AV_{CC} = 4.5V, 5V, 5.5V; DV_{CC} = 2.2V, 2.5V, 3.6V	-	1550	
60			LPM; PGA bypassed; AV_{CC} = 4.5V, 5V, 5.5V; DV_{CC} = 2.2V, 2.5V, 3.6V	-	660	
61	$\overline{CS}$ ↓ to BUSY ↑	t_{BUSYLH}	Normal Mode; PGA Gain = 2; AV_{CC} = 4.5V, 5V, 5.5V; DV_{CC} = 2.2V, 2.5V, 3.6V; C_L = 10pF	-	100	ns
62			Normal Mode; PGA bypassed; AV_{CC} = 4.5V, 5V, 5.5V; DV_{CC} = 2.2V, 2.5V, 3.6V; C_L = 10pF	-	30	
63			LPM; PGA Gain = 2; AV_{CC} = 4.5V, 5V, 5.5V; DV_{CC} = 2.2V, 2.5V, 3.6V; C_L = 10pF	-	100	
64			LPM; PGA bypassed; AV_{CC} = 4.5V, 5V, 5.5V; DV_{CC} = 2.2V, 2.5V, 3.6V; C_L = 10pF	-	30	
65	SDO Data Valid Delay from BUSY ↓	$t_{DBUSYLSDOV}$	Normal Mode; AV_{CC} = 4.5V, 5V, 5.5V; DV_{CC} = 2.2V, 2.5V, 3.6V; C_L = 10pF	-	0	ns
66			LPM; AV_{CC} = 4.5V, 5V, 5.5V; DV_{CC} = 2.2V, 2.5V, 3.6V; C_L = 10pF	-	0	

Table 3. ISL73148SEH Datasheet Total Dose Parameters (TA = 25ºC)

Fig.	Parameter	Symbol	Test Conditions	Low Limit	High Limit	Unit
67	SDO Data Valid Delay from SCK ↑	$t_{DSCKSDOV}$	Normal Mode; AV_{CC} = 4.5V, 5V, 5.5V; DV_{CC} = 2.2V, 2.5V, 3.6V; C_L = 10pF	-	20	ns
68			LPM; AV_{CC} = 4.5V, 5V, 5.5V; DV_{CC} = 2.2V, 2.5V, 3.6V; C_L = 10pF	-	20	
69	SDO Data Valid Hold Time from SCK ↑	t_{HSDOV}	Normal Mode; AV_{CC} = 4.5V, 5V, 5.5V; DV_{CC} = 2.2V, 2.5V, 3.6V; C_L = 10pF	7	-	ns
70			LPM; AV_{CC} = 4.5V, 5V, 5.5V; DV_{CC} = 2.2V, 2.5V, 3.6V; C_L = 10pF	7	-	
71	SDO Bus Acquisition Time from $\overline{CS}$ ↓	$t_{DCSLSDOL}$	Normal Mode; AV_{CC} = 4.5V, 5V, 5.5V; DV_{CC} = 2.2V, 2.5V, 3.6V; C_L = 10pF	-	25	ns
72			LPM; AV_{CC} = 4.5V, 5V, 5.5V; DV_{CC} = 2.2V, 2.5V, 3.6V; C_L = 10pF	-	25	
73	SDO Bus Relinquish Time after $\overline{CS}$ ↑	$t_{DCSHSDOZ}$	Normal Mode; AV_{CC} = 4.5V, 5V, 5.5V; DV_{CC} = 2.2V, 2.5V, 3.6V; C_L = 10pF	-	25	ns
74			LPM; AV_{CC} = 4.5V, 5V, 5.5V; DV_{CC} = 2.2V, 2.5V, 3.6V; C_L = 10pF	-	25	
75	G2:0, S2:0 to $\overline{CS}$ ↑	$t_{SUDIGCSH}$	Normal Mode; AV_{CC} = 4.5V, 5V, 5.5V; DV_{CC} = 2.2V, 2.5V, 3.6V	5	-	ns
76			LPM; AV_{CC} = 4.5V, 5V, 5.5V; DV_{CC} = 2.2V, 2.5V, 3.6V	15	-	
77	G2:0, S2:0 from $\overline{CS}$ ↑	$t_{HDIGCSH}$	Normal Mode; AV_{CC} = 4.5V, 5V, 5.5V; DV_{CC} = 2.2V, 2.5V, 3.6V	25	-	ns
78			LPM; AV_{CC} = 4.5V, 5V, 5.5V; DV_{CC} = 2.2V, 2.5V, 3.6V	10	-	
79	SCAN to $\overline{CS}$ ↑	$t_{SCANCSH}$	LPM; AV_{CC} = 4.5V, 5V, 5.5V; DV_{CC} = 2.2V, 2.5V, 3.6V	20	-	ns
80	Wake-Up time from Power-Down Mode	t_{WAKE}	Normal Mode (but results apply to LPM); AV_{CC} = 4.5V, 5V, 5.5V; DV_{CC} = 2.2V, 2.5V, 3.6V	-	25	µs

Related Literature

For a full list of related documents, visit our website:

▪ ISL73148SEH device page
▪ MIL-STD-883 test method 1019

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