ISL71441SLH

Low Dose Rate Total Ionizing Dose Testing of the ISL71441SLH 12V Half-Bridge GaN FET Driver

Introduction

This report summarizes the results of Low Dose Rate (LDR) total ionizing dose (TID) testing of the ISL71441SLH 12V Half Bridge GaN FET Driver. The test was conducted to provide an assessment of the total dose hardness of the part and to provide an estimate of the bias sensitivity. Parts were irradiated either under bias or with all pins grounded at LDR (0.01rad(Si)/s) to 100krad(Si). The ISL71441SLH is rated to 75krad(Si) at LDR and is assurance tested on a wafer-by-wafer basis to the datasheet limits.

Product Description

The ISL71441SLH is a Radiation Hardened PWM input 12V Half-Bridge GaN FET Driver that drives low $r_{DS(ON)}$ Gallium Nitride FETs for DC/DC switching regulators. An integrated programmable GaN FET gate drive voltage, high-side bootstrap switch, and strong gate drive current provide a compact and robust GaN FET half-bridge driver.

The ISL71441SLH can interface directly to the ISL73847SLH dual-phase PWM buck controller to create a high-efficiency point-of-load regulator to power many of the latest low voltage high current FPGA and DSP digital core rails.

The ISL71441SLH operates across the military temperature range from -55ºC to +125ºC and is available in a 20Ld plastic 5x5mm QFN package. The pin assignments for the ISL71441SLH are shown in Figure 1, and the pin descriptions are shown in Table 1.

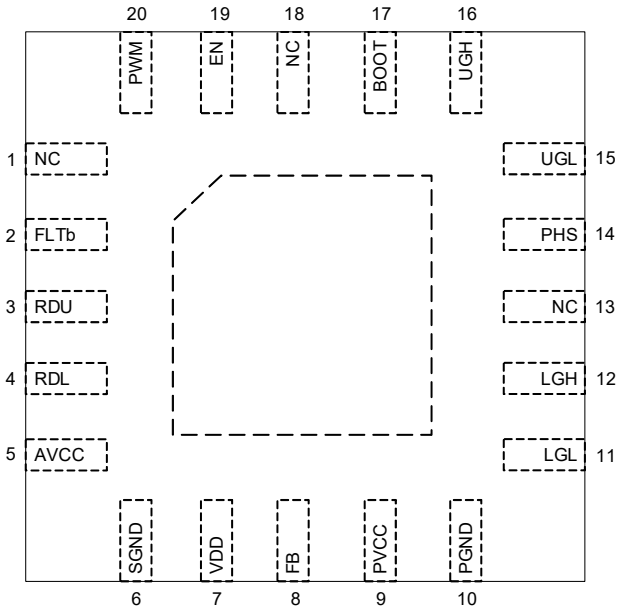


Figure 1. ISL71441SLH Pin Assignments - Top View

Table 1. ISL71441SLH Pin Descriptions

Pin Number	Pin Name	Description
1	NC	No connection.
2	FLTb	I/O pin. As an open-drain output, FLTb is an active low indicator for when EN = 0, AVCC UVLO, PVCC UVLO or in an over-temperature fault. As a high-impedance input, FLTb disables the driver outputs when driven low. Place a pull-resistor on the FLTb pin to AVCC. Place a 10pF capacitor from FLTb to GND for SET mitigation.
3	RDU	Dead time delay control for the high-side turn-on. A 1kΩ-10kΩ resistor to GND sets the rising edge delay of Upper Gate High (UGH) to the falling edge of Lower Gate Low (LGL) in the range of 5ns to 50ns. Connect RDU to SGND for 5ns delay.
4	RDL	Dead time delay control for low-side turn-on. A 1kΩ-10kΩ resistor to GND sets the rising edge delay of Lower Gate High (LGH) to the falling edge of Upper Gate Low (UGL) in the range of 5ns-50ns. Connect RDL to SGND for 5ns delay.
5	AVCC	Output of the internal 5V LDO regulator for chip bias. Input is VDD. A minimum of 1µF ceramic decoupling capacitor is necessary on AVCC to SGND.
6	SGND	Analog signal GND. Anti-parallel diodes are connected between SGND and PGND.
7	VDD	Input supply to chip. Bias range is 4.75V to 18V.
8	FB	PVCC LDO error amplifier inverting input. A resistor divider network from FB to PVCC and SGND sets the PVCC LDO output voltage. If FB is connected to PVCC, PVCC output voltage is 4.5V.
9	PVCC	Output of the LDO for the low-side gate drive voltage. Recommended PVCC range is 4.5V to 5.5V. A minimum 1µF ceramic decoupling capacitor is necessary on PVCC to PGND.
10	PGND	Low-side driver output reference pin. Anti-parallel diodes are connected between SGND and PGND.
11	LGL	Low-side sink driver for gate turn-off. Connect this pin to LGH and to the GaN FET gate.
12	LGH	Low-side source driver for gate turn-on. Connect this pin to LGL and to the GaN FET gate.
13	NC	No connection.
14	PHS	High-side GaN FET source reference. Connect to the phase switching node of the half-bridge.
15	UGL	High-side sink driver for gate turn-off. Connect this pin to UGH and to the GaN FET gate.
16	UGH	High-side source driver for gate turn-on. Connect this pin to UGL and to the GaN FET gate.
17	BOOT	High-side bootstrap bias pin. Connect a bootstrap capacitor from this pin to PHS. An internal boostrap switch refreshes the bootstrap capacitor when PWM = 0 and PHS voltage is within 300mV of PGND.
18	NC	No connection.
19	EN	Enable input pin. When EN is low, driver outputs are in a high-impedance state and do not respond to PWM inputs. The PVCC LDO is shutdown and the FLTb pin is internally pulled low. When EN is high, the PVCC LDO is enabled and the driver outputs respond to PWM inputs.
20	PWM	Tri-Level PWM input pin. Logic high turns on the high-side gate driver. Logic low turns on the low-side gate driver. Mid-Level actively turns off both gate drivers. Internal pull-up and pull-down resistors bias pin to mid-level when not externally driven.
EPAD	-	Package bottom thermal pad. Connect to SGND and PGND pins.

Contents

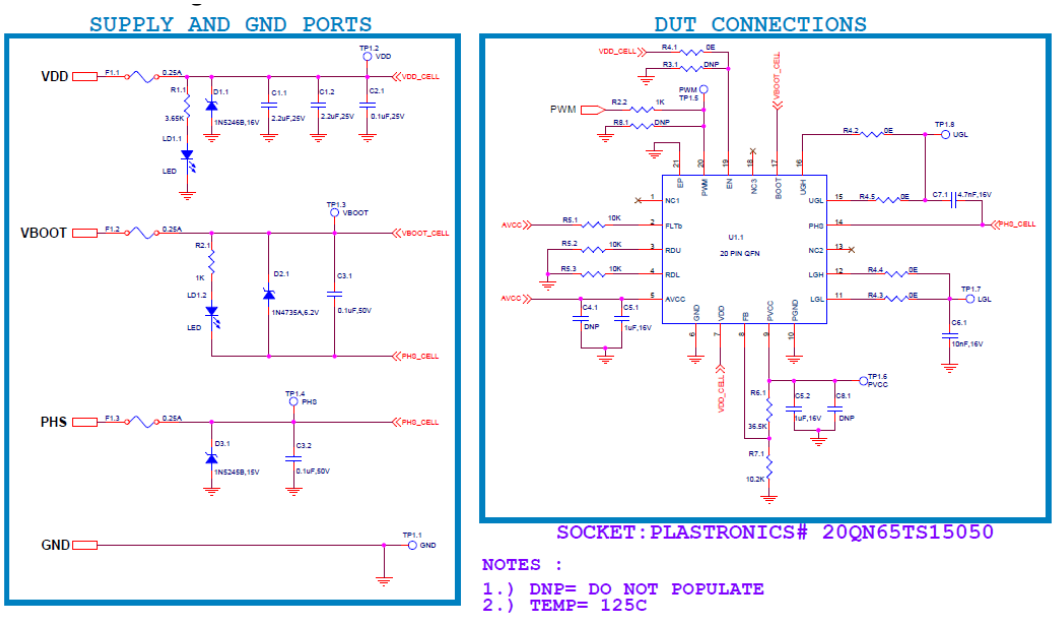
1. Test Description

1.1 Irradiation Facility

LDR testing was performed at a dose rate of 0.01rad(Si)/s using a Hopewell Designs N40 vault-type LDR irradiator. The irradiator is located in the Palm Bay, Florida, Renesas facility. A PbAl box shielded the test fixture and devices under test against low energy, secondary gamma radiation.

1.2 Test Fixturing

Figure 2 shows the configuration used for the biased TID testing.



CONN. NAME	CURRENT	STATIC	DYNAMIC
VDD	4mA/DEVICE	+13.2V	+13.2V
PHS	4mA/DEVICE	+13.2V	1KHz(0 TO +13.2V)50% DUTY CYCLE
VBOOT	4mA/DEVICE	+18.7V	+5.5V FLOATING SUPPLY
PWM		+5.5V	10KHz(0 TO +5.5V) 50%DUTY CYCLE

Figure 2. ISL71441SLH Bias Configuration

1.3 Characterization Equipment and Procedures

All electrical testing was performed outside the irradiator using the production Automated Test Equipment (ATE) with data logging at each downpoint. Downpoint electrical testing was performed at room temperature.

1.4 Experimental Matrix

Irradiation was performed in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of ten samples irradiated at LDR under bias and eight irradiated at LDR with all pins grounded. Two control units were used.

The 20 ISL71441SLH samples were drawn from wafer lot F6V880.2. All samples were packaged in the 20Ld QFN.

1.5 Downpoints

Planned irradiation downpoints for the LDR test were 0krad(Si), 10krad(Si), 30krad(Si), 50krad(Si), 60krad(Si), 75krad(Si), and 100krad(Si).

2. Results

TID testing of the ISL71441SLH is complete. All tested parameters passed the datasheet limits. Table 2 summarizes the results.

2.1 Attributes Data

Table 2. ISL71441SLH Attributes Data

Dose Rate (rad(Si)/s)	Condition	Sample Size	Downpoint	Pass[1]	Fail
0.01	Biased (Figure 2)	10	Pre-irradiation	10	0
			10krad(Si)	10	0
			30krad(Si)	10	0
			50krad(Si)	10	0
			60krad(Si)	10	0
			75krad(Si)	10	0
			100krad(Si)	10	0
0.01	Grounded	8	Pre-irradiation	8	0
			10krad(Si)	8	0
			30krad(Si)	8	0
			50krad(Si)	8	0
			60krad(Si)	8	0
			75krad(Si)	8	0
			100krad(Si)	8	0

1. A Pass indicates a sample that passes all datasheet limits.

2.2 Variables Data

The plots in Figure 3 through Figure 27 illustrate the LDR response of the selected parameters shown in Table 3. The plots show the average tested values of the parameters as a function of the total dose for each irradiation condition, biased, and grounded. The plots also include error bars at each downpoint, representing the samples' minimum and maximum measured values. However, in some plots, the error bars might not be visible due to their values compared to the scale of the graph.

All samples passed the datasheet limits after irradiation at LDR to each level up to 100krad(Si).

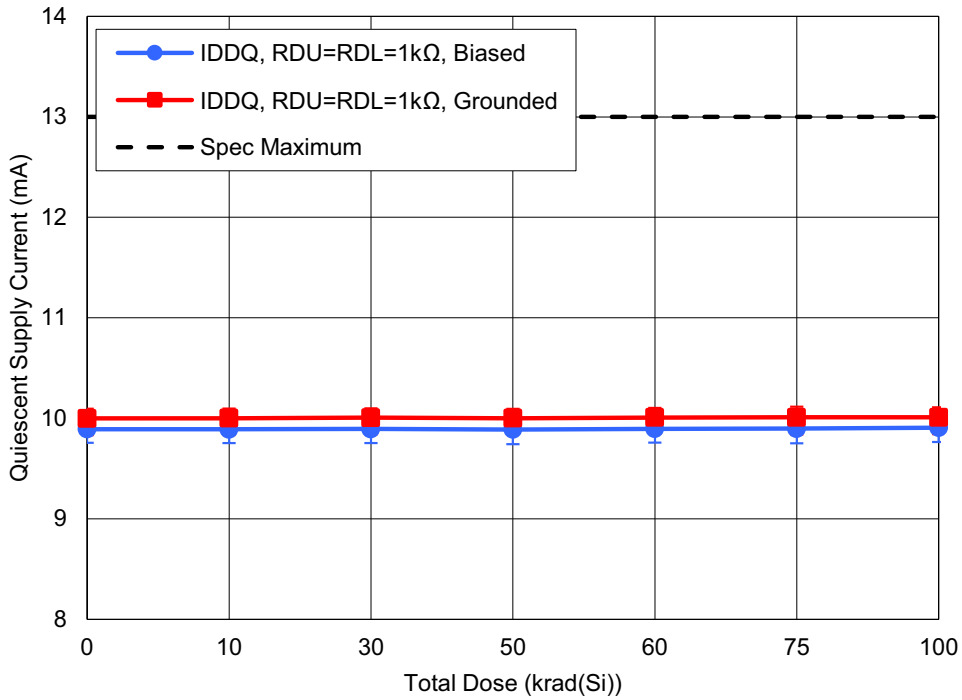


Figure 3. ISL71441SLH quiescent supply current (I_{DDQ}) with V_{DD} = 13.2V, EN = V_{DD}, PWM = Float, and RDU = RDL = 1kΩ to GND as a function of LDR irradiation for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 13mA.

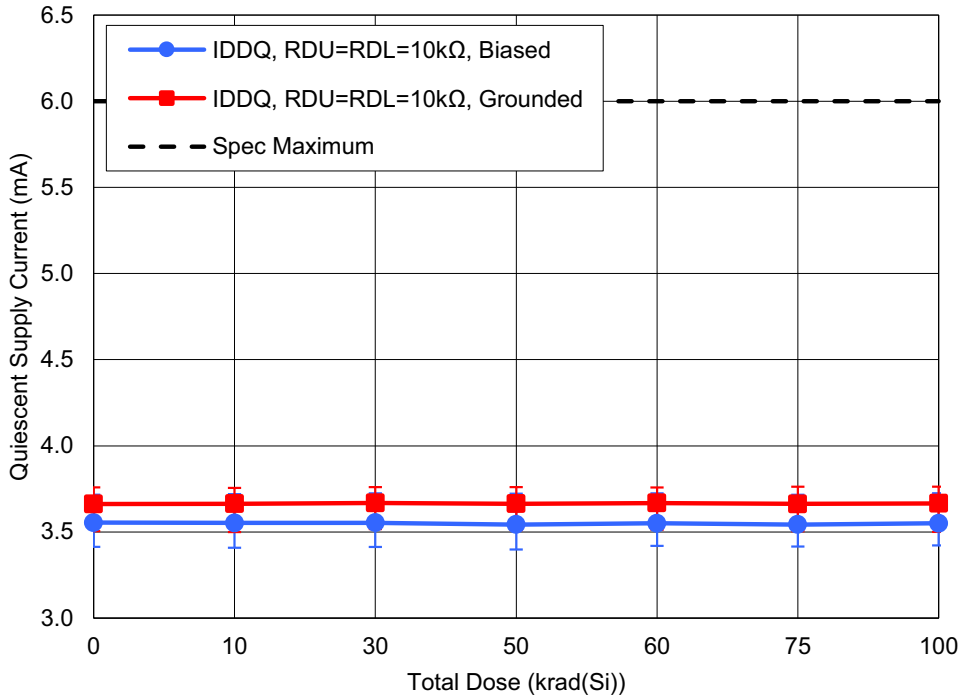


Figure 4. ISL71441SLH quiescent supply current (I_{DDQ}) with V_{DD} = 13.2V, EN = V_{DD}, PWM = Float, and RDU = RDL = 10kΩ to GND as a function of LDR irradiation for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 6mA.

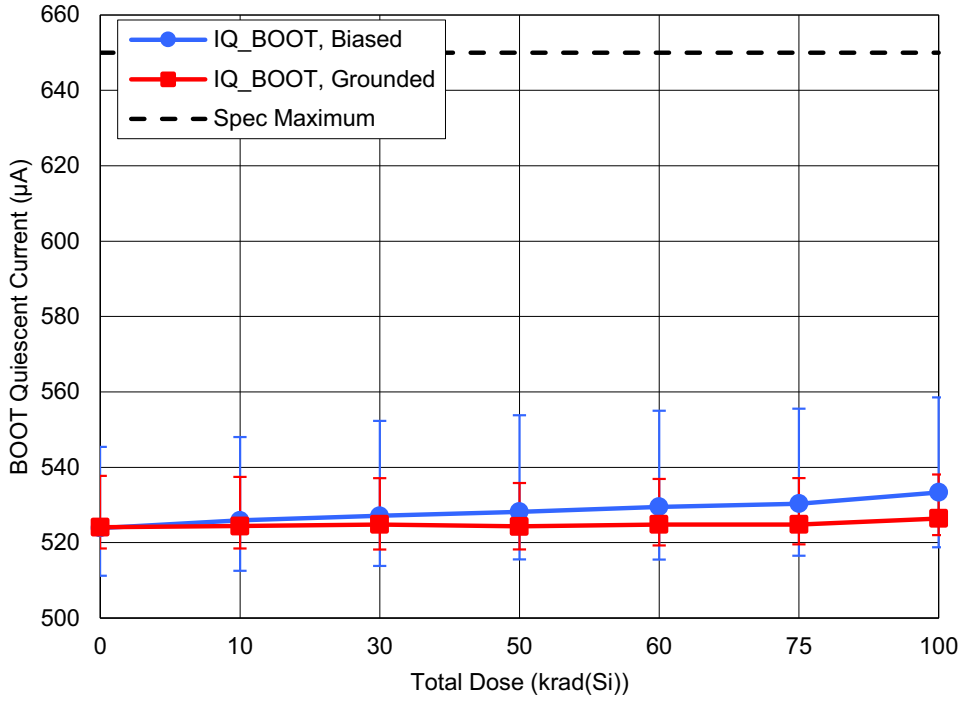


Figure 5. ISL71441SLH BOOT quiescent supply current (I_{Q_BOOT}) with V_{DD} = 13.2V, EN = V_{DD}, PWM = Float, and BOOT-PHS = 4.5V as a function of LDR irradiation for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 650µA.

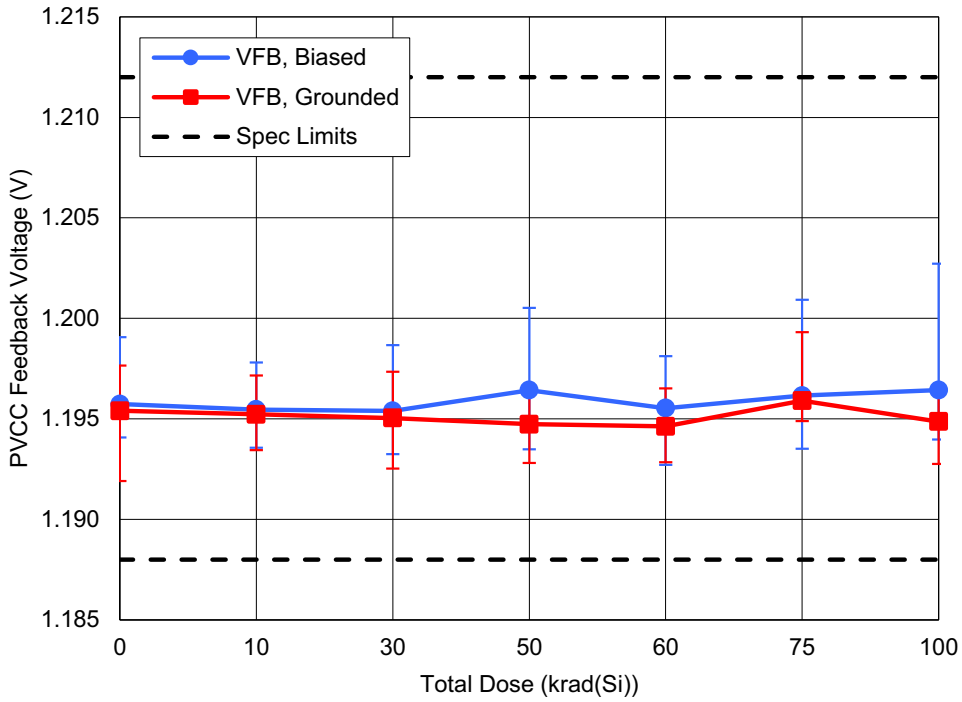


Figure 6. ISL71441SLH PVCC feedback voltage (V_{FB}) with V_{DD} = 13.2V as a function of LDR irradiation for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 1.188V and a maximum of 1.212V.

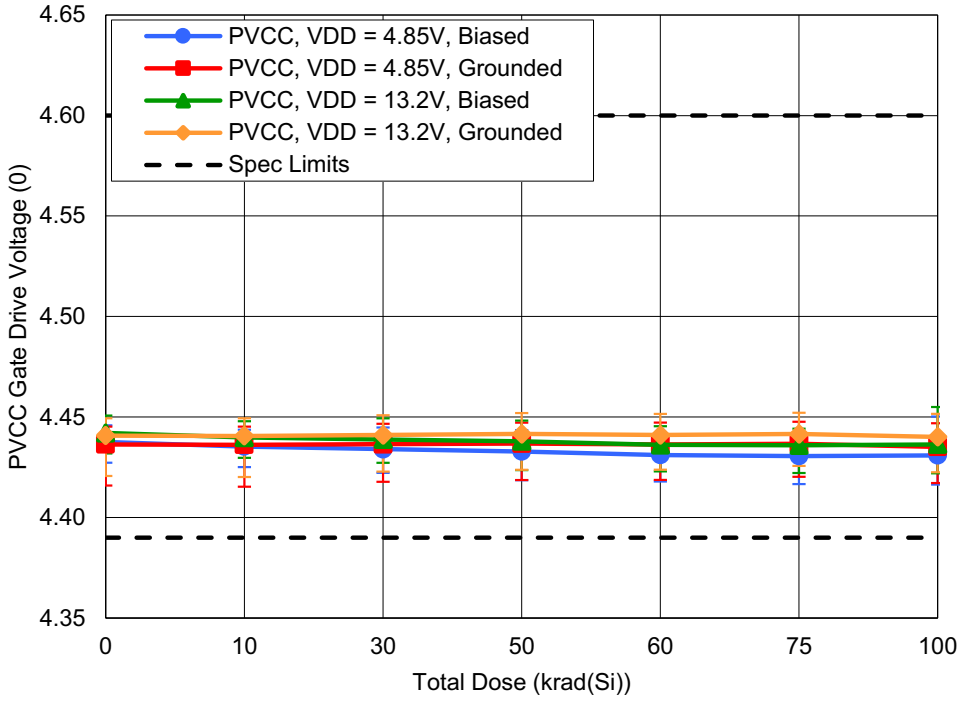


Figure 7. ISL71441SLH PVCC gate drive voltage (PVCC) with V_{DD} = 4.85V or 13.2V, FB = PVCC, and I_{OUT} = 150mA as a function of LDR irradiation for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 4.39V and a maximum of 4.6V.

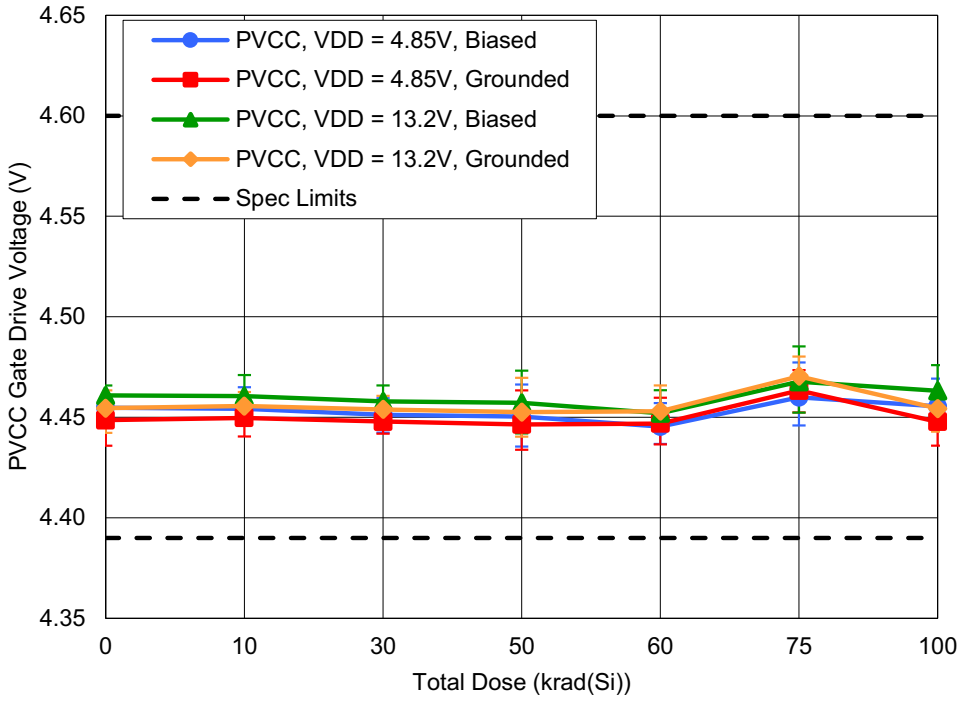


Figure 8. ISL71441SLH PVCC gate drive voltage (PVCC) with V_{DD} = 4.85V or 13.2V, FB = 0.266 • PVCC, and I_{OUT} = 150mA as a function of LDR irradiation for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 4.39V and a maximum of 4.6V.

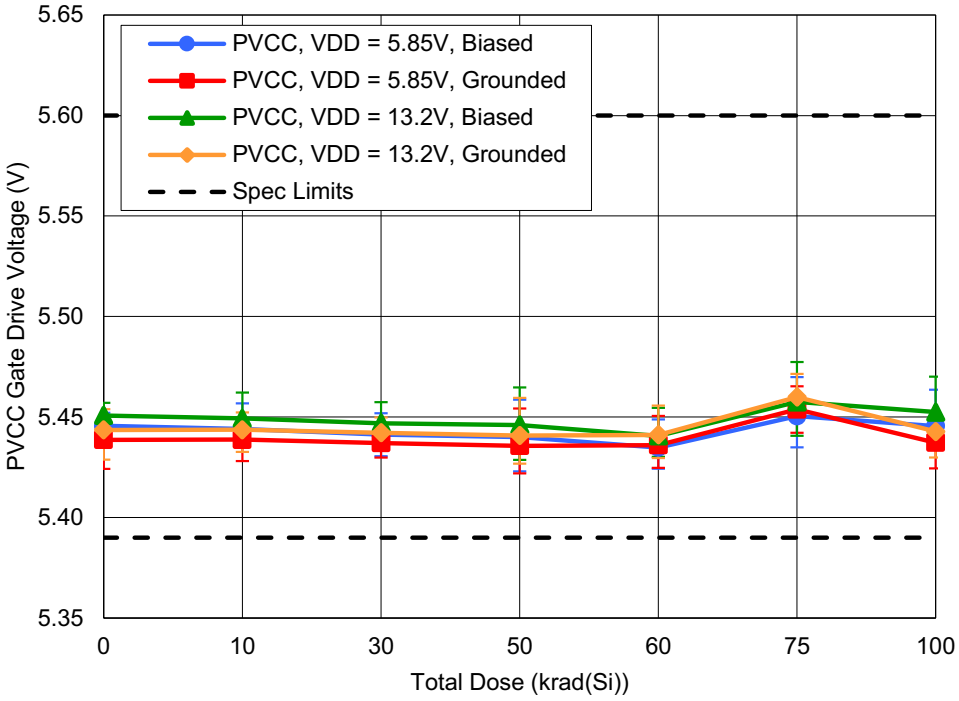


Figure 9. ISL71441SLH PVCC gate drive voltage (PVCC) with V_{DD} = 5.85V or 13.2V, FB = 0.218 • PVCC, and I_{OUT} = 150mA as a function of LDR irradiation for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 5.39V and a maximum of 5.6V.

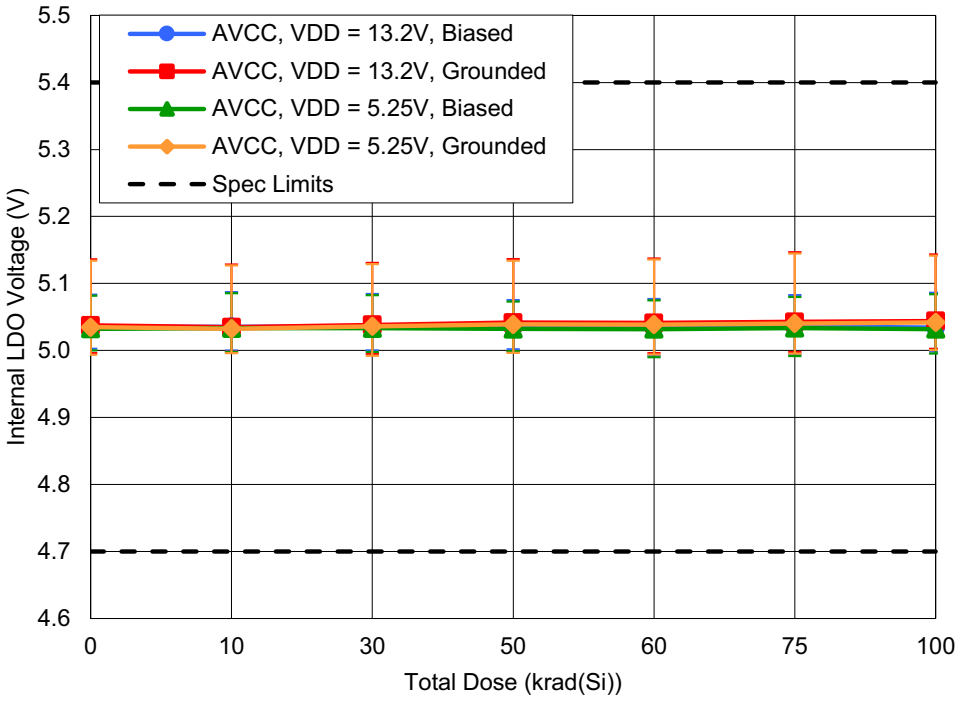


Figure 10. ISL71441SLH internal LDO voltage (AVCC) with V_{DD} = 5.25V or 13.2V, and with I_{OUT} = 20mA as a function of LDR irradiation for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 4.7V and a maximum of 5.4V.

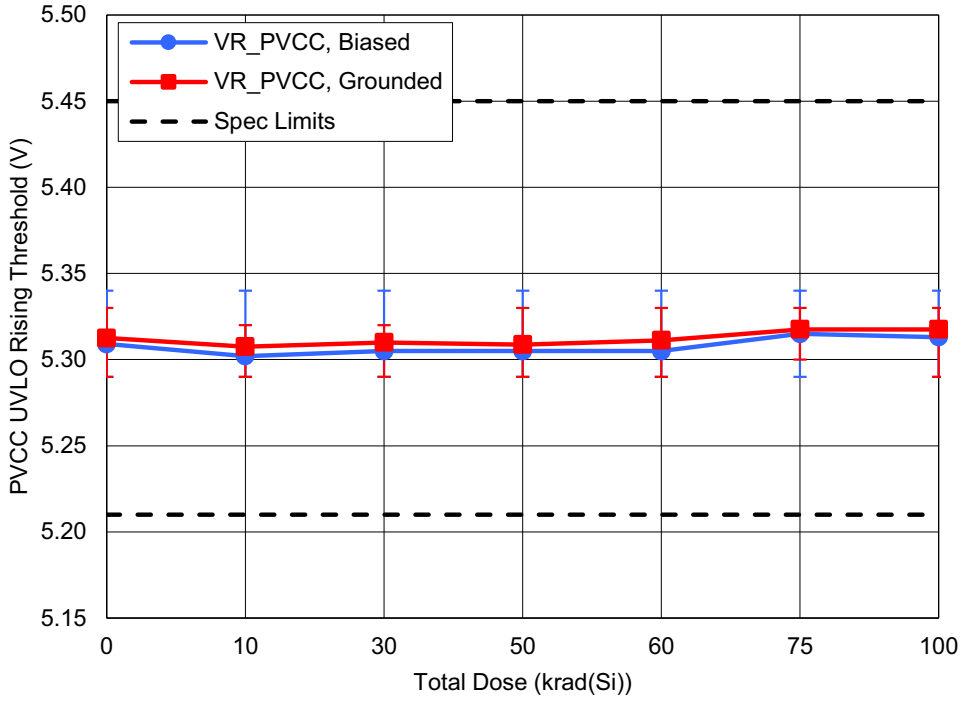


Figure 11. ISL71441SLH PVCC UVLO rising threshold (VR_{PVCC}) with V_{DD} = 13.2V, PVCC = 5.5V and with external FB resistors, as a function of LDR irradiation for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 5.21V and a maximum of 5.45V.

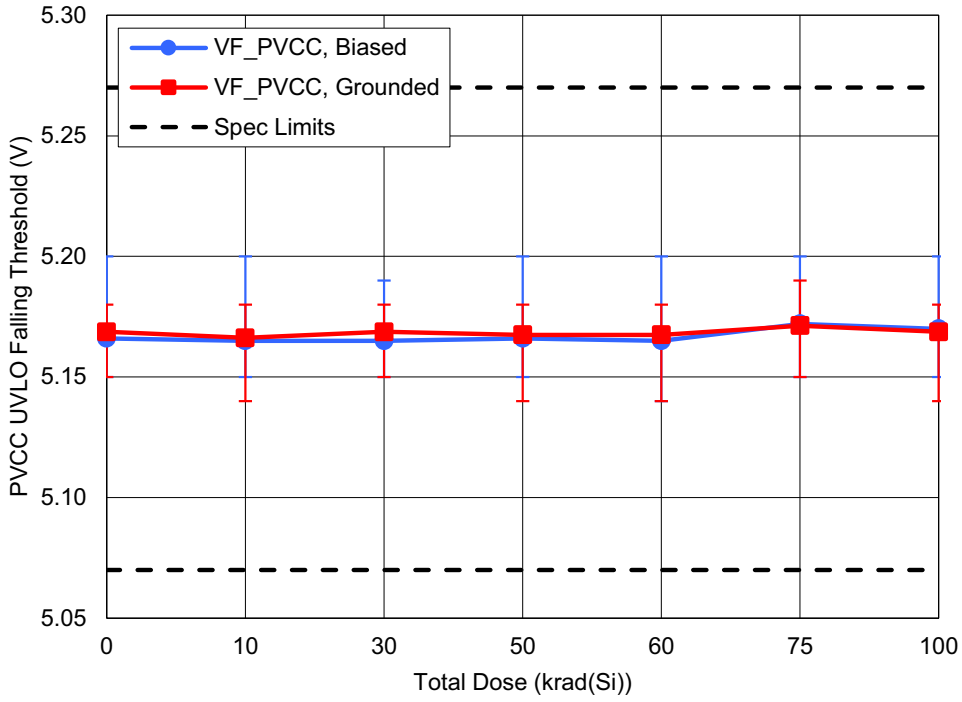


Figure 12. ISL71441SLH PVCC UVLO falling threshold (VF_{PVCC}) with V_{DD} = 13.2V, PVCC = 5.5V and with external FB resistors as a function of LDR irradiation for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 5.07V and a maximum of 5.27V.

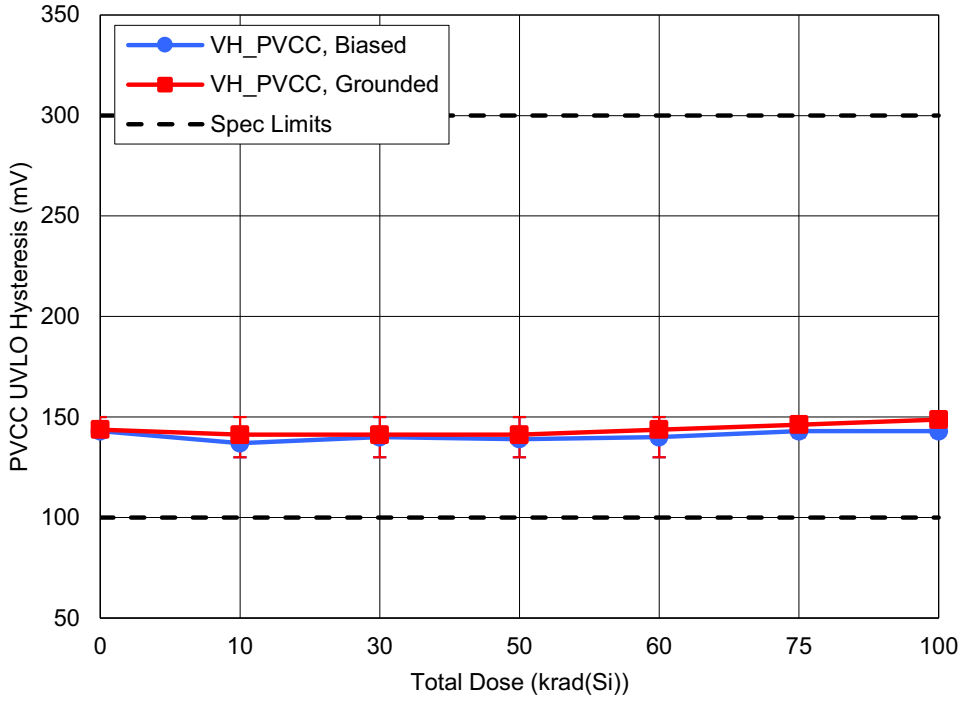


Figure 13. ISL71441SLH PVCC UVLO hysteresis (VH_{PVCC}) with V_{DD} = 13.2V as a function of LDR irradiation for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 100mV and a maximum of 300mV.

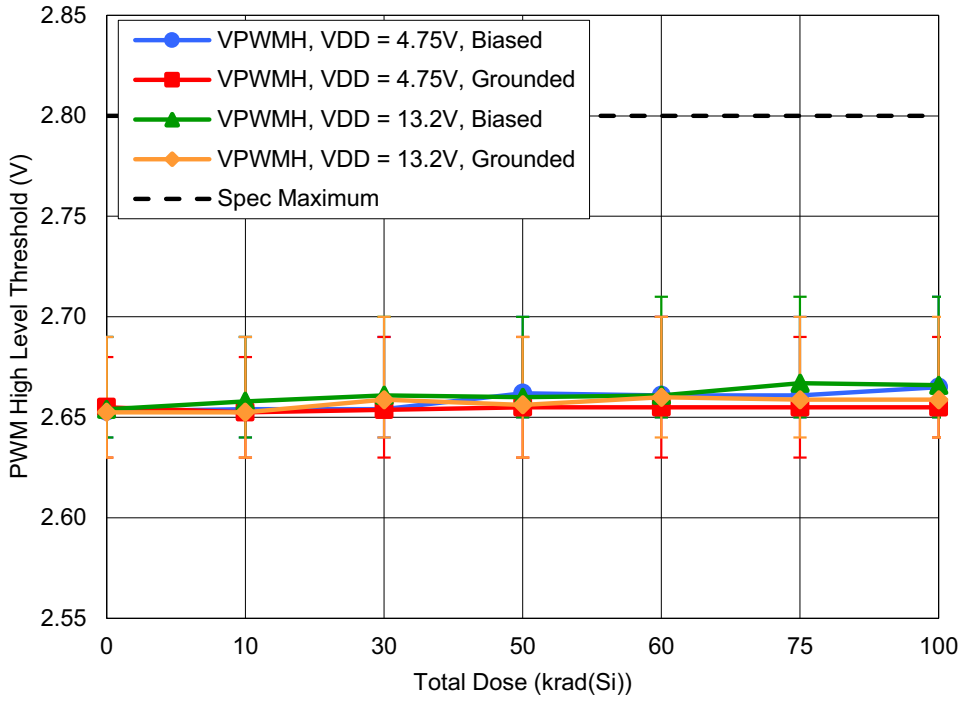


Figure 14. ISL71441SLH PWM high level threshold (V_{PWMH}) with V_{DD} = 4.75V or 13.2V as a function of LDR irradiation for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 2.8V.

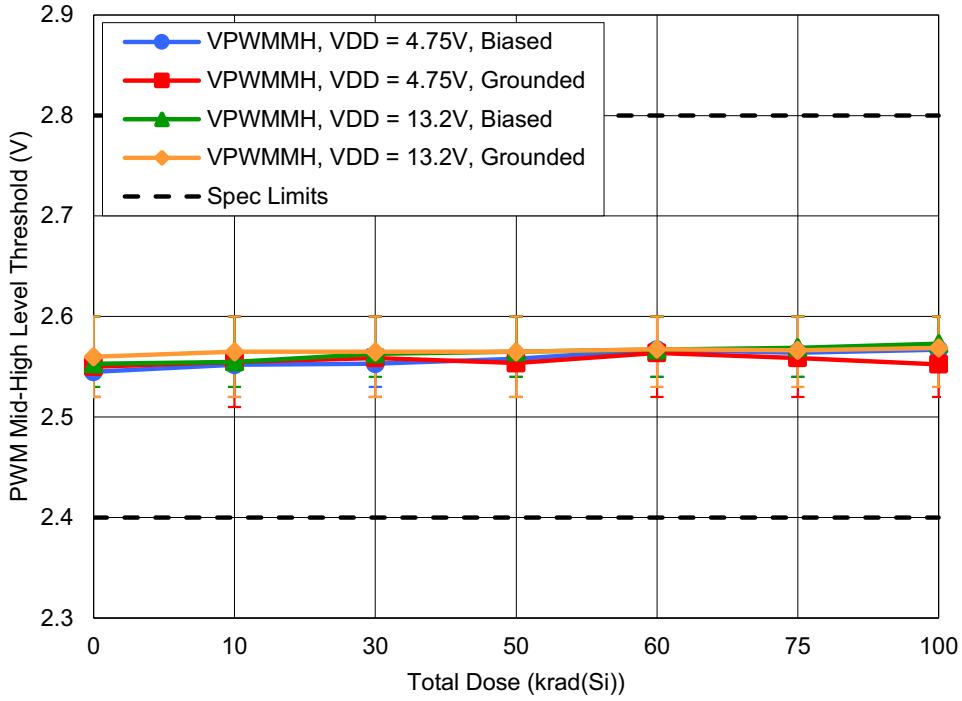


Figure 15. ISL71441SLH PWM high mid-level threshold (V_{PWMMH}) with V_{DD} = 4.75V or 13.2V as a function of LDR irradiation for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 2.4V and a maximum of 2.8V.

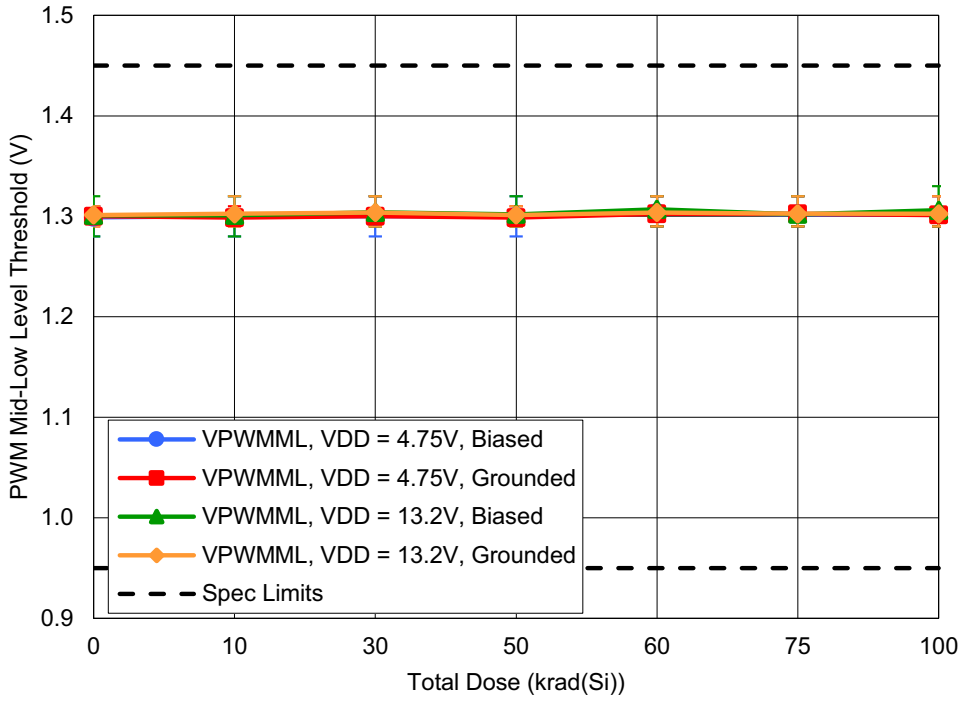


Figure 16. ISL71441SLH low mid-level threshold (V_{PWMML}) with V_{DD} = 4.75V or 13.2V as a function of LDR irradiation for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0.95V and a maximum of 1.45V.

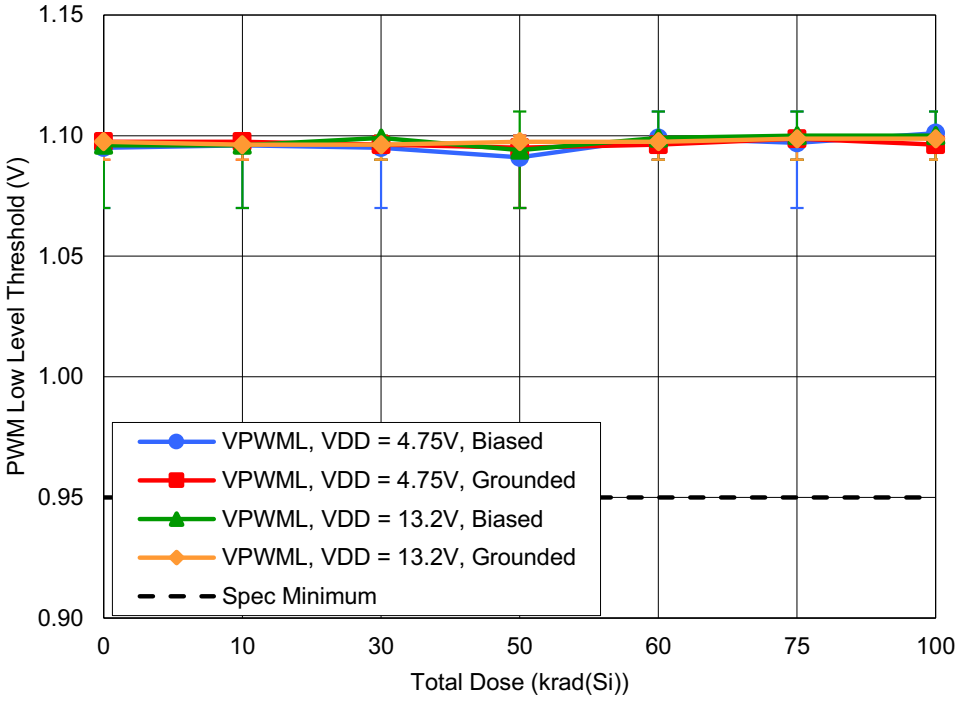


Figure 17. ISL71441SLH PWM low level threshold (V_{PWML}) with V_{DD} = 4.75V or 13.2V as a function of LDR irradiation for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a minimum of 0.95V.

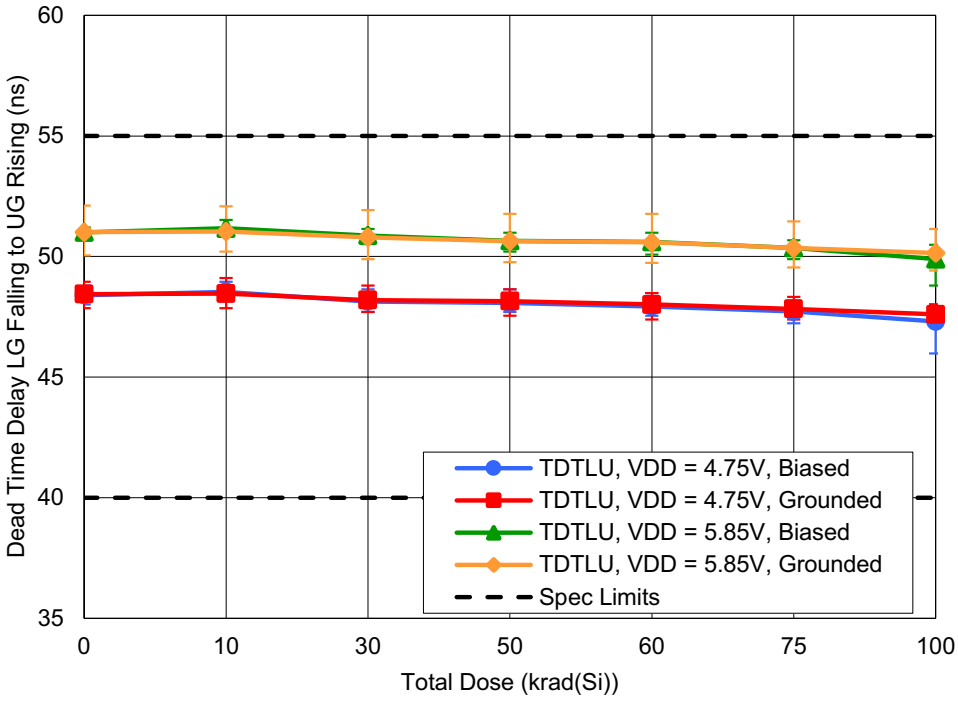


Figure 18. ISL71441SLH dead time delay, LG falling to UG rising (t_{DTLU}) with V_{DD} = 4.75V or 5.85V, and with RDU = RDL = 10kΩ to GND as a function of LDR irradiation for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 40ns and a maximum of 55ns.

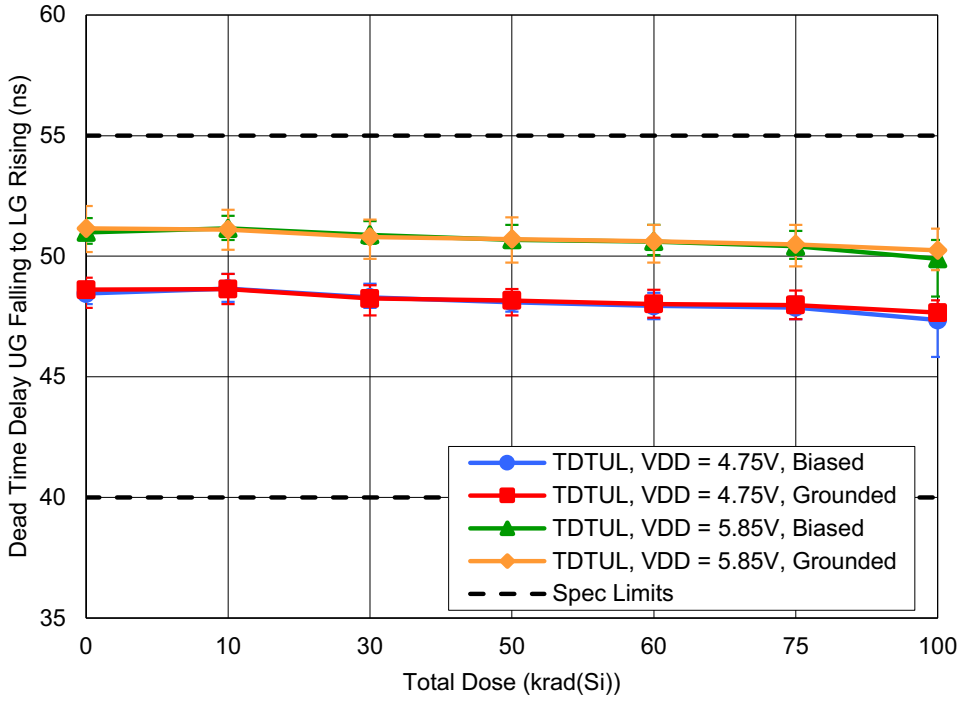


Figure 19. ISL71441SLH dead time delay, UG falling to LG rising (t_{DTUL}) with V_{DD} = 4.75V or 5.85V, and with RDU = RDL = 10kΩ to GND as a function of LDR irradiation for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 40ns and a maximum of 55ns.

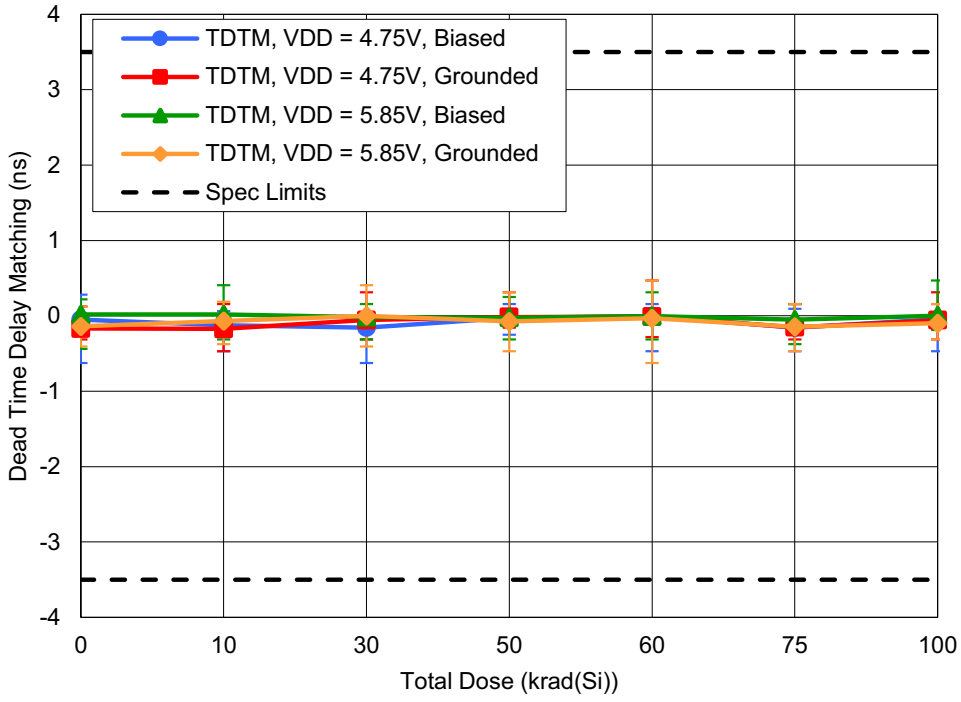


Figure 20. ISL71441SLH dead time delay matching (t_{DTM}) with V_{DD} = 4.75V or 5.85V, and RDU = RDL = 10kΩ to GND as a function of LDR irradiation for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -3.5ns and a maximum of 3.5ns.

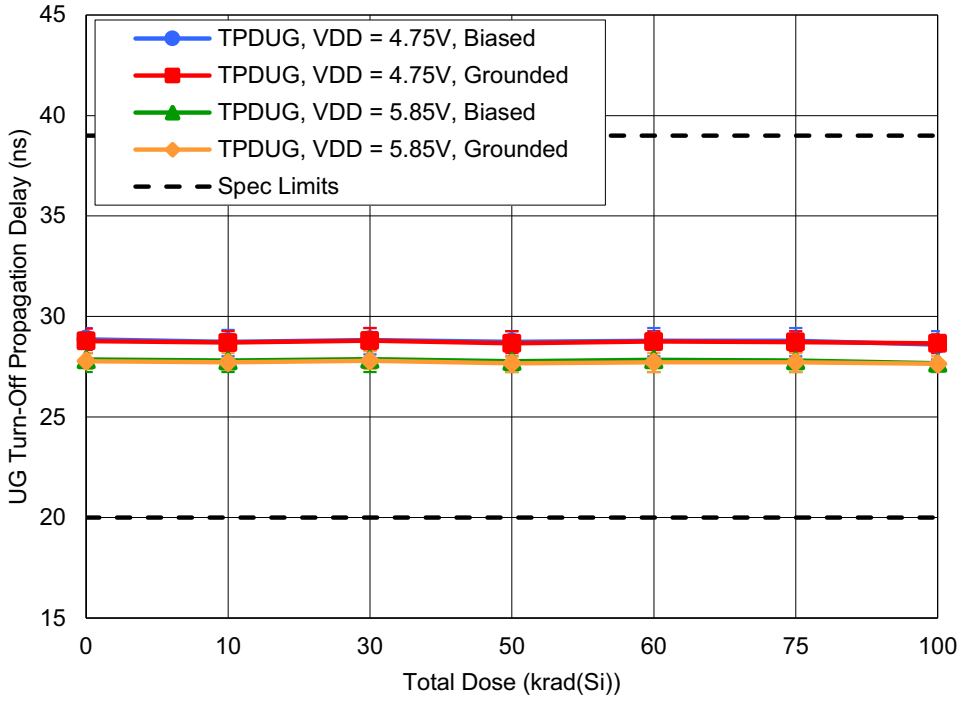


Figure 21. ISL71441SLH UG turn-off propagation delay, PWM falling to UG falling, (t_{PDUG}) with V_{DD} = 4.75V or 5.85V, and with PVCC = BOOT-PHS = 4.5V as a function of LDR irradiation for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 20ns and a maximum of 39ns.

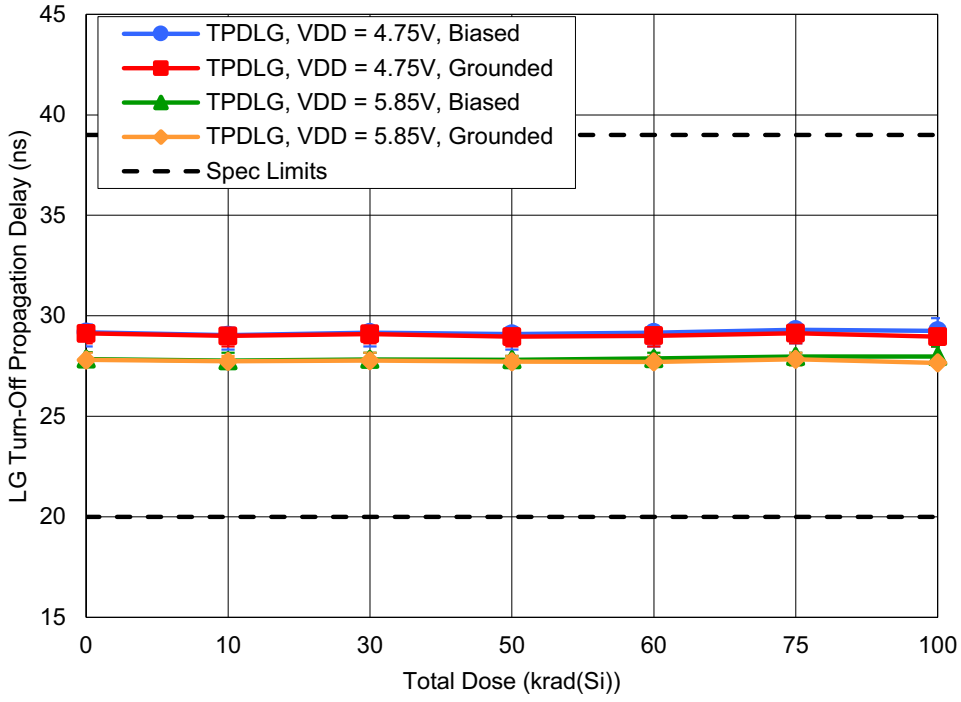


Figure 22. ISL71441SLH LG turn-off propagation delay, PWM rising to LG falling, (t_{PDLG}) with V_{DD} = 4.75V or 5.85V, and with PVCC = BOOT-PHS = 4.5V as a function of LDR irradiation for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 20ns and a maximum of 39ns.

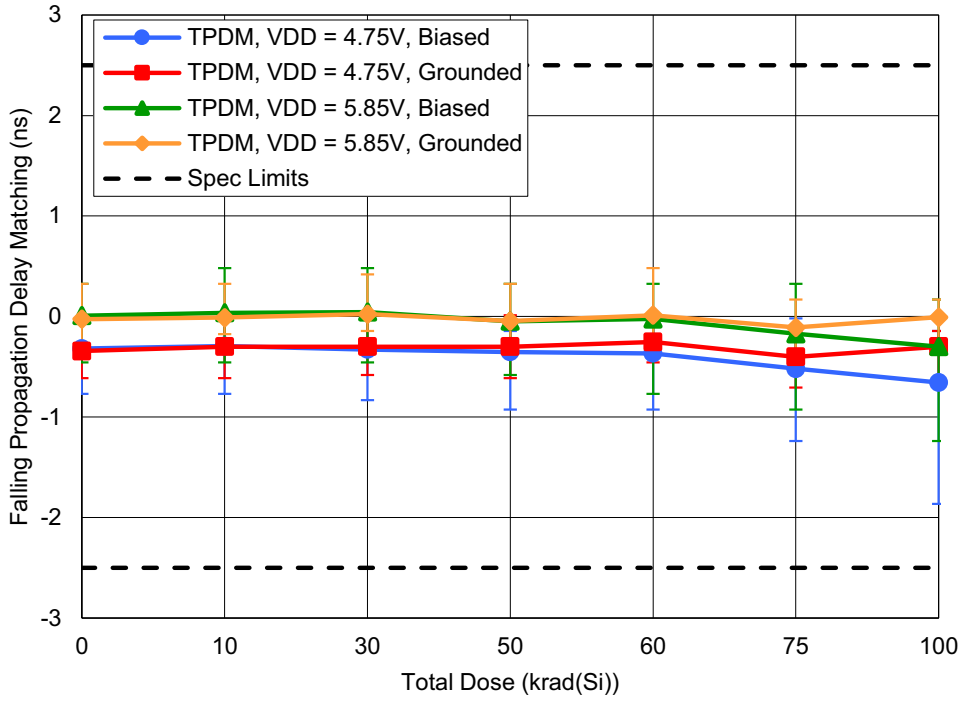


Figure 23. ISL71441SLH propagation delay matching (t_{PDM}) with V_{DD} = 4.75V or 5.85V, and with PVCC = BOOT-PHS = 4.5V as a function of LDR irradiation for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -2.5ns and a maximum of 2.5ns.

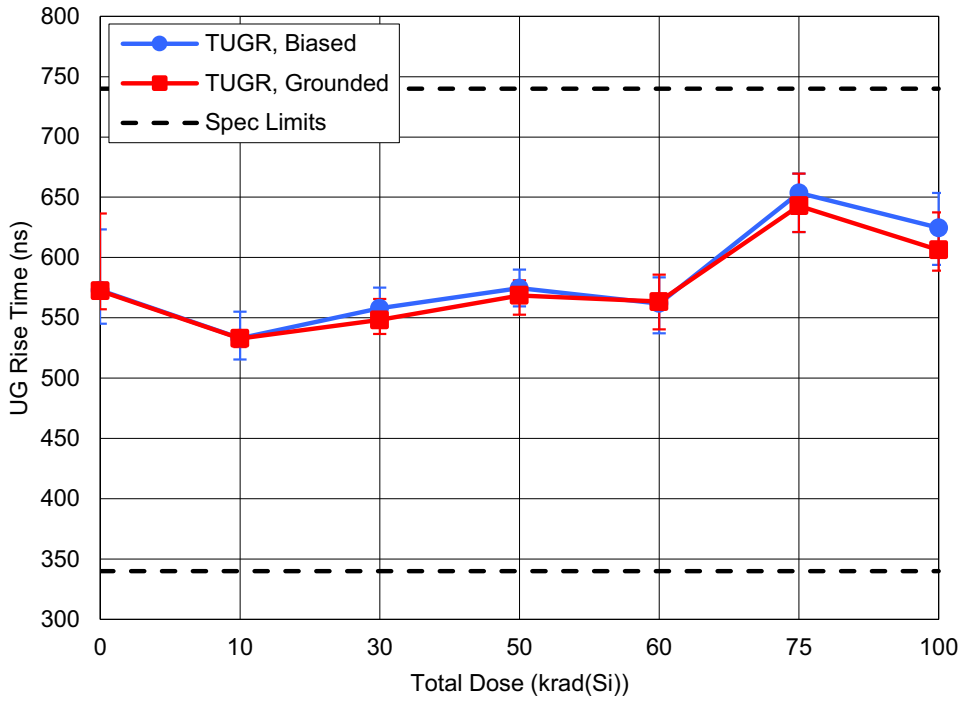


Figure 24. ISL71441SLH UG 30% to 70% rise time (t_{UGR}) with V_{DD} = 4.75V, PVCC = BOOT-PHS = 4.5V and with UG C_{LOAD} = 470nF as a function of LDR irradiation for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 340ns and a maximum of 740ns.

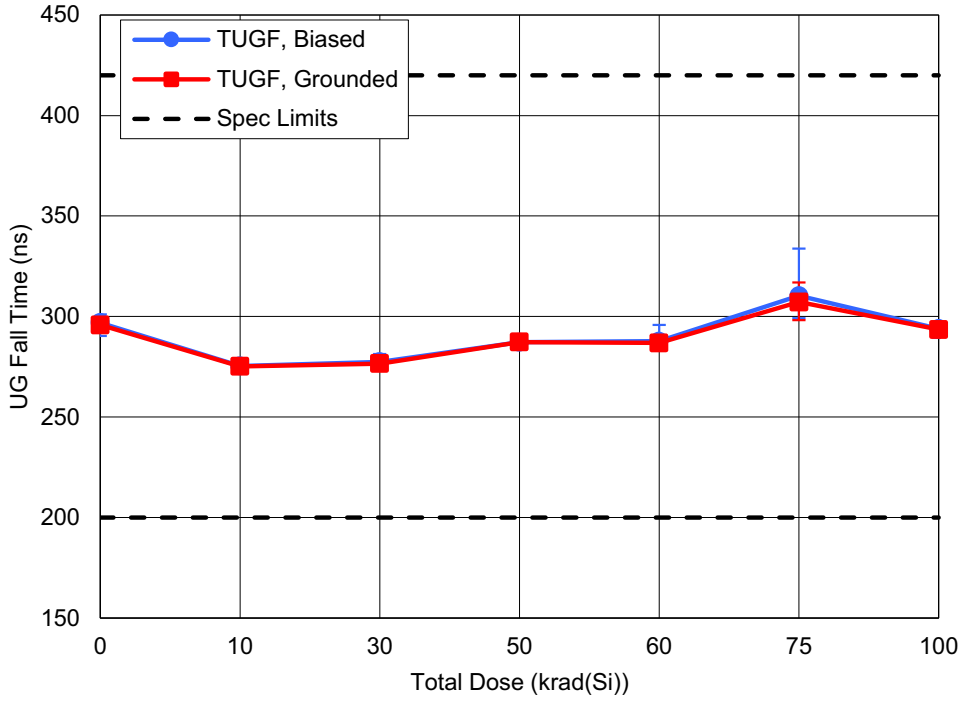


Figure 25. ISL71441SLH UG 70% to 30% fall time (t_{UGF}) with V_{DD} = 4.75V, PVCC = BOOT-PHS = 4.5V and with UG C_{LOAD} = 470nF as a function of LDR irradiation for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 200ns and a maximum of 420ns.

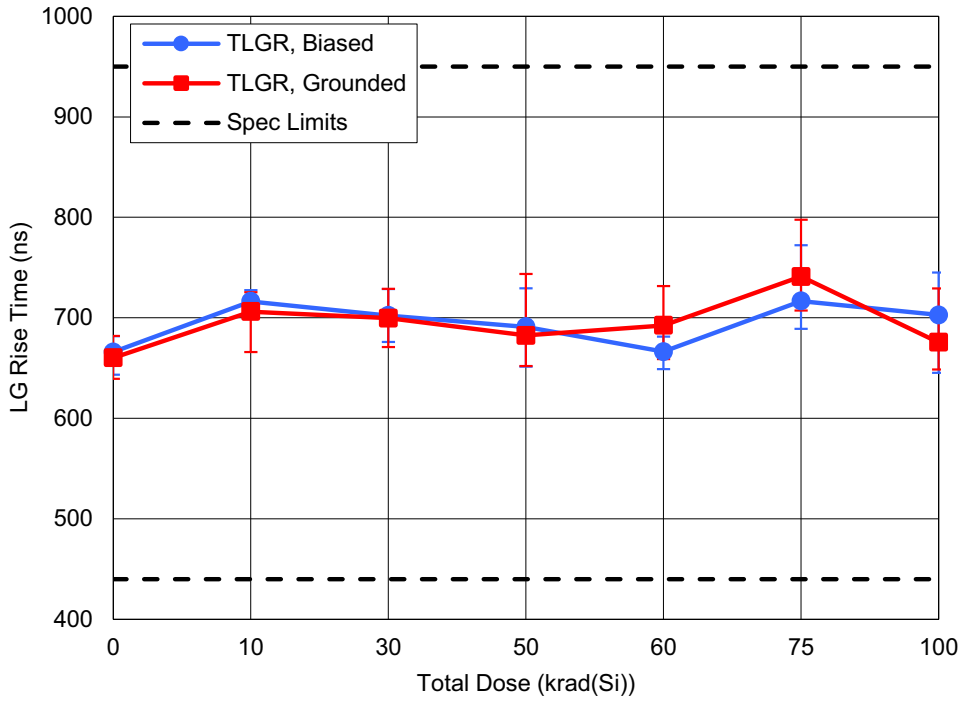


Figure 26. ISL71441SLH LG 30% to 70% rise time (t_{LGR}) with V_{DD} = 4.75V, PVCC = BOOT-PHS = 4.5V and with LG C_{LOAD} = 940ns as a function of LDR irradiation for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 440ns and a maximum of 950ns.

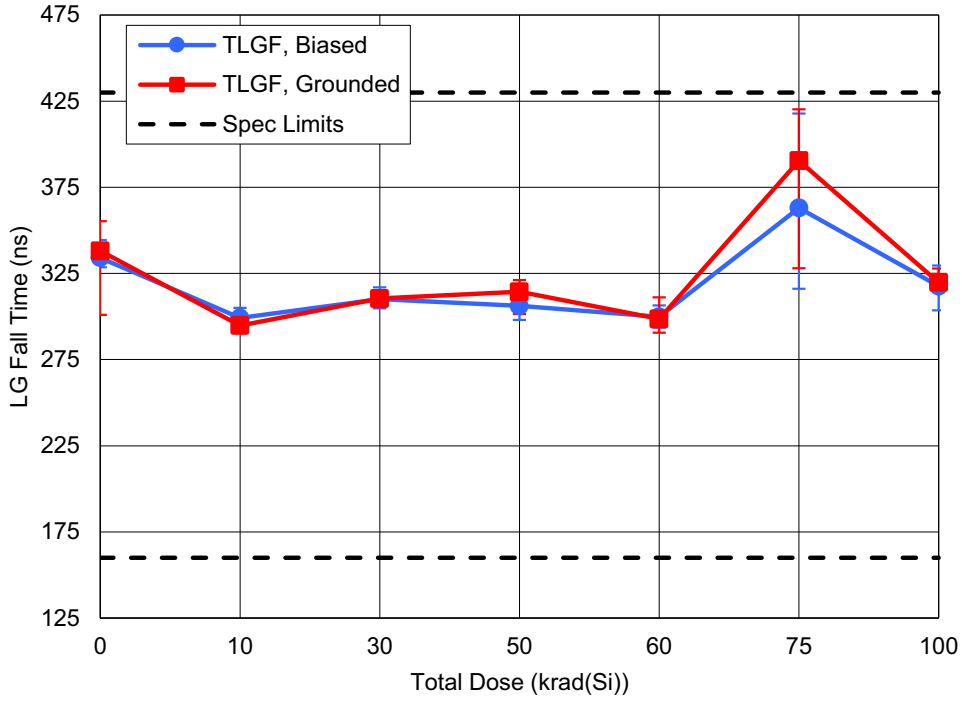


Figure 27. ISL71441SLH LG 70% to 30% fall time (t_{LGF}) with V_{DD} = 4.75V, PVCC = BOOT-PHS = 4.5V and with LG C_{LOAD} = 940nF as a function of LDR irradiation for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 160ns and a maximum of 430ns.

3. Discussion and Conclusion

This document reports the results of the TID test of the ISL71441SLH radiation hardened 12V Half Bridge GaN FET Driver. Biased and grounded samples were irradiated to 100krad(Si) at LDR of 0.01rad(Si)/s. All datasheet parameters passed at all downpoints. No evidence of bias dependence was observed.

4. Revision History

Revision	Date	Description
1.00	Sep 11, 2024	Initial release.

A. Appendix

A.1 Reported Parameters

Table 3 lists the datasheet parameters that are considered indicative of part performance. These parameters are plotted in Figure 3 through Figure 27. All limits are taken from the ISL71441SLH datasheet, which may have more details on test conditions.

Table 3. ISL71441SLH Datasheet Total Dose Parameters (TA = 25ºC)

Fig.	Parameter	Symbol	Test Conditions	Lower Limit	Upper Limit	Unit
3	Quiescent Supply Current	I_{DDQ}	V_{DD} = 13.2V; EN = V_{DD}; PWM = Float; RDU = RDL = 1kΩ to GND	-	13	mA
4			V_{DD} = 13.2V; EN = V_{DD}; PWM = Float; RDU = RDL = 10kΩ to GND		6	
5	Boot Quiescent Current	I_{Q_BOOT}	V_{DD} = 13.2V; EN = VDD; PWM = Float; BOOT-PHS = 4.5V	-	650	µA
6	PVCC Feedback Voltage	V_{FB}	V_{DD} = 13.2V	1.188	1.212	V
7	PVCC Gate Drive Voltage	PVCC	V_{DD} = 4.85V or 13.2V; FB = PVCC; I_{OUT} = 150mA	4.39	4.6	V
8			V_{DD} = 4.85V or 13.2V; FB = 0.266 × PVCC; I_{OUT} = 150mA			
9			V_{DD} = 5.85V to 13.2V; FB = 0.218 × PVCC; I_{OUT} = 150mA	5.39	5.6	
10	Internal LDO Voltage	AVCC	V_{DD} = 5.25V or 13.2V; I_{OUT} = 20mA	4.7	5.4	V
11	PVCC UVLO Rising Threshold	VR_{PVCC}	V_{DD} = 13.2V; PVCC = 5.5V with external FB resistors	5.21	5.45	V
12	PVCC UVLO Falling Threshold	VF_{PVCC}	V_{DD} = 13.2V; PVCC = 5.5V with external FB resistors	5.07	5.27	V
13	PVCC UVLO Hysteresis	VH_{PVCC}	V_{DD} = 13.2V; VR_{PVCC} - VF_{PVCC}	100	300	mV
14	PWM High Level Threshold	V_{PWMH}	V_{DD} = 4.75V or 13.2V	-	2.8	V
15	PWM High Mid-Level Threshold	V_{PWMMH}	V_{DD} = 4.75V or 13.2V	2.4	2.8	V
16	PWM Low Mid-Level Threshold	V_{PWMML}	V_{DD} = 4.75V or 13.2V	0.95	1.45	V
17	PWM Low Level Threshold	V_{PWML}	V_{DD} = 4.75V or 13.2V	0.95	-	V
18	Dead Time Delay LG falling to UG rising	t_{DTLU}	V_{DD} = 4.75V or 5.85V; PVCC = BOOT-PHS = 4.5V to 5.5V; RDU = RDL = 10kΩ to GND	40	55	ns
19	Dead Time Delay UG falling to LG rising	t_{DTUL}	V_{DD} = 4.75V or 5.85V; PVCC = BOOT - PHS = 4.5V to 5.5V; RDU = RDL = 10kΩ to GND	40	55	ns
20	Dead Time Delay Matching T_{DTLU} - T_{DTUL}	t_{DTM}	V_{DD} = 4.75V or 5.85V; PVCC = BOOT - PHS = 4.5V to 5.5V; RDU = RDL = 10kΩ to GND	-3.5	3.5	ns

Table 3. ISL71441SLH Datasheet Total Dose Parameters (TA = 25ºC)

Fig.	Parameter	Symbol	Test Conditions	Lower Limit	Upper Limit	Unit
21	UG Turn - Off Propagation Delay PWM Falling to UG Falling	t_{PDUG}	V_{DD} = 4.75V or 5.85V; PVCC = BOOT - PHS = 4.5V	20	39	ns
22	LG Turn-Off Propagation Delay PWM Rising to LG Falling	t_{PDLG}	V_{DD} = 4.75V or 5.85V; PVCC = BOOT - PHS = 4.5V	20	39	ns
23	Propagation Delay Matching t_{PDUG} - t_{PDLG}	t_{PDM}	V_{DD} = 4.75V or 5.85V; PVCC = BOOT - PHS = 4.5V	-2.5	2.5	ns
24	UG Rise Time	t_{UGR}	V_{DD} = 4.75V; PVCC = BOOT - PHS = 4.5V; UG C_{LOAD} = 470nF; 30% to 70%	340	740	ns
25	UG Fall Time	t_{UGF}	V_{DD} = 4.75V; PVCC = BOOT - PHS = 4.5V; UG C_{LOAD} = 470nF; 70% to 30%	200	420	ns
26	LG Rise Time	t_{LGR}	V_{DD} = 4.75V; PVCC = BOOT - PHS = 4.5V; LG C_{LOAD} = 940nF; 30% to 70%	440	950	ns
27	LG Fall Time	t_{LGF}	V_{DD} = 4.75V; PVCC = BOOT - PHS = 4.5V; LG C_{LOAD} = 940nF; 70% to 30%	160	430	ns

A.2 Related Information

For a full list of related documents, visit our website:

- ISL71441SLH device page
- MIL-STD-883 test method 1019

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