ISL70244SEH, ISL73244SEH

TID Results of the ISL7x244SEH Radiation Hardened 40V Dual Rail-to-Rail Input-Output, Low-Power Op Amp

This document reports the results of low and high dose rate total dose testing of the ISL7x244SEH quad operational amplifier. This report applies to the ISL70244SEH and the ISL73244SEH as both parts are of the same design and silicon, differing only in radiation assurance testing. The tests were conducted to provide an assessment of the total dose hardness of the part and to provide an estimate of dose rate, bias, or anneal sensitivity. Parts were irradiated under bias and with all pins grounded at LDR to 50krad(Si) and HDR to 300krad(Si). Half of the HDR samples were annealed under bias at an ambient temperature of 100°C for 168 hours after 300krad(Si). No significant differences in total dose response were noted between biased and grounded irradiation for any parameters. The data at all downpoints was well within the pre-irradiation datasheet specifications, confirming that the part is not LDR sensitive.

The ISL70244SEH is rated to 300krad(Si) at HDR (50 - 300rad(Si)/s) and to 50krad(Si) at LDR (0.01rad(Si)/s), ensuring hardness to the specified level for both dose rates. The ISL73244SEH is only rated at 50krad(Si) at LDR (0.01rad(Si)/s). Both part types are acceptance tested on a lot-by-lot basis to these limits.

Product Description

The radiation hardened ISL7x244SEH is a 40V Dual Rail-to-Rail Input-Output, Low-Power Operational Amplifier featuring two low-power amplifiers optimized to provide maximum dynamic range. These operational amplifiers (op amps) feature a unique combination of rail-to-rail operation on the input and output and a slew-rate enhanced front end that provides ultra-fast slew rates positively proportional to a given step size. These features increase accuracy under both periodic and transient conditions. The ISL7x244SEH also offers low power, low offset voltage, and low-temperature drift, making it ideal for applications requiring high DC accuracy and AC performance.

The amplifiers operate over a supply range of 2.7V to 40V or a split supply voltage range of ±1.35V to ±20V.

Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency (DLA) in Columbus, OH. The SMD is the controlling document and must be cited when ordering.

The pinout configuration for the part is shown in Figure 1, and the pin description is shown in Table 1.

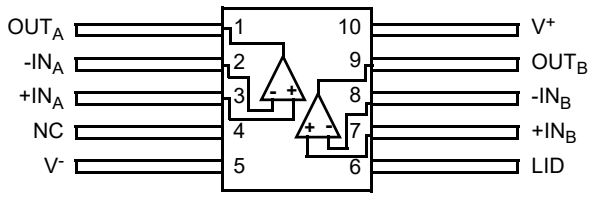

Figure 1. ISL7x244SEH Pin Assignments

Table 1. ISL7x244SEH Pin Descriptions

Pin Number	Pin Name	Description
1	OUT_A	Amplifier A output
2	$-IN_A$	Amplifier A inverting input
3	$+IN_A$	Amplifier A non-inverting input
4	NC	This pin is not electrically connected internally
5	V-	Negative power supply
6	LID	Unbiased, tied to package lid

Table 1. ISL7x244SEH Pin Descriptions (Cont.)

Pin Number	Pin Name	Description
7	$+IN_B$	Amplifier B non-inverting input
8	$-IN_B$	Amplifier B inverting input
9	OUT_B	Amplifier B output
10	V+	Positive power supply

Contents

1. Test Description

1.1 Irradiation Facility

HDR testing was performed using a Gammacell 220 irradiator located in the Palm Bay, Florida, Renesas facility. LDR testing was performed using a Hopewell Designs N40 vault-type LDR irradiator located in the Palm Bay, Florida, Renesas facility. A PbAl box was used to shield the test fixture and devices under test against low energy and secondary gamma radiation. Post-irradiation anneals were performed under bias in a small temperature chamber.

1.2 Test Fixturing

Figure 2 shows the configuration used for biased irradiation. The grounded irradiations were performed in the same fixture type, with all pins hardwired to ground.

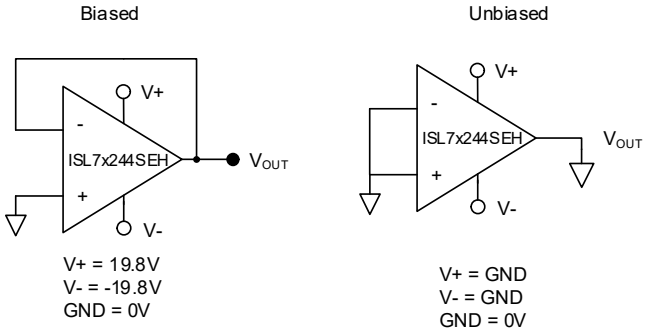

Figure 2. Biased and Grounded Irradiation Bias Configurations for the ISL7x244SEH

1.3 Characterization Equipment and Procedures

All electrical testing was performed at room temperature before and after irradiation using the Renesas production automated test equipment (ATE). Three control units were used to ensure repeatability.

1.4 Experimental Matrix

Irradiation was performed in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 16 samples irradiated at LDR under bias, 16 irradiated at LDR with all pins grounded, 12 irradiated at HDR under bias, and 12 irradiated at HDR with all pins grounded.

Samples of the ISL70244SEH were drawn from lot X2L0T and were packaged in the hermetic 10-lead solder-sealed ceramic flatpack (KCP) package. Samples were processed through the standard burn-in cycle before irradiation, as required by MIL-STD-883, and were screened to the ATE limits at room temperature before the test.

1.5 Downpoints

Downpoints for the LDR tests were zero, 10, 30, and 50krad(Si). Downpoints for the HDR tests were 0, 50, 100, and 300krad(Si). After HDR irradiation to 300krad(Si), half of the HDR samples were annealed under bias for 168 hours at 100°C.

2. Results

Total dose testing of the ISL7x244SEH is complete. All tested parameters passed the SMD limits. Table 2 summarizes the results.

2.1 Attributes Data

Table 2. ISL7x244SEH Total Dose Test Attributes Data

Dose rate (rad(Si)/s)	Condition	Sample Size	Downpoint	Pass[1]	Fail
0.01	Biased (Figure 2)	16	Pre-irradiation	16	0
			10krad(Si)	16	0
			30krad(Si)	16	0
			50krad(Si)	16	0
0.01	Grounded	16	Pre-irradiation	16	-
			10krad(Si)	16	0
			30krad(Si)	16	0
			50krad(Si)	16	0
187.16	Biased (Figure 2)	12	Pre-irradiation	12	-
			50krad(Si)	12	0
			100krad(Si)	12	0
			300krad(Si)	12	0
			Anneal	6	0
187.16	Grounded	12	Pre-irradiation	12	-
			50krad(Si)	12	0
			100krad(Si)	12	0
			300krad(Si)	12	0
			Anneal	6	0

1. A Pass indicates a sample that passes all SMD limits.

2.2 Variables Data

The plots in Figure 3 through Figure 31 show data at all downpoints including the post-anneal data after HDR. The plots show the average tested values of the parameters to total dose irradiation at LDR and HDR for the biased (per Figure 2) and unbiased (all pins grounded) cases. In addition the plots show the response of HDR samples to post-irradiation annealing at 100°C for 168 hours after irradiation to 300krad(Si). The plots also include error bars at each downpoint, representing the samples' minimum and maximum measured values. However, in some plots, the error bars might not be visible due to their values compared to the scale of the graph. All parts passed at all downpoints.

No differences in total dose response were noted between biased and grounded irradiation for any parameters. Additionally, no channel-to-channel differences were noted, either in the pre-irradiation data or in the total dose response of the parts.

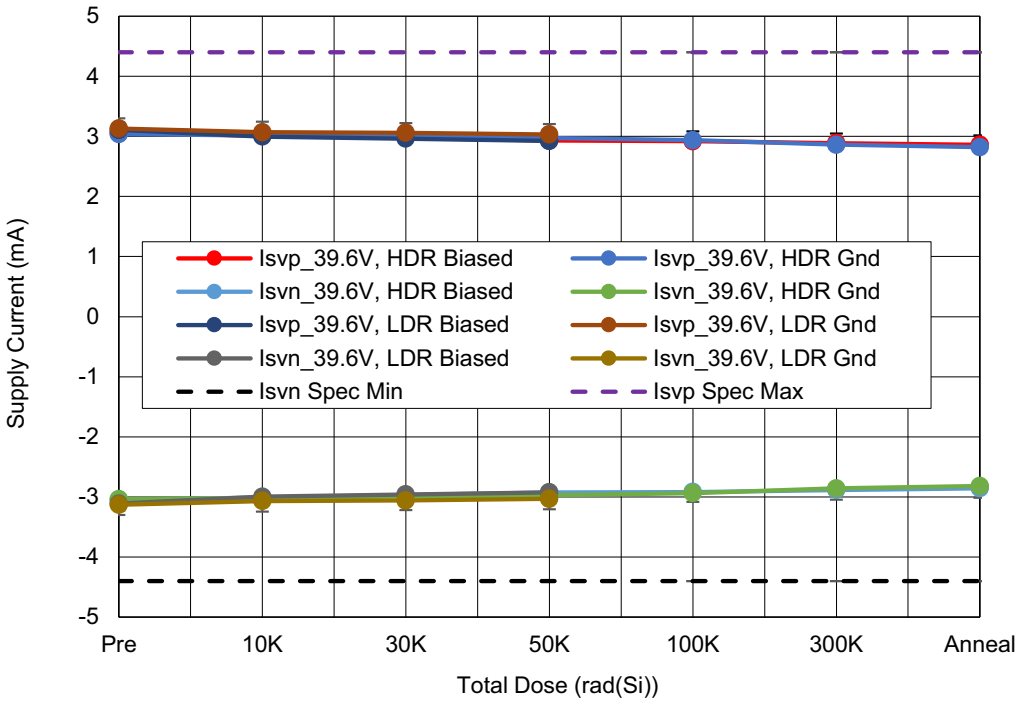

Figure 3. ISL7x244SEH average positive (I_{SVP}) and negative (I_{SVN}) supply current (sum of both channels) at V_S = ±19.8V as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -4.4mA minimum and 4.4mA maximum.

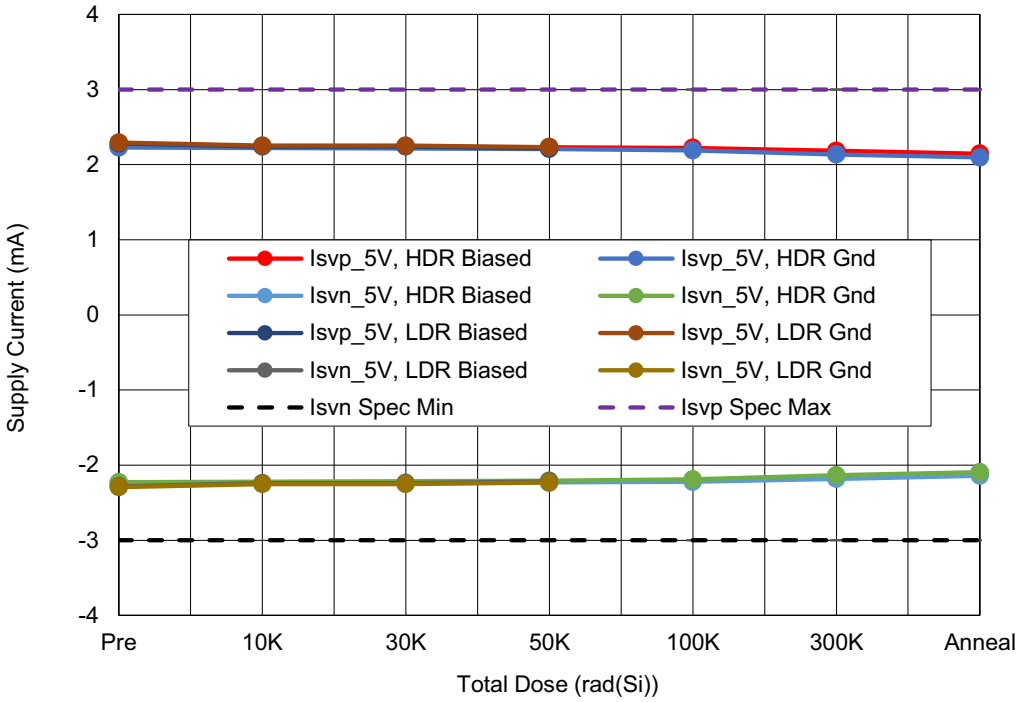

Figure 4. ISL7x244SEH average positive (I_{SVP}) and negative (I_{SVN}) supply current (sum of both channels) at V_S = ±2.5V as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -3mA minimum and 3mA maximum.

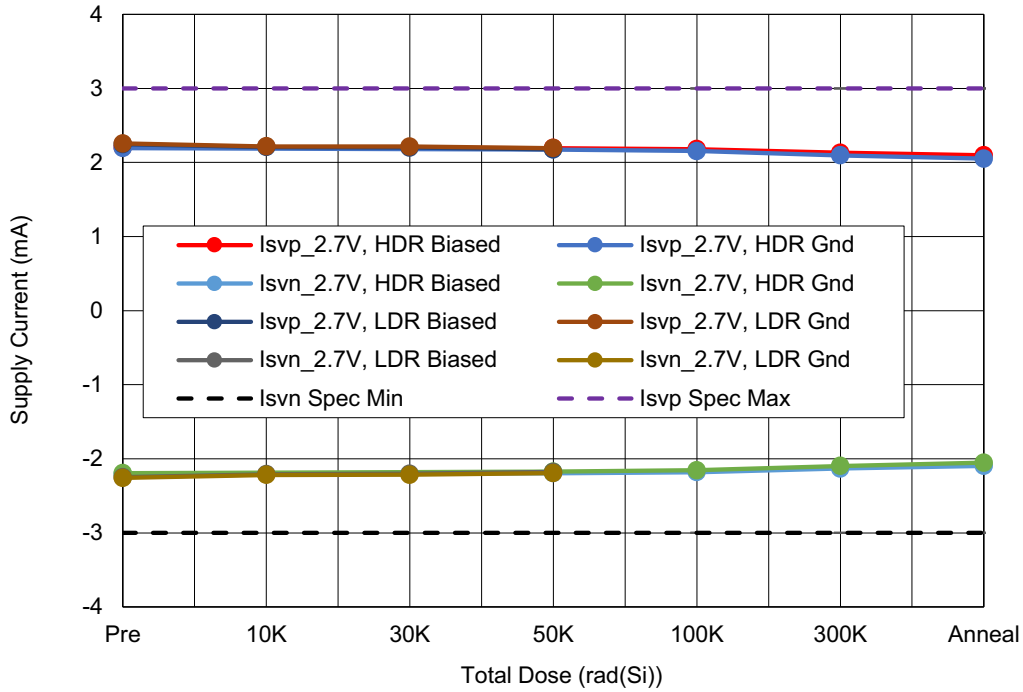

Figure 5. ISL7x244SEH average positive (I_{SVP}) and negative (I_{SVN}) supply current (sum of both channels) at V_S = ±1.35V as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -3mA minimum and 3mA maximum.

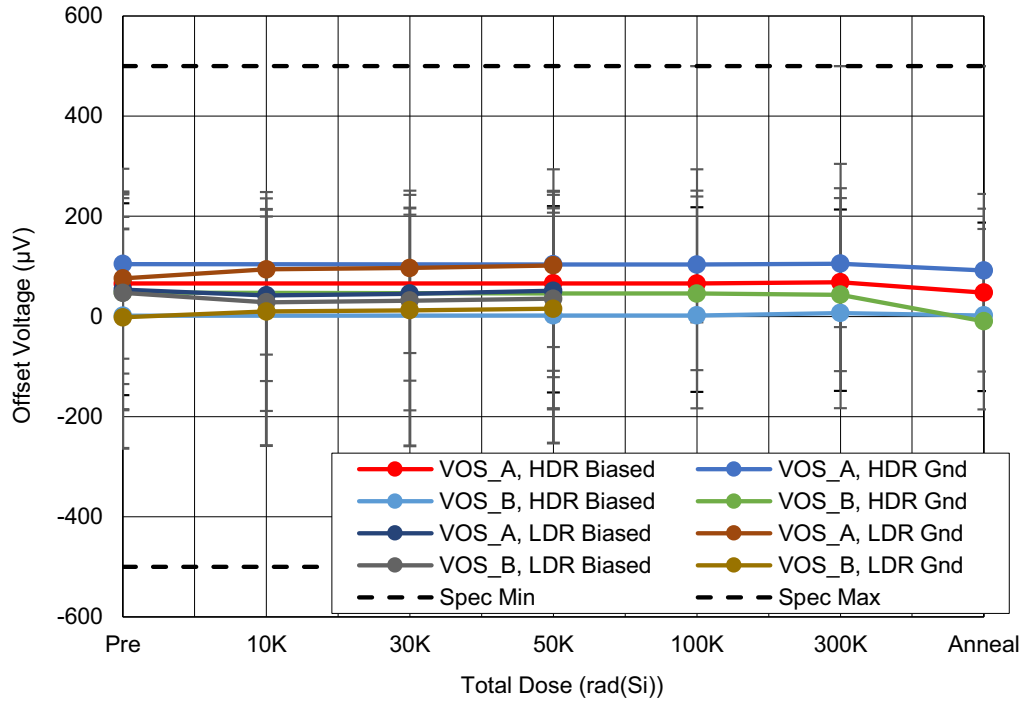

Figure 6. ISL7x244SEH average input offset voltage (V_{OS}) at V_S = ±19.8V and V_{CM} = 0V, +19.8V and -19.8V as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars represent the minimum and maximum measured values. The SMD limits are -500µV minimum and 500µV maximum.

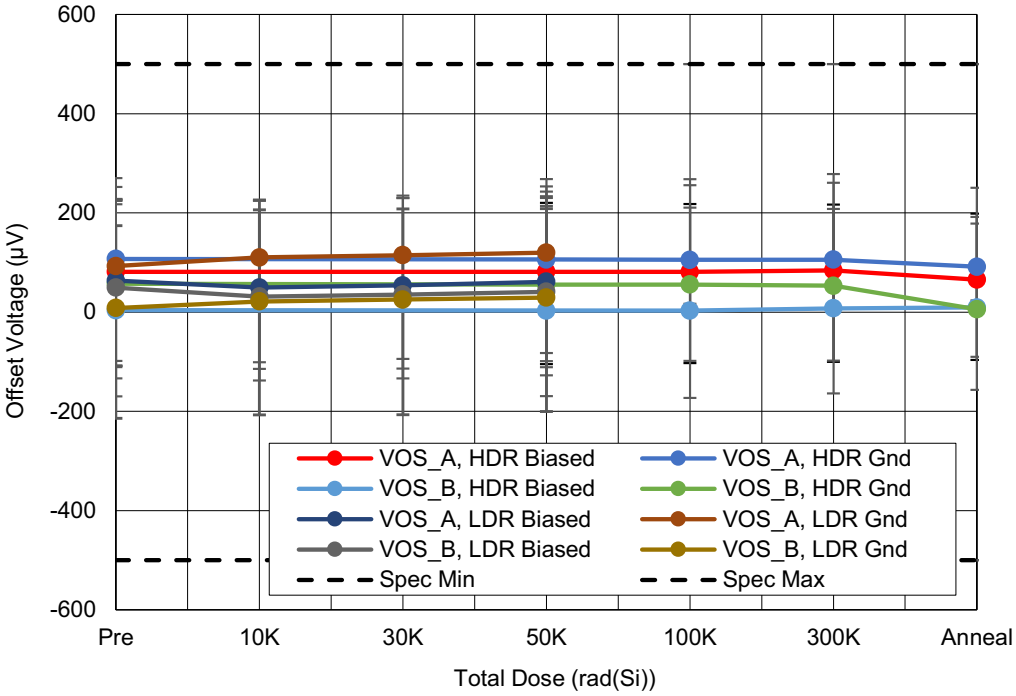

Figure 7. ISL7x244SEH average input offset voltage (V_{OS}) at V_S = ±2.5V and V_{CM} = 0V as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars represent the minimum and maximum measured values. The SMD limits are -500µV minimum and 500µV maximum.

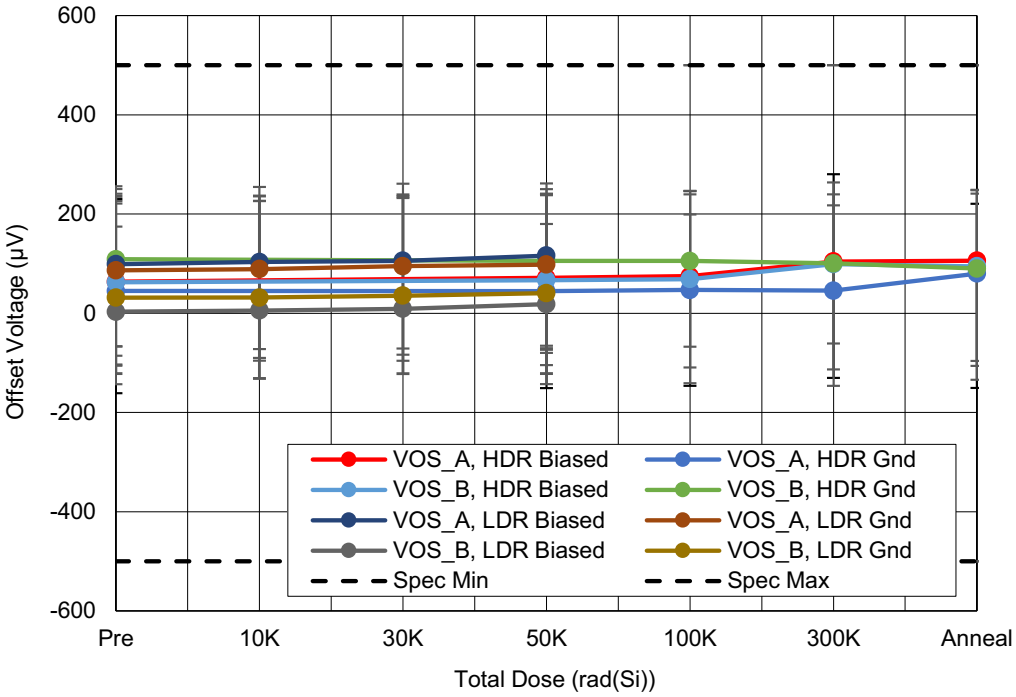

Figure 8. ISL7x244SEH average input offset voltage (V_{OS}) at V_S = ±1.35V and V_{CM} = 0V as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars represent the minimum and maximum measured values. The SMD limits are -500µV minimum and 500µV maximum.

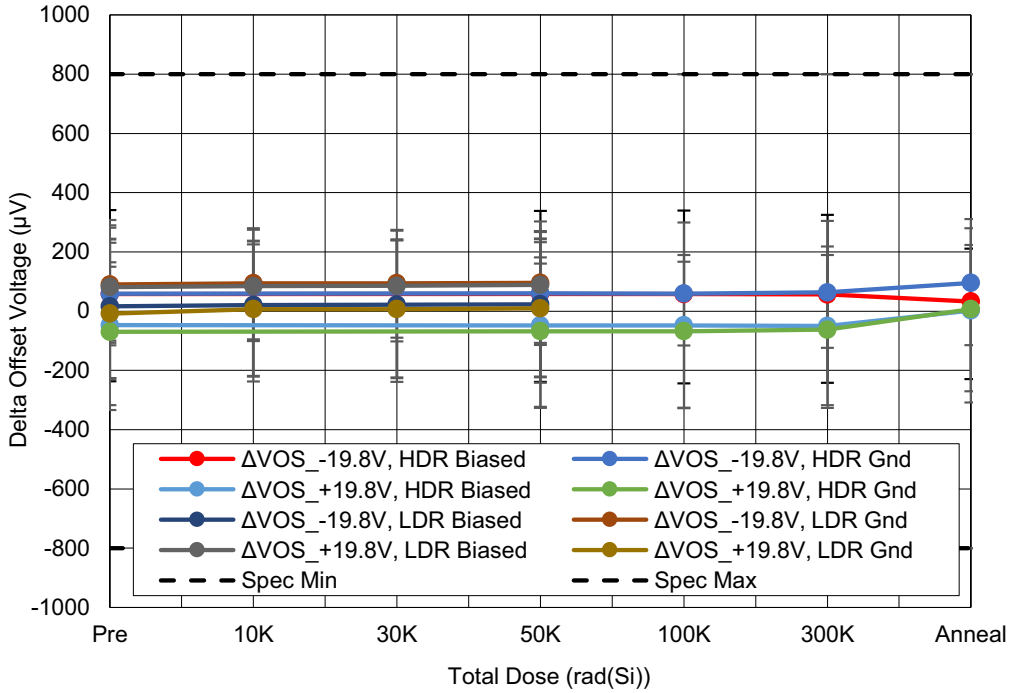

Figure 9. ISL7x244SEH average input offset channel to channel match (ΔV_{OS}) at V_S = ±19.8V and V_{CM} = ±19.8V as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars represent the minimum and maximum measured values. The SMD limits are -800µV minimum and 800µV maximum.

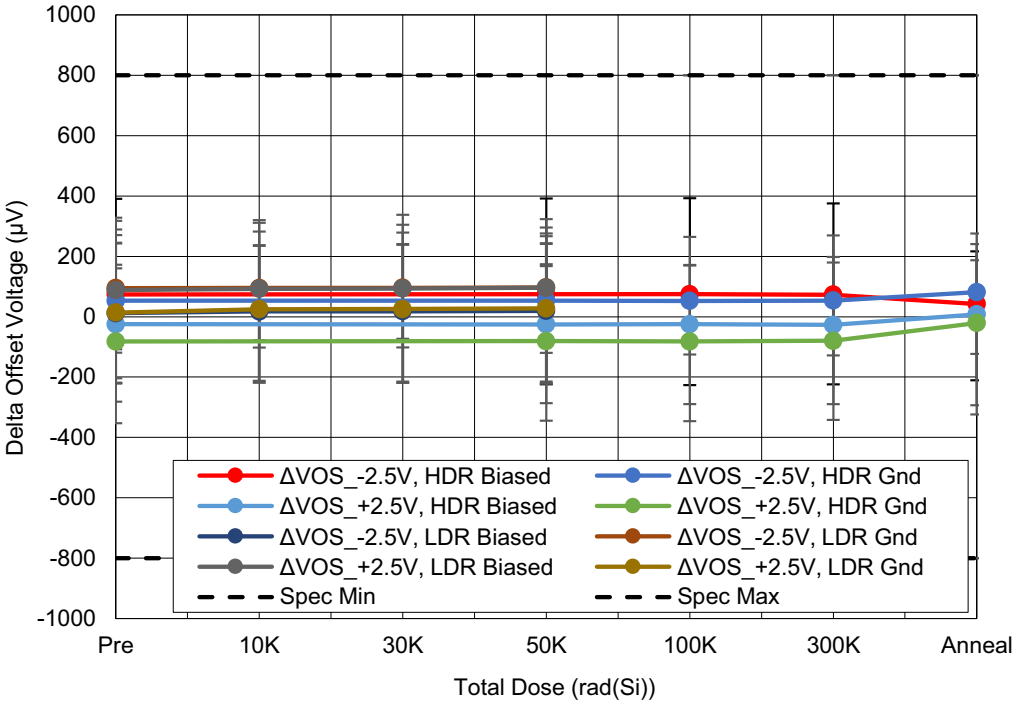

Figure 10. ISL7x244SEH average input offset channel to channel match (ΔV_{OS}) at V_S = ±2.5V and V_{CM} = ±2.5V as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars represent the minimum and maximum measured values. The SMD limits are -800µV minimum and 800µV maximum.

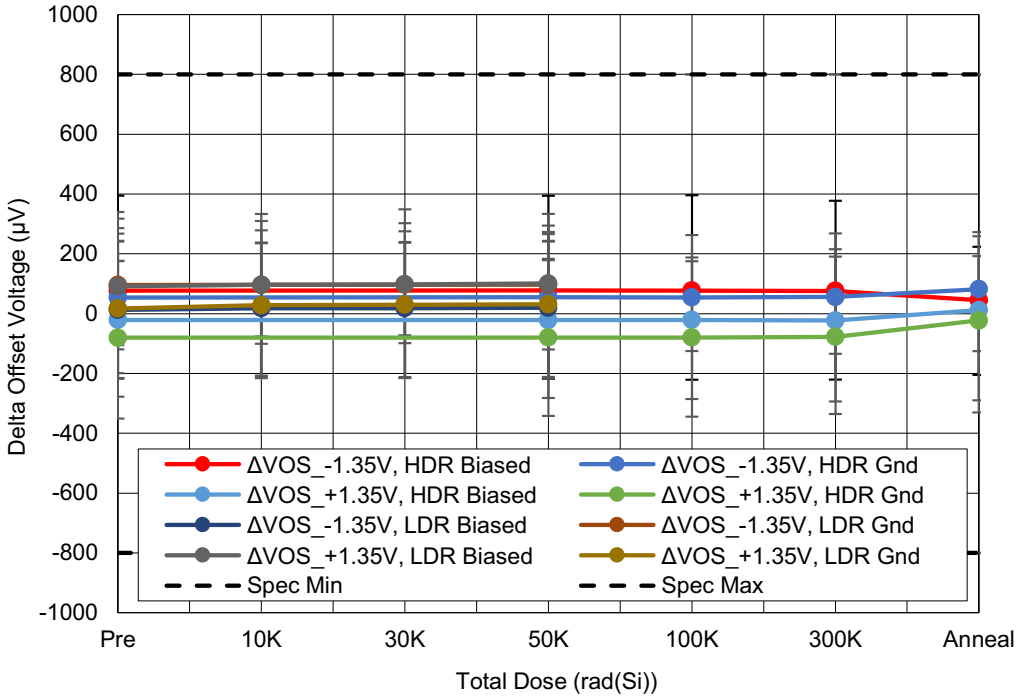

Figure 11. ISL7x244SEH average input offset channel to channel match (ΔV_{OS}) at V_S = ±1.35V and V_{CM} = ±1.35V as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars represent the minimum and maximum measured values. The SMD limits are -800µV minimum and 800µV maximum.

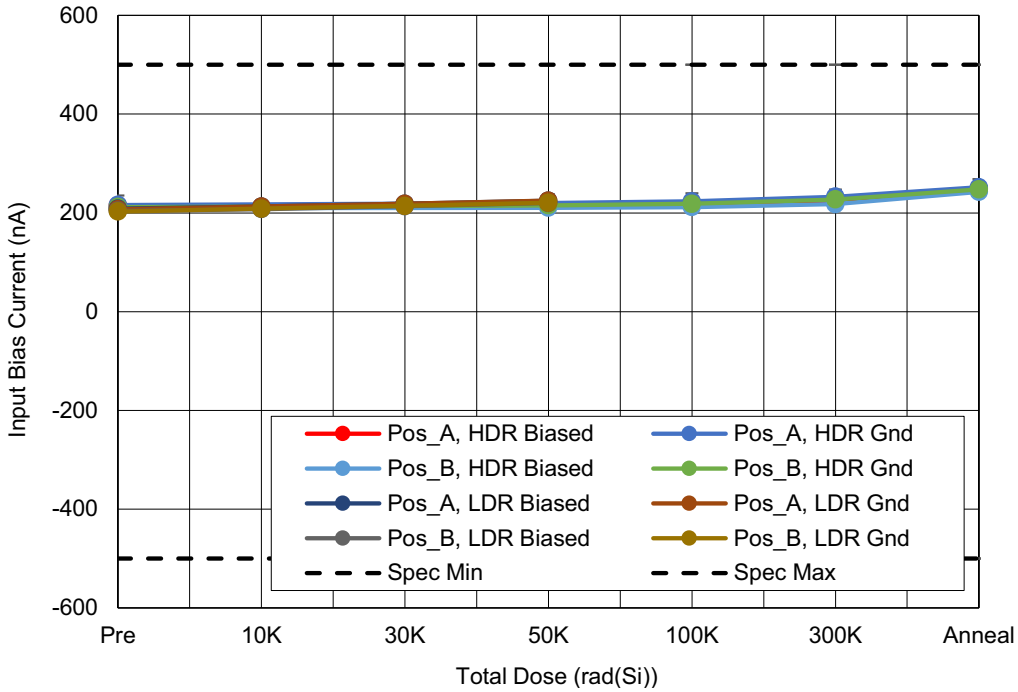

Figure 12. ISL7x244SEH average input bias current (I_B) at V_S = ±19.8V and V_{CM} = 0V as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -500nA minimum and 500nA maximum.

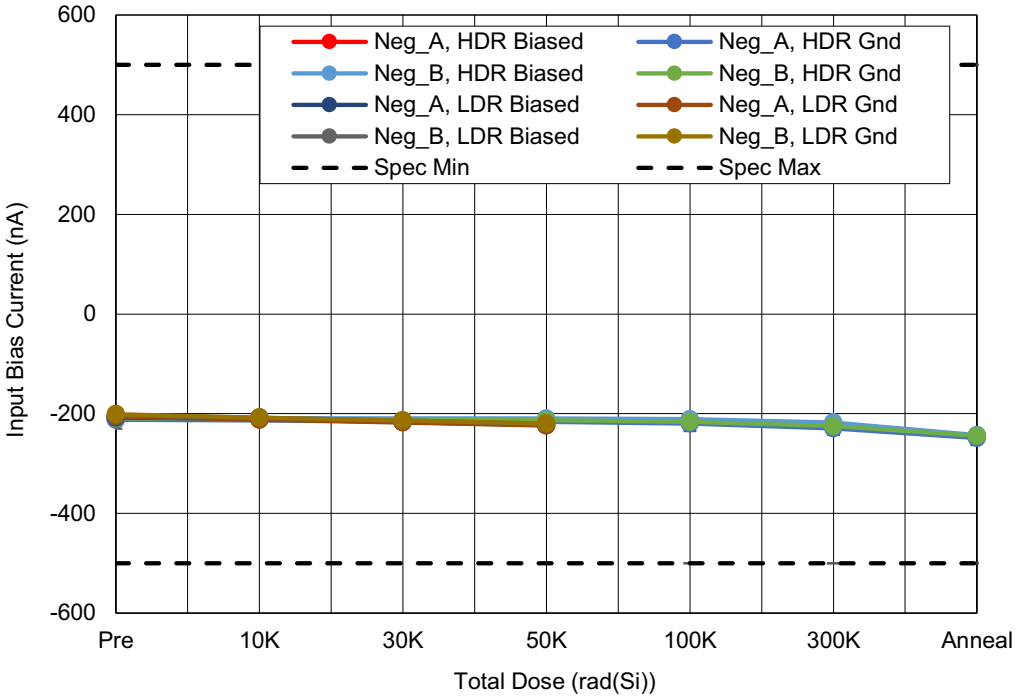

Figure 13. ISL7x244SEH average input bias current (I_B) at V_S = ±19.8V and V_{CM} = 0V as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -500nA minimum and 500nA maximum.

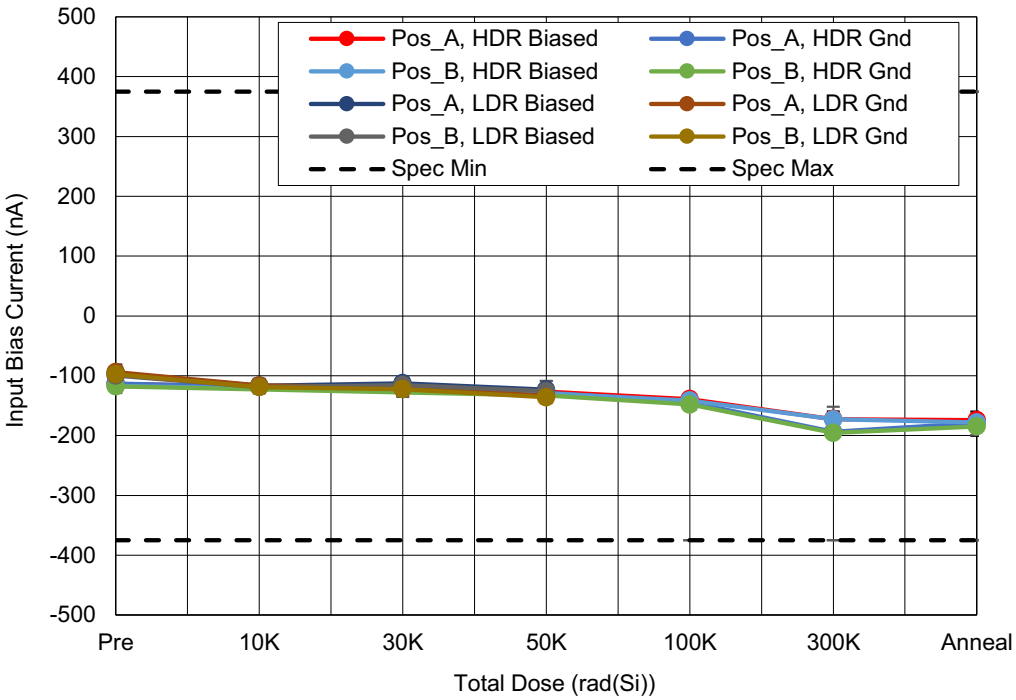

Figure 14. ISL7x244SEH average input bias current (I_B) at V_S = ±1.35V and V_{CM} = 0V as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -375nA minimum and 375nA maximum.

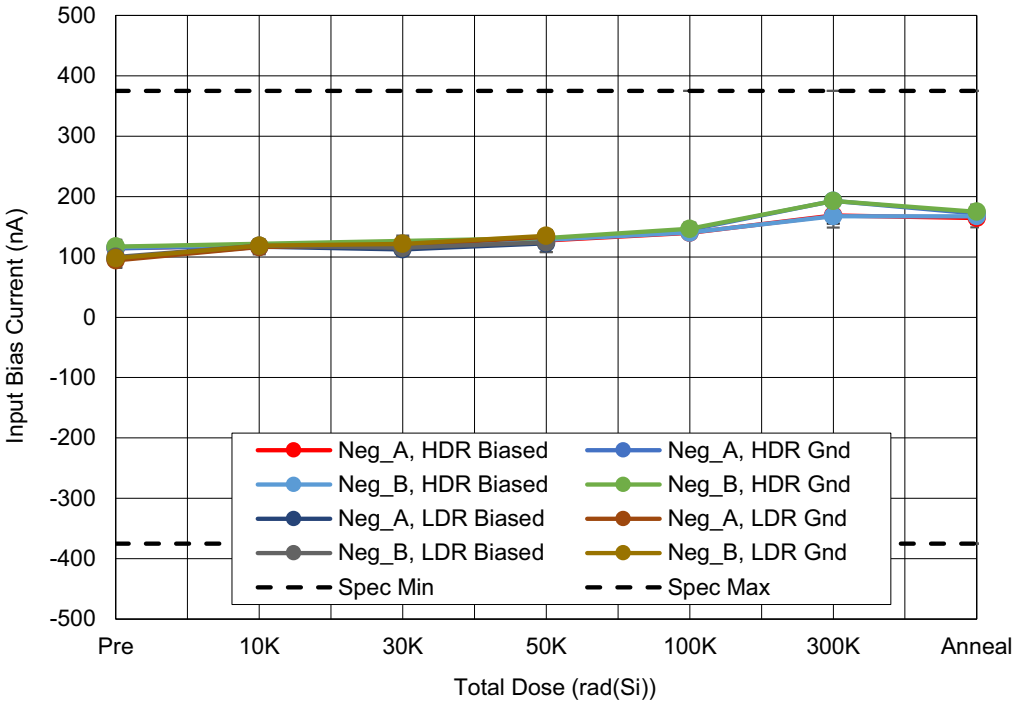

Figure 15. ISL7x244SEH average input bias current (I_B) at V_S = ±1.35V and V_{CM} = 0V as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -375nA minimum and 375nA maximum.

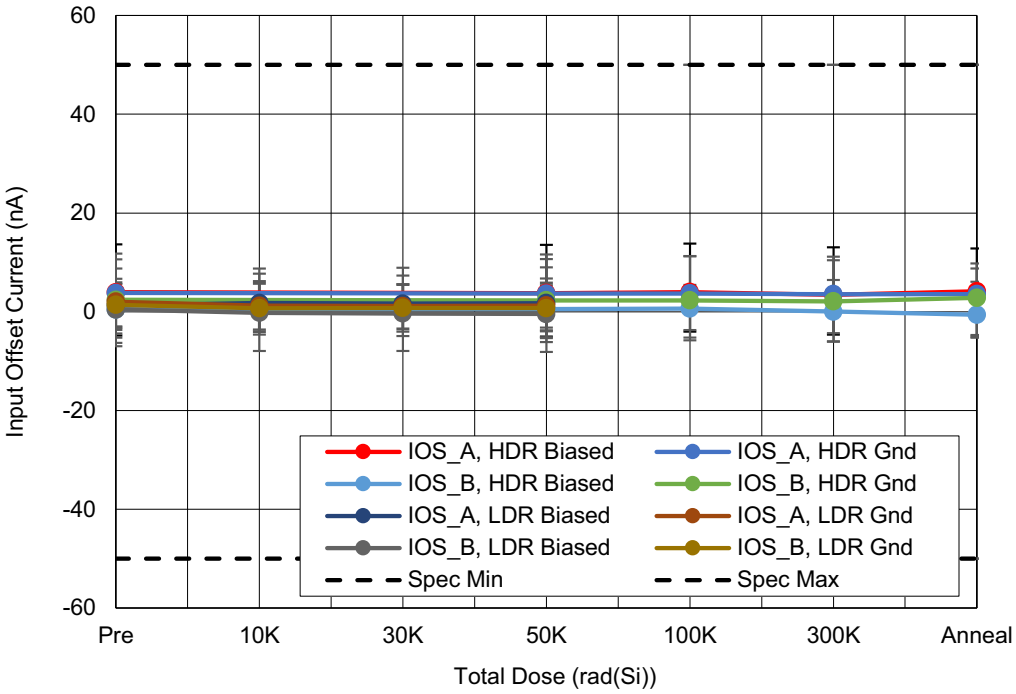

Figure 16. ISL7x244SEH average input offset current (I_{OS}) at V_S = ±19.8V and V_{CM} = 0V as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars represent the minimum and maximum measured values. The SMD limits are -50nA minimum and 50nA maximum.

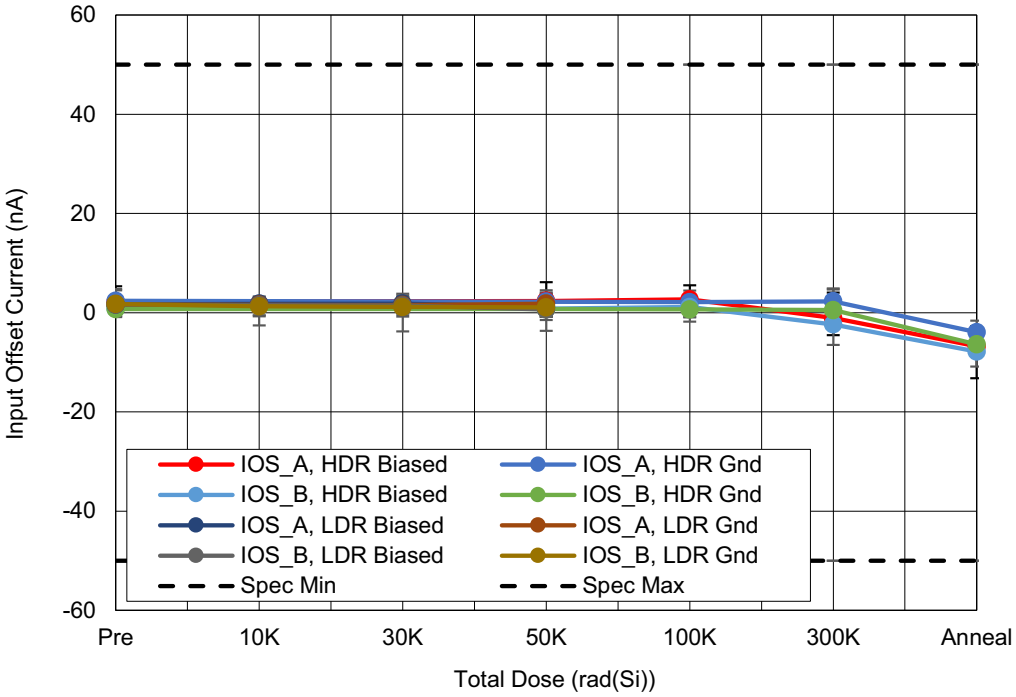

Figure 17. ISL7x244SEH average input offset current (I_{OS}) at V_S = ±1.35V and V_{CM} = 0V as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars represent the minimum and maximum measured values. The SMD limits are -50nA minimum and 50nA maximum.

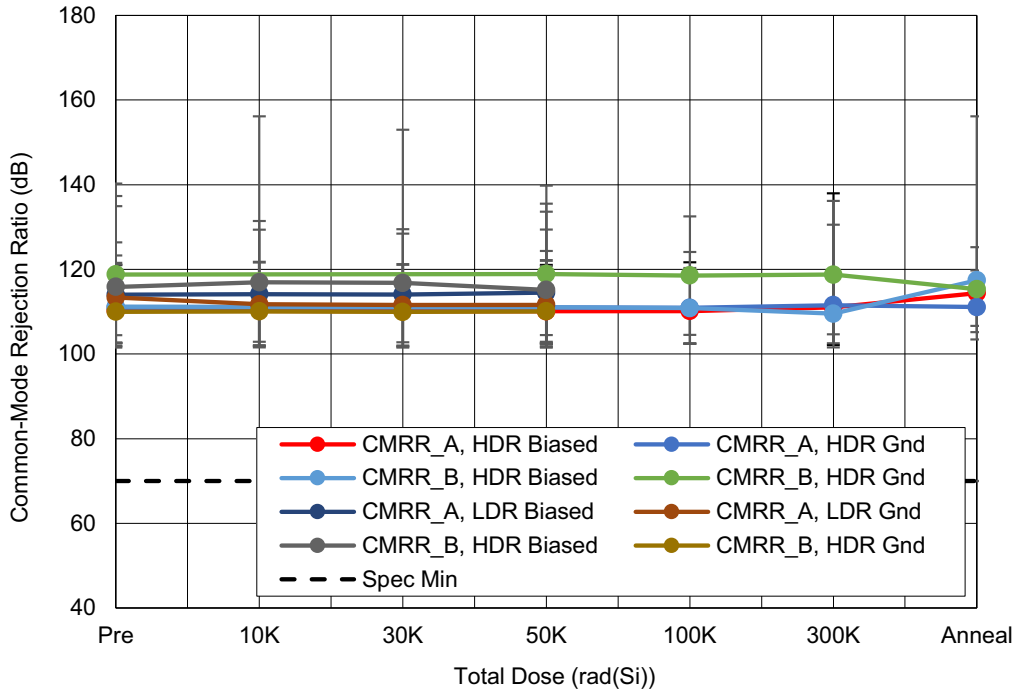

Figure 18. ISL7x244SEH average common-mode rejection ratio (CMRR) at V_S = ±19.8V and V_{CM} = -V_S to +V_S as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars represent the minimum and maximum measured values. The SMD limit is 70dB minimum.

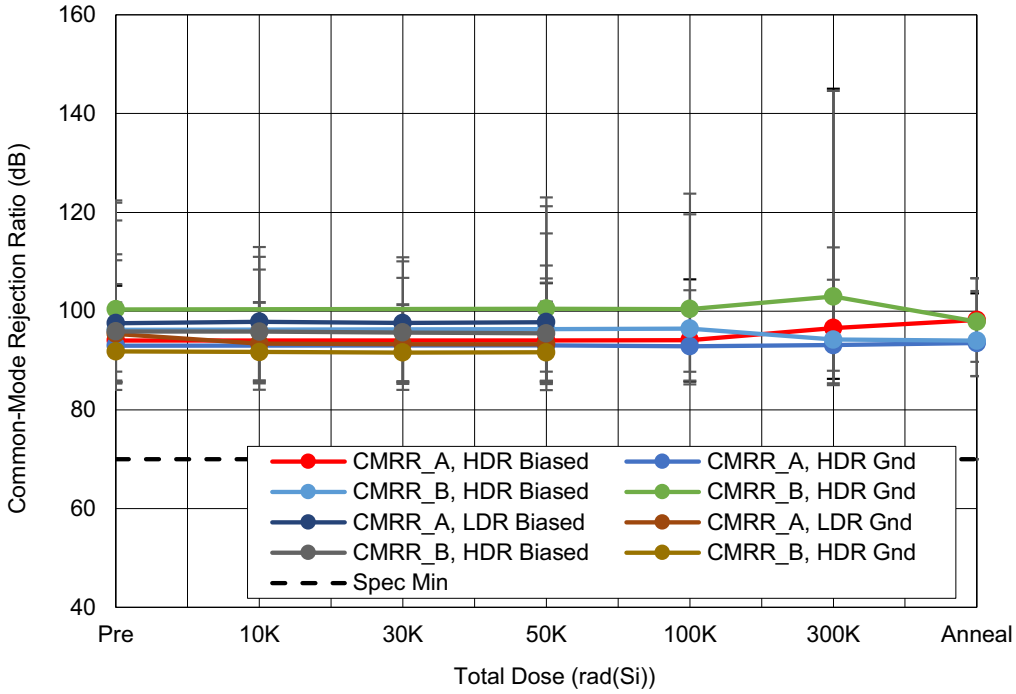

Figure 19. ISL7x244SEH average common-mode rejection ratio (CMRR) at V_S = ±2.5V and V_{CM} = -V_S to +V_S as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars represent the minimum and maximum measured values. The SMD limit is 70dB minimum.

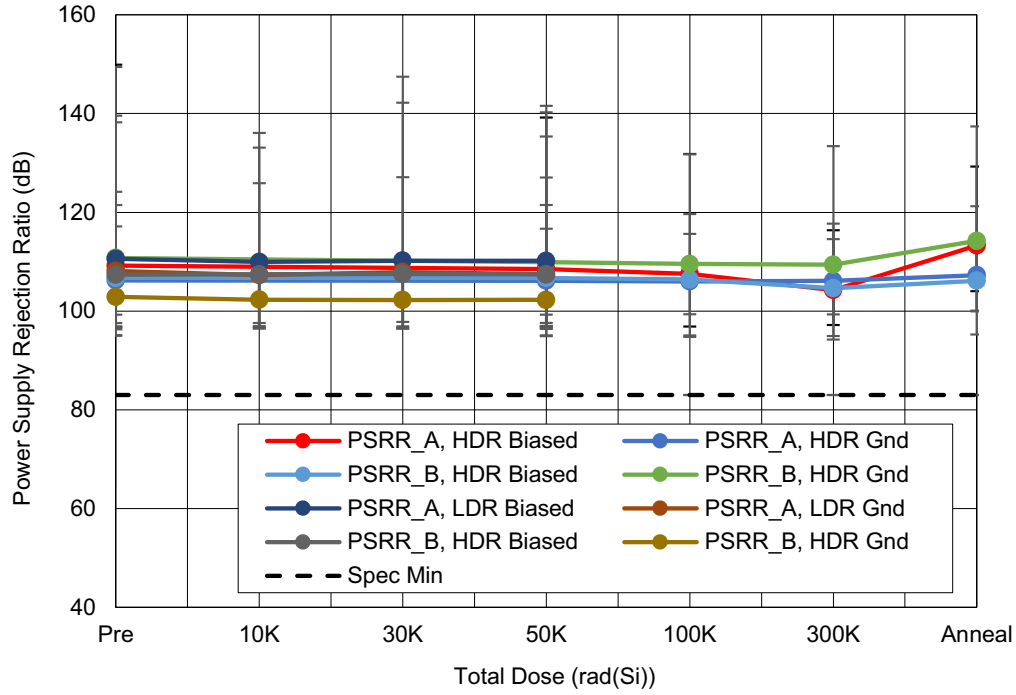

Figure 20. ISL7x244SEH average power supply rejection ratio (PSRR) at V_S = ±19.8V as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars represent the minimum and maximum measured values. The SMD limit is 83dB minimum.

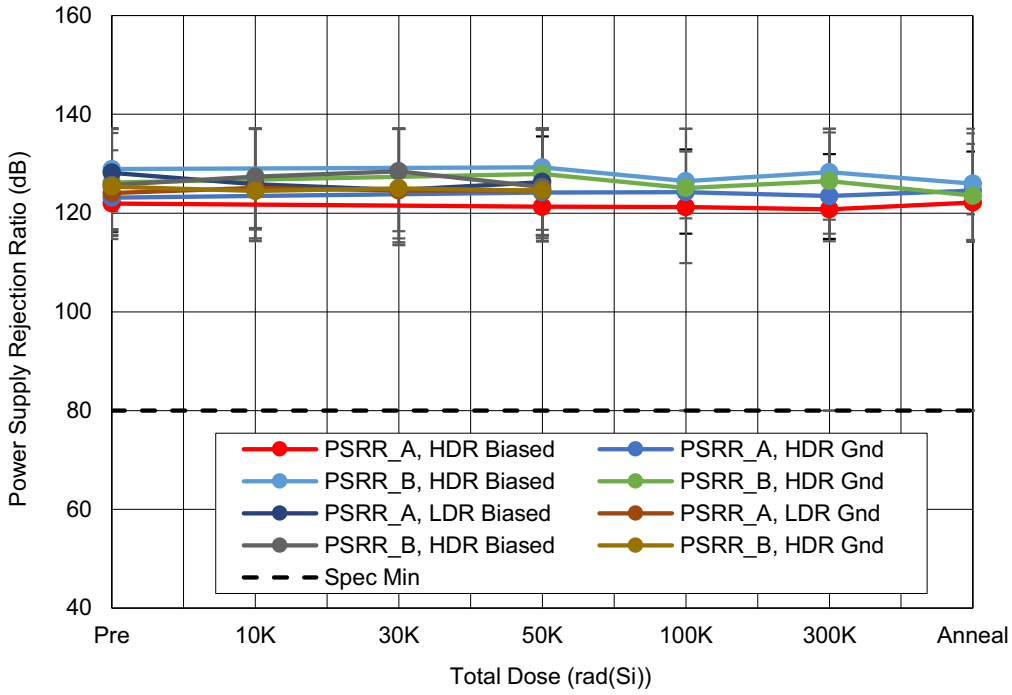

Figure 21. ISL7x244SEH average power supply rejection ratio (PSRR) at V_S = ±2.5V as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars represent the minimum and maximum measured values. The SMD limit is 80dB minimum.

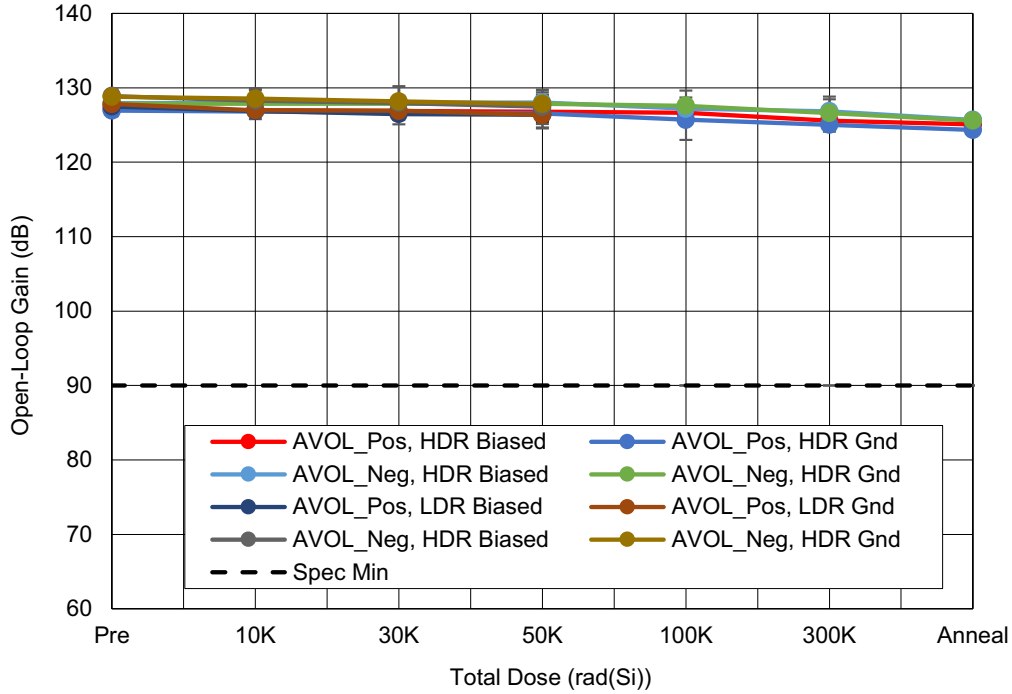

Figure 22. ISL7x244SEH average open-loop gain (A_{VOL}) at V_S = ±19.8V and R_L = 10kΩ to ground as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars the minimum and maximum measured values. The SMD limit is 90dB minimum.

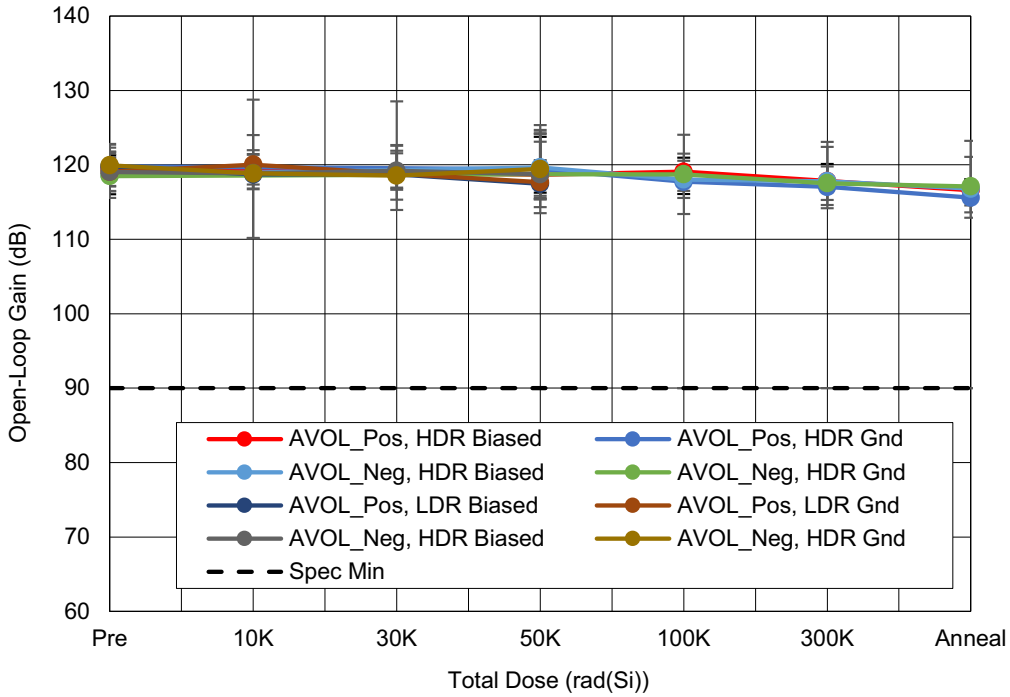

Figure 23. ISL7x244SEH average open-loop gain (A_{VOL}) at V_S = ±2.5V and R_L = 10kΩ to ground as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars represent the minimum and maximum measured values. The SMD limit is 90dB minimum.

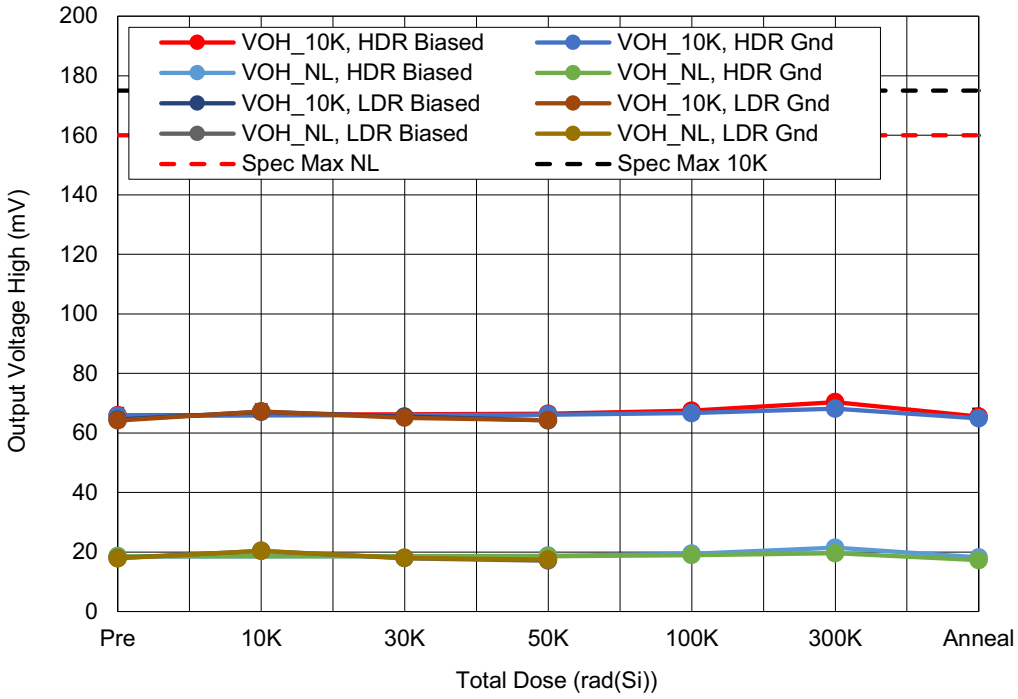

Figure 24. ISL7x244SEH average output voltage high (V_{OH}) at V_S = ±19.8V and R_L = 10kΩ to ground and No Load (NL) as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 175mV maximum for R_L = 10kΩ and 160mV maximum for NL.

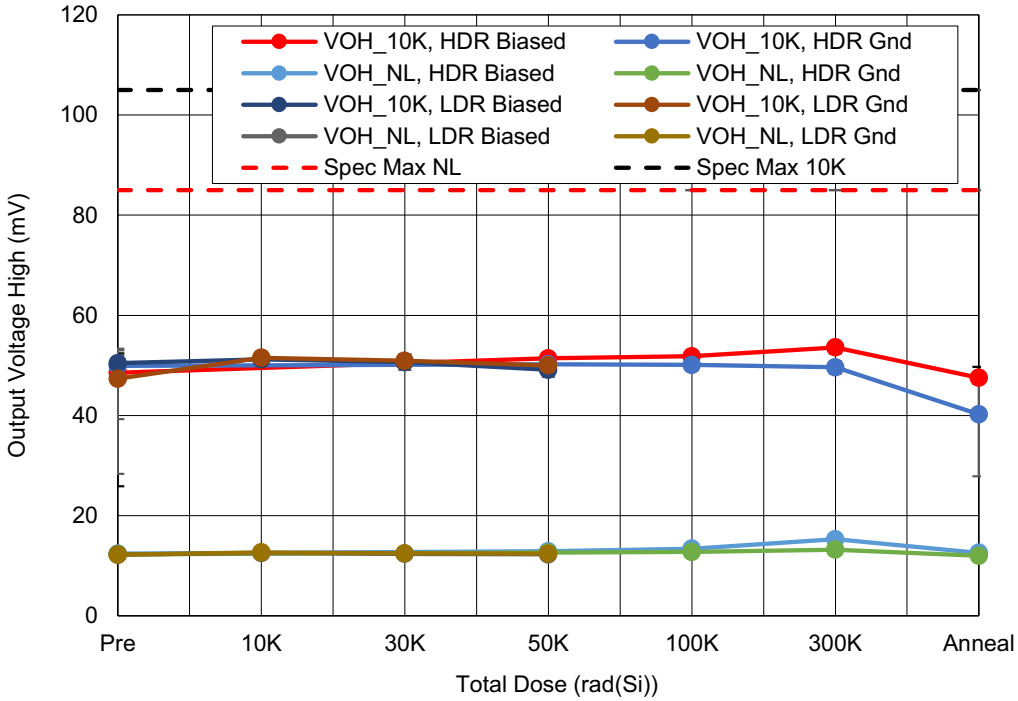

Figure 25. ISL7x244SEH average output voltage high (V_{OH}) at V_S = ±2.5V and R_L = 10kΩ to ground and No Load (NL) as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 105mV maximum for R_L = 10kΩ and 85mV maximum for NL.

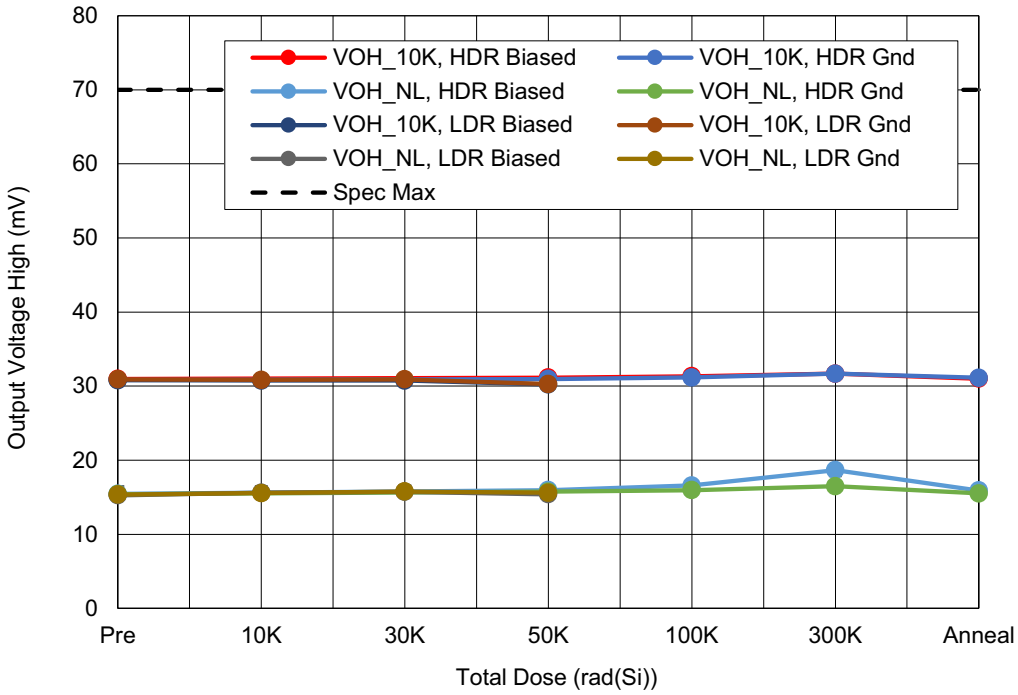

Figure 26. ISL7x244SEH average output voltage high (V_{OH}) at V_S = ±1.35V and R_L = 10kΩ to ground and No Load (NL) as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 70mV maximum for R_L = 10kΩ and NL.

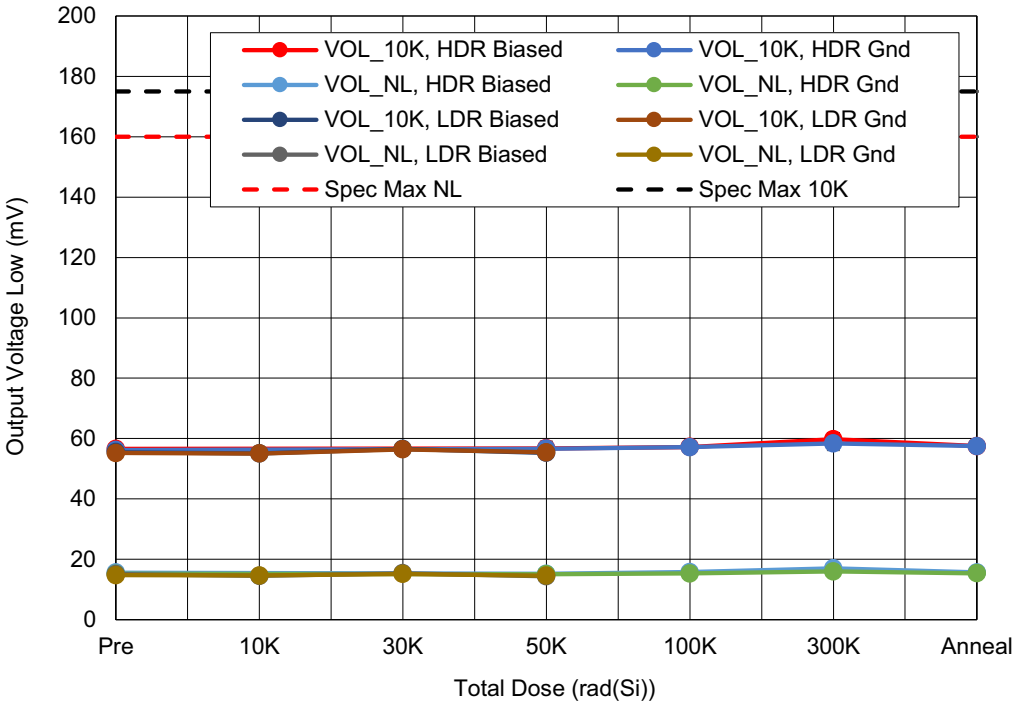

Figure 27. ISL7x244SEH average output voltage low (V_{OL}) at V_S = ±19.8V and R_L = 10kΩ to ground and No Load (NL) as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 175mV maximum for R_L = 10kΩ and 160mV maximum for NL.

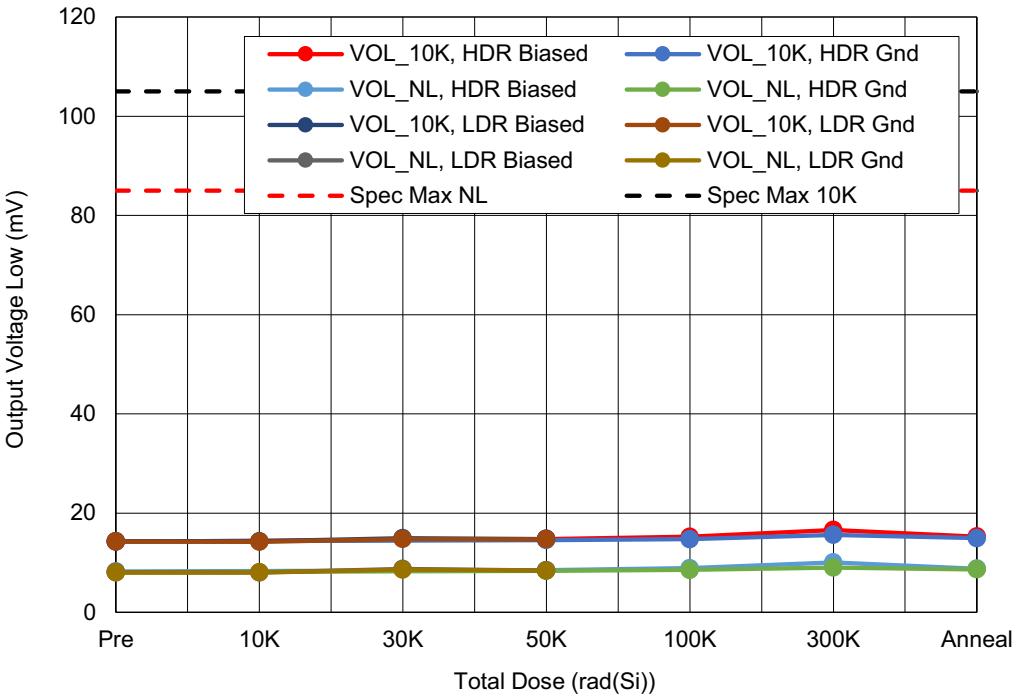

Figure 28. ISL7x244SEH average output voltage low (V_{OL}) at V_S = ±2.5V and R_L = 10kΩ to ground and No Load (NL) as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 105mV maximum for R_L = 10kΩ and 85mV maximum for NL.

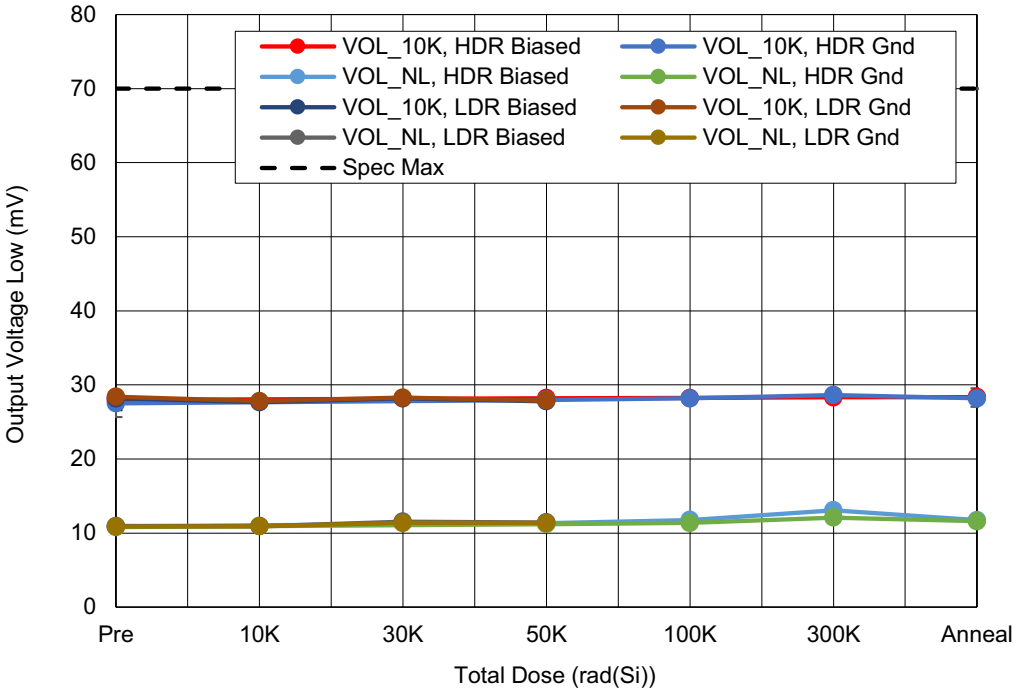

Figure 29. ISL7x244SEH average output voltage low (V_{OL}) at V_S = ±1.35V and R_L = 10kΩ to ground and No Load (NL) as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 70mV maximum for R_L = 10kΩ and NL.

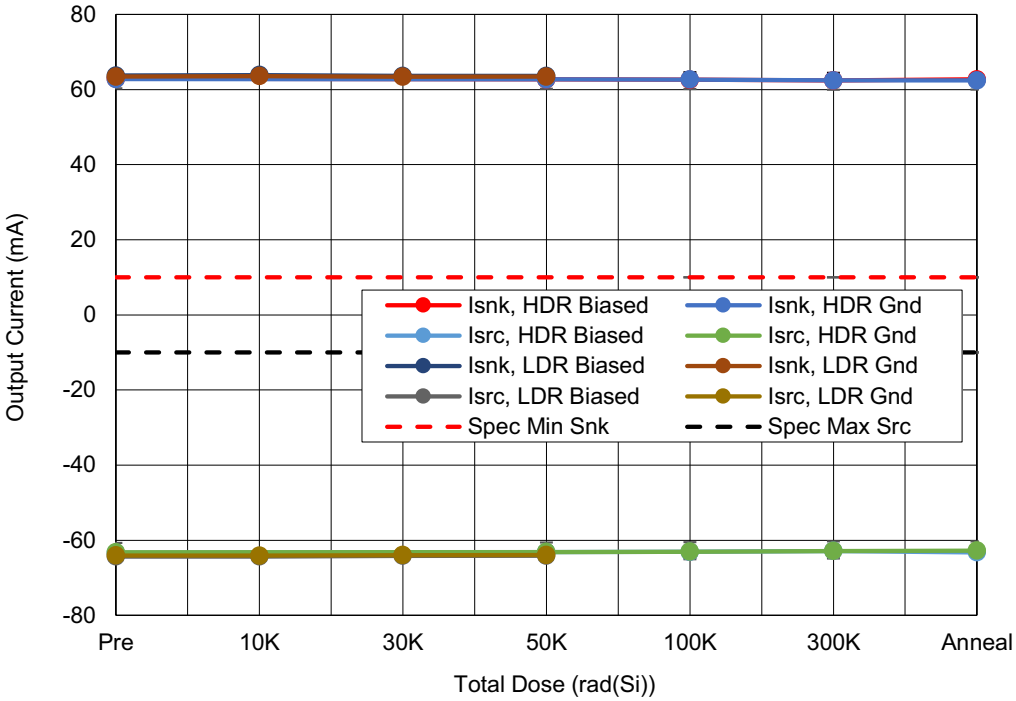

Figure 30. ISL7x244SEH average output short-circuit current (I_{SC}), sourcing and sinking at V_S = ±19.8V and V_{OUT} = -18V sourcing and +18V sinking, as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 10mA minimum (sinking) and -10mA maximum (sourcing).

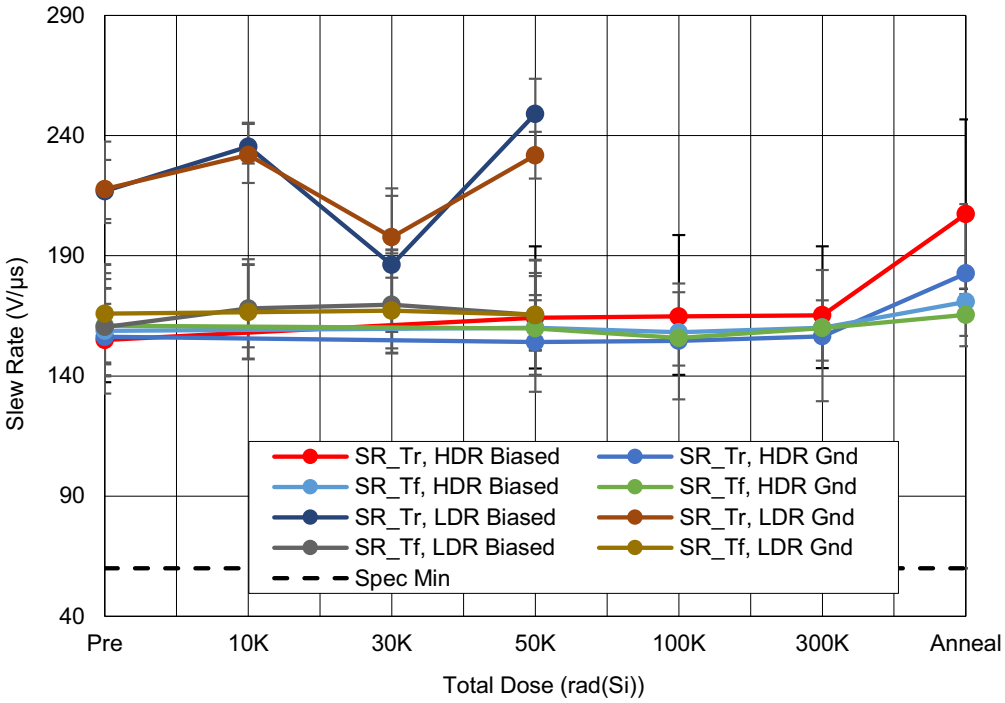

Figure 31. ISL7x244SEH average slew rate (SR) at V_S = ±19.8V and A_V = 1, R_L = 10kΩ to ground and V_O = 10 V_{PP} as a function of LDR irradiation for biased and grounded configurations to 50krad(Si) or HDR irradiation to 300krad(Si) and anneal for biased and grounded configurations. The error bars represent the minimum and maximum measured values. The SMD limit is 60V/µs minimum.

3. Discussion and Conclusion

This document reports the results of the HDR and LDR TID testing of the ISL7x244SEH Radiation Hardened 40V Dual Rail-to-Rail Input-Output, Low-Power Operational Amplifier. Twelve biased and 12 grounded samples were irradiated to 300krad(Si) at a dose rate of 187.16rad(Si)/s. This was followed by a 168-hour anneal of 12 samples (six from the biased samples and six from the unbiased samples) at 100ºC under bias. Sixteen biased and 16 grounded samples were irradiated to 50krad(Si) at a dose rate of 0.01rad(Si)/sec.

All SMD parameters passed at all downpoints. No evidence of bias dependence or LDR sensitivity was observed.

4. Revision History

Revision	Date	Description
1.00	Dec 8, 2023	Initial release.

A. Appendices

A.1 Reported Parameters

Table 3 lists the key parameters that are considered indicative of part performance. These parameters are plotted in Figure 3 through Figure 31. All limits are taken from the ISL7x100SEH SMD.

Table 3. ISL7x244SEH Key Total Dose SMD Parameters (T_A = 25°C)

Fig.	Parameter	Symbol	Low Limit	High Limit	Unit	Notes
3	Supply Current, V_S = ±19.8V	I_{SVN}	-4.4	-	mA	Sum of both Channels
		I_{SVP}	-	4.4		
4	Supply Current, V_S = ±2.5V	I_{SVN}	-3	-	mA	Sum of both Channels
		I_{SVP}	-	3		
5	Supply Current, V_S = ±1.35V	I_{SVN}	-3	-	mA	Sum of both Channels
		I_{SVP}	-	3		
6	Input Offset Voltage, V_{CM} = 0V, ±19.8V	V_{OS}	-500	500	µV	V_S = ±19.8V
7	Input Offset Voltage, V_{CM} = 0V, ±2.5V	V_{OS}	-500	500	µV	V_S = ±2.5V
8	Input Offset Voltage, V_{CM} = 0V, ±1.35V	V_{OS}	-500	500	µV	V_S = ±1.35V
9	Offset Voltage Match, V_{CM} = ±19.8V	ΔV_{OS}	-800	800	µV	V_S = ±19.8V
10	Offset Voltage Match, V_{CM} = ±2.5V					V_S = ±2.5V
11	Offset voltage match, V_{CM} = ±1.35V					V_S = ±1.35V
12	Input Bias Current, V_{CM} = 0V	I_{B+}	-500	500	nA	V_S = ±19.8V
13		I_{B-}				
14	Input Bias Current, V_{CM} = 0V	I_{B+}	-375	375	nA	V_S = ±1.35V
15		I_{B-}				
16	Input Offset Current, V_{CM} = 0V	I_{OS}	-50	50	nA	V_S = ±19.8V
17	Input Offset Current, V_{CM} = 0V	I_{OS}	-50	50	nA	V_S = ±1.35V
18	Common-Mode Rejection Ratio, V_{CM} = $-V_S$ to $+V_S$	CMRR	70	-	dB	V_S = ±19.8V
19	Common-Mode Rejection Ratio, V_{CM} = $-V_S$ to $+V_S$	CMRR	70	-	dB	V_S = ±2.5V
20	Power Supply Rejection Ratio	PSRR	83	-	dB	V_S = ±19.8V
21			80			V_S = ±2.5V
22	Open-Loop Gain, R_L = 10kΩ to ground	A_{VOL}	90	-	dB	V_S = ±19.8V
23						V_S = ±2.5V
24	Output Voltage High, V_S = ±19.8V	V_{OH}	-	175	mV	R_L = 10kΩ
				160		R_L = NL
25	Output Voltage High, V_S = ±2.5V	V_{OH}	-	105	mV	R_L = 10kΩ
				85		R_L = NL
26	Output Voltage High, V_S = ±1.35V	V_{OH}	-	70	mV	R_L = NL or 10kΩ
27	Output Voltage Low, V_S = ±19.8V	V_{OL}	-	175	mV	R_L = 10kΩ
				160		R_L = NL

Table 3. ISL7x244SEH Key Total Dose SMD Parameters (T_A = 25°C) (Cont.)

Fig.	Parameter	Symbol	Low Limit	High Limit	Unit	Notes
28	Output Voltage Low, V_S = ±2.5V	V_{OL}	-	105	mV	R_L = 10kΩ
				85		R_L = NL
29	Output Voltage Low, V_S = ±1.35V	V_{OL}	-	70	mV	R_L = NL or 10kΩ
30	Output Short-Circuit Current, Sourcing	I_{SC}	-	-10	mA	V_{OUT} = -18 V
	Output Short-Circuit Current, Sinking		10	-		V_{OUT} = +18 V
31	Slew Rate, A_V = 1, R_L = 10kΩ, V_O = $10V_{PP}$	SR	60	-	V/µs	V_S = ±19.8V

A.2 Related Literature

For a full list of related documents, visit our website:

- ISL70244SEH and ISL73244SEH device pages

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use o any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.