# ISL70003ASEH

Total Dose Testing

TR023
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## Introduction

This report provides results of a low and high dose rate total dose test of the ISL70003ASEH point-of-load converter. The test was conducted in order to determine the sensitivity of the part to the total dose environment and to determine if the part is low dose rate sensitive. The test also performed biased high temperature anneals after the completion of irradiation in order to evaluate time dependent effects.

## Reference Documents

- MIL-STD-883 test method 1019
- ISL70003ASEH datasheet
- DSCC Standard Microcircuit Drawing (SMD) 5962-14203

## Part Description

The ISL70003ASEH is an improved version of the ISL70003SEH radiation tolerant synchronous buck regulator with improved load regulation (<0.3% typical) and a higher output current rating of 9A. The part uses integrated power MOSFET switching transistors and operates over an input voltage range of 3.0V to 13.2V. The tightly regulated output voltage is externally adjustable from 0.6V to ~90% of the input voltage. Continuous output load current capability is 9A for $T_J \leq +125°C$ and 6A for $T_J \leq +150°C$.

The ISL70003ASEH uses voltage mode control architecture with feed-forward and switches at a selectable frequency of 300kHz or 500kHz. Loop compensation is externally adjustable to allow for an optimum balance between stability and output dynamic performance. The device features two logic-level disable inputs that can be used to inhibit pulses on the phase (LXx) pins in order to maximize efficiency based on the load current. The ISL70003ASEH also supports DDR applications and contains a buffer amplifier for generating the VREF voltage. Typical ISL70003ASEH applications include FPGA, CPLD and DSP power management, CPU core and I/O supply and DDR memory power management in high-density distributed power systems for space applications. All existing ISL70003SEH supporting collateral is relevant to the ISL70003ASEH and can be used as such.

The ISL70003ASEH is radiation tolerant to a Total Dose (TID) rating of 100krad(Si) at both high (50rad(Si)/s to 300rad(Si)/s) and low (<0.01rad(Si)/s) dose rates as specified in MIL-STD-883 test method 1019. The present document reports data for 75krad(Si) at low dose rate and 150krad(Si) at high dose rate, with the irradiations followed by a biased anneal at 100°C for 168 hours. No failures were encountered at any downpoint and the samples displayed excellent stability. The part is acceptance tested on a wafer-by-wafer basis to 50krad(Si) at low dose rate and to 100krad(Si) at high dose rate, as indicated by the (-EH) suffix in the part number.

The ISL70003ASEH is also Single-Event Effects (SEE) tolerant to a Linear Energy Transfer (LET) value of $86.4MeV \cdot cm^2/mg$. Single-Event Transients (SET) are a major issue in power management parts driving voltage-sensitive loads, and the ISL70003ASEH provides superior performance in this environment. In [1] we report results of SEE testing of the ISL70003SEH, which apply directly to the ISL70003ASEH.

The ISL70003ASEH is implemented in a submicron BiCMOS process optimized for power management applications. The process is in volume production under MIL-PRF-38535 certification and is used for a wide range of commercial power management devices.

Specifications for radiation tolerant QML devices are controlled by the Defense Logistics Agency, Land and Maritime (DLA) in Columbus, OH. The SMD is the controlling document and must be cited when ordering.

## Test Description

### Irradiation Facilities

High dose rate testing was performed using a Gammacell 220 $^{60}Co$ irradiator located in the Palm Bay, Florida Intersil facility. Low dose rate testing used a Hopewell Designs (Alpharetta, GA) N40 vault-type low dose rate irradiator located in the same facility. The high dose rate irradiations were performed at approximately 54rad(Si)/s and the low dose rate work was performed at 0.010rad(Si)/s, both per MIL-STD-883 Method 1019. In the low dose rate facility, PbAl spectrum hardening boxes are used to shield the test fixture and devices under test against low energy secondary gamma radiation. The post-irradiation biased anneals were performed at 100°C using a small temperature chamber.

### Test Fixturing

Figure 1 on page 2 shows the configuration used for biased low and high dose rate irradiation in conformance with Standard Microcircuit Drawing (SMD) 5962-14203.

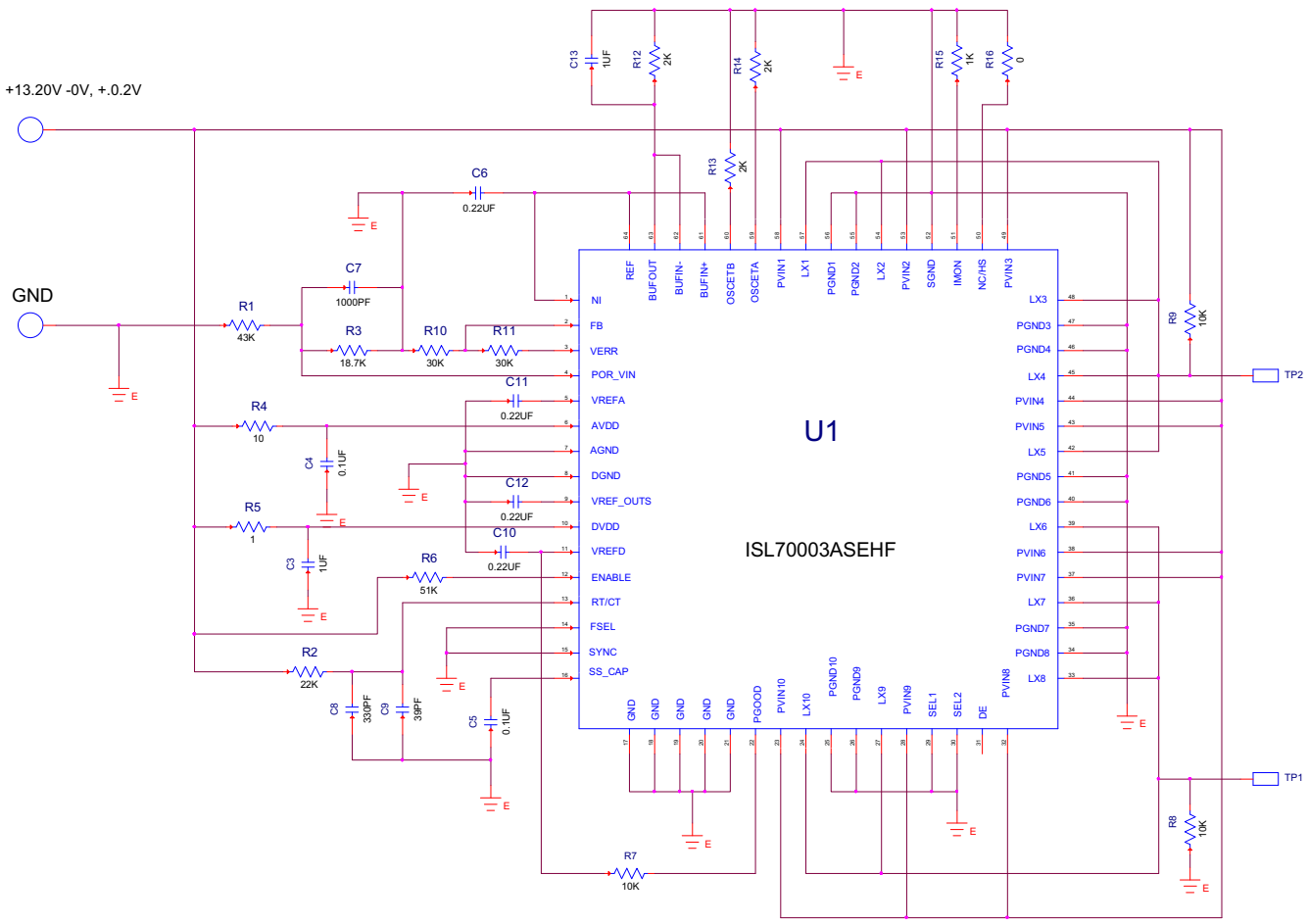


FIGURE 1. IRRADIATION BIAS CONFIGURATION FOR THE ISL70003ASEH PER STANDARD MICROCIRCUIT DRAWING (SMD) 5962–14203

## Characterization Equipment and Procedures

All electrical testing was performed outside the irradiator using the production automated test equipment (ATE) with datalogging at each downpoint. Downpoint electrical testing was performed at room temperature.

## Experimental Matrix

Testing proceeded in accordance with the low dose rate sensitivity diagnostic protocol outlined in MIL-STD-883 Test Method 1019 with enhanced sample sizes to insure repeatable data. The experimental matrix consisted of ten samples irradiated at high dose rate with all pins grounded, ten samples irradiated at high dose rate under bias, twelve samples irradiated at low dose rate with all pins grounded and twelve samples irradiated at low dose rate under bias. Three control units were used.

A biased anneal at 100°C for 168 hours was performed following all irradiations to evaluate the Time Dependent Effect (TDI) characteristics of the process. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal.

Samples of the ISL70003ASEH were drawn from Lot 4Q01B00000, wafer VZAP4SW (lot sealed 19 February 2015). Samples were packaged in hermetic 64 Ld Ceramic Quad Flatpacks (CQFP), code RKV. Samples were processed through the standard QML-V burn-in screens of 180 hours dynamic burn-in and 72 hours static burn-in cycle before irradiation, as required by MIL-STD-883, and were screened to the SMD 5962-14203 limits at room, low and high temperatures before the start of total dose testing.

## Downpoints

High dose rate downpoints were 0, 30, 50, 100 and 150krad(Si) and low dose rate downpoints were 0, 10, 30, 50 and 75rad(Si). The biased anneals were performed at 100°C for 168 hours.

# Results

Total dose testing of the ISL70003ASEH is complete and showed no reject devices after irradiation at either dose rate. All samples were classified as Bin 1 at all downpoints, indicating full compliance with all datasheet and SMD parametric limits.

## Attributes Data

TABLE 1. ATTRIBUTES DATA

| PART | DOSE RATE, rad(Si)/s | BIAS | SAMPLE SIZE | DOWNPOINT | PASS (Note 1) | FAIL |
|---|---|---|---|---|---|---|
| ISL70003ASEH | 0.01 | Biased | 12 | Pre-irradiation | 12 | 0 |
| | | | | 10krad(Si) | 12 | 0 |
| | | | | 30krad(Si) | 12 | 0 |
| | | | | 50krad(Si) | 12 | 0 |
| | | | | 75krad(Si) | 12 | 0 |
| | | | | Anneal | 12 | 0 |
| ISL70003ASEH | 0.01 | Grounded | 12 | Pre-irradiation | 12 | 0 |
| | | | | 10krad(Si) | 12 | 0 |
| | | | | 30krad(Si) | 12 | 0 |
| | | | | 50krad(Si) | 12 | 0 |
| | | | | 75krad(Si) | 12 | 0 |
| | | | | Anneal | 12 | 0 |
| ISL70003ASEH | 54 | Biased | 10 | Pre-irradiation | 10 | 0 |
| | | | | 30krad(Si) | 10 | 0 |
| | | | | 50krad(Si) | 10 | 0 |
| | | | | 100krad(Si) | 10 | 0 |
| | | | | Post 100krad(Si) anneal | 5 | 0 |
| | | | | 150krad(Si) | 5 | 0 |
| | | | | Post 150krad(Si) anneal | 5 | 0 |
| ISL70003ASEH | 54 | Grounded | 10 | Pre-irradiation | 10 | 0 |
| | | | | 30krad(Si) | 10 | 0 |
| | | | | 50krad(Si) | 10 | 0 |
| | | | | 100krad(Si) | 10 | 0 |
| | | | | Post 100krad(Si) anneal | 5 | 0 |
| | | | | 150krad(Si) | 5 | 0 |
| | | | | Post 150krad(Si) anneal | 5 | 0 |

NOTE:

1. ‘Pass’ indicates a sample that passes all SMD limits.

## Variables Data

The ISL70003ASEH is a complex part and plotting all of the approximately 300 tested parameters would be a lengthy undertaking. Figures 2 through 30 show data for representative parameters at all downpoints. The plots show the average as a function of total dose for each of the irradiation conditions. The anneals are shown as ‘LDR anneal’ for the anneal following 75krad(Si) at low dose rate, ‘HDR anneal 1’ for the anneal of half the HDR samples after 100krad(Si) at high dose rate and ‘HDR anneal 2’ for the anneal of the remaining HDR samples after 150krad(Si) at high dose rate.

All parts showed excellent stability over irradiation and anneal, with no observed dose rate or bias sensitivity. It should be noted that the SMD data tables contain no post-total dose limits; the pre- and post-irradiation limits are identical. This implies that the part has no dose rate sensitivity by definition, and this conclusion is confirmed by the data. Figure 7 reports the total dose response of the reference tolerance parameter ($V_{REF}$ + error amplifier input offset voltage), and we have plotted the average, minimum and maximum at each downpoint for this parameter of particular interest.

# Variables Data Plots

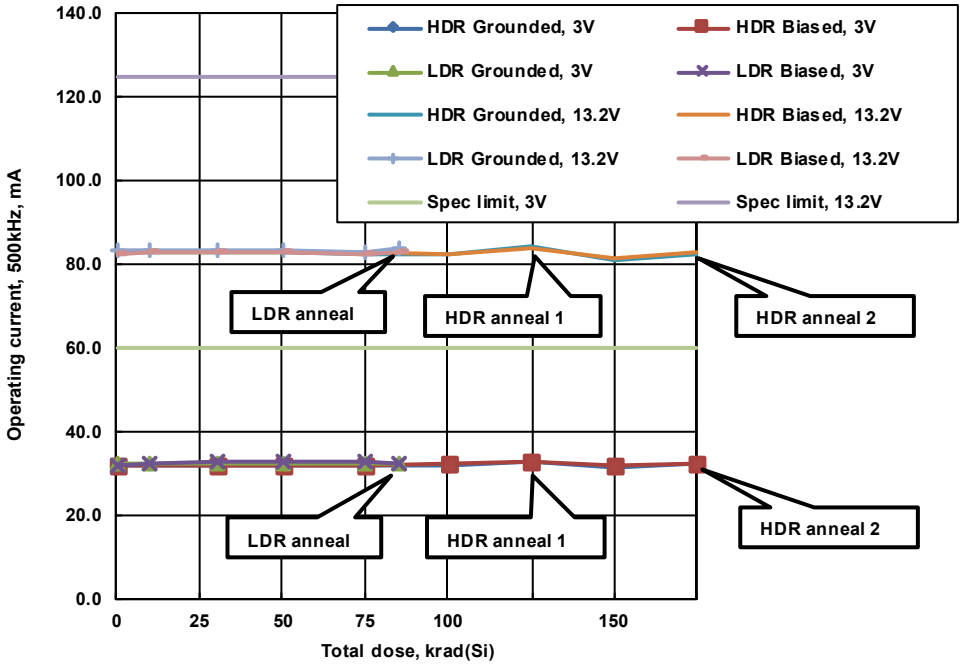


**FIGURE 2. ISL70003ASEH operating current at 500kHz, 3V and 13.2V supply cases, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limits are 60mA maximum (3V case) and 125mA maximum (13.2V case).**

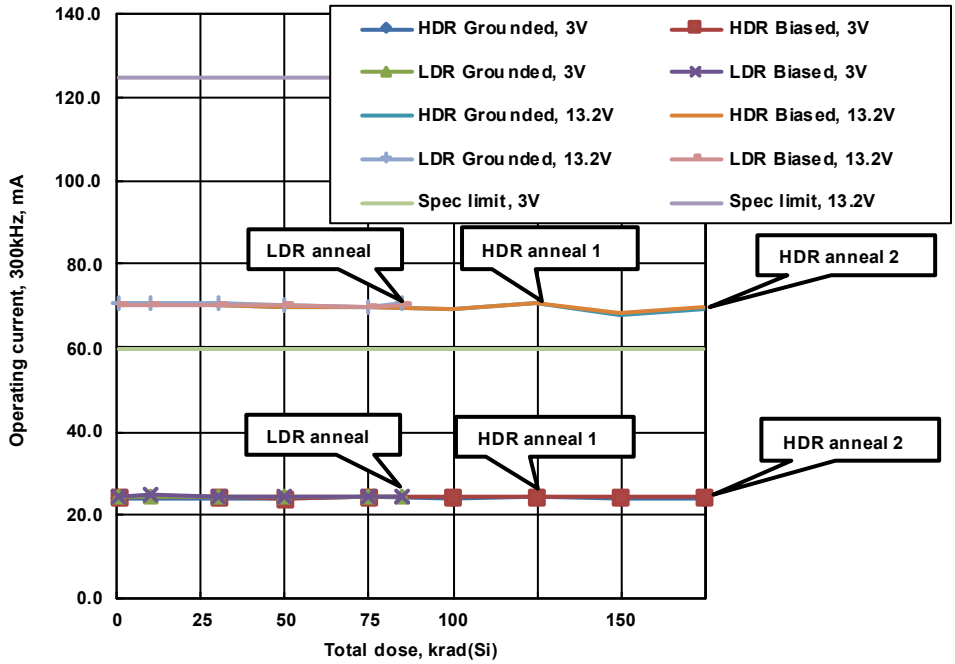


**FIGURE 3. ISL70003ASEH operating current at 300kHz, 3V and 13.2V supply cases, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limits are 60mA maximum (3V case) and 125mA maximum (13.2V case).**

## Variables Data Plots (Continued)

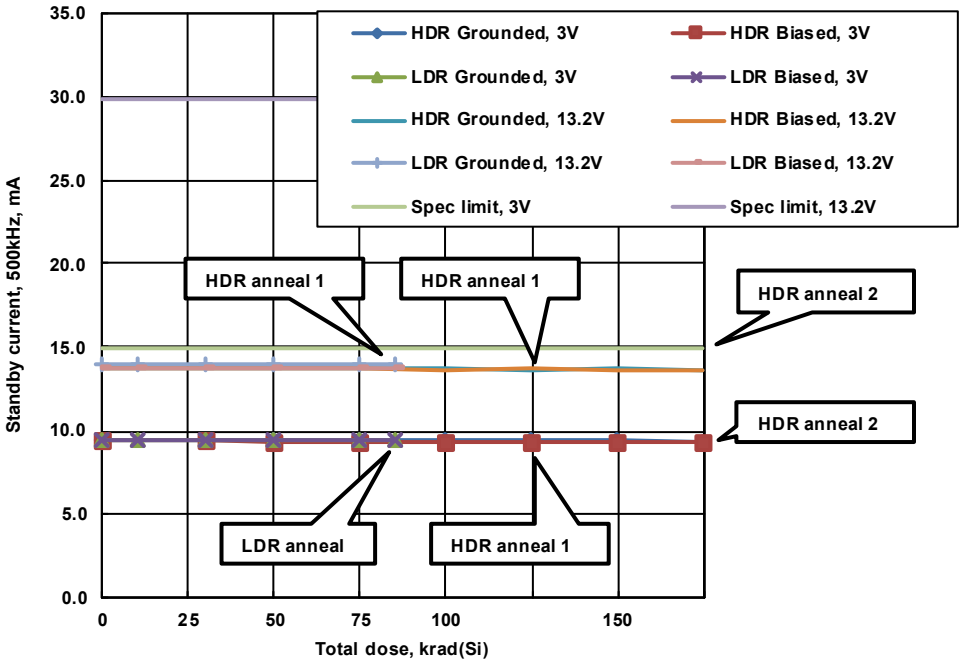


**FIGURE 4. ISL70003ASEH standby current at 500kHz, 3V and 13.2V supply cases, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limits are 15mA maximum (3V case) and 30mA maximum (13.2V case).**

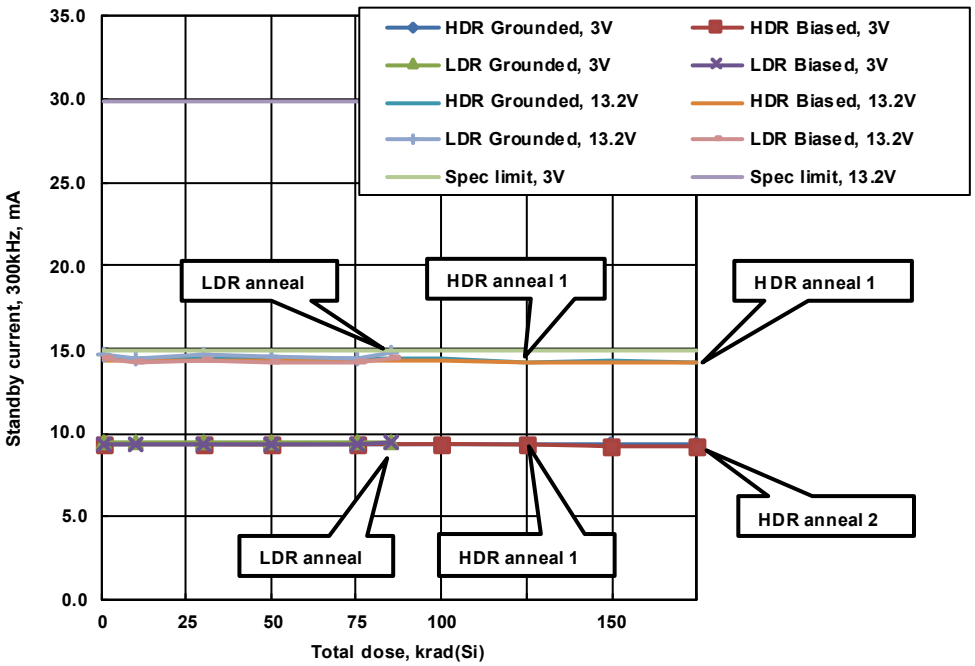


**FIGURE 5. ISL70003ASEH standby current at 300kHz, 3V and 13.2V supply cases, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limits are 15mA maximum (3V case) and 30mA maximum (13.2V case).**

## Variables Data Plots (Continued)

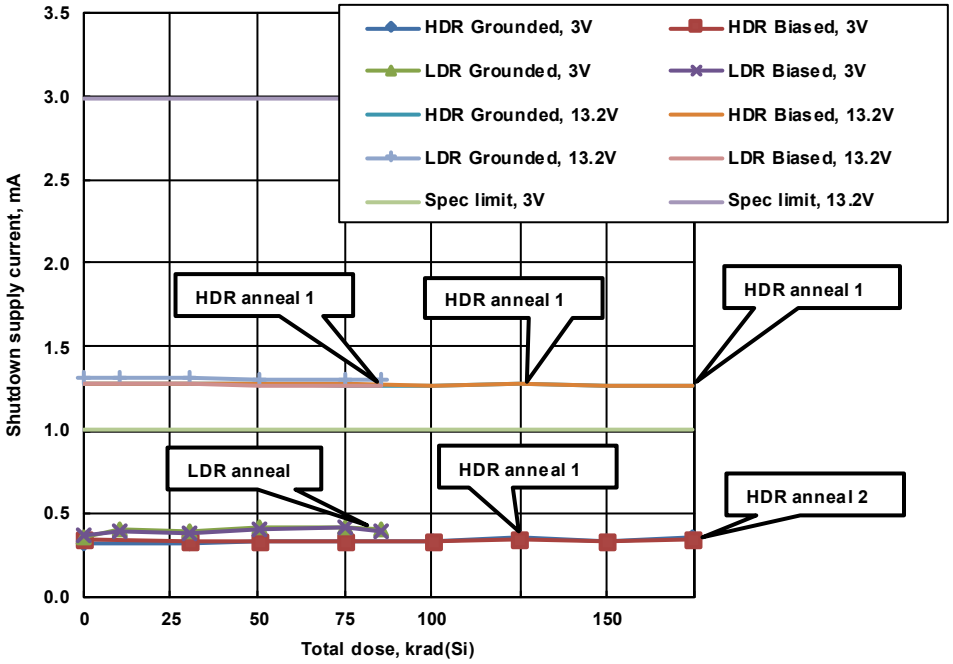


**FIGURE 6. ISL70003ASEH shutdown ('quiescent') supply current, 3V and 13.2V supply cases, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limits are 1mA maximum (3V case) and 3mA maximum (13.2V case).**

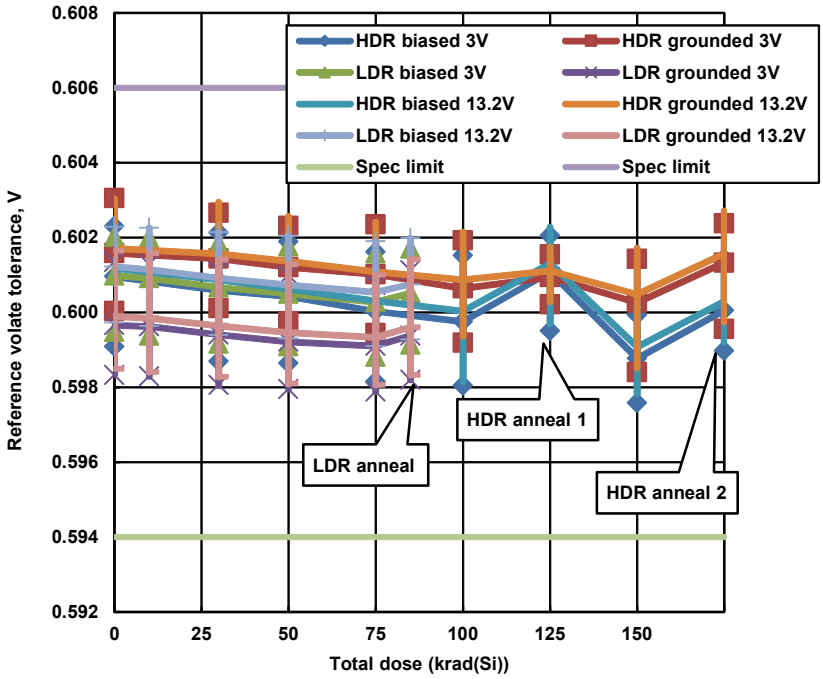


**FIGURE 7. ISL70003ASEH reference voltage tolerance, reference voltage + error amplifier offset voltage, 3V and 13.2V supply cases, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limits are 0.594V to 0.606V. The plot shows the average, minimum and maximum at each downpoint.**

## Variables Data Plots (Continued)

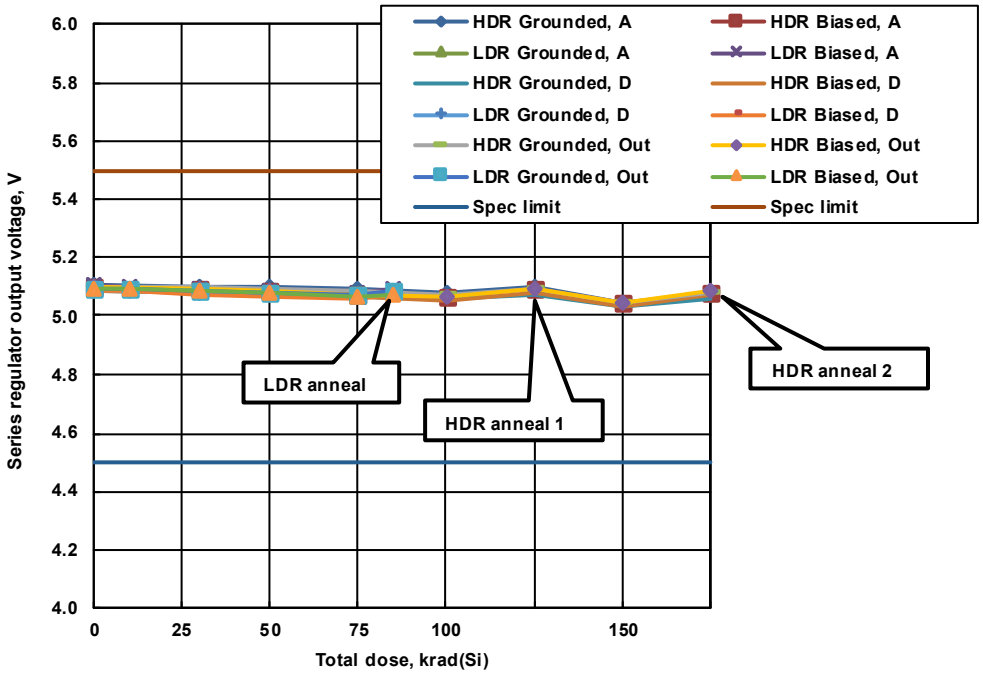


**FIGURE 8. ISL70003ASEH on-chip series regulator output voltage, 13.2V supply, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limits are 4.5V to 5.5V.**

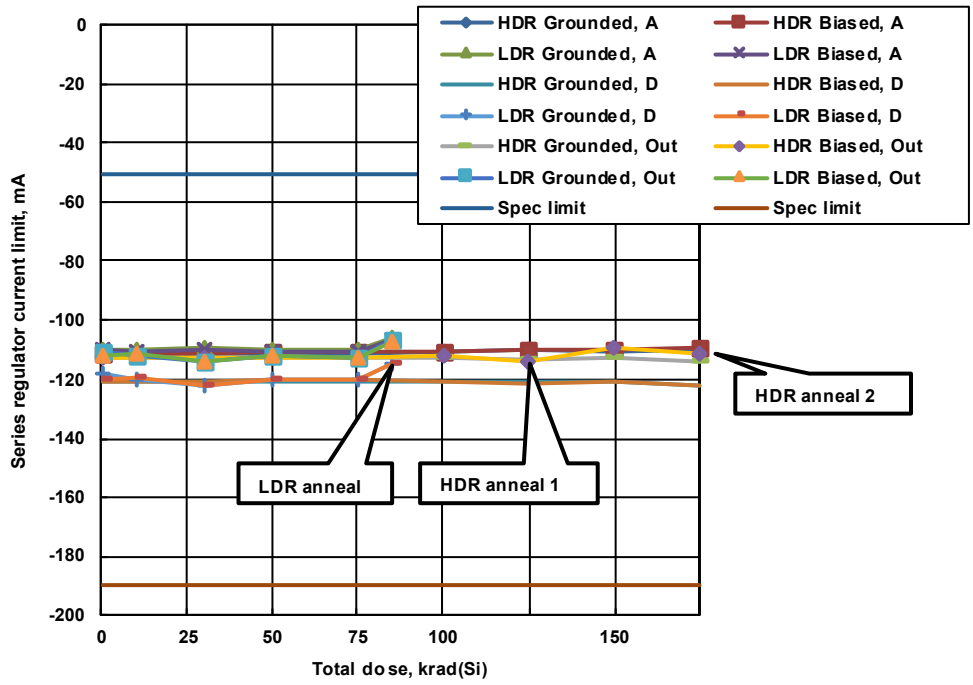


**FIGURE 9. ISL70003ASEH on-chip series regulator current limit as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limits are -50mA to -190mA.**

## Variables Data Plots (Continued)

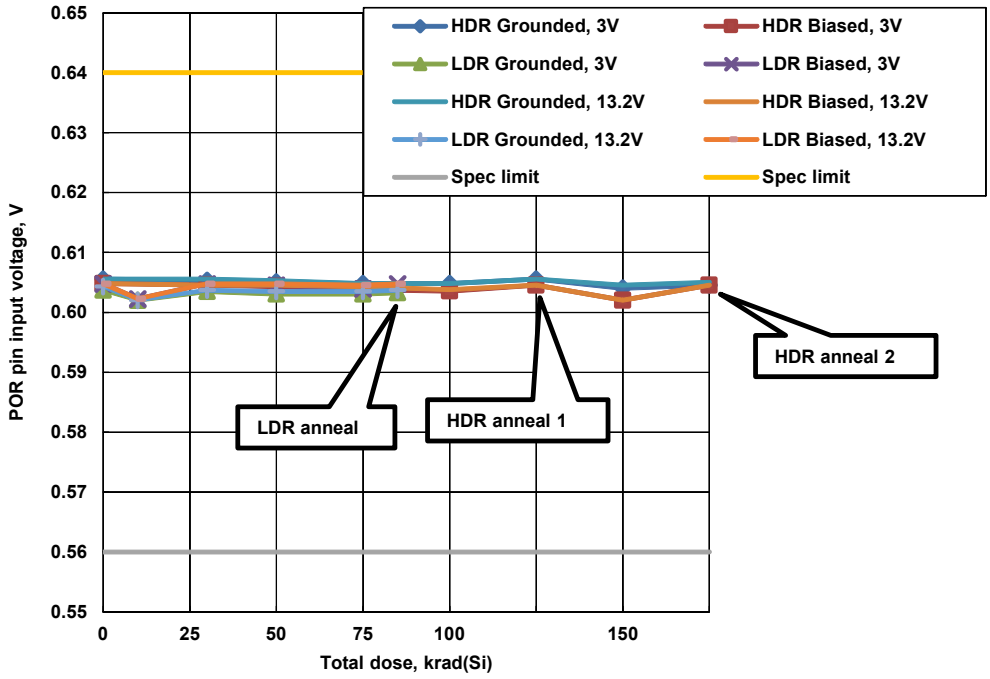


**FIGURE 10. ISL70003ASEH Power-On Reset (POR) input pin voltage, 3V and 13.3V supply cases, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limits are 0.56V to 0.64V.**

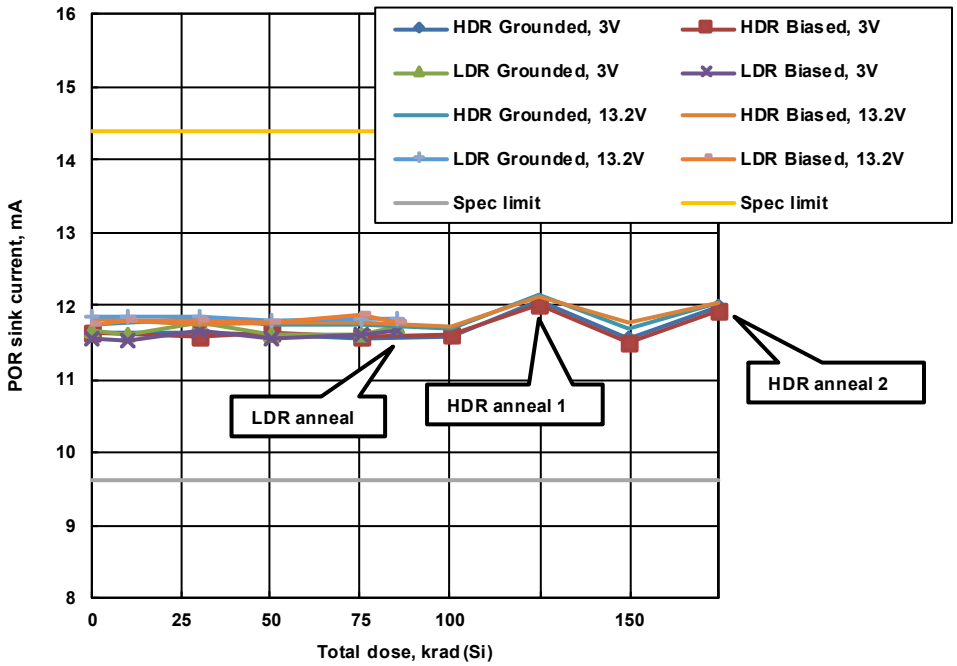


**FIGURE 11. ISL70003ASEH Power-On Reset (POR) sink current, 3V and 13.3V supply cases, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limits are 9.6mA to 14.4mA.**

## Variables Data Plots (Continued)

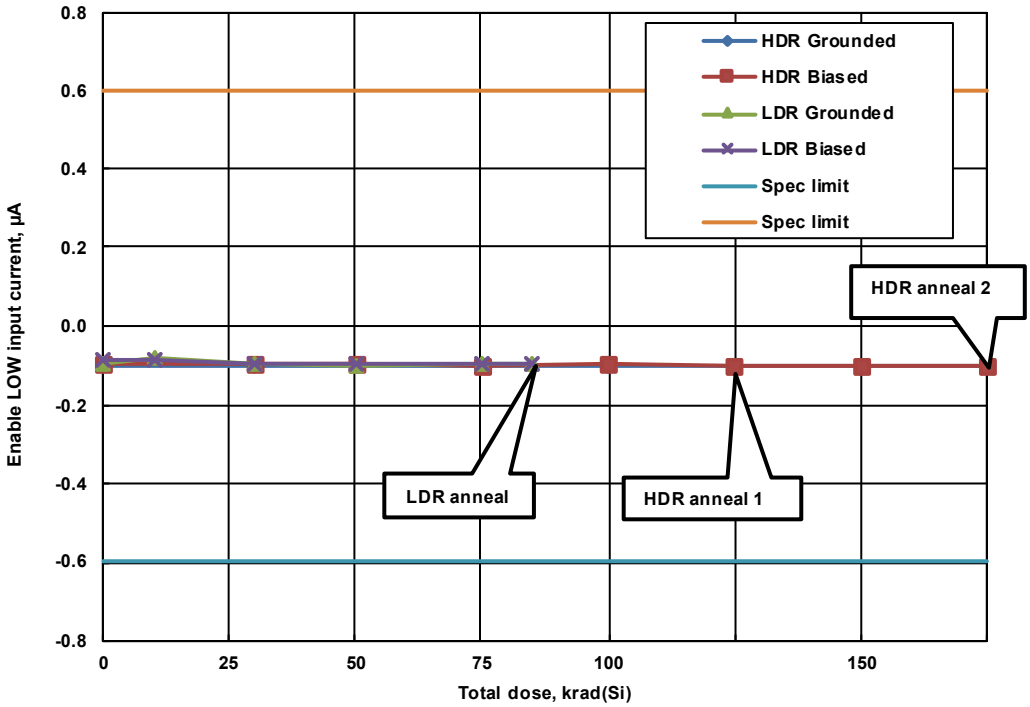


**FIGURE 12. ISL70003ASEH enable LOW input current, 13.2V supply, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The ATE limits are -0.6µA to +0.6µA; the parameter is not specified in the SMD.**

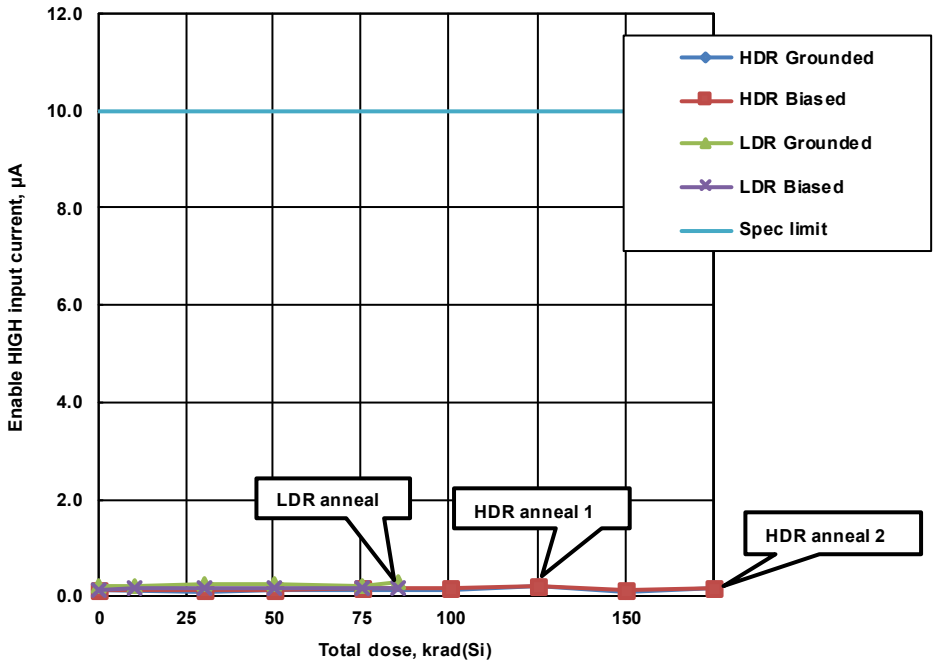


**FIGURE 13. ISL70003ASEH enable HIGH input current, 13.2 supply, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limit is 10.0µA maximum.**

## Variables Data Plots (Continued)

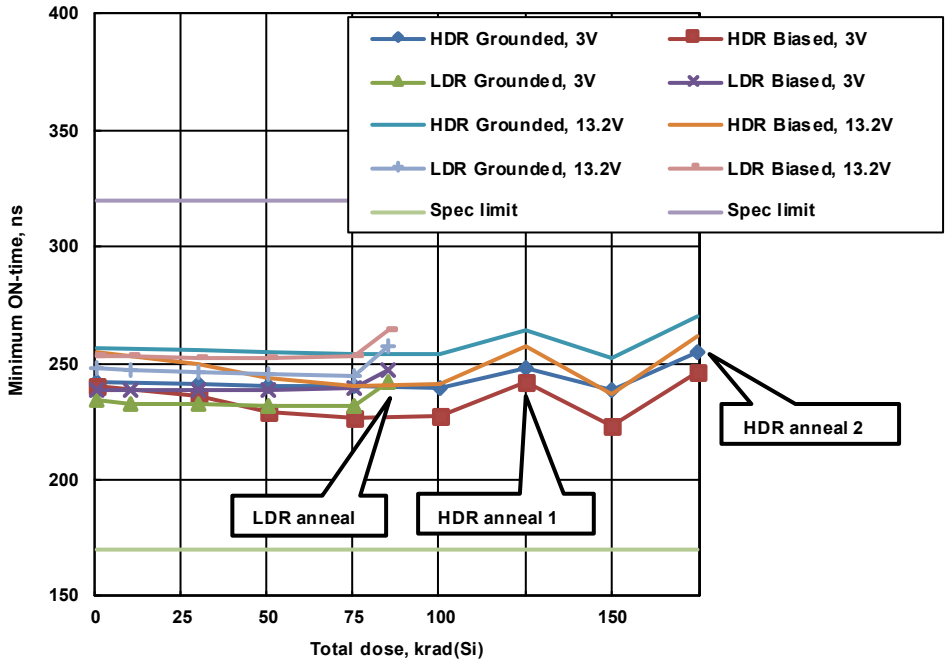


FIGURE 14. ISL70003ASEH minimum ON-time, 3V and 13.2V supply cases, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limit is 320ns maximum; the 170ns lower bound is an ATE 'sanity' limit.

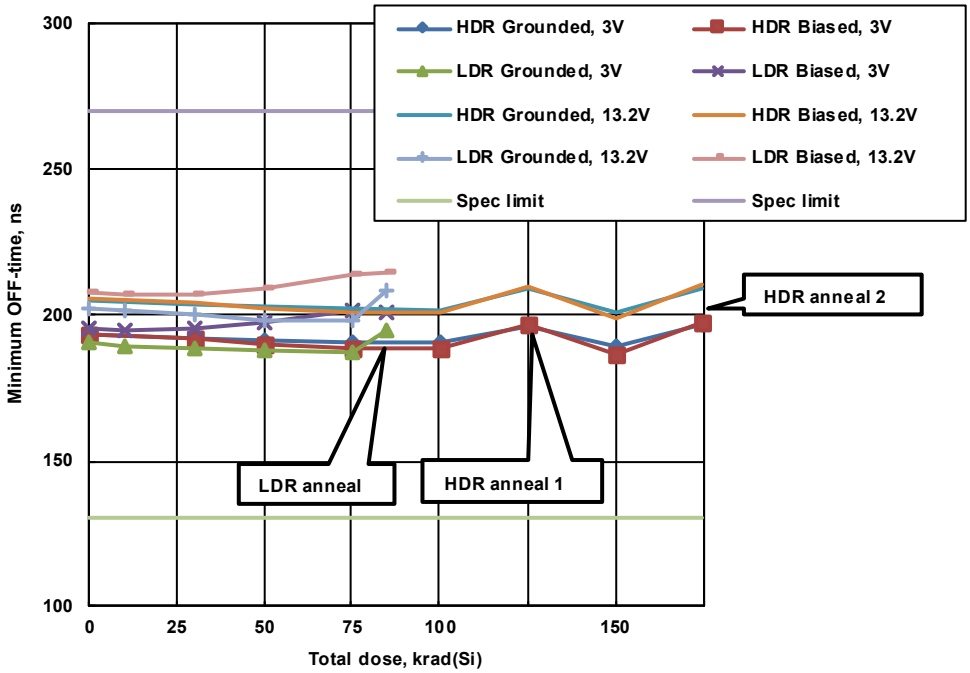


FIGURE 15. ISL70003ASEH minimum OFF-time, 3V and 13.2V supply cases, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limit is 270ns maximum; the 130ns lower bound is an ATE 'sanity' limit.

## Variables Data Plots (Continued)

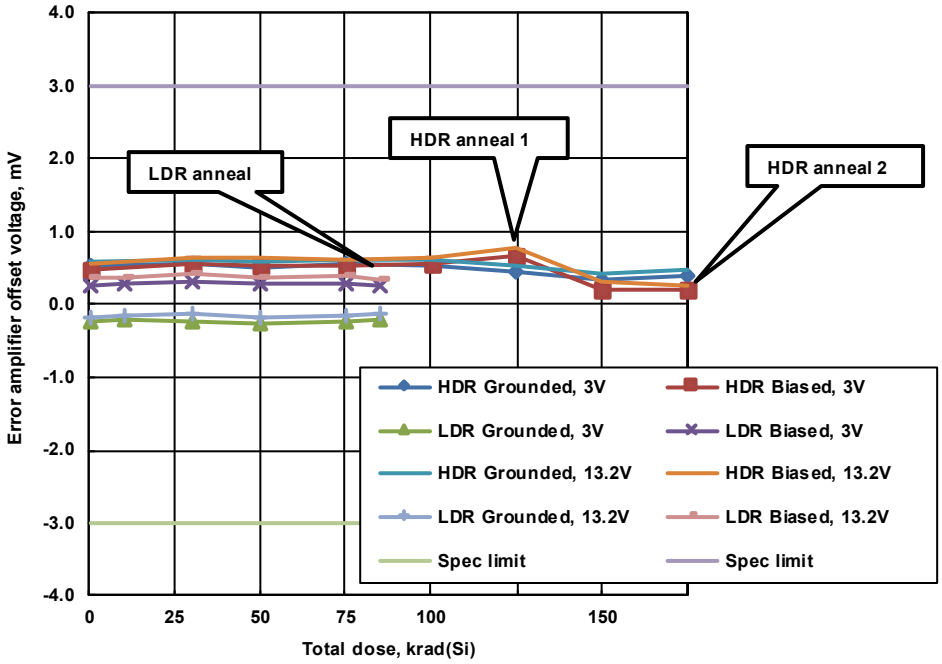


**FIGURE 16. ISL70003ASEH error amplifier input offset voltage, 3V and 13.2V supply cases, as a function of total dose unbiased and biased cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limits are -3.0mV to 3.0mV.**

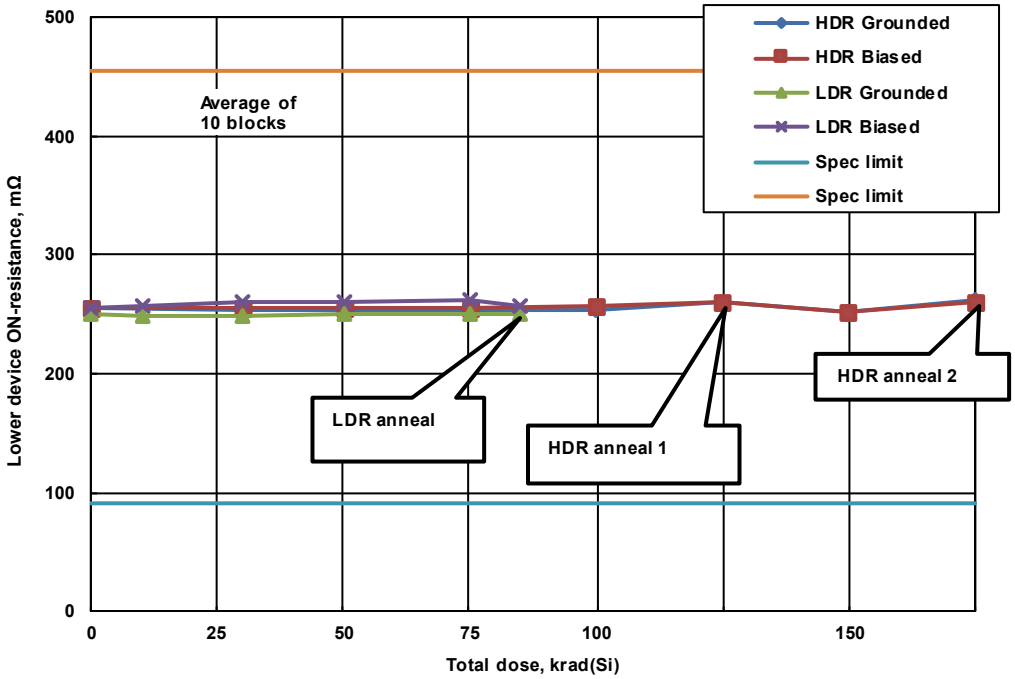


**FIGURE 17. ISL70003ASEH lower device ON-resistance at 3V supply, average of ten power blocks, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limits are 90mΩ to 455mΩ.**

## Variables Data Plots (Continued)

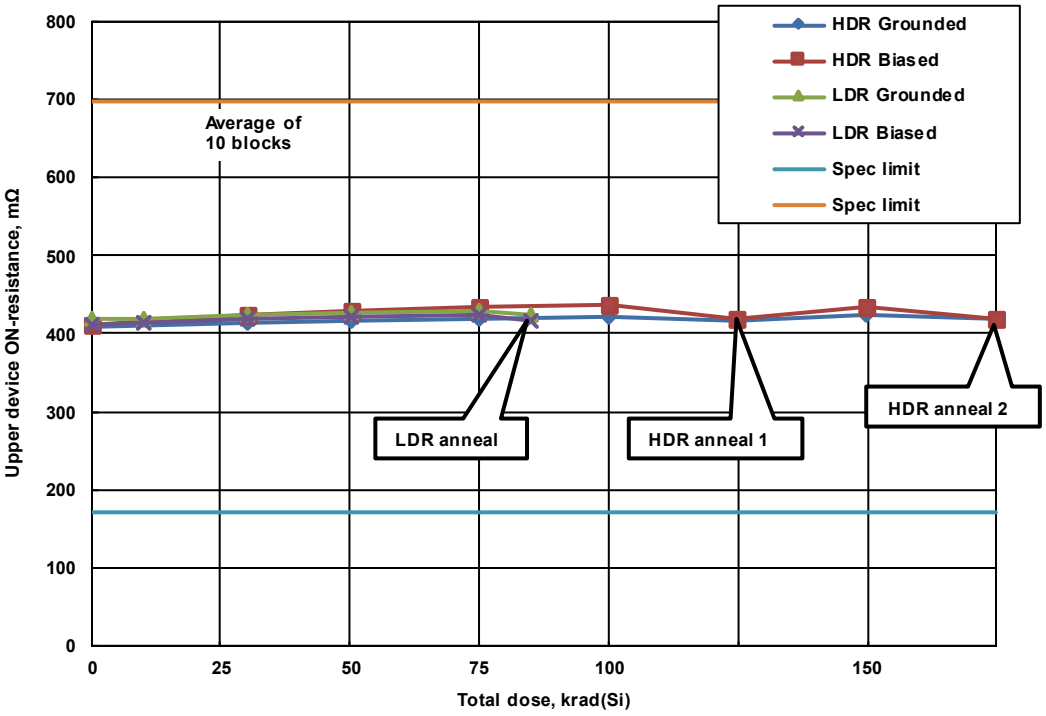


**FIGURE 18. ISL70003ASEH upper device ON-resistance at 3V supply, average of ten power blocks, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limits are 170mΩ to 700mΩ.**

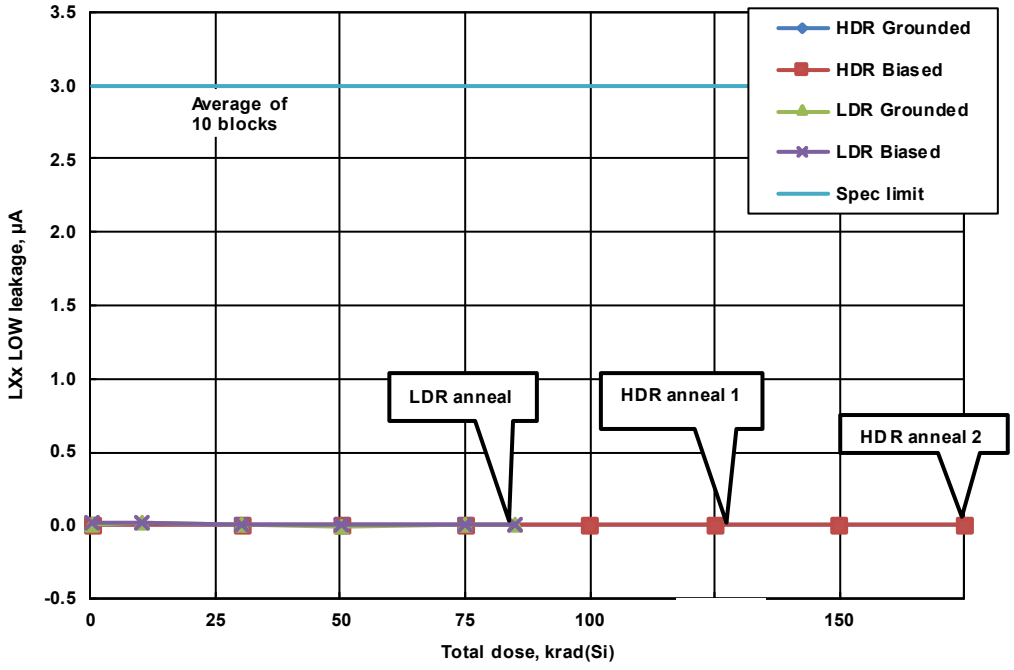


**FIGURE 19. ISL70003ASEH LXx LOW leakage current, average of ten power blocks, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limit is 3.0µA maximum.**

## Variables Data Plots (Continued)

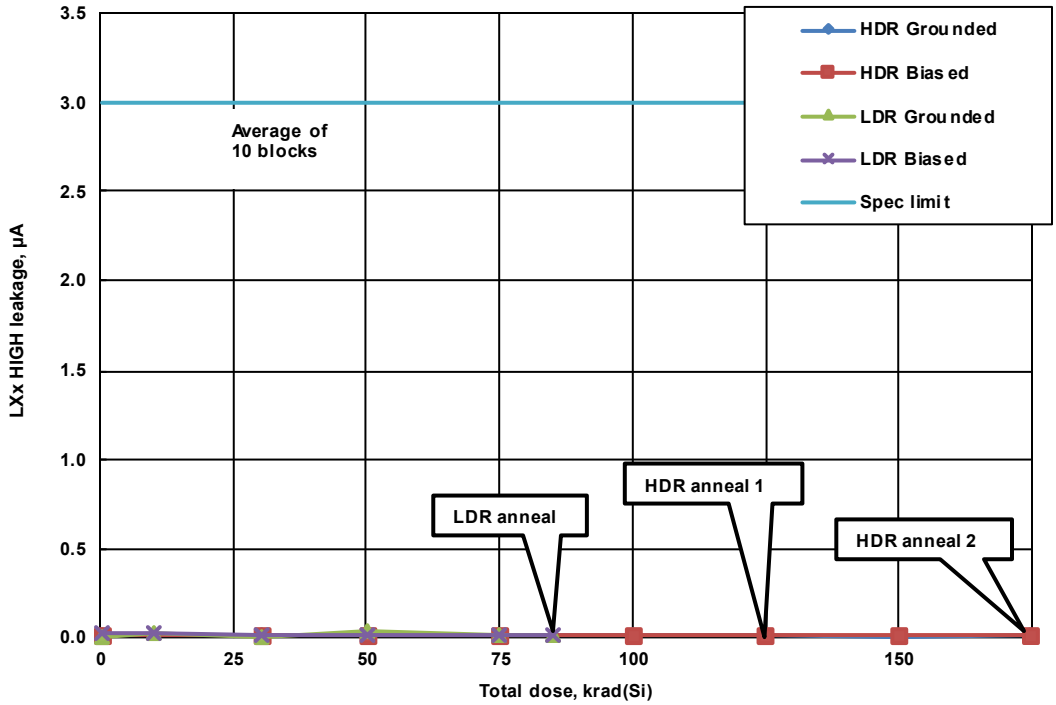


FIGURE 20. ISL70003ASEH LXx HIGH leakage current, average of ten power blocks, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limit is 3.0µA maximum.

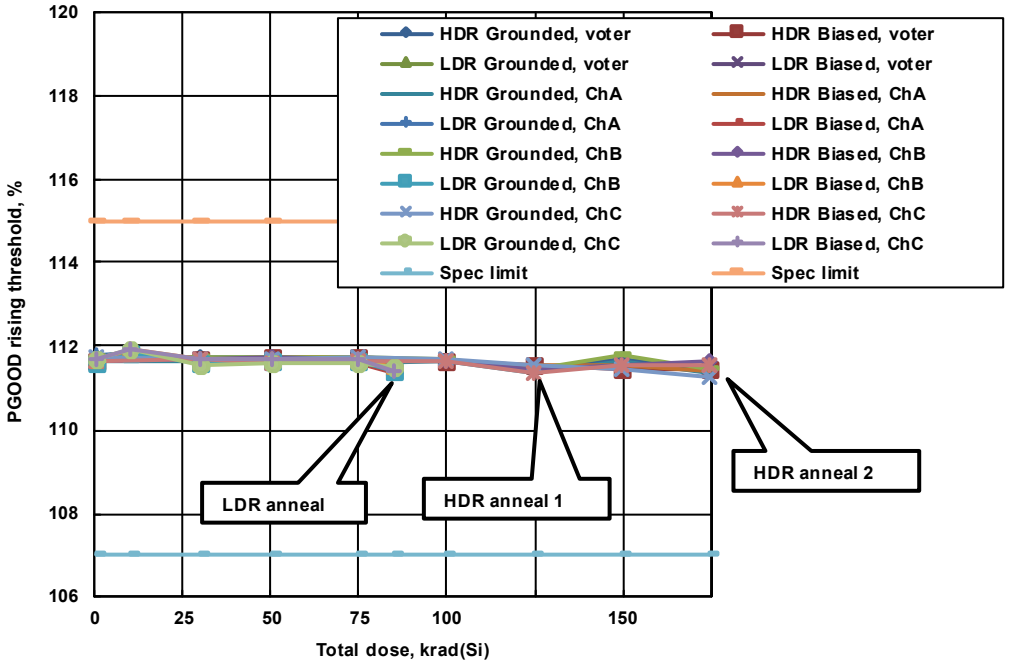


FIGURE 21. ISL70003ASEH Power-Good (PGOOD) rising threshold as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limits are 107% to 115%.

## Variables Data Plots (Continued)

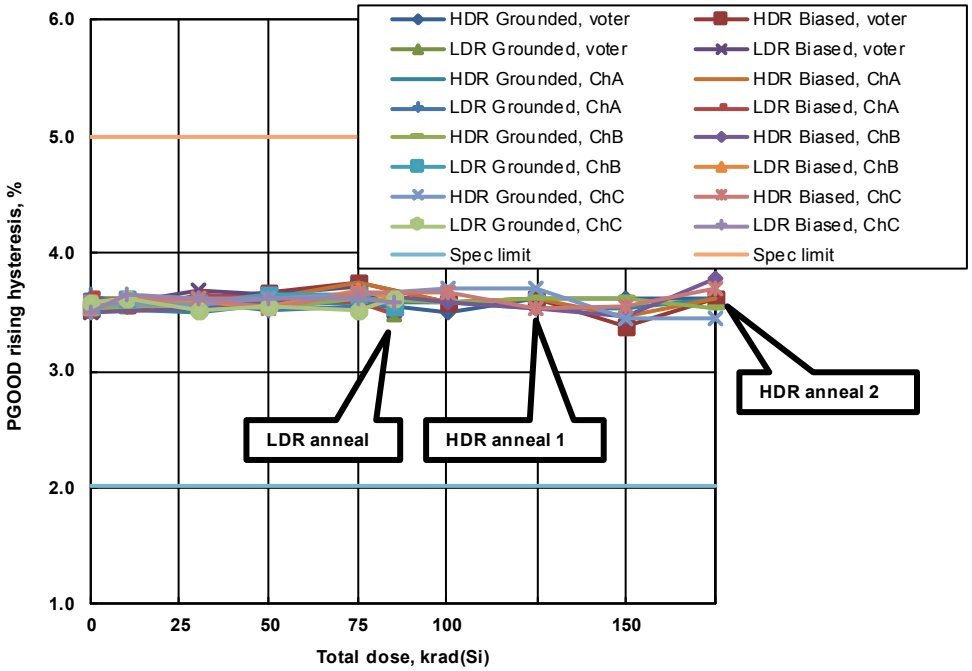


**FIGURE 22. ISL70003ASEH Power-Good (PGOOD) rising hysteresis as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limits are 2% to 5%.**

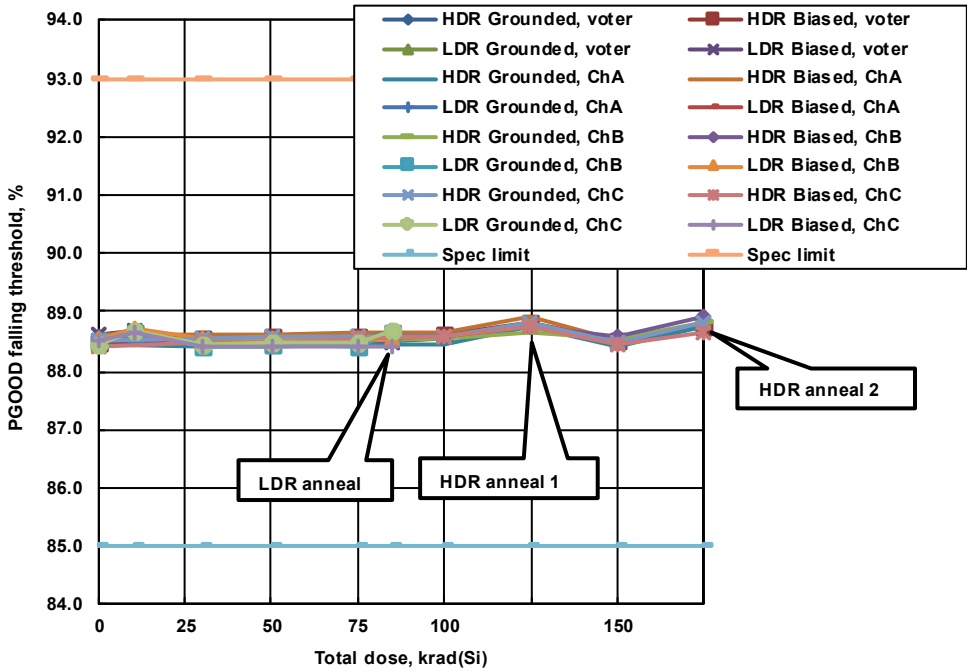


**FIGURE 23. ISL70003ASEH Power-Good (PGOOD) falling threshold as a function of total dose unbiased and biased cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limits are 85% to 93%.**

# Variables Data Plots (Continued)

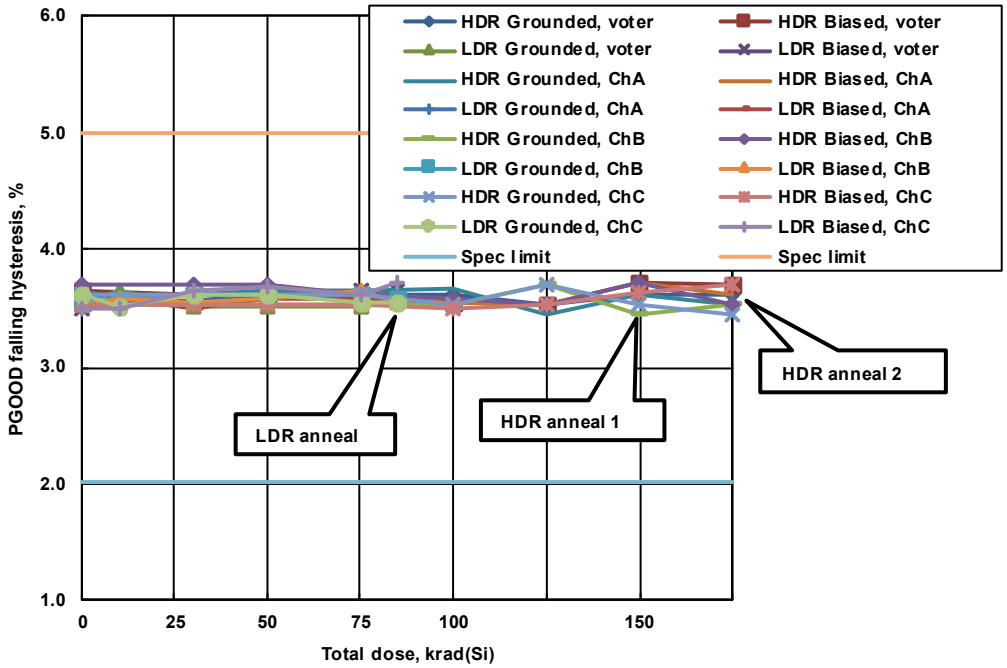


**FIGURE 24. ISL70003ASEH Power-Good (PGOOD) falling hysteresis as a function of total dose unbiased and biased cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limits are 2% to 5%.**

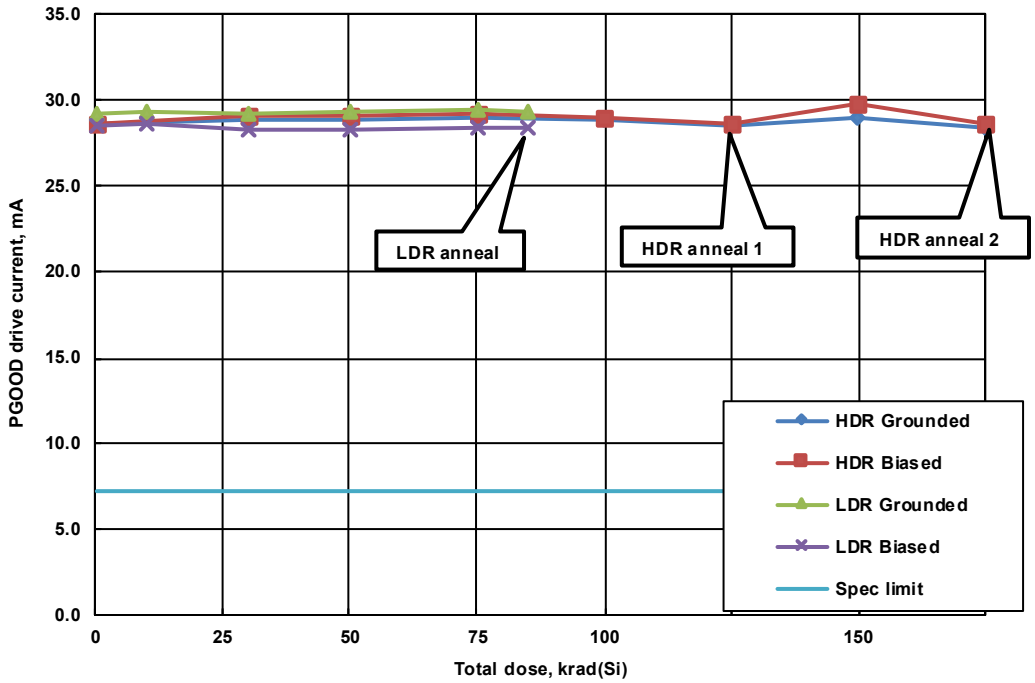


**FIGURE 25. ISL70003ASEH Power-Good (PGOOD) output drive current, 3V supply, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limit is 7.2mA minimum.**

## Variables Data Plots (Continued)

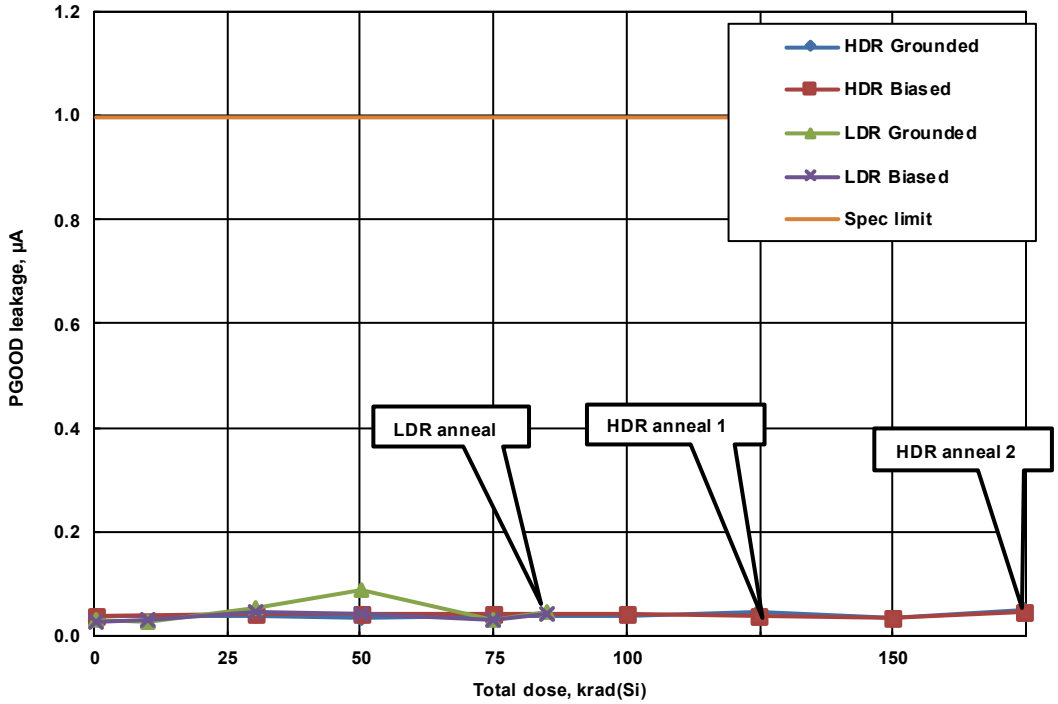


FIGURE 26. ISL70003ASEH Power-Good (PGOOD) output leakage, 3V supply, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limit is 1.0µA maximum.

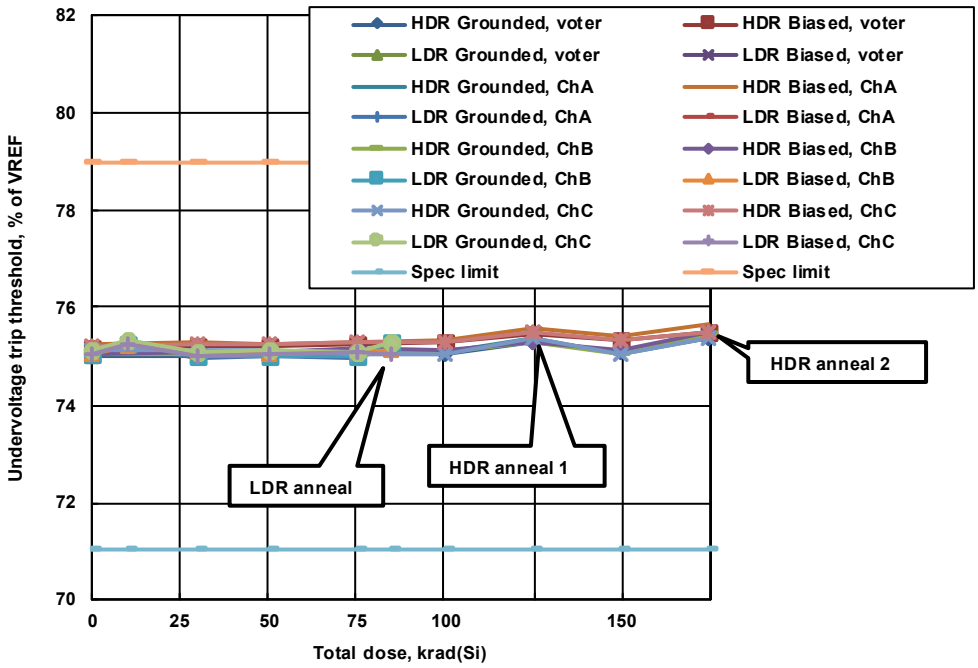


FIGURE 27. ISL70003ASEH undervoltage trip threshold as function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limits are 71% to 79%.

## Variables Data Plots (Continued)

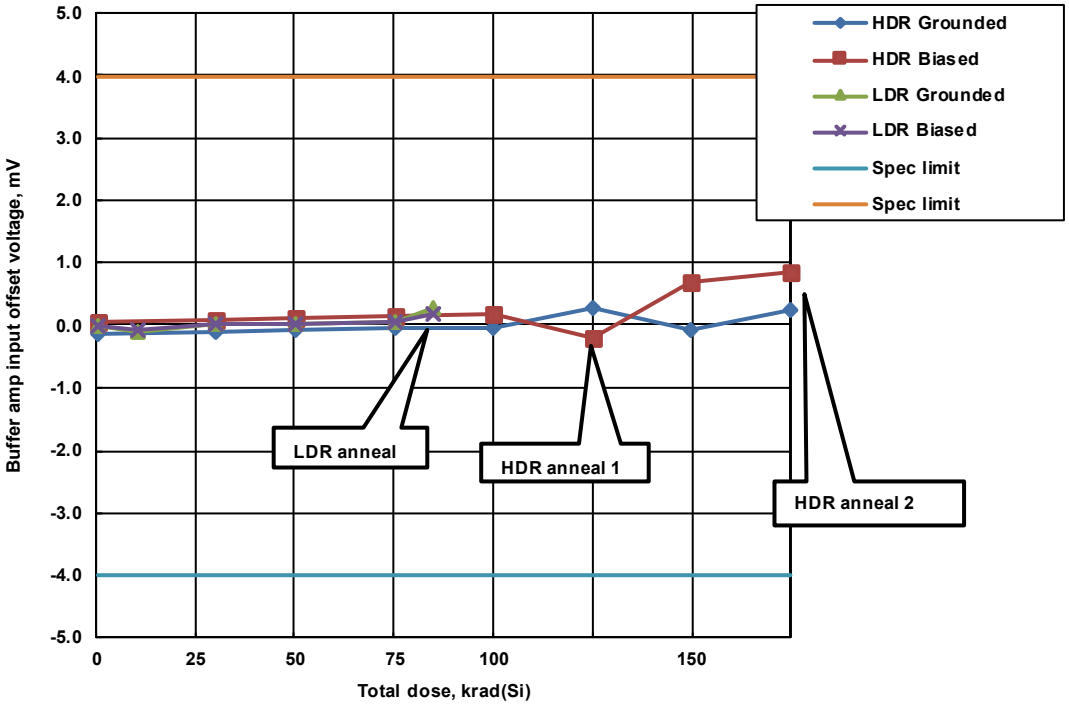


**FIGURE 28. ISL70003ASEH buffer amplifier input offset voltage as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The data sheet limits are -4.0mV to 4.0mV.**

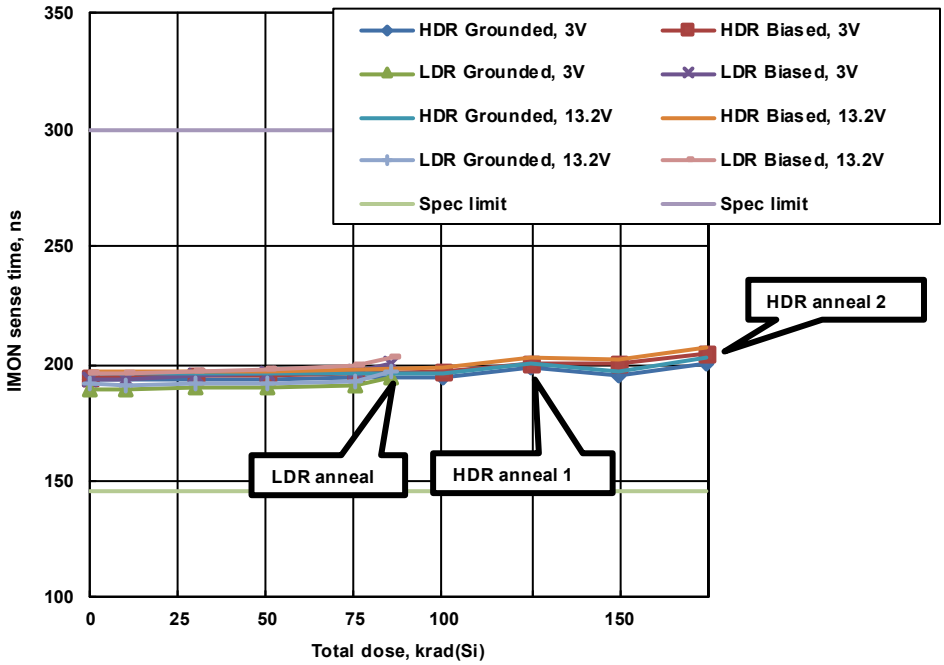


**FIGURE 29. ISL70003ASEH current monitor (IMON) sense time, for the 3V and 13.2V supply cases, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. The SMD limits are 145ns to 300ns.**

## Variables Data Plots (Continued)

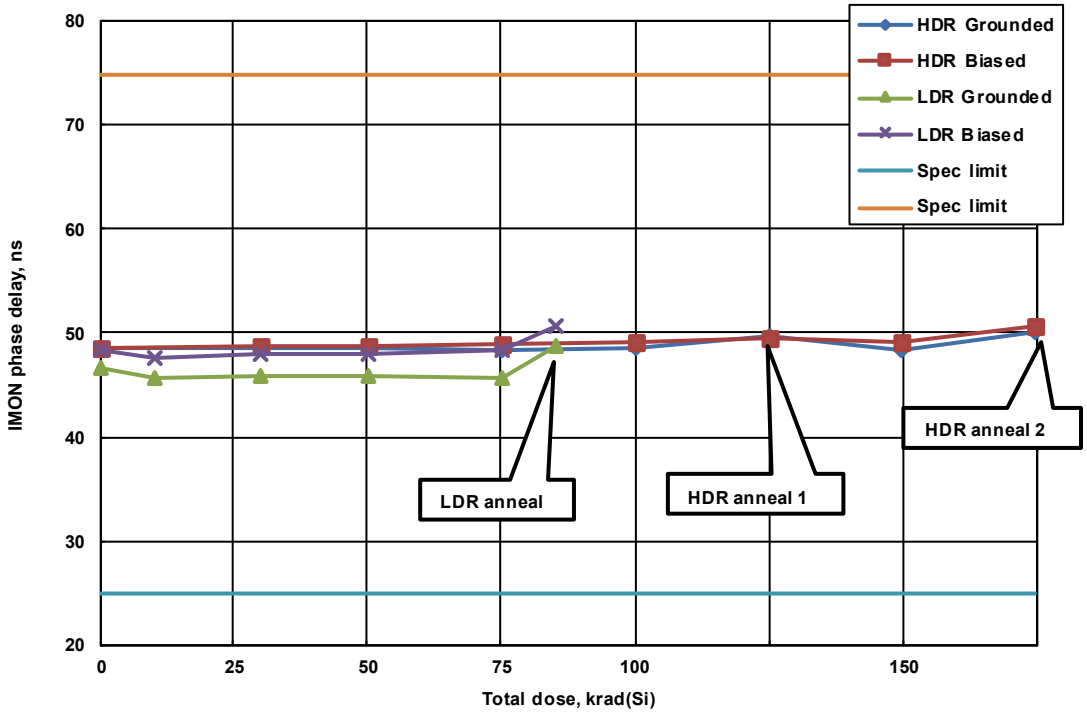


**FIGURE 30. ISL70003ASEH current monitor (IMON) phase delay time, 3V supply, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The low dose rate irradiations were followed by a high temperature anneal at 100°C for 168 hours. The high dose rate groups were split after 100krad(Si), with five samples undergoing anneal and the remaining five samples irradiated for a further 50krad(Si) followed by anneal. The low dose rate was 0.01rad(Si)/s and the high dose rate was 54rad(Si)/s. Sample sizes are given in "Experimental Matrix" on page 2. This is an informational parameter and is not formally specified; the ATE limits are 25ns to 75ns.**

## Discussion and Conclusion

This document reports the results of total dose testing of the ISL70003ASEH radiation tolerant Point-of-Load (POL) regulator. Parts were tested at low and high dose rate under biased and unbiased conditions, as outlined in MIL-STD-883 Test Method 1019, to a total dose of 150krad(Si) at high dose rate and to 75krad(Si) at low dose rate.

All parts showed excellent stability over irradiation and anneal, with no observed low dose rate sensitivity (or high dose rate sensitivity, for that matter). It should be noted that the SMD data tables contain no post-total dose limits; the pre- and post-irradiation limits are identical. This implies that the part has no dose rate sensitivity by definition, and this conclusion is confirmed by the data.

No differences between biased and unbiased irradiation were noted, and the part is not considered bias sensitive.

A detailed discussion of the response of the plotted parameters will be omitted as it is somewhat superfluous. A quick inspection of the figures will show that there was very little change.

## References

[1] 'Single Event Effects Testing of the ISL70003SEH, a 3V to 13.2V, 6A Synchronous Buck Regulator', Intersil application note AN1913, (March 2015).

# Appendix

## Reported Parameters

TABLE 2. REPORTED PARAMETERS

| REFERENCE | PARAMETER | LIMIT, LOW | LIMIT, HIGH | UNIT | NOTES |
|---|---|---|---|---|---|
| Figure 2 | Operating current, 500kHz | - | 60.0/125.0 | mA | 3V and 13.2$V_{IN}$ |
| Figure 3 | Operating current, 300kHz | - | 60.0/125.0 | mA | 3V and 13.2$V_{IN}$ |
| Figure 4 | Standby current, 500kHz | - | 15.0/30.0 | mA | 3V and 13.2$V_{IN}$ |
| Figure 5 | Standby current, 300kHz | - | 15.0/30.0 | mA | 3V and 13.2$V_{IN}$ |
| Figure 6 | Shutdown current, 500kHz | - | 1.0/3.0 | mA | 3V and 13.2$V_{IN}$ |
| Figure 7 | Reference voltage tolerance | 0.594 | 0.606 | V | 3V and 13.2$V_{IN}$ |
| Figure 8 | Series regulator output voltage | 4.5 | 5.5 | V | 13.2$V_{IN}$ |
| Figure 9 | Series regulator current limit | -50.0 | -190.0 | mA | 13.2$V_{IN}$ |
| Figure 10 | POR input pin voltage | 0.56 | 0.64 | V | 3V and 13.2$V_{IN}$ |
| Figure 11 | POR sink current | 9.6 | 14.4 | mA | 3V and 13.2$V_{IN}$ |
| Figure 12 | Enable LOW input current | -0.6 | 0.6 | µA | 13.2$V_{IN}$ |
| Figure 13 | Enable HIGH input current | - | 10.0 | µA | 13.2$V_{IN}$ |
| Figure 14 | Minimum ON time | - | 320.0 | ns | 3V and 13.2$V_{IN}$ |
| Figure 15 | Minimum OFF time | - | 270.0 | ns | 3V and 13.2$V_{IN}$ |
| Figure 16 | Error amplifier offset voltage | -3.0 | 3.0 | mV | 3V and 13.2$V_{IN}$ |
| Figure 17 | Upper device ON resistance | 90.0 | 455.0 | mΩ | 3V and 13.2$V_{IN}$ |
| Figure 18 | Lower device ON resistance | 170.0 | 700.0 | mΩ | 3V and 13.2$V_{IN}$ |
| Figure 19 | LXx LOW leakage current | - | 3.0 | µA | 3$V_{IN}$ |
| Figure 20 | LXx HIGH leakage current | - | 3.0 | µA | 3$V_{IN}$ |
| Figure 21 | PGOOD rising threshold | 107.0 | 115.0 | % | 3$V_{IN}$ |
| Figure 22 | PGOOD rising hysteresis | 2.0 | 5.0 | % | 3$V_{IN}$ |
| Figure 23 | PGOOD falling threshold | 85.0 | 93.0 | % | 3$V_{IN}$ |
| Figure 24 | PGOOD falling hysteresis | 2.0 | 5.0 | % | 3$V_{IN}$ |
| Figure 25 | PGOOD output drive current | 7.2 | - | mA | 3$V_{IN}$ |
| Figure 26 | PGOOD output leakage | - | 1.0 | µA | 3$V_{IN}$ |
| Figure 27 | Undervoltage trip threshold | 71.0 | 79.0 | % | 3$V_{IN}$ |
| Figure 28 | Buffer amplifier offset voltage | -4.0 | 4.0 | mV | 3$V_{IN}$ |
| Figure 29 | Current monitor sense time | 145.0 | 300.0 | ns | 3V and 13.2$V_{IN}$ |
| Figure 30 | Current monitor phase delay | 25.0 | 75.0 | ns | |

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