HS-508BEH, HS-508BRH

Neutron Testing of the HS-508BEH 8-Channel Analog Multiplexer

Introduction

This report summarizes the 1MeV equivalent neutron testing results of the HS-508BEH, HS-508BRH, an 8-channel analog multiplexer. The test was conducted to determine the sensitivity of the part to displacement damage (DD) caused by neutron or proton environments. Neutron fluences ranged from 5×10^{11}n/cm^2 to 1×10^{13}n/cm^2.

Product Description

The HS-508BEH and HS-508BRH are dielectrically isolated, radiation hardened, CMOS analog multiplexers incorporating an important feature; they withstand analog input voltages much greater than the supplies. This feature is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10V greater than either supply, eliminating the possibility of damage when supplies are off, but input signals are present. Equally important, they can withstand brief input transient spikes of several hundred volts, which otherwise would require complex external protection networks. Necessarily, ON-resistance is somewhat higher than similar unprotected devices, but a low leakage current combines to produce low errors.

The HS-508BRH and HS-508BEH have been specifically designed to meet exposure to radiation environments. Operation from -55°C to +125°C is guaranteed.

The HS-508BRH and HS-508BEH functional block diagram is shown in Figure 1.

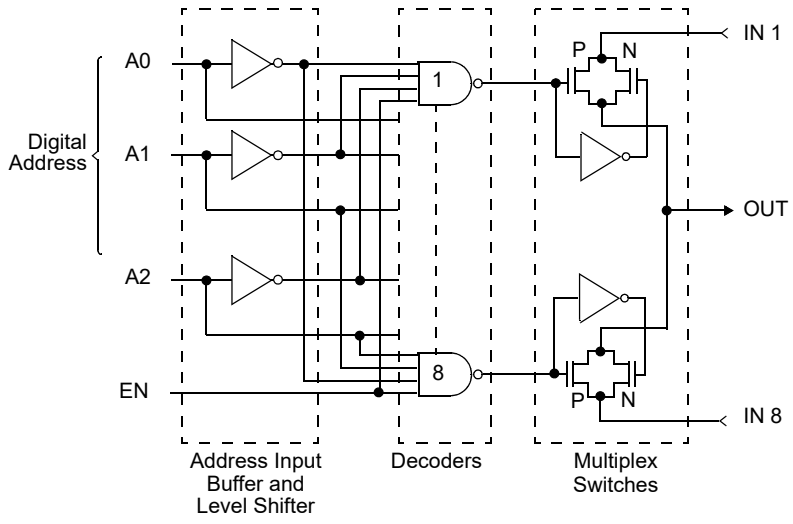

Figure 1. HS-508BEH, HS-508BRH Function Block Diagram

Contents

1. Test Description

1.1 Irradiation Facility

Neutron fluence irradiations were performed on the test samples on March 29, 2023, at the University of Massachusetts, Lowell (UMASS Lowell) fast neutron irradiator per Mil-STD-883G, Method 1017.2, with each part unpowered during irradiation. The target irradiation levels were 5×10^{11}n/cm^2, 2×10^{12}n/cm^2, and 1×10^{13}n/cm^2. As neutron irradiation activates many of the heavier elements found in a packaged integrated circuit, the parts exposed at the higher neutron levels required (as expected) some cooldown time before being shipped back to Renesas (Palm Bay, FL) for electrical testing.

1.2 Test Fixturing

No formal irradiation test fixturing is involved, as these DD tests are bag tests in the sense that the parts are irradiated with all leads unbiased.

1.3 Radiation Dosimetry

Table 1 shows dosimetry from UMASS Lowell indicating the total accumulated gamma dose and actual neutron fluence exposure levels for each set of samples.

Table 1. Neutron Fluence Dosimetry Data

Irradiation	Requested Fluence (n/cm^2)	Reactor Power (kW)	Time (s)	Fluence Rate (n/cm^2-s)[1][2]	Gamma Dose (rad(Si))[3]	Measured Fluence (n/cm^2)[4]
CRF#77981-B	5.00E+11	50	131	3.83E+09	75	5.30E+11
CRF#77981-C	2.00E+12	80	327	6.12E+09	298	2.33E+12
CRF#77981-D	1.00E+13	1000	131	7.65E+10	1492	1.04E+13

1. Dosimetry method: ASTM E-265.
2. The neutron fluence rate is determined from *Initial Testing of the New Ex-Core Fast Neutron Irradiator at UMass Lowell (6/18/02)*. Validated on 6/07/2011 under the Trident II D5LE neutron facility study by Navy Crane.
3. Based on reactor power at 1000kW, the gamma dose is 41krad(Si)/hr ±5.3% as mapped by TLD-based dosimetry.
4. Validated by S-32 flux monitors.

1.4 Characterization Equipment and Procedures

Electrical testing was performed before and after irradiation using the Renesas production automated test equipment (ATE). All electrical testing was performed at room temperature.

1.5 Experimental Matrix

Testing proceeded in general accordance with the guidelines of MIL-STD-883 TM 1017. The experimental matrix consisted of six samples to be irradiated at 5×10^{11}n/cm^2, six at 2×10^{12}n/cm^2, and six at 1×10^{13}n/cm^2. The actual levels achieved were 5.30×10^{11}n/cm^2, 2.33×10^{12}n/cm^2, and 1.04×10^{13}n/cm^2, as shown in Table 2. Two control units were used.

The 20 HS-508BEH samples were drawn from Lot DTC4ECD. Samples were packaged in the 16-lead hermetically sealed Ceramic Dual Flat-Pack (CDFP) production package. Samples were processed through burn-in before irradiation and screened to the SMD limits at room, low, and high temperatures before the neutron testing.

2. Results

Neutron testing of the HS-508BEH is complete, and the results are reported in the balance of this report. It should be understood when interpreting the data that each neutron irradiation was performed on a different set of samples; this is not total dose testing, where the damage is cumulative.

2.1 Attributes Data

Table 2. Attributes Data

1MeV Fluence, (n/cm^2)		Sample Size	Pass[1]	Fail	Notes
Planned	Actual				
5×10^{11}	5.30×10^{11}	6	6	0	All passed
2×10^{12}	2.33×10^{12}	6	6	0	All passed
1×10^{13}	1.04×10^{13}	6	6	0	All passed

1. A pass indicates a sample that passes all SMD limits.

2.2 Variables Data

The plots in Figure 2 through Figure 18 show data plots for key parameters before and after irradiation to each level. The plots show the mean of each parameter as a function of neutron irradiation. The plots also include error bars at each down-point, representing the minimum and maximum measured values of the samples. However, in some plots, the error bars might not be visible because of their values compared to the scale of the graph. The applicable electrical limits taken from the SMD are also shown.

Some graphs and captions state that they are the average; this denotes that the average of the measurements of multiple channels or pins was plotted. The error bars on these graphs represent the maximum and minimum measured values across all the channels or pins. All samples passed the post-TID irradiation SMD limits after all three exposures up to and including 1.04×10^{13}n/cm^2.

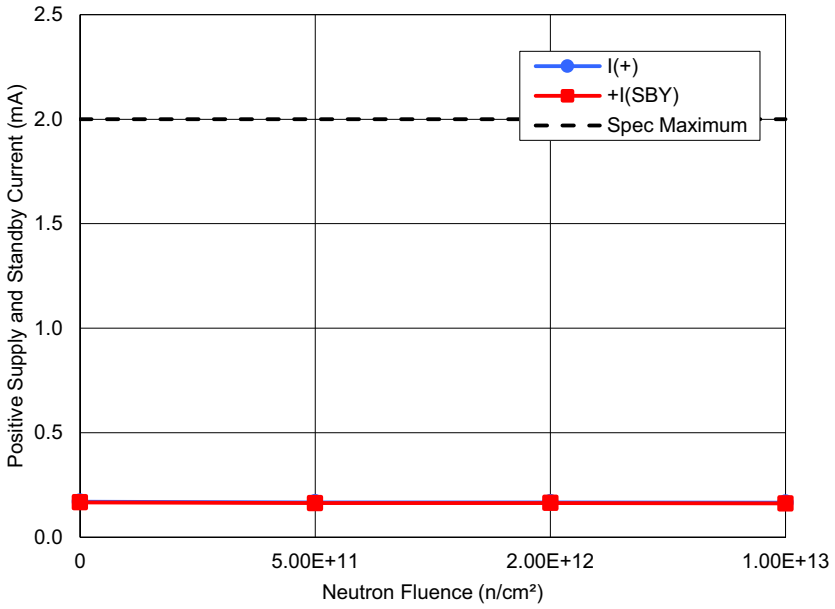

Figure 2. HS-508BEH positive supply current ($I_{(+)}$) and standby current ($+I_{(SBY)}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a maximum of 2mA.

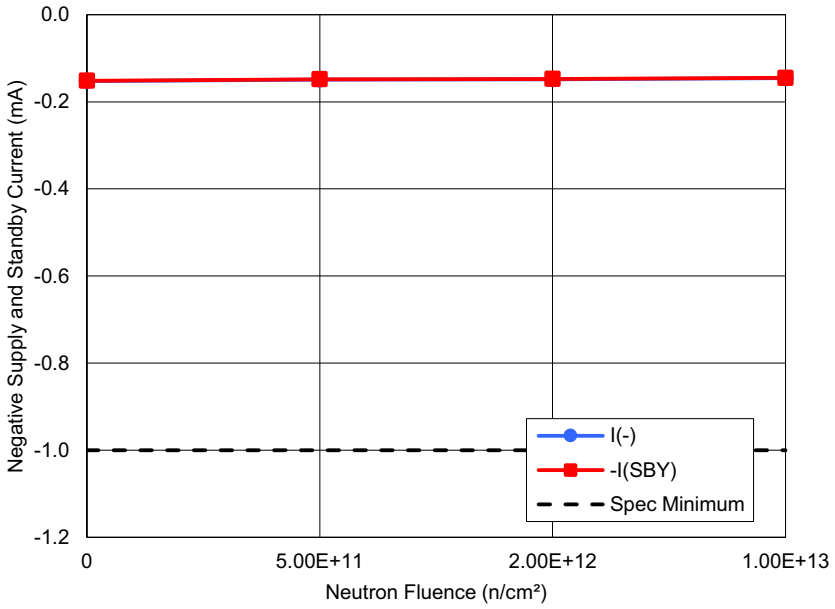

Figure 3. HS-508BEH negative supply current ($I_{(-)}$) and standby current ($-I_{(SBY)}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a minimum of -1mA.

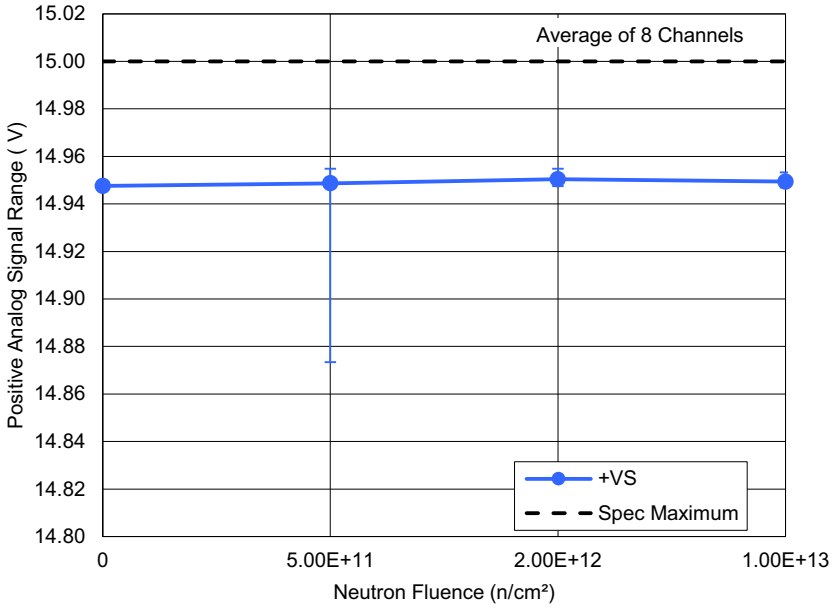

Figure 4. HS-508BEH average positive analog signal range ($+V_S$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post-TID irradiation SMD limit is a maximum of 15V.

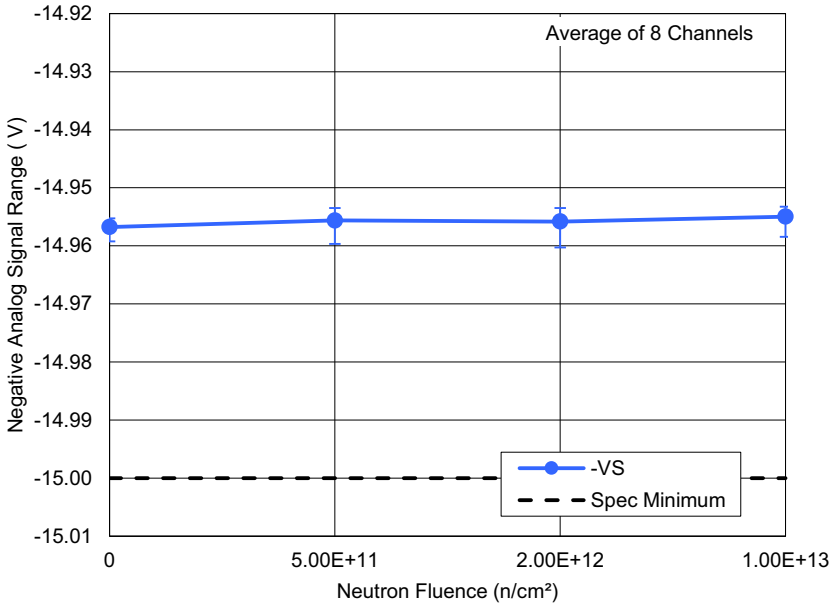

Figure 5. HS-508BEH average negative analog signal range ($-V_S$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post-TID irradiation SMD limit is a maximum of -15V.

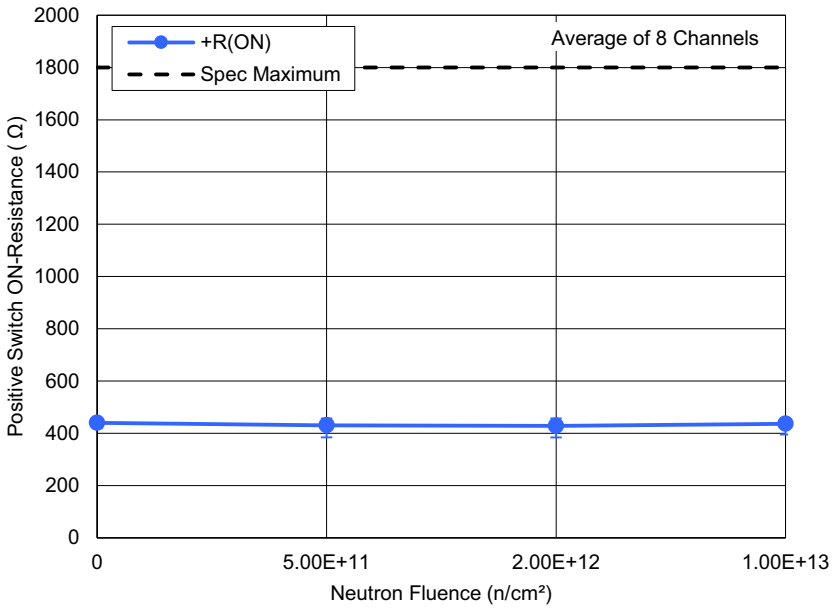

Figure 6. HS-508BEH average positive ON-resistance ($+R_{(ON)}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post-TID irradiation SMD limit is a maximum of 1800Ω.

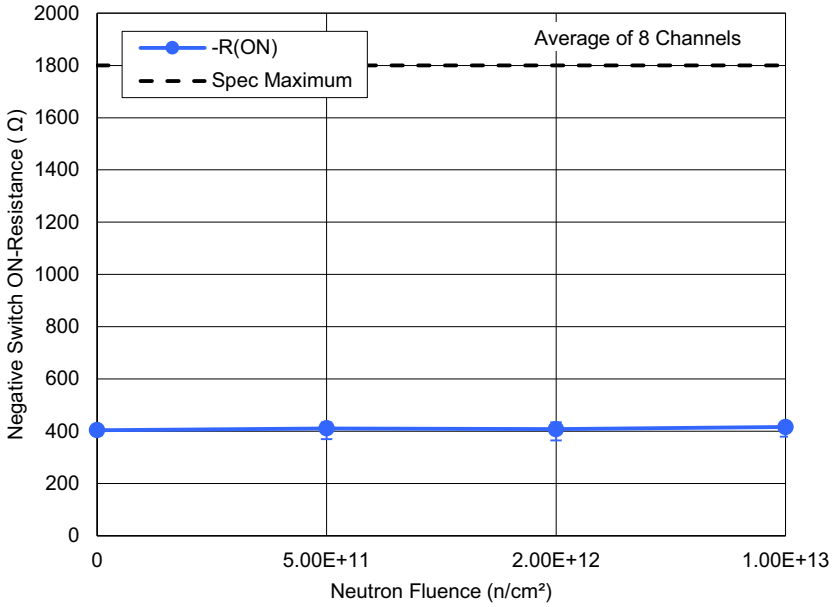

Figure 7. HS-508BEH average negative ON-resistance (-$R_{(ON)}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post-TID irradiation SMD limit is a maximum of 1800Ω.

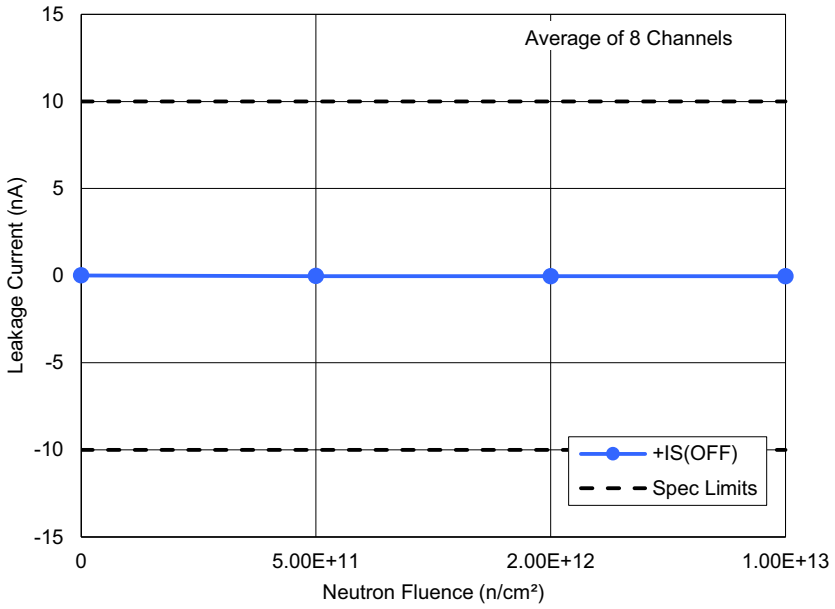

Figure 8. HS-508BEH average positive OFF-source leakage (+$I_{S(OFF)}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post-TID irradiation SMD limits are a minimum of -10nA and a maximum of 10nA.

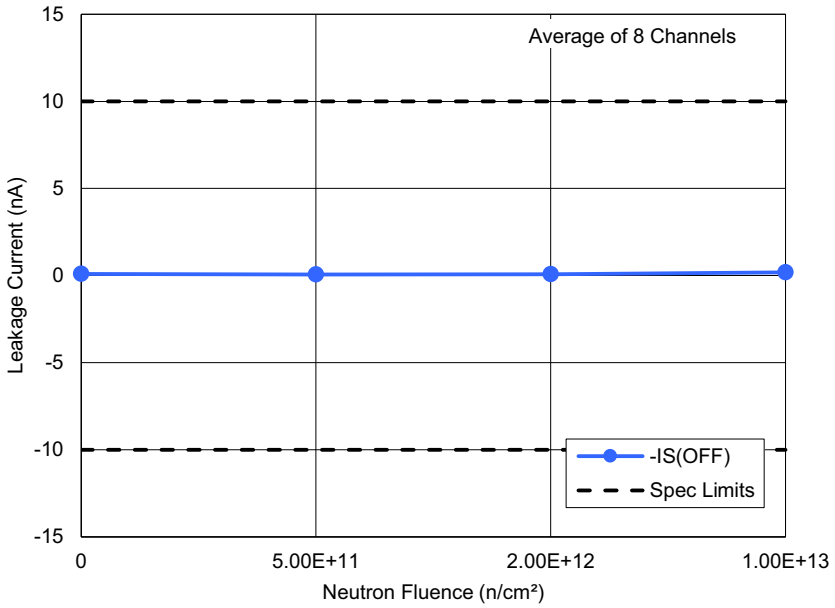

Figure 9. HS-508BEH average negative OFF-source leakage ($-I_{S(OFF)}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post-TID irradiation SMD limits are a minimum of -10nA and a maximum of 10nA.

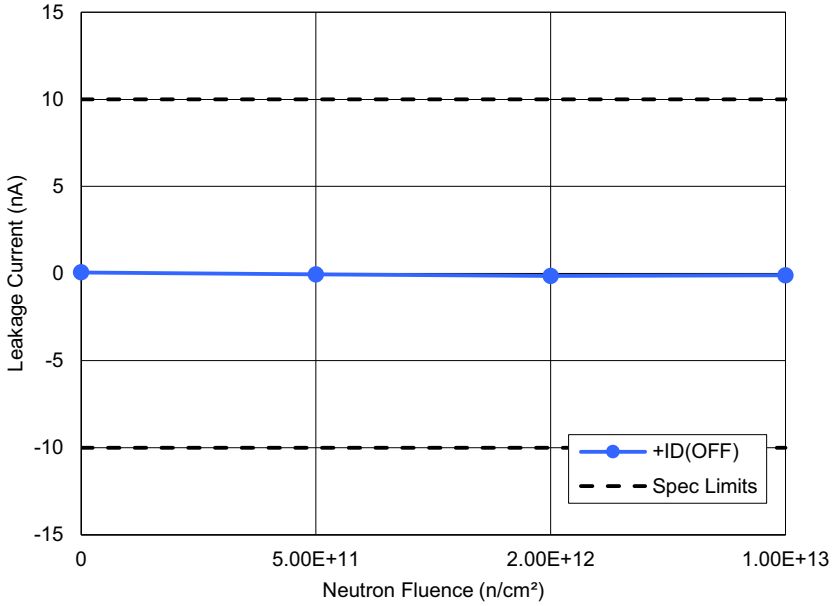

Figure 10. HS-508BEH positive OFF-drain leakage ($+I_{D(OFF)}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of -10nA and a maximum of 10nA.

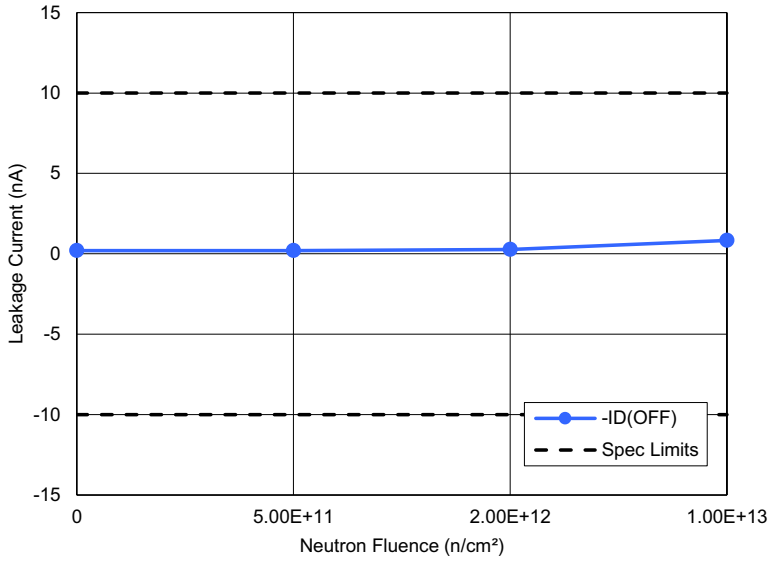

Figure 11. HS-508BEH negative OFF-drain leakage ($-I_{D(OFF)}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of -10nA and a maximum of 10nA.

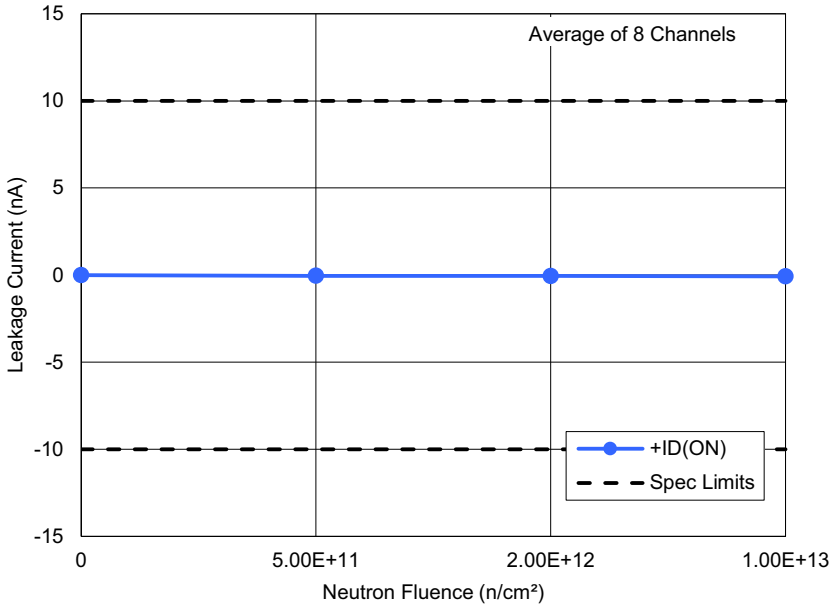

Figure 12. HS-508BEH average positive ON-drain leakage ($+I_{D(ON)}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post-TID irradiation SMD limits are a minimum of -10nA and a maximum of 10nA.

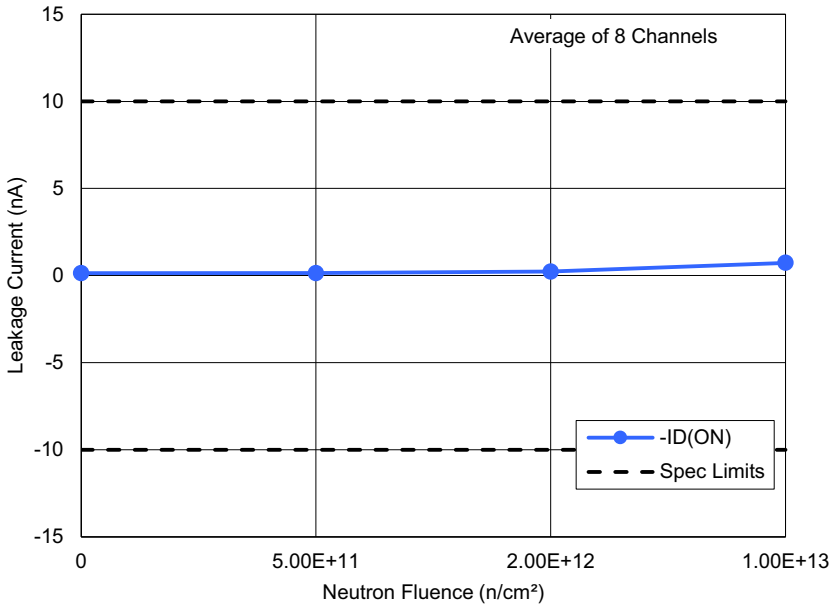

Figure 13. HS-508BEH average negative ON-drain leakage ($-I_{D(ON)}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post-TID irradiation SMD limits are a minimum of -10nA and a maximum of 10nA.

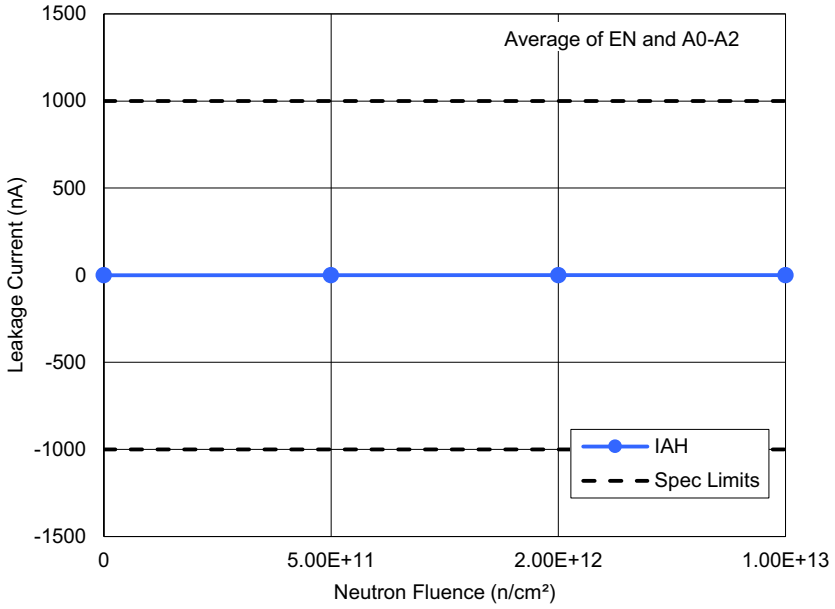

Figure 14. HS-508BEH average input HIGH leakage current, enable and address pins, (I_{AH}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all pins. The post-TID irradiation SMD limits are a minimum of -1000nA and a maximum of 1000nA.

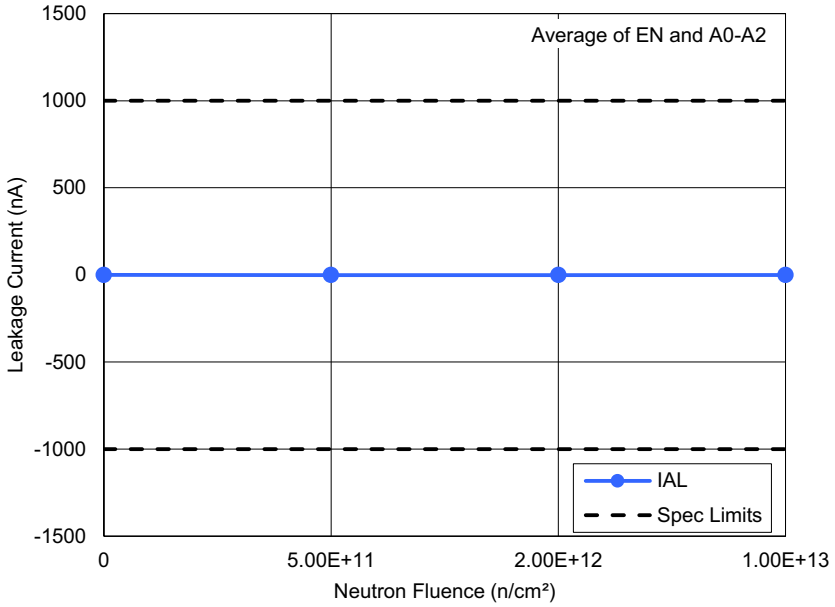

Figure 15. HS-508BEH average input LOW leakage current, enable and address pins, (I_{AL}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all pins. The post-TID irradiation SMD limits are a minimum of -1000nA and a maximum of 1000nA.

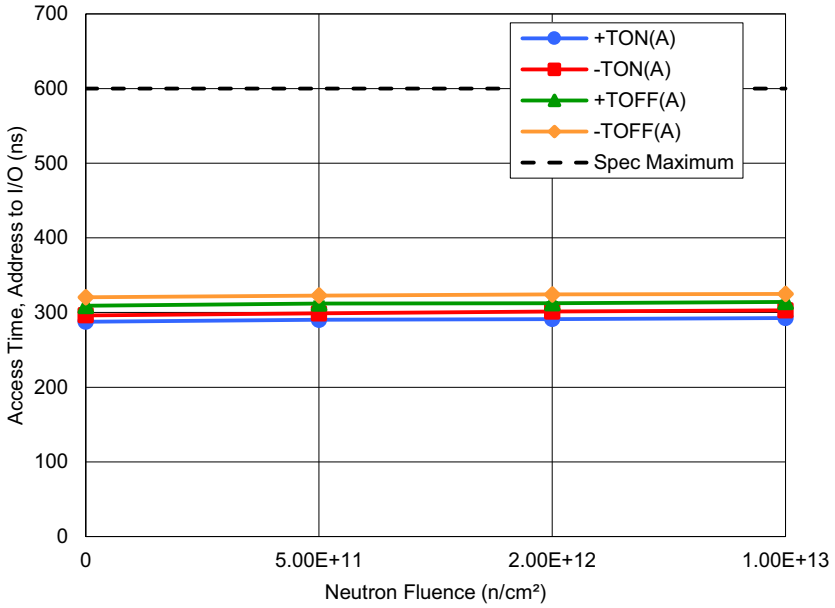

Figure 16. HS-508BEH address to switch access time ($T_{ON(A)}$, $T_{OFF(A)}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a maximum of 600ns.

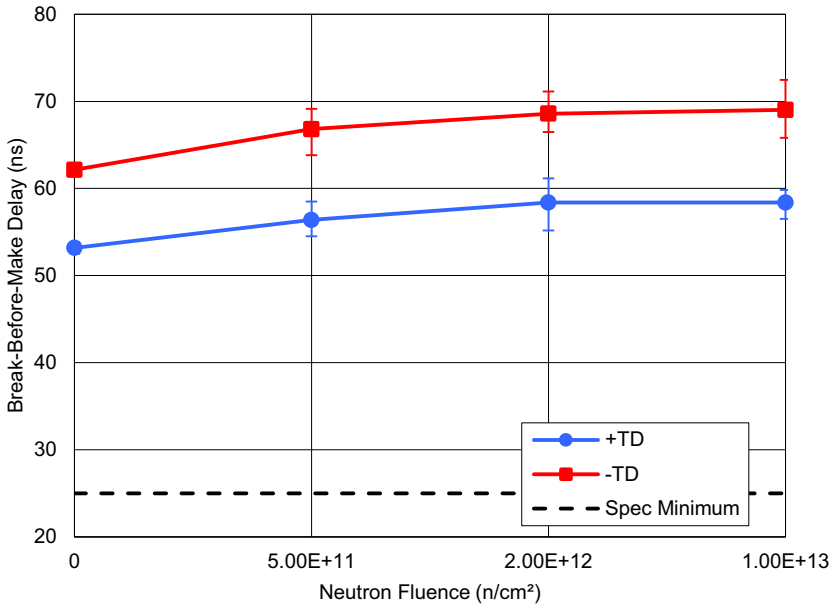

Figure 17. HS-508BEH break-before-make delay (T_D) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a minimum of 25ns.

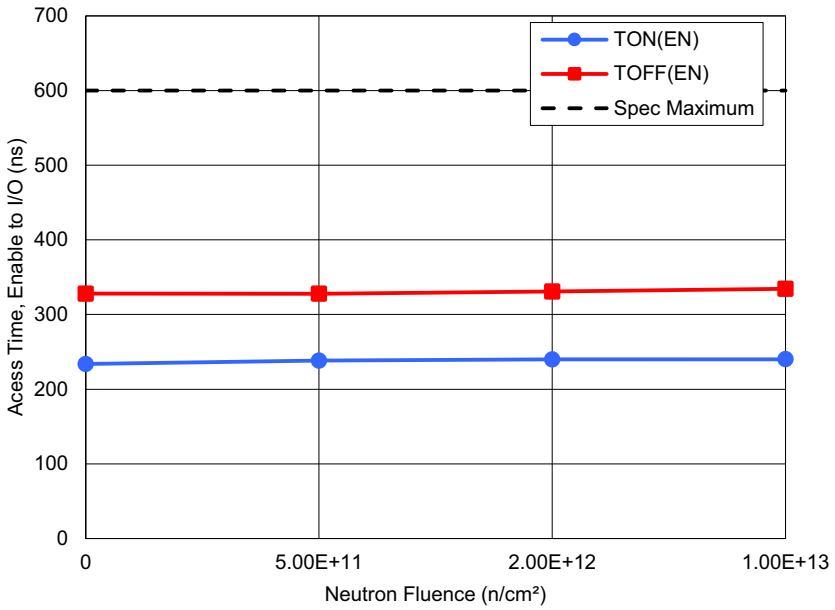

Figure 18. HS-508BEH enable to switch access time ($T_{ON(EN)}$, $T_{OFF(EN)}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a maximum of 600ns.

3. Discussion and Conclusion

This document reports the 1MeV equivalent neutron testing results of the HS-508BEH, the 8-channel analog multiplexer. Parts were tested at actual fluences of 5.30×10^{11}n/cm^2, 2.33×10^{12}n/cm^2, and 1.04×10^{13}n/cm^2. The results of key parameters before and after irradiation to each level are plotted in Figure 2 through Figure 18. The plots show the mean of each parameter as a function of neutron irradiation, with error bars representing the minimum and maximum measured values. The figures also show the applicable electrical limits taken from the SMD.

All samples passed the post-TID irradiation SMD limits after all three exposures up to and including 1.04×10^{13}n/cm^2.

4. Revision History

Revision	Date	Description
1.01	Jun 6, 2025	Minor update to the Variables Data and Discussion and Conclusion sections.
1.00	Jul 3, 2023	Initial release.

A. Appendix

A.1 Reported Parameters

Figure	Parameter	Symbol	Conditions	Low Limit	High Limit	Unit
2	Positive Supply Current	$I_{(+)}$	V_{EN} = 4V	-	2	mA
	Positive Standby Supply Current	$+I_{(SBY)}$	V_{EN} = 0.8V			
3	Negative Supply Current	$I_{(-)}$	V_{EN} = 4V	-1	-	mA
	Negative Standby Supply Current	$-I_{(SBY)}$	V_{EN} = 0.8V			
4	Positive Analog Signal Range	$+V_S$		-	15	V
5	Negative Analog Signal Range	$-V_S$		-	-15	V
6	Positive ON-Resistance	$+R_{(ON)}$	V_S = +10V, V_{EN} = 4V, I_{OUT} = -100µA	-	1800	Ω
7	Negative ON-Resistance	$-R_{(ON)}$	V_S = -10V, V_{EN} = 4V, I_{OUT} = +100µA	-	1800	Ω
8	Positive OFF Source Leakage	$+I_{S(OFF)}$	V_S = +10V, all unused input and outputs = -10V, V_{EN} = 0.8V	-10	10	nA
9	Negative OFF Source Leakage	$-I_{S(OFF)}$	V_S = -10V, all unused input and outputs = +10V, V_{EN} = 0.8V	-10	10	nA
10	Positive OFF Drain Leakage	$+I_{D(OFF)}$	V_D = +10V, all unused input and outputs = -10V, V_{EN} = 0.8V	-10	10	nA
11	Negative OFF Drain Leakage	$-I_{D(OFF)}$	V_D = -10V, all unused input and outputs = +10V, V_{EN} = 0.8V	-10	10	nA
12	Positive ON Drain Leakage	$+I_{D(ON)}$	V_S = V_D = +10V, V_{EN} = 4V, all unused inputs = -10V	-10	10	nA
13	Negative ON Drain Leakage	$-I_{D(ON)}$	V_S = V_D = -10V, V_{EN} = 4V, all unused inputs = +10V	-10	10	nA
14	Input HIGH Leakage Current	I_{AH}	Enable and Address pins	-1000	1000	nA
15	Input LOW Leakage Current	I_{AL}	Enable and Address pins	-1000	1000	nA
16	Address to Switch Access Time	$T_{ON(A)}$ / $T_{OFF(A)}$	R_L = 10kΩ, C_L = 50pF	-	600	ns
17	Break-Before-Make Delay	T_D	R_L = 1000Ω, C_L = 50pF	25	-	ns
18	Enable to Switch Access Time	$T_{ON(EN)}$ / $T_{OFF(EN)}$	R_L = 1000Ω, C_L = 50pF	-	600	ns

A.2 Related Information

For a full list of related documents, visit our website:

- HS-508BEH, HS-508BRH device page
- MIL-STD-883 test method 1017

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