

IS-2100ARH

Neutron Testing of the HS-2100RH Radiation Hardened High Frequency Half Bridge Driver

Introduction

This report summarizes results of 1MeV equivalent neutron testing of the [IS-2100ARH](#) High Frequency Half Bridge Driver. The test was conducted to determine the sensitivity of the part to Displacement Damage (DD) caused by neutron or proton environments. Neutron fluences ranged from $7.3 \times 10^{11} \text{n/cm}^2$ to $3.2 \times 10^{13} \text{n/cm}^2$. This project was carried out in collaboration with Honeywell Aerospace Corporation and their support is gratefully acknowledged.

Product Description

The radiation hardened IS-2100ARH is a high frequency, 100V half bridge N-Channel MOSFET driver, which is a functional, pin-to-pin replacement for the Renesas HIP2500 and the industry standard 2110 types. The low-side and high-side gate drivers are independently controlled. This gives the user maximum flexibility in dead time selection and driver protocol.

The device also has on-chip error detection and correction circuitry, which monitors the state of the high-side latch and compares it to the H_{IN} signal. If the states do not match, a set or reset pulse is generated to correct the high-side latch. This feature protects the high-side latch from Single Event Upsets (SEUs).

Undervoltage on the high-side supply forces HO low. When that supply returns to a valid voltage, HO goes to the state of H_{IN} . Undervoltage on the low-side supply forces both LO and HO low. When that supply becomes valid, LO returns to the L_{IN} state and HO returns to the H_{IN} state.

These devices are constructed with the Renesas dielectrically isolated Rad Hard Silicon Gate (RSG) BiCMOS process. They are immune to single event latch-up and have been specifically designed to provide highly reliable performance in harsh radiation environments.

Specifications for radiation hardened QML devices are controlled by the Defense Logistics Agency (DLA) in Columbus, OH. The SMD is the controlling document and must be cited when ordering.

Related Literature

For a full list of related documents, visit our website

- [IS-2100ARH](#) product page
- MIL-STD-883 test method 1017

Content

1. Test Description	2
1.1 Irradiation Facility	2
1.2 Test Fixturing	2
1.3 Characterization Equipment and Procedures	2
1.4 Experimental Matrix	2
2. Results	2
2.1 Attributes Data	2
2.2 Variables Data	3
2.3 Variables Data Plots	3
3. Discussion and Conclusion	12
3.1 Reported Parameters	12
4. Revision History	12

1. Test Description

1.1 Irradiation Facility

Neutron fluence irradiations were performed on the test samples on July 8, 2015, at the WSMR Fast Burst Reactor (FBR) per MIL-STD-883G, Method 1017.2, with each part unpowered during irradiation and all leads shorted. Because neutron irradiation activates many of the heavier elements found in a packaged integrated circuit, the parts exposed at the higher neutron levels required (as expected) some cool-down time before being shipped back to Renesas (Palm Bay, FL) for electrical testing.

1.2 Test Fixturing

No formal irradiation test fixturing is involved. These DD tests are bag tests, meaning that the parts are irradiated with all leads shorted together.

1.3 Characterization Equipment and Procedures

Electrical testing was performed before and after irradiation using Renesas production Automated Test Equipment (ATE). All electrical testing was performed at room temperature.

1.4 Experimental Matrix

Testing proceeded in general accordance with the guidelines of MIL-STD-883 TM 1017. The experimental matrix consisted of five samples irradiated at $7.3 \times 10^{11} \text{ n/cm}^2$, five samples irradiated at $1.8 \times 10^{12} \text{ n/cm}^2$, five samples irradiated at $1.2 \times 10^{13} \text{ n/cm}^2$, and five samples irradiated at $3.2 \times 10^{13} \text{ n/cm}^2$. Five control units were used.

IS-2100ARH samples were drawn from Lot G2X8LDA. Samples were packaged in the standard hermetic 16 lead ceramic flatpack production package, code CDFP4-F16. Samples were processed through burnin before irradiation and were screened to the SMD limits at room, low, and high temperatures before the start of neutron testing.

2. Results

The following section list the IS-2100ARH neutron testing results. Each neutron irradiation was performed on a different set of samples; this is *not* total dose testing, in which the damage is cumulative.

2.1 Attributes Data

Table 1. Attributes Data

Fluence, (n/cm ²)	Sample Size	Pass ^[1]	Fail
7.3×10^{11}	10	10	0
1.8×10^{12}	5	5	0
1.2×10^{13}	5	5	0
3.2×10^{13}	5	5	0

1. A Pass indicates a sample that passes all SMD limits.

2.2 Variables Data

The plots in Figure 1 through Figure 17 show data plots for key parameters before and after irradiation to each level. The plots show the mean of each parameter as a function of neutron irradiation. The plots also include error bars at each datapoint, representing the minimum and maximum measured values of the samples, although the error bars might not be visible in some plots due to their values compared to the scale of the graph. The applicable electrical limits taken from the SMD are also shown.

All samples passed the post-irradiation SMD limits after all exposures up to and including $3.2 \times 10^{13} \text{ n/cm}^2$.

2.3 Variables Data Plots

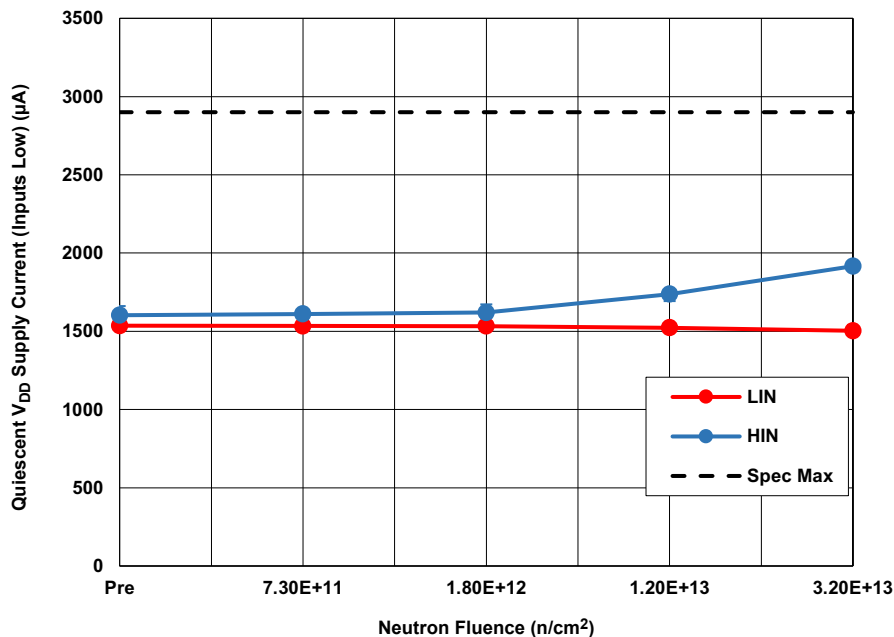


Figure 1. IS-2100ARH quiescent V_{DD} supply current (I_{QDD}) with inputs low (L_{IN} and H_{IN}) following neutron irradiation to each level. The error bars represent the minimum and maximum measured values. The SMD limit is 2900 μA maximum.

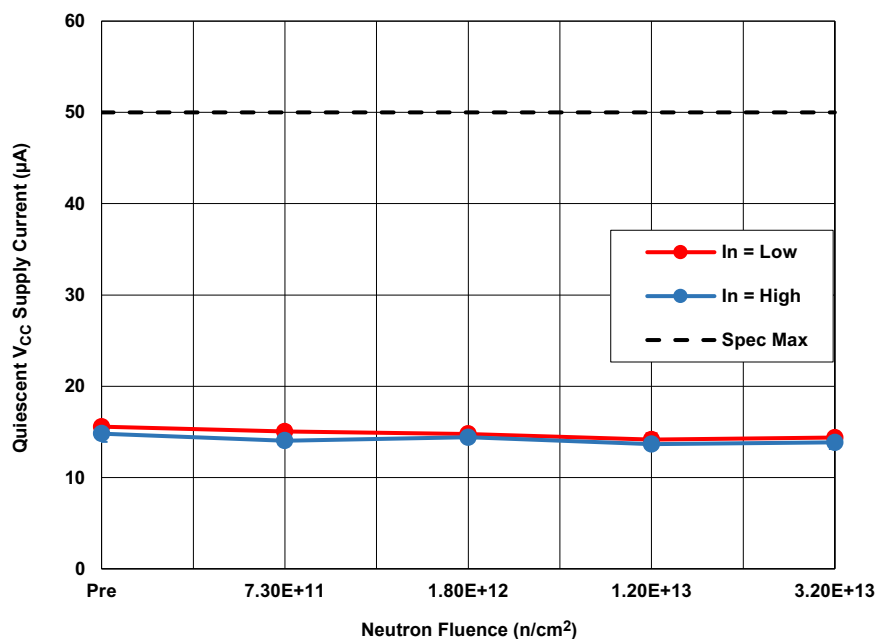


Figure 2. IS-2100ARH quiescent V_{CC} supply current (I_{QCC}) with inputs low or high following neutron irradiation to each level. The error bars represent the minimum and maximum measured values. The SMD limit is 50µA maximum.

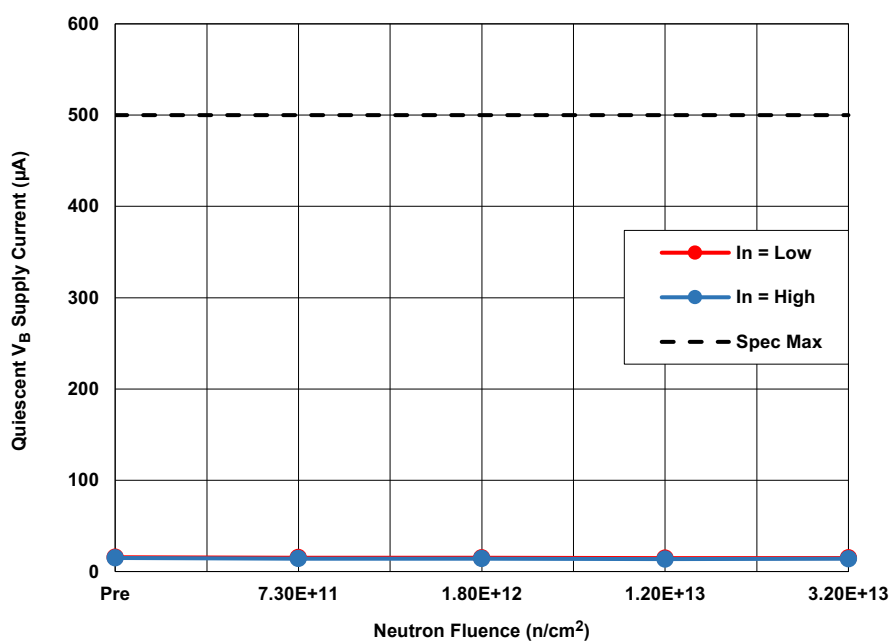


Figure 3. IS-2100ARH quiescent V_B supply current (I_{QB}) with inputs low or high following neutron irradiation to each level. The error bars represent the minimum and maximum measured values. The SMD limit is 500µA maximum.

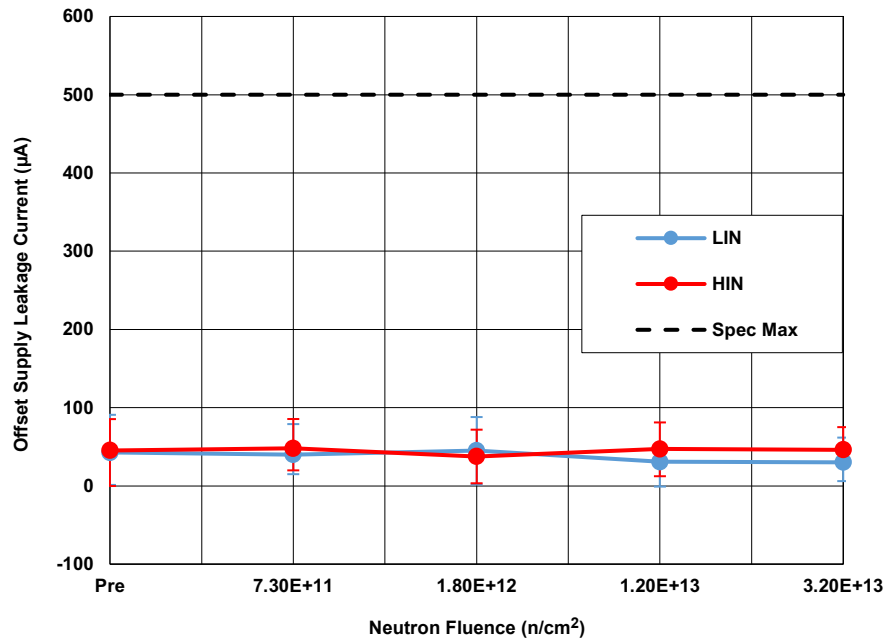


Figure 4. IS-2100ARH offset supply leakage current (I_{LK}) following neutron irradiation to each level. The error bars represent the minimum and maximum measured values. The SMD limit is 500µA maximum.

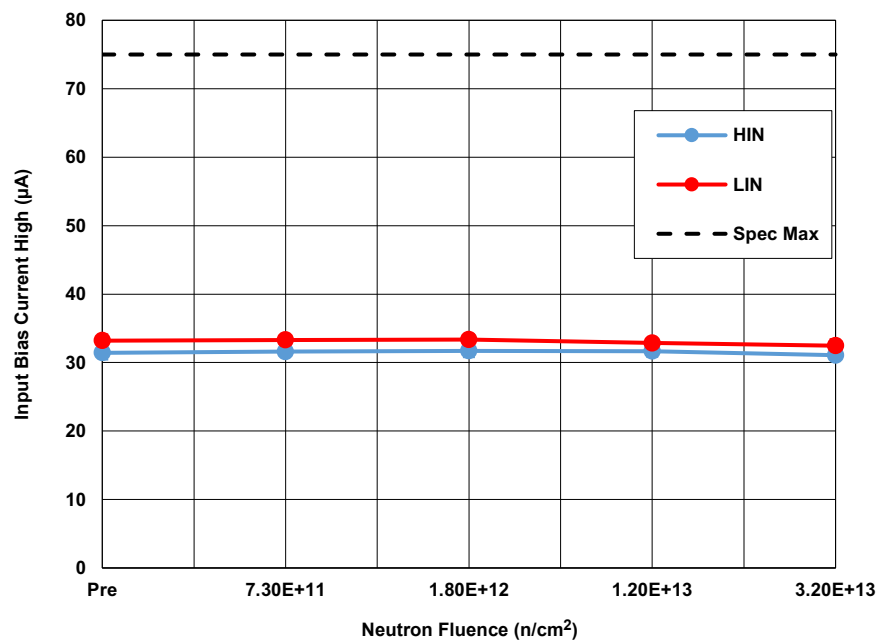


Figure 5. IS-2100ARH logic "1" input bias current ($+I_{IN}$) following neutron irradiation to each level. The error bars represent the minimum and maximum measured values. The SMD limit is 75µA maximum.

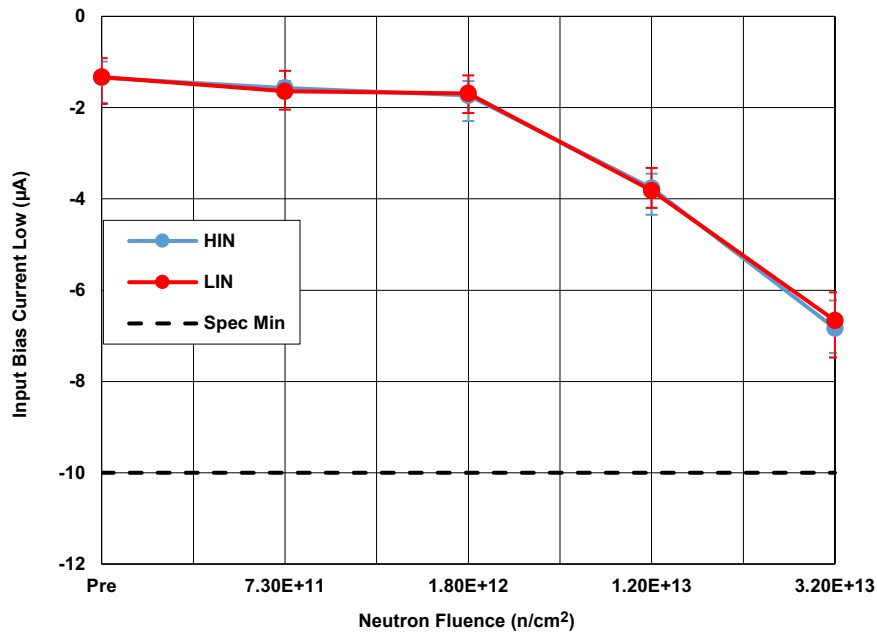


Figure 6. IS-2100ARH logic “0” input bias current ($-I_{IN}$) following neutron irradiation to each level. The error bars represent the minimum and maximum measured values. The SMD limit is $-10\mu\text{V}$ minimum.

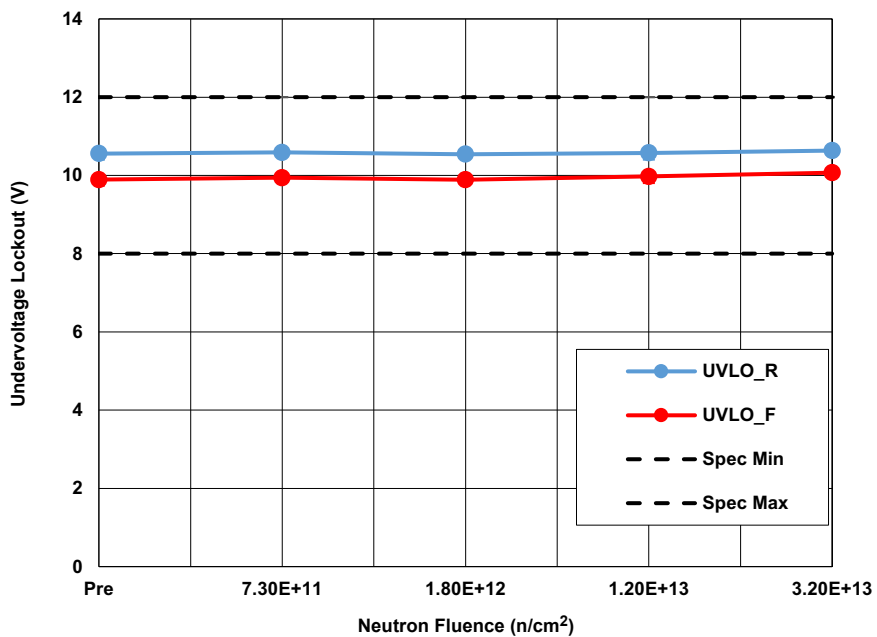


Figure 7. IS-2100ARH undervoltage lockout voltage (V_{THUV}) following neutron irradiation to each level. The error bars represent the minimum and maximum measured values. The SMD limits are 8V minimum and 12V maximum.

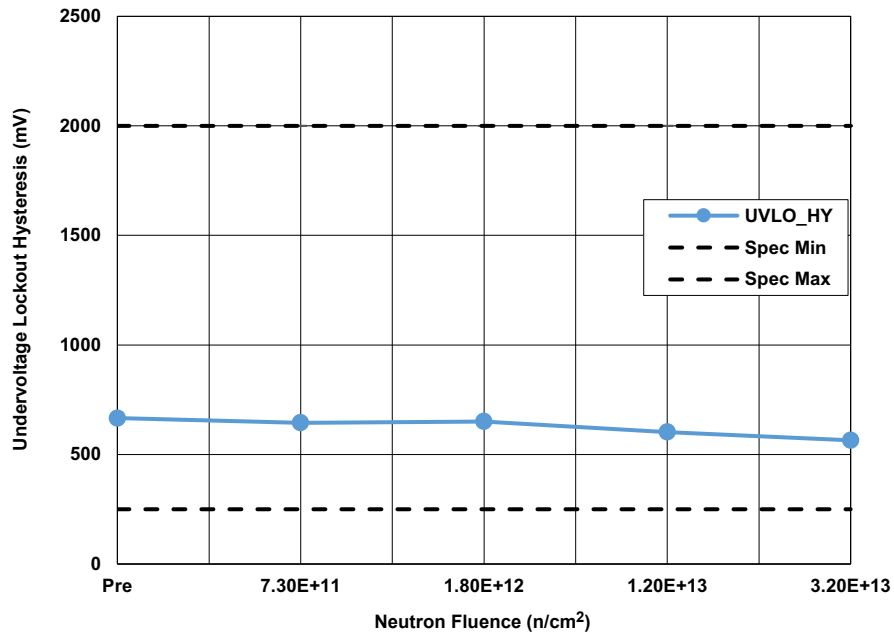


Figure 8. IS-2100ARH undervoltage lockout voltage hysteresis (V_{THUVs}) following neutron irradiation to each level. The error bars represent the minimum and maximum measured values. The SMD limits are 250mV minimum and 2000mV maximum.

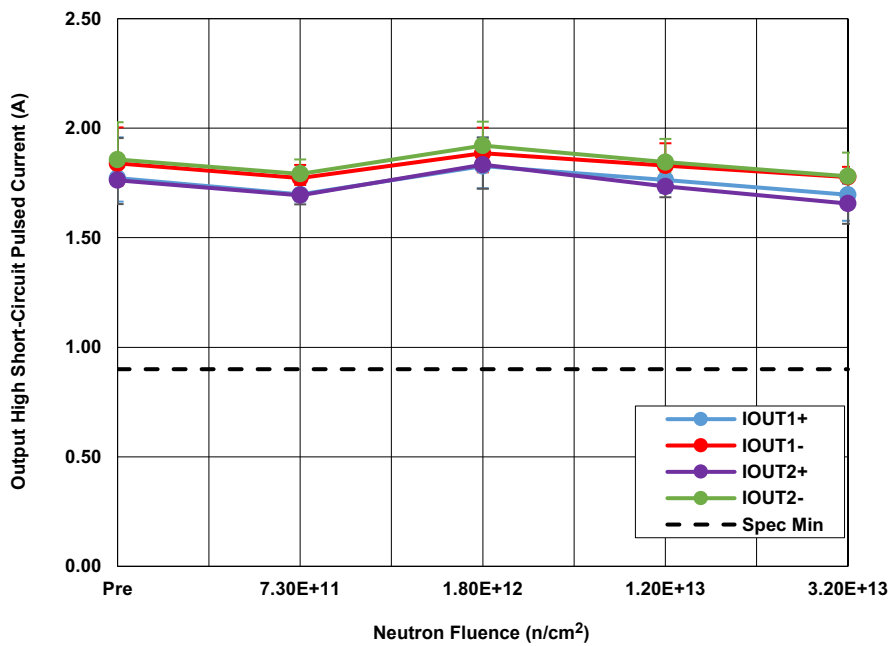


Figure 9. IS-2100ARH output high short-circuit current (pulsed) ($+I_{OUT}$, $-I_{OUT}$) following neutron irradiation to each level. The error bars represent the minimum and maximum measured values. The SMD limit is 0.9A minimum.

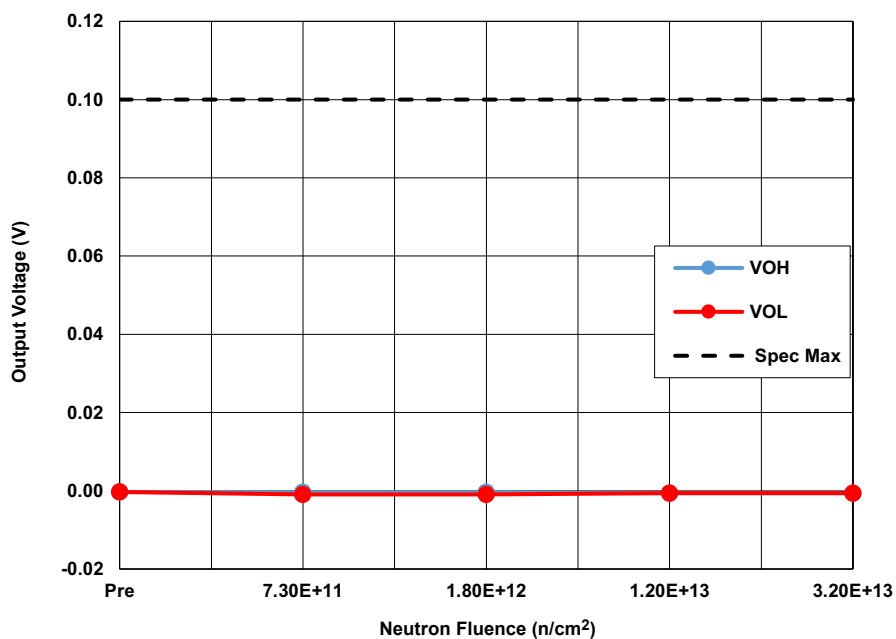


Figure 10. IS-2100ARH output voltage (differential from supply) (V_{OH} , V_{OL}) following neutron irradiation to each level. The error bars represent the minimum and maximum measured values. The SMD limit is 0.1V maximum.

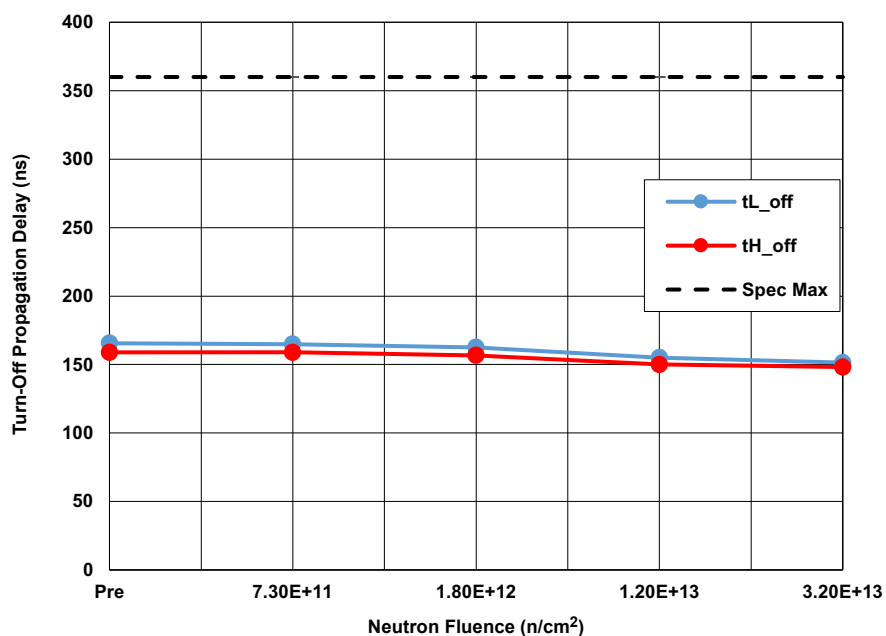


Figure 11. IS-2100ARH high-side and low-side turn-off propagation delay (t_{L_off} , t_{H_off}) following neutron irradiation to each level. The error bars represent the minimum and maximum measured values. The SMD limit is 360ns maximum.

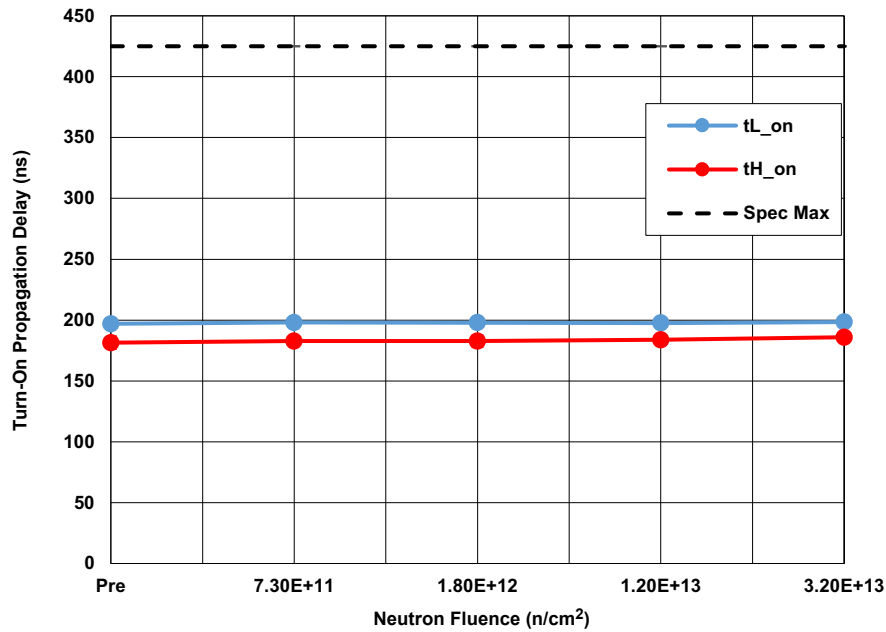


Figure 12. IS-2100ARH high-side and low-side turn-on propagation delay (tL_on, tH_on) following neutron irradiation to each level. The error bars represent the minimum and maximum measured values. The SMD limit is 425ns maximum.

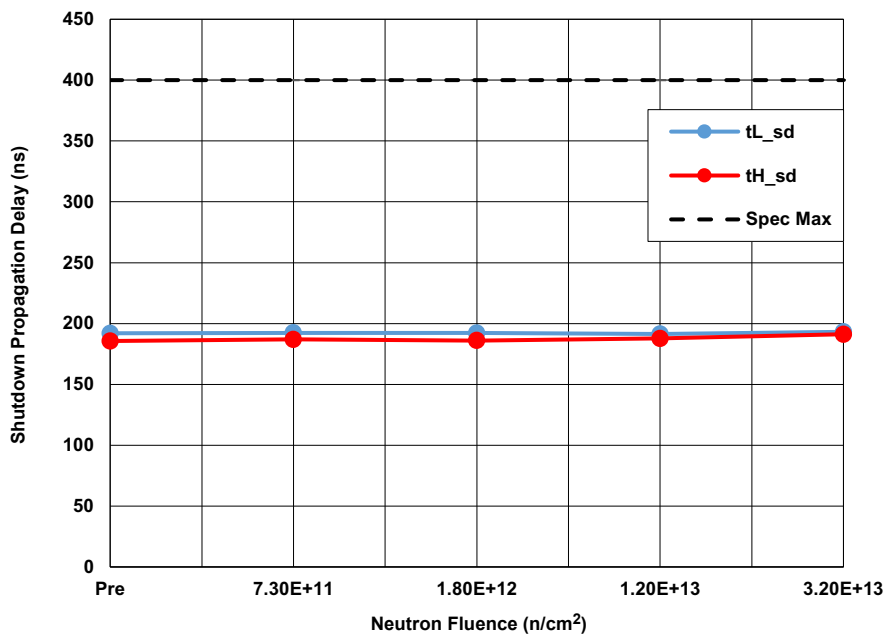


Figure 13. IS-2100ARH high-side and low-side shutdown propagation delay (tL_sd, tH_sd) following neutron irradiation to each level. The error bars represent the minimum and maximum measured values. The SMD limit is 400ns maximum.

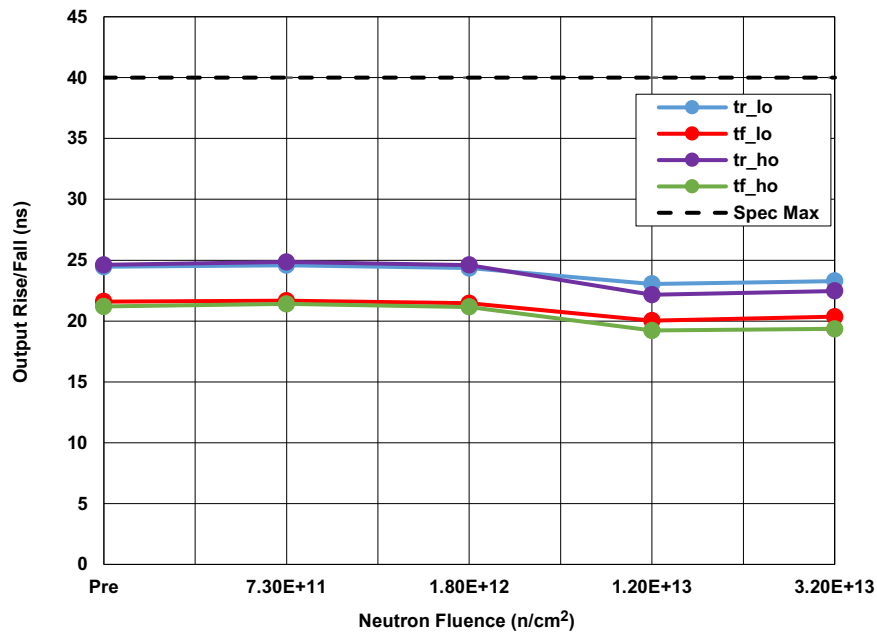


Figure 14. IS-2100ARH output rise and fall times (t_R , t_F) following neutron irradiation to each level. The error bars represent the minimum and maximum measured values. The SMD limit is 40ns maximum.

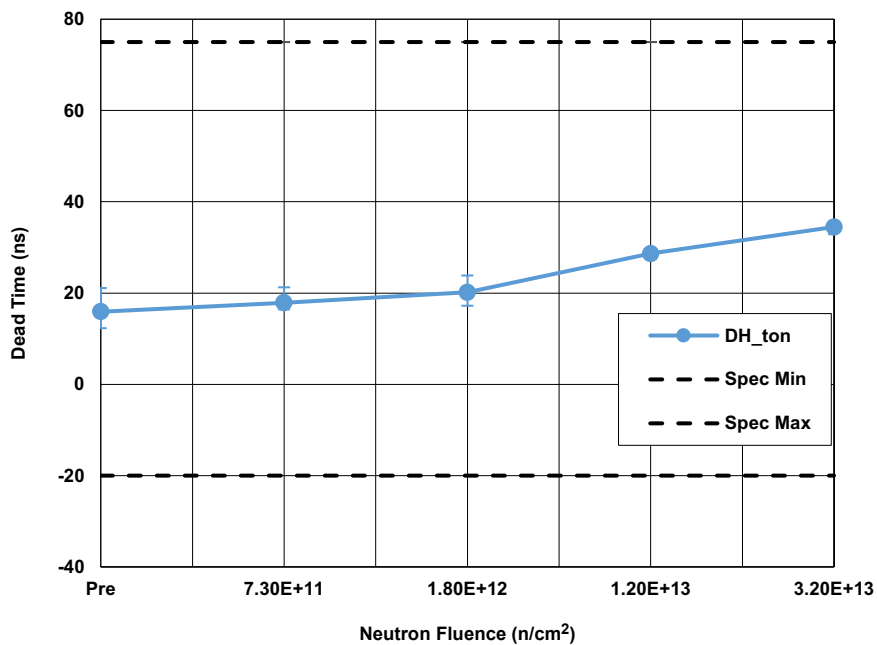


Figure 15. IS-2100ARH dead time (LO turn-off to HO turn-on) (DH_{ton}) following neutron irradiation to each level. The error bars represent the minimum and maximum measured values. The SMD limits are -20ns minimum and 75ns maximum.

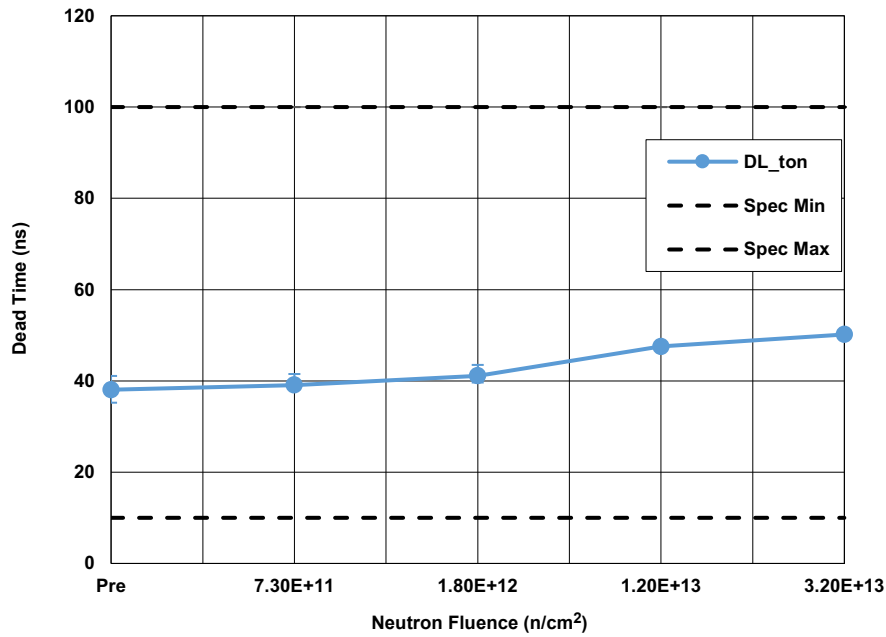


Figure 16. IS-2100ARH dead time (HO turn-off to LO turn-on) (DL_{ton}) following neutron irradiation to each level. The error bars represent the minimum and maximum measured values. The SMD limits are 10ns minimum and 100ns maximum.

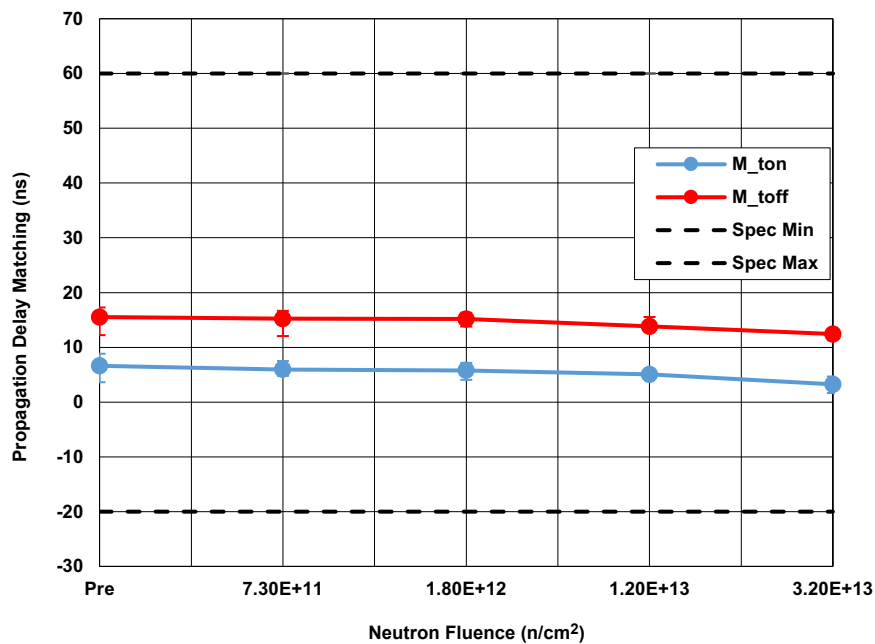


Figure 17. IS-2100ARH turn-on propagation delay matching (M_{ton}) following neutron irradiation to each level. The error bars represent the minimum and maximum measured values. The SMD limits are -20ns minimum and 60ns maximum.

3. Discussion and Conclusion

This document reports the results of 1MeV equivalent neutron testing of the IS-2100ARH radiation hardened high frequency half bridge driver. Parts were tested at $7.3 \times 10^{11} \text{ n/cm}^2$, $1.8 \times 10^{12} \text{ n/cm}^2$, $1.2 \times 10^{13} \text{ n/cm}^2$, and $3.2 \times 10^{13} \text{ n/cm}^2$. All samples passed the SMD limits after all exposures up to and including $3.2 \times 10^{13} \text{ n/cm}^2$. The results of key parameters before and after irradiation to each level are plotted in [Figure 1](#) through [Figure 17](#). The plots show the mean of each parameter as a function of neutron irradiation, with error bars that represent the minimum and maximum measured values. The figures also show the applicable electrical limits taken from the SMD.

3.1 Reported Parameters

Figure	Parameter	Limit, Low	Limit, High	Units	Notes
1	Quiescent V_{DD} supply current (inputs low)	-	2900	μA	All inputs = 0V
2	Quiescent V_{CC} supply current	-	50	μA	$V_{IN} = 0\text{V}$ or V_{DD}
3	Quiescent V_B supply current	-	500	μA	$V_{IN} = 0\text{V}$ or V_{DD}
4	Offset supply leakage current	-	500	μA	$V_B = V_S = 150\text{V}$
5	Logic "1" input bias current	-	75	μA	$V_{IN} = V_{DD}$
6	Logic "0" input bias current	-10	-	μA	$V_{IN} = 0\text{V}$
7	V_{DD} / V_{SS} undervoltage lockout threshold	8	12	V	-
8	V_{DD} / V_{SS} undervoltage lockout threshold hysteresis	250	2000	mV	-
9	Output high short-circuit pulsed current	0.9	-	A	$V_{OUT} = 0\text{V}$, $PW < 80\mu\text{S}$
10	Output voltage	-	0.1	V	$I_{OUT} = 0\text{mA}$, $V_{BIAS} - V_{OH}$
11	Turn-off propagation delay	-	360	ns	$C_L = 1000\text{pF}$
12	Turn-on propagation delay	-	425	ns	$C_L = 1000\text{pF}$
13	Shutdown propagation delay	-	400	ns	$C_L = 1000\text{pF}$
14	Output rise/fall time	-	40	ns	$C_L = 1000\text{pF}$
15	Dead time LO turn-off to HO turn-on	-20	75	ns	$C_L = 1000\text{pF}$
16	Dead time HO turn-off to LO turn-on	10	100	ns	$C_L = 1000\text{pF}$
17	Propagation delay matching	-20	60	ns	$C_L = 1000\text{pF}$

4. Revision History

Revision	Date	Description
1.00	Jun 6, 2025	Applied the latest template. Minor update to the Variables Data and Discussion and Conclusion sections.
0.00	Apr 4, 2018	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.