

RELIABILITY REPORT

SERIES: UPC4570GR(20)

DEVICE: UPC4570GR(20)-9LG-E1-A
UPC4570GR(20)-9LG-E1-AT

QUALITY GRADE: High Quality

For both products assembled by Renesas Semiconductor (Kedah) Sdn. Bhd. and Greatek Electronics Inc.

Quality Assurance Div.
Renesas Electronics Corporation

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Q100 Qualification Test Results for UPC4570GR(20)

[Note : Basically qualification tests were performed using a representative product with the same wafer process and the same package structure .]

APR-22-H0185-B

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
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TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS

PC	A1	JESD22 A113 J-STD-020	SMD only; Moisture Preconditioning (Test @ Rm) for THB/HAST, AC/UHST, TC, PTC ; Peak Reflow Temp= 260C	Min.MSL=1			Min.MSL=1	-
THB	A2	JESD22 A101 or JESD22 A110	Temperature Humidity Bias: (Test @ Rm/Hot) Ta=85C, RH=85%, 1000hrs	3	77	231	0 of 231	-
THS	A3	JESD22 A118	Unbiased Highly Accelerated Stress Test: (Test @ Rm) Ta=85C, RH=85%, 1000hrs	3	77	231	0 of 231	-
TC	A4	JESD22 A104	Temperature Cycle: (Test @ Rm/Hot) Ta=-65C to 150C, 500cycles	3	77	231	0 of 231 0 Fails after TC (WBP)	-
PTC	A5	JESD22 A105	Power Temperature Cycle: (Test @ Rm/Hot) -	-	-	-	-	N/A
HTSL	A6	JESD22 A103	High Temperature Storage Life: (Test @ Rm/Hot) Ta=150C, 1000hrs	3	45	135	0 of 135	-

TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS

HTOL	B1	JESD22 A108	High Temp Operating Life: (Test @ Rm/Cold/Hot) Ta=125C, 1000hrs	3	77	231	0 of 231	-
ELFR	B2	AEC-Q100-008	Early Life Failure Rate: (Test @ Rm/Hot) Ta=125C, 48hrs	3	800	2400	0 of 2400	-
EDR	B3	AEC-Q100-005	NVM Endurance & Data Retention Test: (Test @ Rm/Hot)	For HTOL	-	-	-	N/A
				For HTSL	-	-	-	N/A

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
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TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS

WBS	C1	AEC-Q100-001 AEC-Q003	Wire Bond Shear Test: (Cpk > 1.67)	30 bonds	5 parts Min.	30 bonds	0 of 30 bonds	Cpk>1.67
WBP	C2	Mil-STD-883 Method 2011 AEC-Q003	Wire Bond Pull: (Cpk > 1.67); Each bonder used	30 bonds	5 parts Min.	30 bonds	0 of 30 bonds	Cpk>1.67
SD	C3	JSTD-002D	Solderability: (>95% coverage)	1	15	15	0 of 15	
PD	C4	JESD22 B100, JESD22 B108 AEC-Q003	Physical Dimensions: (Cpk > 1.67)	3	10	30	0 of 30	Cpk>1.67
SBS	C5	AEC-Q100-010 AEC-Q003	Solder Ball Shear: (Cpk > 1.67)	-	-	-	-	N/A
LI	C6	JESD22 B105	Lead Integrity: (No lead cracking or breaking); Through-hole only; 10 leads from each of 5 devices	-	-	-	-	N/A
BST	C7	JESD22-B117	Bump Shear: (Cpk > 1.67)	-	-	-	-	N/A

TEST GROUP D – DIE FABRICATION RELIABILITY TESTS

EM	D1	JESD61	Electromigration:	-	-	-	Pass	Confirmed by process TEG
TDDDB	D2	JESD35	Time Dependent Dielectric Breakdown:	-	-	-	-	N/A Process without MOSFETs
HCI	D3	JESD60 & 28	Hot Carrier Injection:	-	-	-	-	N/A Process without MOSFETs
NBTI	D4	JESD90	Negative Bias Temperature Instability:	-	-	-	-	N/A Process without MOSFETs
SM	D5	JESD61,87 & 202	Stress Migration:	-	-	-	Pass	Confirmed by process TEG

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
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TEST GROUP E- ELECTRICAL VERIFICATION

TEST	E1	User/Supplier Specification	Pre and Post Stress Electrical Test:	All	All	All	0 of All	-
HBM	E2	AEC-Q100-002	Electrostatic Discharge, Human Body Model: (Test @ Rm/Hot); 2KV HBM Classification 2 or better	1	3	3	0 of 3 ESD Level= HBM:2	HBM>2KV
CDM	E3	AEC-Q100-011	Electrostatic Discharge, Charged Device Model: (Test @ Rm/Hot); Test Condition 750 corner pins, Test Condition 500 all other pins (Classification C2A or better)	1	3	3	0 of 3 ESD Level= CDM:C2A	Corner leads: 750V Pass All other leads:500V Pass
LU	E4	AEC-Q100-004	Latch-Up: (Test @ Rm/Hot)	1	3	3	0 of 3	-
ED	E5	AEC-Q100-009 AEC-Q003	Electrical Distributions: (Test @ Rm/Hot/Cold) (where applicable, Cpk>1.67)	3	30	90	Cpk>1.67	-
FG	E6	AEC-Q100-007	Fault Grading:	-	-	-	-	N/A
CHAR	E7	AEC-Q003	Characterization: (Test @ Rm/Hot/Cold)	-	-	-	Pass	According to Renesas standard procedure
EMC	E9	SAE J1752/3	Electromagnetic Compatibility (Radiated Emissions)	-	-	-	-	N/A. This product only follows the input signal to output, so there is no EMI concern.
SC	E10	AEC Q100-012	Short Circuit Characterization	-	-	-	-	N/A
SER	E11	JESD89-1 JESD89-2 JESD89-3	Soft Error Rate	-	-	-	-	N/A
LF	E12	AEC-Q005	Lead (Pb) Free: (see AEC-Q005)	-	-	-	Pass	Solderability: See SD (C3) result. Whisker: Performed on product TEG with test method based on JESD201.

TEST GROUP F – DEFECT SCREENING TESTS

PAT	F1	AEC-Q001	Process Average Testing: (see AEC-Q001)	All	All	All	Reject units outside PAT limits	Apply to mass production according to Renesas standard procedure
SBA	F2	AEC-Q002	Statistical Bin/Yield Analysis: (see AEC-Q002)	All	All	All	Reject units outside criteria	Apply to mass production according to Renesas standard procedure

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
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TEST GROUP G – CAVITY PACKAGE INTEGRITY TESTS (for Ceramic Package testing only)

MS	G1	JESD22 B110	Mechanical Shock: (Test @ Rm)	-	-	-	-	N/A
VFV	G2	JESD22 B103	Variable Frequency Vibration: (Test @ Rm)	-	-	-	-	N/A
CA	G3	MIL-STD-883 Method 2001	Constant Acceleration: (Test @ Rm)	-	-	-	-	N/A
GFL	G4	MIL-STD-883 Method 1014	Gross and Fine Leak:	-	-	-	-	N/A
DROP	G5	-----	Drop Test: (Test @ Rm) MEMS cavity parts only. Drop part on each of 6 axes once from a height of 1.2m onto a concrete surface.	-	-	-	-	N/A
LT	G6	MIL-STD-883 Method 2004	Lid Torque:	-	-	-	-	N/A
DS	G7	MIL-STD-883 Method 2019	Die Shear:	-	-	-	-	N/A
IWV	G8	MIL-STD-883 Method 1018	Internal Water Vapor:	-	-	-	-	N/A