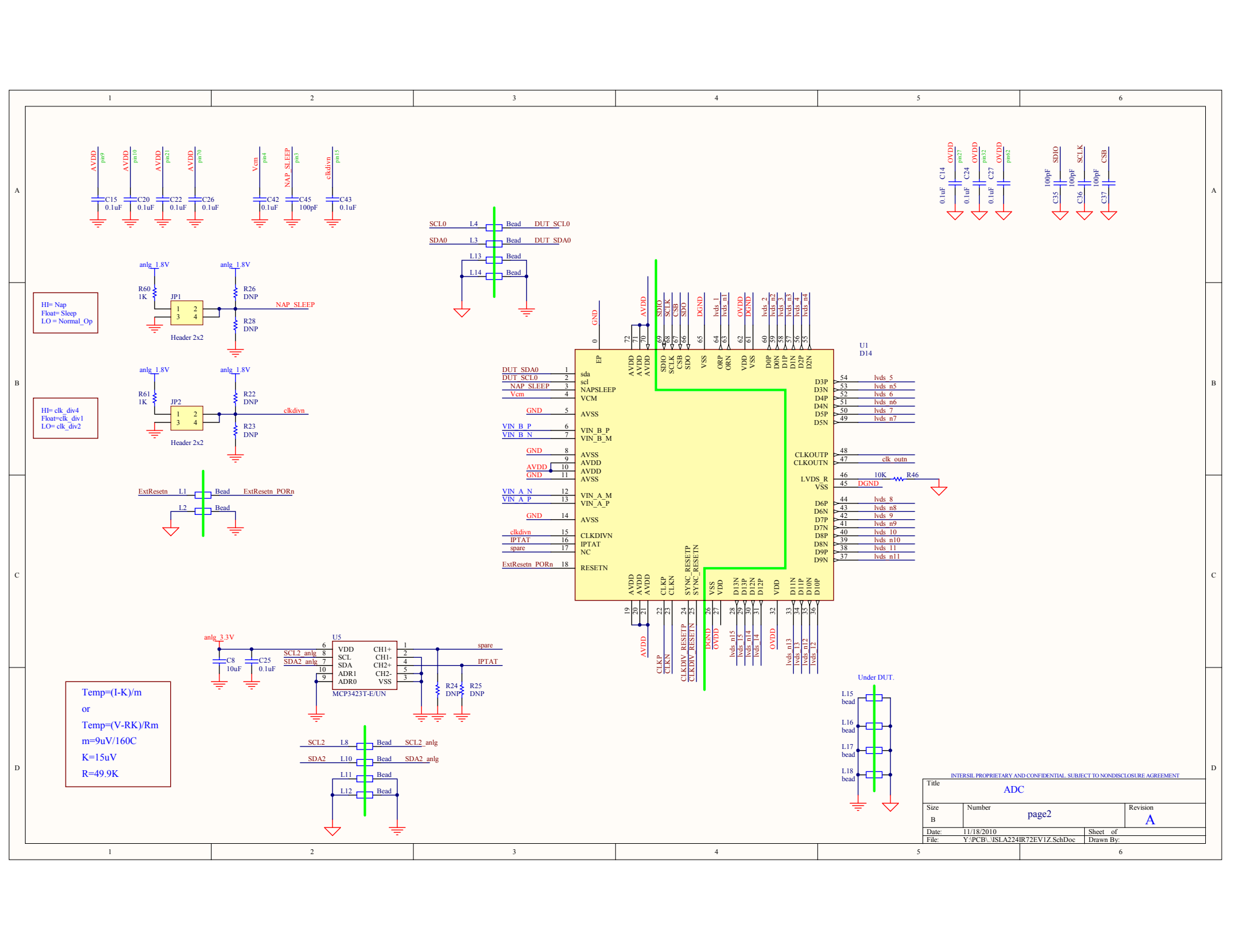
ISL224P25 DUAL INPUT CUSTOMER EVALUATION DAUGHER CARD

-ISL224P25EV1Z

-ISL224P25EV1Z_ ANALOG FRONT-END/CLOCK/SYNCRONOUS RESET

-ISL224P25EV1Z_ IO/LEVEL TRANSLATOR ID/PROM

Title	Title	
Size: B	Number: Page 1	Revision: A
Date: 11/18/2010	Sheet of	
File: Y:\PCB\..\ISLA224IR72EV1Z_TITLE.SchDoc	Drawn By:	


AVDD C15 0.1uF
AVDD C20 0.1uF
AVDD C22 0.1uF
AVDD C26 0.1uF
Vcm C42 0.1uF
NAP_SLEEP C45 100pF
clkdivn C43 0.1uF
OVDD C14 0.1uF
OVDD C24 0.1uF
OVDD C27 0.1uF
SDIO 100pF C35
SCLK 100pF C36
CSB 100pF C37
HI= Nap
Float= Sleep
LO = Normal_Op
anlg_1.8V R60 1K
JP1
R26 DNP
NAP_SLEEP
R28 DNP
Header 2x2
HI= clk_div4
Float=clk_div1
LO= clk_div2
anlg_1.8V R61 1K
JP2
R22 DNP
clkdivn
R23 DNP
Header 2x2
ExtResetn L1 Bead ExtResetn_PORn
L2 Bead
SCL0 L4 Bead DUT_SCL0
SDA0 L3 Bead DUT_SDA0
L13 Bead
L14 Bead
U1
D14
EP
DUT_SDA0 1 sda
DUT_SCL0 2 scl
NAP_SLEEP 3 NAPSLEEP
Vcm 4 VCM
GND 5 AVSS
VIN_B_P 6 VIN_B_P
VIN_B_N 7 VIN_B_M
GND 8 AVSS
9 AVDD
AVDD 10 AVDD
GND 11 AVSS
VIN_A_N 12 VIN_A_M
VIN_A_P 13 VIN_A_P
GND 14 AVSS
clkdivn 15 CLKDIVN
IPTAT 16 IPTAT
spare 17 NC
ExtResetn_PORn 18 RESETN
D3P 54 lvds_5
D3N 53 lvds_n5
D4P 52 lvds_6
D4N 51 lvds_n6
D5P 50 lvds_7
D5N 49 lvds_n7
CLKOUTP 48
CLKOUTN 47 clk_outn
LVDS_R 46 10K R46
VSS 45 DGND
D6P 44 lvds_8
D6N 43 lvds_n8
D7P 42 lvds_9
D7N 41 lvds_n9
D8P 40 lvds_10
D8N 39 lvds_n10
D9P 38 lvds_11
D9N 37 lvds_n11
anlg_3.3V
C8 10uF
C25 0.1uF
U5
SCL2_anlg 8
SDA2_anlg 7
VDD SCL SDA ADR1 ADR0
CH1+ CH1- CH2+ CH2- VSS
MCP3423T-E/UN
spare
IPTAT
R24 DNP
R25 DNP
SCL2 L8 Bead SCL2_anlg
SDA2 L10 Bead SDA2_anlg
L11 Bead
L12 Bead
Under DUT.
L15 bead
L16 bead
L17 bead
L18 bead
Temp=(I-K)/m
or
Temp=(V-RK)/Rm
m=9uV/160C
K=15uV
R=49.9K
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Title ADC
Size B
Number page2
Revision A
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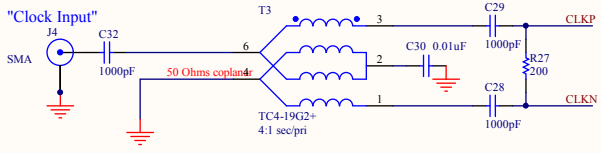
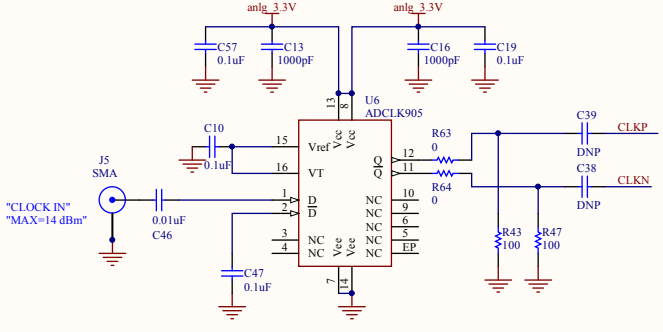
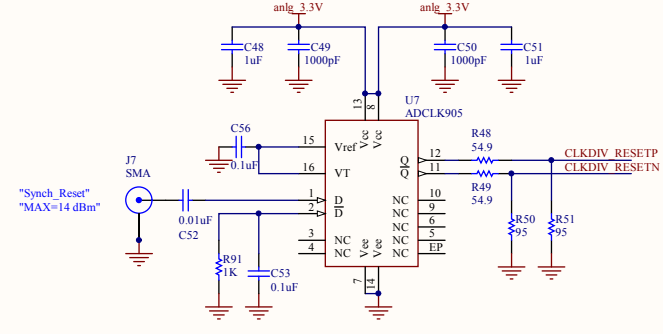
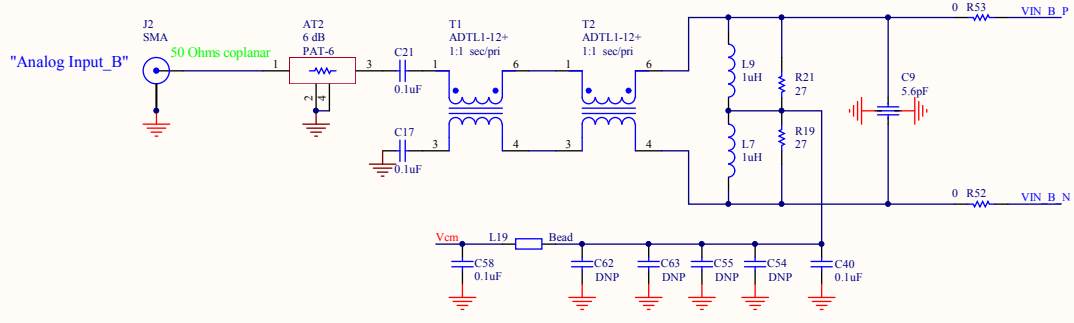
File: Y:\PCB\..\ISLA224IR72EV1Z.SchDoc
Drawn By:

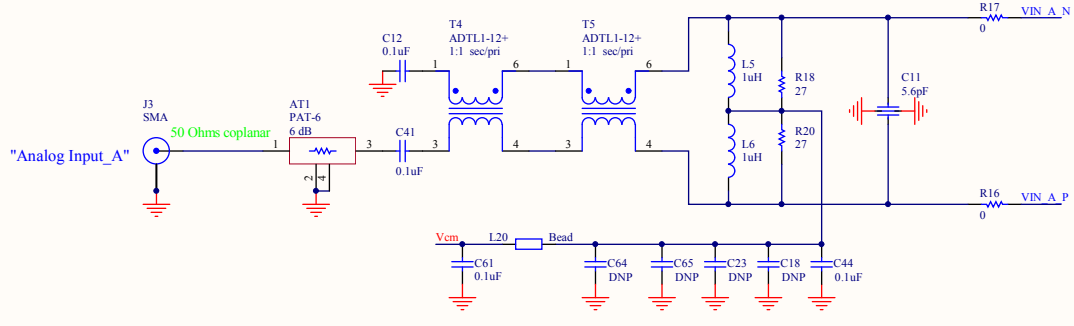
Sampling Clock	Populate	Depopulate
Sine	C28, C29	C38, C39
LVDS	C38, C39	C28, C29











Title: Analog Front End, Clock, Sync Reset		
Size: B	Number: page3	Revision: A
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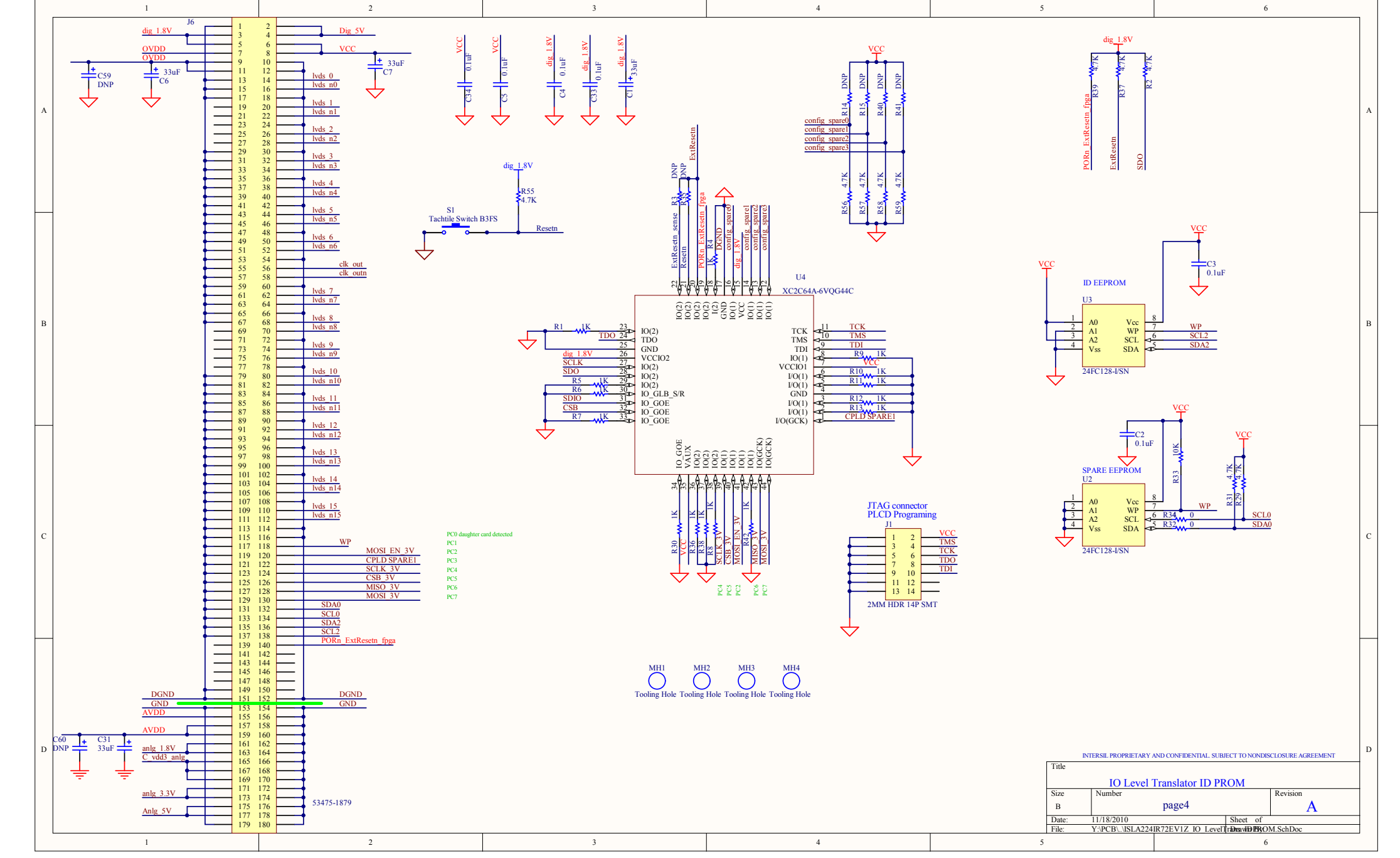
File: Y:\PCB\..\ISLA224IR72EV1Z_Analog_Input_Drive.SchDoc		


J6
dig_1.8V
OVDD
OVDD
C59
DNP
C6
33uF
Dig_5V
VCC
C7
33uF
lvds_0
lvds_n0
lvds_1
lvds_n1
lvds_2
lvds_n2
lvds_3
lvds_n3
lvds_4
lvds_n4
lvds_5
lvds_n5
lvds_6
lvds_n6
clk_out
clk_outn
lvds_7
lvds_n7
lvds_8
lvds_n8
lvds_9
lvds_n9
lvds_10
lvds_n10
lvds_11
lvds_n11
lvds_12
lvds_n12
lvds_13
lvds_n13
lvds_14
lvds_n14
lvds_15
lvds_n15
WP
MOSI_EN_3V
CPLD SPARE1
SCLK_3V
CSB_3V
MISO_3V
MOSI_3V
SDA0
SCL0
SDA2
SCL2
PORn_ExtResetn_fpga
DGND
GND
AVDD
AVDD
C60
DNP
C31
33uF
anlg_1.8V
C_vdd3_anlg
anlg_3.3V
Anlg_5V
53475-1879
VCC
0.1uF
C341
VCC
0.1uF
C5
dig_1.8V
0.1uF
C4
dig_1.8V
0.1uF
C33
dig_1.8V
3.3uF
C1
dig_1.8V
R55
4.7K
S1
Tachtile Switch B3FS
Resetn
PC0 daughter card detected
PC1
PC2
PC3
PC4
PC5
PC6
PC7
DNP
R3
DNP
R4
1K
ExtResetn
ExtResetn_sense
Resetn
PORn_ExtResetn_fpga
DGND
dig_1.8V
config_spare0
config_spare1
config_spare2
config_spare3
U4
XC2C64A-6VQG44C
IO(2)
TDO
GND
VCCIO2
IO(2)
IO(2)
IO(2)
IO_GLB_S/R
IO_GOE
IO_GOE
IO_GOE
TCK
TMS
TDI
IO(1)
VCCIO1
I/O(1)
I/O(1)
GND
I/O(1)
I/O(1)
I/O(GCK)
R1
1K
TDO
dig_1.8V
SCLK
SDO
R5
1K
R6
1K
SDIO
CSB
R7
1K
R9
1K
R10
1K
R11
1K
R12
1K
R13
1K
CPLD SPARE1
VCC
R30
1K
R36
1K
R38
1K
R8
1K
R40
1K
R41
1K
SCLK_3V
CSB_3V
MOSI_EN_3V
MISO_3V
MOSI_3V
PC4
PC5
PC2
PC6
PC7
JTAG connector
PLCD Programing
J1
VCC
TMS
TCK
TDO
TDI
2MM HDR 14P SMT
MH1
MH2
MH3
MH4
Tooling Hole
Tooling Hole
Tooling Hole
Tooling Hole
VCC
DNP
R14
DNP
R15
DNP
R40
DNP
R41
config_spare0
config_spare1
config_spare2
config_spare3
4.7K
R56
4.7K
R57
4.7K
R58
4.7K
R59
dig_1.8V
4.7K
R39
4.7K
R37
4.7K
R2
PORn_ExtResetn_fpga
ExtResetn
SDO
VCC
C3
0.1uF
ID EEPROM
U3
A0
A1
A2
Vss
Vcc
WP
SCL
SDA
WP
SCL2
SDA2
24FC128-I/SN
VCC
C2
0.1uF
SPARE EEPROM
U2
10K
R33
WP
R34
0
R32
0
SCL0
SDA0
24FC128-I/SN
4.7K
R31
4.7K
R29
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Title
IO Level Translator ID PROM
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A
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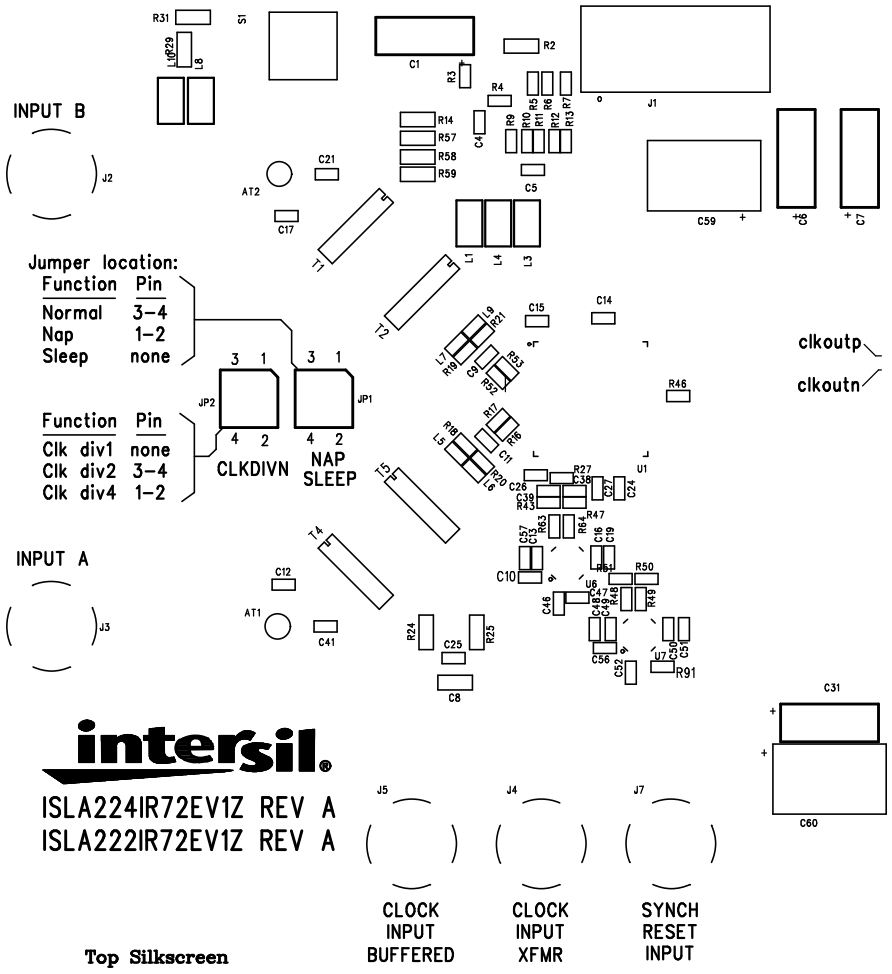
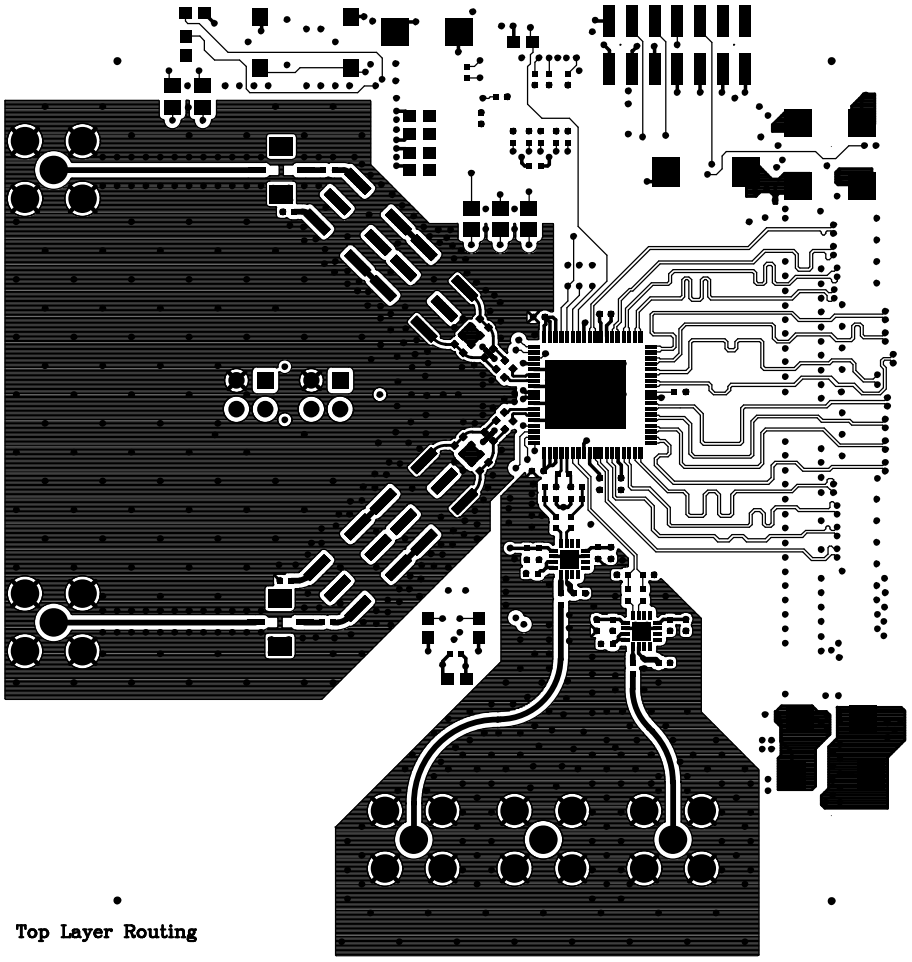
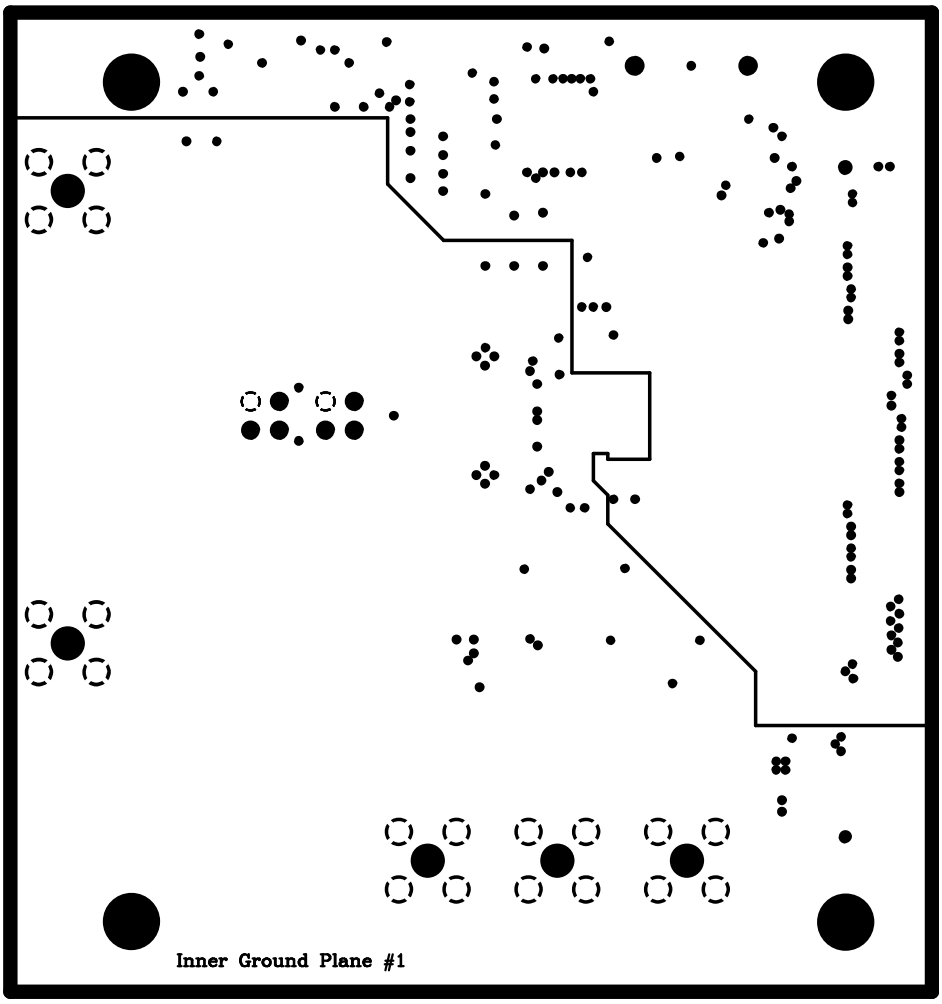
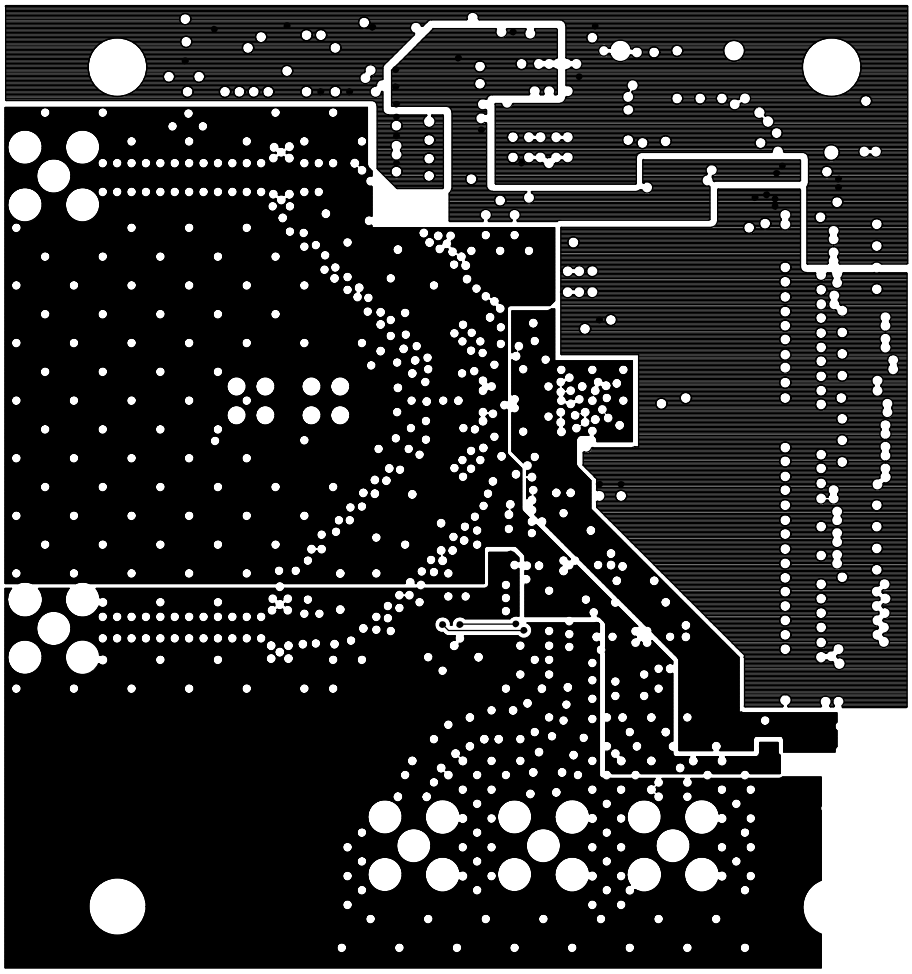


Top Silkscreen

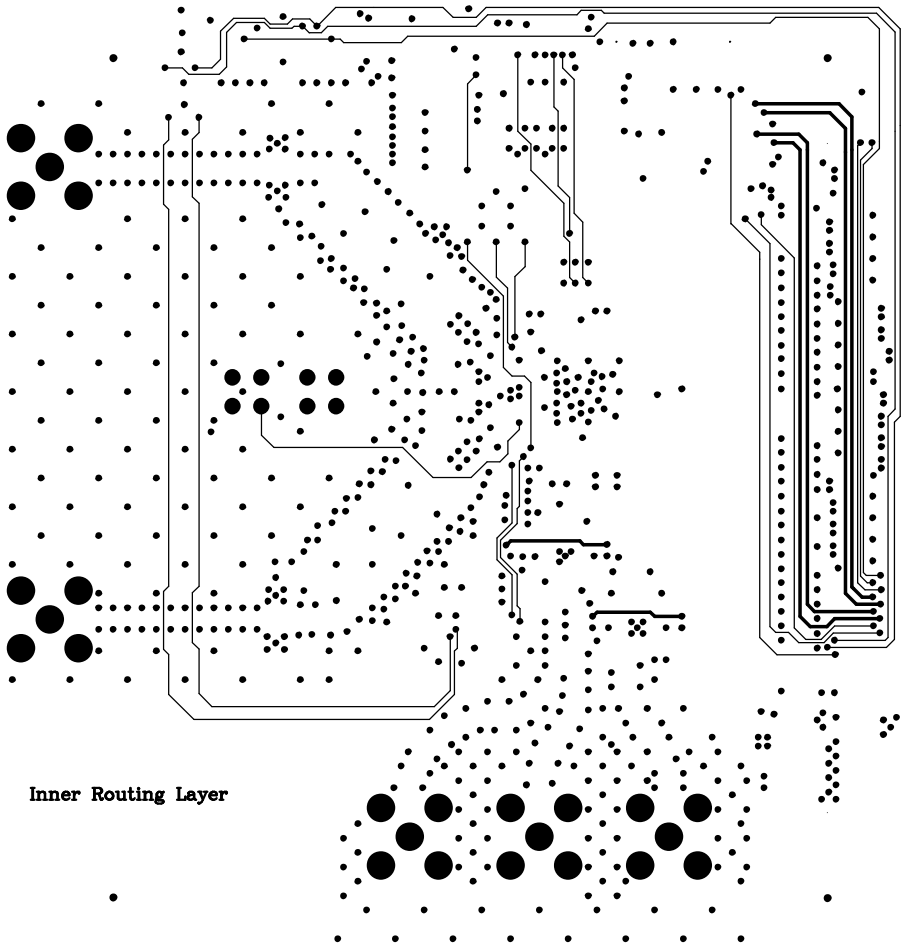


Top Layer Routing

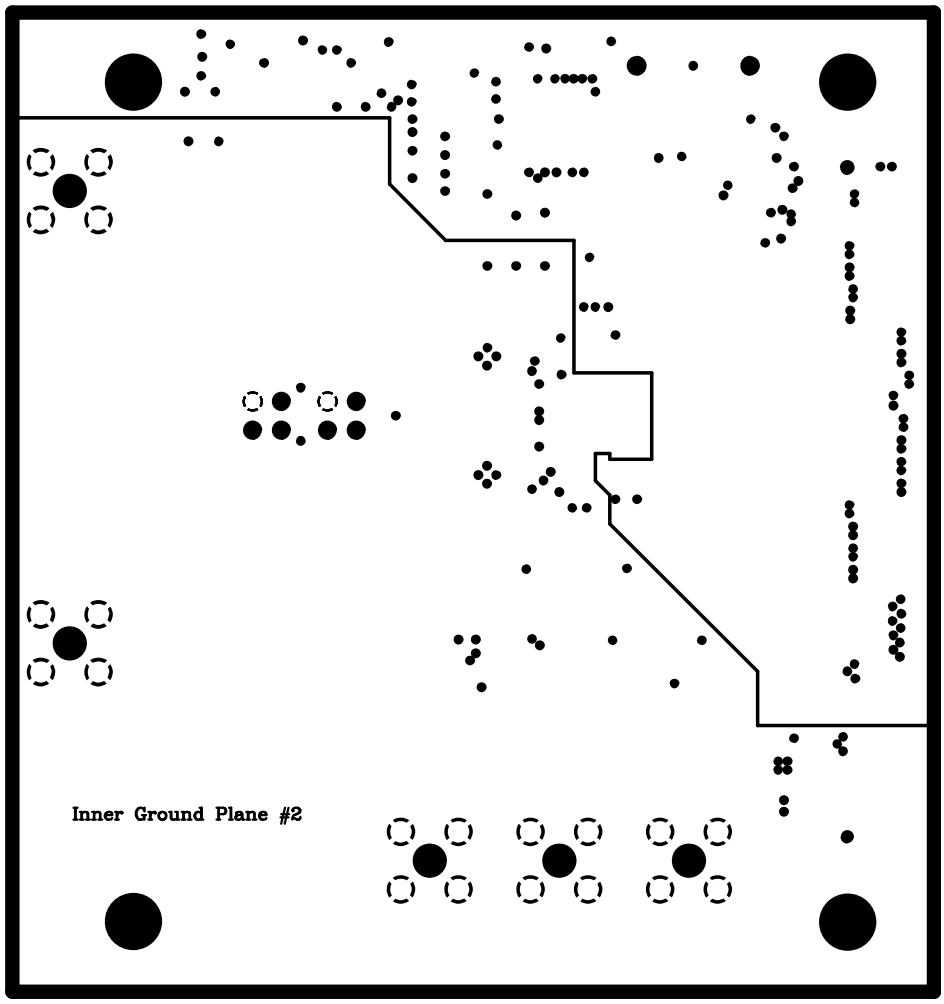

Inner Ground Plane #1

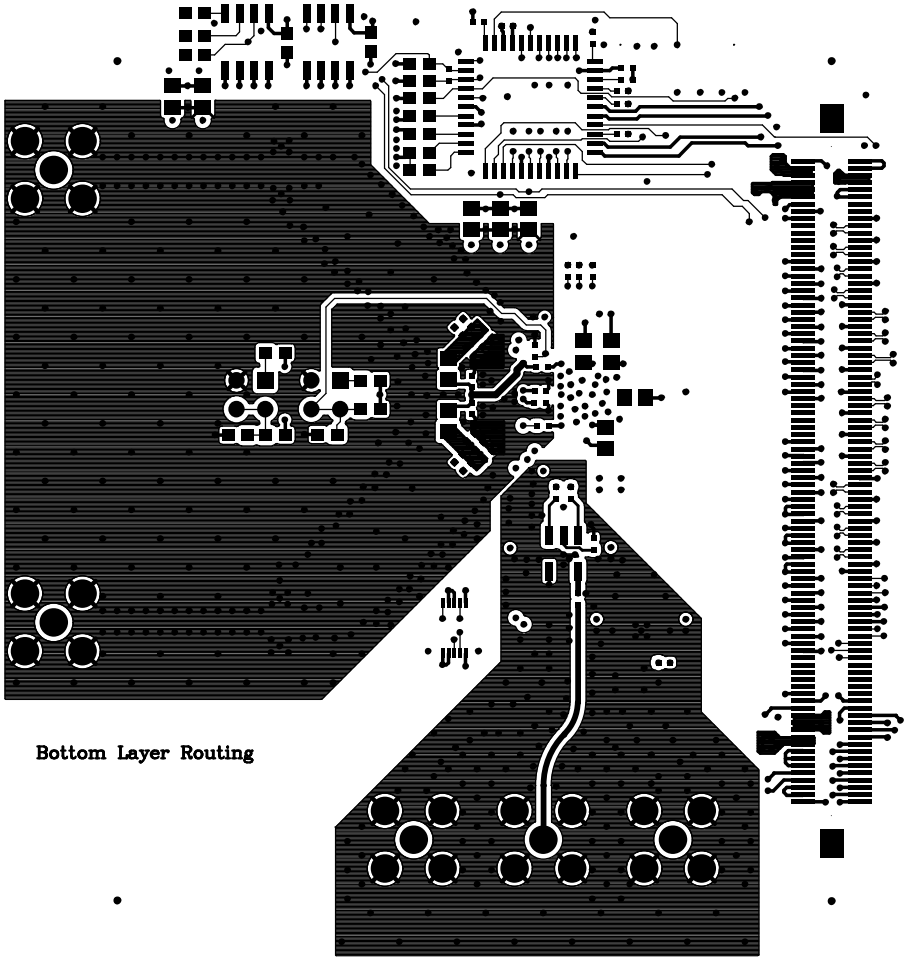


Split Power Plane

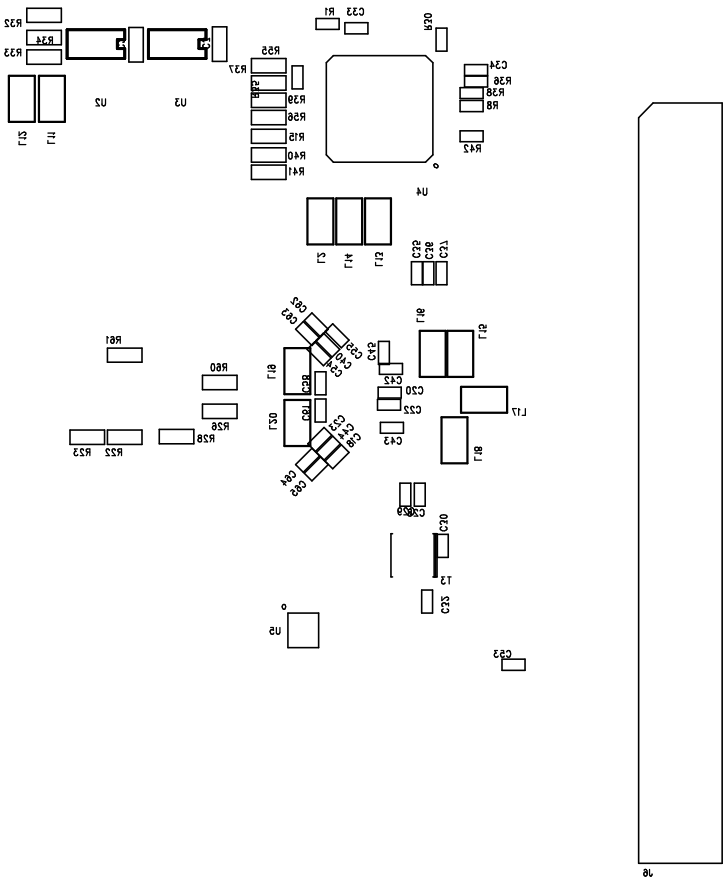


Inner Routing Layer


Inner Ground Plane #2



Bottom Layer Routing



Bottom Silkscreen