

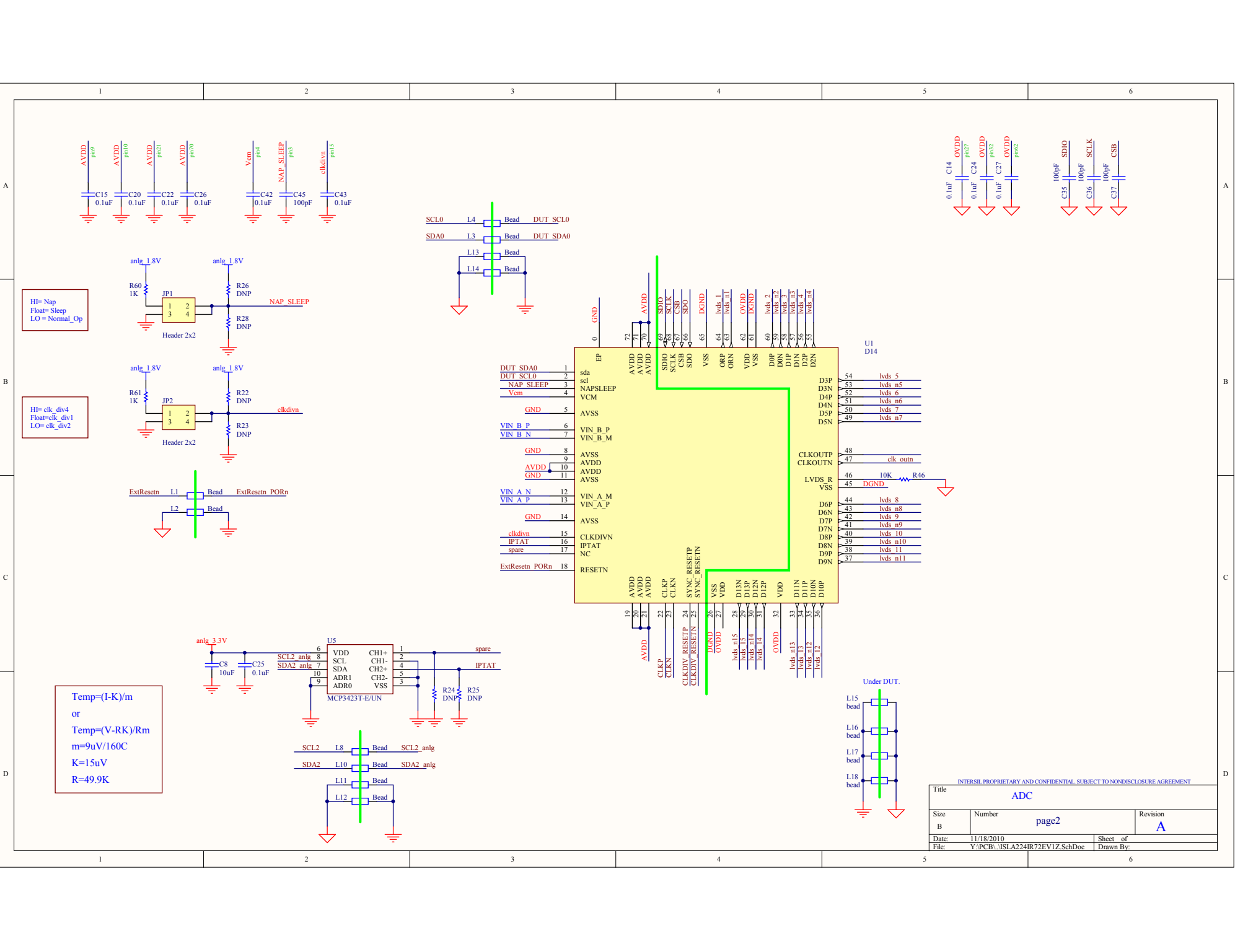
ISL224P25 DUAL INPUT CUSTOMER EVALUATION DAUGHER CARD

-ISL224P25EV1Z

-ISL224P25EV1Z_ ANALOG FRONT-END/CLOCK/SYNCRONOUS RESET

-ISL224P25EV1Z_ IO/LEVEL TRANSLATOR ID/PROM

Title		Title	
Size	Number	Revision	
B	Page 1	A	
Date:	11/18/2010	Sheet of	
File:	Y:\PCB\ISLA224R72EV1Z TITLE.Sch		



HI= Nap
 Float= Sleep
 LO= Normal_Op

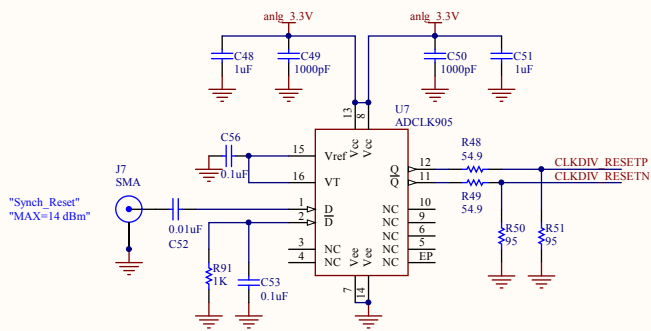
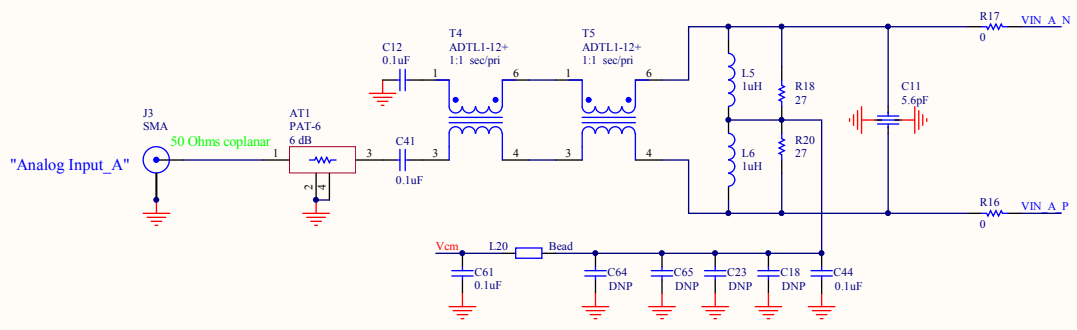
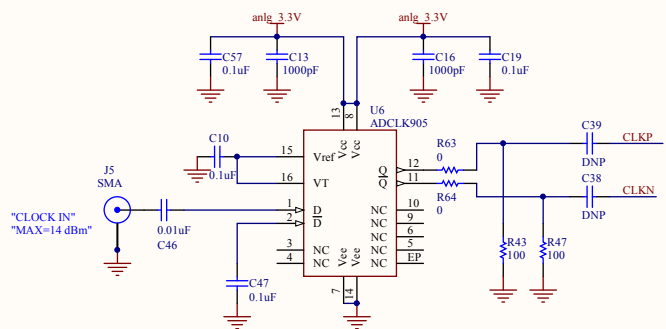
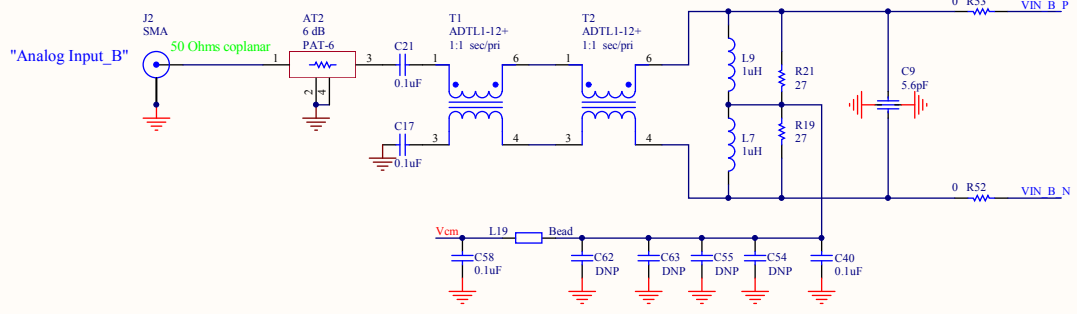
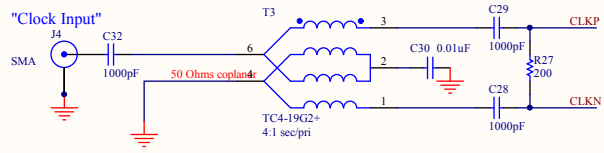
HI= clk_div4
 Float=clk_div1
 LO= clk_div2

Temp=(1-K)/m
 or
 Temp=(V-RK)/Rm
 m=9uV/160C
 K=15uV
 R=49.9K

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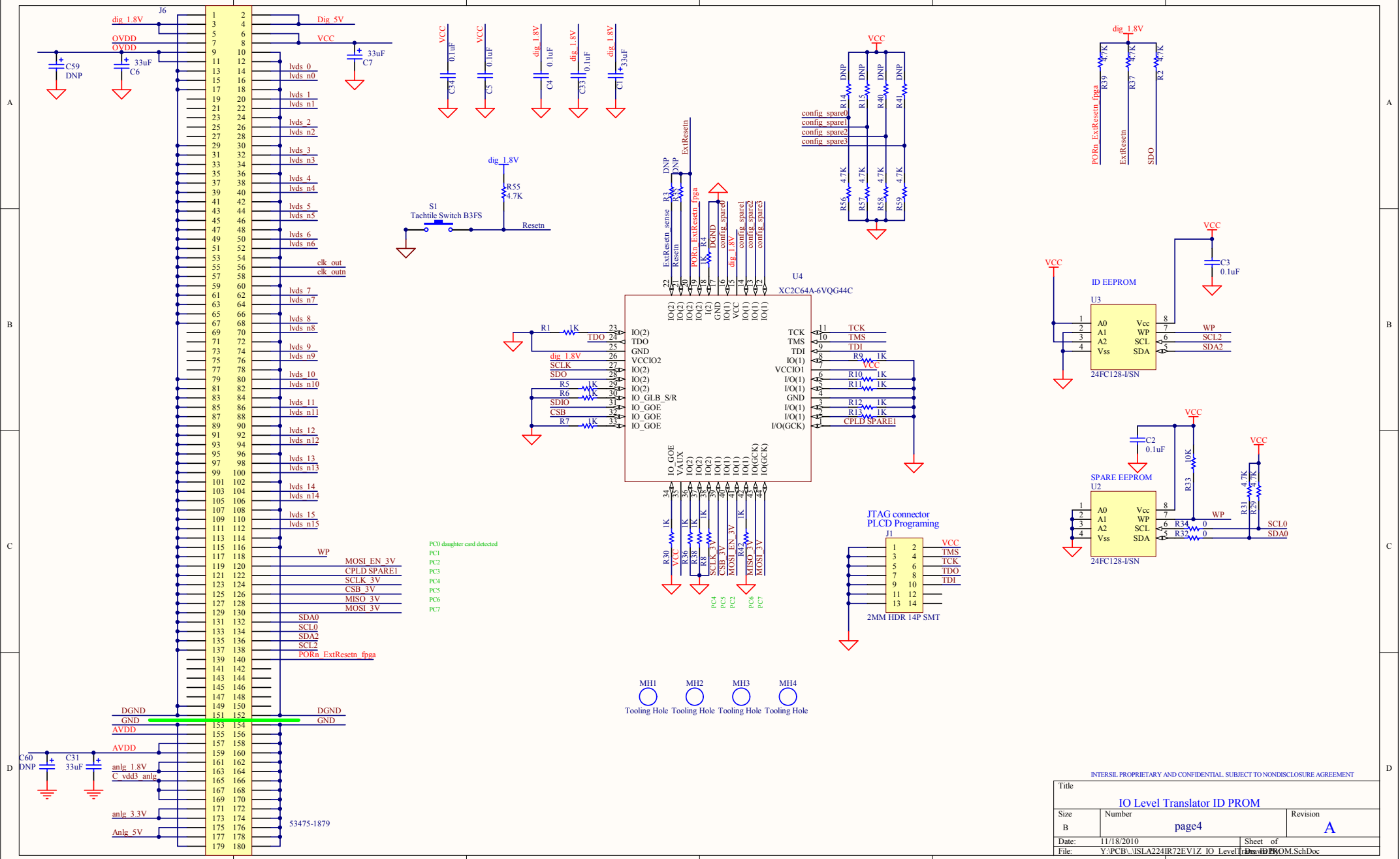
Title		ADC	
Size	Number	page2	Revision
B			A
Date:	11/18/2010	Sheet of	
File:	Y:\PCB\USL\A224R72EV1Z SchDoc	Drawn By:	

	Populate	Depopulate
Sampling Clock	C28, C29	C38, C39
Sine	C38, C39	C28, C29
LVDS		



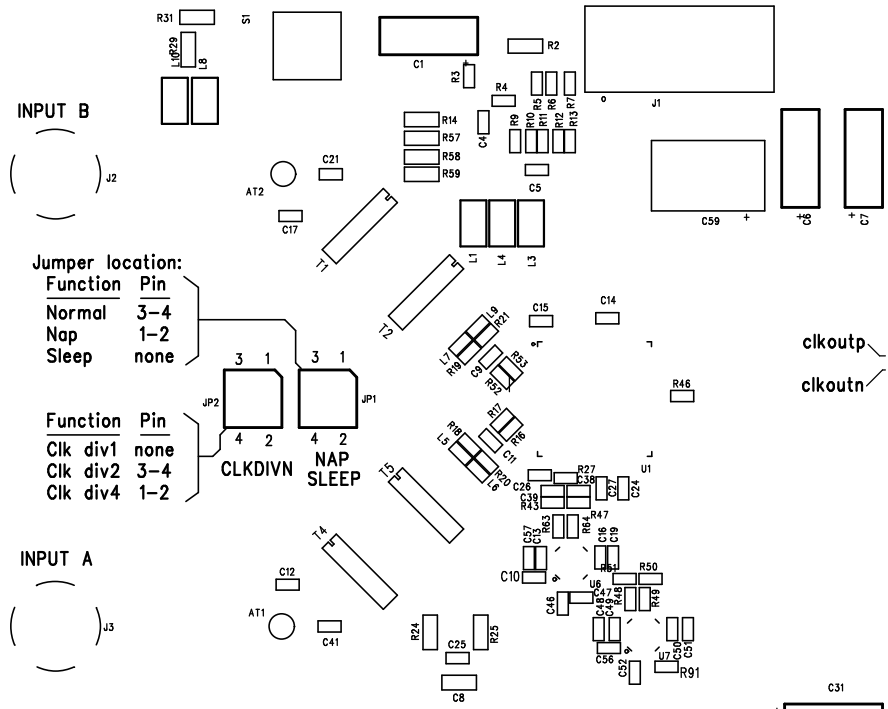
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Title		
Analog Front End, Clock, Synch Reset		
Size	Number	Revision
B	page3	A
Date:	11/18/2010	Sheet of
File:	Y:\PCB\USL A224IR72EVIZ Analog Input	Doc



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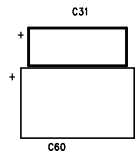
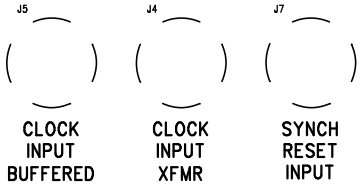
Title		
IO Level Translator ID PROM		
Size	Number	Revision
B	page4	A
Date:	11/18/2010	Sheet of
File:	Y:\PCB\MSLA224IR72EV1Z_IO Level Translator ID PROM.SchDoc	

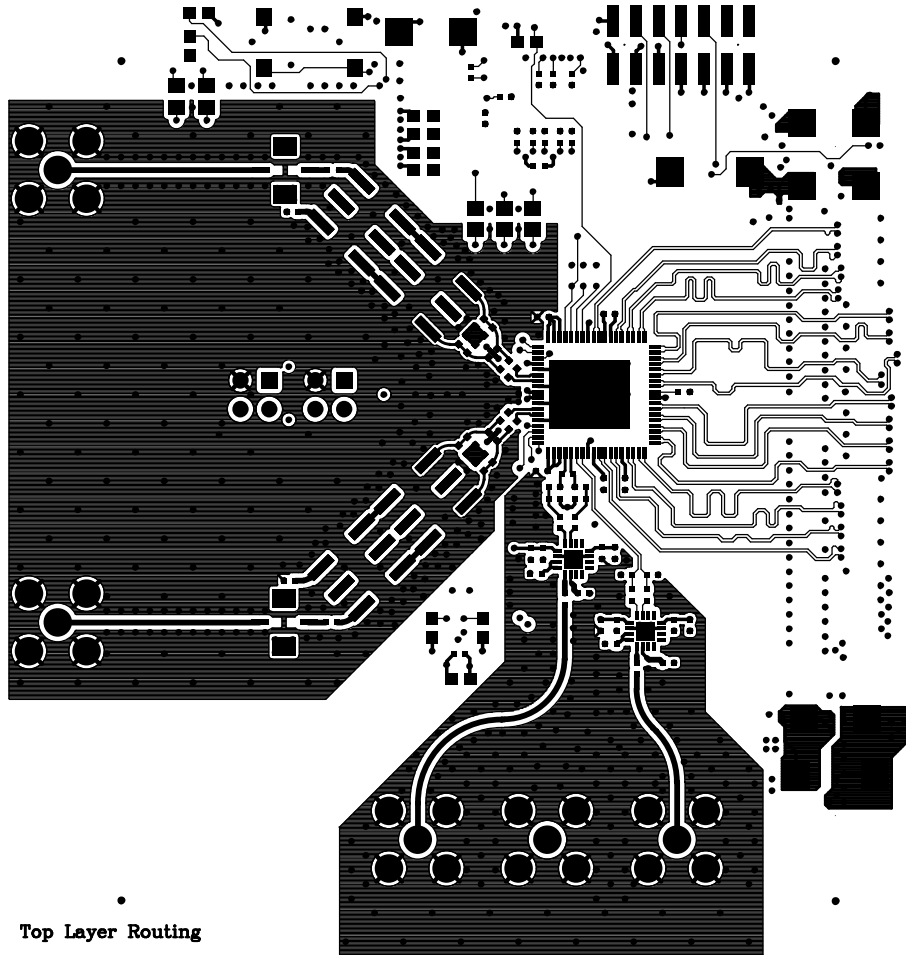


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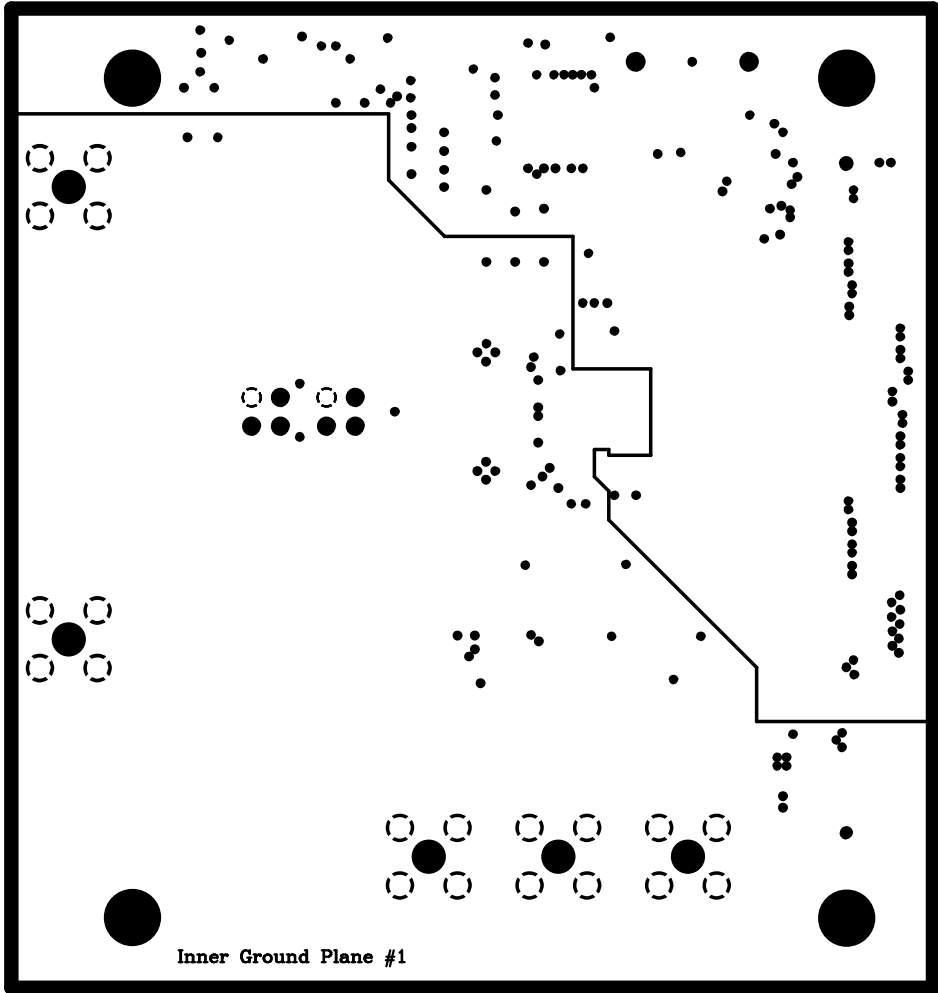
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 ISLA222IR72EV1Z REV A

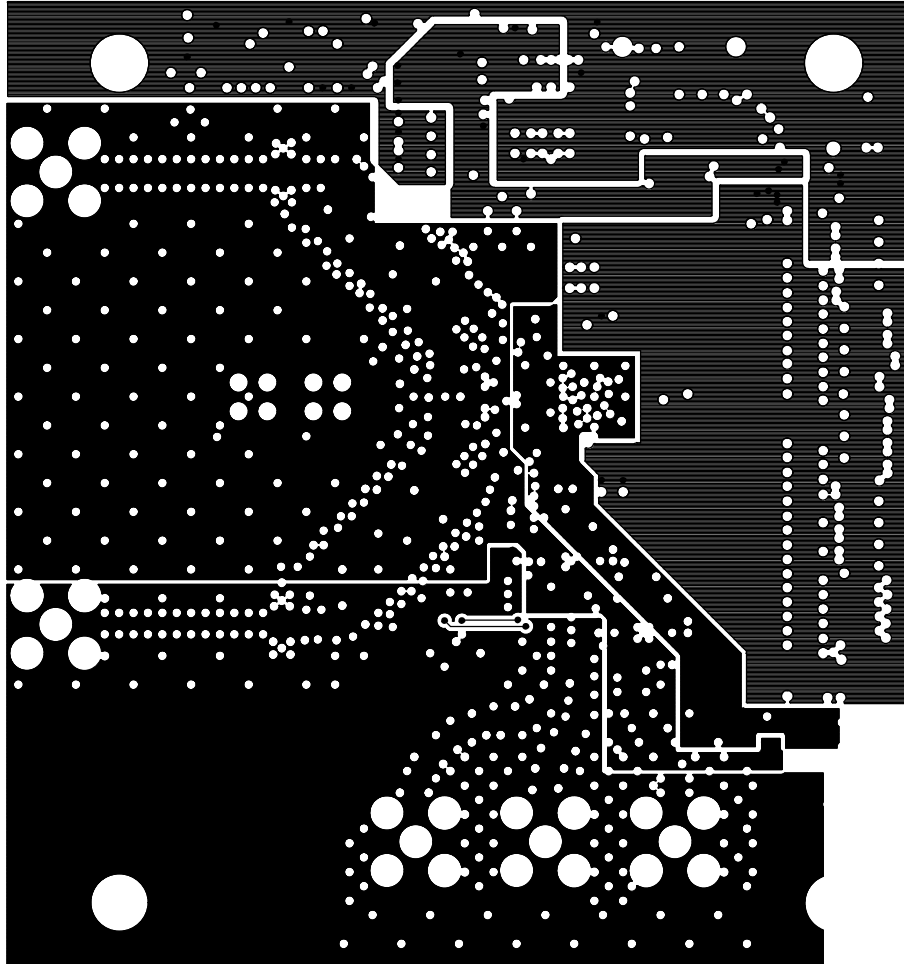
Top Silkscreen



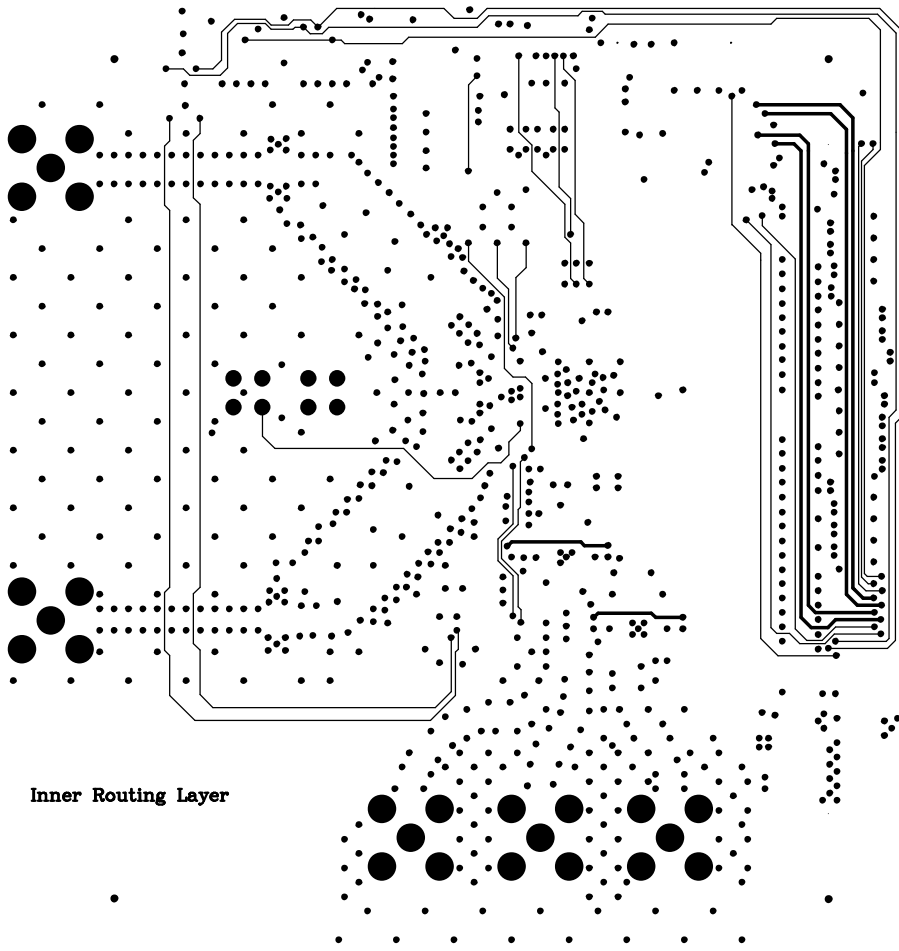


Top Layer Routing

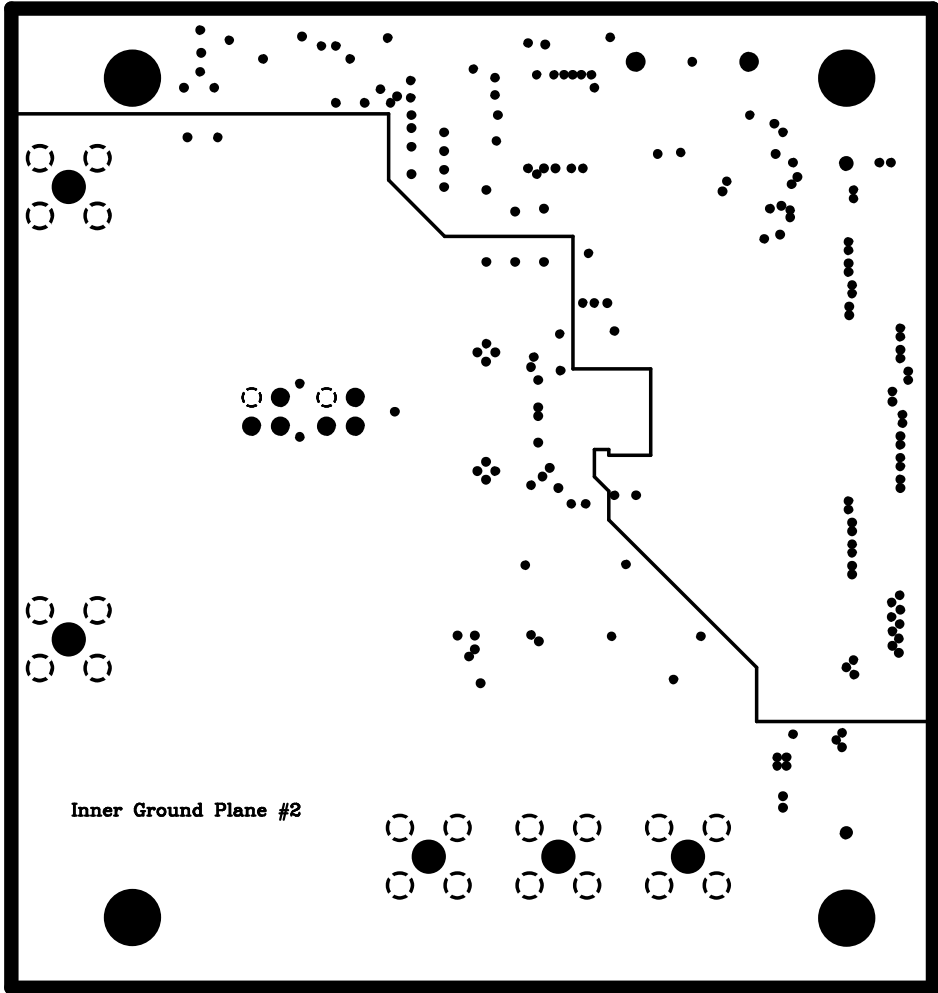


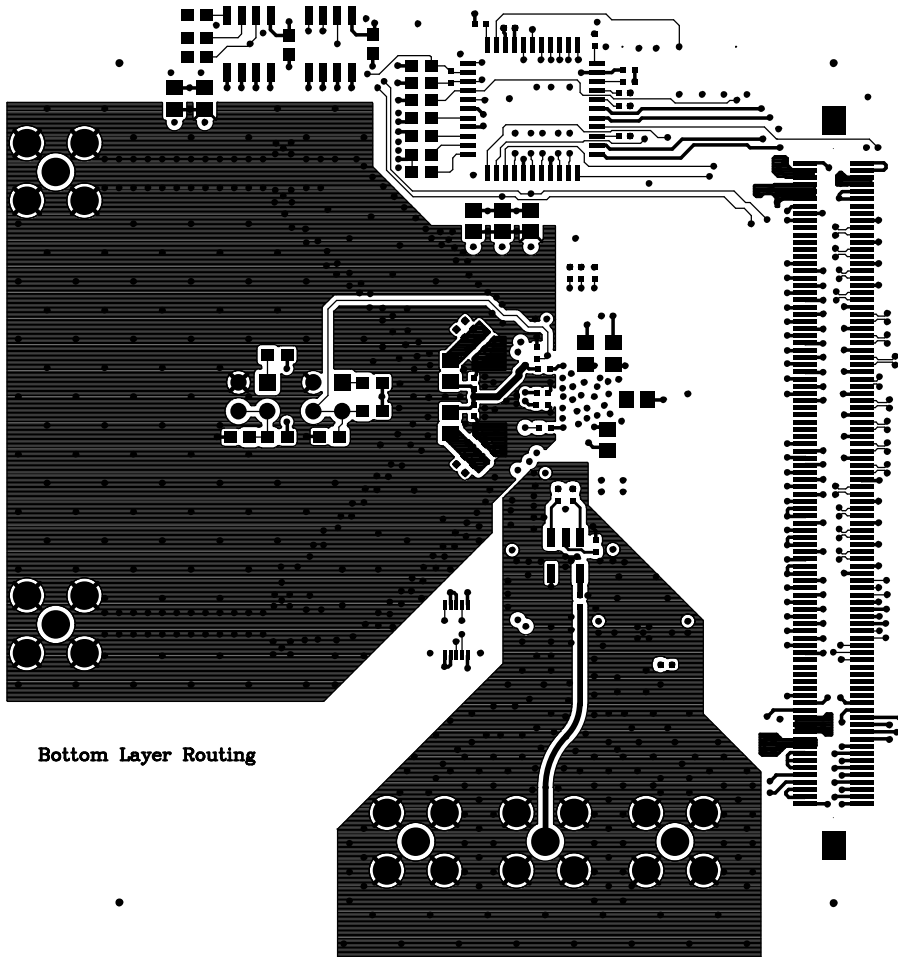


Split Power Plane



Inner Routing Layer





Bottom Layer Routing

Bottom Silkscreen

