

Integrated Device Technology, Inc. 6024 Silver Creek Valley Road, San Jose, CA - 95138

# PRODUCT/PROCESS CHANGE NOTICE (PCN)

TROD	CC1/1 ROCESS CI	THIOLICE (LCII)		
PCN #: <b>A1504-03</b>	DATE: 18-Aug-2015	MEANS OF DISTINGUISHING CHANGED DEVICES:		
19mm x 19r 31mm x 31r Refer to Attachment II	nm PBGA-240 nm PBGA-324 nm PBGA-640 for the affected part numbers	☐ Product Mark ☐ Back Mark ☐ Date Code Lot # will have: ☐ Other "P" prefix for ATP, Philippines		
	8-Nov-2015	<u> </u>		
Contact: IDT PCN DESI	X .	Attachment: Yes No		
E-mail: pcndesk@idt.c	<u>com</u>	Samples: Please contact your local sales representative for sample request.		
DESCRIPTION AND PURPOSI	E OF CHANGE:			
Die Technology Wafer Fabrication Process Assembly Process Equipment Material Testing Manufacturing Site Data Sheet Other  Die Technology Wafer Fabrication Process This notification is to advise our customers that IDT is transferring the affected products assembled at Amkor, Korea (ATK) to Amkor Philippines (ATP) as ATK will discontinue their assembly tooling for this product.  There is no change to the assembly material sets and no change to the moisture performance.  Attachment I details the qualification results and Attachment II shows the affected list of part numbers.				
RELIABILITY/QUALIFICATI Refer to qualification data shown				
to grant approval or request addit it will be assumed that this change	uire written notification of this cha ional information. If IDT does not e is acceptable. her version manufactured after the	inge. Please use the acknowledgement below or E-Mail receive acknowledgement within 30 days of this notice process change effective date until the inventory		
Customer:	⊏	Approval for shipments prior to effective date.		
Name/Date:	E-	Mail Address:		
Title:	Ph	none# /Fax# :		
CUSTOMER COMMENTS:				
IDT ACKNOWLEDGMENT O	E DECEIDT.			
	r neceiri;			
RECD. BY:		DATE:		

Integrated Device Technology, Inc. 6024 Silver Creek Valley Road, San Jose, CA - 95138

# PRODUCT/PROCESS CHANGE NOTICE (PCN)

**ATTACHMENT I - PCN # : A1504-03** 

PCN Type: Manufacturing Site - Transfer Assembly Location

**Data Sheet Change:** None

**Detail Of Change:** 

This notification is to advise our customers that IDT is transferring the affected products assembled at Amkor, Korea (ATK) to Amkor, Philippines (ATP) as ATK will discontinue their assembly tooling for this product. Presently, ATP is a qualified IDT Subcontractor.

The material set details of the current and new assembly location is as shown in Table 1. The die attach and mold compound used at the new assembly are qualified IDT materials. There is no change from the existing qualified substrate material, solder ball material, and wire for the new assembly location.

There is no change to the moisture performance.

Table 1: Assembly Material Sets for The Existing and New Assembly Locations

	Existing Assembly: ATK	New Assembly: ATP
Die Attach	Ablestik 2300	Ablestik 2300
Wire	Au wire	Au wire
Mold Compound	EME G770, Nitto GE100L	EME G770, Nitto GE100L
Solder Ball	63Sn37Pb (Standard) Sn96.5/Ag3.0/Cu0.5 (Green)	63Sn37Pb (Standard) Sn96.5/Ag3.0/Cu0.5 (Green)

## PRODUCT/PROCESS CHANGE NOTICE (PCN)

#### **ATTACHMENT I - PCN # : A1504-03**

#### **Qualification Information and Qualification Data:**

**Affected Packages:** PBGA-240, 324, 640

**Assembly Material:** The affected package type is using ATP standard materials shown on page 2 of

this attachment.

**Qual Plan & Results:** Tests are in accordance with JEDEC47 recommended tests.

**Qualification Vehicle:** 31mm x 31mm PBGA-640 (1 lot)

35mm x 35mm PBGA-352 (2 lots)

Test Description	Test Method	Test Results (Rej / SS)
* HAST - unbiased (130 °C/85% RH, 96 Hrs)	JESD22-A118	0/25, 0/25, 0/25
* Temperature Cycling (-55°C to 125°C, 700 cycles)	JESD22-A104	0/25, 0/25, 0/25
High Temperature Storage Bake (150°C, 1000 Hrs)	JESD22-A103	0/25, 0/25, 0/25

<sup>\*</sup> Tests were subjected to Preconditioning per JESD22-A113 prior to stress test

# PRODUCT/PROCESS CHANGE NOTICE (PCN)

### ATTACHMENT II - PCN #: A1504-03

#### **Affected Part Numbers**

Part Number	Part Number	Part Number	Part Number
82P2828BHG	72T7285L4-4BB	72T36125L5BB	72T18125L5BBI
72T72115L5BBI	82P2828BH	72T18125L4-4BBG	72T36125L4-4BBG
72T72115L5BBGI	82P2821BHG	72T18125L4-4BB	72T36125L4-4BB
72T72115L5BB	82P2821BH	72T18125L10BB8	72T36125L10BB
72T72115L4-4BBG	82P2521BHG	72T18125L10BB	72T36115L6-7BB
72T72115L4-4BB	82P2521BH-ECI	72T18115L6-7BB	72T36115L5BBI
72T72115L10BB	82P2521BH	72T18115L5BBI	72T36115L5BB
72T72105L6-7BB	72T7295L6-7BB	72T18115L5BB	72T36115L4-4BBG
72T72105L5BBGI	72T7295L5BB	72T18115L4-4BB	72T36115L4-4BB
72T72105L5BB	72T7295L4-4BBG	72T18115L10BB	72T36115L10BB
72T72105L4-4BBG	72T7295L4-4BB	72T18105L6-7BB	72T36105L6-7BB
72T72105L4-4BB	72T7295L10BB	72T18105L5BBI	72T36105L5BBI
72T72105L10BB	72T7285L6-7BB	72T18105L5BBGI	72T36105L5BB
72T6360L7-5BBG	72T7285L5BBG	72T18105L5BB	72T36105L4-4BB
72T36125L6-7BB	72T7285L5BB	72T18105L4-4BBG	72T36105L10BB
72T36125L5BBI	72T7285L4-4BBG	72T18105L4-4BB	72T18125L6-7BB
72T72115L6-7BB	72T36125L5BBGI	72T18125L5BB	72T18105L10BB
72T7285L10BB	72T36125L5BBG	72T18125L5BBGI	

		Current Site	New Site
	Pkg and Si Attribute	ATK	ATP
	Pkg type	TEPBGA	TEPBGA
Pkg	Pkg x & y (mm)	31mm x 31mm	31mm x 31mm
	Pkg z (mm)	2.23mm	2.23mm
	Max Voltage	1.8V	1.8V
	Capacitors	NA	NA
	Si Process	1P6M	1P6M
	Wafer Size	8"	8"
	Die size (mm2)	9.5mm x 10.32mm	9.5mm x 10.32mm
	Die Aspect Ratio	1.1	1.1
	Die thickness (mils)	10	10
	Polyimide (Y/N)	N	N
	Silicon Metal Layers	6 metal layers	6 metal layers
_	Scribe Width (um)	0.22um to 0.44um	0.22um to 0.44um
교	UBM source	NA	NA
Silicon & FL	Silicon UBM Stack-up	NA	NA NA
o u	Bump source	NA	NA
<u>:</u>	Bump pitch	NA NA	NA NA
Si	Total Bump count	NA	NA
	Bump Diameter	NA NA	NA NA
	Bump Height	NA	NA NA
	Bump Metallurgy	NA NA	NA
	Wafer Bump Flux	NA NA	NA NA
	CAM Flux	NA NA	NA
	Underfill Material	NA	NA
	Silicon UBM/SRO	NA NA	NA NA
	Halogen Free ?	Yes	Yes
	Substrate Layers	4	4
	Substrate thickness	0.56mm	0.56mm
	Core thickness (um)	150	150
	Core Material	HL832NX-A	HL832NX-A
	Outer layer Lines/space	55 /60	55 /60
	Bump Pre-solder (SOP)	NA	NA
	Bump presolder (SOP)	NA NA	NA
Substrate	Bump Capture Pad/SRO IO	450	450
stra	Substrate Ball Capture	600	600
ä	Number of PTH/M1-M2	662	662
ง	Core PTH/Capture pad	350/400	350/400
	Substrate Design Rule &	NA	NA
	Substrate Supplier	Samsung	Samsung
	Build up layer (thickness)	NA	NA
	Solder mask (thickness)	Top: 0.02mm min.	Top: 0.02mm min.
	C1 & C4 thickness (plate)	12um	12um
	C2 & C3 thickness (foil +	18um	18um
	Surface finish (thickness)	NiPdAu	NiPdAu
	2nd level Ball count	640	640
	2nd level BA Flux	WS609	WS609
	2nd Ball Dia (mm)	0.635	0.635
SLI			
	2nd level metallurgy	sac305	sac305
	2nd level ball pitch (mm)	1	1