

**EXAMPLE OF CAPACITOR  
PLACEMENT  
RH850/U2C4, U2C2 HLQFP144**

r01an7914jj0100-rh850u2c

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# 1. DECOUPLING CAPACITORS

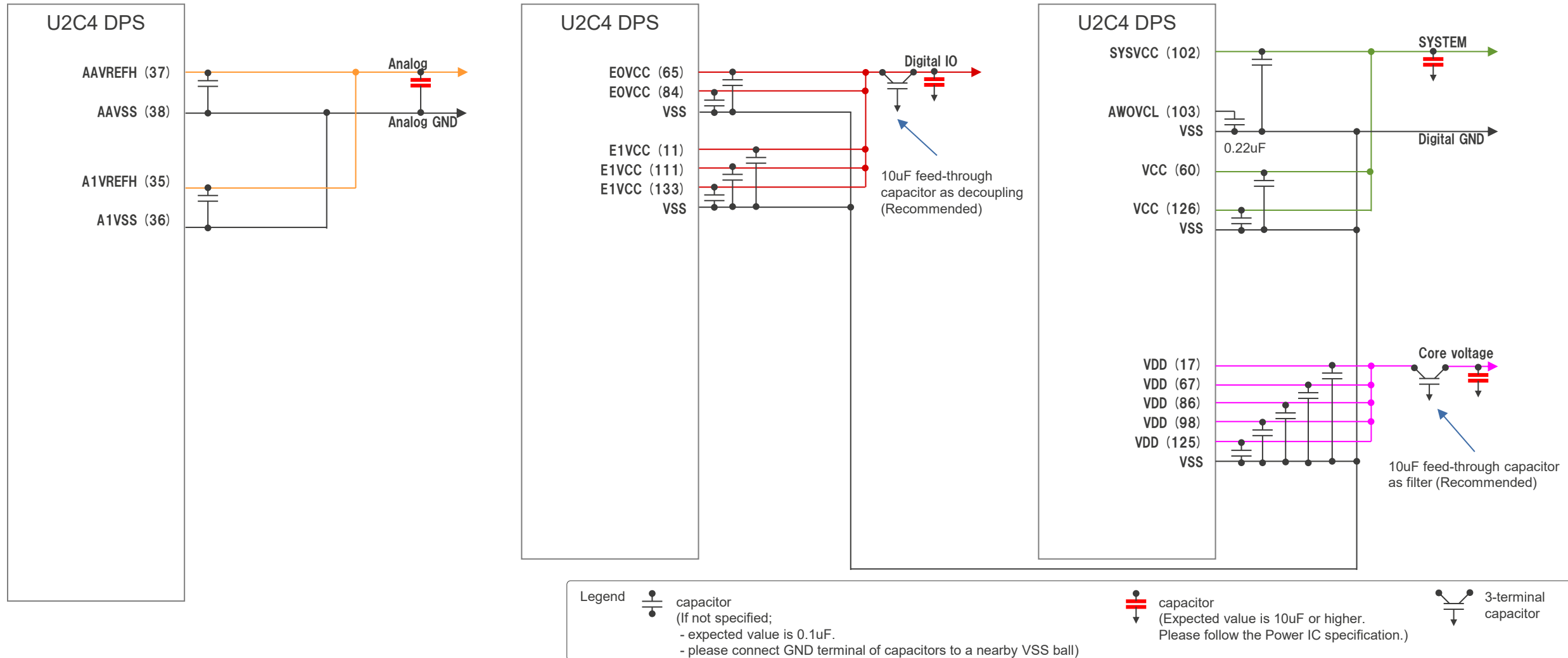
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- Capacitor placement and number of capacitors: Please refer page 4 to 6.
  - Capacitors has been kept as close as feasible to the related supply pin.
  
- Types of capacitors:
  - 0.1uF, 0.22uF, 10uF or higher\*1 ceramic capacitor (Low ESR/ESL is required)  
\*1: This is expected value. Please follow the Power IC specification.
  - 10uF 3-terminal ceramic capacitor (Very low ESR/ESL is required)
  
- 3-terminal capacitor
  - 3-terminal capacitor is recommended for reduction of radiation noise.

# 2. EXAMPLE OF CAPACITOR PLACEMENT

## 2.1 U2C4 DPS HLQFP144

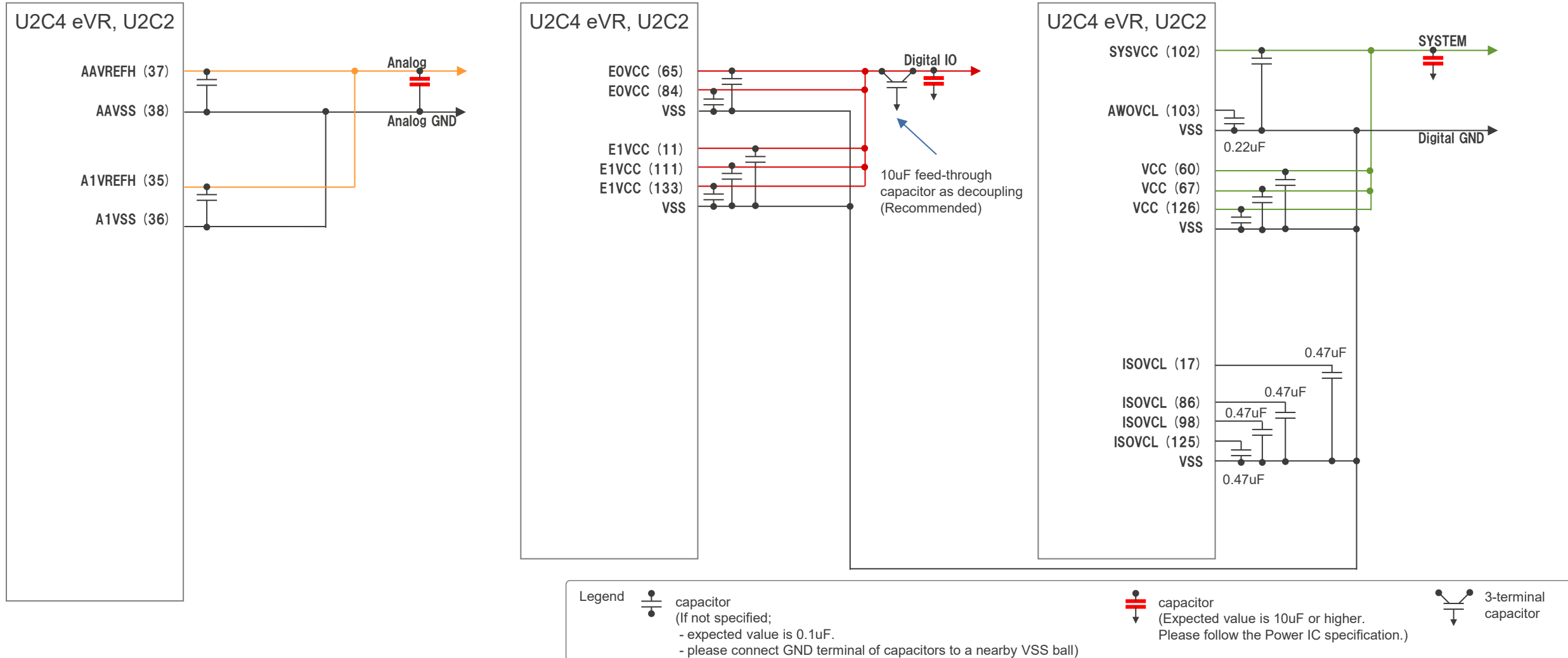
Example capacitor connection for U2C4 DPS HLQFP144 package.



# 2. EXAMPLE OF CAPACITOR PLACEMENT

## 2.2 U2C4 EVR HLQFP144 (VCC=3.3V), U2C2 HLQFP144

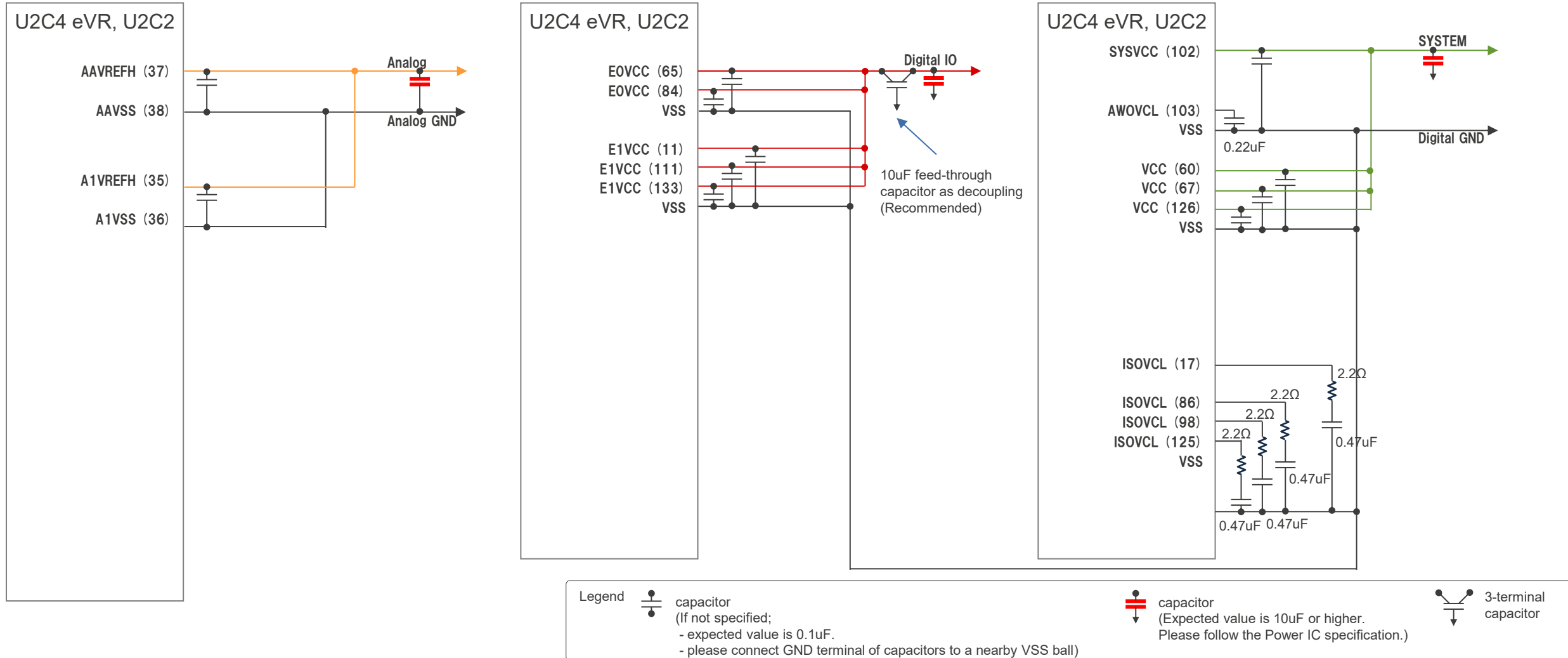
Example capacitor connection for U2C4 eVR HLQFP144 package on VCC=3.3V condition and U2C2 HLQFP144 package.



# 2. EXAMPLE OF CAPACITOR PLACEMENT

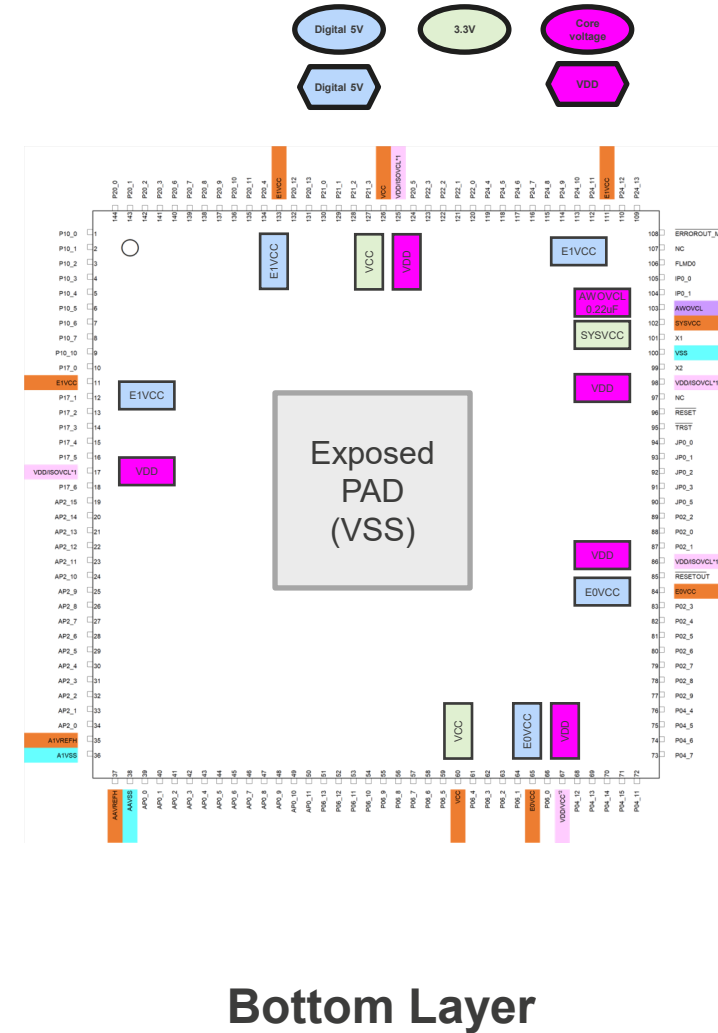
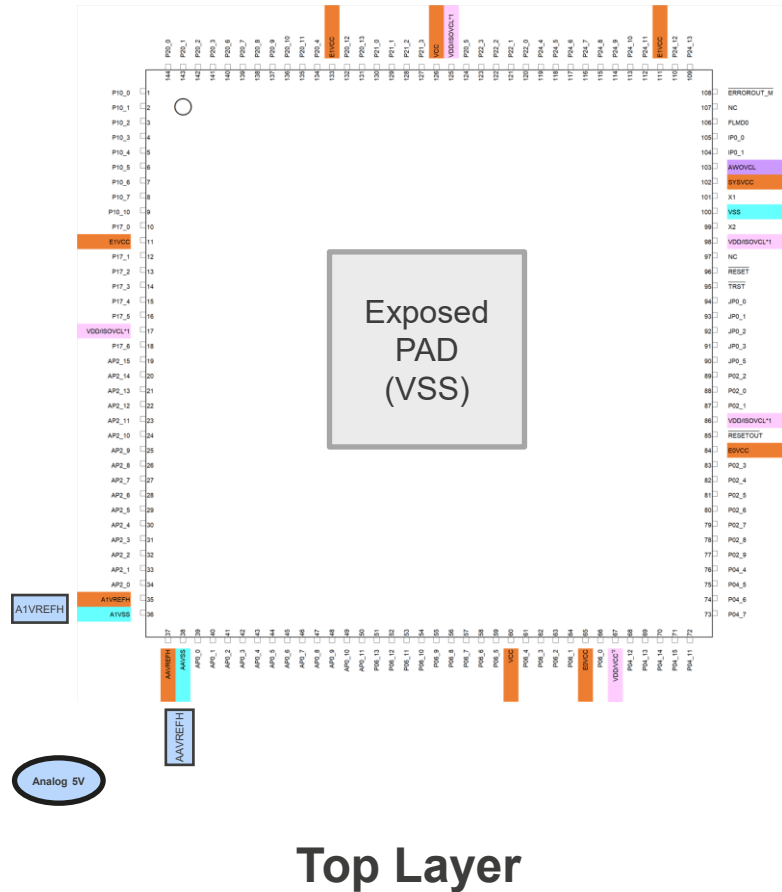
## 2.3 U2C4 EVR HLQFP144 (VCC=5V)

Example capacitor connection for U2C4 eVR HLQFP144 package on VCC=5V condition.



# 3. PCB LAYOUT GUIDELINES -TOP LAYER / BOTTOM LAYER-

## 3.1 Example capacitor placement for U2C4 DPS HLQFP144 package



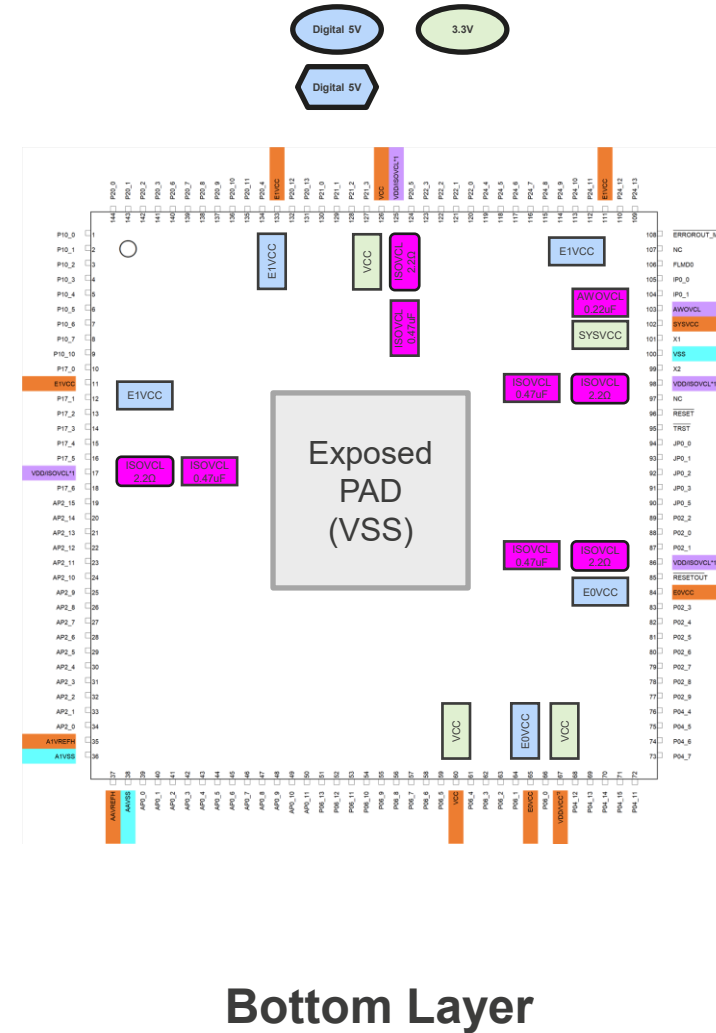
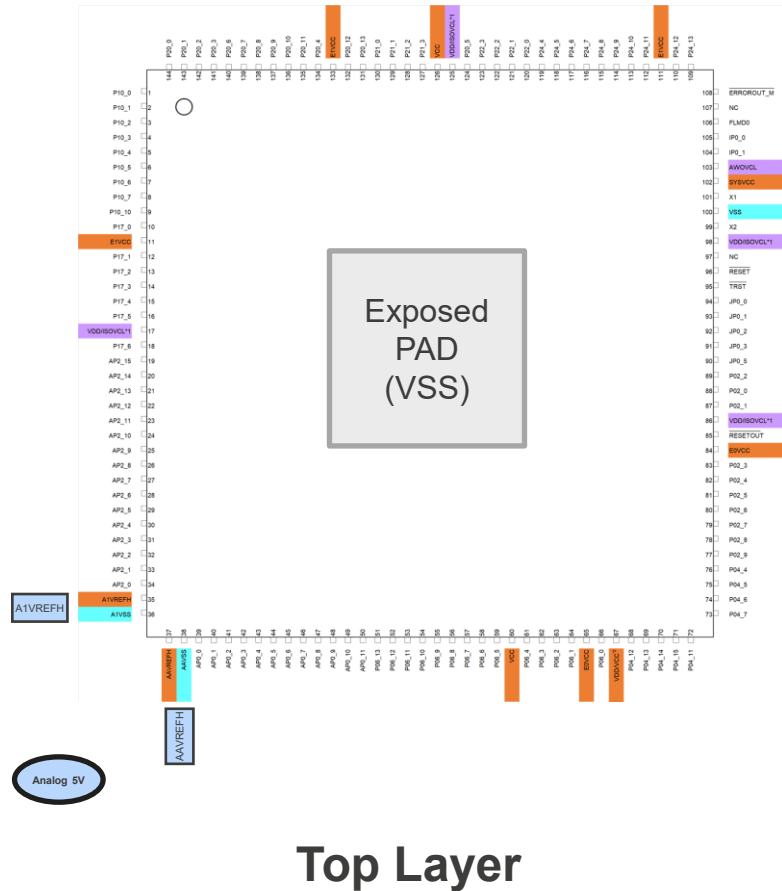
**Legend**

- capacitor (analog, Digital IO) (The capacitance is 0.1uF if not specified.)
- capacitor (system) (The capacitance is 0.1uF if not specified.)
- capacitor (Core voltage) (The capacitance is 0.1uF if not specified.)
- capacitor (analog, Digital IO) (Expected value is 10uF or higher. Please follow the Power IC specification.)
- capacitor (system) (Expected value is 10uF or higher. Please follow the Power IC specification.)
- capacitor (Core voltage) (Expected value is 10uF or higher. Please follow the Power IC specification.)
- 3-terminal capacitor (analog, Digital IO)
- 3-terminal capacitor (Core voltage)



# 3. PCB LAYOUT GUIDELINES -TOP LAYER / BOTTOM LAYER-

## 3.3 Example capacitor placement for U2C4 eVR HLQFP144 package on VCC=5V condition.



**Legend**

- capacitor (analog, Digital IO) (The capacitance is 0.1uF if not specified.)
- capacitor (system) (The capacitance is 0.1uF if not specified.)
- capacitor (Core voltage) (The capacitance is 0.1uF if not specified.)
- capacitor (analog, Digital IO) (Expected value is 10uF or higher. Please follow the Power IC specification.)
- capacitor (system) (Expected value is 10uF or higher. Please follow the Power IC specification.)
- capacitor (Core voltage) (Expected value is 10uF or higher. Please follow the Power IC specification.)
- 3-terminal capacitor (analog, Digital IO)
- 3-terminal capacitor (Core voltage)
- Resistor (Core voltage)

# U2C4 DPS QFP144 パソコン及びVIA配置例



1層 端子接続線

2層 EVCC供給

3層 GND  
(非表示)  
発振回路の  
直下は抜き  
パターン

4層 VSS配線

2層VDD供給

4層 GND (発振回路)

2層VCC供給

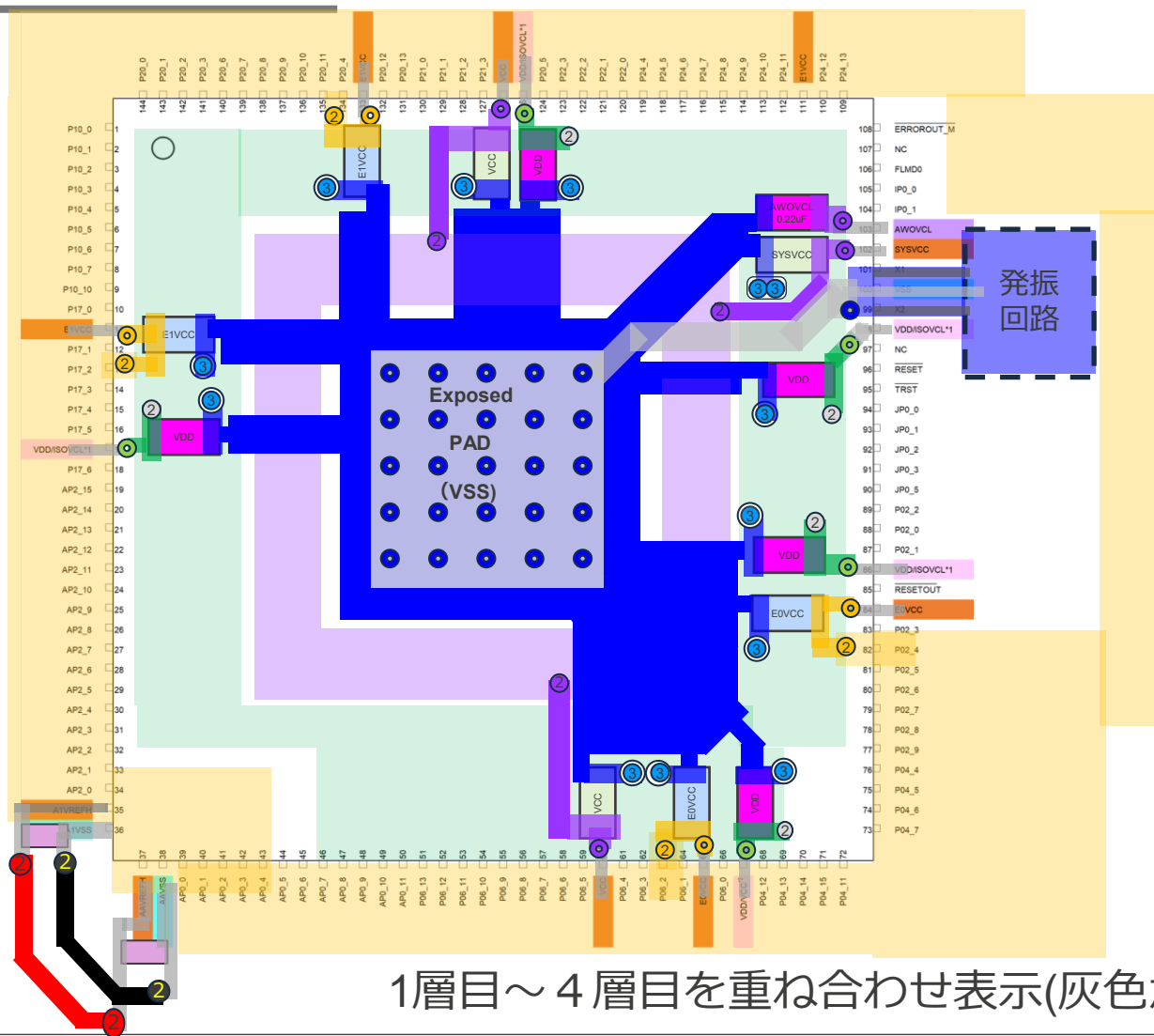
4層 EVCC配線

2層Analog

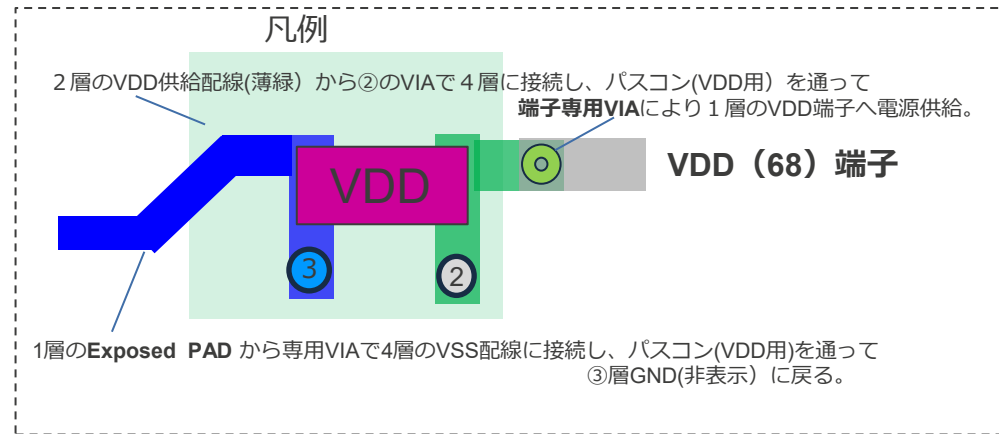
4層 VDD配線

2層Analog-GND

4層 VCC配線



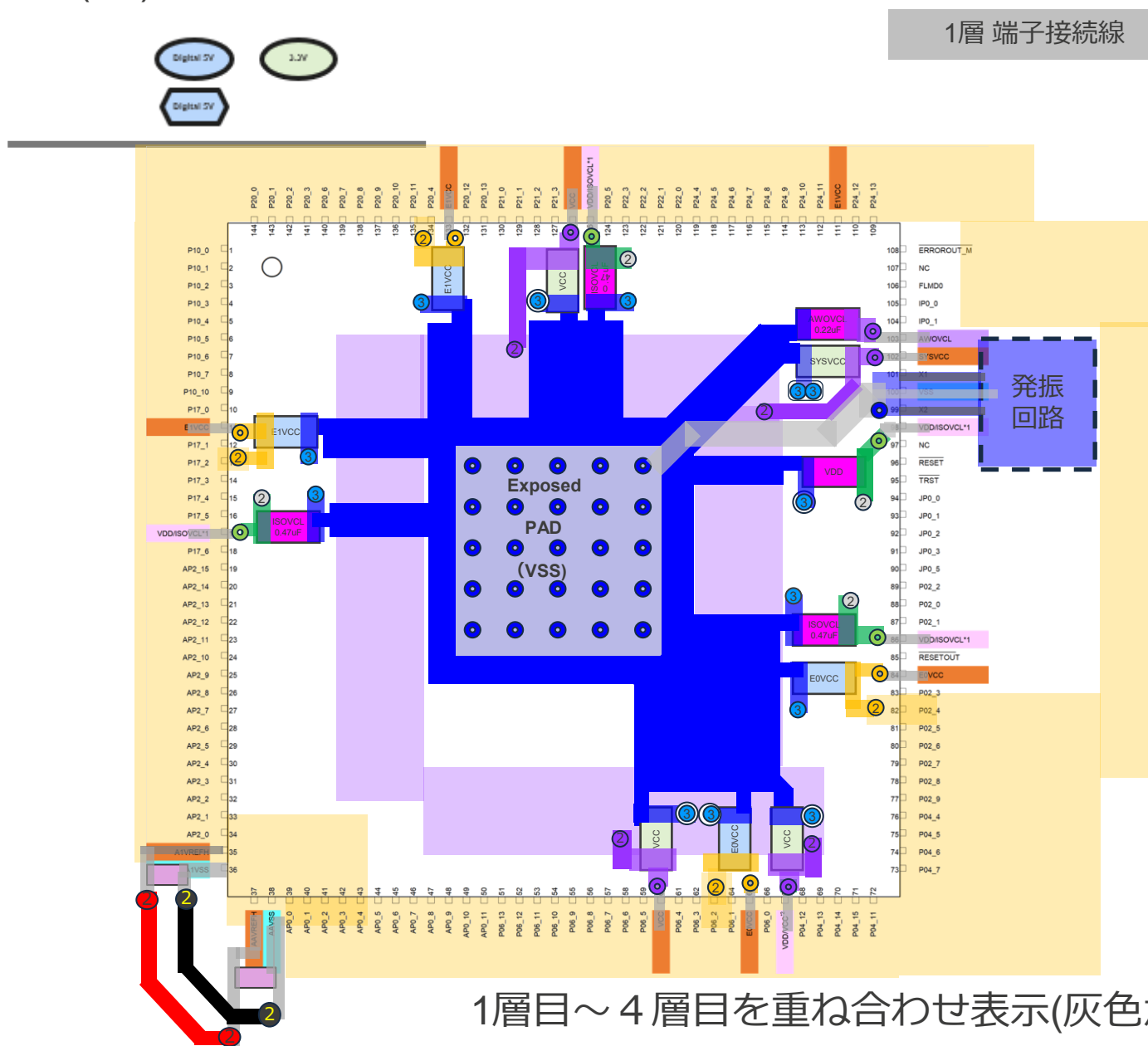
◎内層の電源/グランド層と接続しないVIA  
○内の数字は4層と各VIAの接続



- 緑 : VDD
- 紫 : System(VCC/SYSVCC)電源
- 赤 : Analog(AxVCC)電源
- 黄色 : Digital IO(ExVCC)電源
- 青 : VSS

1層目～4層目を重ね合わせ表示(灰色が1層目、カラーが2層目、4層目)

# U2C4(3V)/U2C2 eVR QFP144 パソコン及びVIA配置例



1層 端子接続線

2層 EVCC供給

3層 GND  
(非表示)  
発振回路の  
直下は抜き  
パターン

4層 VSS配線

4層 GND (発振回路)

4層 EVCC配線

4層 ISOVCL配線

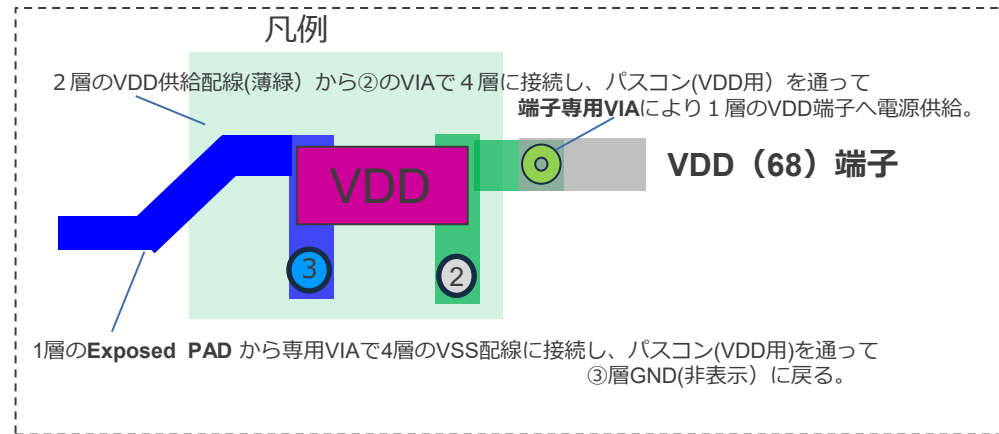
4層 VCC配線

2層VCC供給

2層Analog

2層Analog-GND

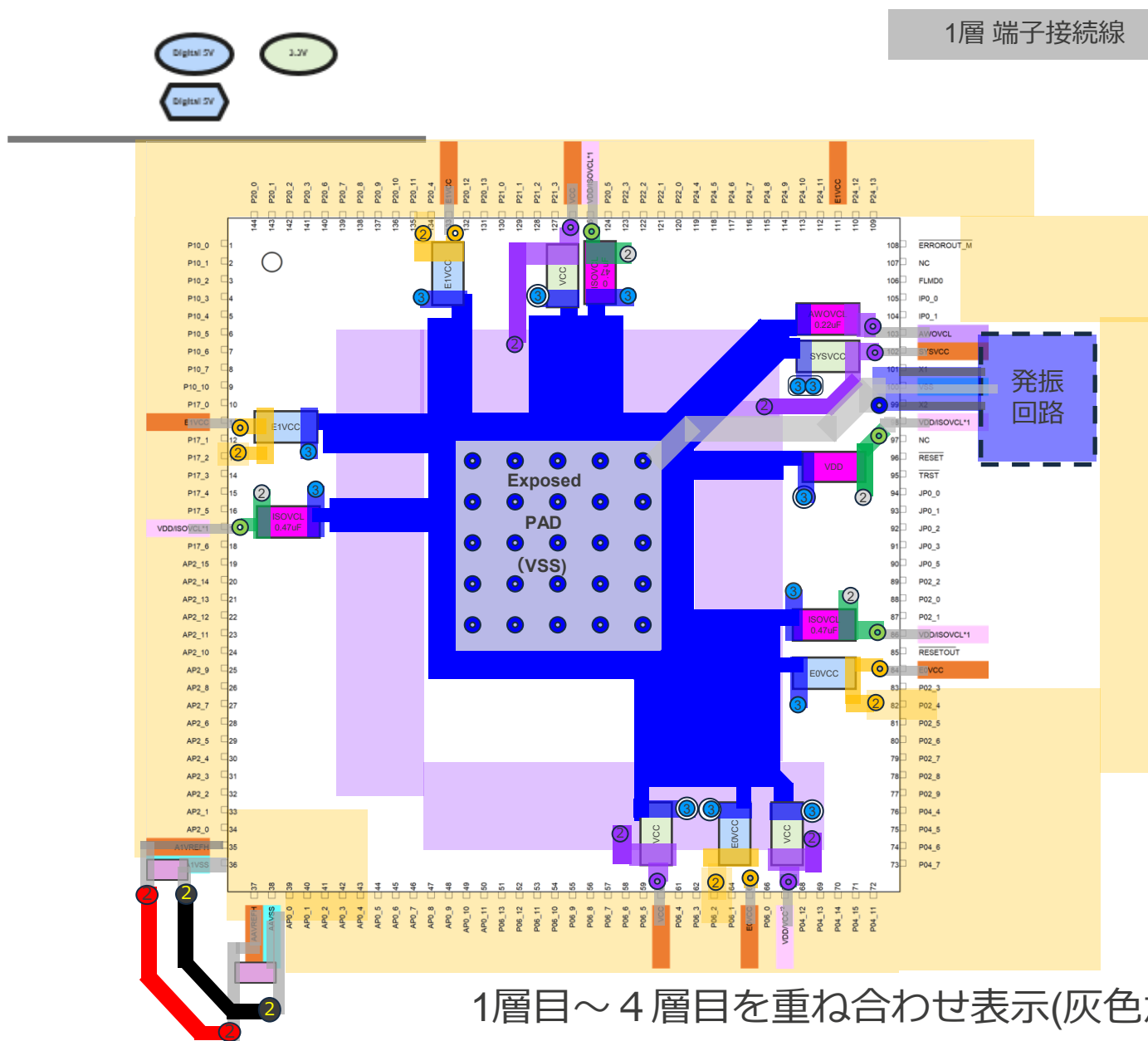
◎内層の電源/グランド層と接続しないVIA  
○内の数字は4層と各VIAの接続



- 緑 : ISOVCL
- 紫 : System(VCC/SYSVCC)電源
- 赤 : Analog(AxVCC)電源
- 黄色 : Digital IO(ExVCC)電源
- 青 : VSS

1層目～4層目を重ね合わせ表示(灰色が1層目、カラーが2層目、4層目)

# U2C4(3V)/U2C2 eVR QFP144 パソコン及びVIA配置例



1層 端子接続線

2層 EVCC供給

3層 GND  
(非表示)  
発振回路の  
直下は抜き  
パターン

4層 VSS配線

4層 GND (発振回路)

4層 EVCC配線

4層 ISOVCL配線

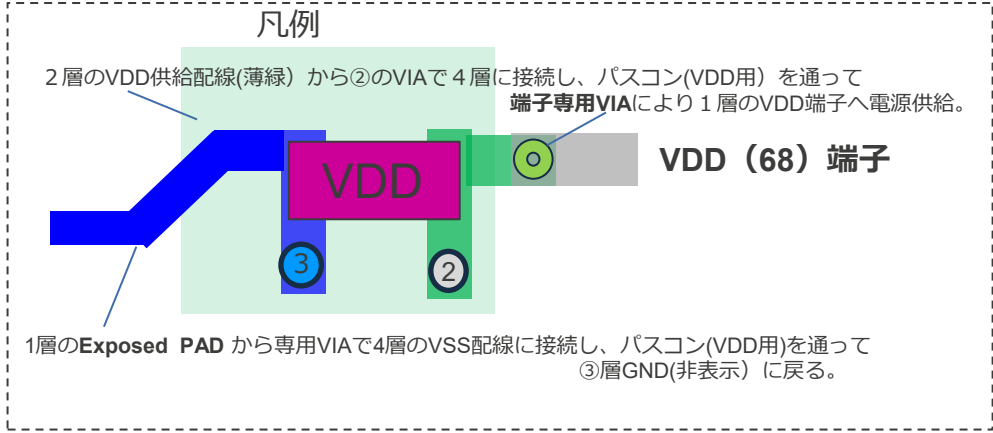
4層 VCC配線

2層VCC供給

2層Analog

2層Analog-GND

◎内層の電源/グランド層と接続しないVIA  
○内の数字は4層と各VIAの接続



- 緑 : ISOVCL
- 紫 : System(VCC/SYSVCC)電源
- 赤 : Analog(AxVCC)電源
- 黄色 : Digital IO(ExVCC)電源
- 青 : VSS

1層目～4層目を重ね合わせ表示(灰色が1層目、カラーが2層目、4層目)

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