User's Manual

V850 JTAG OCD Checker

User's Manual

Supported Devices:
V850 Family

Renesas Electronics
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(2012.4)

Contents

1. Overview

V850 JTAG OCD Checker is Emulator Utility software for V850 for simply testing the PC-connected OCD emulator (QB-V850MINI(L) , IE-V850E1-CD-NW, E1 Emulator, E20 Emulator) and the target CPU operation.

1.1 Details of tested items

This section describes the test items that are performed by the V850 JTAG OCD Checker.

♦ **Emulator test**

OCD Emulator connection, initialization, and target CPU register read/write are checked.
The test results can be output to the log viewer and a log file.

- **Connect Test**

  OCD Emulator is started up and the connection with the target CPU is tested.

- **DCU Reg Test**

  0x00000000, 0xFFFFFFFF, 0x55555555, 0xAAAAAAAA, 0x33333333, and 0xCCCCCCCC are written in that order to the monitor register in the on-chip debug unit and the values are read to check if they have been read/written normally.

- **CPU Reg Test**

  A target CPU register read/write test is performed using the monitor program.
  (Target CPU registers: r1, r2, r3/sp, r4/gp, r5, r6, r7, r8, r9, r10, r11, r12, r13, r14, r15, r16, r17, r18, r19, r20, r21, r22, r23, r24, r25, r26, r27, r28, r29, r30/ep, r31/lp, eipc, eipsw, fepc, fepsw, psw, ctpc, ctpsw, dbpc, dbpsw, ctbp, asid, DIR, BPC0, BPAV0, BPAM0, BPDV0, BPDM0, BPC1, BPAV1,BPAM1, BPDV1, BPDM1, and pc)

  Release the security setting using the ID code before accessing a register, if necessary.

- **Test All**

  Connect Test, DCU Reg Test, and CPU Reg Test is performed in that order.

♦ **DCK waveform test**

The data set from OCD Emulator is output to the DDI signal in order to check the waveform of the DCK signal on the target system with an oscilloscope.

1.2 Test result

The results of the tests in **Emulator Test** are output to the log viewer and a log file. If the test results are NG, refer to **5. Corrective Actions in Case of NG** for general causes and corrective actions.

2. How to Startup

2.1 V850 JTAG OCD Checker startup

Start the V850 JTAG OCD Checker.

- Apply power to the OCD emulator and then the target board.
- Terminate Debugger if it is active.

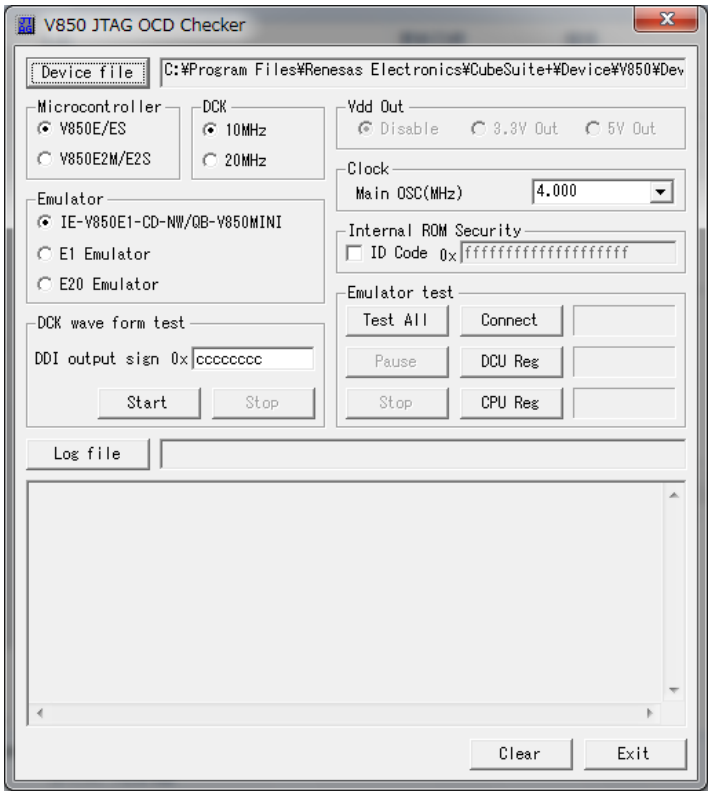


Figure 1. V850 JTAG OCD Checker Main Dialog Box

2.2 Preparation of V850 JTAG OCD Checker

(1) Click the [Device file] button and specify the device file corresponding to the target device used.

(2) Select the core series for target CPU in the **Microcontroller** area.
Please choose either [V850E/ES] core series or [V880E2M/E2S] core series.

(3) Select the JTAG Clock(DCK) in the **DCK** area.
Selection is required only when [V850E/ES] core series in the **Microcontroller** area is chosen.

(4) Select the OCD Emulator in the **Emulator** area.

- IE-V850E1-CD-NW/QB-V850MINI : When using with IE-V850E1-CD-NW and QB-V850MINI(L)
- E1 Emulator : When using with E1 Emulator
- E20 Emulator : When using with E20 Emulator

(5) Please choose from OCD Emulator the power supply supplied to target system.
Selection is required only when [E1 Emulator] in the **Emulator** area is chosen.

(6) Input the frequency of the main clock input to the device in the **Clock** area.
Selection is required only when [V850E/ES] core series in the **Microcontroller** area is chosen.

(7) When using a device having the security function in single-chip mode, check the "ID code" checkbox and input the ID code in the **Internal ROM Security** area.
When [V850E/ES] core series in the **Microcontroller** area is chosen: ID code is 10 bytes
When [V850E2M/E2S] core series in the **Microcontroller** area is chosen: ID code is 12 bytes
The **Connect** and **DCU Reg** tests are possible even if the ID code is not set.

2.3 Emulator test

(1) Click the [Test All] button.
Each item can be tested by clicking the [Connect], [DCU reg], or [CPU reg] button independently.

(2) When the test has finished, confirm that OK is displayed for each test item.
If NG is displayed, refer to **5 Corrective Actions in Case of NG**.

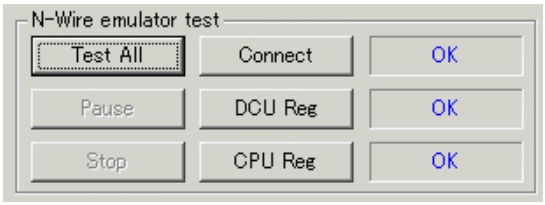


Figure 2. Display When All Test Results are OK

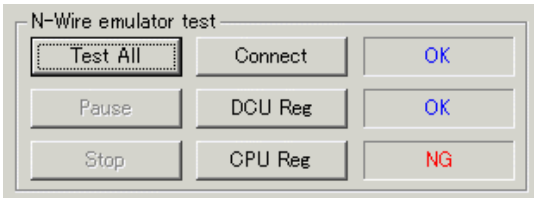


Figure 3. Display When Error Is Detected

2.4 DCK wave form test

(1) Connect the DCK signal of the target board to the oscilloscope probe.

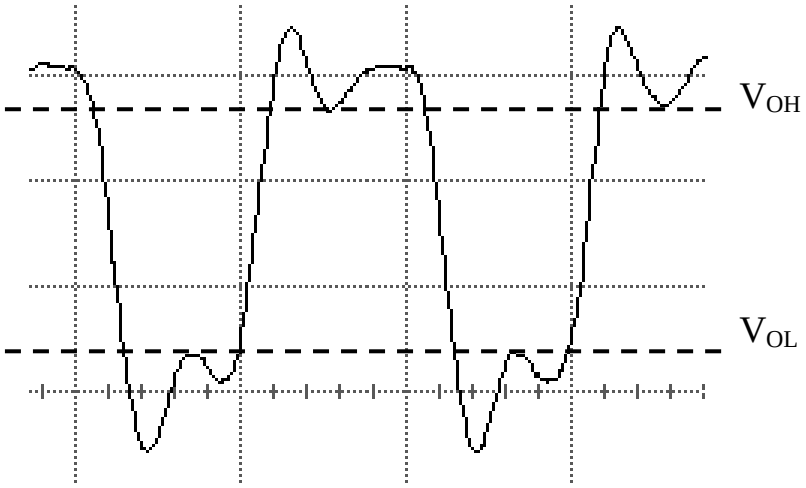
Remark Switch off the power supply of the OCD emulator and target system before performing this connection.

(2) Input 4-byte data (0xCCCCCCCC at shipment) in the **DDI output signal for oscilloscope** area and then click the [Start] button.
This function can be used, when [V850 E/ES] is chosen in [Microcontroller] area and [IE-V850E1-CD-NW/QB-V850MINI] is chosen in [Emulator] area.

(3) Monitor the waveform on the oscilloscope.

(4) Check whether the waveform noise (reflection) is within the standard range below.

Remark If it is not within the standard range, refer to **5. Corrective Actions in Case of NG**.



VOH, VOL: Refer to the data sheet supplied with the emulator.

Caution The data is output from the lowermost bit.

Even if data from the target board changes, the same data is always output because data is shifted inside the emulator.

3. Explanation of Each Area and Button

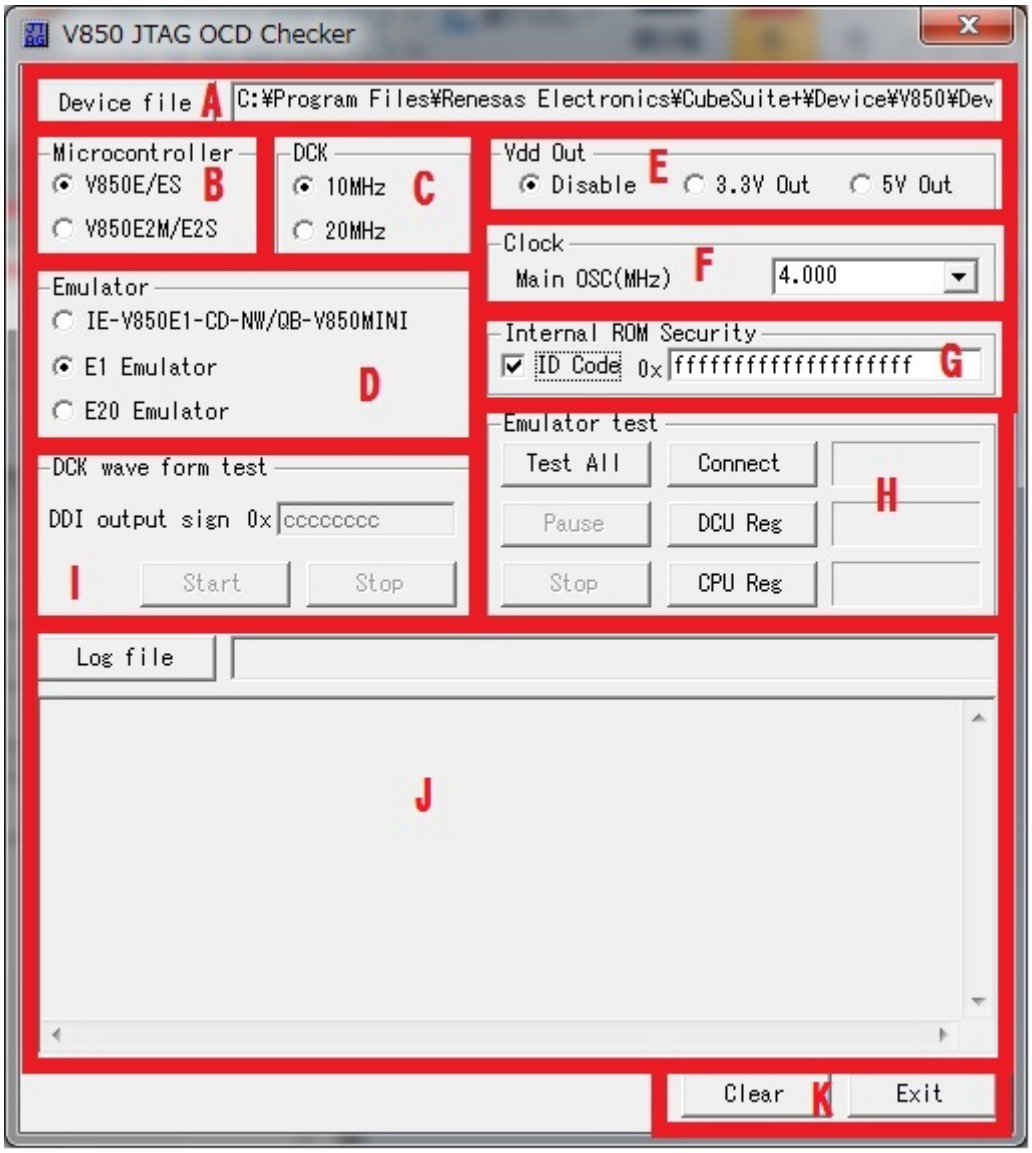


Figure 4. Areas in V850 JTAG OCD Checker Main Dialog Box

A. Operating environment setting area

Object	Function
[Device file] button	Displays the dialog box for specifying the device file name of the target CPU.
Text area	Displays the device file name of the target CPU and its path. Specify this at V850 JTAG OCD Checker startup.

B. Microcontroller selecting area

Object	Function
V850E/ES	Select this item when V850E/ES core series is used.
V850E2M/E2S	Select this item when V850E2M/E2S core series is used.

C. DCK selecting area

(Selection is required only when [V850E/ES] core series in the **Microcontroller** area is chosen.**)**

Object	Function
20MHz	Select this item when DCK = 20 MHz is set via the debugger.
10MHz	Select this item when DCK = 10 MHz is set via the debugger. ("DCK = 10 MHz" is the setting for the case where the V850 JTAG OCD Checker is used for the self-check board (supplied with the QB-V850MINI(L)) or for a device that does not operate unless DCK = 10 MHz, or for cases where the operation is unstable with DCK = 20 MHz, like when a long (2 m) N-Wire cable is used.)

D. Emulator selecting area

Object	Function
IE-V850E1-CD-NW/ QB-V850MINI	Select this item when the IE-V850E1-CD-NW or QB-V850MINI(L) is used.
E1 Emulator	Select this item when the E1 Emulator is used.
E20 Emulator	Select this item when the E20 Emulator is used.

E. Vdd Out selecting area

(Selection is required only when [E1 Emulator] in the **Emulator** area is chosen.**)**

Object	Function
Disable	Select this item when the IE-V850E1-CD-NW or QB-V850MINI(L) is used.
3.3V Out	Select this item when from OCD Emulator the power supply supplied to target system.(3.3V)
5V Out	Select this item when from OCD Emulator the power supply supplied to target system.(5V)

F. Main clock frequency setting area

(Selection is required only when [V850E/ES] core series in the **Microcontroller** area is chosen.**)**

Object	Function
Frequency setting area	Input the frequency of the main clock input to the device.

G. Internal ROM Security ID code specification area

Object	Function
ID code setting box	Check the check box when a device with the security function is used in the single-chip mode.
ID code setting area	Input an ID code when a product device with the security function is used in the single-chip mode.

H. OCD emulator test area

Object	Function
[Test All] button	Executes Connect, DCR Reg, and CPU Reg tests in sequence.
[Pause] button	Pauses the test. (Testing resumes when this button is clicked again.)
[Stop] button	Stops the test.
[Connect] button	Starts up the N-Wire emulator, opens communication with the target, and executes testing for initialization.
[DCU Reg] button	Performs testing for DCU register read/write.
[CPU Reg] button	Performs testing for CPU register read/write.

I. DCK waveform test area

Object	Function
DDI output signal for oscilloscope area	Sets the data of the DDI signal output from the OCD emulator. When a value of 0xffffffff or greater is set, an error occurs when the [Start] button is pressed.
[Start] button	Outputs the value (0 to 0xffffffff) specified in the DDI output signal for oscilloscope text area.
[Stop] button	Stops the signal for value testing specified in the DDI output signal for oscilloscope text area.

Object	Function
DDI output signal for oscilloscope area	Sets the data of the DDI signal output from the OCD emulator. When a value of 0xffffffff or greater is set, an error occurs when the [Start] button is pressed.
[Start] button	Outputs the value (0 to 0xffffffff) specified in the DDI output signal for oscilloscope text area.
[Stop] button	Stops the signal for value testing specified in the DDI output signal for oscilloscope text area.

J. Log viewer area

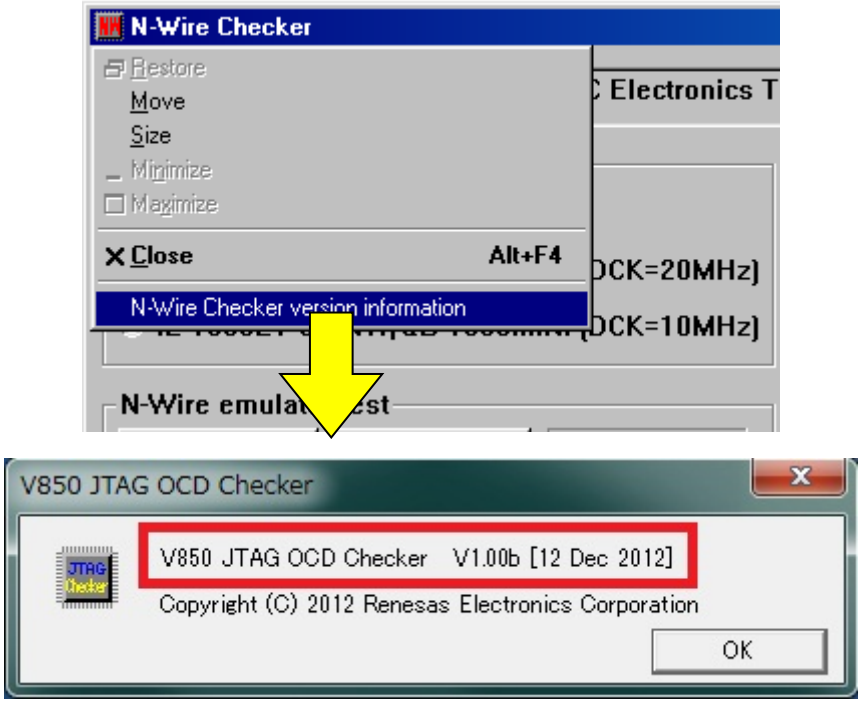
Object	Function
[Log file] button	Displays the dialog box for specifying the test result log file name. The log file is overwritten when the V850 JTAG OCD Checker is started up. A log file is created in the current folder when the file path name is not specified.
Text area	Displays the log file name and its path.
Log viewer area	Displays the test results as a log (up to approx. 21,000 characters). The same contents are output to the log file specified in the log file text area.

K. Other

Object	Function
[Exit] button	Terminates V850 JTAG OCD Checker.
[Clear] button	Clears the log viewer display. If a log file name is specified in the log file text area, the log file contents are not cleared.

4. Version Confirmation

Select the “V850 JTAG OCD Checker version information” menu on the system menu.



5. Corrective Actions in Case of NG

5.1 V850 JTAG OCD emulator test

The corrective actions for errors and corresponding error numbers are shown below.

Note that errors may occur due to causes other than those below.

5.1.1 When V850 E/V850ES is chosen

Note *1: Selection is required only when [E1 Emulator] in the **Emulator** area is chosen.

Italic font: Selection is required only when [IE-V850E1-CD-NW/QB-V850MINI] in the **Emulator** area is chosen.

No.	Error No.	Error Messages and Corrective Action
1	0x0100	**[Driver couldn't be opened.]** The PC and Emulator may be not connected. The PC may be not able to recognize after it has entered suspend mode, so restart the PC. The device driver may be not installed. Install the driver.
2	0x0105	**[Failed in reading device file (dxxxx.800).]** The necessary file may be damaged. Reinstall the device file.
3	0x0109	**[USB access failed.]** Exit this utility and re-connect up Emulator.
4	0x010a 0x01a6	**[EXEC already work.]** Exit the debugger.
5	0x01a0	**[Processing of a monitor was not completed to within a time.]** Confirm that the resonator oscillates normally. Confirm that the correct value is set to MainOSC. *Check the noise level using a DCK waveform test.* The problem may also be caused by an internal chip problem. Check the connection of the N-Wire I/F(DCK, DMS, DDI, DDO, DRST).
6	0x03a0	**[The Power supply of target is OFF.]** Check the target power supply. Check the cable connecting the Emulator and target board. Check that the VDD signal is input to the connector of the target board.
7	0x0400	**[Incorrect value of MainOSC.]** MainOSC can't be set to 0.
8	0x0B04	**[Although the power supply of target is ON, Vdd Out is set Enable.] (*1)** Set Vdd Out as Disable, or shut off the power supply of the target.
9	0x0c01	**[During access of register, CPU did timeout.]** Confirm that the resonator oscillates normally. Confirm that the correct value is set to MainOSC. *Check the noise level using a DCK waveform test.* The problem may also be caused by an internal chip problem. Check the connection of the N-Wire I/F(DCK, DMS, DDI, DDO, DRST).
10	0x0c02	**[During access of memory, CPU did timeout.]** Confirm that the resonator oscillates normally. Confirm that the correct value is set to MainOSC. *Check the noise level using a DCK waveform test.* The problem may also be caused by an internal chip problem. Check the connection of the N-Wire I/F(DCK, DMS, DDI, DDO, DRST).
11	0x0c03	**[During access of I/O register, CPU did timeout.]** Confirm that the resonator oscillates normally. Confirm that the correct value is set to MainOSC. *Check the noise level using a DCK waveform test.* The problem may also be caused by an internal chip problem. Check the connection of the N-Wire I/F(DCK, DMS, DDI, DDO, DRST).

No.	Error No.	Error Messages and Corrective Action
12	0x0c23	**[Bus hold under continuation.]** Confirm that the resonator oscillates normally. Confirm that the correct value is set to MainOSC. *Check the noise level using a DCK waveform test.* The problem may also be caused by an internal chip problem. Check the connection of the N-Wire I/F(DCK, DMS, DDI, DDO, DRST).
13	0x0c24	**[It couldn't shift to debug mode.]** Confirm that the resonator oscillates normally. Confirm that the correct value is set to MainOSC. Check the clock signal. This may be caused by a stopped clock or a slow clock. Check the connection of the N-Wire I/F(DCK, DMS, DDI, DDO, DRST).
14	0x0c2e	**[During access of flash memory information, CPU did timeout.]** Confirm that the correct device is selected. The problem may also be caused by an internal chip problem.
15	0x0c2f	**[During access of flash memory information, the response from CPU was not right.]** Confirm that the correct device is selected. The problem may also be caused by an internal chip problem.
16	0x0c35	**[IRAM cannot be accessed.]** Confirm that the correct device file(IRAM size) is selected.
17	0x0c43	**[Connection of Emulator couldn't be performed.]** *The switch setting may be wrong if a desktop computer is used and two or more PC cards are inserted.* Check the setting. The Emulator may also have malfunctioned.
18	0x0c70 0x0c76 0x0c77	**[It has not accessed to DCU.]** A DCU access error may occur when the DCK = 20 MHz setting is selected due to noise in the N-Wire I/F(DCK, DMS, DDI, DDO, DRST) or because the specification is not satisfied, so select the DCK = 10 MHz setting. Check the power to the device and the interface voltage. Check the connection of the signal lines (N-Wire I/F). The device executes the program in user mode until the [Start] button is clicked in the V850 JTAG OCD Checker. Therefore, the device cannot be connected to the Emulator if a program to clear the OCDM0 bit to 0 is under execution. When using a device with the OCDM0 bit (OCDM register), set the OCDM0 bit to 1. *Check the noise level using a DCK waveform test.*
19	0x0c71	**[Reset couldn't be performed.]** Confirm that the resonator oscillates normally. Confirm that the correct value is set to MainOSC. Check the clock signal. This may be caused by a stopped clock or a slow clock. Check the connection of the N-Wire I/F(DCK, DMS, DDI, DDO, DRST).
20	0x0c72	**[Monitor memory couldn't be accessed.]** Confirm that the resonator oscillates normally. Confirm that the correct value is set to MainOSC. *Check the noise level using a DCK waveform test.* The problem may also be caused by an internal chip problem. Check the connection of the N-Wire I/F(DCK, DMS, DDI, DDO, DRST).
21	0x0c73	**[Monitor execution couldn't be performed.]** Confirm that the resonator oscillates normally. Confirm that the correct value is set to MainOSC. *Check the noise level using a DCK waveform test.* The problem may also be caused by an internal chip problem. Check the connection of the N-Wire I/F(DCK, DMS, DDI, DDO, DRST).
22	0x0c74	**[CPU register cannot be accessed.]** Confirm that the correct device is selected. Confirm that the resonator oscillates normally. Confirm that the correct value is set to MainOSC. *Check the noise level using a DCK waveform test.* The problem may also be caused by an internal chip problem. Check the connection of the N-Wire I/F(DCK, DMS, DDI, DDO, DRST).
23	0x0ca2 0x0ca3	**[Incorrect selection of a device file]** Confirm that the correct device is selected.
24	0xf603	**[Incorrect ID Code.]** The ID code is incorrect. Input a correct ID code. If the FLMD0 pin is High, confirm that the pin is connected according to the user's manual of the Emulator. Check the N-Wire connection enable flag (bit 7 at address 79). If this flag cannot be connected or the ID code has been forgotten, erase the flash memory using the flash programmer.

No.	Error No.	Error Messages and Corrective Action
25	0xf604	**[Incorrect ID Code. Abort the V850 JTAG OCD Checker.]** The ID code is incorrect. Re-start the V850 JTAG OCD Checker and input a correct ID code. If the FLMD0 pin is High, confirm that the pin is connected according to the user's manual of the Emulator. Check the N-Wire connection enable flag (bit 7 at address 79). If this flag cannot be connected or the ID code has been forgotten, erase the flash memory using the flash programmer.
26	0xf605	**[The ID code input setup is required.]** Check the ID code check box and input the ID code.
27	0xf606	**[IECUBE is connected.]** Remove IECUBE.

5. 1. 2 When V850E2M/V850E2S is chosen

Note *1: Selection is required only when [E1 Emulator] in the **Emulator** area is chosen.

No.	Error No.	Error Messages and Corrective Action
1	0x0100	**[Driver couldn't be opened.]** The PC and Emulator may be not connected. The PC may be not recognized after it has entered suspend mode, so restart the PC. The device driver may be not installed. Install the driver.
2	0x0105	**[Failed in reading device file (dxxxx.800).]** The necessary file may be damaged. Reinstall the device file.
3	0x0109	**[USB access failed.]** Exit this utility and re-connect up Emulator.
4	0x010a 0x01a6	**[EXEC already work.]** Exit the debugger.
5	0x01a0	**[Processing of a monitor was not completed to within a time.]** Confirm that the resonator oscillates normally. Confirm that the correct value is set to MainOSC. The problem may also be caused by an internal chip problem. Check the connection of the NEXUS I/F(TCK, TMS, TDI, TDO, TRST, RDY).
6	0x03a0	**[The Power supply of target is OFF.]** Check the target power supply. Check the cable connecting the Emulator and target board. Check that the VDD signal is input to the connector of the target board.
7	0x0400	**[Incorrect value of MainOSC.]** MainOSC can't be set to 0.
8	0x0b04	**[Although the power supply of target is ON, Vdd Out is set Enable.] (*1)** Set Vdd Out as Disable, or shut off the power supply of the target.
9	0x0c01	**[During access of register, CPU did timeout.]** Confirm that the resonator oscillates normally. Confirm that the correct value is set to MainOSC. The problem may also be caused by an internal chip problem. Check the connection of the NEXUS I/F(TCK, TMS, TDI, TDO, TRST, RDY).
10	0x0c02	**[During access of memory, CPU did timeout.]** Confirm that the resonator oscillates normally. Confirm that the correct value is set to MainOSC. The problem may also be caused by an internal chip problem. Check the connection of the NEXUS I/F(TCK, TMS, TDI, TDO, TRST, RDY).
11	0x0c24	**[It couldn't shift to debug mode.]** Confirm that the resonator oscillates normally. Confirm that the correct value is set to MainOSC. Check the clock signal. This may be caused by a stopped clock or a slow clock. Check the connection of the NEXUS I/F(TCK, TMS, TDI, TDO, TRST, RDY).
12	0x0c2e	**[During access of flash memory information, CPU did timeout.]** Confirm that the correct device is selected. The problem may also be caused by an internal chip problem.
13	0x0c2f	**[During access of flash memory information, the response from CPU was not right.]** Confirm that the correct device is selected. The problem may also be caused by an internal chip problem.
14	0x0c43	**[Connection of Emulator couldn't be performed.]** Confirm that the resonator oscillates normally. Check the OPJTAG bit of OPBT0. If OPJTAG bit is set to 1 (JTAG I/F is enable), Emulator can connect to the device. Confirm the RESET circuit on the target board. It might have been unable to shift to a debug mode, because the device was during RESET. Set the OPBT0 to stop the Watchdog timer using the flash programmer. It might have been unable to shift to a debug mode, because often generating RESET by the Watchdog timer. The Emulator may also have malfunctioned.
15	0x0c70 0x0c77	**[It has not accessed to DCU.]** Check the power to the device and the interface voltage. Check the connection of the NEXUS I/F(TCK, TMS, TDI, TDO, TRST, RDY).

No.	Error No.	Error Messages and Corrective Action
16	0x0c71	**[Reset couldn't be performed.]** Confirm that the resonator oscillates normally. Confirm that the correct value is set to MainOSC. Check the clock signal. This may be caused by a stopped clock or a slow clock. Check the connection of the NEXUS I/F(TCK, TMS, TDI, TDO, TRST, RDY).
17	0x0c72	**[Monitor memory couldn't be accessed.]** Confirm that the resonator oscillates normally. Confirm that the correct value is set to MainOSC. The problem may also be caused by an internal chip problem. Check the connection of the NEXUS I/F(TCK, TMS, TDI, TDO, TRST, RDY).
18	0x0c73	**[Monitor execution couldn't be performed.]** Confirm that the resonator oscillates normally. Confirm that the correct value is set to MainOSC. The problem may also be caused by an internal chip problem. Check the connection of the NEXUS I/F(TCK, TMS, TDI, TDO, TRST, RDY).
19	0x0c74	**[CPU register cannot be accessed.]** Confirm that the correct device is selected. Confirm that the resonator oscillates normally. Confirm that the correct value is set to MainOSC. The problem may also be caused by an internal chip problem. Check the connection of the NEXUS I/F(TCK, TMS, TDI, TDO, TRST, RDY).
20	0x0ca3	**[Incorrect selection of a device file]** Confirm that the correct device is selected.
21	0xf603	**[Incorrect ID Code.]** The ID code is incorrect. Input a correct ID code. If the FLMD0 pin is High, confirm that the pin is connected according to the user's manual of the Emulator. Check the On-chip Debug enable flag (bit 7 at address 79). If this flag is set to disable or the ID code has been forgotten, erase the flash memory using the flash programmer.
22	0xf604	**[Incorrect ID Code. Abort the V850 JTAG OCD Checker.]** The ID code is incorrect. Re-start the V850 JTAG OCD Checker and input a correct ID code. If the FLMD0 pin is High, confirm that the pin is connected according to the user's manual of the Emulator. Check the On-chip Debug enable flag (bit 7 at address 79). If this flag is set to disable or the ID code has been forgotten, erase the flash memory using the flash programmer.
23	0xf605	**[The ID code input setup is required.]** Check the ID code check box and input the ID code.
24	0xf606	**[IECUBE is connected.]** Remove IECUBE.

If data access by [DCU Reg] test results in NG

Normal access to the DCU register is impossible.

Perform a DCK waveform test.

If no anomaly is found with the DCK waveform test, the register may be damaged, so try again with a different chip.

If data access by [CPU Reg] test results in NG

Normal access to the CPU register is impossible.

Perform a DCK waveform test.

If no anomaly is found with the DCK waveform test, the register may be damaged, so try again with a different chip.

5.2 DCK waveform test

Check the following items regarding the design of the target board, in accordance with the user's Manual.

CHAPTER 4 NOTES ON TARGET SYSTEM DESIGN in the IE-V850E1-CD-NW User's Manual or **3.4 Designing Target System Circuits** in the QB-V850MINI(L) User's Manual.

IE-V850E1-CD-NW/QB-V850MINI

- Is the pattern of the N-Wire interface signal 100 mm or less?
- Is the DCK signal shielded by a pull-up resistor[Note] + GND?
- Is a pull-up resistor[Note] connected to the DMS, DDI, and DDO signals?
- Is a pull-down resistor[Note] connected to the _DRSTZ signal (or DRST signal)?

Note The resistance of the resistor must be as specified for each device. Some devices have on-chip pull-up/down resistors. With these devices, an external resistor is not necessary.

Also check the following items regarding the power supply capacity of the target board.

- Is a power supply with a sufficient capacity used?
- Are sufficient capacitors provided on the target board?
- Is a bypass capacitor connected to all the power supply pins of the CPU?
- Is the GND plane on the target board sufficiently large?

6. Changes from N-Wire Checker V1.30/V2.10

The following point has been changed from N-Wire Checker V1.30 and V2.10 to V850 JTAG OCD Checker V1.00.

- The V850E2M core and V850E2S core are now supported.
- The E1 Emulator and E20 Emulator are now supported.

7. Restrictions

- Up to 21,000 characters can be displayed in the log viewer area.

- If the number of characters exceeds the displayable limit, the oldest data will be overwritten. In this case, refer to the log file as all the data is recorded there.

- In cases when there is a severe shortage of system resources, output to the log viewer area will stop. In this case, even though screen output has stopped, data will continue to be recorded in the log file and can be referenced from there. (The log file is overwritten when the V850 JTAG OCD Checker is started up.)

Revision History	V850 JTAG OCD Checker User's Manual

Rev.	Date	Description	
		Page	Summary
1.00	Feb 20, 2013	—	First Edition issued
2.00	Apr 04, 2016	5	1.3 Operating Environment, Deleted.

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