User Manual

SLG47105V Evaluation Board Quick Start UM-GP-001

Abstract

This user manual provides basic guidelines for developers to get familiar with the Evaluation Board for SLG47105V. It consists of the functional descriptions of the board.

Contents

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Tables

1 Terms and Definitions

ADB	Advanced Development Board
EVB	Evaluation Board
PDB	Pro Development Board
TP	Test Point

2 References

[1] SLG47105V, Datasheet - https://www.renesas.com/SLG47105#documents.

[2] NXP «I2C-bus specification and user manual». User manual. UM10204–Rev.6, 4 April 2014. https://www.nxp.com/webapp/Download?colCode=UM10204&location=null

3 Introduction

SLG47105V Evaluation Board (see Figure 1) let's get acquainted with SLG47105's functionality, especially the H-Bridge/Half-Bridge functions, and allows the User to test the power part of the chip.

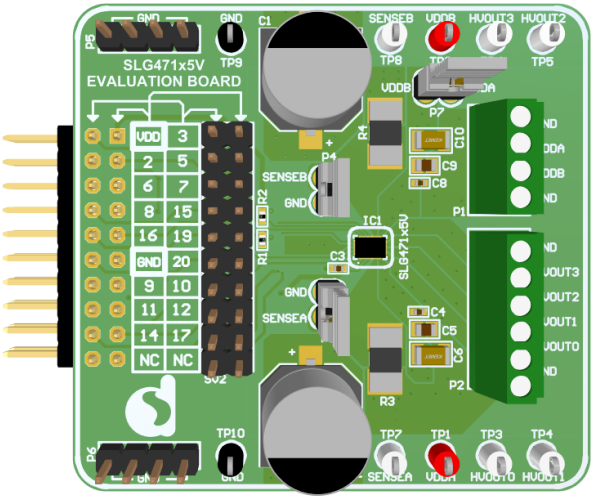


Figure 1: SLG47105V EVB General View

You can emulate/program the SLG47105V chip with the Advanced Development Board (ADB) or Pro Development Board (PDB). Insert EVB expansion connector SV1 into the ADB or PDB socket. In the case with PDB connect EVB expansion connector SV1 into the socket connector. The first pin locates at the right connector side. See Figure 2.

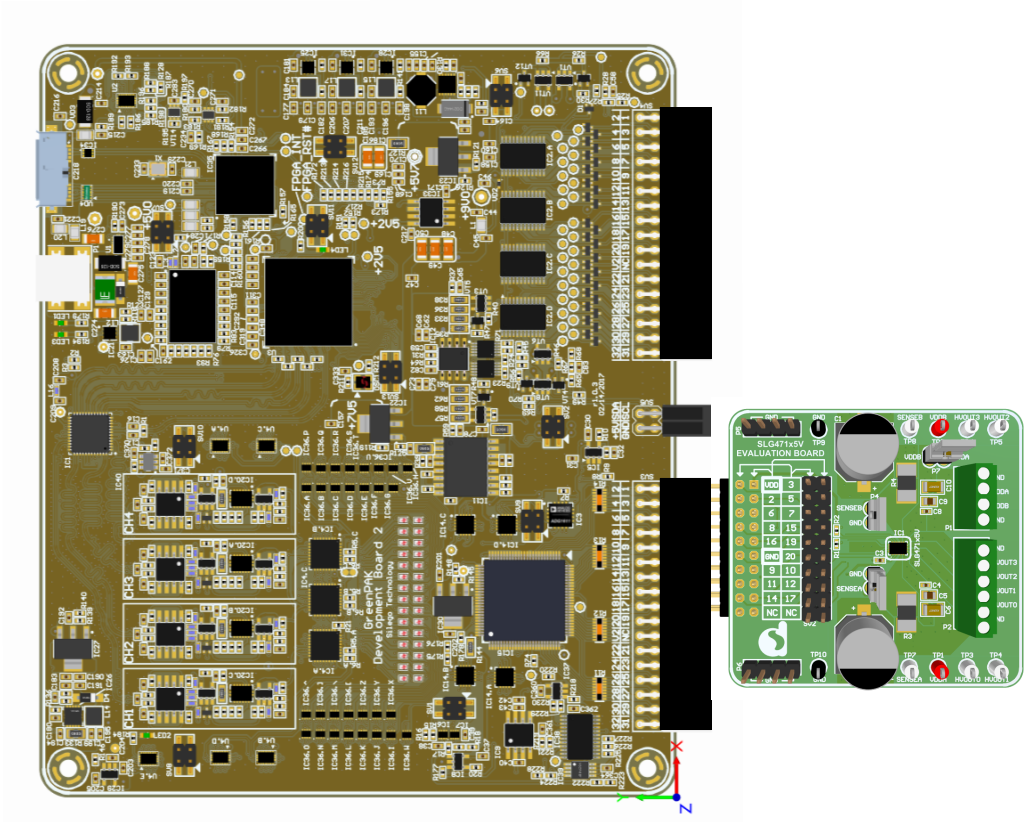


Figure 2: SLG47105V EVB Connected into PDB

4 Functional Description

4.1 Expansion Connectors and Test Points

4.1.1 Expansion Connectors SV1 and SV2

There are two male headers SV1 and SV2 placed on the board.

The SV1 male header is used only to connect SLG47105V Evaluation Board to the GreenPAK Advanced Development Platform or the GreenPAK Pro Development Platform. Therefore, SV1 has a connection with Chip Low Voltage IO Pins only. High Voltage Pins 6, 7, 8, 9, 10, and 11 are not connected to SV1 by default.

Only in case V_{DD} = V_{DD2}, it is possible to connect High Voltage Pins 6, 7, 8, 9, 10, and 11 to SV1 by installing resistors R6-R11 on the board.

The SV2 male header has a connection with all the chip pins and can be used in the debugging process. This allows monitoring the chip functionality by connecting measuring devices (oscilloscope, voltmeter, logic analyzer) to SV2.

Male headers SV1 and SV2 functions can be found in Table 1.

Table 1: Male Headers SV1 and SV2 Functions

Header	Marked on board	IC Pin	Function	Notes
SV1.1 SV2.1	V_{DD}	Pin 1	V_{DD}	
SV1.2 SV2.2	3	Pin 3	GPI	
SV1.3 SV2.3	2	Pin 2	GPIO 0	
SV1.4 SV2.4	5	Pin 5	Sense_A	Pin 5 is connected to SV1.4 through R6 resistor by default
SV1.5 SV2.5	6	Pin 6	V_{DD2_A}	Pin 6 isn't connected to SV1.5. R6 should be mounted on board
SV1.6 SV2.6	7	Pin 7	HV_GPO 0	Pin 7 isn't connected to SV1.6. R7 should be mounted on board
SV1.7 SV2.7	8	Pin 8	HV_GPO 1	Pin 8 isn't connected to SV1.7. R8 should be mounted on board
SV1.8 SV2.8	15	Pin 15	I^2C SCL/GPIO 2	
SV1.9 SV2.9	16	Pin 16	I^2C SDA/GPIO 3	
SV1.10 SV2.10	NC			
SV1.11 SV2.11	GND	Pin 4, 13, 18		
SV1.12 SV2.12	NC			
SV1.13 SV2.13	9	Pin 9	HV_GPO 2	Pin 9 isn't connected to SV1.13. R9 should be mounted on board
SV1.14 SV2.14	10	Pin 10	HV_GPO 3	Pin10 isn't connected to SV1.14. R10 should be mounted on board

Header	Marked on board	IC Pin	Function	Notes
SV1.15 SV2.15	11	Pin 11	VDD2_B	Pin11 isn't connected to SV1.15 R11 should be mounted on board
SV1.16 SV2.16	12	Pin 12	SENSE_B	Pin 12 is connected to SV1.16 through R12 resistor by default
SV1.17 SV2.17	14	Pin 14	GPIO 1	
SV1.18 SV2.18	17	Pin 17	GPIO 4	
SV1.19 SV2.19	19	Pin 19	GPIO 5	
SV1.20 SV2.20	20	Pin 20	GPIO 6	

4.1.2 Power Supply and Power Selection Connectors (P1 and P7)

V_{DD2} is supplied from an external power supply through the connector P1. It is possible to apply two separate Power Supplies, V_{DD2_A} and V_{DD2_B}, for each H-Bridge separately.

For P1 connector pin functions refer to Table 2.

Table 2: P1 Connector Functions

Header	Marked on board	IC Pin	Function	Notes
P1.1	GND			
P1.2	VDDB	Pin 11	V_{DD2_B}	
P1.3	VDDA	Pin 6	V_{DD2_A}	
P1.4	GND			

In case only one Power Supply is used to power both H-Bridges, it is possible to install Jumper P7 to connect V_{DD2_A} and V_{DD2_B} power lines. This allows applying an external voltage to only one (any) terminal, V_{DD2_A}, or V_{DD2_B}.

Warning: if the values of VDD2_A and VDD2_B are different, Jumper P7 must be removed.

Jumper P7 functions can be found in Table 3.

Table 3: Jumper P7 Functions

Jumper	Marked on board	IC Pin	Function	Notes
P7		Pin 6	V_{DD2_A}	OPEN – for powering H-Bridges/Half-Bridges both V_{DD2_A} and V_{DD2_B} are used. CLOSED – for powering H-Bridges/Half-Bridges one of two, V_{DD2_A} or V_{DD2_B}, is used.
		Pin 11	V_{DD2_B}	

Using test points TP1 (V_{DD_A}) and TP2 (V_{DD_B}) the User can control the voltage on V_{DD2_A} and V_{DD2_B} rails.

Capacitors C1 and C2 are used to decouple noise on the V_{DD_A} and V_{DD_B} power lines. They are optional and are not board mounted by default. It is possible to install them by the user independently, for example, when testing a high-power motor close to the chip maximum capabilities.

4.1.3 High-voltage Output Connector (P2)

The connector P2 is used for connecting the electric motor or another high-power load powered by V_{DD2}. For P2 connector pin functions see Table 4.

Table 4: P2 Connector Functions

Header	Marked on board	IC Pin	Function	Notes
P2.1	GND	Pin 1		
P2.2	HVOUT0	Pin 7	HV_GPO 0	Test point TP3 (HVOUT0) mounted on board
P2.3	HVOUT1	Pin 8	HV_GPO 1	Test point TP4 (HVOUT1) mounted on board
P2.4	HVOUT2	Pin 9	HV_GPO 2	Test point TP5 (HVOUT2) mounted on board
P2.5	HVOUT3	Pin 10	HV_GPO 3	Test point TP6 (HVOUT3) mounted on board
P2.6	GND	Pin 1		

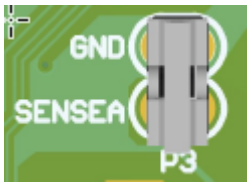
Test points TP3 (HVOUT0), TP4 (HVOUT1), TP5 (HVOUT2), and TP6 (HVOUT3) make possible controlling the output signals.

4.1.4 Current Measurement Shunts P3 and P4

Resistors R3 and R4 are connected to the inputs SENSE_A (Pin 5) and SENSE_B (Pin 12) of the Current Sense Comparator macrocells, which allow controlling the load current of each H-Bridge. This function can be switch on/off with the help of two Jumpers, P3 and P4.

Jumpers P3 and P4 functions can be found in Table 5.

Table 5: Jumpers P3 and P4 Functions

Jumper	Marked on board	IC Pin	Function	Notes
P3		Pin 5	Connect SENSE_A to GND	OPEN – Current Sense Comparator0 current control function is turned on. CLOSED – Current Sense Comparator0 current control function is turned off.
P4		Pin 12	Connect SENSE_B to GND	OPEN – Current Sense Comparator1 current control function is turned on. CLOSED – Current Sense Comparator1 current control function is turned off.

It is possible to control voltage on resistors R3 and R4 by connecting measuring devices (voltmeter, oscilloscope) to test points TP7 (SENSE_A) and TP8 (SENSE_B), installed on the board.

Also, there are two test points TP9 and TP10 (GND) installed on the board. They are connected to Pin 4 (GND_A) and Pin 13 (GND_B) and can be used for measurements **only**.

4.1.5 I²C Pull-Up Resistors

If the board is not connected to the GreenPAK Advanced Development Platform or the GreenPAK Pro Development Platform and used separately, for example, with a programmed chip for debugging in the final production, two Pull-up resistors, R1 and R2 for SDA and SCL, should be installed on the board. Their resistance should be calculated according to the procedure described in Reference [2] (Section 2).

4.1.6 Protection Digital GND from Power GND

PTC1 is used for protecting digital GND from power GND (HV_GND). The maximum current that can flow from power GND through PTC1 to digital GND pin is limited to 50 mA.

5 Conclusions

Evaluation Board has been designed as a high power debugging platform for SLG47105V. It is a convenient tool that allows the customer to get acquainted with SLG47105's functionality, especially the H-Bridge functions.

Appendix A Board Dimensions

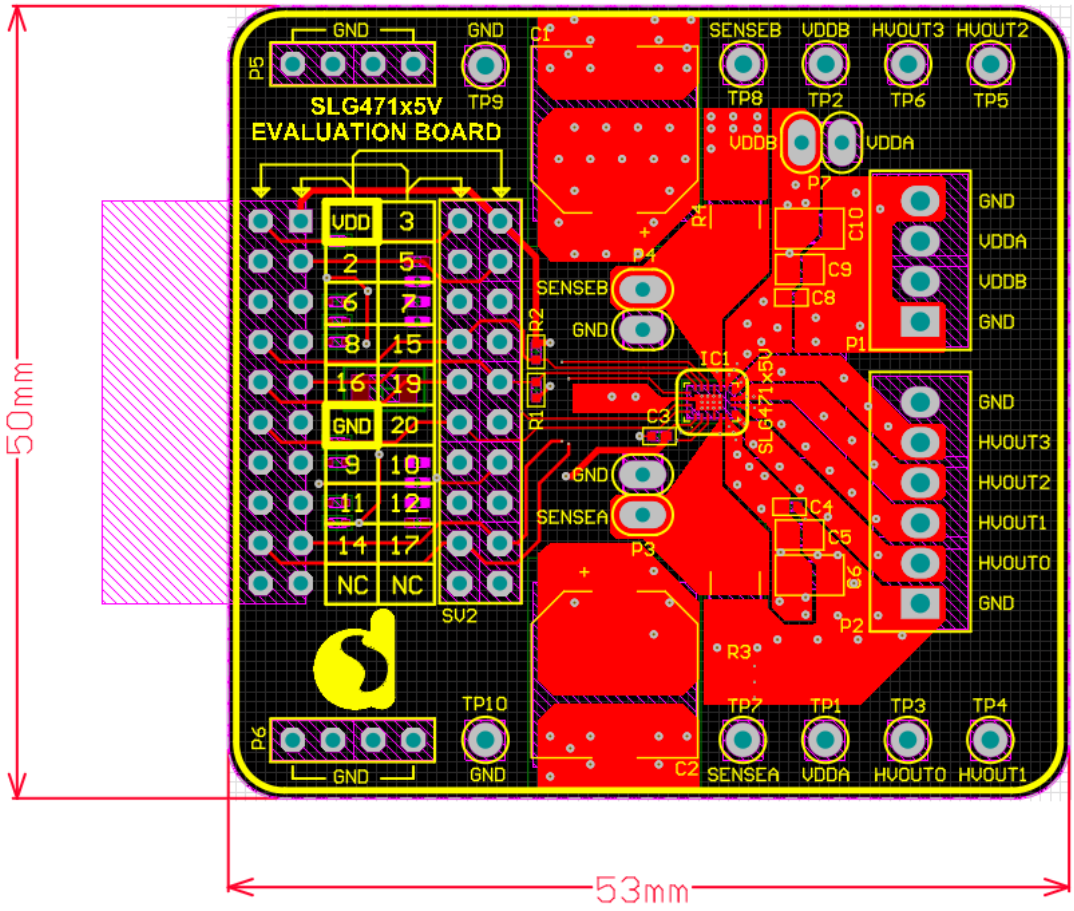


Figure 3: SLG47105V Evaluation Board Dimensions

Appendix B Top View

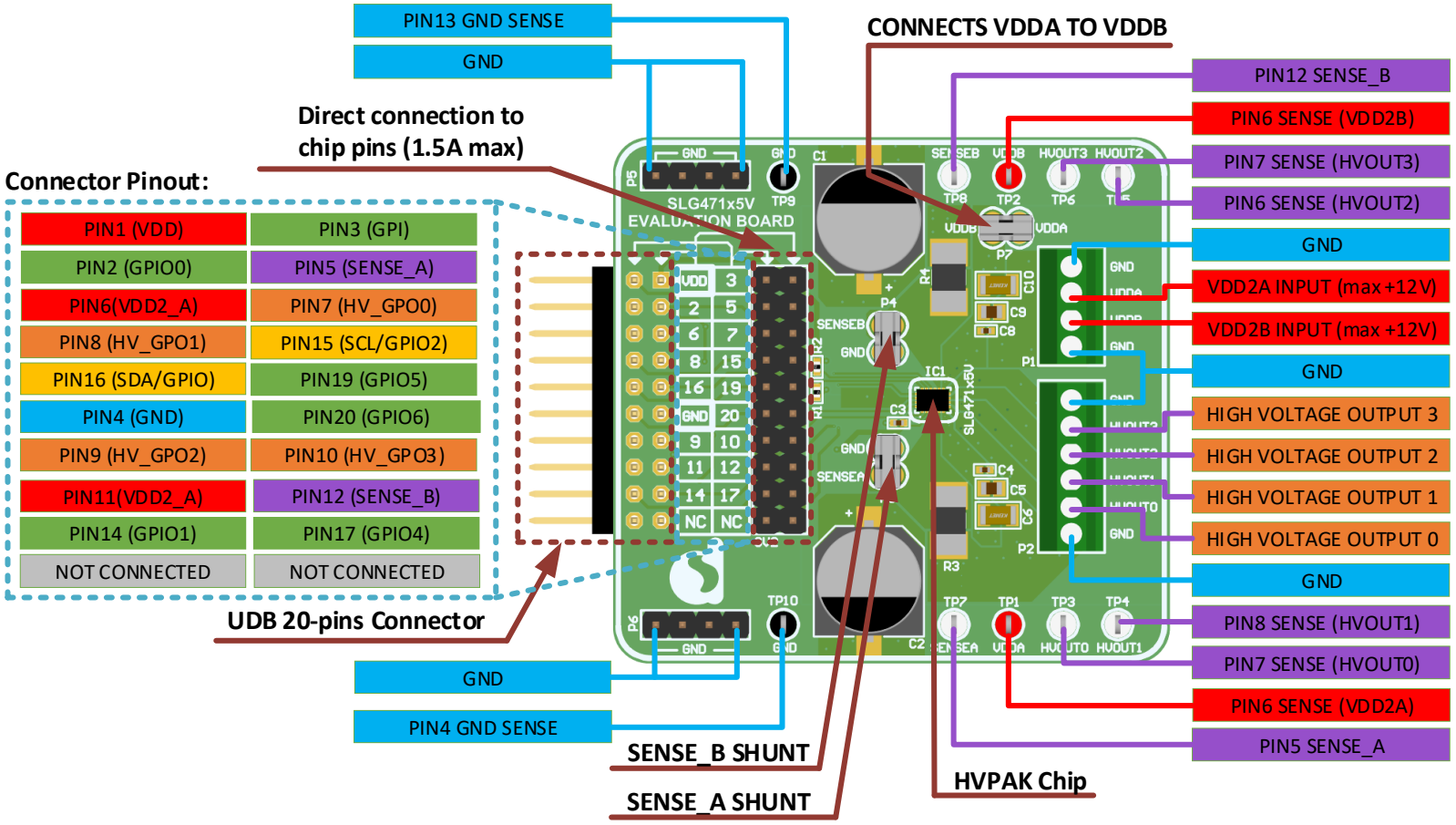


Figure 4: SLG47105V Evaluation Board, Top View

Appendix C Board Schematic

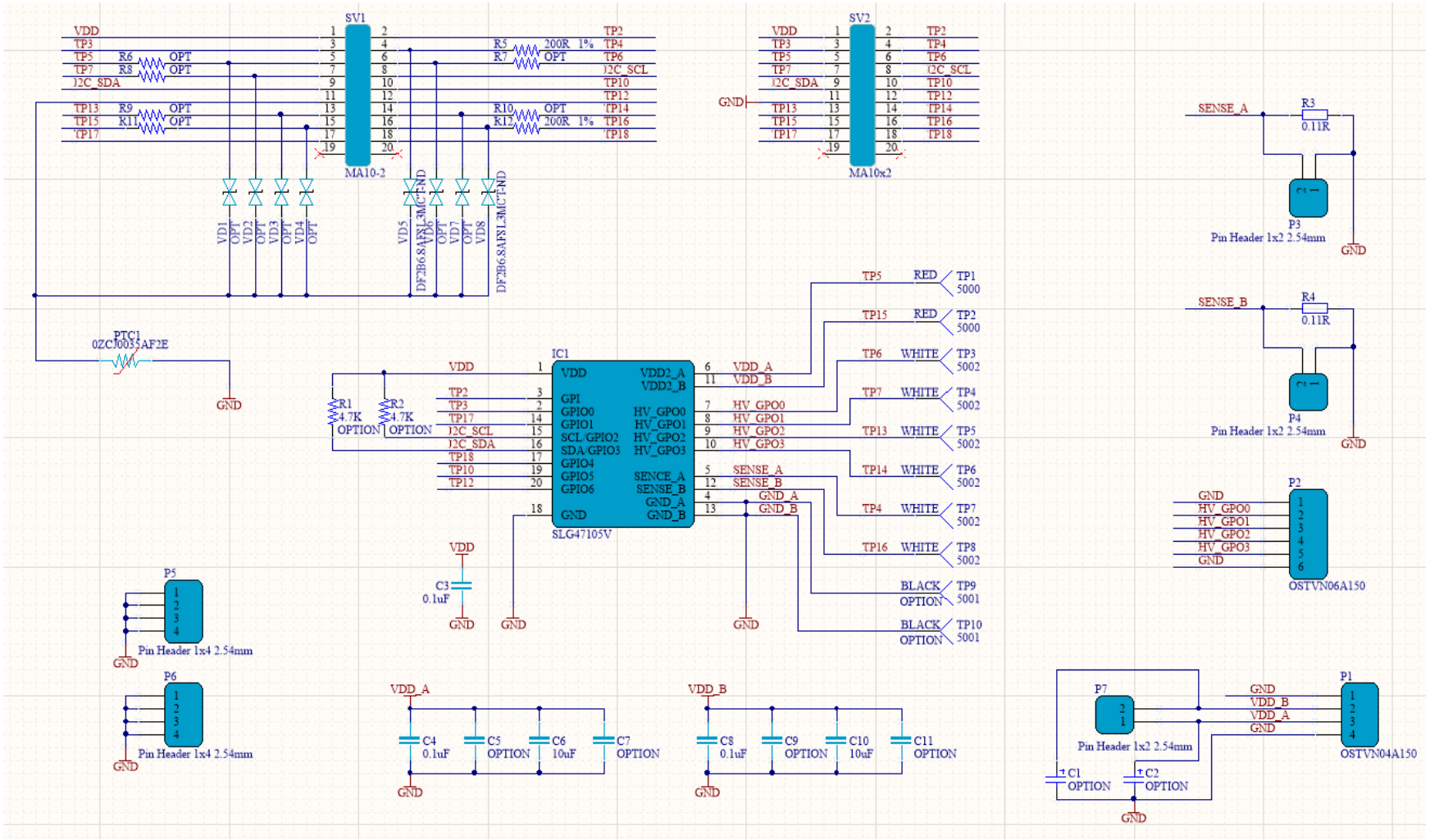


Figure 5: SLG47105V Evaluation Board Schematic

Appendix D BOM

#	Designator	Description	Footprint	Quantity
1	C1, C2	OPTION	Size code: G	2
2	C3, C4, C8	CAP CER 0.1UF 50V X7R 0402	0402 (1005 Metric)	3
3	C5, C9	OPTION	0805 (2012 Metric)	2
4	C6, C10	CAP CER 10UF 50V X5R 1206	1206 (3216 Metric)	2
5	C7, C11	OPTION	1207 (3216 Metric)	2
6	IC1	PROGRAMMABLE MIXED-SIGNAL MATRIX WITH H-BRIDGE FUNCTIONS	STQFN-20L	1
7	J1, J2, J3	CONN JUMPER SHORTING .100" GOLD		3
8	P1	TERM BLK 4P SIDE ENT 2.54MM PCB	4 POSITION TERMINAL BLOCK (2.54MM)	1
9	P2	TERM BLK 6P SIDE ENT 2.54MM PCB	6 POSITION TERMINAL BLOCK (2.54MM)	1
10	P3, P4, P7	CONN HEADER VERT 2POS	2 POSITION PIN HEADER (2.54MM)	3
11	P5, P6	CONN HEADER VERT 4POS	4 POSITION PIN HEADER (2.54MM)	2
12	PTC1	PTC RESET FUSE 60V 50MA 1206	1206 (3216 Metric)	1
13	R3, R4	RES 0.11 OHM 1% 1/2W 2010	2010 (5025 Metric)	2
14	R5, R6, R7, R8, R9, R10, R11, R12	RES SMD 200 OHM 5% 1/16W 0402	0402 (1005 Metric)	8
15	SV1	CONN HEADER R/A 20POS 2.54MM	20 POSITION RIGHT ANGLE (2.54mm)	1
16	SV2	CONN HEADER VERT 20POS 2.54MM	20 POSITION VERTICAL (2.54mm)	1
17	TP1, TP2	TEST POINT MINIATURE RED	Hole Diameter(1.02mm)	2
18	TP3, TP4, TP5, TP6, TP7, TP8	TEST POINT MINIATURE WHITE	Hole Diameter(1.02mm)	6
19	TP9, TP10	OPTION	Hole Diameter(1.02mm)	2
20	VD1, VD2, VD3, VD4, VD5, VD6, VD7, VD8	TVS DIODE 5V 7V FSC	SOD-923	8

Revision History

Revision	Date	Description
1.5	20-Feb-2023	Updated References
1.4	21-Mar-2022	Renesas rebranding
1.3	7-Sep-2021	Updated hyperlinks
1.2	13-May-2020	Updated Figures
1.1	24-Apr-2020	Fixed typos
1.0	4-Feb-2020	Initial version

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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