RENESAS

RTKA271084DE0000BU

7-channel Automotive PMIC Evaluation Board and GUI

Description

The RTKA271084DE0000BU evaluates the performance of the RAA271084 Automotive PMIC with a high voltage primary buck/boost controller, a low voltage synchronous buck controller, and five low-dropout liner regulators (LDO), two of which can be used as trackers. The evaluation board is intended for providing MCU power in automotive applications.

In addition to four output voltages, the evaluation board also contains an SPI interface.

The RAA271084 is offered in a 7mm×7mm 48-lead Step Cut QFN (SCQFN) package or 9mm×9mm 48-lead thin QFP (LQFP) with an exposed pad. The RAA271084 is qualified to AEC-Q100, Grade1.

Features

- V_{IN} operating range from 2.7 to 42V including cold crank
- Start range 4.5 to 42V
- Two DC/DC controllers with integrated drivers
 - Buck-Boost DCDC1 5.7V at 2.2A
 Buck DCDC2 resister programmable (5V at 1.2A, 3.3V at 1.8A, 1.09V at 4.2A)
- Five linear regulators
 - LDO0 (VCC), 5V (always on)
 - LDO1-4, programmable 3.3V/5V (LDO1-2 at 350mA, LDO3-4 at 200mA)
 - LDO3-4, configurable as trackers with short-to-battery/short-to-ground and reverse current protection
- Configurable Frequency 440kHz/2.2MHz
- Over-temperature, overcurrent, overvoltage, and negative overcurrent protection







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1. Functional Description

The evaluation board with connections, headers, and test points is shown in Figure 2.



Figure 2. RAA271084 Evaluation Board: Connections, Headers, and Test Points

- To start the board, apply the input voltage(2.7V < VIN < 42) to the VIN supply terminals J1(+) and J2(-) (see Figure 2).
- For EN control, use WAKE1 and WAKE2 at J25 and J26 (see Figure 2).
- For VDDIO voltage supply, use the VDDIO voltage jumpers to select the supply source (see Figure 2).
- For tracker reference input, use the VTR3/4 Input jumpers to select the supply source (see Figure 2).

1.1 Manual Output Control using WAKE1 and WAKE2

For manual control of EN, ensure that the J25 and J26 jumpers are not installed. WAKE1/WAKE2 enables the IC (see Figure 2).

The following are the states of WAKE1/WAKE2:

- WAKE1/WAKE2 < 0.4V
- The IC is off and in its lowest power state.
- WAKE1 or WAKE2 > 1.4V
 - The IC is enabled.

The status of the regulators depends on the PMIC STATE and settings. Refer to the *RAA271084 Datasheet*, section *Operation of the PMIC*.



1.2 Testing the Outputs

When the WAKE1 or WAKE2 inputs are configured, the outputs can be loaded to perform tests such as load regulation, startup and shutdown, and load transients.

1.2.1 Input and Output Connections and Test Points

The input and output connections are shown in Figure 1 and Table 1.

Connection	(+) Test Point	GND Test Point	Default Value (V)
VBAT (input)	TP1	TP61	12 (2.7V to 42V, 4.5V to start)
Vout1	TP6	TP10	5.7
Vout2	TP5	TP10	5.0 or 3.3 or 1.09
LDO0 (VCC)	J5 (VCC)	TP62	5.0
LDO1	TP21	TP45	5.0 or 3.3
LDO2	TP22	TP45	5.0 or 3.3
LDO3/TRACKER3	TP23	TP45	5.0 or 3.3
LDO4/TRACKER4	TP24	TP45	5.0 or 3.3

Table 1. Connections and Test Points

The following are more test points (see Figure 1):

- RSTB and INTB test points, located on the upper-side of J4.
- WAKE1 and WAKE2 test points, located on the middle of J4.

2. GUI Operation

The RAA271084 GUI can be used to configure feature sets by creating an OTP file, which generates customer samples. For initial samples of the RAA271084, the Renesas Application Engineering Team provides a short-form questionnaire for customer inputs on major options. (The customer can also review the datasheet and specify additional configuration options as required.)

The RAA271084 OTP Initial Configuration:

- Input voltage range
- DCDC1 (Buck/Boost) and DCDC2 (Buck) switching frequency
- DCDC1 (Buck/Boost) output current
- DCDC2 (Buck) output voltage and current
- Output voltage and current for LDO1-4
- Output rails startup and shutdown timing and sequencing requirements
- LDO3/LDO4 usage (LDO or tracker)

The following are requirements before starting the GUI software:

- A USB interface cable must be connected between the host computer and the EVB.
- The VDDIO supply to the EVB must be 3.3V minimum.

Figure 3 shows the list of the GUI files to be downloaded. Double-click the **RAA271084.exe** file to start the GUI software.

setup_RAA271084_Customer_GUI_0.0.0.11.exe

Figure 3. GUI Files



When powered up, the GUI appears as shown in Figure 4.



Figure 4. State/Status Tab with Labels

The GUI functions are grouped into rows or columns. Figure 4 displays the **State/Status** tab, which is detailed in this section along with other tabs such as the **Feature Set**, **Fault Management**, **Misc**, and **Table View**.

In the center of Figure 4, the **Status Information** label points to data that is grouped into rows. *Note:* These rows are shown for the **State/Status** tab, and other tabs show different options. The rows are explained as follows:

- **Tab Select** This row contains buttons for the different tabs in the GUI. Each tab controls a set of functions. When the tab is selected, the GUI displays the dropdowns and options associated with that tab.
- **Connection Status** This row shows the Connection Status with the GUI tool and EVB. Green signals a correct connection. Yellow signals no connection. Red signals an incorrect connection.
- Manual register Read / Write This row contains the Bus interface, ChipSelect Pin, Reg. Address, Send Data, Read Data, and Advanced Mode column. A bus interface can be used to select RAA271084_ISL_SPI or RAA271084_SAM3U_SPI. Select to suit for the EVB and GUI connection. (If the EVB and PC are connected directly, select RAA271084_ISL_SPI. For a register read/write, input the register address and use Send Data to write or Read Data to read. To control the Frequency, Dev Num, CLK Mode, Write Flag, Dummy Bytes, and CRC Flag, check the Advanced Mode box.
- **Register Polling Enable / Disable** This row contains the register polling function. Set the button to enable or disable the register polling function.
- File IO This row contains file related functions. The GUI can export or import the OTP setting from a CSV or TXT file.



Complete the following steps to create an OTP file:

- 1. Make the selections for these tabs: Feature Set, Fault Management, and Misc.
- 2. Review the selections using the Table View tab.
- 3. Start the OTP programming widget located in the Tools dropdown menu (Figure 5).

From the main menu, select Tools > RAA271084 OTP Programmer to start the OTP Programmer Widget. —	RAA27 File Too RA C	1084 Is Search View Help fodel IO ustom Tabs AA271084 OTP Programme	p Ianagement Mi	sc Table View							- • ×
	te/Stat	DEV ID LO BYTE		DEV ID HI BYTE		DEV REV LO BYTE		DEV REV HI BYTE		Communication	
	Sta	ID_LO_BITE	132	ID_HI_BYTE	16 💌	REV_LO_BITE	1	REV_HI_BYTE	12 ×	USB conne	ztion
		0x0000	0x84	0x0001	0x10	0x0002	0x01	0x0003	0x0C	RAA271084	Device Communication
		Regulator Status				1				Reconn	ect to device
		SEQ_STATUS		PG_STATUS						Bus Interface	RAA271084 SAM
		LDO4_ENABLED	disabled	LDO0_PG	not good					ChipSelect Pin	0x00 +1
		LDO3_ENABLED	disabled	LDO4_PG	not good					Reg. Address	0x0000 쉬
		LDO2_ENABLED	disabled	LDO3_PG	not good					Send Data	0,00 -
		DCDC2_ENABLED	disabled	LDO2_PG	not good					Read Data	0,00
		DCDC1 ENABLED	disabled	DCDC2 PG	not good					Advanced Mode	
				DCDC1_PG	not good					Polling	
		0x0004	0x00	0x0005	0x00					D	isabled
						2				O Poll All Register	s Poll Visible Only
		PMIC State								- 110 -	
		DCDC_STATE		LDO_STATE		CONTROLLER_STAT		FUSA_STATE		Read /	All Registers
		DCDC2_STATE	idle 🔤	LDO4_STATE	idle 😿	SEQUENCER_STATE	OFF	FUSA_EN	Monitors disabled	C	

Figure 5. OTP Programming Sequence

4. In the OTP programmer screen, click Load From Registers (Figure 6).



Figure 6. Import OTP Changes from Default Configuration



5. Save the configuration using the **.ini** format (Figure 7).

RAA271084 OTP Program	nmer	Load Table Values				Transfer Table Values			- U	×
		Load Table values	Load from File			Save to	File			
			Load from Registers			Transfer to R	egisters			
		Stepping Next Unprogrammed Char	nge N	ext Invalid Change		CRC Checks	Tab	le CRC 0CCA		
		Colour Key Zero Value	Non-Zero		Unprogrammed	l Change	Programmed Value		Invalid Char	ige
Reg Addr	Register Name	OTP Value Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x00 0x0010 OPT_SEQ_	CTRL	0x00			OPT_EN_DS_			Reserved	10_472	
		¥					Use the dro	pdown		
	Save OTP Config	uration				×	menu to se	lect an		
	$\leftarrow \rightarrow \cdot \cdot \uparrow$	Desktop	ٽ ~	Search Deskt	op	۹		<i>α</i> ι.		
	File name	RAA271084_OTP_config_00	CCA.ini			~				
	Save as type	s INI *.ini				\sim				
	✓ Browse Folders			Save	Can	icel	 Click Save. 			

Figure 7. Save the OTP Configuration as .ini File

- Load defaults Use this button to update the register values to default.
- Info window This row describes information (see Figure 4).
- Status menu tabs These tabs are the **Console** tab, used for scripts, and the **Log** tab, used to view activity logs.
- Status information This indicates the register settings. The value can be changed by clicking.
- Chip ID Reads the device ID and silicon revision.

When powered up, the GUI should initially appear as in Figure 4. When the IC is enabled and connected with a USB, the GUI automatically detects the EVB.



2.1 Changing Programming Options

Complete the following steps to make changes in the options on this tab such as Output Voltage and V_{OUT} OV Threshold:

- 1. Input the VBAT and WAKE1 or WAKE2 to place the IC in enabled. All the options on the **State/Status** tab can be changed only when the device is Enabled.
- 2. Select the options by clicking the relevant menu button.

Note: There are options not shown on this **State/Status** tab. These other options are located on the **Feature Set**, **Misc**, and **Table View** tabs. Changes on that tab can be made by moving to that tab and selecting the required options.

3. Changes are applied immediately when the button is clicked.

Note: While options can be selected, the accuracy of the selected options can be slightly outside the datasheet specifications. Datasheet accuracy limits are assured only for the factory-programmed settings. As an example, if LDO1 is selected to the default value of 5.0V, the output value is finely adjusted at the factory for LDO1 set to 5.0V. If V_{OUT1} is later changed to a different voltage setting, the new V_{OUT1} voltage might be slightly less accurate than the default setting. However, the change in accuracy is minor and should not significantly affect system or board level testing. After the required options are chosen, the device can be ordered and factory-adjusted with those specific options to provide the best accuracy available.

Note: If any option is set to a value other than the factory-programmed value and OPT_SPI_CRC is enabled, this creates a CRC Recheck fault. This CRC Recheck error is ignored if the OPT_SPI_CRC is disabled.



2.2 Feature Set Tab

View the Feature Set information by clicking the Feature Set button in the tab row.

ols Searc	h View Help								
1084									
Status	Feature Set Fault Mana	agement Misc	Table View						Rail Timing
	Rail Timing								4
C	OPT_SEQ_CTRL		OPT_SLOT_TIME		OPT_SLOT_DCDC		OPT_SLOT_LDO		
- 0	OPT_EN_DS_SLOT	Are enabled as soo	OPT_SLOT3_TIME	Oms 🗸	OPT_SLOT_DCDC2	slot 0 🗸 🗸	DPT_SLOT_LDO4 sl	ot 0 🗸	
R	leserved_10_472	0	OPT_SLOT2_TIME	Oms v			DPT_SLOT_LDO3 si	ot 0 v	
			OF 1_3COT1_TIME	una -			DPT SLOT LDO1	ot 0	
0	x0010	0x00	0x0011	0x00 🗄	0x0012	0x00 🗄 (0x0013	x00 🗄	
C	OPT_HP		OPT_DS		OPT_TOFF_TIME				
0	OPT_HP_LDO4_DIS	enabled	OPT_DS_LDO4_DIS	enabled	OPT_TOFF_DLY_LDO4	100us			
0	OPT_HP_LDO3_DIS	enabled	OPT_DS_LDO3_DIS	enabled	OPT_TOFF_DLY_LDO3	100us			
0	OPT_HP_LDO2_DIS	enabled	OPT_DS_LDO2_DIS	enabled	OPT_TOFF_DLY_LDO2	100us			
a	OPT_HP_DCDC2_DIS	enabled	OPT_DS_DCDC2_EN	disabled	OPT_TOFF_DLY_DCDC2	100us			
0	0x0014	0x00 🗄	0x0015	0x00 🗄	0x0016	0x00 🗄			
			· · · · · · · · · · · · · · · · · · ·						
C.	Regulator Control]	Regulat	or Control			
0	OCDC_CTRL		LDO_CTRL						
D	CDC2_START	ignored	LDO4_START	ignored					
D	CDC1_STOP	ignored	LDO3_STOP	ignored					
D	CDC1_START	ignored	LDO3_START	ignored					
			LDO2_STOP	ignored					
			LDO1_STOP	ignored					
			LDO1_START	ignored					
0	x0020	0x00	0x0021	0x00					
									d Manitan
	Monitor		ODT VMONR CTRL1		AMUX CEL		EPPP CTPL2		
0	PT_ERRB_MODE	ERRB low runs ER	OPT_VMONB_RSTB_W	Startup does not w	AMUX_OD_SEL	use push/pull	ERRB_PER_USED	OPT_ERRB_PER	
0	PT_ERRB_PER1	ERRB input ignon 🗸	OPT_VMONB_PER1	VMON8 input igr \vee	AMUX_SEL	AMUX disabled	Reserved_34_43	Low	
							ERRB_PER2	ERRB input ignore V	
0	xuu30	[ux00 🗄	Ux0031	Ux00 🗄	Ux0032	[0x00	UX0034	ux00 🗄	
V	MONB_CTRL2								
VI	MUNB_PER_USED	OPT_VMONB_PER							
V	MONB_PER2	VMONB input igr							
0	x0035	0x00							
	Surteen Self Tert		·						A System Solf Test
N	VAKE_PIN_CTRL		PWR_PIN_CTRL		INTB_PIN_CTRL		VMONOUT_PIN_CTRL		- System Seir Test
W	VAKE2_IN_LATCHED	Low	PSTBYB_IN_LATCHED	Low	INTB_TEST_DATA	Low	VMONOUT_IN_LATCHED	Low	
W	VAKE2_MODE	transparent 🗸	PSTBYB_MODE	transparent 🗸	INTB_TEST_EN	mission mode	VMONOUT_MODE	transparent 🗸	
W	WAKE1_IN_LATCHED	Low	PWRCTRLB_IN_LATCHED	Low	INTO_SENSED				
w	WAKE1_MODE	transparent 🗸	PWRCTRLB_MODE	transparent 🗸					
W	VAKE1_IN	Low	PWRCTRLB_IN	Low	0.0040	[a.co	0.0040		
	00040	0000	0x0041	0000	0x0042		0x0043		
E	RRB IN LATCHED	Low	RSTB_PIN_CTRL RSTB TEST DATA	Low	SSPB_PIN_CTRL SSPB_TEST_DATA	Low	WDENB_PIN_CTRL WDENB DATA	Low	
EF	RRB_MODE	transparent 🗸	RSTB_TEST_EN	mission mode	SSPB_TEST_EN	mission mode	WDENB_SEL	monitor power go	
EF	RRB_IN	Low	RSTB_SENSED	Low	SSPB_SENSED	Low	WDENB_OD	push/pull	
							WDENB_IN_LATCHED	transparent V	
							WDENB_IN	Low	
0	x0044	0x00	0x0045	0x00	0x0046	0x00	0x0047	0x00	
P	WR_MODE_CTRL								
W	VAKE2_CTRL	WAKE2 level level V							
P	MIC_OFF	Powers down DCD							
									J
	EOT								← EOT
0	D SPEEDUP	1Hz	CD RUNNING	not running	EOT_CTRLS	do nothing 🗸	EOT_PD0 EOT PD0	0	
d	D_STOP	Run	CD_ALARM_EN	Ignore	EOT_PD_CTRL	do nothing 🗸			
C	D_SET	no action	EOT_RUNNING	not running	EOT_WU_CTRL	do nothing 🗸 🗸			
0	D_ENABLE	disabled	OVF_ALARM_EN	Ignore					
E	OT_STOP	Run	WU_ALARM_EN	Ignore wake up					
B	OT_RST	no action							
E	OT_ENABLE	disabled							
0	x0060	0x00 🗄	0x0061	0x00	0x0062	0x00	0x0063	0x00	
Ð	OT_PD1		EOT_WU0		EOT_WU1		EOT_WU2		
E	OT_PD1	0 V	EOT_WU0	0 2	EOT_WU1		EOT_WU2		
0	IXUU64	0000	0x0065	000	0x0066	0000	0x0067	0000	
Đ	OT_TMR0		EOT_TMR1		EOT_TMR2	0	EOT_CD	0	
	01_1MR0	0x00	0x0069	0x00	0x006A	0x00	0x0068	0x3F	
			FOT WHEN		FOT HUDT				
B	OT PDDB0	0	EOT_WUDB0	0	EOT_WODB1	0			
0	x006C	0x00	0x006D	0x00	0x006E	0x00			
9									
6	WDT CTRL1		WDT_CTRL2		OPT WDT CONFIGN		WDT CONFIG2		← WDT
v	NDT_RUNNING	WDT stopped	WDT_STOP	Low	OPT_USE_SST_KICK	Not required to en	WDT_PIN_KICK_EDGE	either edge 🛛 🗸	
V	WDT_START	Low			OPT_WDT_SST_TIMEOUT	64ms 🗸	WDT_PIN_KICK_CTRL	Not used for pin ki	
					OPT_SST_RESP	lignore V	WDT_TOACC_FAULT_RE	Ignore V	
					OPT_WDT_WDEN8_CTRL	High at ACTIVE stat	AND TO ACCUPAULT_RESP	-gnore V	
0	0x0080	0x00	0x0081	0x00	0x0082	0x00	0x0083	0x00	
6	WDT CONFIGE		WDT SST		WDT KICK REG		WDT LESR		
v	NDT_DIS_LFSR	random question	SST_RUNNING	SST stopped	WDT_KICK_REG	0 🗸	WDT_LPSR	0	
	NDT_ANS_IDX	answer 0 🗸	EXIT_SST	Low					
V	NDT_MODE	Basic mode, Kick	0×0095	0.00	0×0090	0.00	0×0097	0.00	
v		ux00 🗄	UX0085	[Ux00 🗄	UX0086	ux00	Ux0087	ux00	
v Q	0x0084				WDT_ACC_CLEAR		WDT_TOACC_THRESH	1	
v o v	0x0084 WDT_ACC_THRESH		WDT_ACC		A REAL PROPERTY OF A READ PROPERTY OF A REAL PROPER	Low	WDT_TOACC_THRESH	U V	
v o v v	0x0084 WDT_ACC_THRESH NDT_ACC_THRESH 0x0088	0 ~	WDT_ACC WDT_ACC 0x0089	0	WDT_ACC_CLEAR	0x00	0x008B	0,00	
	0x0084 WDT_ACC_THRESH NDT_ACC_THRESH 0x0088	0 V 0x00 +	WDT_ACC WDT_ACC 0x0089	0 × 0x00	0x008A	0x00	0x008B	0x00	
> > 0 > > 0 > >	0x0084 WDT_ACC_THRESH WDT_ACC_THRESH 0x0088 WDT_TOACC		WDT_ACC WDT_ACC 0x0089 WDT_TOACC_CLEAR WDT_TOACC_CLEAR	0 × 000	WDT_ACC_CLEAR 0x008A WDT_TICK	0x00	0x008B WDT_LLCNT	0x00	
	XX0084 WDT_ACC_THRESH WDT_ACC_THRESH XX0088 WDT_TOACC WDT_TOACC		WDT_ACC WDT_ACC 0x0089 WDT_TOACC_CLEAR WDT_TOACC_CLEAR	0 ¥ 0x00	WDT_ACC_CLEAR 0x008A WDT_TICK WDT_ULTICK WDT_LLTICK	0x00	0x008B WDT_LLCNT WDT_LLCNT	0x00	
> < () < < () < < ()	00084 WDT_ACC_THRESH WDT_ACC_THRESH 00088 WDT_TOACC WDT_TOACC 0008C	0 V 0x00 ÷	WDT_ACC WDT_ACC 0x0089 WDT_TOACC_CLEAR WDT_TOACC_CLEAR 0x008D	0 ¥ 0x00 Low	WDT_ACC_CLEAR 0x008A WDT_TICK WDT_ULTICK WDT_ULTICK 0x008E	0x00 + + + + + + + + + + + + + + + + + +	0x0088 WDT_LLCNT WDT_LLCNT 0x008F	0.00 ÷	
	00084 WDT_ACC_THRESH NDT_ACC_THRESH 00088 WDT_TOACC NDT_TOACC 0008C WDT_ULCNT	0 V 0x00 ÷	WDT_ACC WDT_ACC 0x0089 WDT_TOACC_CLEAR WDT_TOACC_CLEAR 0x008D WDT_TOTICK	0 ¥ 0x00	WDT_ACC_CLEAR 0x008A WDT_TICK WDT_ULTICK WDT_ULTICK 0x008E WDT_TOCNT	0x00 10us pulse 10us pulse 0x00 0x0	0X008B WDT_LLCNT WDT_LLCNT 0X008F		
	xx0084 WDT_ACC_THRESH wDT_ACC_THRESH xx0088 WDT_TOACC xx008C WDT_ULCNT wDT_ULCNT		WDT_ACC WDT_ACC 0x0089 WDT_TOACC_CLEAR 0x008D WDT_TOTICK	0 20 0x00 0x00 0x00 0x00 0x00 0x00 0x00	WDT_ACC_CLEAR 0X008A WDT_TICK WDT_ULTICK WDT_LLTICK 0X008E WDT_TOCNT WDT_TOCNT	0x00 + 10us pulse > 10us pulse > 0x00 + 0 >	0x008B WDT_LLCNT WDT_LLCNT 0x008F		
	xx0084 NDT_ACC_THRESH NDT_ACC_THRESH xx0088 MDT_TOACC xx0080 Xx0080 MDT_ULCNT xx0090	0 V 0x00 2 0 V 0x00 V 0x00 V 0x00 2 0x00	WDT_ACC WDT_ACC Dx0089 WDT_TOACC_CLEAR Dx008D WDT_TOTICK WDT_TOTICK Dx0091	0 ≥ 2000	WDT_ACC_CLEAR 0x008A WDT_TICK WDT_URICK WDT_URICK 0x008E WDT_TOCNT WDT_TOCNT 0x0092	0x00	0x0088 WDT_LLCNT WDT_LLCNT 0x008F		

Figure 8. Feature Set Tab



The **Feature Set** tab information is arranged in columns as follows: Rail Timing, Regulator Control, Monitor, System Self Test, EOT, and WDT. The first column on top, Rail Timing lists OPT settings related to sequence timings, such as SLOT selection and delay time of each regulators and signals. For details on the sequence timing, refer to the *RAA271084 Datasheet*, section *Timing Summary*.

The remaining columns are described as follows:

- The Regulator Control column lists the start and stop settings of each regulator.
- The Monitor column lists monitoring function settings: such as the ERRB, VMONB, and AMUX monitoring mode settings.
- The System Self Test column lists the IC pin settings, such as WAKE1, WAKE2, PSTBYB, PWRCTRLB, INTB, VMONOUT, ERRB, RSTB, SSPB, and WDENB.

2.2.1 Fault Management

To view any detected faults, use the **Fault Management** tab. Any detected faults highlight with a green background such as in Figure 9 where the detected faults are the Overvoltage on LDO1 and LDO2.



Figure 9. Fault Management (LDO1 and LDO2 Severe OV Detected)

Note: If a fault is detected, the fault status bit for that fault is set to logic 1 and stays at logic 1 until the bit is cleared.

To clear a fault, go to the **Fault Management** dropdown and click the relevant button. This button changes to **no fault detected**, and the button background now appears white.



2.3 Misc Tab

The **Misc** tab is selected by clicking the **Misc** button in the tab row (see Figure 10). This tab controls miscellaneous options that are not contained in the **Feature Set** tab and **Fault Management** tab. The control method is the same as the other tabs.



Figure 10. Misc Tab



2.4 Table View Tab

The **Table View** tab is selected by clicking the **Table View** button in the tab row (see Figure 11). This tab contains all the registers that are shown in other tabs.

	RAA271084											
	File Tools Search View Help											
	RAA271084											
Register Value	State / Status Feature Set Fault	Management M	isc Table View									
Desister Address		Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit O		
Register Address:	0x0000: DEV_ID_LO_BYTE	0 x84				ID_LO 0x	_BYTE: 84					
Register Marile	0x0001: DEV_ID_HI_BYTE	0x10					BYTE: 10					
	0x0002: DEV_REV_LO_BYTE	0x01	NE_LU_0712 0x01									
	0x0003: DEV_REV_HI_BYTE	0x0C	REV_H_ 0x0/				I BYTE: .0C					
	0x0004: SEQ_STATUS	0x00	unu:	sed	0x00	0x00	0x00	0x00	0x00	0x00		
	0x0005: PG_STATUS	0x00	unused	0x00	0x00	0x00	0x00	0x00	0x00	0x00		
	0x0008: DCDC_STATE	0x00	1004.1	uni	used	CTATE-	00002	00 00	0x	00 00		
	0x0009: LDO_STATE	0x00	0x	NO SECUENC		00	0	00 I		00		
	0x000A: CONTROLLER_STATE	0x00		0	00	FUSA EN:	unused					
	0x000B: FUSA_STATE	0x00		unused		0x00	unused		0x00 Reserved	10 472		
	0x0010: OPT_SEQ_CTRL	0x00		unused	OPT SLC	0x00	OPT SIC	Ised	0x	T1 TIME		
	0x0011: OPT_SLOT_TIME	0x00	unu:	sed	_ 0x	.00	0	<00 ⁻	OPT SLOT	00 T DCDC2:		
	0x0012: OPT_SLOT_DCDC	0x00	OPT SLC	T LDO4:	OPT SLC	DT LD03:	OPT SL	DT LDO2:	Ox OPT SLC	00 DT LDO1:		
	0x0013: OPT_SLOT_LDO	0x00	0xl	00 ⁻	LDO4_DIS:	LDO3_DIS:	LDO2_DIS:	LDO1_DIS:	DCDC2_DIS:	00		
	0x0014: OP1_HP		unu		0x00 LDO4_DIS:	0x00 LDO3_DIS:	0x00 LDO2_DIS:	0x00 LDO1_DIS:	0x00 DCDC2_EN:	unused		
		0x00		and and	0x00 OPT_TOFF_DLY_LDO4:	0x00 OPT_TOFF_DLY_LDO3:	0x00 OPT_TOFF_DLY_LDO2:	0x00 OPT_TOFF_DLY_LDO1:	0x00 OPT_TOFF_DLY_DCD	unused		
		0x00			0x00	0x00	0x00 DCDC2_STOP:	0x00 DCDC2_START:	0x00 DCDC1_STOP:	DCDC1_START:		
	0x0020: DCDC_CTRL		LDO4_STOP:	LDO4_START:	LD03_STOP:	LDO3_START:	0x00 LD02_STOP:	0x00 LDO2_START:	0x00 LDO1_STOP:	0x00 LDO1_START:		
	0x0020-OPT EDDR CTDI 1	0x00	OPT_ERR	B_MODE:	unused	0x00	0800	OPT_ERRB_PER1:	UXUU	0x00		
	0x0031: OPT_VMONB_CTRL1	0x00	OPT_VMONB_RSTB	unu	used			OPT_VMONB_PER1:				
	0x0032: AMUX SEL	0x00	AMUX_OD_SEL:	uni	ised			AMUX_SEL:				
	0x0034: ERRB CTRL2	0x00	ERRB_PER_USED:	Reserved_34_43:	unused			ERRB_PER2:				
	0x0035: VMONB_CTRL2	0x00	VMONB_PER_USED: 0x00	Reserved_35_40: 0x00	unused			VMONB_PER2: 0x00				
	0x0040: WAKE_PIN_CTRL	0x00	WAKE2_IN_LATCHED: 0x00	WAKE2	_MODE:	WAKE2_IN: 0x00	WAKE1_IN_LATCHED: 0x00	WAKE 1	_MODE:	WAKE1_IN: 0x00		
	0x0041: PWR_PIN_CTRL	0x00	PSTBYB_IN_LATCHED: 0x00	PSTBYE 0	3_MODE: 600	PSTBYB_IN: 0x00	PWRCTRLB_IN_LATC 0x00	PWRCTR 0:	LB_MODE: (00	PWRCTRLB_IN: 0x00		
	0x0042: INTB_PIN_CTRL	0x00		uni	ised		INTB_TEST_DATA: 0x00	INTB_TEST_EN: 0x00	unused	INTB_SENSED: 0x00		
	0x0043: VMONOUT_PIN_CTRL	0x00		uni	ised		VMONOUT_IN_LATCH 0x00	VMONOL 0:	JT_MODE: 60	VMONOUT_IN: 0x00		
	0x0044: ERRB_PIN_CTRL	0x00		uni	used		ERRB_IN_LATCHED: 0x00	ERRB_0	MODE: 00	ERRB_IN: 0x00		

Figure 11. Table View

On the left side, the register address, name, and its value are described; on the right side, the settings for each bit are described. By clicking a bit, the value can be changed.



2.5 Reg Map link

The Reg Map (register map) link is selected by clicking **Help** from the main menu (see Figure 12). The GUI can show the register map in an HTML file by clicking the link.

RAA271084	
File Tools Search View	Help
	Register Map
RAA271084	About
State / Status Feature Set	Fault Management Misc Table View

Figure 12. Reg Map link

2.6 Log Tab

The **Log** tab is selected by clicking the **Log** tab in the tab row (see Figure 13). This tab maintains a log of read/write operations completed between the GUI and the RAA271084, which is useful for analyzing and understanding the register read/write operations used to configure the device options. For example, clicking **Read All** at any time initiates a read of many registers, and this series of register reads is displayed in the Log window. This Log feature can be useful when tracking the relationship between selecting device options and the registers associated with those options.

The **Log** tab also contains a **Clear Log** button that clears away all previous read/write information. This is helpful in tracking individual register operations.

2/1084 2 / Status Feature Set Fault	Management Misc	Table View							
FAULT STATUS 5 LDOQ SEVERE UV 7 LDOQ SEVERE UV 7 LDOQ WRNI, UV 7A LDOQ WRNI, UV 7A DGM JAWIT, PECO WG, OV 7AUT, PECO	NU no fault detected no fault detected no fault detected no fault detected fault detected fault detected no fault detected no fault detected no fault detected no fault detected no fault detected	FAULT_STATUS_6 FOT_CD_ALRM_RECORD FOT_CD_ALRM_RECORD FOT_VD_ALRM_RECORD FOT_WU_ALRM_RECORD DCDC2_OC2_FAULT_RE CRC_RECHECX_FAULT SPL_CRC_FAULTRECORD SPL_WRITE_FAULT_RECORD SPL_WRITE_FAULT_RECORD SPL_WRITE_FAULT_RECORD	no fault detected no fault detected (bx00)	FAULT_STATUS_7 RWLREG_FAULT_RECORD REGT_BUCKBOOST_M	no fault detected buck mode no fault detected no fault detected no fault detected no fault detected no fault detected 0x00 T	FAULT_STATUS_8 WDT_SST_FAULT_RECO WDT_TOACC_FAULT_REC WDT_LOC_FAULT_REC WDT_ACC_FAULT_REC WDT_LATE_FAULT_REC WDT_LATE_FAULT_REC WDT_ACC_FAULT_REC WDT_ACF_AULT_REC WDT_ACF_AULT_REC	no fault detected no fault detected		
VDDIO_OK_FAULT_R DCDC1_OC2_FAULT_ MANHAI FAIHT BF(C no fault detected RE no fault detected TO no fault detected	ive to file	Filter (reg expr	Status 17:	Enumera	te Mode	Log level:	Info	_

Figure 13. Log Tab



3. Board Design



Figure 14. RTKA271084DE0000BU Evaluation Board (Top)



Figure 15. RTKA271084DE0000BU Evaluation Board (Bottom)







Figure 16. RTKA271084DE0000BU Schematic (1 of 2)





RENESAS

3.2 Bill of Materials

Qty	Reference Designator	Description	Manufacturer Part Number
1	РСВ	PWB-PCB, RTKA271084DE0000BU, REVD, ROHS	RTKA271084DE0000BURVDPCB
1	C46	CAP, SMD, 0603, 10pF, 25V, 10%, C0G/NP0, ROHS	CGA3E2C0G2A100D080AA-T
2	C1, C72	CAP-AEC-Q200, SMD, 0603, 2.2µF, 10V, 10%, X7S, ROHS	CGA3E3X7S1A225K080AE-T
2	C12, C13	CAP-AEC-Q200, SMD, 2220, 4.7µF, 100V, 10%, X7R, ROHS	CGA9N2X7R2A475K230KA-T
1	C54	CAP-AEC-Q200, SMD, 0603, 4.7nF, 100V, 10%, X7R, ROHS	GCM188R72A472KA37D-T
1	C21	CAP-AEC-Q200, SMD, 0603, 10nF, 100V, 10%, X7R, ROHS	GCM188R72A103KA37D-T
1	C45	CAP-AEC-Q200, SMD, 0603, 10000pF, 50V, X7R, ROHS	CGA3E2X7R1H103K080AA
2	C22, C42	CAP-AEC-Q200, SMD, 0603, 0.047µF, 50V, 10%, X8R, ROHS	GCM188R91H473KA37D-T
2	C56, C58	CAP-AEC-Q200, SMD, 0805, 1.0µF, 16V, 10%, X7R, ROHS	GCM219R71C105KA37D-T
6	C57, C59, C60, C62, C64, C66	CAP-AEC-Q200, SMD, 0805, 4.7µF, 25V, 10%, X7S, ROHS	GCM21BC71E475KE36L-T
9	C31, C32, C33, C34, C35, C36, C47, C48, C49	CAP-AEC-Q200, SMD, 1210, 22µF, 16V, 10%, X7R, ROHS	GCM32ER71C226KE19L-T
2	C40, C41	CAP-AEC-Q200, SMD, 0805, 4.7µF, 16V, 10%, X7R, ROHS	GCM21BR71C475KA73K-T
3	C2, C7, C74	CAP-AEC-Q200, SMD, 0603, 0.1µF, 25V, 10%, X7R, ROHS	CGA3E2X7R1E104K080AA-T
0	a) C3, C4, C5, C6, C23, C24, C25, C29, C30,	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS	H1045-DNP
0	b) C43, C44, C55, C61, C71	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS	H1045-DNP
0	C63, C68	CAP, SMD, 0805, DNP-PLACE HOLDER, ROHS	H1046-DNP
0	C37, C38, C50, C51, C52, C65, C67	CAP, SMD, 1210, DNP-PLACE HOLDER, ROHS	H1082-DNP
2	C39, C69	CAP-AEC-Q200, SMD, 0603, 1.0µF, 25V, 10%, X7R, ROHS	ТМК107АВ7105КАНТ-Т
2	C17, C73	CAP, SMD, 0603, 1.0µF, 50V, 10%, X7R, ROHS	UMK107AB7105KA-T
1	C53	CAP-AEC-Q200, SMD, 0805, 1.0µF, 50V, 10%, X7R, ROHS	UMK212B7105KGHT-T
1	C15	CAP-AEC-Q200, SMD, 10.3mm, 120μF, 50V, 20%, 28mΩ, ROHS	EEH-ZC1H121P-T
3	C8, C9, C75	CAP, SMD, 0603, 4.7µF, 25V, 10%, X5R, ROHS	GRT188R61E475KE13D-T
1	L1	COIL-PWR CHOKE, SMD, 7.3*6.8*3, 0.68µH	VCMT063T-R68MN5TM-T
1	L2	COIL-PWR INDUCTOR, SMD, 4.5*4.3*2.1, 0.68µH	VCHA042A-R68MS62M-T
4	J1, J9, J11, J14	CONN-GEN, BIND.POST, INSUL-RED, THMBNUT- GND	111-0702-001
3	J2, J10, J12	CONN-GEN, BIND.POST, INSUL-BLK, THMBNUT- GND	111-0703-001
4	TP10, TP45, TP61, TP62	CONN-TURRET, TERMINAL POST, TH, ROHS	1514-2
1	J7	CONN-RECEPTACLE, TH, 9.6x8.4, 5-CONTACT, MINI B, ROHS	UX60-MB-5S8



RTKA271084DE0000BU Evaluation Board Manual

Qty	Reference Designator	Description	Manufacturer Part Number
28	TP1, TP2, TP3, TP5, TP6, TP7, TP8, TP9, TP11, TP12, TP13, TP15, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28, TP30, TP31, TP32, TP63	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	5002
3	J4, J5, J6	CONN-HEADER, 2x20, BRKAWY-2x36, 2.54mm, ROHS	67996-272HLF-2X20
28	J3, J35, J36, J38, J40, J42, J44, J65, J66, J72, J73, J74, J75, J76, J77, J78, J79, J80, J81, J82, J83, J84, J85, J90, J94, J95, J96, J97	CONN-HEADER, 1x2, BRKAWY 1x36, 2.54mm, ROHS	68000-236HLF-1X2
10	J8, J25, J26, J27, J30, J33, J34, J91, J92, J93	CONN-HEADER, 1x3, BREAKAWY 1x36, 2.54mm, ROHS	68000-236HLF-1X3
4	R5, R32, R67, R115 *SOLDER SHORT PADS	CONN-JUMPER, SOLDER SHORT	ASSEMBLY-SOLDER JUMPER
1	D3	DIODE-SCHOTTKY, AEC-Q101, SMD, 3P, TO-277, 45V,15A, ROHS	PMEG045V150EPDZ-T
2	D1, D2	DIODE-SCHOTTKY, SMD, SOT-323, 70V, 200mA, ROHS	SMMBD770T1G-T
1	U1	IC-PMIC, AUTOMOTIVE GRADE, 48P, SCQFN, ROHS	RAA271084A4HNP#AA0
1	U2	IC-USB uCONTROLLER, 32P, LQFP, HID-REV2.4 PROGRAM, ROHS	C8051F320-GQ/HID-REV2.4
1	U3	IC-SINGLE USB PORT TVS, SMD, 6P, SOT-23-6, ROHS	SN65220DBVR-T
3	Q1, Q2, Q3	TRANSISTOR-MOS, N-CHANNEL, SMD, LFPAK-33-8, 40V, 40A, 9.5m Ω , ROHS	BUK9M9R5-40HX-T
2	Q5, Q6	TRANSISTOR-MOS, N-CHANL, SMD, 8P, PowerDI3333-8, 30V, 14A, ROHS	DMG7430LFGQ-7-T
1	Q8	TRANSISTOR, N-CHANNEL, 3LD, SOT-23, 60V, 115mA, ROHS	2N7002-7-F-T
1	R64	RES, SMD, 0603, 2K, 1/10W, 1%, TF, ROHS	AC0603JR-072KL
1	R71	RES-AEC-Q200, SMD, 0603, 2.2Ω, 1/10W, 1%, TF, ROHS	ERJ-3RQF2R2V-T
1	R20	RES-AEC-Q200, SMD, 0603, 10Ω, 1/10W, 1%, ROHS	ERJ-3EKF10R0V-T
9	R3, R4, R12, R13, R100, R101, R102, R103, R116	RES-AEC-Q200, SMD, 0402, 0Ω, 1/10W, ROHS	ERJ-2GE0R00X-T
1	R129	RES-AEC-Q200, SMD, 0603, 10K, 1/10W, 1%, TF, ROHS	ERJ-3EKF1002V-T
19	R21, R23, R26, R29, R31, R36, R46, R50, R51, R52, R53, R60, R62, R66, R73, R79, R98, R99, R130	RES-AEC-Q200, SMD, 0603, 0Ω, 1/10W, TF, ROHS	ERJ-3GEY0R00V-T
1	R1	RES-AEC-Q200, SMD, 0603, 2.2Ω, 1/10W, 1%, TF, ROHS	ERJ-3RQF2R2V-T
2	R134, R135	RES, SMD 0603, 300Ω	RK73B1JTTD301J-T
1	LED1	LED, SMD, 1206, RED, 2.0V, 6mcd, 635nm, 20mA, ROHS	SML-LX1206IW-TR-T
1	LED2	LED, SMD, 1206, GREEN, 2.2V, 10mcd, 565nm, 20mA, ROHS	SML-LX1206GW-TR-T



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Qty	Reference Designator	Description	Manufacturer Part Number
0	R2, R8, R9, R10, R11, R15, R16, R47, R54, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R104, R105, R106, R107, R108, R109, R110, R111, R112, R113, R118, R119, R120, R121, R122, R127, R128	RES, SMD, 0402, DNP, DNP, DNP, TF, ROHS	-
0	R6, R7, R25, R27, R34, R58, R59, R68, R70	RES, SMD, 0603, DNP-PLACE HOLDER, ROHS	-
0	R38, R39, R56, R57	RES, SMD, 0805, DNP-PLACE HOLDER, ROHS	-
1	R55	RES, SMD, 0402, 100K, 1/16W, 1%, TF, ROHS	RC0402FR-07100KL-T
4	R95, R96, R97, R117	RES-AEC-Q200, SMD, 0402, 10K, 1/16W, 1%, TF, ROHS	RMCF0402FT10K0-T
3	R75,R77, R126	RES-AEC-Q200, SMD, 0603, 100K, 1/10W, 1%, TF, ROHS	RMCF0603FT100K-T
2	R74, R76 (ALT:RN73R1JTTD3612F50)	RES, SMD, 0603, 36.5K, 1/10W, 0.5%, 50ppm, THINFILM, ROHS	RT0603DRE0736K5L-T
1	R69	RES-AEC-Q200, SMD, 1206, 0.005Ω, 1W, 1%, METAL, CURR.SENSE, ROHS	TLR2BWDTD5L00F75-T
1	R28	RES-CURR.SENSE, SMD, 1206, 0.01Ω, 1W, 1%, 75ppm, ROHS	WSLP1206R0100FEA-T
5	Four corners top PCB + near J11	SCREW, 4-40X1/4in, PHILLIPS, PANHEAD, STAINLESS, ROHS	4-40X1/4-SCREW-SS
5	Four corners bottom PCB + near J11	STANDOFF, 4-40X3/4in, F/F, HEX, ALUMINUM, 0.25 OD, ROHS	4-40X3/4-STANDOFF-METAL
1	Place assy in bag	BAG, STATIC, 6X8, ZIPLOC, ROHS	6X8-STATIC-BAG
0	C10, C11, C16	Do not populate or purchase	DNP
0	Q9	Do not populate or purchase	DNP
2	D1, D2	DIODE-SCHOTTKY, SMD, SOT-323, 70V, 200mA,ROHS	SMMBD770T1G-T
1	Affix To Back Of PCB	LABEL-DATE CODE = LINE 1:YRWK-REV#, LINE 2:BOM NAME	LABEL-DATE CODE
10	J26.1&2, J27.1&2, J30.1&2, J25.1&2, J33.1&2, J34.1&2, J92.1&2, J77, J85, J93.1&2	CONN SHUNT 2POS 100 CLOSED TOP	880584-4
1	Bag & ship w/board	CABLE-USB 2.0, A MALE TO MINI B MALE, 1.8M, WHITE, ROHS	887328800



3.3 Board Layout



Figure 18. Top Layer

Figure 19. Layer 2



Figure 20. Layer 3

Figure 21. Layer 4



Figure 22. Layer 5

Figure 23. Bottom Layer



Figure 24. Silk Screen Top

Figure 25. Silk Screen Bottom



Figure 26. Assembly Top Layer

Figure 27. Assembly Bottom Layer

4. Ordering Information

Part Number	Description
RTKA271084DE0000BU	RAA271084 evaluation board

5. Revision History

Revision	Date	Description
1.00	Mar 19, 2025	Initial release.



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