

ISL78226EVKIT1Z, ISL78224EVKIT2Z Evaluation Kits and Software User Manual

Automotive Group

User's Manual

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RENESAS

ISL78226EVKIT1Z, ISL78224EVKIT2Z

Evaluation Kits and Software User Guide

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USER'S MANUAL

1. Overview

This user guide enables you to quickly install the software, set up and configure the hardware, use the hardware with the ISLUSBADAPT-EVZ dongle, and use the software to read and write to the ISL78226 and ISL78224 data registers. This guide includes step-by-step setup instructions for the software and hardware, an overview of software operation, and a detailed description of the software functions. Operation is similar for both the ISL78226 and ISL78224. This guide describes the operation of the ISL78226. Details specific to the ISL78224 are highlighted and discussed.

The ISL78226 and ISL78224 software enables control and observation of register settings and functional status of the controllers. It works primarily through a USB to I^2C interface dongle that enables logic (GPIO) control of discrete pins of the controllers.

This software allows you to interact and evaluate all aspects of the <u>ISL78226</u> and <u>ISL78224</u> PWM controllers. It is designed to enable you to quickly configure register settings and mode selections. The approximately 60 control selections are programmable at the register hex level or from user-selectable combo controls in the software. The software can also poll more than 70 alert and operation indicators.

1.1 Software Key Features

- I²C/PMBus compatible digital interface
- Read/write registers using direct hex or human translated interface elements
- Quick access control of EN and PWM_EN pins
- Functional combo box selection of more than 60 control register setting selections
- Direct hex read of fault and status registers
- Functional display of faults and operating status
- File-based save and recall of control register values
- User-selectable automatic startup options

1.2 Specifications

The ISL78226EVKIT1Z and ISL78224EVKIT2Z are configured and optimized for the following operating conditions:

- $V_{IN} = 5V$ to 64V
- BAT12 = 12V
- BAT48 = 48V
- VIN_FLY = 5V to 64V
- Efficiency = >95%, 12V at 100A, Buck mode input at 48V

1.3 Related Literature

For a full list of related documents visit our website:

• ISL78226 and ISL78224 product pages

1.4 Ordering Information

| Part Number Description | |
|-------------------------|--|
| ISL78226EVKIT1Z | Evaluation kit for the ISL78226 6-phase PWM controller |
| ISL78224EVKIT2Z | Evaluation kit for the ISL78224 4-phase PWM controller |



1.5 Kit Contents

The evaluation kit contains:

- ISL78226EVAL1Z or ISL78224EVAL2Z evaluation board
- \bullet ISLUSBADAPT-EVZ REV A USB to I^2C interface kit
- USB cable, I²C cable (four wires), and GPIO cable (11 wires)



Figure 1. ISL78226 Simplified Typical Application Schematic





Figure 2. ISL78224 Simplified Typical Application Schematic



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2. Quick Start Videos

The following quick start videos explain how to load the software and describe the basic functionality of the software. The titles of the videos are:

- ISL78226 PWM Controller Webinar
- <u>Automotive 6-Phase Bidirectional PWM Controller Video</u>
- ISL78226EVAL1Z: Software and Hardware
- ISL78226EVKIT1Z: Phase Dropping and Tracking



3. Functional Description

These boards can be used to boost 12V to 48V or buck from 48V to 12V. Use the software to program fault conditions and control the status of the board.

3.1 Operating Range

- V_{IN} voltage operating conditions: 6V to 64V
- BAT12 voltage: 6V to 40V
- BAT48 voltage: 48V to 64V (72V if V_{IN} is not driven by BAT48)

The size of the inductors enables the ISL78226 board to deliver 3kW of power with forced air. The ISL78224 board delivers 2kW of power with forced air. Monitor the temperature of the FETs and provide air flow as needed. See <u>"Maximum Operating Power for Evaluation Boards" on page 50</u> for more information about the operating range.

3.2 Getting Started

The software was developed on a 64-bit Windows 8 platform. Because the software registers as a Human Interface Device (HID) and uses standard HID calls, it works on Windows 7 and Windows XP operating systems or later (32-bit and 64-bit).

This user guide contains screenshots of the software at the time it was written. Subsequent software versions can appear differently.

3.3 Quick Hardware Setup Guide

The hardware must be connected to a computer through the USB cable for the software to start. Figure 3 shows the connection of the cables to the USB to I^2C board.



Figure 3. Connection of Cables to the USB to I²C Board



Figure 4 shows the connection of the cables on the ISL78226EVAL1Z REV A evaluation board. Pin 1 of the I²C cable is connected to J₇₄ and is marked with a white line on the connector. The GPIO cable is connected to J₇₇.

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Figure 5 shows the connection of the cables on the ISL78224EVAL2Z Rev A evaluation board. Pin 1 of the I²C cable is connected to J74 and is marked with a white line on the connector. The GPIO cable is connected to J77.



Figure 5. Connecting Cables to the ISL78224EVAL2Z



3.4 Installing the Software

(1) Download the software from the Renesas <u>website</u>. The screen in <u>Figure 6</u> appears.

| 🖳 View Downloads - Internet Explorer 💦 🗕 🗖 🌄 | | | | | | | |
|--|---------|-------------------------------------|----------|------------|------|-------|---|
| View and track your dow | nloads | | Search d | ownloads | | | ٩ |
| Name | | Location | | Actions | | | |
| intersil-isl7822exe intersil.com | 2.84 MB | Do you want to run this program? | or save | Run | Save | • | × |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| Options | | | | Clear list | | Close | |

Figure 6. Download Screen

(2) Click **Run** and approve the request to download the software. The Setup Wizard screen in Figure 7 appears.



Figure 7. Setup Wizard

(3) Click Next and select the location to save the file. The default location is C:\Users\Public\ISL78226. Click Browse to save the file in a different location. When finished, click Next.

| B Setup - ISL78226 | × |
|--|------------|
| Select Destination Location Where should ISL78226 be installed? | |
| Setup will install ISL78226 into the following folder. | |
| To continue, click Next. If you would like to select a different folder, cli | ck Browse. |
| C:\Users\Public\ISL78226 | Browse |
| At least 14.0 MB of free disk space is required. | |
| At least 14.0 Mb of free disk space is required. | |
| < Back Next > | Cancel |

Figure 8. Setup Wizard



(4) The Startup menu folder appears. Click **Browse** to save the shortcut in a different location. When finished, click **Next.**



Figure 9. Select Destination Location

(5) To create a desktop icon, check the box next to Create a desktop icon and click Next.

| 15 | Setup - ISL78226 - | □ × |
|-----|---|--------|
| | Additional Tasks ch additional tasks should be performed? | |
| | ect the additional tasks you would like Setup to perform while installing ISL782 n click Next. | 226, |
| Add | litional icons: | |
| ~ | Create a desktop icon | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | < Back Next > | Cancel |

Figure 10. Select Destination Location

(6) Click **Install** to install the software.



Figure 11. Select Destination Location



(7) To launch the software, check the box next to Launch ISL78226 and click Finish. The installation is now complete. Restart your computer if instructed to do so.

| 6 | Setup - ISL78226 🛛 🗕 🗆 🗙 |
|---|---|
| | Completing the ISL78226 Setup Wizard |
| | Setup has finished installing ISL78226 on your computer. The application may be launched by selecting the installed icons. |
| | Click Finish to exit Setup. |
| | Launch ISL78226 |
| R | |
| | |
| | Finish |

Figure 12. Select Destination Location

- (8) Select either ISL78226 Ready: Proceed to Standard Demo or ISL78224 Ready: Proceed to Standard Demo from the drop-down menu.
 - (a) Figure 13 shows the ISL78226 startup screen.



Figure 13. Software Startup Screen (ISL78226 Selected)



(b) <u>Figure 14</u> shows the ISL78224 startup screen.



Figure 14. Software Startup Screen (ISL78224 Selected)

(c) The flashing green bars indicate connections to the board. When the device under test is selected, the screen in Figure 15 on page 13 appears. The Quick Access Control Panel to the right in Figure 15 provides quick access to enable and disable the part, select either Buck or Boost operation, turn on the PWM, select either DE or CCM operation mode of operation, set the fault response to Hiccup or Latch, check fault registers, clear all faults, and automatically update the status of changes made in the Control and Observation panels.



| Control and Observation Panel | 6 6-Phase Bi-Directional Synchro | onous PWM Controller | Quick Access Control Panel |
|--|--|---|--|
| Control Registers Config & Status Alert Display Control Registers Status Regs (Hex) Startup Options T Statup Read Startup File Options Execute Startup T Image: Auto Load File Name ISL78224_Configuration_Default.csv Startup Configuration T Startup Configuration ISL78224_Configuration_Default.csv Startup Configuration Startup Configuration Image: Set Enable On (Device On GPIO_EN Pin 1) Startup Completed Image: Set Startup Completed Image: Set Enable On (Device On GPIO_EN Pin 1) Startup Completed Image: Set Startup Completed Image: Set Device Control Registers from File Image: Clear Faults Set PWM Image: Set PWM Read Control and Status Registers (I2C) Sample Interval (mSec) 1000 Active Devices Image: Startup Clear Faults Set Multi-Device Displays per Check Boxes Image: Set Multi-Device Displays per Check Boxes Set Multi-Device Displays per Check Boxes | est Access RSVD Device ID / Revision / Write Enable Device IDs AD 82 26 R Master • Device Revision AE 0C 01 R Master • Write Enable 10 00 R 00 W Master • | B0 0 R 0 0 W C0 0 R 0 0 W Sample Processor GPI0 Ports Sample GPI0 P0 P1 P2 30 P0 70 P1 00 P2 P1 00 P2 P1 P1 | System Controls Enable Disable Code ADR DD ACK Mode Pins Selection BT/BK Buck PWM EN ON Mode Selection DE / COM PGMCU PSTAT PGMCU PSTAT PGMCU PSTAT Alett / Fault Registers AL DF M ED |
| | |] | D8 D7 D6 D5 D4 D3 D2 M M GUI Sample Timers (Polling) GPIO: XSTAT XHIC XSYS Go 12C: 0xC0 Alerts Go 1000 mSec Update Interval |

Figure 15. Software Status Screen with Control and Observation Panel and Quick Access Control Panel

3.5 Connecting Hardware

3.5.1 Buck Mode

Caution: This is a high power application board. Renesas recommends disabling the part through the software and turning off all supplies before making connections to the board. Failure to do this could damage the board.

- (1) Verify that the computer is connected to the USB to I²C board and the evaluation board.
 - (a) See <u>Figures 3</u> and <u>4</u> for the ISL78226EVAL1Z setup.
 - (b) See <u>Figures 3</u> and $\frac{5}{5}$ for the ISL78224EVAL2Z setup.
- (2) Verify the jumper connections in <u>Table 1</u>. Note: Jumpers not listed in the table are not populated. Some of these "jumpers" are measurement terminals and cannot tolerate being shorted.

| Jumper ID | Device | Action | Function |
|------------------------------------|----------|-----------|----------------------------------|
| J ₁₄ | ISL78226 | Installed | BAT48 Bode Injection, |
| TP ₂₃ | ISL78224 | Installed | Jumper for normal operation |
| J ₁₅ | ISL78226 | Installed | BAT12 Bode Injection, |
| TP ₂₄ | ISL78224 | Installed | Jumper for normal operation |
| J ₂₀ Pin 2 connected to | ISL78226 | Installed | Short ISET to ISHARE, |
| J ₂₁ Pin 2 | ISL78224 | NA | Jumper for master only operation |
| J ₂₆ | ISL78226 | Installed | MCUVDD Bode Injection, |
| | ISL78224 | Not Used | Jumper for normal operation |

Table 1. Jumper Configuration



| Jumper ID | Device | Action | Function | | |
|--|---------------|---------------|--|--|--|
| J ₃₅ | ISL78226 | Switch | PD_CTRL Switch toward BAT48 (Phase drop ON) Switch toward BAT12 (Phase drop OFF) | | |
| J ₁ | ISL78224 | No Jumper | Phase drop ON | | |
| | | Installed | Phase drop OFF | | |
| J ₆₃ | ISL78226 | Installed | Disable V _{IN} voltage clamp | | |
| | ISL78224 | N/A | | | |
| J ₇₀ | ISL78226 | No Jumper | BT/BK Control | | |
| | ISL78224 | No Jumper | Remove for software operation | | |
| J ₇₁ | ISL78226 | Installed 1-2 | PWM_TRI | | |
| | ISL78224 | N/A | Enable tri-state driver operation | | |
| J ₈₀ | ISL78226 | Installed 2-3 | TRACK | | |
| | ISL78224 | Installed 2-3 | | | |
| J ₈₁ | ISL78226 | Installed 2-3 | ADDR1 | | |
| | ISL78224 | N/A | Configures as master | | |
| J ₈₂ ISL78226 Installed 2-3 | Installed 2-3 | ADDR2 | | | |
| | ISL78224 | N/A | Configures as master | | |
| J ₈₈ | ISL78226 | No Jumper | DE/CCM | | |
| | ISL78224 | No Jumper | Remove for software operation | | |
| J ₈₉ | ISL78226 | No Jumper | HIC/LAT | | |
| | ISL78224 | No Jumper | Remove for software operation | | |
| JP ₃₁₀ | ISL78226 | Installed | Jumper to enable Phase 3 | | |
| | ISL78224 | N/A | | | |
| JP ₄₁₀ | ISL78226 | Installed | Jumper to enable Phase 4 | | |
| | ISL78224 | N/A | | | |
| JP ₅₁₀ | ISL78226 | Installed | Jumper to enable Phase 5 | | |
| | ISL78224 | N/A | | | |
| JP ₆₁₀ | ISL78226 | Installed | Jumper to enable Phase 6 | | |
| | ISL78224 | N/A | | | |

Table 1. Jumper Configuration (Continued)

- (3) Connect the 48V supply or battery to one or more of the BAT48 connectors. See Figure 55 for ISL78226 connections and Figure 56 for ISL78224 connections. Note: the PCB connects all BAT48 phases together and all BAT48 PGNDs together. For high power evaluations, Renesas recommends connecting the 48V supply or battery to all six phases for distribution of power across the board.
- (4) Connect a DC electronic load or a 12V battery to one or more of the BAT12 connectors. See Figure 55 for ISL78226 connections and Figure 56 for ISL78224 connections. Note: the PCB connects all BAT12 phases together and all BAT12 PGNDs together. For high power evaluations, Renesas recommends connecting the DC electronic load or a 12V battery to all six phases for distribution of power across the board.
- (5) Connect a 12V supply to the VIN and VIN_FLY with its ground connected to FLYGND.
- (6) Connect a 5V supply to BAT12_IN with its ground connected to DGND. See <u>Figure 55</u> for ISL78226 connections and <u>Figure 56</u> for ISL78224 connections.

- (7) Connect the probes to the evaluation board. Use the connections shown in <u>Table 2</u> and <u>Figure 16</u> (ISL78226) or <u>Figure 17</u> (ISL78224). Note: Renesas recommends disabling the part through the software and turning off all supplies before making connections to the board.
 - (a) (ISL78226) Use the connections shown in Figure 16 and Table 2.



Figure 16. ISL78226 Scope Probe Connections

| Table 2 | . ISL78226 | Probe C | Connections | to I | Monitor | Phase | Voltages |
|---------|------------|---------|-------------|------|---------|-------|----------|
|---------|------------|---------|-------------|------|---------|-------|----------|

| Jumper | Phase |
|--------|-------|
| 29 | 1 |
| 31 | 2 |
| 34 | 3 |
| 37 | 4 |
| 40 | 5 |
| 44 | 6 |

(b) (ISL78224) Use the connections shown in Figure 17 and Table 3 on page 16.



Figure 17. ISL78224 Scope Probe Connections



| Jumper | Phase |
|------------------|-------|
| TP ₂₆ | 1 |
| TP ₂₇ | 2 |
| TP ₂₈ | 3 |
| TP ₂₉ | 4 |
| N/A | 5 |
| N/A | 6 |

Table 3. ISL78224 Probe Connections to Monitor Phase Voltages

- (8) Turn on the 12V supplies, 5V supplies, and the 48V supply (with no particular power supply sequence).
- (9) The first time you power up the board after configuring the board for the Buck mode operation, verify the operation is set to Buck mode.
- (a) In the software, navigate to the Quick Access Control Panel under Mode Pin Selection.
- (b) Select Buck mode from the BT/BK drop-down menu.
- (c) Click the **Enable** button at the top of the Quick Access Control Panel. The indicator next to the **Enable** button turns red.
- (d) Verify the flyback circuit is working by measuring the voltages at V6 and V12 (see Figure 55 for ISL78226 connections and Figure 56 for ISL78224 connections). V6 should measure about 6V and V12 around 12V. If the V6 and V12 measurements are correct, the controller is running and providing the proper clock signal to the flyback circuit. If the measurements are correct, proceed to Step 10.
 If the V6 and V12 measurements are not correct, disable the part through the software, turn off all the

If the V6 and V12 measurements are not correct, disable the part through the software, turn off all the supplies, and recheck all the connections.

(10) To automatically start the converter, click the Read Startup Files Options button shown in <u>Figure 18</u>. This loads the startup.csv file in the project directory that specifies startup options that set initial device settings. Note: You can manually edit the file.



Figure 18. Read Startup File Options

(11) Click **Execute Startup**. The program sets the initial device registers as well as the GUI controls and value windows.



| a | SL78224 4-Phase Bi- | Directional Synchi |
|--|---------------------|-------------------------|
| About | | |
| Control Registers Config & Status Alert Display | | |
| Control Regs (Hex) Status Regs (Hex) Startup Options | RSVD | RSVD |
| Startup | Device ID / Re | vision / Write Enable — |
| Read Startup File Options Execute Startu | P Devicec | IDs |
| ✓ Auto Load File Name ISL7822X_Configuration_Default.csv | AD [| R Master |
| - Startup Configuration | | |
| ✓ Set Enable On (Device On GPIO EN Pin 1) | | |
| | | |
| Read ID and Revision | | |
| Enable Writes (0x10 = 0) | Device F | Revision |
| Update Device Control Registers from File | AE | Master |
| 🔽 Clear Faults | | K |
| 🔽 Set PWM | | |
| Read Control and Status Registers (I2C) | | |
| | | |
| | | |
| Sample Interval (mSec) 1000 mSec Set Sample Intervals | Write E | nabla |
| | | Master |
| | 10 R | 00 W Master |

Figure 19. Execute Startup

(12) Observe the Startup Running window for several seconds.

| ISL782 | 224 4-Phase Bi-Di | irectional Synchro |
|---|--|--------------------|
| About | | |
| Control Registers Config & Status Alert Display | | |
| Control Regs (Hex) Status Regs (Hex) Startup Options | RSVD | RSVD |
| Startup Istraction Istraction | Device ID / Revis Device ID AD 82 20 Device Re AE 0B 0 | 5 R Master |
| ✓ Set PWM ✓ Read Control and Status Registers (I2C) Sample Interval (mSec) 1000 mSec Set Sample Intervals | Write Ena | ble |

Figure 20. Startup Running



(13) Wait for the "Startup Completed" message to display. The setup process takes a few seconds to complete.

| R | ISL78224 4-Phase Bi-Di | rectional Synchro |
|---|------------------------|-------------------|
| About | | |
| Control Registers Config & Status Alert Display | | |
| Control Regs (Hex) Status Regs (Hex) Startup Options | RSVD | RSVD |
| StartupRead Startup File OptionsExecute Star V Auto Load File Name ISL7822X_Configuration_Default.csv Startup Configuration V Set Enable On (Device On GPIO EN Pin 1) Startup Comple | | s — — — — — |
| Read ID and Revision Enable Writes (0x10 = 0) Update Device Control Registers from File Clear Faults Set PWM Read Control and Status Registers (I2C) | Device Rev | — <u> </u> |

Figure 21. Startup Completed

3.5.2 Boost Mode

Caution: This is a high power application board. Renesas recommends disabling through the software and turning off all supplies before making connections to the board. Failure to do this could damage the board.

- (1) Verify that the computer is connected to the USB to I²C board and the evaluation board
 - (a) See <u>Figures 3</u> and <u>4</u> for the ISL78226EVAL1Z setup.
 - (b) See <u>Figures 3</u> and <u>5</u> for the ISL78224EVAL2Z setup.
- (2) Verify the jumper connections in <u>Table 4</u>. Note: Jumpers not listed in the table are not populated. Some "jumpers" are measurement terminals and do not tolerate being shorted.

| Jumper ID | Device | Action | Function |
|---------------------------------|----------|-----------|---|
| J ₁₄ | ISL78226 | Installed | BAT48 Bode Injection, |
| TP ₂₃ | ISL78224 | Installed | Jumper for normal operation |
| J ₁₅ | ISL78226 | Installed | BAT12 Bode Injection, |
| TP ₂₄ | ISL78224 | Installed | Jumper for normal operation |
| J ₂₀ Pin 2 connected | ISL78226 | Installed | Short ISET to ISHARE, |
| to J ₂₁ Pin 2 | ISL78224 | N/A | Jumper for master only operation |
| J ₂₆ | ISL78226 | Installed | MCUVDD Bode Injection, |
| | ISL78224 | N/A | Jumper for normal operation |
| J ₃₅ | ISL78226 | Switch | PD_CTRL, Switch toward BAT48 (Phase drop ON) Switch toward BAT12 (Phase drop OFF) |
| J ₁ | ISL78224 | Jumper | PD_CTRL, Jumper for no Phase drop No jumper for Phase drop |
| J ₁ | ISL78224 | Jumper | Phase drop OFF |
| | | No Jumper | Phase drop ON |

Table 4. Jumper Configuration



| Jumper ID | Device | Action | Function |
|-------------------|----------|---------------|---------------------------------------|
| J ₆₃ | ISL78226 | Installed | Disable V _{IN} voltage clamp |
| | ISL78224 | N/A | |
| J ₇₀ | ISL78226 | No Jumper | BT/BK Control |
| | ISL78224 | No Jumper | Remove for software operation |
| J ₇₁ | ISL78226 | Installed 1-2 | PWM_TRI |
| | ISL78224 | N/A | Enable tri-state driver operation |
| J ₈₀ | ISL78226 | Installed 2-3 | TRACK |
| | ISL78224 | Installed 2-3 | |
| J ₈₁ | ISL78226 | Installed 2-3 | ADDR1 |
| | ISL78224 | N/A | Configures as master |
| J ₈₂ | ISL78226 | Installed 2-3 | ADDR2 |
| | ISL78224 | N/A | Configures as master |
| J ₈₈ | ISL78226 | No Jumper | DE/CCM |
| | ISL78224 | No Jumper | Remove for software operation |
| J ₈₉ | ISL78226 | No Jumper | HIC/LAT |
| | ISL78224 | No Jumper | Remove for software operation |
| JP ₃₁₀ | ISL78226 | Installed | Jumper to enable Phase 3 |
| | ISL78224 | N/A | |
| JP ₄₁₀ | ISL78226 | Installed | Jumper to enable Phase 4 |
| | ISL78224 | N/A | |
| JP ₅₁₀ | ISL78226 | Installed | Jumper to enable Phase 5 |
| | ISL78224 | N/A | |
| JP ₆₁₀ | ISL78226 | Installed | Jumper to enable Phase 6 |
| | ISL78224 | N/A | |

Table 4. Jumper Configuration (Continued)

- (3) Connect the DC electronic load or 48V battery to one or more of the BAT48 connectors. See Figure 55 for ISL78226 connections and Figure 56 for ISL78224 connections. Note: the PCB connects all BAT48 phases together and all BAT48 PGNDs together. For high power evaluations, Renesas recommends connecting the 48V load or battery to all six phases for distribution of power across the board.
- (4) Connect a 12V supply or battery to one or more of the BAT12 connectors. See Figure 55 for ISL78226 connections and Figure 56 for ISL78224 connections. Note: the PCB connects all BAT12 phases together and all BAT12 PGNDs together. For high power evaluations, Renesas recommends connecting the 12V supply or battery to all six phases for distribution of power across the board.
- (5) Connect a 12V supply to the VIN and VIN_FLY with its ground connected to FLYGND. Disconnect the 5V supply from BAT12_IN if it was previously connected. See <u>Figure 55</u> for ISL78226 connections and <u>Figure 56</u> for ISL78224 connections. The evaluation board has a diode to prevent the reverse current flowing from the BAT12 supply to the 5V supply so the 5V supply can be safely disconnected. A normal application circuit has a 12V battery for precharge and the BAT12_IN voltage is not required.
- (6) Connect probes as shown in <u>Table 2</u> and <u>Figure 16</u> or <u>17</u>. Note: Renesas recommends disabling the part through the software and turning off all supplies before making connections to the board.
- (7) Turn on the 12V supplies, 5V supplies, and the 48V supply (no particular power supply sequence).

- (8) The first time you power up the board after configuring the board for Boost mode operation, verify the operation is set to Boost mode.
- (a) In the software, navigate to the Quick Access Control Panel under Mode Pin Selection.
- (b) Select Boost mode from the BT/BK drop-down menu.
- (c) Click the **Enable** button at the top of the Quick Access Control Panel. The indicator next to the **Enable** button turns red.
- (d) Verify the flyback circuit is working by measuring the voltages at V6 and V12 (see Figure 55 for ISL78226 connections and Figure 56 for ISL78224 connections). V6 should measure about 6V and V12 should measure around 12V. If the V6 and V12 measurements are correct, the controller is running and providing the proper clock signal to the flyback circuit. If the measurements are correct, proceed to Step <u>9</u>.
- (9) To automatically start the converter, click the Read Startup Files Options button shown in Figure 22. This loads the startup.csv file in the project directory that specifies startup options that set initial device settings. Note: You can manually edit the file.

| 🖬 ISL7 | 8224 4-Phase Bi-D | irectional Synchro |
|--|---------------------------------|---------------------------|
| About | | |
| Control Registers Config & Status Alert Display | | |
| Control Regs (Hex) Status Regs (Hex) Startup Options | RSVD | RSVD |
| - Startup Read Startup File Options | Device ID / Revis Devicec ID | sion / Write Enable)s |
| Auto Load File Name ISL7822X_Configuration_Default.csv Startup Configuration Image: Startup Configuration Image: Startup Configuration | AD | - R Master |
| Read ID and Revision Enable Writes (0x10 = 0) Update Device Control Registers from File Clear Faults Set PWM Read Control and Status Registers (I2C) | Device Re | - R Master |
| Sample Interval (mSec) 300 mSec Set Sample Intervals | Write Ena | able |

Figure 22. Read Startup File Options



(10) Click **Execute Startup**. The program sets the initial device registers as well as the GUI controls and value windows.

| ISL782 | 24 4-Phase Bi-Dire | ectional Synchro |
|--|----------------------|------------------|
| About | | |
| Control Registers Config & Status Alert Display | | |
| Control Regs (Hex) Status Regs (Hex) Startup Options | RSVD | RSVD |
| Startup | Device ID / Revision | n / Write Enable |
| Read Startup File Options Execute Startup | Devicec IDs | |
| ✓ Auto Load File Name ISL7822X_Configuration_Default.csv | AD | R Master |
| Startup Configuration | | |
| ▼ Set Enable On (Device On GPIO EN Pin 1) | | |
| | | |
| 🔽 Read ID and Revision | | |
| Enable Writes (0x10 = 0) | Device Revis | ion |
| Update Device Control Registers from File | AE | Master |
| 🔽 Clear Faults | | |
| I Set PWM | | |
| Read Control and Status Registers (I2C) | | |
| | | |
| Sample Interval (mSec) 1000 mSec Set Sample Intervals | Write Enable | |
| | | Master |
| | 110 R 00 | W |

Figure 23. Execute Startup

(11) Observe the Startup Running window for several seconds.

| ISL7822 | 4 4-Phase Bi-Direct | tional Synchro |
|--|---------------------------------------|----------------|
| About | | |
| Control Registers Config & Status Alert Display | | |
| Control Regs (Hex) Status Regs (Hex) Startup Options | RSVD | RSVD |
| Startup V Auto Load File Name ISL7822X_Configuration_Default.csv | Device ID / Revision / Devicec IDs | Write Enable |
| Startup Configuration Image: Startup Configuration | | |
| Enable Writes (0x10 = 0) Update Device Control Registers from File Clear Faults Set PWM Read Control and Status Registers (I2C) | Device Revision | R Master 👩 |
| Sample Interval (mSec) 1000 mSec Set Sample Intervals | Write Enable | w Master o |





(12) Wait for the "Startup Completed" message to display. The setup process takes a few seconds to complete.



Figure 25. Startup Completed

The Quick Access Control Panel in Figure 26 shows the status for multi-chip operation with one master and three slaves.

Figure 26. Master and Three Slave Selection

To simplify the screen for single master operation, click the **Master** box in the **Active Devices** section of the Startup Options screen and click the **Set Multi-Device Displays per Checked Boxes** bar. Figure 27 on page 23 shows the **Startup Options** and the Quick Access Control Panel for this configuration.





Figure 27. Master Only Selection



4. Overview - Using the Software

4.1 Quick Access Control Panel

Figure 28 shows the Quick Access Control Panel configured as a single master with zero slaves.

| System Control | \$ |
|-----------------|-------------------------------|
| Code ADR | Disable • IEN D ACK 382 |
| ⊂ Mode Pins Se | |
| BT/BK | |
| PWM EN | ON V |
| Mode Selection | |
| DE / CCM | DE |
| HIC / LAT | Hiccup - |
| | |
| KSYS C | DrvEN |
| Alert / Fault F | legisters |
| AL DF | DE DD DC DA D9 |
| | |
| | |
| D8 D7 | D6 D5 D4 D3 D2 |
| | |
| | |
| GPIO: XSTAT | imers (Polling) |
| | |
| 12C: 0xC | |
| 300 mSec | Update Interval |

Figure 28. One Master and Zero Slaves



System Controls Enable • Disable EN EN Code ADR M 4C S1 4D S2 4E III S3 4F IIII Mode Pins Selection BT/BK Buck PWM EN ON -Mode Selection DE / CCM DE HIC / LAT Hiccup -KSYS DrvEN Alert / Fault Registers AL DF DE DD **S**3 GUI Sample Timers (Polling) SPIO: XSTAT XHIC XSY Go I2C: 0xC0 Alerts Go 300 Update Interval

Figure 29 shows the Quick Access Control Panel configured as a master with three slaves.

Figure 29. One Master and Three Slaves

The controllers can be configured with up to four devices. **Note:** The customer evaluation boards are equipped for single controller operation only. See the <u>ISL78226</u> and <u>ISL78224</u> datasheets for information about multi-chip operation. Notice the red ACK (acknowledgment) for the slave devices indicates a failed transfer, because no slaves are connected.

The Quick Access Control Panel shows the top level status of all devices.

4.1.1 System Controls

The top portion of the **System Controls** section controls the main EN (enable) pin for turning the master device on and off. Click **Enable** to bring up the internal LDO and enable I²C communications.

The ID window (device ID) and ADR window (I²C addresses) are located below Enable in the System Controls panel. The ID Register I²C read back value is displayed along with a Green or Red indicator for I²C Acknowledge.

4.1.2 Mode Pins Selection

The Mode Pins Selection section controls the GPIO interface pins.

Figure 29 shows five GPIO pins being controlled: four in the **Mode Pins Selection** section and the main Enable pin above. Below the GPIO pins, five status pins are also monitored (PGMCU, XSTAT, XHIC, XSYS, and DrvEN).



4.1.3 Alert/Fault Registers

A main function of the ISL78226 and ISL78224 is to monitor the many different digital and analog fault indicators. As many as 70 different conditions are monitored. However, the controllers have a digital architecture to simplify the verification of these indicators. A common Fault Index Register provides a top level way to check the status conditions. Each bit in the Fault Index Register (0xC0) indicates that one or more of eight different fault registers is active. By reading Register 0xC0 with a single I²C byte read transaction, the controller can check all 56+ fault indicators.

The ideal design target has minimal overhead, a single I²C byte read, and all faults can be monitored. The discrete outputs monitored in **Mode Pins Selection** (XSTAT, XHIC, XSYS) can also be used as a total monitor of all fault conditions.

4.1.4 GUI Sample Timers (Polling)

This section enables timer controlled polling. The software has two different timers that both sample all I^2C fault registers (0xC0, 0xD2 to 0xDA) and system status registers (0xDC, 0xDD, and 0xDF).

Click Go to enable timer controlled polling, which continues until you click Stop.

The software reads all fault registers and system status registers during every poll.

Note: When polling is active, all other software inputs are disabled. To enable them, click **Go** again to stop polling.

4.1.5 Quick Access Control Panel Summary

The Quick Access Control Panel design enables a quick power down using the EN or PWM_EN GPIO controls. If polling is enabled, the panel provides a visual monitor if the GPIO pins or the 0xC0 fault index register detect faults. Therefore, the screen design provides the ability to detect faults and power down the device quickly no matter which tab is active.

4.2 Understanding Device Operation

Although the analog aspects of the buck/boost process and the related multiple phase circuitry are key to successful performance, it is easier to understand device operation from a digital standpoint. The <u>RegisterDefinitions</u> provide detailed register definitions for both control registers and status registers.

The spreadsheet workbook has two tabs, Control Regs and Status Reg.

| 139 | | | | |
|-----|---|--------------|------------|-----|
| 140 | | | | |
| | • | Control_Regs | Status_Reg | (+) |

Review the control and status registers for an overview of the controller's major functions.

4.2.1 Control Registers 0xB0 - 0xBF

The first tab in the spreadsheet lists the control registers. These registers are both readable and writable and control the operational aspects of the device.

4.2.2 Fault and Status Registers 0xC0, 0xD2-0xDF

The second tab in the spreadsheet lists the status registers. While the ISL78226 and ISL78224 control Buck/Boost and Phase operation, the system status is also monitored in real time. This information includes many Faults/Alert functions. In addition, the system status registers feedback from programmed conditions and self adjusting operating parameters.



4.2.3 Register Summary Overview

50% of the digital capability is focused on control and 50% is focused on monitoring. This also drives the tabs of the software.

4.3 Tab Overviews

Figures 30 shows the tabs.

| Control Regs (Hex) | Status Regs (Hex) | Startup Options | Test Access | RSVD | RSVD | RSVD |
|--------------------|----------------------|-----------------|-------------|--------------|-------------------------|-----------------|
| Control Registers | Config & Status | Alert Display | | | | |
| ☞ Master C S1 C | S2 C S3 Read Registe | er Settings | | S1 🔽 S2 🔽 S3 | Write Register Settings | ⊢ Auto Write |

Figure 30. Display Tabs

4.3.1 Startup Options Tab

The **Startup Options** tab configures the first options after the software connects to the USB dongle as shown in Figure 27 on page 23.

Although a certain amount of startup automated convenience is desirable when working with the ISL78226 and ISL78224, sometimes only operator requested specific actions take place. A portion of this tab deals with operator options for initializing the device and the project software/hardware.

Other portions of this tab deal with basic functions such as reading the ID register, reading the revision level, and enabling register writes. This tab also controls some requested general purpose register access tools that enable you to access any register.

The **Active Devices** portion allows you to force the active devices setting (Master, Slave 1, Slave 2, and Slave 3). This tab is mostly used during program development, but also helps convey master to slave signal/interconnect.

4.3.2 Alert Display Tab

The **Alert Display** tab displays all Faults/Alerts and is shown in <u>Figure 47 on page 38</u>. The information is presented in datasheet terminology. Faults that go active change the indicator color to dark red. Use the macro buttons to clear faults.

4.3.3 Control Registers Tab

The **Control Registers** tab (shown in <u>Figure 39 on page 33</u>) provides a user-level way to interactively select specific options related to each register. English language settings enable you to better understand functional operation.

4.3.4 Config & Status Tab

The **Config & Status** tab displays device conditions (Registers 0xDC, 0xDD, and 0xDF) and interprets bits in the same descriptive terms used in the datasheet as shown in Figure 49 on page 39.

4.3.5 Hex Tabs

The **Control Regs (Hex)** and **Status Regs (Hex)** tabs control the basic register (Hex) contents that verify device content at the byte level and are useful for verifying firmware performance during development.



4.3.5.1 Control Regs (Hex) Tab

The **Control Regs (Hex)** tab allows you to directly read and write hex data to each register location as shown in Figure 38 on page 32. These bidirectional registers set up the device operation.

This tab enables the basic read/write for all active devices and contains buttons that enable you to write to and read from configuration files. You can also use the buttons to create and load new files.

Note: use the **Save Configuration File** button to save user-developed specific settings. If you do not save these settings, you must reprogram all the operational options from scratch after each power up. See <u>"Editing Startup Files for Fault Response" on page 35</u> and <u>"Quick Start Videos" on page 6</u> for more information about using the software.

4.3.5.2 Status Regs (Hex) Tab

The **Status Regs (Hex)** tab is similar to the **Control Regs (Hex)** tab except these registers are read only. The tab is shown in Figure 46 on page 37. There is no provision for initialization of these registers. This tab also accommodates configurations of one to four devices.



5. Using the Software - Detailed

The following section details the main features of the software.

5.1 Startup

5.1.1 Startup Options Tab

The **Startup Options** tab (<u>Figure 26 on page 22</u>) enables automated startup or lets you manually perform specific steps. The Automatic feature goes through the four steps shown in <u>Figure 31</u>.



Figure 31. Automatic Startup Using the Startup Tab

5.1.1.1 Startup Panel (Startup Options Tab)

Start the Automatic process in the **Startup** panel of the **Startup Options** tab. Complete the following steps to use the Automatic process.

(1) Click Read Startup File Options (see Figure 32).





Figure 32. Startup Screen

(2) The program opens the startup.csv file in the project directory.Figure 33 shows the contents of the startup.csv file.

| | A | В | С | D | E | F | G | Н | 1 |
|----|--|-------|-----------|-----------|---------|---------|---------|-------|-------|
| 1 | ISL78226 Startup File | Date | 030316 | | | | | | |
| 2 | Auto Load | True | File Name | ISL78226_ | Configu | ration_ | Default | | |
| 3 | Auto Detect | False | Master | True | Slave1 | False | Slave2 | False | Slave |
| 4 | Set Enable | True | | | | | | | |
| 5 | ReadID and Revision | True | | | | | | | |
| 6 | Enable Write 0x10 | True | | | | | | | |
| 7 | Write Control Registers and Set Status | True | | | | | | | |
| 8 | Read Control Registers Status | True | | | | | | | |
| 9 | Set Buck | True | | | | | | | |
| 10 | Set Boost | True | | | | | | | |
| 11 | Set PWM On | True | | | | | | | |
| 12 | GPIO_Sample Interval | 300 | | | | | | | |
| 13 | IC2_Sample Interval | 300 | | | | | | | |
| 1/ | | | | | | | | | |

Figure 33. Startup.csv Options Definition File

(3) The file contents set the option buttons in the Startup Configuration panel shown in Figure 34.



Figure 34. Execute Startup

- (4) After loading the file and before executing the automatic startup, you can change the startup conditions by checking or unchecking the boxes. When you are ready for startup, click **Execute Startup**.
- (5) The software executes the enabled functions specified in the **startup.csv** file. The status window turns red during processing and indicates when the process is complete. As shown in Figure 31 on page 29, various fields are updated when completed.



5.1.1.2 Device ID/Revision/Write Enable Frame

Review the datasheet and register definitions related to Address 0xAD, 0xAE, and especially Address 0x10. The Write Enable Register must be set to 0x00 to modify the contents of the ISL78226 and ISL78224 I²C registers.

| | 2 26 R M | |
|-------------|----------------|--------|
| De AE 02 | evice Revision | aster |
| | /rite Enable | Master |



5.1.1.3 User Register Access

| JSELIN | egisteri | Access | Hex | Decin | nal | ACK |
|--------|----------|--------|-----|-------|-----|-----|
| BO | 0 | R | 0 | 0 | W | • |
| CO | 0 | R | 0 | 0 | w | |
| CO | 0 | R | 0 | 0 | W | |
| CO | 0 | R | 0 | 0 | W | |



The User Register Access panel provides a general purpose tool for accessing I^2C registers. You can edit the yellow address field. After you edit the field, you can read or write the contents with a typed in hex or decimal value. A green ACK indicates a successful transfer. A red ACK indicates a failed transfer. Make sure the address is valid; if writing, register 0x10 (Write Enable) must be written with a 0x00.

5.1.1.4 GPIO Monitor Panel

<u>Figure 37</u> shows the GPIO monitor panel. The panel is used for advanced troubleshooting and displays the GPIO port read values of the Renesas dongle. Contact Renesas <u>support</u> for more information.

| Sample | GPIO P1 P2 |
|--------|------------|
| 30 | - P0 |
| 05 | - P1 |
| 00 | - P2 |

Figure 37. GPIO Monitor



5.2 Control Regs (Hex) Tab

The **Control Regs (Hex)** tab (Figure 38 on page 32) enables you to both read and write locations 0xB0 to 0xBF and 0xEC to 0xED. The tab's registers control the 60+ mode/operation settings of the ISL78226 and ISL78224. The form is designed to configure up to four controllers at a time. Figure 38 shows operation of the master controller only.

| Control Registers | Config & Status | Alert | Displ | ay | | | | | | |
|----------------------------------|--|-------------|--------|----|-----------|-------------|------|---|------|--------------------------------|
| ontrol Regs (Hex) | Status Regs (Hex) | Startup (| | | ľ | Test Access | RSVD | ľ | RSVD | RSVD |
| | | Contro | l Regi | | (R74 M | /) | | | | - I2C Comm, Statu ACK |
| Control Register | r : Tracking PINV Clea | ar Enable | | R | | w | | | | |
| 1 Individual Fault | Response 1 : BAT12∨ | olt | | R | | w | | | | Write EN (0x10=00 |
| | Response 2 : BAT48 ∨ | olt | | R | | w | | | | |
| _ | Response 3: V12/V6 | | | R | | w | | | | |
| 4 Individual Fault 5 Reserved | Individual Fault Response 4 : Fly OC ACP Fly S | | | | | w | | | | Read All Control Registers |
| _ | Response 5 : Phase R | emoval C | | R | | w | | | | Write All Control Registers |
| 7 Individual Fault | Response 6 : BAT12∨ | oltage | | R | | w | | | | |
| | Response 7 : BAT48 ∨ | olt | | R | | w | | | | Load Configuration |
| _ | Itage Setting Control | | | R | - | w | | | | from File |
| | Under Voltage Control | | | R | | w | | | | Save Configuration File |
| _ | Itage Setting Contol | | | R | | w | | | | |
| _ | e Removal Control | | | R | - | w | | | | |
| D Serious Fault Re | | | | R | | w | | | | |
| E Minimum On Tin | | | _ | R | | W | | | | Set Read = Write |
| F Maximum On Du | | | | R | | W | | | | Set Write = Read |
| C Boot Refresh Co | | | _ | R | | W | | | | |
| | t Protection Limit | | | R | | w . | | | | |
| File Name Un-Named | | | | | | | | | | |
| | | | | | | | | | | |
| | | | | | | | | | | |

Figure 38. Control Regs (Hex) Tab (After Clicking Read All Control Registers Button)

The low level hex interface form enables you to verify and write fundamental contents of each register, which is useful when troubleshooting. The displayed results can be compared to the datasheet or Excel register tables.

You can read or write to individual byte locations. Each register also has an activity indicator that changes color whenever a register is accessed.

Enter hex data in the W text box. The R text box returns the hex value of the contents of the selected register.

Use the **Read All Control Registers** button to read all values. Use the **Write All Control Registers** button to write all values. You can also write register information to a configuration file in the project directory.

The configuration file(s) enable you to store and recall device settings for all control registers, which allows you to return to multiple test setups and experiments.

The ACK indicator provides immediate feedback if I²C communication problems occur. A green ACK indicates that no communication problems occurred. A red ACK indicates a communication problem.



5.3 Control Registers Tab

The Control Registers tab is hierarchically a level up from the Control Regs (Hex) tab and is shown in Figure 39.

| out | | | | | | | | | |
|--------------------------------------|---------------------|--|-----------------------------|------------------------------|-------------------------------|-----------|---|----------|-----------------|
| Control Regs (Hex) | Status Regs (Hex) | Startup Options | Test A | ccess | RSVD | Ť | RSVD | Ϋ́ | RSVD |
| ontrol Registers 📋 | Config & Status | Alert Display | | | | | | | |
| Master | Read Reg | ister Settings | | M | | V | /rite Register Settings | | □ Auto Write |
| Fault Response Setti | ngs | | | | | | e EN (0x10=00) | 1 | |
| B0-7 Individual F Respo | | Write / Update B0-7 dividual Fault Response enable combo boxes below | | | | | e en (0x10-00) | | |
| B1-1 BAT 12 Outp | ut OV Flag 👻 | B1-3 BAT 12 Output UV | Flag 🚽 | B1-5 B/ | AT 12 Input OV | Flag | B1-7 BAT 12 | Input UV | Flag |
| B2-1 BAT 48 Outp | ut OV Flag 🚽 | B2-3 BAT 48 Output UV | Flag 👻 | B2-5 B/ | AT 48 Input OV | Flag | B2-7 BAT 48 | Input UV | Flag |
| B7-1 BAT 12 Out O | V LMT Hiccup - E | 37-3 BAT 12 Out UV LMT | Hiccup 👻 | B7-5 BAT | 12 Inp OV LMT | Hiccup | B7-7 BAT 12 Ing | ₽ UV LMT | Hiccup |
| B8-1 BAT 48 Out O | V LMT Hiccup - | 88-3 BAT 48 Out UV LMT | Hiccup 👻 | B8-5 BAT | 48 Inp OV LMT | Hiccup | → B8-7 BAT 48 Ing | D UV LMT | Hiccup |
| B3-1 V1 | 12 OV Hiccup - | B3-3 V12 UV | Hiccup 👻 | | B3-5 V6 OV | Hiccup | - B3 | -7 V6 UV | Hiccup |
| B6-7 | OC2 Hiccup - | B4-5 ACP | Hiccup 👻 | B4- | 1 Flyback OCP | Hiccup | B4-7 Flyb F | ET Short | Latch |
| BD-0 H/S FET Short XSYS_FAIL Pull | | D-4 L/S FET Short Buck XSYS_FAIL Pull Down | Enable - B | | 12 GND Short AIL Pull Down | Enable | BD-6 BAT48 GN Buck XSYS_FAIL P | | Enable |
| BD-1 H/S FET Short XSYS_FAIL Pull | | D-5 L/S FET Short Boost XSYS_FAIL Pull Down | | | | | BD-7 BAT48 GM BOOST XSYS_FAIL F | | Enable |
| Configuration Registe | er Settings | | | | | | | | |
| B9-2 BAT12 OV Warning Threshold | | AT12 OV 150% - | BA-2 BAT12 Warning Three | | _ | B6-5 Fai | ult Phase Disable 👻 Removal | | |
| BB-2 BAT48 OV Warning Threshold | | AT48 OV 125% - Threshold | BA-5 BAT48 Warning Three | | ВС | 7 V6/V1 | 2 Check Enable 👻 | | |
| BC 5-0 Individual | Phase Control PH1 (| DN 🖵 PH2 ON 🖵 PH3 | 3 ON 🚽 PH4 | ION 🔻 P | H5 ON 🚽 PHE | 5 ON 👻 | | | |
| BE-1 Minimum On | Time 340nS 👻 | BE-2 WithinDevice Curre | nt Balance | Disable 👻 | BE-3 Between | n Devices | Current Balance | sable 👻 | |
| B0-4 Tracking | Digital 🚽 | 8F-2 Maximum On Duty | 91.7% 👻 | B0- | 5 PWM Polarity | Non-Inve | erting 👻 | | |
| EC-2 Boot Refresh Interval | | oot Refresh 1/12 👻 Pulse Width | | oot Refresh nitial / Subs | | | -6 Phase Drop 1.5 n Mode Count Select | nS 🔻 | |
| ED-2 CCL Threshol | d 2.4V 👻 ED- | 5 ACP Threshold 2.7V | - | | | | | | |

Figure 39. Control Registers Tab

This tab provides information on an address-by-address basis. Therefore, the information is presented at the byte level, so you must parse the fields, review the options, and calculate the end byte value.

Figure 40 shows the 0xB8 portion of the Control Regs (Hex) tab.



Figure 40. Control Regs Hex Tab: 0xB8

The 0xB8 location content values can be read and written in hex.

The **Control Registers** tab has a much more user friendly way to set or interpret the 0xB8 contents. On the **Control Registers** Tab, the 0xB8 register is set or read using four different combo boxes highlighted in red in Figure 39 on page 33.

The <u>RegisterDefinitions</u> link provided here contains detailed register definitions for both Control Registers and Status Registers.

The combo boxes shown in Figure 41 allow only combinations recognized by the device.





Figure 41. Combo Boxes with Drop-down Selection Shown

The example byte of the control register in Figure 42 shows that one byte manages four different mode settings and that more than 60 different individual operator settings can exist.

| Name | Address | Bit | R/W | Name/ Purpose | Default Value | Description |
|--|---------|-----|-----|---|---------------|---|
| Individual Fault Response Control Register 7 | OxB8 | 0 | R/W | BAT48 Output Over Voltage Limit Fault Response Control bit | 0x0 | 0,0 =Flagging only (Default) 0,1 = Hiccup 1,0 = Latch-off 1,1 = Ignore |
| | | 1 | | | | |
| | | 2 | R/W | BAT48 Output Under Voltage Limit Fault Response Control bit | 0x0 | 0,0 = Flagging only (Default) 0,1 = Hiccup 1,0 = Latch-off 1,1 = Ignore |
| | | 3 | | | | |
| | | 4 | R/W | BAT48 Input Over Voltage Limit Fault Response Control bit | 0x0 | 0,0 = Flagging only (Default) 0,1 = Hiccup 1,0 = Latch-off 1,1 = Ignore |
| | | 5 | | | | |
| | | 6 | R/W | BAT48 Input Under Voltage Linit Fault Response Control bit | 0x0 | 0,0 = Flagging only (Default) 01 = Hiccup 10 = Latch-off 11 = Ignore |
| | | 7 | | | | |

Figure 42. Portion of Control Regs (Hex) Tab Spreadsheet

Because many of these settings can have four to eight different combinations (combo selections), there can be hundreds of operator options when determining device setup.

5.3.1 Control Register Programming

Figure 43 on page 35 shows the top section of the **Control Registers** tab. From the tab you can select which device (Master, Slave 1, Slave 2, or Slave 3) is read. The right side controls which (or all) devices are programmed during an update or write operation.

The Auto Write check box sets a flag so that the software updates registers as individual combo box selections are changed. When the Auto Write check is off, you can make several changes, but you can have them written only to the device registers when you click Write Register Settings.



| Control Regs (Hex) | Status Regs (Hex) | Startup Options | Test Access | RSVD | RSVD | RSVD |
|--------------------|----------------------|-----------------|-------------|--------------|-------------------------|-----------------|
| Control Registers | Config & Status | Alert Display | | | | |
| | S2 C S3 Read Registe | r Settings 🔲 | V M V | S1 및 S2 및 S3 | Write Register Settings | ⊢ Auto Write |

Figure 43. Control Register Programming

5.3.2 Combo Box Options

Flag: If a fault is detected, the fault response is to notify the user and continue operation.

Latch: If a fault is detected, the fault response is to shut the system down. The only way to recover is to cycle the supplies.

Hiccup: If a fault is detected, the fault response is to shut the system down and restart the system every 500ms. If a fault is still present, shut the system down and repeat until the fault is removed.

5.3.3 Fault Response Settings

A portion of the control registers in the digital domain select the actions to be taken when fault(s) occur. The software combo boxes have specific options for each register and guide you through the setup process.

5.3.4 Editing Startup Files for Fault Response

You can save fault responses in the startup file during the initial startup from the software. This option enables you to preload fault responses the next time you resume the project. Refer to the *Phase Dropping and Tracking* video to see this procedure (<u>"Quick Start Videos" on page 6</u>). The selection discussing saving fault responses to a file is at the end of the video.

Complete the following steps to set the fault responses for the input and output UV and OV limits from the **Control Registers** tab.

- (1) You can set the fault response for the input and output UV and OV limits from the Control Registers tab (Figure 39 on page 33). In the Fault Response Settings section of the Control Registers tab, change the combo box from Disabled to Enabled and click the yellow Write / Update B0-7 Individual Fault Response button beside the Enable/Disable combo box. This setting enables all the fault responses to be changed from their individual combo boxes.
- (2) When the fault responses have been set, click **Write Register Settings** (top right of the **Control Registers** tab) to save the fault responses.
- (3) Click Read Register Settings (top left of the Control Register tab) to verify the settings have been saved.
- (4) To save these settings to a file for later use, click the Control Regs (Hex) tab (Figure 38 on page 32).
- (5) Click Save Configuration File (lower right side of the Control Regs (Hex) tab).
- (6) A pop-up window prompts you to save the file on the C: drive. If the default locations are selected when the software is loaded, click **Open** to save the file to this location on the C: drive (C:PC8\Users\Public\ISL78226).

Complete the following steps to reload the fault response settings at startup.

- (7) Click Read Startup File Option (yellow button) in the Startup Options tab (Figure 26 on page 22).
- (8) Check the box beside Update Device Control Registers from File.
- (9) Check the box beside **Read Control and Status Registers (I²C)**.
- (10) Click the yellow Execute Startup button. The saved fault responses are now loaded into the controller.

Complete the following steps to confirm the fault responses have been loaded into the registers.

- (11) Click the Control Registers tab (Figure 39 on page 33).
- (12) In the Fault Response Setting section, change the combo box from Disabled to Enabled.
- (13) Click the yellow **Write / Update B0-7 Individual Fault Response** button beside the **Enable/Disable** combo box. The fault responses for the individual faults are now indicated in the combo boxes.



5.3.5 Configuration Register Settings

From a device operation viewpoint, several parameters can be varied based on your application. These options can modify analog thresholds or set digital mode options. The combo boxes allow only combinations recognized by the device.

The **Control Registers** tab enables programming of many device settings with hundreds of options. The drop-down combo boxes shown in <u>Figure 44 on page 36</u> provide an English language indication of each possible option.

Note that each description label contains a reference to a hex value coupled with a bit value as well. For example, "B9-2" designates location 0xB9, and Bit 2 designates a location definition. This information helps clarify specifically which register bits are read or written in the associated combo box.

| B9-2 BAT12 OV Threshold | 115% | - |
|----------------------------|------|---|
| Inresnoid | | |

Figure 44. Description Label in Control Reg Tab

In Figure 44, the label and combo box refer to the entry in Figure 45 from the Excel register definitions file.

| Name | Address | Bit | R/W | Name/ Purpose | Default Value | Description |
|-----------------|---------|-----|-----|---------------|------------------|---|
| | 0xB9 | 2:0 | R/W | BAT12 Over | 0x0 | BAT12 is higher than the Target Voltage |
| Voltage Setting | | | | Voltage | | 000=115% (Default), |
| Register | | | | Threshold | | 001=110%, |
| | | | | Control | | 010=120%, |
| | | | | | | 011=125%, |
| | | | | | | 100=130%, |
| | | | | | | 101=135%, |
| | | | | | | 110=140%, |
| | | | | | | 111=145%. |

Figure 45. Excel Register Definitions File

5.4 Status Regs (Hex) Tab

The second half of the ISL78226 and ISL78224 device registers address the important faults/alerts monitoring capability of the controllers. These registers address Fault detection (Fault Status: 0xD0 to 0xDA) and observation of dynamic operating conditions such as operating conditions that can change as the device runs (System Status: 0xDC, 0xDD, and 0xDF).

This tab also enables a quick and direct way for you to verify actual register contents, which is useful during development and verification work.

Each location can be individually read using the R button. The Read All Status button provides a read all function.

The I²C **ACK** indicator reveals if successful access occurs. Each location has an activity indicator that changes color whenever a register is accessed (see Figure 46 on page 37).

See the "Fault Index Register 0xC0" section in the datasheet or the Excel file <u>RegisterDefinitions</u>. This fault register serves as a "Master Flag" indicator to signify a non-zero (active fault) condition in registers 0xD2 to 0xDF.


| Ţ | ISL78226 6-Phase Bi-I | Directi | ional Synch | ronous PW | /M Controlle | | | | |
|--------|--|------------------------|-----------------|-----------------|--------------|------------------|--|--|--|
| About | | | | | | | | | |
| Cor | trol Registers Config & Status Alert Display | | | | | | | | |
| Contro | Regs (Hex) Status Regs (Hex) Startup Options RSVD | | RSVD | Ĭ | RSVD | RSVD | | | |
| | м | | Fault and Syste | em Registers (F | Read Only) | 12C Comm. Status | | | |
| CO F | ault Index Register 84 R | | | | | ACK | | | |
| · · | | M | 4 | | | | | | |
| | | <u></u> | 10 | | | | | | |
| D2 | FSR 1: (BAT12/ BAT48 Input & Output Power Good Fault) | <u> </u> | в | | | | | | |
| D3 | FSR 2: (Device Power Supply Status: Flyback Power Good: Over Current : VIN OV) | 00 | B | | | | | | |
| D4 | Fault Status Register 3: (LDO Outputs (MCU_LCO/ PVCC) Power Good) | 20 | в | | | | | | |
| D5 | Fault Status Register 4 | 00 | R | | | | | | |
| D6 | Fault Status Register 5 (Serious Over Current Fault) | 00 | R ^O | | | | | | |
| D7 | Fault Status Register 6 (BAT12/BAT48 OVP) | 00 | в | | | | | | |
| D8 | Fault Status Register 7 (Serious Fault) | 00 | в | | | | | | |
| D9 | Fault Status Register 10 (Fault Phase Indicator) | 00 | R | | | | | | |
| DA | Fault Status Register 11 (Fault Phase Indicator) | 00 | R | | | | | | |
| DB | Reserved | $\left[\cdot \right]$ | R [●] | | | | | | |
| DC | System Status Register 1 | BO | R ^O | | | | | | |
| DD | System Status Register 2 | | r ^o | | | | | | |
| DE | System Status Register 3 (Reserved) | 10 | R | | | | | | |
| DF | System Status Register 4 | OE | R | | | | | | |
| | B0-6 CLEAR FAULTs | | | | | | | | |
| Read | Read All Status Toggle PWM-EN Pin 13 | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | _ | | | | | | | |

Figure 46. ISL78226 Status Regs (Hex) Tab

5.5 Alert Display Tab

The Alert Display and Config & Status tabs serve as the "next step up" to the Status Regs (Hex) tab.

Just as the **Control Registers** tab provides a user-friendly interface to control registers, the **Alert Display** and **Config & Status** tabs help you interpret the read only registers. Specifically, the **Alert Display** tab provides a visual indication of the Fault Registers (0xD2 to 0xDA).

5.5.1 Alert Display Tab Buttons

The Alert Display tab has several buttons for debugging the design. Update Status reads all registers and displays their values. Clear Faults and Toggle PWM_EN perform interconnect sequences as described in the datasheet. Clear I²C Error performs an internal device reset on the I²C state machine.

As polling runs, **Update Status** is executed automatically once per second. A red window indicates an active fault. Figure 47 on page 38 shows the **Alert Display** tab with a single master configuration. The dark red cells indicate that a fault condition was detected.



| About Control Regitters Contro | ISL78224 4-Phase Bi-Directional Synchronous PWM Controller | _ 🗆 🗙 |
|---|---|---------------------|
| Control Registres Config & Status Alert Display Alert / Status Flags Dydae Status Alert Display Alert / Status Flags Dydae Status Alert Display Alert / Status Flags Fault Reg 10 D Fault Reg 10 D Fault Reg 2 | About | |
| Aleric / Status Flags 0.0-6 CLEAR FAULTS Toggle PWH-EN Pin 13 Auto Clear Fault Fault Reg 10 D9 Fault Reg 2 D3 Fault Reg 2 D4 Fault Reg 2 D7 Fault Reg 2 D7 Fault Reg 10 D9 Fault Reg 1 DA Sye Status 1 DC (Sys. Status 2 DD (Sys. Status 4 DF) Mode Pins Selection Mater Error Status Flags D3-4 Flyback CC IZC Comm Error D8-0 HS NHOS D8-1 LS NHOS D8-1 LS TO SHORT D4-4 RCU VDD DV D3-4 Flyback CC IZC Comm Error D8-0 HS NHOS D8-2 LS NHOS D8-1 BAT12 CMD Bas BAT48 CMB D3-7 DR Event: D3-6 BAT12 UVLO D6-2 CONT OC2 D8-0 HS NHOS D4-0 PVCC NG D3-5 VIN OV D5-5 ACP D5-7 TSD D2-0 BAT12 UVLO D6-2 CANT OC2 D8-2 VIZ OV D7-4 BAT48 CMP D2-5 BAT48 INPUT D2-7 BAT48 INPUT D2-8 BAT48 INPUT D2-8 BAT48 INPUT D2-7 BAT48 INPUT D3-1 V6 UV D3-0 V6 OV D3-3 VI2 UV D3-2 VI2 OV DF-5 PL COMP DF-7 FSYNC D5-4 CCL AL OF DE D0 DC DA D8 D5-0 OC1 LINT D7-2 BAT12 UNPUT OV-2 BAT12 INPUT OV-2 BAT48 OUT D7-5 BA | Control Regs (Hex) Status Regs (Hex) Startup Options RSVD RSVD RSVD RSVD RSVD RSVD | System Controls |
| Arter 1 Status Flags BD-6 CLEAR FAULTS Toggle PWM-EN Pin 13 Auto Clear Faults Fault Reg 10 D2 Fault Reg 2 D3 Fault Reg 2 D4 Fault Reg 2 D0 Fault Reg 2 D4 Fault Reg 10 D9 Fault Reg 1 DA Sys Status 1 DC Sys. Status 2 DD Sys. Status 4 DF Master Euror Status Flags D4-5 ENGU VDD UV D3-4 Efyback CC IZC Comm Enror D8-0 HS NHOS D8-2 LS NHOS D8-1 BAT32 GND D8-3 BAT4E GNT D4-5 MCU VDD UV D3-4 Efyback CC IZC Comm Enror D8-0 HS NHOS D8-2 LS NHOS D8-1 BAT32 GND D8-3 BAT4E GNT D4-5 MCU VDD UV D3-4 Efyback ACC IZC Comm Enror D8-0 HS NHOS D8-2 LS NHOS D8-1 BAT32 GND D8-1 BAT32 GND D8-1 BAT32 GND D3-7 DOR Event D3-4 Efyback ACC IZC Comm Enror D8-0 HS NHOS D2-5 BAT48 GNT SIGNT SIGNT Mode Pins Selection D2-0 BAT32 D2-1 BAT12 UVLO D6-2 CONT CC2 D2-4 BAT48 D2-5 BAT48 INPUT D2-4 BAT48 D2-5 BAT48 INPUT D2-4 BAT48 INPUT D2-6 BAT48 INPUT D2-7 BAT42 INPUT ALA DF DE DD DC DA D6 D2-0 BAT32 D2-1 BAT12 UVLO D3-3 V12 UV D3-2 V12 OV D7-5 BAT48 OUT D7-6 BAT48 INPUT </td <td>Control Registers Config & Status Alert Display</td> <td></td> | Control Registers Config & Status Alert Display | |
| Oppose Status Toggle PVMH-EN Pin 13 Auto Clear Faults Fault Reg1 D2 Fault Reg2 D3 Fault Reg2 D4 Fault Reg2 D6 Fault Reg2 D7 Fault Reg2 D7 Fault Reg 10 D9 Fault Reg1 DA Sys Status 1 DC Sys. Status 2 DD Sys. Status 4 DF Matter Error Status D3-4 Rtyback OC IZC Comm Error D6-0 H5 MHOS D8-2 LS MHOS D6-1 BAT12 GND D8-2 BAT84 GMD D3-4 Rtyback OC IZC Comm Error D6-0 H5 MHOS D8-2 LS MHOS D6-1 BAT12 GND D8-2 BAT84 GMD D7/5K Buck - D3-4 Rtyback OC IZC Comm Error D6-0 H5 MHOS D8-2 LS MHOS D6-1 BAT13 GND D8-2 LS MHOS D6-1 BAT132 GND D8-2 BAT84 GMD D3-4 Rtyback OC IZC Comm Error D6-0 H5 MHOS D8-2 LS MHOS D6-1 BAT132 GND D8-2 LS MHOS D6-1 BAT132 GND D8-2 LS MHOS D6-1 BAT132 GND D8-2 MSC MIC D2-0 BAT12 D2-1 BAT12 D2-2 BAT12 INPUT D2-3 BAT12 INPUT D2-4 BAT48 D2-5 BAT48 INPUT D2-2 BAT88 INPU | | |
| Fault IndexxCD0 Fault Reg2 D2 Fault Reg2 D4 Fault Reg3 D4 Fault Reg2 D5 Fault Reg2 D7 Fault Reg2 D7 Fault Reg 10 D9 Fault Reg1 DA Sys Status 1 DC Sys. Status 2 D0 Sys. Status 4 DF Matter Enor Status Flags D2-4 BX184 GMD BD-1 BAT12 GND BD-3 BAT48 GMD D4-5 MCU VDD UV D2-4 Hyback OC IZC Comm Error D8-0 HIS NHOS D8-2 LS NHOS D8-1 BAT12 GND BD-3 BAT48 GMD D4-4 MCU VDD OV D8-4 Hyback FET Short Cleari20 Error D8-0 HIS NHOS D8-1 BAT12 GND BD-3 BAT48 GMD D3-7 POR Event D3-6 BAT12 UVLO D6-2 CONT OC2 D6-8 BAT32 UVLO D6-2 CONT OC2 D6-8 BAT32 UVLO D6-2 CONT OC2 D6-8 BAT32 UVLO D5-5 TSD D3-7 POR Event D3-6 BAT12 UVLO D6-2 CONT OC2 D6-4 BAT48 D2-5 BAT48 INVIT D2-5 BAT48 INVIT D2-6 BAT48 INVIT D2-7 BAT48 INVIT D3-7 VG UV D3-0 VG OV D3-3 V12 UV D3-2 V12 UV D3-2 V12 UV D7-5 BYNC D7-6 ESYNC Constant Current D7-0 BAT132 OUT D7-2 BAT121 NPT D7-3 BAT12 INP | | Code ADR ID ACK |
| Fault Reg 10 D9 Fault Reg 11 DA Sys. Status 1 DC Sys. Status 2 DD Sys. Status 4 DF Master Error Status Flags D3-4 Flyback OC IZC Comm Error D8-0 HS NMOS D8-1 IS NMOS D8-2 LS NMOS D8-1 IS NMOS SHORT D8-0 HS NMOS D8-1 IS NMOS D8-1 IS NMOS D8-1 IS NMOS D8-1 IS NMOS D8-2 LS NMOS D8-1 IS NMOS D8-2 LS NMOS D8-1 IS | logger in extin 15 | M 4C |
| Master Error Status Flags II2C Comm Error D8-0 HS NMOS D8-2 LS NMOS D8-1 BAT12 GND D8-3 BAT48 GND D4-4 MCU VDD OV D8-4 Flyback PET Short Deval 20 Error Deval 20 Error <td< td=""><td>Fault Reg2 D2 Fault Reg2 D3 Fault Reg3 D4 Fault Reg4 D5 Fault Reg5 D6 Fault Reg5 D7 Fault Reg7 D8</td><td></td></td<> | Fault Reg2 D2 Fault Reg2 D3 Fault Reg3 D4 Fault Reg4 D5 Fault Reg5 D6 Fault Reg5 D7 Fault Reg7 D8 | |
| Master Error Status Flags II2C Comm Error D8-0 HS NMOS D8-2 LS NMOS D8-1 BAT12 GND D8-3 BAT48 GND D4-4 MCU VDD OV D8-4 Flyback PET Short Deval 20 Error Deval 20 Error <td< td=""><td></td><td></td></td<> | | |
| Master Error Status Flags 12C. Comm Error D8-0 HS NMOS D8-2 LS NMOS D8-1 BAT12 GND D8-3 BAT45 GHU PWH EN PWH EN PWH EN OFF Image: Comm Error Image: Comm Error Image: Comm Error D8-0 HS NMOS D8-2 LS NMOS D8-1 BAT12 GND D8-3 BAT45 GHU FWH EN OFF Image: Comm Error I | Fault Reg 10 D9 Fault Reg11 DA Sys Status 1 DC Sys. Status 2 DD Sys. Status 4 DF | |
| Master Error Status Flags 12C. Comm Error D8-0 HS NMOS D8-2 LS NMOS D8-1 BAT12 GND D8-3 BAT45 GHU PWH EN PWH EN PWH EN OFF Image: Comm Error Image: Comm Error Image: Comm Error D8-0 HS NMOS D8-2 LS NMOS D8-1 BAT12 GND D8-3 BAT45 GHU FWH EN OFF Image: Comm Error I | | Mada Dias Calcalian |
| D4-5 MCU VDD UV D3-4 Flyback OC I2C Comm Error D8-0 H5 KHOS D8-1 BAT12 GND D1-3 BAT48 GHB D4-4 MCU VDD OV D8-4 Flyback PET Short ICew I2C Enx D8-0 H5 KHOS D8-1 BAT12 GND D1-3 BAT48 GHB D3-7 POR Event D3-6 BAT12 UVLO D6-2 CONT OC2 D6-0 H5 KHOS D4-0 PVCC NG D3-5 VIN OV D5-5 ACP D5-7 TSD D2-0 BAT12 D2-1 BAT12 IPUT D2-4 BAT48 D2-5 BAT48 D2-6 BAT48 INPUT D2-7 BAT48 INPUT D2-4 BAT48 D2-5 BAT48 D2-6 BAT48 INPUT D2-7 BAT48 INPUT D2-4 BAT48 INPUT I | Master Fron Status Flans | |
| D4-4 MCU VDD OV D8-4 Hyback FET Shot SHOKI | D4 E MCILVOD IN D2 4 Elybert OC I2C Comm Error D8-0 HS NMOS D8-2 LS NMOS D8-1 BAT12 GND D8-3 BAT48 GND | |
| Clear I2C Error Error / Fault Status D3-7 POR Event D3-6 BAT12 UVLO D6-2 CONT OC2 D4-0 PVCC NG D3-5 VIN OV D5-5 ACP D5-7 TSD D2-0 BAT12 D2-1 BAT12 D2-2 BAT12 INPUT D2-4 BAT48 D2-5 BAT48 D2-6 BAT48 INPUT D2-7 BAT48 INPUT D2-8 BAT48 INPUT D2-7 BAT48 INPUT D2-7 BAT42 INPUT | SHORT SHORT SHORT SHORT | Mode Selection |
| D3-7 POR Event D3-6 BAT12 UVLO D6-2 CONT OC2 D6-4 CONT NOC D4-0 PVCC NG D3-5 VIN OV D5-5 ACP D5-7 TSD PFGMCU PkSTAT PkHC D2-0 BAT12 D2-1 BAT12 D2-2 BAT12 INPUT D2-3 BAT132 INPUT D2-4 BAT49 D2-5 BAT48 D2-5 BAT48 INPUT D2-7 BAT48 INPUT D2-8 BAT48 INPUT D2-7 BAT48 INPUT D2-8 BAT48 INPUT D7-7 BAT48 INPUT D2-8 BAT48 INPUT D7-7 BAT48 INPUT D7-8 BAT48 INPUT D7-7 BAT48 INPUT D7-8 BAT48 INPUT | | DE/CCM DE |
| D2-0 BAT12 OUTPUT OV OUTPUT OV OUTPUT OV D2-2 BAT12 INPUT D2-3 BAT12 INPUT OV D2-2 BAT12 INPUT D2-3 BAT12 INPUT D2-4 BAT48 OUTPUT OV OUTPUT UV OV D2-5 BAT48 INPUT D2-7 BAT48 INPUT OV D2-7 BAT48 INPUT D2-7 BAT48 INPUT OV D2-7 BAT42 INPUT D2-7 BAT442 INPUT D2-7 | Error / Fault Status | |
| D2-0 BAT12 OUTPUT OV D2-1 BAT12 OUTPUT UV D2-3 BAT12 INPUT OV D2-4 BAT48 OUTPUT UV D2-5 BAT48 INPUT OV D2-7 BAT48 INPUT OV D2-8 BAT48 INPUT OV D2-7 BAT48 INPUT OV D2-7 BAT48 INPUT OV D2-7 BAT48 INPUT OV D2-7 BAT48 INPUT OV D2-8 BAT48 INPUT OV D2-7 BAT48 INPUT OV D2-7 BAT48 INPUT OV D2-8 BAT48 INPUT OV D2-7 BAT48 INPUT OV D2-7 BAT48 INPUT OV D2-8 BAT48 INPUT OV D2-7 BAT48 INPUT | D3-7 POR Event D3-6 BAT12 UVLO D6-2 CONT OC2 D6-4 CONT NOC D4-0 PVCC NG D3-5 VIN OV D5-5 ACP D5-7 TSD | |
| D2-0 BAT12 OUTPUT OV D3-1 V6 UV D3-0 V6 OV D3-3 V12 UV D3-2 V12 OV D3-2 V12 OV D5-5 PLL COMP D5-7 FSYNC Current High OVER VOLT LIMIT D7-6 BAT12 OUT D7-6 BAT12 OUT D7-7 BAT28 INPUT OVER VOLT LIMIT D7-6 BAT12 INP D7-6 BAT12 INP D7-7 BAT28 INPUT D7-7 BAT28 INPUT D7-8 BAT12 INP D7-8 BAT12 INP D7-8 BAT12 INP D7-4 BAT12 OUT D7-7 BAT28 INPUT D7-7 BAT28 INPUT D7-7 BAT28 INPUT D7-7 BAT28 INPUT D7-7 BAT28 INPUT D7-8 BAT12 INP D7-8 BAT12 INP D7-9 | | |
| OUTPUT OV OUTPUT UV OV UV OUTPUT UV OV UV AL DF DE DD DC DA P9 D3-1 V6 UV D3-0 V6 OV D3-3 V12 UV D3-2 V12 OV DF-5 PLL COMP DF-7 FSYNC DF-6 FSYNC D5-4 CCL D7-0 BAT12 OUT D7-1 BAT12 OUT D7-2 BAT12 INP D7-4 BAT12 INP D7-4 BAT49 OUT D7-5 BAT49 INPUT D7-5 BAT48 INPUT D7-7 BAT49 INPUT | D2-0 BAT12 D2-1 BAT12 D2-2 BAT12 INPI/IT D2-3 BAT12 INPI/IT D2-4 BAT48 D2-5 BAT48 D2-5 BAT48 INPI/IT D2-7 BAT48 INPI/IT | |
| D3-1 V6 UV D3-0 V6 OV D3-3 V12 UV D7-2 BAT12 UV D7-2 BAT12 UV D7-2 BAT12 INP OVER VOLT LIMIT D7-4 BAT48 OUT D7-5 BAT48 OUT D7-5 BAT48 OUT D7-5 BAT48 OUT D7-6 BAT48 INPUT OVER VOLT LIMIT D7-6 BAT48 INPUT D7-7 BA | | |
| D3-1 V6 UV D3-0 V6 OV D3-3 V12 UV D3-2 V12 OV D5-5 PLI COMP SHORT Current High Current Low Constant Current D5-6 BAT4S INPUT OVER VOLT LIMIT D7-6 BAT4S INPUT OVER VOLT LIMIT D7-7 BAT48 INPUT OVER VOLT LIMIT D7-7 BAT48 INPUT D7-7 BAT48 INPUT OVER VOLT LIMIT D7-7 BAT48 INPUT D7-7 | | |
| SHORT Current High Current Low Constant Current D7-0 BAT12 OUT D7-2 BAT12 INP D7-3 BAT12 INP D7-4 BAT4S OUT D7-5 BAT48 OUT D7-6 BAT4S INPUT D7-7 BAT46 INP D7-0 BAT12 OUT LIMIT D7-2 BAT12 INP D7-3 BAT12 INP D7-4 BAT4S OUT D7-5 BAT48 OUT D7-7 BAT46 INP D7-7 BAT46 INP D5-0 OC1 LST D9 5:0 D5-1 OC2 LST DA 5:0 D5-2 NOC LST D9 5:0 D5-2 NO | D3-1 V6 UV D3-0 V6 OV D3-3 V12 UV D3-2 V12 OV DF-5 PLL COMP DF-7 FSYNC DF-6 FSYNC D5-4 CCL | |
| OVER VOLT LIMIT UNDR VOLT LIMIT OVER VOLT LIMIT UNDR VOLT LIMIT OVER VOLT LIMI | | |
| OVER VOLT LIMIT UNDR VOLT LIMIT OVER VOLT LIMIT UNDR VOLT LIMIT OVER VOLT LIMI | | |
| D5-0 OC1 LST D9 5:0 D5-1 OC2 LST D9 5:0 D5-2 NOC LST D9 5:0 M P1 P2 P3 P4 P1 P2 P3 P4 GUI Sample Timers (Polling) GPI0: XSTAT XHIC XSYS Go • 12:: 0xC0 Alerts Go • | D7-0 BAT12 OUT D7-1 BAT12 OUT D7-2 BAT12 INP D7-3 BAT12 INP D7-4 BAT48 OUT D7-5 BAT48 OUT D7-6 BAT48 INPUT D7-7 BAT48 INPUT | |
| DS-0 OC1 LST D9 5:0 D5-1 OC2 LST DA 5:0 D5-2 NOC LST D9 5:0 M P1 P2 P3 P4 P1 P2 P3 P4 P1 P2 P3 P4 B1 | OVER VOLT LIMIT UNDR VOLT LIMIT OVER VOLT LIMIT UNDR VOLT LIMIT OVER VOLT LIMIT UNDR VOLT LIMIT UNDR VOLT LIMIT | |
| M P1 P2 P3 P4 P1 P2 P3 P4 P2 P3 P4 GUI Sample Timers (Polling) GPI0: XSTAT XHC XSYS Go 12C: 0xC0 Alerts Go | | |
| M P1 P2 P3 P4 P1 P2 P3 P4 P2 P3 P4 GUI Sample Timers (Polling) GPI0: XSTAT XHC XSYS Go 12C: 0xC0 Alerts Go | | |
| GUI Sample Timers (Polling) GPI0: XSTAT XHIC XSVS Go 12C: 0xC0 Alerts Go | | |
| GPI0: XSTAT XHIC XSYS Go ● 12C: 0xC0 Alerts Go ● | M P1 P2 P3 P4 P1 P2 P3 P4 P1 P2 P3 P4 | |
| I2C: 0xC0 Alerts Go | | |
| | | |
| 300 mSec Update Interval | | |
| | | Update Interval |

Figure 47. Alert Display Tab Buttons Master Only

Figure 48 shows the form operating with one master and three slaves.

| Control Regs (Hex) | Status Regs (Hex) | Startup Options | RSVD | RSVD | RSVD | RSVD | | | | |
|---|----------------------------|--|---|-----------------------|---------------------------|-----------------------------------|--|--|--|--|
| Control Registers | Config & Status | Alert Display | | | | | | | | |
| Alerts / Status Flags | | | | | | | | | | |
| Update Status | C0-7 XSTAT | FLAG B0-6 | CLEAR FAULTS | | | | | | | |
| Toggle PWM-EN Pin 13 Auto Clear Faults | | | | | | | | | | |
| Fault Index C0 | Fault Reg1 D2 | ault Reg2 D3 Fault F | Reg3 D4 Fault Reg4 I | D5 Fault Reg5 D6 | Fault Reg6 D7 | Fault Reg7 D8 | | | | |
| M S1 S2 S3 | | | | | | | | | | |
| Fault Reg 10 D9 | Fault Reg11 DA | Sys Sta | atus 1 DC Sys. Status 2 | DD Sys. Status 4 DF | | | | | | |
| M S1 S2 S3 | M S1 S2 S3 | | S2 S3 M S1 S2 | S3 M S1 S2 S3 | | | | | | |
| | | M S1 | S2 S3 M S1 S2 | 53 M 51 52 53 | | | | | | |
| Master Error Status | Flags | I2C Comn | Error D8-0 HS | IMOS D8-2 LS NMOS | D8-1 BAT12 GND | | | | | |
| D4-5 MCU VDD U | V D3-4 Flyba | ck OC | S2 S3 SHOR | | SHORT | SHORT | | | | |
| D4-4 MCU VDD O | V D8-4 Flyback | FET Short Clear I2C | M C1 C | 2 S3 M S1 S2 S | 3 M S1 S2 S3 | M S1 S2 S3 | | | | |
| rror / Fault Status — | | | | | · · · · · | , , , , | | | | |
| | 03-6 BAT12 UVLO D | 5-2 CONT OC2 D6-4 C | ONT NOC D4-0 PVC | C NG D3-5 VIN OV | D5-5 ACP | D5-7 TSD | | | | |
| | M S1 S2 S3 M | | S2 M S1 S | | 3 M S1 S2 S3 | M S1 S2 S3 | | | | |
| M 31 32 33 | m 31 32 33 m | 31 32 M 31 | 32 11 31 3 | 2 33 1 1 31 32 3 | | | | | | |
| D2-0 BAT12 OUTPUT OV | D2-1 BAT12 D2 OUTPUT UV | | T12 INPUT D2-4 BA JV OUPUT | | D2-6 BAT48 INPUT OV | D2-7 BAT48 INPUT UV | | | | |
| | M S1 S2 S3 M | | S2 S3 M S1 S | | | M S1 S2 S3 | | | | |
| | | | | | | | | | | |
| D3-1 V6 UV | D3-0 V6 OV | D3-3 V12 UV D3-2 | V12 OV DF-5 PLL C SHOR | | DF-6 FSYNC Current Low | D5-4 CCL Constant Current | | | | |
| M S1 S2 S3 | M S1 S2 S3 M | S1 S2 S3 M S1 | S2 S3 M S1 S | | | M S1 S2 S3 | | | | |
| | | | | | | | | | | |
| D7-0 BAT12 OUT | | 7-2 BAT12 INP D7-3 BA R VOLT LIMIT UNDR V | AT12 INP D7-4 BAT4 OLT LIMIT OVER VOLT | | | D7-7 BAT48 INP UNDR VOLT LIMIT | | | | |
| | M S1 S2 S3 M | S1 S2 S3 M S1 | S2 S3 M S1 S | | 3 M S1 S2 S3 | M S1 S2 S3 | | | | |
| | | | | | | | | | | |
| D5-0 OC1 LST D9 5:0 D5-1 OC2 LST DA 5:0 D5-2 NOC LST D9 5:0 | | | | | | | | | | |
| M P1 P2 P3 | | P2 P3 P4 P5 P6 | P1 P2 P3 P4 P5 | | | | | | | |
| S1 P1 P2 P3 | | P2 P3 P4 P5 P6 | | P6 | | | | | | |
| S2 P1 P2 P3 | P4 P5 P6 P1 | P2 P3 P4 P5 P6 | | P6 | | | | | | |
| S3 P1 P2 P3 | P4 P5 P6 P1 | P2 P3 P4 P5 P6 | | P6 | | | | | | |
| | | | | | | | | | | |

Figure 48. Alerts Display Tab with Four Active Devices

The Auto Clear Faults check box at the top of the form provides options during polling. Auto Clear Faults is used during testing to automatically clear faults, which is useful for simulating various faults when polling is active.



5.6 Config & Status Tab

The **Config & Status** tab shown in <u>Figure 49</u> deals specifically with the system status registers (0xDC, 0xDD, and 0xDF). Like the alert registers, these registers are read only. However, these registers are general information registers.

| Control Regs (Hex) Status Reg | gs (Hex) Startı | up Options | RSVD | RSVD | RSVD | RSVD | | | | | |
|--------------------------------------|------------------------------|----------------------------|--------------------------------|---------------|-------------|-------------------|--|--|--|--|--|
| Control Registers Config & S | tatus Alert (| Display | | | | | | | | | |
| Update Status BO-6 CLEAR FAULT FLAGS | | | | | | | | | | | |
| System Status Register 1 0xDC | | | | | | | | | | | |
| Device DC-7 PWM Output Ready | DC-5 PWM Output Mode | DC-4 Protection Mode | DC-3 Switching Mode | DC-2 Position | DC-0 BT/BK | | | | | | |
| M 0x4C Driver Enabled 3 | 3 State | Hiccup | DE_Mode | Master | Buck Mode | | | | | | |
| | | | | | | | | | | | |
| System Status Register 2 OxDD | | | | | | | | | | | |
| Device DD-6 Maximum Phase | DD-3 Operatin Phase | | ase Drop / Disable | | | | | | | | |
| M 0x4C 000 6 Phase | 110 2 Phase | Phase Dro | p Enabled | | | | | | | | |
| | | | | | | | | | | | |
| | | | | | | | | | | | |
| System Status Register 4 OxDF | | | | | | | | | | | |
| | F-6 FSYNC DF-5 gh Current | PLL Short DF-4 C Source | Clock DF-3 Soft Change Done | | | 0 Clock Jource | | | | | |
| M 0x4C FSYNC Normal FSY | NC Normal PLL N | ORMAL CLK Sta | able Normal | SS Done | Locked Inte | rnal | | | | | |
| | | | | | | | | | | | |
| | | | | | | | | | | | |
| | | | | | | | | | | | |

Figure 49. Config & Status Tab

The system status registers provide two functions:

- (1) They provide a read-back that verifies how the setup programming has been interpreted. The part read-back indicates the processes mode selections are as desired.
- (2) They provide real-time feedback of device "on-the-fly" decision making. The ISL78226 or ISL78224 is constantly calculating proper mode adjustment as conditions change. The registers provide a real-time window of the functionality of the device internal mode controls and adjustments. Like the other step-up tabs, this tab provides an English language interpretation of the read hex value.

Review the register information about the system status registers. As <u>Figure 50 on page 40</u> shows, location 0xDD provides mode setting verification (Bits 6, 5, 4, and 0) and real time status (Bits 3, 2, and 1).



ISL78226EVKIT1Z, ISL78224EVKIT2Z

| Name | Address | Bit | R/ W | Name/ Purpose | Default Value | Description | Comment |
|----------------------|---------|-----|---------|----------------------------------|--|---|--|
| | | о | R | Phase Drop Enable/Disa ble | 0×0 | -1 = Phase Drop Disabled -0 = Phase Drop Enabled | Reflecting PD_CTRL pin configuration |
| | | 1 | | Operating Phase (While in | | 1,1,1 = 6-phase 1,0,1 = 4-phase 0,1,1 = 3-phase | |
| System | | 2 | R | | e in 0x0 0,0,1 = not assigned 0pera 1,1,0 = 2-phase Reflect | 0,0,1 = not assigned 1,1,0 = 2-phase | Operating Phase count indication (Master) and Reflecting PD_0 and PD_1 pin status for Slave |
| Status Register 2 | 0xDD | з | | Operation) | | | |
| | | 4 | | Maximum | | 0,0,0 = 6-Phase 0,0,1 = 4-Phase 0,1,0 = 3-Phase | Reflecting PWM Pin Configuration at Initialization Phase If PWM5 or PWM6 = VCC, 4-Phase |
| | | 5 | R | Phase Setting | | 0,1,1 = 2-Phase 1,0,0 = 1-Phase | If PWM4 = Vcc, 3-Phase If PWM3 = VCC, 2-Phase If PWM2 = VCC, 1-Phase |
| | | 6 | | | | 1,1,1 = Setting Errot (1,1,0 and 1,0,1 are not used) | If PWM2 = VCC, I-Phase If PWM1 = VCC, Error and Latch Off |
| | | 7 | 1 | Reserved | | | 1 |

Figure 50. System Status Registers

The Update Status button calls the same routine as the Update Status button on the Alerts Display tab. A duplicate is on this tab for your convenience.

The Clear Faults Flags button is a duplicate of the same function on the Alerts Display tab.



6. Alternate Configurations

The ISL78224EVAL2Z and ISL78226EVAL1Z evaluation boards can be configured to operate without the support of the flyback converter or without the support of the external computer and GUI.

The ISL78224EVAL2Z and ISL78226EVAL1Z can be configured in buck or boost operation. Each of those can be configured without a flyback and with or without the GUI dongle.

- Buck operation of the ISL78224EVAL2Z without flyback and with the GUI
- Buck operation of the ISL78224EVAL2Z without flyback and without GPIO from the GUI
- · Boost operation of the ISL78224EVAL2Z without flyback and with the GUI
- · Boost operation of the ISL78224EVAL2Z without flyback and without GPIO from the GUI
- Buck operation of the ISL78226EVAL1Z without flyback and with the GUI
- Buck operation of the ISL78226EVAL1Z without flyback and without GPIO from the GUI
- · Boost operation of the ISL78226EVAL1Z without flyback and with the GUI
- · Boost operation of the ISL78226EVAL1Z without flyback and without GPIO from the GUI

6.1 Buck Operation of the ISL78224EVAL2Z without Flyback and with the GUI

- (1) Configure the phase drop, jumper J_1 to disable phase drop and leave it open to enable phase drop.
- (2) Connect a disabled ~48V source to the BAT48 terminal lug.
- (3) Connect a disabled electronic load to the BAT12 terminal lug.
- (4) Connect a disabled ~6V bias (~0.5A) to the BAT_IN node (TP₁₃).
- (5) All Bode plot functions are already disabled on the ISL78224EVAL2Z.
- (6) Address is already set to 0 on the ISL78224EVAL2Z.
- (7) Driver DRV_EN pins are already connected on the ISL78224EVAL2Z.
- (8) PWM TRI is already connected to VCC on the ISL78224EVAL2Z.
- (9) Remove jumper J_4 to disconnect VIN_FLY from VIN.
- (10) Connect V6 (TP_{19}) to a disabled external 6V source.
- (11) Connect VIN (TP_{14}) and V12 (TP_{18}) to a disabled external 12V source.
- (12) Connect the GUI dongle to J_{77} (GPIO) and J_{74} (I²C). Note the Pin 1 locations.
- (13) Enable the BAT48, BAT IN, V6, VIN, and V12 voltage sources.
- (14) Use the GUI to exercise the converter in buck mode and EN.
- (15) Enable can be verified by observing the presence of voltages at PVCC, VCC, MCUVDD, and CLK_OUT.
- (16) Use the GUI to exercise PWM_EN.
- (17) Observe 12V at the unloaded BAT12 output.
- (18) BAT12 can now be loaded. Maintain the FET surface temperatures below 100°C with fans.
- (19) The I²C connections at J_{74} is available using the GUI.
- (20) The 6V bias to BAT_IN is no longer needed and can be turned off at this point.
- (21) To shut down the converter:
 - (a) Turn off the BAT_IN 6V bias if present.
 - (b) Remove the BAT12 load.
 - (c) Disable PWM_EN using the GUI.
 - (d) Disable EN using the GUI.
 - (e) Turn off the V6, VIN, and V12 sources.
 - (f) Turn off the BAT48 source.



- (g) Disconnect V6 and V12.
- (22) To reconfigure for buck, flyback, and GUI operation disconnect all of the jumpers and reconfigure with the following jumpers:

(a) J₁ (Phase Drop), J₄ (VIN_FLY), J₈₀ (2-3) (TRACK), TP₂₃ (BAT48 Bode), and TP₂₄ (BAT12 Bode).

6.2 Buck operation of the ISL78224EVAL2Z without flyback and without GPIO from the GUI

- (1) Configure the phase drop, jumper J_1 to disable phase drop and leave it open to enable phase drop.
- (2) Connect a disabled ~48V source to the BAT48 terminal lug.
- (3) Connect a disabled electronic load to the BAT12 terminal lug.
- (4) Connect a disabled ~6V bias (~0.5A) to the BAT_IN node (TP_{13}).
- (5) All Bode plot functions are already disabled on the ISL78224EVAL2Z.
- (6) Address is already set to 0 on the ISL78224EVAL2Z.
- (7) Driver DRV_EN pins are already connected on the ISL78224EVAL2Z.
- (8) PWM_TRI is already connected to VCC on the ISL78224EVAL2Z.
- (9) Jumper J_{70} Pin 2 to J_{70} Pin 3 (PGND) to command buck operation.
- (10) Jumper J₈₈ Pin 2 to J₈₈ Pin 1 (VCC) to command continuous conduction mode (CCM) or J₈₈ Pin 2 to J₈₈ Pin 3 (GND) to command diode emulation mode (DE).
- (11) Jumper J₈₉ Pin 2 to J₈₉ Pin 1 (VCC) to command Latch off Fault protection (LAT) or J₈₉ Pin 2 to J₈₉ Pin 3 (GND) to command hiccup fault protection (HIC).
- (12) Remove jumper J_4 to disconnect VIN_FLY from VIN.
- (13) Connect V6 (TP_{19}) to a disabled external 6V source.
- (14) Connect VIN (TP_{14}) and V12 (TP_{18}) to a disabled external 12V source.
- (15) Enable the BAT48, BAT_IN, V6, VIN, and V12 voltage sources.
- (16) Jumper J_{58} to command enable.
- (17) Enable can be verified by observing the presence of voltages at PVCC, VCC, MCUVDD, and CLK_OUT.
- (18) Jumper J₇₇ Pin 5 to J₇₇ Pin 6 to command PWM_EN, see Figure 51. Avoid bounce to this connection.



Figure 51.

- (19) Observe 12V at the unloaded BAT12 output.
- (20) BAT12 can now be loaded. Maintain the FET surface temperatures below 100°C with fans.
- (21) The I²C connections at J_{74} remains available for use, with or without the GUI dongle.
- (22) The 6V bias to BAT_IN is no longer needed and can be turned off at this point.
- (23) To shut down the converter:
 - (a) Turn off the BAT_IN 6V bias if present.
 - (b) Remove the BAT12 load.
 - (c) Remove the J_{77} jumper to terminate PWM_EN.
 - (d) Remove the J_{58} jumper to terminate EN.
 - (e) Turn off the V6, VIN, and V12 sources.



- (f) Turn off the BAT48 source.
- (g) Disconnect V6 and V12.
- (24) To reconfigure for buck, flyback, and GUI operation disconnect all of the jumpers and reconfigure with the following jumpers:
 - (a) J₁ (Phase Drop, J₄ (VIN_FLY), J₈₀ (2-3) (TRACK), TP₂₃ (BAT48 Bode), and TP₂₄ (BAT12 Bode).

6.3 Boost Operation of the ISL78224EVAL2Z without Flyback and with the GUI

- (1) Configure the phase drop, jumper J_1 to disable phase drop and leave it open to enable phase drop.
- (2) Connect a disabled \sim 12V source to the BAT12 terminal lugs.
- (3) Connect a disabled electronic load to the BAT48 terminal lugs.
- (4) A 6V BAT_IN (TP_{13}) bias is not needed in Boost mode.
- (5) All Bode plot functions are already disabled on the ISL78224EVAL2Z.
- (6) Address is already set to 0 on the ISL78224EVAL2Z.
- (7) Driver DRV_EN pins are already connected on the ISL78224EVAL2Z.
- (8) PWM_TRI is already connected to VCC on the ISL78224EVAL2Z.
- (9) Remove jumper J_4 to disconnect VIN_FLY from VIN.
- (10) Connect V6 (TP₁₉) to a disabled external 6V source.
- (11) Connect VIN (TP₁₄) and V12 (TP₁₈) to a disabled external 12V source.
- (12) Connect the GUI dongle to J_{77} (GPIO) and J_{74} (I²C). Note Pin 1 locations.
- (13) Enable the BAT12, V6, VIN, and V12 voltage sources.
- (14) Use the GUI to exercise the converter in Boost mode and EN.
- (15) Enable can be verified by observing the presence of voltages at PVCC, VCC, MCUVDD, and CLK_OUT.
- (16) Use the GUI to exercise PWM EN.
- (17) Observe 48V at the unloaded BAT48 output.
- (18) BAT48 can now be loaded. Maintain the FET surface temperatures below 100°C with fans.
- (19) The I²C connections at J_{74} is available using the GUI.
- (20) To shut down the converter:
 - (a) Disable the BAT48 load.
 - (b) Disable PWM_EN using the GUI.
 - (c) Disable EN using the GUI.
 - (d) Turn off the V6, VIN, and V12 sources.
 - (e) Turn off the BAT12 source.
 - (f) Disconnect V6 and V12.
- (21) To reconfigure for boost and flyback and GUI operation disconnect all of the jumpers and reconfigure with the following jumpers:
 - (a) J₁ (Phase Drop, J₄ (VIN_FLY), J₈₀ (2-3) (TRACK), TP₂₃ (BAT48 Bode), and TP₂₄ (BAT12 Bode).

6.4 Boost Operation of the ISL78224EVAL2Z without Flyback and without GPIO from the GUI

- (1) Configure the phase drop, jumper J_1 to disable phase drop and leave it open to enable phase drop.
- (2) Connect a disabled ~12V source to the BAT12 terminal lugs.
- (3) Connect a disabled electronic load to the BAT48 terminal lugs.
- (4) A 6V BAT_IN (TP_{13}) bias is not needed in Boost mode.
- (5) All Bode plot functions are already disabled on the ISL78224EVAL2Z.
- (6) Address is already set to 0 on the ISL78224EVAL2Z.
- (7) Driver DRV EN pins are already connected on the ISL78224EVAL2Z.
- (8) PWM_TRI is already connected to VCC on the ISL78224EVAL2Z.
- (9) Jumper J_{70} Pin 2 to J_{70} Pin 3 (VCC) to command boost operation.
- (10) Jumper J₈₈ Pin 2 to J₈₈ Pin 1 (VCC) to command continuous conduction mode (CCM) or J₈₈ Pin 2 to J₈₈ Pin 3 (GND) to command diode emulation mode (DE).
- (11) Jumper J₈₉ Pin 2 to J₈₉ Pin 1 (VCC) to command Latch off Fault protection (LAT) or J₈₉ Pin 2 to J₈₉ Pin 3 (GND) to command hiccup fault protection (HIC).
- (12) Remove jumper J_4 to disconnect VIN_FLY from VIN.
- (13) Connect V6 (TP₁₉) to a disabled external 6V source.
- (14) Connect VIN (TP_{14}) and V12 (TP_{18}) to a disabled external 12V source.
- (15) Enable the BAT12, V6, VIN, and V12 voltage sources.
- (16) Jumper J_{58} to command enable.
- (17) Enable can be verified by observing the presence of voltages at PVCC, VCC, MCUVDD, and CLK_OUT.
- (18) Jumper J₇₇ Pin 5 to J₇₇ Pin 6 to command PWM_EN, see Figure 52. Avoid bounce to this connection.



Figure 52.

- (19) Observe 48V at the unloaded BAT48 output.
- (20) BAT48 can now be loaded. Maintain the FET surface temperatures below 100°C with fans.
- (21) The I²C connections at J₇₄ remains available for use, with or without the GUI dongle.
- (22) To shut down the converter:
 - (a) Disable the BAT48 load.
 - (b) Remove the J_{77} jumper to terminate PWM_EN.
 - (c) Remove the J_{58} jumper to terminate EN.
 - (d) Turn off the V6, VIN, and V12 sources.
 - (e) Turn off the BAT12 source.
 - (f) Disconnect V6 and V12.
- (23) To reconfigure for boost and flyback and GUI operation disconnect all of the jumpers and reconfigure with the following jumpers:
 - (a) J₁ (Phase Drop, J₄ (VIN_FLY), J₈₀ (2-3) (TRACK), TP₂₃ (BAT48 Bode), and TP₂₄ (BAT12 Bode).



6.5 Buck Operation of the ISL78226EVAL1Z without Flyback and with the GUI

- (1) Configure the Phase Drop Switch SW_1 on for no phase drop, off for phase drop.
- (2) Connect a disabled ~48V source to the BAT48 terminal lugs.
- (3) Connect a disabled electronic load to the BAT12 terminal lugs.
- (4) Connect a disabled ~6V bias (~0.5A) to the BAT12_IN node (J_{50} banana socket).
- (5) Place a jumper on J_{14} to disable the BAT48 Bode plot function.
- (6) Place a jumper on J_{15} to disable the BAT12 Bode plot function.
- (7) Place a jumper on J_{26} to disable the MCUVDD Bode plot function.
- (8) Jumper J_{81} Pin 2 to J_{81} Pin 3 (GND) to command ADDR1 low.
- (9) Jumper J_{82} Pin 2 to J_{82} Pin 3 (GND) to command ADDR2 low.
- (10) Verify that JP_{310} , JP_{410} , JP_{510} , and JP_{610} are installed. Install them if they are not already present.
- (11) Jumper J₇₁ Pin 2 to J₇₁ Pin 1 (VCC) to command PWM_TRI operation.
- (12) Remove jumper J₄ to disconnect VIN_FLY from VIN.
- (13) Connect V6 (TP $_8$ banana) to a disabled external 6V source.
- (14) Connect VIN (J55 banana) and V12 (TP7 banana) to a disabled external 12V source.
- (15) Connect the GUI dongle to J_{77} (GPIO) and J_{74} (I²C). Note Pin 1 locations.
- (16) Enable the BAT48, BAT12_IN, V6, VIN, and V12 voltage sources.
- (17) Use the GUI to exercise the converter in buck mode and EN.
- (18) Enable can be verified by observing the presence of voltages at PVCC, VCC, MCUVDD, and CLK_OUT.
- (19) Use the GUI to exercise PWM_EN.
- (20) Observe 12V at the unloaded BAT12 output.
- (21) BAT12 can now be loaded. Maintain the FET surface temperatures below 100°C with fans.
- (22) The I²C connections at J_{74} is available using the GUI.
- (23) The 6V bias to BAT12_IN (J₅₀) is no longer needed and can be turned off at this point.
- (24) To shut down the converter:
 - (a) Turn off the BAT12_IN 6V bias if present.
 - (b) Disable the BAT12 load.
 - (c) Disable PWM_EN using the GUI.
 - (d) Disable EN using the GUI.
 - (e) Turn off the V6, VIN, and V12 sources.
 - (f) Turn off the BAT48 source.
 - (g) Disconnect V6 and V12.
- (25) To reconfigure for buck, flyback, and GUI operation disconnect all of the jumpers and reconfigure with the following jumpers:
 - (a) J_4 (VIN_FLY), J_{14} (BAT48 Bode), J_{15} (BAT12 Bode), J_{26} (MCUVDD Bode), J_{71} (1-2) (PWM_TRI), J_{80} (2-3) (TRACK), J_{81} (2-3) (ADDR1), J_{82} (2-3) (ADDR2), JP_{310} (DRV_EN), JP_{410} (DRV_EN), JP_{510} (DRV_EN), and JP_{610} (DRV_EN).
 - (b) Set phase drop switch SW_1 to on.



6.6 Buck Operation of the ISL78226EVAL1Z without Flyback and without GPIO from the GUI

- (1) Configure the Phase Drop Switch SW_1 on for no phase drop, off for phase drop.
- (2) Connect a disabled ~48V source to the BAT48 terminal lugs.
- (3) Connect a disabled electronic load to the BAT12 terminal lugs.
- (4) Connect a disabled ~6V bias (~0.5A) to the BAT12_IN node (J_{50} banana socket).
- (5) Place a jumper on J_{14} to disable the BAT48 Bode plot function.
- (6) Place a jumper on J_{15} to disable the BAT12 Bode plot function.
- (7) Place a jumper on J_{26} to disable the MCUVDD Bode plot function.
- (8) Place a jumper on J_{62} .
- (9) Jumper J_{81} Pin 2 to J_{81} Pin 3 (GND) to command ADDR1 low.
- (10) Jumper J_{82} Pin 2 to J_{82} Pin 3 (GND) to command ADDR2 low.
- (11) Verify that JP₃₁₀, JP₄₁₀, JP₅₁₀, and JP₆₁₀ are installed. Install them if they are not already present.
- (12) Jumper J₇₁ Pin 2 to J₇₁ Pin 1 (VCC) to command PWM_TRI operation.
- (13) Jumper J_{70} Pin 2 to J_{70} Pin 3 (GND) to command buck operation.
- (14) Jumper J₈₈ Pin 2 to J₈₈ Pin 1 (VCC) to command continuous conduction mode (CCM) or J₈₈ Pin 2 to J₈₈ Pin 3 (GND) to command diode emulation mode (DE).
- (15) Jumper J₈₉ Pin 2 to J₈₉ Pin 1 (VCC) to command Latch off Fault protection (LAT) or J₈₉ Pin 2 to J₈₉ Pin 3 (GND) to command hiccup fault protection (HIC).
- (16) Remove jumper J_4 to disconnect VIN_FLY from VIN.
- (17) Connect V6 (TP $_8$ banana) to a disabled external 6V source.
- (18) Connect VIN (J₅₅ banana) and V12 (TP₇ banana) to a disabled external 12V source.
- (19) Enable the BAT48, BAT12_IN, V6, VIN, and V12 voltage sources.
- (20) Jumper J_{58} to command enable.
- (21) Enable can be verified by observing the presence of voltages at PVCC, VCC, MCUVDD, and CLK_OUT.
- (22) Jumper J₇₇ Pin 5 to J₇₇ Pin 6 to command PWM_EN. See Figure 53. Avoid bounce to this connection.



Figure 53.

- (23) Observe 12V at the unloaded BAT12 output.
- (24) BAT12 can now be loaded. Maintain the FET surface temperatures below 100°C with fans.
- (25) The I²C connections at J₇₄ remains available for use, with or without the GUI dongle.
- (26) The 6V bias is no longer needed and can be turned off at this point.
- (27) To shut down the converter:
 - (a) Turn off the BAT12_IN 6V bias if present.
 - (b) Disable the BAT12 load.



- (c) Remove the J₇₇ jumper to terminate PWM_EN.
- (d) Remove the J_{58} jumper to terminate EN.
- (e) Turn off the V6, VIN, and V12 sources.
- (f) Turn off the BAT48 source.
- (g) Disconnect V6 and V12.
- (28) Do not reinstall the GUI dongle after these connections have been made as the dongle provides drive to some of the above mentioned signals and bus contention occurs.
- (29) To reconfigure for buck, flyback, and GUI operation disconnect all of the jumpers and reconfigure with the following jumpers:
 - (a) J_4 (VIN_FLY), J_{14} (BAT48 Bode), J_{15} (BAT12 Bode), J_{26} (MCUVDD Bode), $J_{71}(1-2)$ (PWM_TRI), J_{80} (2-3) (TRACK), $J_{81}(2-3)$ (ADDR1), $J_{82}(2-3)$ (ADDR2), JP_{310} (DRV_EN), JP_{410} (DRV_EN), JP_{510} (DRV_EN), and JP_{610} (DRV_EN).
 - (b) Set phase drop switch SW_1 to on.

6.7 Boost Operation of the ISL78226EVAL1Z without Flyback and with the GUI

- (1) Configure the Phase Drop Switch SW_1 on for no phase drop, off for phase drop.
- (2) Connect a disabled \sim 12V source to the BAT12 terminal lugs.
- (3) Connect a disabled electronic load to the BAT48 terminal lugs.
- (4) A 6V BAT12_IN (J₅₀ banana) bias is not needed in Boost mode.
- (5) Place a jumper on J_{14} to disable the BAT48 Bode plot function.
- (6) Place a jumper on J_{15} to disable the BAT12 Bode plot function.
- (7) Place a jumper on J_{26} to disable the MCUVDD Bode plot function.
- (8) Jumper J_{81} Pin 2 to J_{81} Pin 3 (GND) to command ADDR1 low.
- (9) Jumper J_{82} Pin 2 to J_{82} Pin 3 (GND) to command ADDR2 low.
- (10) Verify that JP₃₁₀, JP₄₁₀, JP₅₁₀, and JP₆₁₀ are installed. Install them if they are not already present.
- (11) Jumper J_{71} Pin 2 to J_{71} Pin 1 (VCC) to command PWM_TRI operation.
- (12) Remove jumper J_4 to disconnect VIN_FLY from VIN.
- (13) Connect V6 (TP₈ banana) to a disabled external 6V source.
- (14) Connect VIN (J₅₅ banana) and V12 (TP7 banana) to a disabled external 12V source.
- (15) Connect the GUI dongle to J_{77} (GPIO) and J_{74} (I²C). Note Pin 1 locations.
- (16) Enable the BAT12, V6, VIN, and V12 voltage sources.
- (17) Use the GUI to exercise the converter in Boost mode and EN.
- (18) Enable can be verified by observing the presence of voltages at PVCC, VCC, MCUVDD, and CLK_OUT.
- (19) Use the GUI to exercise PWM_EN.
- (20) Observe 48V at the unloaded BAT48 output.
- (21) BAT48 can now be loaded. Maintain the FET surface temperatures below 100°C with fans.
- (22) The I²C connections at J_{74} is available using the GUI.
- (23) To shut down the converter:
 - (a) Disable the BAT48 load.
 - (b) Disable PWM_EN using the GUI.
 - (c) Disable EN using the GUI.
 - (d) Turn off the V6, VIN, and V12 sources.
 - (e) Turn off the BAT12 source.
 - (f) Disconnect V6 and V12.



- (24) To reconfigure for boost and flyback and GUI operation disconnect all of the jumpers and reconfigure with the following jumpers:
 - (a) J_4 (VIN_FLY), J_{14} (BAT48 Bode), J_{15} (BAT12 Bode), J_{26} (MCUVDD Bode), J_{71} (1-2) (PWM_TRI), J_{80} (2-3) (TRACK), J_{81} (2-3) (ADDR1), J_{82} (2-3) (ADDR2), JP_{310} (DRV_EN), JP_{410} (DRV_EN), JP_{510} (DRV_EN), and JP_{610} (DRV_EN).
 - (b) Set phase drop switch SW_1 to on.

6.8 Boost Operation of the ISL78226EVAL1Z without Flyback and without GPIO from the GUI

- (1) Configure the Phase Drop Switch SW_1 on for no phase drop, off for phase drop.
- (2) Connect a disabled \sim 12V source to the BAT12 terminal lugs.
- (3) Connect a disabled electronic load to the BAT48 terminal lugs.
- (4) A 6V BAT12_IN (J₅₀ banana) bias is not needed in Boost mode.
- (5) Place a jumper on J_{14} to disable the BAT48 Bode plot function.
- (6) Place a jumper on J_{15} to disable the BAT12 Bode plot function.
- (7) Place a jumper on J_{26} to disable the MCUVDD Bode plot function.
- (8) Place a jumper on J_{62} .
- (9) Jumper J_{81} Pin 2 to J_{81} Pin 3 (GND) to command ADDR1 low.
- (10) Jumper J_{82} Pin 2 to J_{82} Pin 3 (GND) to command ADDR2 low.
- (11) Verify that JP_{310} , JP_{410} , JP_{510} , and JP_{610} are installed. Install them if they are not already present.
- (12) Jumper J₇₁ Pin 2 to J₇₁ Pin 1 (VCC) to command PWM_TRI operation.
- (13) Jumper J_{70} Pin 2 to J_{70} Pin 1 (VCC) to command boost operation.
- (14) Jumper J₈₈ Pin 2 to J₈₈ Pin 1 (VCC) to command continuous conduction mode (CCM) or J₈₈ Pin 2 to J₈₈ Pin 3 (GND) to command diode emulation mode (DE).
- (15) Jumper J₈₉ Pin 2 to J₈₉ Pin 1 (VCC) to command Latch off Fault protection (LAT) or J₈₉ Pin 2 to J₈₉ Pin 3 (GND) to command hiccup fault protection (HIC).
- (16) Remove jumper J₄ to disconnect VIN_FLY from VIN.
- (17) Connect V6 (TP $_8$ banana) to a disabled external 6V source.
- (18) Connect VIN (J₅₅ banana) and V12 (TP₇ banana) to a disabled external 12V source.
- (19) Enable the BAT12, V6, VIN, and V12 voltage sources.
- (20) Jumper J_{58} to command enable.
- (21) Enable can be verified by observing the presence of voltages at PVCC, VCC, MCUVDD, and CLK_OUT.
- (22) Jumper J₇₇ Pin 5 to J₇₇ Pin 6 to command PWM_EN, see Figure 54. Avoid bounce to this connection.



Figure 54.

(23) Observe 48V at the unloaded BAT48 output.



- (24) BAT48 can now be loaded. Maintain the FET surface temperatures below 100°C with fans.
- (25) The I²C connections at J_{74} remains available for use, with or without the GUI dongle.
- (26) To shut down the converter:
 - (a) Disable the BAT48 load.
 - (b) Remove the J_{77} jumper to terminate PWM_EN.
 - (c) Remove the J_{58} jumper to terminate EN.
 - (d) Turn off the V6, VIN, and V12 sources.
 - (e) Turn off the BAT12 source.
 - (f) Disconnect V6 and V12.
- (27) Do not reinstall the GUI dongle after these connections have been made as the dongle provides drive to some of the above mentioned signals and bus contention occurs.
- (28) To reconfigure for boost and flyback and GUI operation disconnect all of the jumpers and reconfigure with the following jumpers:
 - (a) J_4 (VIN_FLY), J_{14} (BAT48 Bode), J_{15} (BAT12 Bode), J_{26} (MCUVDD Bode), $J_{71}(1-2)$ (PWM_TRI), J_{80} (2-3) (TRACK), J_{81} (2-3) (ADDR1), $J_{82}(2-3)$ (ADDR2), JP_{310} (DRV_EN), JP_{410} (DRV_EN), JP_{510} (DRV_EN), and JP_{610} (DRV_EN).
 - (b) Set phase drop switch SW_1 to on.



7. PCB Layout Guidelines

The AC performance of this circuit depends greatly on the care taken in designing the Printed Circuit Board (PCB). The following are recommendations to achieve optimum high performance from the PCB.

ISL78226EVAL1Z evaluation board: six layers, 0.125 inch thick FR4 material, +125°C maximum temperature, 2oz copper top/bottom, 4oz copper layers 2 through 5.

ISL78224EVAL2Z evaluation board: eight layers, 0.125 inch thick FR4 material, +125°C maximum temperature, 2oz copper top/bottom, 4oz copper layers 2 through 7.

- The use of low inductance components, such as chip resistors and chip capacitors, is strongly recommended.
- Minimize signal trace lengths, especially for the VDD, charge pump decoupling, CS1, CS2, and VC0 to VC8 inputs. Trace inductance and capacitance can easily affect circuit performance. Avoid placing vias in the signal lines because they add inductance at high frequency.
- Match channel-to-channel analog I/O trace lengths and layout symmetry, especially for the CS1 and CS2 lines, because their inputs are normally very low voltage.
- Maximize use of AC decoupled PCB layers. Route all signal I/O lines over continuous ground planes (for example, no split planes or PCB gaps under these lines). Avoid vias in the signal I/O lines.
- When testing, use good quality connectors and cables, matching cable types, and keep cable lengths to a minimum.
- Caution: Avoid flexing the board because this can cause stress on the capacitors, resulting in either a short or open capacitor.

7.1 Maximum Operating Power for Evaluation Boards

7.1.1 ISL78226

Conditions: No heatsink, +24°C ambient, phase balance enabled, Forced CCM mode, no phase drop.

- 2.4kW without airflow
- 3kW with airflow (airflow \sim 5M/s)

7.1.2 ISL78224

Conditions: No heatsink, +24°C ambient, phase balance enabled, Forced CCM mode, no phase drop.

- 1.2kW without airflow
- 2kW with airflow (airflow \sim 3.3M/s)



7.2 Evaluation Boards



Figure 55. ISL78226EVAL1Z 12V to 48V Bidirectional Customer Evaluation Board



Figure 56. ISL78224EVAL2Z 12V to 48V Bidirectional Customer Evaluation Board



7.3 ISL78226EVAL1Z Circuit Schematics

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Figure 57. ISL78226EVAL1Z Schematic Page 1 of 10

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Figure 61. ISL78226EVAL1Z Schematic Page 5 of 10





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7. PCB Layout Guidelines

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Figure 64. ISL78226EVAL1Z Schematic Page 8 of 10

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Figure 65. ISL78226EVAL1Z Schematic Page 9 of 10





Figure 66. ISL78226EVAL1Z Schematic Page 10 of 10

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7.4 ISL78224EVAL2Z Circuit Schematics



Figure 67. ISL78224EVAL2Z Schematic Page 1 of 8

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Figure 68. ISL78224EVAL2Z Schematic Page 2 of 8



Figure 69. ISL78224EVAL2Z Schematic Page 3 of 8

ISL78226EVKIT1Z, ISL78224EVKIT2Z



Figure 70. ISL78224EVAL2Z Schematic Page 4 of 8

ISL78226EVKIT1Z, ISL78224EVKIT2Z





Figure 71. ISL78224EVAL2Z Schematic Page 5 of 8

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U2A 3

U5F 2

• U5E 4

DE/CCM

HIC/LAT

IN

<i>ENESAS











7. PCB Layout Guidelines

ISL78226EVKIT1Z, ISL78224EVKIT2Z

7.5 ISLUSBADAPT-EVZ Schematic



Figure 75. Schematic ISLUSBADAPT-EVZ Page 1 of 1



7.6 ISL78226EVAL1Z Bill of Materials

| | | | | Tol. | | Package | | |
|----|-----|--|---------|------|---------|---------|----------------|--------------------------|
| | Qty | Reference Designator | Value | (%) | Voltage | Туре | Manufacturer | Manufacturer Part Number |
| 1 | | BB1, BB3 | DNP | | | | E-Fab, Inc. | EFI-41111 |
| 2 | _ | BB2, BB4 | DNP | | | | E-Fab, Inc. | EFI-41110 |
| 3 | 10 | C1, C2, C54, C56, C132, C232, C332, C432, C532, C632 | 0.1µF | 10 | 50V | 0603 | Generic | Various |
| 4 | 6 | C102, C202, C302, C402, C502, C602 | 220µF | 20 | 100V | Radial | Nippon | EGPD101ELL221MK25H |
| 5 | 0 | C101, C201, C301, C401, C501, C601 | DNP | | | | | |
| 6 | 1 | C11 | 1µF | 10 | 100V | 1206 | Generic | Various |
| 7 | 37 | C68, C110-C115, C210-C215, C310-C315, C410-C415, C510-C515, C610- C615 | 3.3µF | 10 | 100V | 2220 | ТDК | CGA9N2X7R2A335K230KA |
| 8 | 38 | C66, C71, C120-C125, C220-C225, C320-C325, C420-C425, C520-C525, C620-C625 | 0.1µF | 10 | 100V | 805 | ТDК | CGA4J2X7R2A104K125AA |
| 9 | 6 | C134, C234, C334, C434, C534, C634 | 1000pF | 10 | 100V | 0603 | Generic | Various |
| 10 | 6 | C141, C241, C341, C441, C541, C641 | 330µF | 20 | 63V | Radial | NIC Components | NRE-WY331M63V12.5X25 |
| 11 | 0 | C140, C240, C340, C440, C540, C640 | DNP | | | | | |
| 12 | 72 | C144-C155, C244-C255, C344-C355, C444-C455, C544-C555, C644-C655 | 2.2µF | 10 | 50V | 0805 | TDK | CGA4J3X7R1H225K125AB |
| 13 | 36 | C160-C165, C260-C265, C360-C365, C460-C465, C560-C565, C660-C665 | 0.1µF | 10 | 50V | 0805 | TDK | CGA4J2X7R1H104K125AA |
| 14 | 11 | C1, C2, C45, C54, C56, C132, C232, C332, C432, C532, C632 | 0.1µF | 10 | 50V | 0603 | Generic | Various |
| 15 | 2 | C3, C57 | 10µF | 10 | 25V | 0805 | Generic | Various |
| 16 | 2 | C4, C7 | 100µF | 20 | 50V | Radial | Nichicon | UBT1H101MPD1TD |
| 17 | 0 | C43, C44, C46, C48, C58, C69, C133, C135, C136, C233, C235, C236, C333, C335, C336, C433, C435, C436, C533, C535, C536, C633, C635, C636 | DNP | | | 0603 | | Various |
| 18 | 1 | C51 | 0.33µF | 10 | 50V | 0805 | Generic | Various |
| 19 | 7 | C65, C130, C230, C330, C430, C530, C630 | 0.22µF | 10 | 50V | 0603 | Generic | Various |
| 20 | 1 | C52 | 0.068µF | 10 | 50V | 0603 | TDK | C1608X7R1H683K |
| 21 | 3 | C55, C61, C78 | 1000pF | 10 | 50V | 0603 | Generic | Various |
| 22 | 2 | C47, C59 | 0.01µF | 10 | 50V | 0603 | Generic | Various |
| 23 | 1 | C63 | 330pF | 10 | 50V | 0603 | Generic | Various |
| 24 | 1 | C64 | 6800pF | 10 | 50V | 0603 | Generic | Various |
| 25 | 38 | C66, C71, C120-C125, C220-C225, C320-C325, C420-C425, C520-C525, C620-C625 | 0.1µF | 10 | 100V | 0805 | TDK | CGA4J2X7R2A104K125AA |
| 26 | 1 | C67 | 10µF | 10 | 100V | 2220 | TDK | CGA9N3X7S2A106K230KB |

| | | | | Tol. | | Package | | |
|------|-----|---|--------|-------|----------|-------------|----------------|--------------------------|
| ltem | Qty | Reference Designator | Value | - | Voltage | Туре | Manufacturer | Manufacturer Part Number |
| 27 | 4 | C73-C76 | 0.1µF | 10 | 25V | 0603 | Kemet | C0603X104K3RACTU |
| 28 | 1 | C77 | 2200pF | 10 | 50V | 0603 | Generic | Various |
| 29 | 2 | C79, C80 | 10µF | 10 | 25V | 1206 | Taiyo Yuden | TMK316B7106KL-TD |
| 30 | 8 | C8, C53, C131, C231, C331, C431, C531, C631 | 1µF | 10 | 25V | 0603 | Murata | GRM188R71E105KA12 |
| 31 | 2 | C9, C10 | 100µF | 20 | 100V | Radial | NIC Components | NRE-WY101M100V12.5X20 |
| 32 | 5 | D1, D2, D7, D11, D12 | 2A | | 70V | SMD2 | Diodes | B270-13F |
| 33 | | D101-D104, D201-D204, D301-D304, D401-D404, D501-D504, D601-D604 | 2A | | 30V | SOD123 | Diodes | MBR230S1F |
| 34 | 6 | D105, D205, D305, D405, D505, D605 | 2A | | 80V | SMD2 | Diodes | B280-13F |
| 35 | 3 | D13-D15 | GREEN | LED | | SMD | Dialight | 597-3311-407NF |
| 36 | 1 | D3 | 225mW | | 5.6V | SM3 | On Semi | MMBZ5232B |
| 37 | 1 | D4 | 500mW | | 62V | SM2 | On Semi | MMSZ5265B |
| 38 | 1 | D5 | 1A | | 100V | SMD2 | Diodes | B1100LB-13F |
| 39 | 1 | D6 | 3A | | 150V | SMD2 | Diodes Inc | SBR3150SB |
| 40 | 3 | D8-D10 | RED | LED | | SMD | Dialight | 597-3111-407 |
| 41 | | J1, J4, J14, J15, J17, J18, J20-J27, J29-J40, J42-J48, J58-J63, J65-J68, J73, J76, J79, J83, JP101-JP108, JP201-JP208, JP301-JP310, JP401-JP410, JP501-JP510, JP601-JP610 | | | | THOLE | Generic | JUMPER2_100 |
| 42 | 24 | J101-J104, J201-J204, J301-J304, J401-J404, J501-J504, J601-J604 | | | | B2C | IHI Connectors | B2C-PCB-45-HEX |
| 43 | 8 | J12, J70, J71, J80-J82, J88, J89 | | | | THOLE | Generic | JUMPER-3-100 |
| 44 | 1 | J2 | | | | 2COLSX3ROWS | Samtec | TSW-103-08-T-D-RA |
| 45 | 10 | J49, J50, J52-J56, J78, TP7, TP8 | | | | CONN | Keystone | 575-4 |
| 46 | 1 | J74 | | | | IN-LINE | Generic | CONN-1X4 |
| 47 | 1 | J75 | | | | THOLE | Generic | JUMPER-3-100 |
| 48 | 1 | J77 | | | | HDR | Samtec | HTSW-110-07-G-D |
| 49 | 6 | L101, L201, L301, L401, L501, L601 | 6.8µH | UA79 | 19-AE | Custom | Coilcraft | UA7919-AE |
| 50 | 0 | L102, L202, L302, L402, L502, L602 | DNP | IHTH? | 1500TZEF | R6R8M5A | Vishay | IHTH1500TZER6R8M5A |
| 51 | 2 | Q1, Q2 | 5.4A | P-CH | -12V | 2-2U1A | Toshiba | SSM3J132TU |
| 52 | 24 | Q101-Q104, Q201-Q204, Q301-Q304, Q401-Q404, Q501-Q504, Q601-Q604 | 55A | N-CH | 100V | DPAK | Toshiba | TK55S10N1 |
| 53 | 2 | Q3, Q4 | 50A | N-CH | 100V | TO252 | VISHAY | SQD50N10-8M9L |
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|-------------|----------------|--|--|
| | | | |

| | | | r | 1 | r | | | |
|------|-----|---|-------|-------------|---------|-----------------|--------------|--------------------------|
| ltem | Qty | Reference Designator | Value | Tol. (%) | Voltage | Package Type | Manufacturer | Manufacturer Part Number |
| 54 | 6 | Q9-Q14 | 4.2A | N-CH | 20V | 2-2U1A | Toshiba | SSM3K123TU |
| 55 | 47 | R1, R5, R6, R11, R44, R105, R108, R109, R110, R114, R117, R127, R205, R208, R209, R210, R214, R217, R227, R305, R308, R309, R310, R314, R317, R327, R405, R408, R409, R410, R414, R417, R427, R505, R508, R509, R510, R514, R517, R527, R605, R608, R609, R610, R614, R617, R627 | 0 | | | 0603 | Generic | Various |
| 56 | 24 | R101, R103, R130, R132, R201, R203, R230, R232, R301, R303, R330, R332, R401, R403, R430, R432, R501, R503, R530, R532, R601, R603, R630, R632 | 4.7 | 10 | | 0805 | Generic | Various |
| 57 | 6 | R107, R207, R307, R407, R507, R607 | 100k | 1 | | 0603 | Generic | Various |
| 58 | 0 | R111, R112, R131, R133, R211, R212, R231, R233, R311, R312, R331, R333, R411, R412, R431, R433, R511, R512, R531, R533, R611, R612, R631, R633 | DNP | | | 0805 | Generic | Various |
| 59 | 12 | R115, R116, R215, R216, R315, R316, R415, R416, R515, R516, R615, R616 | 0.001 | 1 | | 2512 | Vishay | WSLP25121L000FEA |
| 60 | 24 | R120-R123, R220-R223, R320-R323, R420-R423, R520-R523, R620-R623 | 499 | 1 | | 0603 | Generic | S0603CPX4990F10 |
| 61 | 0 | R128, R129, R228, R229, R328, R329, R428, R429, R528, R529, R628, R629 | DNP | | | 0603 | Generic | Various |
| 62 | 1 | R18 | 30.1k | 1 | | 0603 | Generic | Various |
| 63 | 1 | R19 | 51.1k | 1 | | 0603 | Generic | Various |
| 64 | 1 | R20 | 26.7k | 1 | | 0603 | Generic | Various |
| 65 | 1 | R21 | 38.3k | 1 | | 0603 | Generic | Various |
| 66 | 32 | R2, R3, R4, R22, R48, R61, R62, R66, R72, R73, R74, R75, R76, R88, R102, R104, R106, R202, R204, R206, R302, R304, R306, R402, R404, R406, R502, R504, R506, R602, R604, R606 | 10.0k | 1 | | 0603 | Generic | Various |
| 67 | 4 | R23, R24, R45, R59 | 49.9 | 1 | | 0603 | Generic | Various |
| 68 | 0 | R25, R27, R113, R118, R119, R124-R126, R128, R129, R213, R218, R219, R224-R226, R228, R229, R313, R318, R319, R324-R326, R328, R329, R413, R418, R419, R424-R426, R428, R429, R513, R518, R519, R524-R526, R528, R529, R613, R618, R619, R624-R626, R628, R629 | DNP | | | 0603 | Generic | Various |
| 69 | 1 | R26 | 2.8k | 1 | | 0603 | Generic | Various |
| 70 | 1 | R28 | 4.22K | 1 | | 0603 | Generic | Various |
| 71 | 1 | R29 | 20.0k | 1 | | 0603 | Generic | Various |
| 72 | 2 | R30, R33 | 68.1k | 1 | | 0603 | Generic | Various |
| 73 | 2 | R31, R32 | 33.2k | 1 | | 0603 | Generic | Various |
| 74 | 2 | R34, R38 | 7.5k | 1 | | 0603 | Generic | Various |
| 75 | 1 | R36 | 33k | 1 | | 0603 | Generic | CRCW060333K0FKEA |
| 76 | 2 | R37, R50 | 51k | 1 | | 0603 | Generic | CRCW060351K0FKEA |

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| | 00 |

| Item | Qty | Reference Designator | Value | Tol. (%) | Voltage | Package Type | Manufacturer | Manufacturer Part Number |
|------|-----|------------------------------------|--------------|-------------|---------|-----------------|--------------|--------------------------|
| 77 | 1 | R39 | 27.4 | 1 | | 0603 | Generic | Various |
| 78 | 1 | R40 | 10.2k | 0.1 | | 0603 | Generic | Various |
| 79 | 1 | R43 | 54.9k | 1 | | 0603 | Generic | Various |
| 80 | 1 | R46 | 10.2k | 1 | | 0603 | Generic | Various |
| 81 | 1 | R47 | 21.5k | 1 | | 0603 | Generic | Various |
| 82 | 3 | R42, R49, R64 | 10 | 1 | | 0603 | Generic | S0603CPZ10R0F10 |
| 83 | 9 | R51, R52, R55, R56, R60, R68-R71 | 1.00k | 1 | | 0603 | Generic | Various |
| 84 | 1 | R53 | 3.24k | 1 | | 0603 | Generic | Various |
| 85 | 1 | R57 | 46.4k | 1 | | 0603 | Generic | Various |
| 86 | 1 | R58 | 3.01k | 1 | | 0603 | Generic | Various |
| 87 | 1 | R63 | 1Ω | 1 | | 0603 | Generic | Various |
| 88 | 1 | R65 | 30.1k | 1 | | 1206 | Generic | Various |
| 89 | 1 | R67 | 0.015 | 1 | | 1206 | Vishay | WSLP12065L000FEA |
| 90 | 1 | SW1 | | | | SPST | C&K | GT12MSCBETR |
| 91 | 1 | Τ1 | 4.9µH | 10 | | HPH4-0060L | Coilcraft | HPH4-0060LB |
| 92 | 1 | U1 | ISL78226 | 6ANZ | | 64TQFP | Renesas | ISL78226ANZ |
| 93 | 6 | U101, U201, U301, U401, U501, U601 | ISL78420AVEZ | | | 14HTSSOP | Renesas | ISL78420AVEZ |
| 94 | 1 | U2 | MM74HC | COOMT | CX-T | 14TSSOP | Fairchild | MM74HC00MTC |
| 95 | 2 | U3, U4 | MM74HC | CO2MT | CX-T | 14TSSOP | Fairchild | MM74HC02MCT |
| 96 | 1 | U5 | MM74HC | CO4MT | CX-T | 14TSSOP | Fairchild | MM74HC04MCT |

7.7 ISL78224EVAL2Z Bill of Materials

| Item | Qty | Reference Designator | Value | Tol. (%) | Voltage (V) | Package Type | Manufacturer | Manufacturer Part Number |
|------|-----|---|---------|-------------|----------------|-----------------|------------------|--------------------------|
| 1 | 6 | C2, C54, C56, C73, C74, C76 | 0.1µF | 10 | 25 | 0603 | Kemet | C0603X104K3RACTU-T |
| 2 | 24 | C160-C165, C260-C265, C360-C365, C460-C465 | 0.1µF | 10 | 50 | 0805 | TDK | CGA4J2X7R1H104K125AA-T |
| 3 | 33 | C71, C120-C127, C220-C227, C320-C327, C420-C427 | 0.1µF | 10 | 100 | 0805 | TDK | CGA4J2X7R2A104K125AA-T |
| 4 | 48 | C144-C155, C244-C255, C344-C355, C444-C455 | 2.2µF | 10 | 50 | 0805 | TDK | CGA4J3X7R1H225K125AE-T |
| 5 | 29 | C68, C110-C116, C210-C216, C310-C316, C410-C416 | 3.3µF | 10 | 100 | 2220 | TDK | CGA9N2X7R2A335K230KA-T |
| 6 | 1 | C67 | 10µF | 10 | 100 | 2220 | TDK | CGA9N3X7S2A106K230KB-T |
| 7 | 2 | C8, C53 | 1µF | 10 | 25 | 0603 | Murata | GRM188R71E105KA12D-T |
| 8 | 4 | C131, C231, C331, C431 | 4.7µF | 10 | 25 | 0805 | TDK | CGA4J1X7R1E475K125AC |
| 9 | 4 | C105, C205, C305, C405 | 100pF | 10 | 50 | 0603 | Generic | Various |
| 10 | 4 | C134, C234, C334, C434 | 1000pF | 10 | 100 | 0603 | Generic | Various |
| 11 | 3 | C55, C61, C78 | 1000pF | 10 | 50 | 0603 | Generic | Various |
| 12 | 2 | C47, C59 | 0.01µF | 10 | 50 | 0603 | Generic | Various |
| 13 | 6 | C1, C45, C132, C232, C332, C432 | 0.1µF | 10 | 50 | 0603 | Generic | Various |
| 14 | 1 | C77 | 2200pF | 10 | 50 | 0603 | Generic | Various |
| 15 | 5 | C65, C130, C230, C330, C430 | 0.22µF | 10 | 50 | 0603 | Generic | Various |
| 16 | 1 | C63 | 330pF | 10 | 50 | 0603 | Generic | Various |
| 17 | 1 | C64 | 6800pF | 10 | 50 | 0603 | Generic | Various |
| 18 | 1 | C52 | 0.068µF | 10 | 50 | 0603 | Generic | Various |
| 19 | 0 | C43, C44, C46, C48, C50, C58 | | | | | Do Not Populate | Do Not Populate |
| 20 | 2 | C3, C57 | 10µF | 10 | 25 | 0805 | Generic | Various |
| 21 | 1 | C51 | 0.33µF | 10 | 50 | 0805 | Generic | Various |
| 22 | 1 | C11 | 1µF | 10 | 100 | 1206 | Generic | Various |
| 23 | 2 | C79, C80 | 10µF | 10 | 25 | 1206 | Taiyo Yuden | TMK316B7106KL-TD |
| 24 | 4 | C102, C202, C302, C402 | 220µF | 20 | 100 | RADIAL | Nippon Chemi-Con | EGPD101ELL221MK25H |
| 25 | 1 | T1 | 4.9µH | 10 | | CUSTOM | Coilcraft | HPH4-0060LB |
| 26 | 2 | C9, C10 *(ALT:UBT2A101MHD1TO) | 100µF | 20 | 100 | RADIAL | NIC Comp Corp. | NRE-WY101M100V12.5X20F |
| 27 | 4 | C141, C241, C341, C441 | 330µF | 20 | 63 | RADIAL | NIC Comp Corp. | NRE-WY331M63V12.5X25F |
| 28 | 2 | C4, C7 | 100µF | 20 | 50V | RADIAL | Nichicon | UBT1H101MPD |
| 29 | 4 | L101, L201, L301, L401 | 6.8µH | | | CUSTOM | Cyntec Co.,Itd. | VCHH2324AF-6R8MS6-87 |
| 30 | 11 | TP6-TP11, TP13, TP14, TP16, TP18, TP19 | | | | | Keystone | 5000 |

7. PCB Layout Guidelines

| | | | | Tol. | Voltage | Package | | |
|------|-----|--|--------|-------|---------|---------|------------------|--------------------------|
| Item | Qty | Reference Designator | Value | (%) | (V) | Туре | Manufacturer | Manufacturer Part Number |
| 31 | 4 | TP12,TP15,TP17,TP20 | | | | | Keystone | 5001 |
| 32 | 1 | J77 | | | | | Samtec | HTSW-110-07-G-D |
| 33 | 2 | J1, J4 | | | | | Sullins | SPC02SYAN |
| 34 | | J1, J4, J58-J60, J65, JP103, JP203, JP303, JP403, TP1-TP5, TP21, TP23-TP31, TP50, TP51, TP80, TP101-TP106, TP201-TP204, TP301-TP304, TP401-TP404 | | | | | Samtec | TSW-150-08-F-S-1X2 |
| 35 | 4 | J70, J80, J88, J89 | | | | | Samtec | TSW-150-08-F-S-1X3 |
| 36 | 1 | J74 | | | | | Samtec | TSW-150-08-F-S-1X4 |
| 37 | 1 | D5 | 1A | | 100 | 2P | Diodes Inc. | B1100LB-13-F-T |
| 38 | 4 | D1, D2, D7, D12 | 2A | | 70 | 2P | Diodes Inc. | B270-13-F-T |
| 39 | 0 | D101-D104, D201-D204, D301-D304, D401-D404 | | | | | Do Not Populate | |
| 40 | 1 | D3 | 225mW | | 5.6 | SOT-23 | On Semiconductor | MMBZ5232BLT1G-T |
| 41 | 1 | D6 | 3A | | 150 | 2P | Diodes Inc. | SBR3150SB-13-T |
| 42 | 3 | D8, D9, D10 | 30mA | RED | | 1206 | Dialight | 597-3111-407F-T |
| 43 | 3 | D13, D14, D15 | 75mW | GREEN | | 1206 | Dialight | 597-3311-407NF-T |
| 44 | 1 | U1 | | | | TQFP-EP | Intersil | ISL78224ANZ |
| 45 | 4 | U101, U201, U301, U401 | | | 100 | HTSSOP | Intersil | ISL424AVEZ |
| 46 | 1 | U2 | | | | TSSOP | Fairchild | MM74HC00MTCX-T |
| 47 | 1 | U4 | | | | TSSOP | Fairchild | MM74HC02MTCX-T |
| 48 | 1 | U5 | | | | TSSOP | Fairchild | MM74HC04MTCX-T |
| 49 | 1 | Q4 | | | | | Vishay/Siliconix | SQD50N10-8M9L-GE3-T |
| 50 | 1 | Q2 | | | | | Toshiba | SSM3J132TU-T |
| 51 | 3 | Q9, Q12, Q14 | 4.2A | | 20V | | Toshiba | SSM3K123TU,LF-T |
| 52 | 16 | Q101-Q104, Q201-Q204, Q301-Q304, Q401-Q404 | 55A | | 100 | | Toshiba | TK55S10N1, LQ-T |
| 53 | 1 | R67 | 0.015Ω | 1 | | 1206 | Panasonic | ERJ-8CWFR015V-T |
| 54 | 0 | R25, R27, R35, R41, R52 | | 0.1 | | 0603 | Do Not Populate | DO NOT POPULATE |
| 55 | 3 | R42, R49, R64 | 10Ω | 1 | | 0603 | Generic | VARIOUS |
| 56 | 13 | R1, R7, R8, R9, R39, R105, R109, R205, R209, R305, R309, R405, R409 | 0Ω | | | 0603 | Generic | VARIOUS |
| 57 | 7 | R5, R6, R60, R68, R69, R70, R71 | 1k | 1 | | 0603 | Generic | Various |
| 56 | | R2, R3, R4, R44, R48, R61, R62, R66, R72-R76, R88, R102, R104, R202, R204, R302, R304, R402, R404 | 10k | 1 | | 0603 | Generic | Various |
| 59 | 4 | R107, R207, R307, R407 | 100k | 1 | | 0603 | Generic | Various |

| ltem | Qty | Reference Designator | Value | Tol. (%) | Voltage (V) | Package Type | Manufacturer | Manufacturer Part Number |
|------|-----|--|--------|-------------|----------------|-----------------|------------------------------|--------------------------|
| 60 | 1 | R46 | 10.2k | 1 | | 0603 | Generic | Various |
| 61 | 2 | R34,R38 | 7.5k | 1 | | 0603 | Generic | Various |
| 62 | 1 | R29 | 20.0k | 1 | | 0603 | Generic | Various |
| 63 | 1 | R40 | 15k | 0.1 | | 0603 | Generic | Various |
| 64 | 1 | R47 | 21.5k | 1 | | 0603 | Generic | Various |
| 65 | 1 | R20 | 0Ω | 1 | | 0805 | Generic | Various |
| 66 | 1 | R26 | 2.80k | 0.1 | | 0603 | Generic | Various |
| 67 | 1 | R58 | 3.01k | 1 | | 0603 | Generic | Various |
| 68 | 1 | R18 | 30.1k | 0.1 | | 0603 | Generic | Various |
| 69 | 1 | R53 | 3.24k | 1 | | 0603 | Generic | Various |
| 70 | 1 | R36 | 33k | 1 | | 0603 | Generic | Various |
| 71 | 1 | R31 | 33.2k | 1 | | 0603 | Generic | Various |
| 72 | 1 | R21 | 64.9k | 0.1 | | 0603 | Generic | Various |
| 73 | 1 | R57 | 46.4k | 1 | | 0603 | Generic | Various |
| 74 | 1 | R43 | 42.2k | 1 | | 0603 | Generic | Various |
| 75 | 16 | R120-R123, R220-R223, R320-R323, R420-R423 | 499Ω | 1 | | 0603 | Generic | Various |
| 76 | 2 | R37, R50 | 51k | 1 | | 0603 | Generic | Various |
| 77 | 1 | R19 | 51.1k | 0.1 | | 0603 | Generic | Various |
| 78 | 1 | R28 | 4.22kΩ | 1 | | 0603 | Generic | Various |
| 79 | 1 | R33 | 68.1k | 1 | | 0603 | Generic | Various |
| 80 | 32 | R101, R103, R111, R113, R130, R132, R140, R142, R201, R203, R211, R213, R230, R232, R240, R242, R301, R303, R311, R313, R330, R332, R340, R342, R401, R403, R430, R411, R413, R432, R440, R442 | 4.7Ω | 1 | | 0805 | Generic | Various |
| 81 | 1 | R65 | 30.1k | 1 | | 1206 | Generic | Various |
| 82 | 8 | R115, R116, R215, R216, R315, R316, R415, R416 | 1.0mΩ | 1 | | 2512 | Vishay/Dale | WSLP2512L000FEA |
| 83 | 4 | J101-J104 | | | | | International Hydraulics Inc | B2C-PCB-HEX |
| 84 | 6 | Perimeter of PCB | | | | | 4-40 SCREW | |
| 85 | 6 | Perimeter of PCB | | | | | 4-40 STANDOFF | |
| 86 | 1 | Place assy in bag | | | | | Renesas Common Stock | 8X12-STATIC-BAG |

7.8 ISL78226EVAL1Z Board Layout (Six Layers)



Figure 76. Assembly Top





Figure 77. Silkscreen Top





Figure 78. Top Layer





Figure 79. PCB – Inner Layer 2 (Viewed from Top)





Figure 80. PCB – Inner Layer 3 (Viewed from Top)





Figure 81. PCB – Inner Layer 4 (Viewed from Top)





Figure 82. PCB – Inner Layer 5 (Viewed from Top)





Figure 83. PCB – Bottom Layer (Viewed from Top)





Figure 84. Silkscreen Bottom





Figure 85. Bottom Assembly





7.9 ISL78224EVAL2Z Board Layout (Eight Layers)

Figure 86. Assembly Top



ISL78226EVKIT1Z, ISL78224EVKIT2Z



Figure 87. Silkscreen Top





Figure 88. PCB – Top Layer





Figure 89. PCB – Inner Layer 2 (Viewed from Top)





Figure 90. PCB – Inner Layer 3 (Viewed from Top)





Figure 91. PCB – Inner Layer 4 (Viewed from Top)





Figure 92. PCB – Inner Layer 5 (Viewed from Top)





Figure 93. PCB – Inner Layer 6 (Viewed from Top)





Figure 94. PCB – Inner Layer 7 (Viewed from Top)





Figure 95. PCB – Bottom Layer (Viewed from Top)





Figure 96. PCB – Silkscreen Bottom (Viewed from Bottom)





Figure 97. PCB – Assembly Bottom



Typical Performance Curves 8.

8.1 Gain Phase Plots, Buck and Boost

BAT12 = 12V, BAT48 = 48V, V_{IN} = VIN_FLY = 12V, BAT12_IN = 5V

| êne Iw | ndical ↔ Timistana 🕴 Tilgger 🛞 Disglay 💉 Classans 🗄 Measure 🔛 Models 🕺 Violens 🕺 Support | Mormal Zoom | ê re |
|---|--|---|--------------------------|
| | PHASE 1 | | |
| | | | |
| a | PHASE 2 | | 62 |
| ci | PHASE 3 | Boot Refresh | œ |
| о | PHASE 4 | Boot Refresh | 54 |
| C8 | PHASE 5 | Boot Refresh | |
| 68 | PHASE 6 | Boot Refresh | * |
| 5.00 Web 9.850 V of st TELEDYNE LEC | | Timebase 8.0 µl Trigger 5.60 µativ Step 4.28 V 125 k5 2.5 05k Edge Positive | 61 9. TELED |

Figure 98. 2-Phase Load Current 0A CCM Mode

| 8 File I Welical ↔ Timetane Trigger ⊕ Display ≠ Consers Measure @ Modiyuts × Unides ⊕ Support | Zie Maina Zsem |
|--|---|
| PHASE 1 | |
| PHASE 2 | |
| PHASE 3 | Boot Refresh |
| PHASE 4 | Boot Refresh |
| PHASE 5 | Boot Refresh |
| PHASE 6 | Boot Refresh |
| 5 50 1000 500 1000 500 1000 500 1000 500 1000 5.00 1000 5.00 1000 5.00 1000 5.00 1000 5.00 1000 5.00 1000 11.50 100 14.50 10 | Timebase 40 m Trisper 5.00 pable 5.00 pable 5.00 420 V 125 kS 2.5 65% Edge Pusilive |

Figure 99. 2-Phase Load Current 0A DE Mode

| ≜ Tei I Watcal ↔ Timitaza / Tigger ⊗ Display ≠ Canson. 🖯 Massan 🗑 Made 🗠 Madpala 🛠 UMMans | © Sepat 2000 Zoon | ⊜rin I Vedcal ™ Theotona † Theoper 101 Degday /* Cansan: Massare Madh : * Andréa X 1988an ⊕ Sapp | at Kornal Zoen |
|--|--|--|--|
| PHASE 1 | | PHASE 1 | |
| PHASE 2 | | PHASE 2 | |
| BHASE 3 | | PHASE 3 | |
| PHASE 4 PHASE 5 PHASE 6 | Boot Refresh Boot Refresh Boot Refresh | PHASE 4 PHASE 5 PHASE 6 | |
| Service Servic | Current 85A | TLEAVE LIGHT | TREEME 40.00 TREEME USES 20000 Big 1.23 USES 20000 Big 1.03 USES 2 |

Figure 100. 3-Phase Load Current 85A

DATU

Figure 102. Analog Tracking

🗄 File 🚦 Welcal 😁 Timebase 🕴 Tagger 😥 Daphy 🧨 Canses 🗄 Measure 🖶 Mah 🗠 Analysis 🛠 UMiles 🔿 Support



Output Voltage

2.00 Wei

Voltage into Track Pin



P11---- P12---













Figure 108. Boost Gain Phase Low Power ISL78224



Figure 105. Boost Bode Plot, BAT12 Input = 12V, 48V at 55A







Figure 109. Boost Gain Phase High Power ISL78224

BAT12 = 12V, BAT48 = 48V, V_{IN} = VIN_FLY = 12V, BAT12_IN = 5V (Continued)



Figure 110. Efficiency Plot - ISL78224

8.2 Efficiency Curves, Buck and Boost











9. Revision History

| Rev. | Date | Description |
|------|--------------|---|
| 4.00 | Jun 7, 2019 | Added "Alternate Configurations" section. Updated board photos for ISL78224EVAL2Z and ISL78226EVAL1Z from red board to blue board. |
| 3.00 | Nov 26, 2018 | Added information about ISL78224EVKIT2Z evaluation board throughout document. Added Revision History. Updated disclaimer. |



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