ISL70005SEHDEMO1Z

The ISL70005SEHDEMO1Z demonstration board is designed to demonstrate the performance of the ISL70005SEH 3A buck regulator and 1A source/sink LDO. The same board can be used to demonstrate the ISL73005SEH part, which is the same silicon die offered with different radiation assurance screening. The demo board is specifically configured for the DDR Memory VDDQ and VTT supply rail applications. The buck regulator output voltage is pin jumper selectable for 1.5V, 1.8V, and 2.5V. The LDO output voltage is configured to track ½ the buck regulator output voltage. The ISL70005SEHDEMO1Z only requires one input supply voltage at the PVIN terminal for operation. The PVIN accepts an input voltage range of 3V to 5.5V.

Key Features

- Dual point-of-load regulator: 3A buck and 1A source/sink LDO
- Fully independent enable, soft-start, and power-good indicator
- 3V to 5.5V operating voltage
- Configured for LDO tracking buck application (such as DDR memory)

Specifications

- Analog and buck regulator input voltage range (PVIN): 3V to 5.5V
- Buck output voltage selection: 2.5V (DDR), 1.8V (DDR2), or 1.5V (DDR3)
- Maximum buck output current: 3A
- Buck preset switching frequency: 1MHz
- LDO input voltage (L_VIN) range: 1.0V to PVIN
- LDO output voltage tracks 1/2 of buck V_{OUT}
- Maximum LDO output (L_OUT) current: 1A sourcing or 1A sinking
- Board dimension: 11cm width x 7.5cm height
- Board layers: Four
- Board PCB copper weight: 2oz.
- Board revision: A

Ordering Information

Part Number	Description
ISL70005SEHDEMO1Z	ISL70005SEH evaluation board

Related Literature

For a full list of related documents, visit our website:

- ISL70005SEH, ISL73005SEH device page

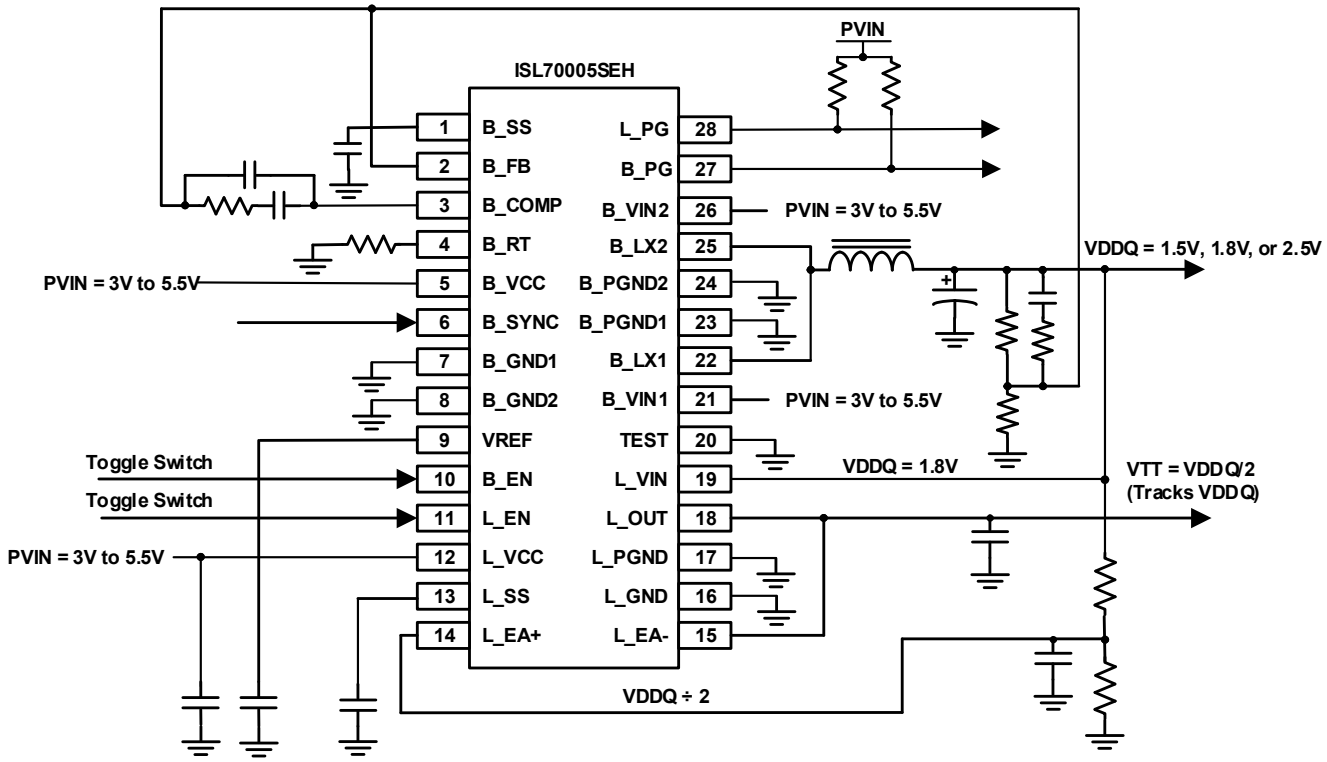

Figure 1. ISL70005SEHDEMO1Z Block Diagram

1. Functional Description

1.1 Operating Range

The buck regulator output B_OUT is capable of sourcing up to 3A. The buck output voltage is board jumper selectable at 1.5V, 1.8V, and 2.5V. The buck regulator is preset with 1MHz switching frequency with a 2.2µH output inductor and 150µF output capacitor with the option of being synchronized to an external clock. The LDO regulator output L_OUT is capable of sourcing or sinking up to 1A. The LDO L_EA+ reference input to the error amplifier is board jumper selectable to either the 0.6V VREF pin voltage on the ISL70005SEH or ½ the buck output voltage for DDR VTT rail applications. The LDO output voltage is board jumper selectable to 1.2V or set to equal the L_EA+ reference voltage (½ of the buck output).

Independent enable control toggle switches are available for the buck and the LDO. The toggle switch control can also be tied together so that one switch controls both.

1.2 Quick Start Guides

1.2.1 Buck with LDO in DDR Tracking Mode

1. See Table 1 to set up the jumpers properly to adjust the buck output voltage and configure the LDO for tracking buck output.
2. Ensure jumper on JP1, JP9, and JP10 are populated. Ensure either SW1 or SW2 is off (down position). Populate jumper JP6 in the 2-3 position.
3. Apply voltage (3V to 5.5V) to PVIN banana connectors BA1 and BA2.
4. Because JP1 is populated, connecting B_EN and L_EN together, either SW1 or SW2 toggle switch enables (up position) and disables (down position) both the buck and LDO together.
5. The LDO L_OUT (VTT rail) is one-half of the buck output voltage (VDDQ rail) determined by the jumper settings on JP2 and JP3.
6. **IMPORTANT:** With the buck output powering the LDO input, care must be taken on the output current loading of the buck regulator. When the LDO is sourcing current, it is supplied by the buck regulator and the buck output B_OUT 3A limit to external loading is decreased by the LDO load. For example, if LDO is sourcing 1A, the buck can only provide an additional 2A to the external load.

1.2.2 Dual Independent Buck and LDO Output

1. **IMPORTANT:** There is a 0.5mΩ resistor (R16) on the back side of the demonstration board that connects the buck output voltage (B_OUT) to the LDO sourcing NMOS FET input (L_VIN). R16 must be removed for dual independent buck and LDO operation.
2. See Table 1 to set up the jumpers properly to adjust the buck output voltage and configure the LDO for independent output.
3. Ensure jumper on JP1, JP9, and JP10 are removed. Populate jumper JP6 in the 1-2 position.
4. Apply voltage (3V to 5.5V) to PVIN banana connectors BA1 and BA2.
5. Apply voltage (1.5V to PVIN) to L_VIN banana connectors BA5 and BA7.
6. If the buck enable switch SW1 is on (up position), the buck is enabled and switching at 1MHz. A voltage defined by the jumper settings of JP2 and JP3 is present on B_OUT at BA3. If SW1 is off (down position), the buck is disabled and B_OUT = 0V.
7. If the LDO enable switch SW2 is on (up position), the LDO is enabled and a voltage of 1.2V is present on L_OUT at BA7. If SW2 is off (down position), the LDO is disabled and L_OUT = 0V.

Table 1. Jumper Settings for ISL70005SEHDEMO1Z

Jumper	Function	Description	Application Configuration	
			Independent Buck and LDO Regulator	Buck and LDO for DDR Power
JP1	Connects B_EN and L_EN together	Populate for single switch control of L_EN and B_EN.	Remove jumper	Populate jumper
JP2	Connects R8 to B_FB	Populate for buck output voltage 1.8V. Ensure JP3 is removed. If no jumper present on JP2 and JP3, buck output voltage is 1.5V. If JP2 and JP3 both have a jumper, buck output voltage is programmed to 2.8V.		
JP3	Connects R7 to B_FB	Populate for buck output voltage 2.5V. Ensure JP2 is removed. If no jumper present on JP2 and JP3, buck output voltage is 1.5V. If JP2 and JP3 both have a jumper, buck output voltage is programmed to 2.8V.		
JP6	Connects L_EA+ to VREF or buck output	Populate in the 1-2 position for connecting L_EA+ to VREF pin. Populate in the 2-3 position for connecting to buck output voltage divided down by the ratio of R15 and R14.	Jumper in 1-2 position	Jumper in 2-3 position
JP9	Shorts resistor R21	Populate for LDO unity gain, setting L_OUT = L_EA+.	Remove jumper	Populate jumper
JP10	Connects buck V_{OUT} to resistor divider	Populate for connecting buck V_{OUT} to the R14 and R15 resistor divider network.	Remove jumper	Populate jumper
J1	LDO output voltage sensing.	Do not populate with jumper. This is a 2-pin header for sensing LDO output voltage.		
J2	Buck B_LXx voltage sensing.	Do not populate with jumper. This is a 2-pin header for sensing buck regulator switching node.		
J3	B_OUT voltage sensing.	Do not populate with jumper. This is a 2-pin header for sensing buck output voltage.		

1.3 Changing Output Voltage on Buck

Jumpers JP2 and JP3 are made available to easily configure the buck output voltage quickly. With no jumpers on JP2 and JP3, the output voltage is 1.5V. With only JP2 populated, it is 1.8V. With only JP3 populated, it is 2.5V. If JP2 and JP3 are both populated, it is 2.8V. If a different output voltage altogether is needed, you must change the R7, R8, or R43 values. Renesas recommends not changing R10 to preserve the characteristics of the Type III compensation network.

Table 2. Buck V_{OUT} Jumper Settings

VOUT	JP2 Jumper	JP3 Jumper
1.5V	Off	Off
1.8V	On	Off
2.5V	Off	On
2.8V	On	On

Note: The buck regulator has minimum on and off-times on the B_LXx pins, combined with the switching frequency, can hit duty cycle limitations for producing the desired output voltage.

1.4 Changing Buck Switching Frequency

The ISL70005SEHDEMO1Z is configured for 1MHz switching by using a R4 = 45.3kΩ resistor on the B_RT pin to B_GND. The demonstration board includes a 2.2µH inductor and 150µF tantalum capacitor for the LC output filter. If you need to select a different switching frequency, see Figure 2 for selecting the appropriate R4 value on B_RT to set the switching frequency. The ISL70005SEHDEMO1Z includes a dual footprint for the inductor to allow for a higher inductance value with similar saturation current characteristics for the lower switching frequencies.

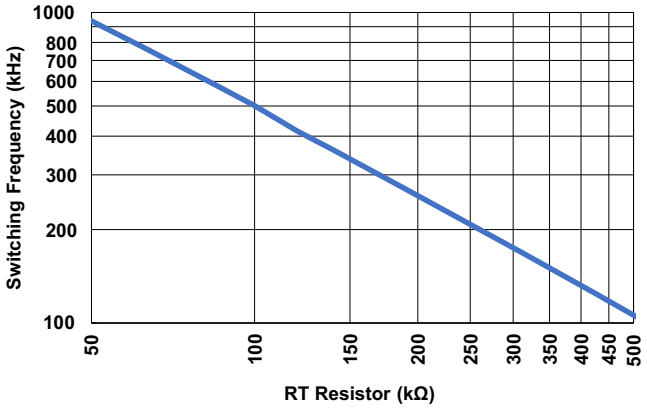

Figure 2. Buck f_{SW} vs RT Resistor on B_RT Pin

1.5 Using External Clock for Buck Switching Frequency

If you need to synchronize the buck switching frequency to an external clock, a test point TP1 is made available for connection. See the ISL70005SEH datasheet for more information about external synchronization.

1.6 Changing Buck Output Inductor

The ISL70005SEHDEMO1Z is populated with a 2.2µH inductor on the L1A footprint targeted for 1MHz switching frequency. The inductor used on the ISL70005SEHDEMO1Z is a Coilcraft XFL4020-222ME. If you need to use a lower switching frequency, a larger inductance must be used to maintain a similar ripple current. The L1B footprint (inductor not populated) is physically larger to accommodate a larger inductance value with similar saturation current ratings. For example, with f_{SW} = 100kHz the L1B footprint is sized to accommodate a Coilcraft XAL6060-153ME 15µH inductor.

1.7 Changing Output Voltage on LDO

The LDO output voltage is set by the equation: L_OUT = L_EA+ * (R21/R22 + 1)

There are three variables to control the LDO output voltage. The L_EA+ voltage can be connected to the ISL70005SEH VREF = 0.6V by setting the jumper in the 1-2 position of JP6 or to one-half of the buck output voltage by setting the jumper in the 2-3 position. Additionally, you can put in an external reference by not having a jumper on JP6 and applying a voltage to pin 2 of JP6 and GND. The ISL70005SEHDEMO1Z is preset with a feedback gain of 2 with R21 = R22 = 1kΩ. You can populate jumper JP9 to short out R21 for unity gain feedback to set L_OUT = L_EA+. You can also change the R21 and R22 resistor values for the desired feedback gain.

1.8 LDO Sinking Load Current

To sink current into the LDO output, R5 (a not populated 2512 sized SMD resistor footprint) is made available on the back side of the ISL70005SEHDEMO1Z demonstration board. This resistor pad is connected between L_OUT and PVIN. The sinking current into the LDO is:

ISINK = PVIN - L_OUT / R, where R is the resistor placed on R5.

2. PCB Layout Guidelines

2.1 ISL70005SEHDEMO1Z Evaluation Board

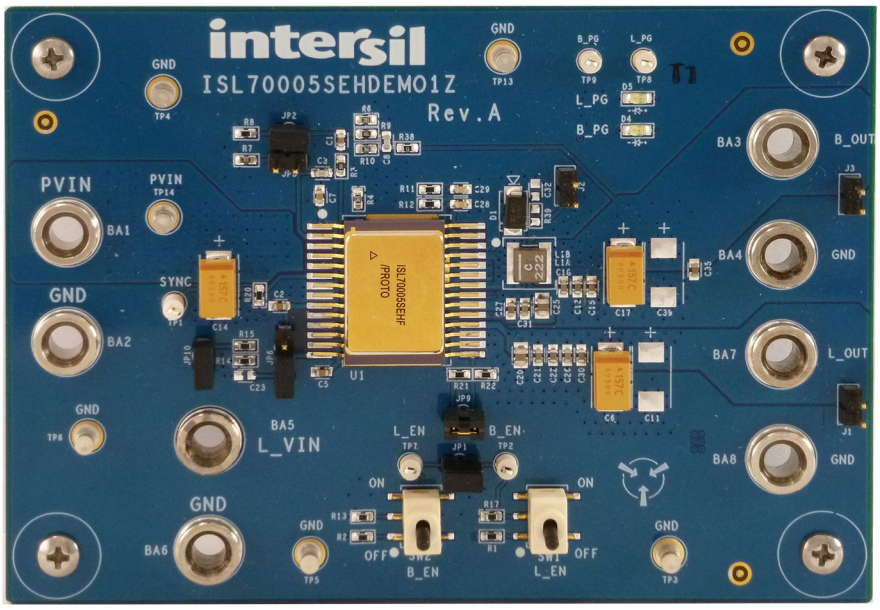

Figure 3. ISL70005SEHDEMO1Z Evaluation Board (Top)

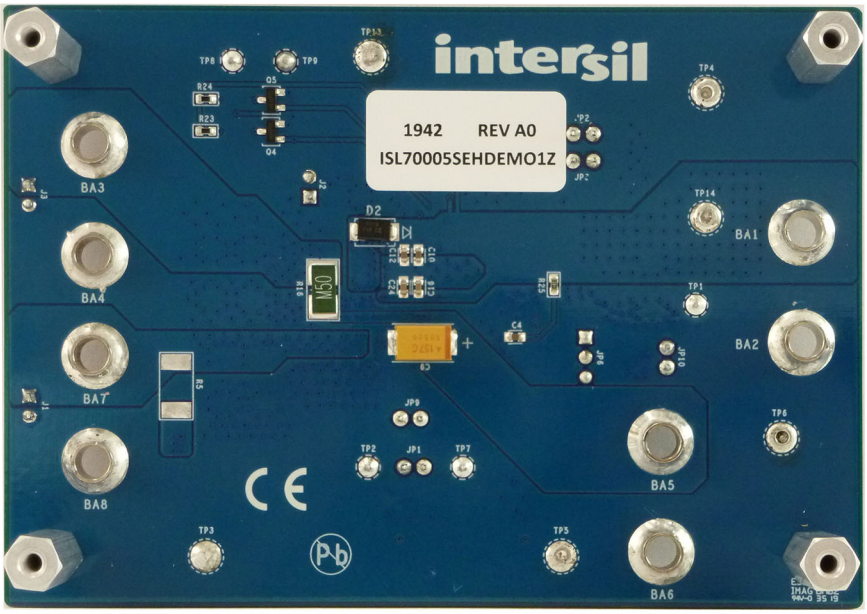

Figure 4. ISL70005SEHDEMO1Z Evaluation Board (Bottom)

2.2 ISL70005SEHDEMO1Z Schematic

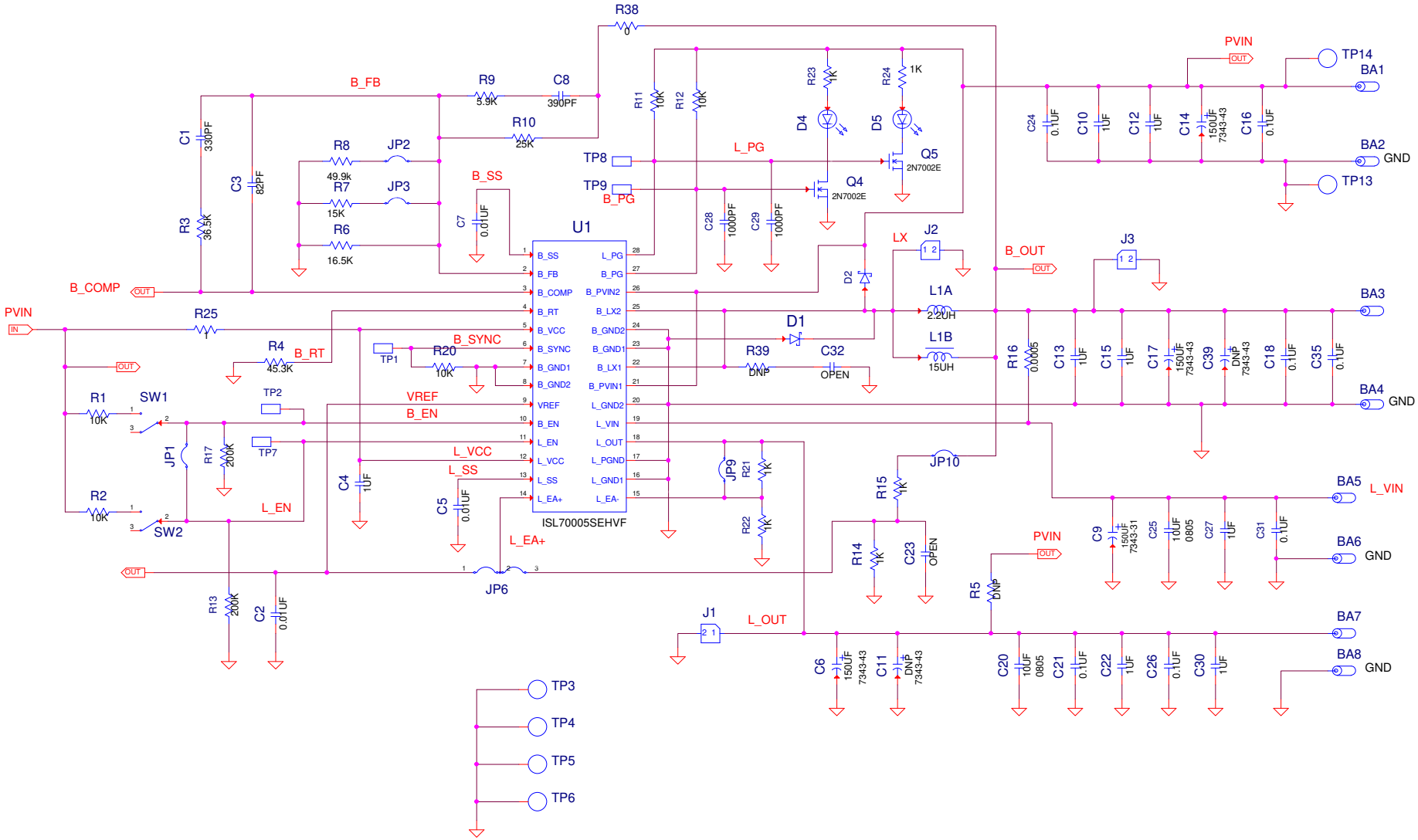

Figure 5. Schematic

2.3 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1		PWB-PCB, ISL70005SEHDEMO1Z, REVA, ROHS	Imagineering Inc	ISL70005SEHDEMO1ZREVAPCB
8	C4, C10, C12, C13, C15, C22, C27, C30	CAP, SMD, 0603, 1.0µF, 16V, 10%, X7R, ROHS	TDK	C1608X7R1C105K
2	C20, C25	CAP, SMD, 0805, 10µF, 16V, 20%, X7R, ROHS	Taiyo Yuden	EMK212BB7106MG-T
2	C28, C29	CAP, SMD, 0603, 1000pF, 16V, 10%, X7R, ROHS	Venkel	C0603X7R160102KNE
3	C2, C5, C7	CAP, SMD, 0603, 0.01µF, 16V, 10%, X7R, ROHS	Venkel	C0603X7R160-103KNE
7	C16, C18, C21, C24, C26, C31, C35	CAP, SMD, 0603, 0.1µF, 16V, 10%, X7R, ROHS	Murata	GCM188R71C104KA37D
5	C4, C10, C12, C13, C15	CAP, SMD, 0603, 1.0µF, 10V, 10%, X7R, ROHS	AVX	0603ZC105KAT2A
1	C1	CAP, SMD, 0603, 330pF, 50V, 10%, X7R, ROHS	Yageo	CC0603KRX7R9BB331
1	C8	CAP, SMD, 0603, 390pF, 50V, 10%, X7R, ROHS	Venkel	C0603X7R500-391KNE
1	C3	CAP, SMD, 0603, 82pF, 50V, 10%, C0G, ROHS	Venkel	C0603COG500-820KNE
0	C23, C32	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS		
4	C6, C9, C14, C17	CAP-TANT, LOWESR, SMD, 7.3x4.3mm, 150µF, 16V, 10%, 30mΩ, ROHS	AVX	TPME157K016R0030
1	L1A	COIL-PWR INDUCTOR, SMD, 4mm, 2.2µH, 20%, 3.5A, 21.3mΩ, ROHS	Coilcraft	XFL4020-222MEB
6	TP3, TP4, TP5, TP6, TP13, TP14	CONN-DBL TURRET, TH, 0.218x0.078 PCB MNT, TIN/BRASS, ROHS	Keystone	1502-1
5	TP1, TP2, TP7, TP8, TP9	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	Keystone	5002
8	BA1-BA8	CONN-JACK, MINI BANANA, 0.175 PLUG, NICKEL/BRASS, ROHS	Keystone	575-4
1	JP6	CONN-HEADER, 1x3, BREAKAWY 1x36, 2.54mm, ROHS	BERG/FCI	68000-236HLF
8	J1, J2, J3, JP1, JP2, JP3, JP9, JP10	CONN-HEADER, 1x2, RETENTIVE, 2.54mm, 0.230x0.120, ROHS	BERG/FCI	69190-202HLF
5	JP1, JP2, JP9, JP10, JP6-Pins 2-3	CONN-JUMPER, SHORTING, 2PIN, BLACK, GOLD, ROHS	Sullins	SPC02SYAN
2	D1, D2	DIODE-SCHOTTKY RECITIFIER, SMD, 2P, SMA, 20V, 1A, ROHS, DNP-PLACE HOLDER		
2	D4, D5	LED-GaAs RED, SMD, 2x1.25mm, 100mW, 40mA, 10mcd, ROHS	Liteon/Vishay	LTST-C170CKT
1	U1	IC-RAD HARD LDO REGULATOR, SMD, 28P, CFP, ROHS	Renesas Electronics America	ISL70005SEHF/PROTO
2	Q4, Q5	TRANSIST-MOS, N-CHANNEL, SMD, SOT23, 60V, 0.24A, ROHS	Vishay/Siliconix	2N7002E
0	R39	RESISTOR, SMD, 0603, 0.1%, MF, DNP-PLACE HOLDER		

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1	R25	RES, SMD, 0603, 1Ω, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3RQF1R0V
1	R38	RES, SMD, 0603, 0Ω, 1/10W, TF, ROHS	Venkel	CR0603-10W-000T
6	R14, R15, R21, R22, R23, R24	RES, SMD, 0603, 1k, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF1001V
5	R1, R2, R11, R12, R20	RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-1002FT
1	R8	RES, SMD, 0603, 49.9k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-4992FT
1	R6	RES, SMD, 0603, 16.5k, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF1652V
2	R13, R17	RES, SMD, 0603, 200k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-2003FT
1	R7	RES, SMD, 0603, 15.0k, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF1502V
1	R10	RES, SMD, 0603, 24.9k, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF2492V
1	R3	RES, SMD, 0603, 36.5k, 1/10W, 1%, TF, ROHS	Vishay	CRCW060336K5FKEA
1	R4	RES, SMD, 0603, 45.3k, 1/10W, 1%, TF, ROHS	Yageo	RC0603FR-0745K3L
1	R9	RES, SMD, 0603, 5.90k, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF5901V
0	R5	RES, SMD, 2512, DNP, DNP, DNP, TF, ROHS		
1	R16	RES, SMD, 2512, 0.5mΩ (0.0005Ω), 3W, 1%, TF, ROHS	IRC	ULRG32512R0005FLFSLT
2	SW1, SW2	SWITCH-TOGGLE, SMD, 6PIN, SPDT, 2POS, ON-NONE-ON, ROHS	ITT Industries/C&K Division	GT11MSCBE
4	Four corners	SCREW, 4-40x1/4in, PHILLIPS, PANHEAD, STAINLESS, ROHS	Building Fasteners	PMSSS 440 0025 PH
4	Four corners	STANDOFF, 4-40x3/4in, F/F, HEX, ALUMINUM, 0.25 OD, ROHS	Keystone	2204
0	C11, C39 (TPME157K016R0030)	DO NOT POPULATE OR PURCHASE		
0	L1B (XAL6060-153MEC)	DO NOT POPULATE OR PURCHASE		

2.4 Board Layout

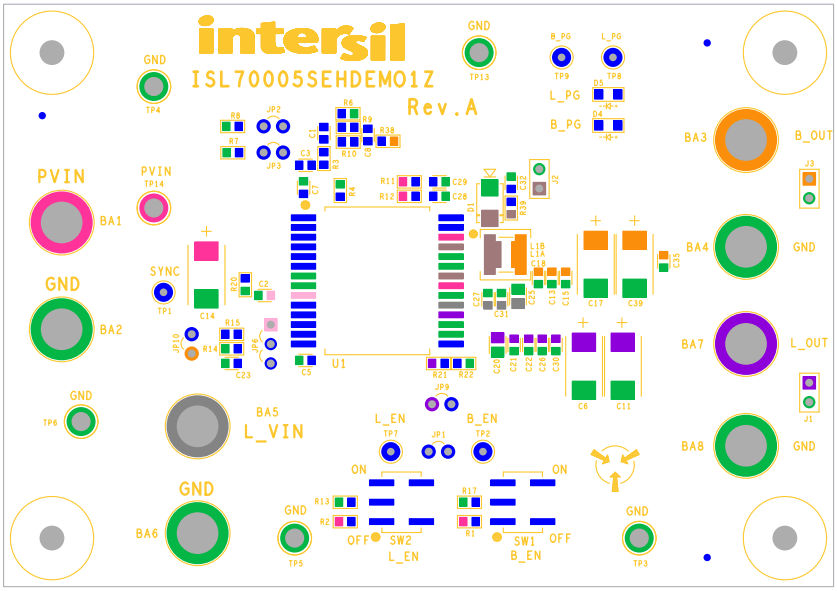

Figure 6. Silkscreen Top Layer

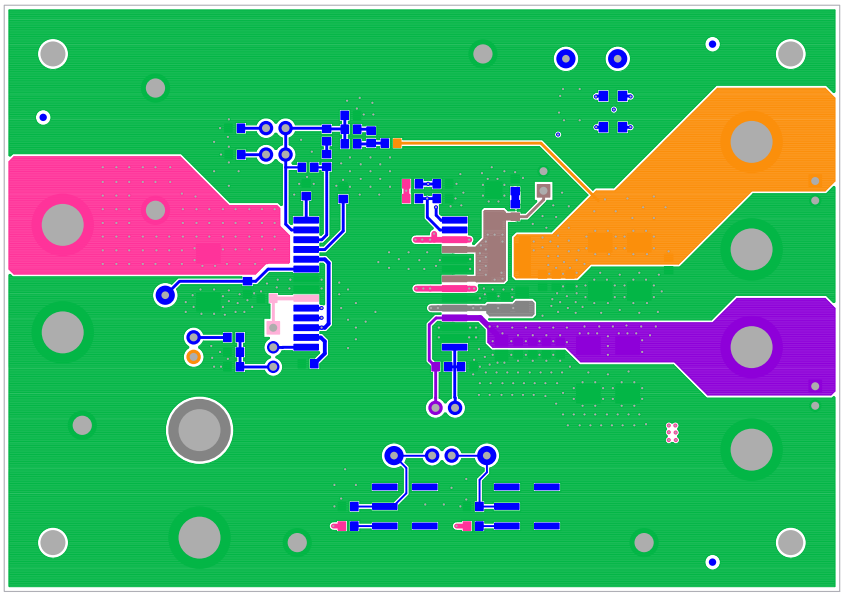

Figure 7. Top Layer

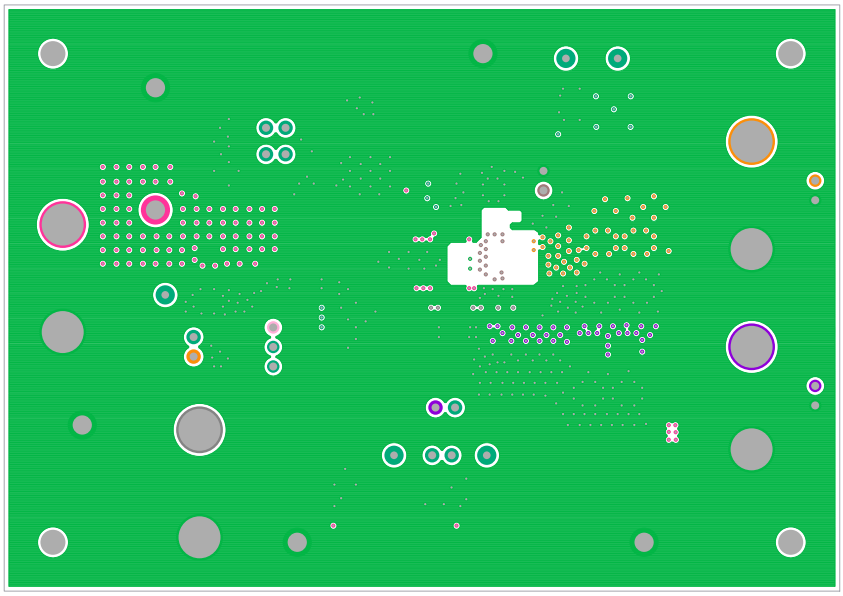

Figure 8. Layer 2

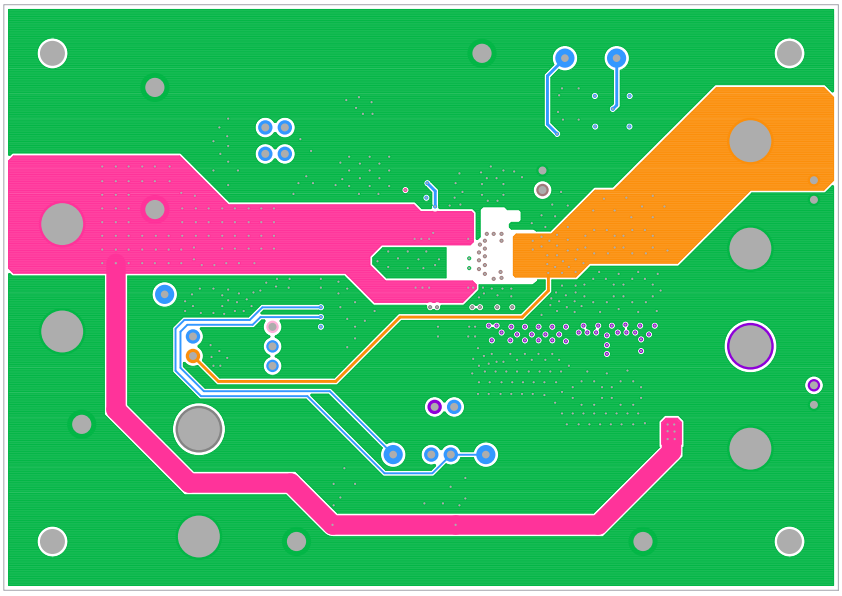

Figure 9. Layer 3

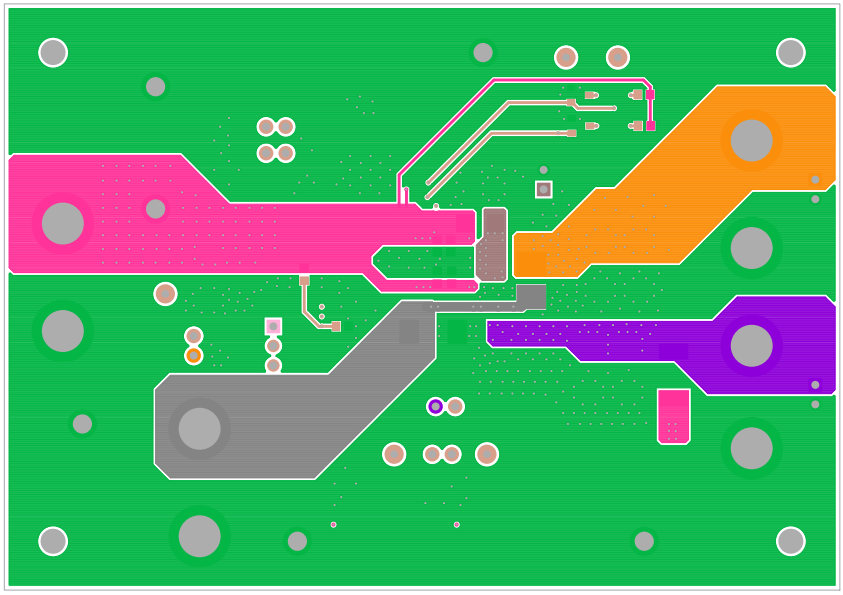

Figure 10. Bottom Layer

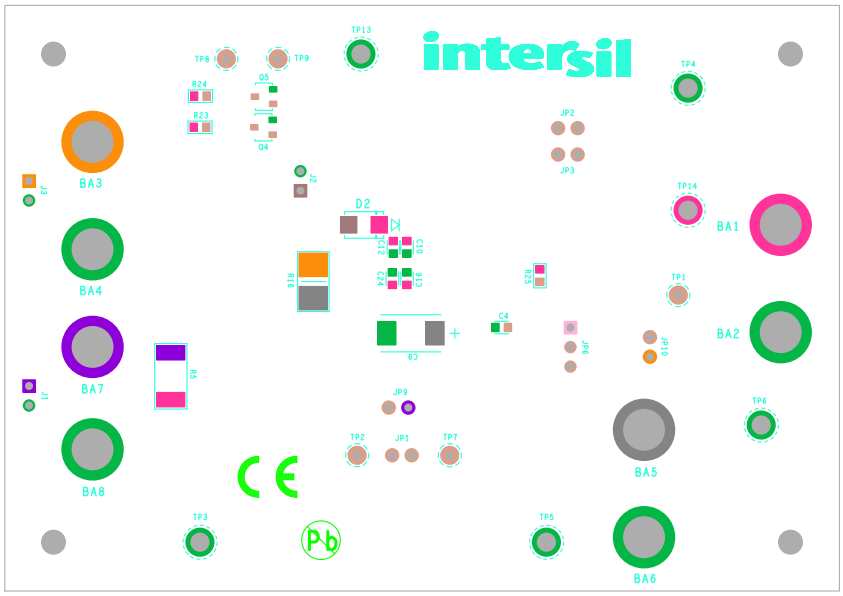

Figure 11. Silkscreen Bottom Layer

3. Typical Performance Curves

Unless otherwise noted, the test platform is the ISL70005SEHDEMO1Z where B_PVIN = B_VCC = L_VCC = 5V; L_VIN = B_OUT; f_{SW} = 1MHz; Buck C_{IN} = 150µF tantalum + 2x1µF ceramic; Buck C_{OUT} = 150µF tantalum + 2x1µF ceramic; L_{OUT} = 2.2µH; LDO C_{IN} = 150µF tantalum + 11µF ceramic; LDO C_{OUT} = 150µF tantalum +12µF ceramic; L_OUT = 0.5*B_OUT; L_EA+ = 0.5*B_OUT; T_A = +25°C.

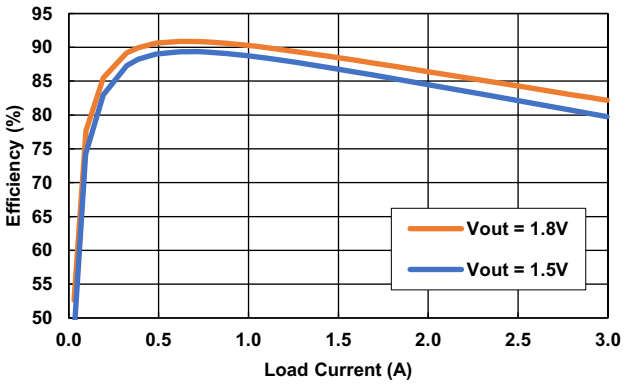

Figure 12. Efficiency vs I_{OUT}; B_VIN = 3V; 1MHz

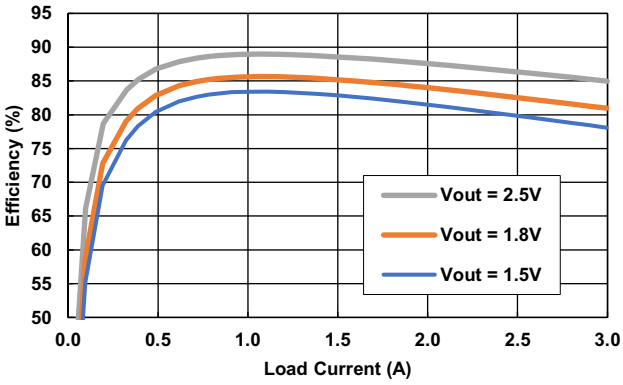

Figure 13. Efficiency vs I_{OUT}; B_VIN = 5V; 1MHz

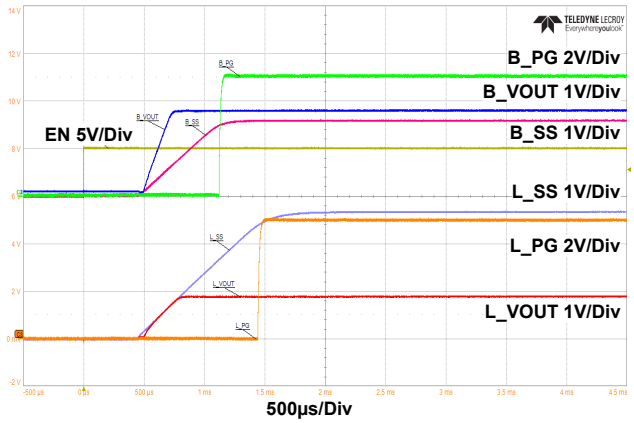

Figure 14. Buck and LDO Soft-Start; B_EN = L_EN; Load = 0A on Buck and LDO; DDR Configuration

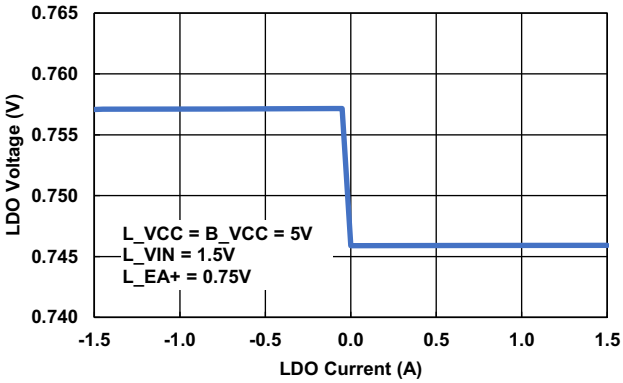

Figure 15. LDO Load Regulation DDR3 Configuration

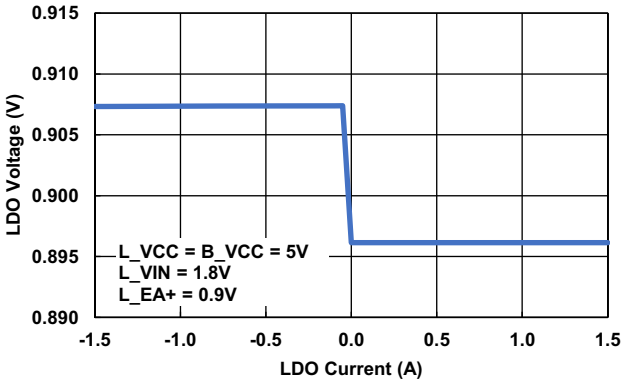

Figure 16. LDO Load Regulation DDR2 Configuration

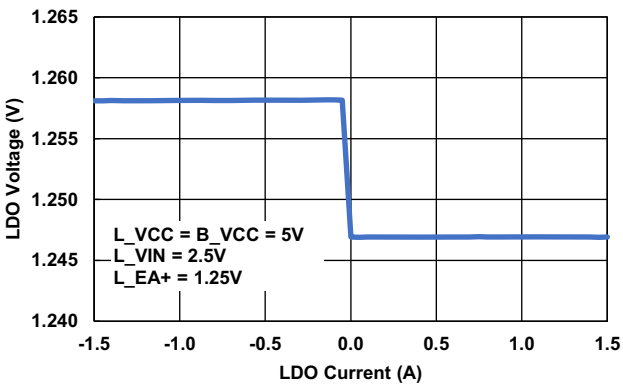

Figure 17. LDO Load Regulation DDR Configuration

Unless otherwise noted, the test platform is the ISL70005SEHDEMO1Z where B_PVIN = B_VCC = L_VCC = 5V; L_VIN = B_OUT; f_{SW} = 1MHz; Buck C_{IN} = 150µF tantalum + 2x1µF ceramic; Buck C_{OUT} = 150µF tantalum + 2x1µF ceramic; L_{OUT} = 2.2µH; LDO C_{IN} = 150µF tantalum + 11µF ceramic; LDO C_{OUT} = 150µF tantalum +12µF ceramic; L_OUT = 0.5*B_OUT; L_EA+ = 0.5*B_OUT; T_A = +25°C. **(Continued)**

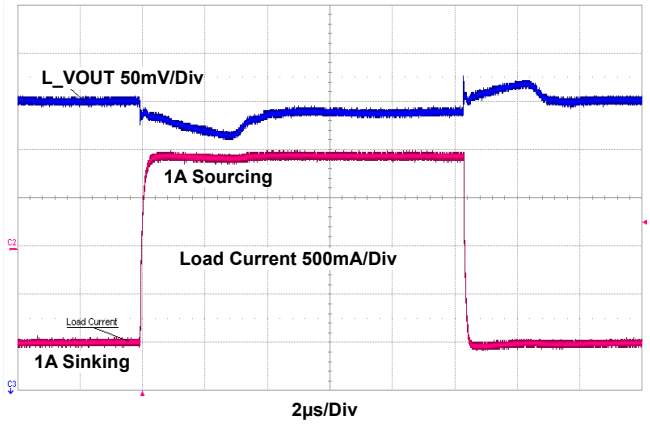

Figure 18. LDO Source-to-Sink Transient Response; L_OUT = L_EA- = L_EA+ = 0.6V

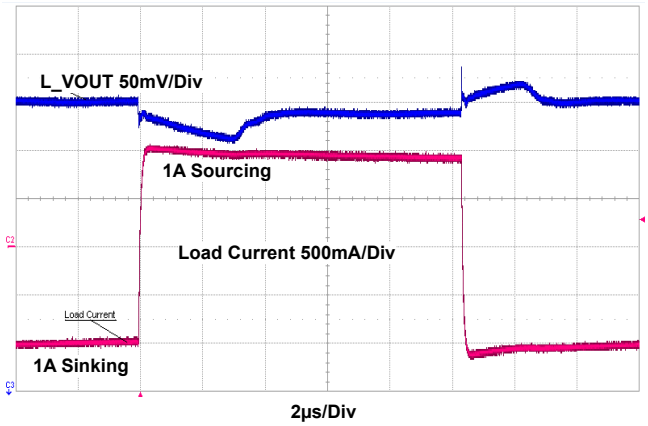

Figure 19. LDO Source-to-Sink Transient Response; L_OUT = L_EA- = L_EA+ = 0.9V

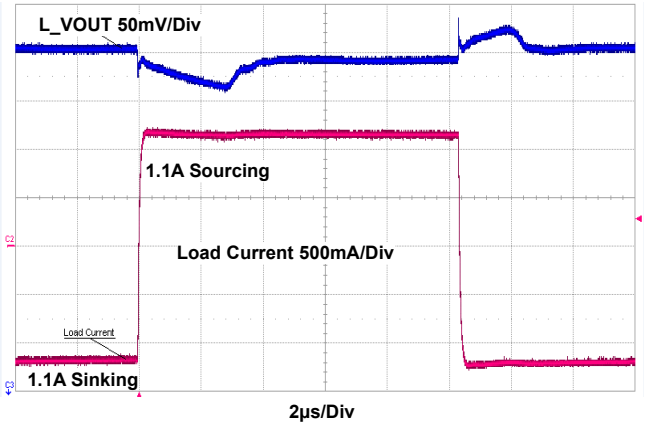

Figure 20. LDO Source-to-Sink Transient Response; L_OUT = L_EA- = L_EA+ = 1.25V

4. Revision History

Rev.	Date	Description
2.01	Nov 16, 2022	Added reference to ISL73005SEH on page 1.
2.00	Jan 16, 2020	Made changes to buck VOUT range from 1.8V, 2.5V, or 3.3V to 1.5V, 1.8V, or 2.5V throughout.
1.01	Jan 6, 2020	Changed diodes D1 and D2 in BOM to DNP.
1.00	Dec 12, 2019	Initial release

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/