ISL33001MSOPEVAL1Z, ISL33002MSOPEVAL1Z, ISL33003MSOPEVAL1Z Evaluation Board

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Description

The ISL33001MSOPEVAL1Z, ISL33002MSOPEVAL1Z, and ISL33003MSOPEVAL1Z evaluation board is designed to provide a quick and easy method for evaluating the ISL33001, ISL33002, ISL33003 2-Channel Bus Buffer.

It is recommended to understand the operation of the IC for a complete utilization of the evaluation board. Refer to the latest datasheet (FN7560) for the features and operation of the ISL33001, ISL33002, ISL33003 2-Channel Bus Buffer. The evaluation board is developed to evaluate the performance of the buffer used in a typical application.

A picture of the main evaluation board is shown in Figure 1. The ISL3300x MSOP package IC is soldered onto the evaluation board and is designated as U1. A typical application of the ISL3300x is an I^2C bus buffer. The evaluation board contains all the necessary components to interface the buffer to an I^2C bus.

Discrete NMOS transistors are used to produce the pull-down functions of a wired-AND bus. Each SDA/SCL pin on the buffer is connected to an external open-drain NMOS transistor. The evaluation board also contains connections for the bus pull-up resistor and load capacitance. The logic input pins on the ISL3300x IC can be held logic High by a pull-up resistor or driven dynamically with an external logic source.

Features

- Evaluation Board for ISL33001IUZ, ISL33002IUZ, and ISL33003IUZ IC in MSOP Package
- +2.3V to +5.5V Supply Operation
- Configured to operate in I^2C environment
- Two Channel Supply for Level Shifting Applications (ISL33002 and ISL33003)
- On-Board Discrete NMOS Open-Drain Transistors Connected to SDA/SCL Pins
- 3V Logic for NMOS Transistor Gate
- On-Board Discrete Bus Pull-Up Resistors and Load Capacitance on SDA/SCL Pins
- Convenient Test Points on SDA/SCL pins

Evaluation Board

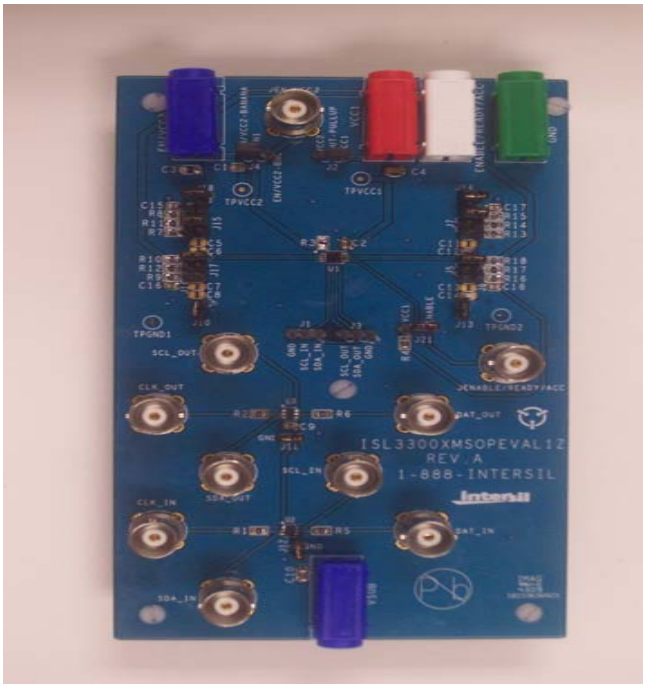


FIGURE 1. TOP VIEW

Board Architecture / Layout

Basic Layout of Evaluation Board

The basic layout of the main board is as follows (refer to Figure 1):

1. V_{CC1}, V_{CC2} and GND connections are at the top of the board. The board operates on a +2.3V to +5.5V power supply.
2. Input connections for the logic control pins are available through BNC connectors or banana jacks.
3. The ISL3300x buffer is located at the center of the board designated as U1.
4. Pull-up resistors and bus capacitance connections to the SDA/SCL pins are available to the right and left of U1.
5. U2 and U3 are the NMOS Open-Drain MOSFETs connected to the SDA/SCL pins of the ISL3300x buffer. The gate and drain of the MOSFETs are brought out to BNC connectors.

ISL3300x Buffers

The ISL33001, ISL33002, ISL33003 family of 2-Channel Bus Buffers are designed to isolate the bus capacitance and improve the rise time performance of heavily loaded buses. The family of buffers offer +2.3V to +5.5V operation, hot swap capability, transient rise time accelerators, low power shutdown (ISL33001 and ISL33003) and level shifting capability (ISL33002 and ISL33003).

The buffers are designed to operate in wired-AND environments such as I^2C bus, supporting 400kHz Fast Mode operation while being capable of driving the I^2C specified maximum capacitive loads of 400pF on the bus.

Power Supply

The ISL3300xMSOPEVAL1Z boards required a +2.3V to +5.5V supply voltage to power the ISL3300x IC. For ISL33002 and ISL33003 with level shifting power supplies, a supply voltage in the +2.3V to +5.5V must be connected to the V_{CC1} and V_{CC2} banana jack connections. The evaluation board contains 0.01µF local decoupling capacitor near the supply pins of the ISL3300x IC.

Note: Jumper J4 connects either banana jack EN/V_{CC2} or BNC connector EN/V_{CC2} to pin 1 of the ISL3300x IC. When the jumper is in the 1-2 position the connection is made to the banana jack. When in the 2-3 position the connection is made to the BNC connector.

Logic Control Inputs

ISL33001

The ISL33001 device contains an enable logic input pin "EN" and a logic output pin "READY".

The enable pin connection can be made at the banana jack or BNC connector. When the EN pin is driven high, the part is enabled and the buffer will be connected once it enters a valid state. When the EN pin is driven low, the part is disabled, the IC draws low ICC current and any signals on one side of the buffer will not appear on the other side of the buffer.

Note: Jumper J4 connects either banana jack EN/V_{CC2} or BNC connector EN/V_{CC2} to pin 1 (EN) of the ISL33001 IC. When the jumper is in the 1-2 position the connection is made to the banana jack. When in the 2-3 position the connection is made to the BNC connector.

The READY pin is an Open-Drain logic output pin on the ISL33001 IC. The evaluation board gives the option to connect the READY pin to a 10kΩ pull-up resistor to V_{CC1} or to an external connector.

Note: Jumper J21 connects either the 10kΩ pull-up resistor or the external connector to pin 4 (READY) on the ISL33001 IC. When J21 is in the 1-2 position the READY pin is connected to the 10kΩ pull-up resistor. When J21 is in the 2-3 position the READY pin is connected commonly to banana jack EN/READY/ACC and BNC connector JEN/READY/ACC.

ISL33002

The ISL33002 device contains a level shifting supply voltage V_{CC2} and an Accelerator disable pin ACC.

The V_{CC2} connection can be made at the banana jack EN/V_{CC2}. For the ISL33002 IC, the threshold voltages on the SDA_OUT and SCL_OUT pins are referred to the V_{CC2} supply.

Note: Jumper J4 connects either banana jack EN/V_{CC2} or BNC connector EN/V_{CC2} to pin 1 (V_{CC2}) of the ISL33002 IC. When the jumper is in the 1-2 position the connection is made to the banana jack. When in the 2-3 position the connection is made to the BNC connector.

Note: Jumper J2 connects the pull-up resistors on the SDA_OUT and SCL_OUT pins to either the V_{CC1} or V_{CC2} supply. When J2 is in the 1-2 position the pull-up resistors are connected to V_{CC2}. When J2 is in the 2-3 position the pull-up resistors are connected to V_{CC2}.

The ACC pin is a logic input pin that enables/disables the bus accelerators on the ISL33002 IC SDA/SCL pins. The evaluation board gives the option to connect the ACC pin to a 10kΩ pull-up resistor to V_{CC1} to enabled the accelerators at all times or to banana jack/BNC connectors for external control.

Jumper J21 connects either the 10kΩ pull-up resistor or the external connector to pin 4 (ACC) on the ISL33002 IC. When J21 is in the 1-2 position the ACC pin is connected to the 10kΩ pull-up resistor. When J21 is in the 2-3 position the ACC pin is connected commonly to banana jack EN/READY/ACC and BNC connector JEN/READY/ACC.

ISL33003

The ISL33003 device contains a level shifting supply voltage V_{CC2} and an enable logic input pin EN.

The V_{CC2} connection can be made at the banana jack EN/V_{CC2}. For the ISL33003 IC, the threshold voltages on the SDA_OUT and SCL_OUT pins are referred to the V_{CC2} supply.

Note: Jumper J4 connects either banana jack EN/V_{CC2} or BNC connector EN/V_{CC2} to pin 1 (V_{CC2}) of the ISL33003 IC. When the jumper is in the 1-2 position the connection is made to the banana jack. When in the 2-3 position the connection is made to the BNC connector.

Note: Jumper J2 connects the pull-up resistors on the SDA_OUT and SCL_OUT pins to either the V_{CC1} or V_{CC2} supply. When J2 is in the 1-2 position the pull-up resistors are connected to V_{CC2}. When J2 is in the 2-3 position the pull-up resistors are connected to V_{CC2}.

SDA / SCL Pins

To include the features to evaluate the ISL3300x buffers on the evaluation board, the necessary components are available to interface with a 2-Channel wired-AND bus such as I^2C.

The I^2C bus utilizes an active pull-down circuit to drive a low on the bus and a pull-up resistor to passively pull the

bus high. The pull-up resistance and the parasitic bus capacitance on the SDA/SCL lines define the transient performance and maximum data rate of the I^2C bus.

On the ISL3300xMSOPEVAL1Z evaluation boards, the SDA/SCL pins on the buffer are connected to an open-drain NMOS transistor, pull-up resistors to the V_{CC} supply, and place holders for adding load capacitance.

Each SDA/SCL pin has three available pull-up resistor values: 1kΩ, 2.7kΩ, and 10kΩ. These values are commonly used for the pull-up resistance in I^2C applications. A two pin jumper on the pull-up resistors (J5, J7, J15, J17) connects one of these resistors to the associated SDA/SCL pin.

Each SDA/SCL pin has two place holders for capacitors to increase the load capacitance to the buffer. The place holders are always connected to the SDA/SCL pins on the IC.

NMOS Open-Drain MOSFETs

In addition to the pull-up resistors and the place holders for bus capacitors, each SDA/SCL pin is connected to the drain terminal of an open-drain NMOS transistor. The transistors emulate the I^2C devices that are connected to the ISL3300x buffer in a typical application.

The gates of the transistors require 3V logic levels and can be interfaced through the BNC connectors on the board (see Table 1 for the connections of the gate to the associated SDA/SCL pin).

TABLE 1. MOSFET CONNECTIONS TO ISL3300x BUFFER

GATE	U2/U3 PIN #	DRAIN	U2/U3 PIN #
CLK_IN	U2-2	SCL_IN	U2-6
CLK_OUT	U3-2	SCL_OUT	U3-6
DAT_IN	U2-5	SDA_IN	U2-3
DAT_OUT	U3-5	SDA_OUT	U3-3

The connections from the NMOS drain to the SDA/SCL pins can be disconnected by the jumpers J18 (SCL_OUT), J10 (SCL_IN), J14 (SDA_OUT), and J13 (SDA_IN). Disconnecting the SDA/SCL pins from the drain of the transistor will isolate the SDA/SCL pin capacitance of the buffer from the Drain-Source capacitance of the MOSFET.

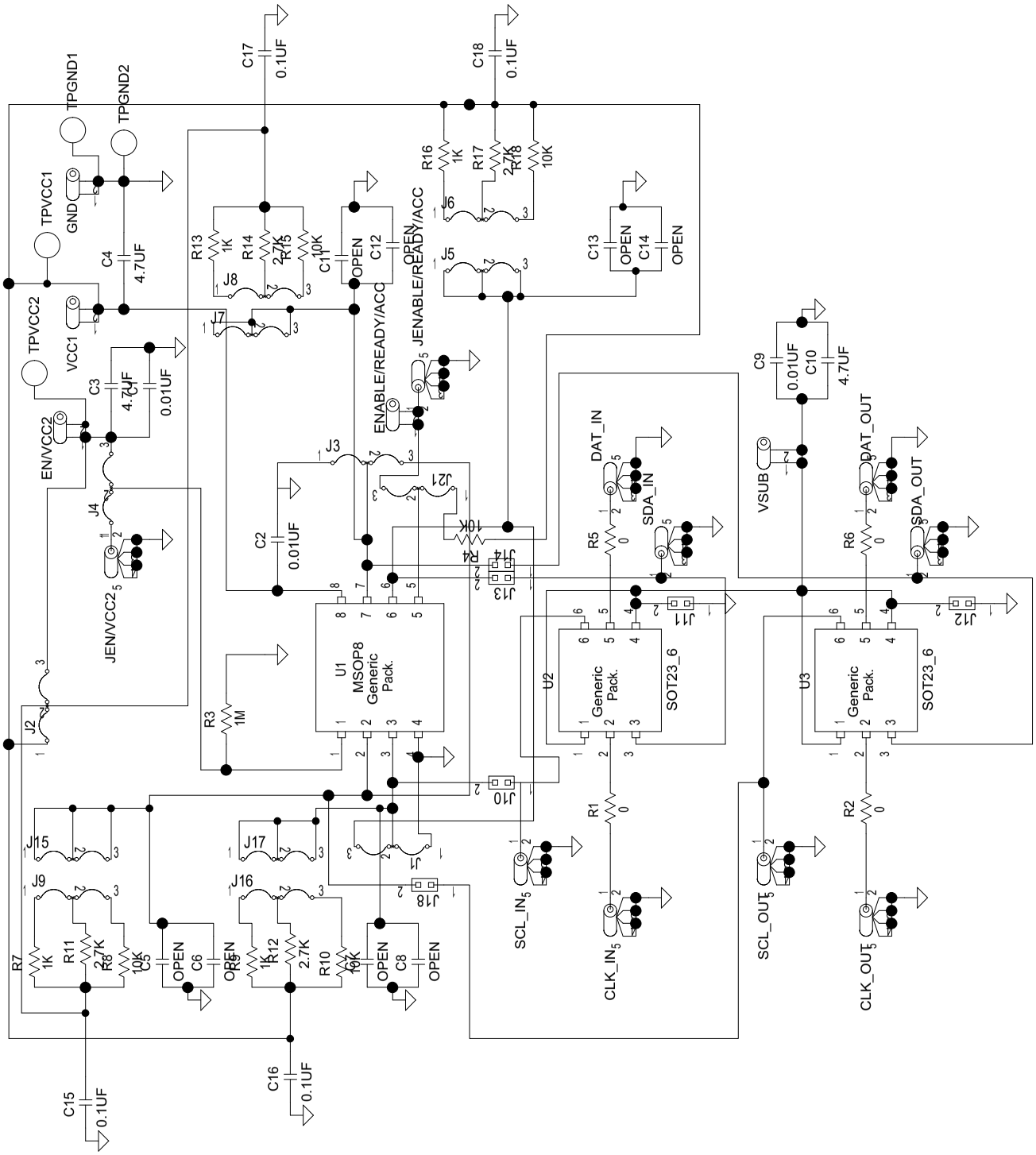
The source of the MOSFETs are connected to GND. through jumpers J11 and J12. The connection to GND can be disconnected by removing these two jumpers. The source potential can then be adjusted by connecting a power supply voltage at the V_{SUB} banana jack connection. This will drive the external input LOW to the buffer with an offset of V_{SUB}. This feature is helpful when evaluating the V_{OS} performance of the I^2C buffers.

Note: When the source voltage is raised above GND, the gate voltage should be compensated to maintain V_{GS} ≥3V. Raising the source potential without changing the gate voltage will provide the gate to the NMOS with less drive and potentially cause the system to operate incorrectly.

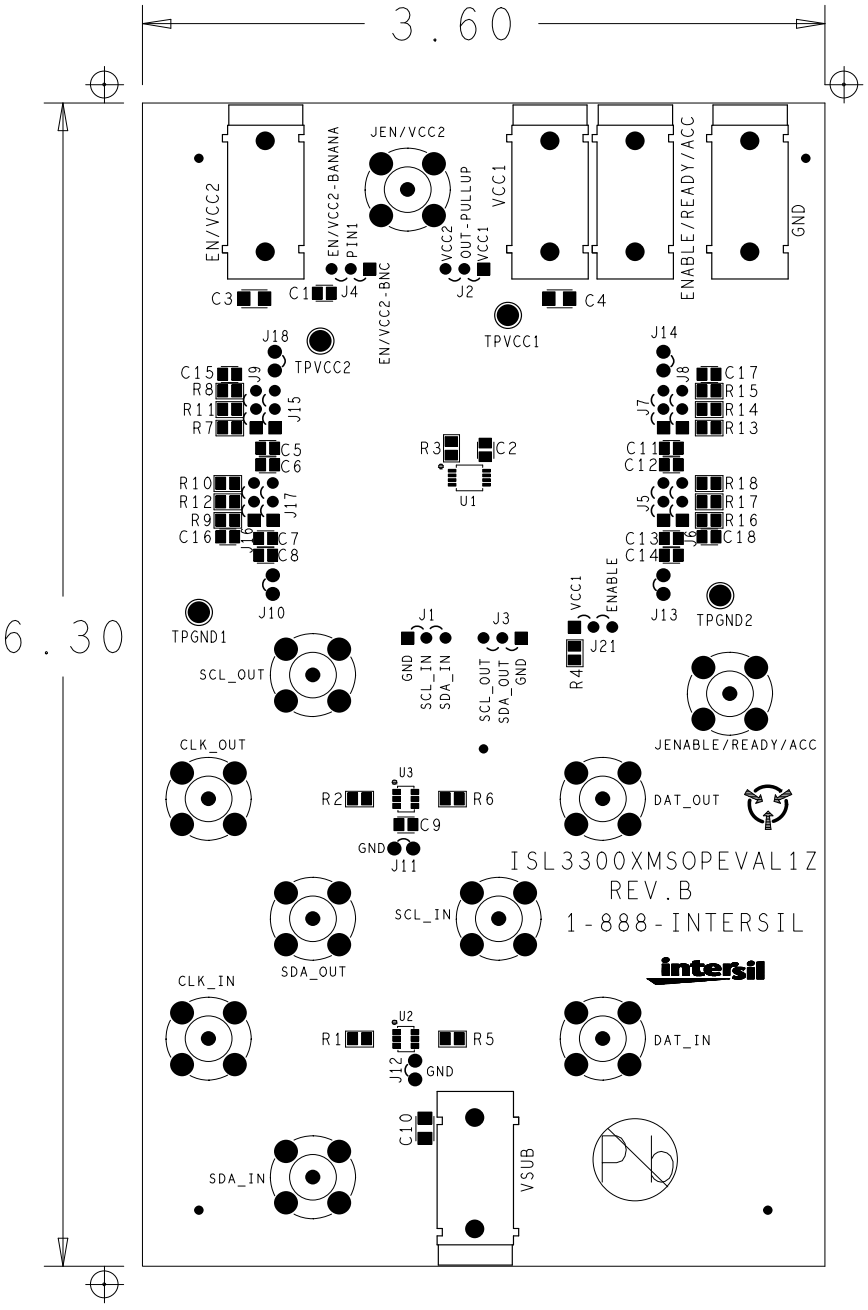
TABLE 2. BOARD COMPONENT DEFINITIONS

DESIGNATOR	DESCRIPTION
U1	ISL33001, ISL33002, or ISL33003 8 Ld MSOP I^2C Buffer IC
V_{CC}	Banana jack connection V_{CC} supply
EN/V_{CC2}	Banana jack connection for EN pin (ISL33001) and V_{CC2} supply pin (ISL33002, ISL33003)
JEN/V_{CC2}	BNC connection for EN pin (ISL33001) and V_{CC2} supply pin (ISL33002, ISL33003)
EN/READY/ACC	Banana jack connection for READY pin (ISL33001), ACC pin (ISL33002) and EN pin (ISL33003)
JEN/READY/ACC	BNC jack connection for READY pin (ISL33001), ACC pin (ISL33002) and EN pin (ISL33003)
SCL_OUT	BNC connection to SCL_OUT pin
CLK_OUT	BNC connection to MOSFET gate for driving SCL_OUT pin
SDA_OUT	BNC connection to SDA_OUT pin
CLK_IN	BNC connection to MOSFET gate for driving SCL_IN pin
SDA_IN	BNC connection to SDA_IN pin
DAT_OUT	BNC connection to MOSFET gate for driving SDA_OUT pin
SCL_IN	BNC connection to SCL_IN pin
DAT_IN	BNC connection to MOSFET gate for driving SDA_IN pin
U2/U3	ROHM SM6K2 4V Drive Nch+Nch MOSFET

Evaluation Board Schematic



Evaluation Board (Top View)



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