Go Configure Development Board R1.0

Development Board for GreenPAK and ForgeFPGA Products

Description

Go Configure™ Development Board provides programming, emulation, and testing functions for the GreenPAK™ and ForgeFPGA™ families of integrated circuits. This development board is intended to work alongside the Go Configure Software Hub.

Specifications

- USB 2.0 interface
- Windows 7/8.1/10/11, macOS (v10.15 or higher) Ubuntu 18.04/20.04/22.04, Debian 11/Testing

Board Contents

- Go Configure Development Board
- USB 2.0 Type-A to Type-C cable
- USB 2.0 Type-C to Type-C cable
- Wall Mount Power Supply

Features

- Read, emulation, and programming functionality
- Three individual programmable power sources with configurable OCP protection
- Flexible power interconnection
- Up to 32 channels Digital Pattern Generator
- Up to 16 channels Analog Waveform Generator

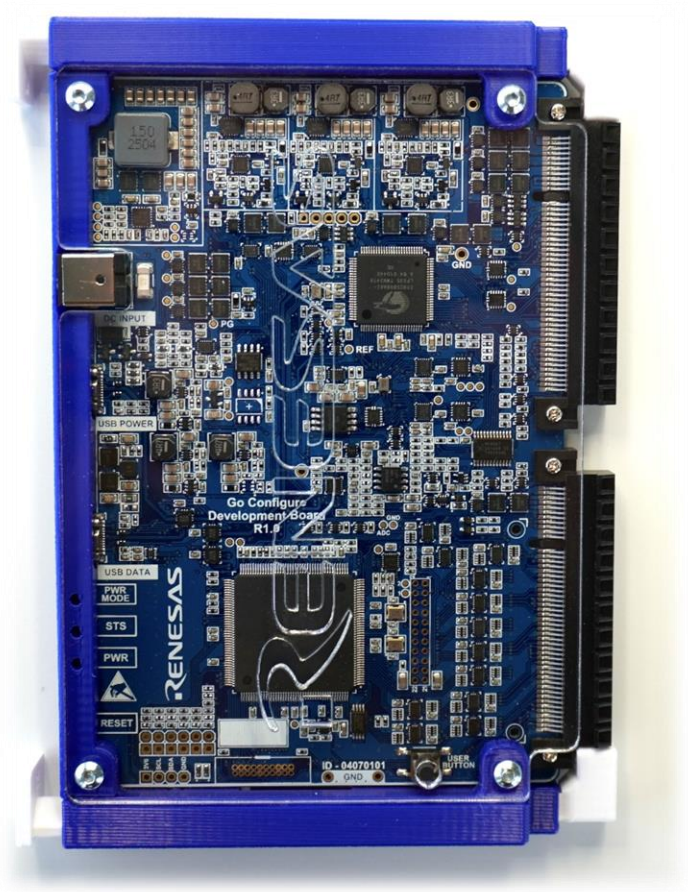

Figure 1. Go Configure Development Board

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1. Overview

The Go Configure Development Board (GCDB) is an updated platform from Renesas. This board is designed for development process for products, such as GreenPAK family mixed-signal ICs and ForgeFPGA programmable arrays. The board is working in combination with the Go Configure Software Hub and provides rich functionality, such as:

- Flexible power management with software-configurable protection (OVP, OCP)
- Three programmable and three fixed power sources
- Digital generators
- Analog generators (AWG)
- Onboard sequencer for Reading, Programming, and Emulating Renesas products
- Up to 80 multi-function configurable IO lines (TP) (availability depends on the connected target board).

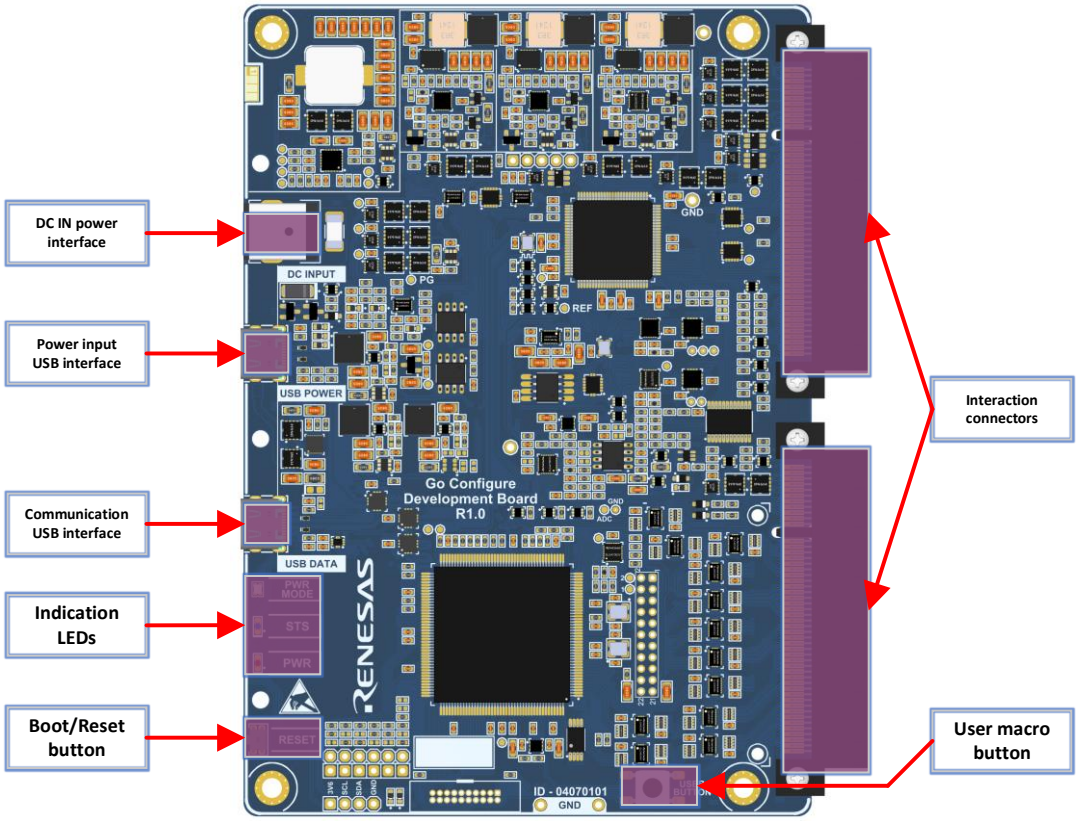


Figure 2. GCDB Main Components

Note 1: The GCDB is designed as the multifunctional Development Tool for Renesas products and not intended for use in the user applications, neither as a separate device nor as a functional part of more complex systems.

Note 2: The GCDB must be used in controlled laboratory conditions (for more information, see Table 11).

The development board interfaces with the target devices through dedicated Interaction Connectors and compatible mating boards, such as the GreenPAK Extension Card (Figure 3) and the ForgeFPGA Socket Card (Figure 4). These connectors expose all onboard signals, communication interfaces, and power lines, enabling seamless access to testing, programming, and debugging.

All devices from the GreenPAK series can be attached to the development board by using a single GreenPAK Extension Card, which is compatible with all existing Socket and DIP Adapters.

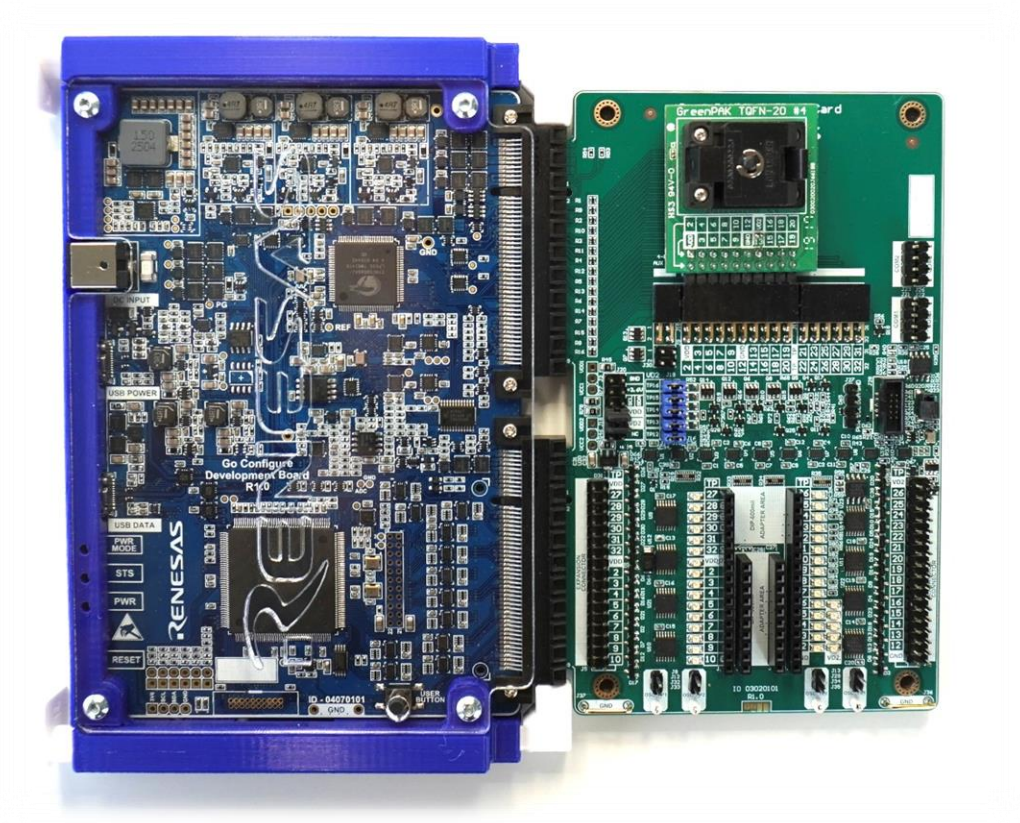


Figure 3. GCDB with GreenPAK Extension Card

The GreenPAK Extension Card supports single and dual V_{DD} products, provides additional functionality, like flexible power selection, extended Socket Adapter area, and prototyping capabilities.

The development of ForgeFPGA products is possible through specialized Socket Cards.

Cards are built for specific parts and packages and provide minimum required set of external components for proper IC configuration and work, as well as some extra features, like power selectors, clocks, IOs exposed to PMOD connectors, and others.

For more information, check documentation for the specific Socket Card.

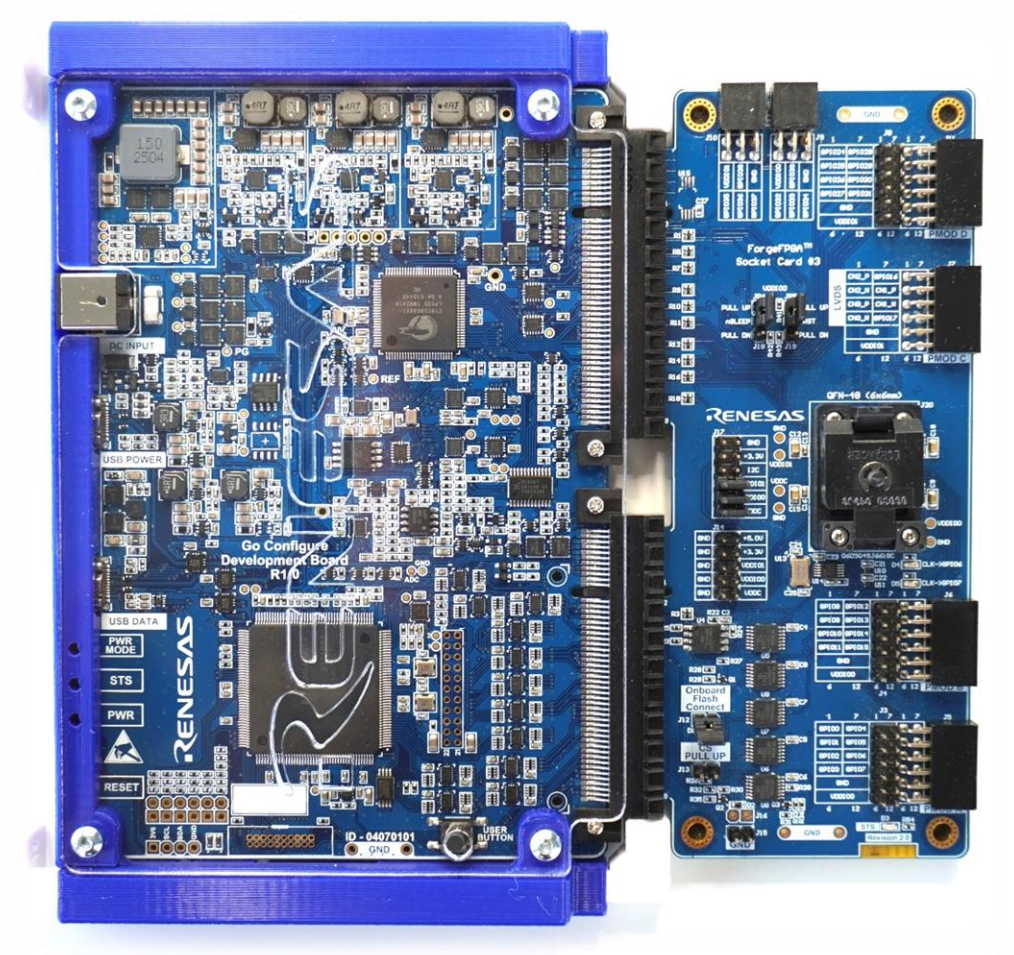


Figure 4. GCDB with Socket Card

Communication with a host PC works through a single USB connection. USB 2.0 Full Speed is supported and sufficient for proper operation of the board.

Although the GCDB remains fully functional with only a single USB DATA connection, it is recommended to use the development board in a combination with an additional USB PD power supply or any compatible power source attached into the DC INPUT connector (see sections 2.2 Power Management and Power Distribution, 3.3 Mixed-Signal Port Connections for more details). Additional power source extends current limits for V_{DD1}, V_{DD2}, V_{DDC} sources and internal 3.3 V, 5 V, 12 V power rails (Note).

Note: Actual for setups with target boards that have internal lines exposed to user connectors.

1.1 Block Scheme

The Go Configure Development Board is designed in a format of a single PCB that virtually can be divided into the following functional blocks (see section 2 Functional Blocks Description for more details):

- User interface
- Power management
- Sequencer for Read, Programming, and Emulation
- Analog generators (AWG)
- Digital generators (Pattern generators).

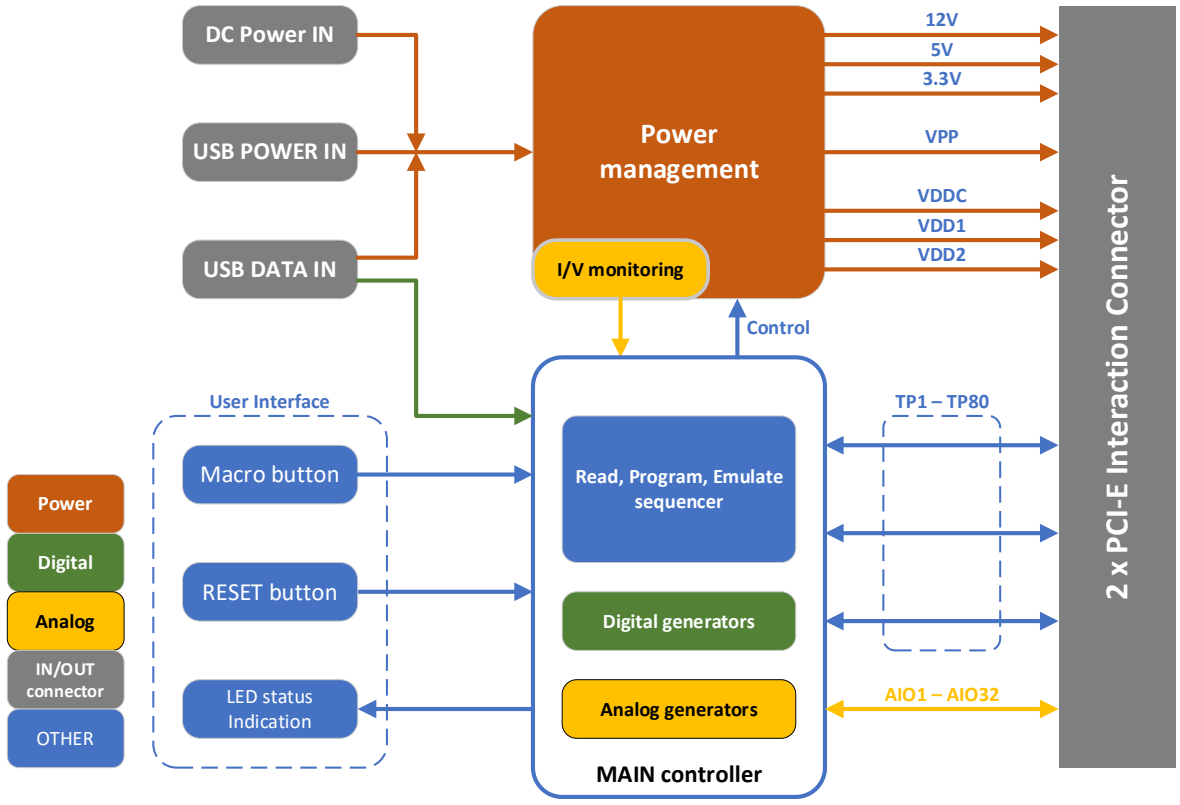
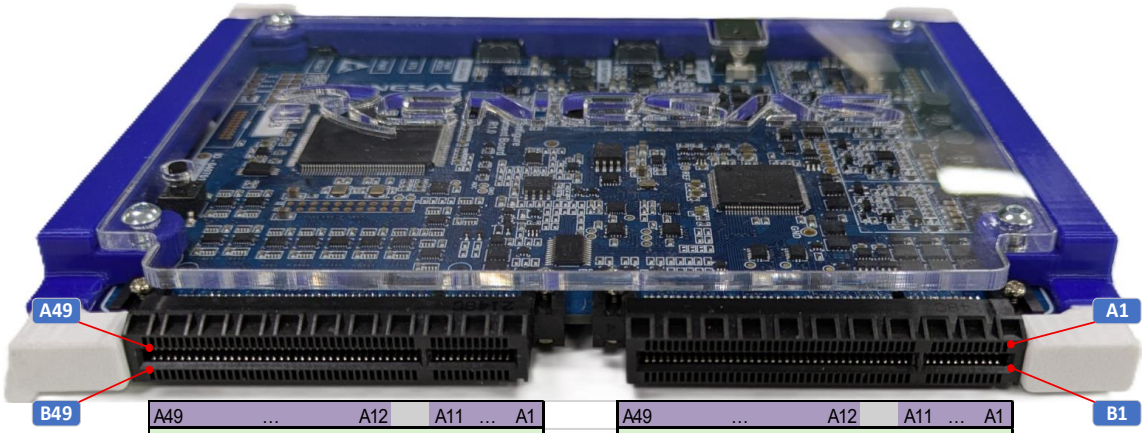


Figure 5. GCDB Simplified Block Scheme

1.2 Interaction Connectors Pinout

As a main communication interface in the GCDB, two Interaction Connectors are used. They contain a set of GPIOs, controlled power lines, service communication lines, and reserved contacts. Figure 6 shows the pinout map for both Interaction Connectors and with the help of colored scheme reflects the correspondence (Note) of GPIO banks to V_{DD1} (light blue) and V_{DD2} (light purple) power sources. See section 2.3 Interaction Connectors GPIOs for more information about GPIOs.

Note: Applicable for setups with dual V_{IO} supply.



	CONNECTOR 2			
Pin name	Pin number		Pin number	Pin name
+12V	A1		B1	+12V
	A2		B2	
RSVR	A3		B3	GND
	A4		B4	
RSVR	A5		B5	
	A6		B6	
RSRV	A7		B7	RSRV
RSRV	A8		B8	RSRV
	A9		B9	
GND	A10		B10	
	A11		B11	GND
RSRV	A12		B12	RSRV
GND	A13		B13	GND
TP21	A14		B14	TP61
TP22	A15		B15	TP62
GND	A16		B16	GND
TP23	A17		B17	TP63
TP24	A18		B18	TP64
GND	A19		B19	GND
TP25	A20		B20	TP65
TP26	A21		B21	TP66
AIO9	A22		B22	AIO25
AIO10	A23		B23	AIO26
TP27	A24	PCB	B24	TP67
TP28	A25		B25	TP68
GND	A26		B26	GND
TP29	A27		B27	TP69
TP30	A28		B28	TP70
GND	A29		B29	GND
TP31	A30		B30	TP71
TP32	A31		B31	TP72
AIO11	A32		B32	AIO27
AIO12	A33		B33	AIO28
TP33	A34		B34	TP73
TP34	A35		B35	TP74
GND	A36		B36	GND
TP35	A37		B37	TP75
TP36	A38		B38	TP76
GND	A39		B39	GND
TP37	A40		B40	TP77
TP38	A41		B41	TP78
AIO13	A42		B42	AIO29
AIO14	A43		B43	AIO30
TP39	A44		B44	TP79
TP40	A45		B45	TP80
GND	A46		B46	GND
AIO15	A47		B47	AIO31
AIO16	A48		B48	AIO32
GND	A49		B49	GND

	CONNECTOR 1			
Pin name	Pin number		Pin number	Pin name
+5V	A1		B1	+5V
	A2		B2	
VDD_C	A3		B3	GND
	A4		B4	
VDD_B	A5		B5	
	A6		B6	
VDD_A	A7		B7	
	A8		B8	
+3V3	A9		B9	
GND	A10		B10	RSRV
	A11		B11	GND
RSRV	A12		B12	RSRV
GND	A13		B13	GND
TP1	A14		B14	TP41
TP2	A15		B15	TP42
VPP	A16		B16	GND
TP3	A17		B17	TP43
TP4	A18		B18	TP44
GND	A19		B19	GND
TP5	A20		B20	TP45
TP6	A21		B21	TP46
AIO1	A22		B22	AIO17
AIO2	A23		B23	AIO18
TP7	A24	PCB	B24	TP47
TP8	A25		B25	TP48
GND	A26		B26	GND
TP9	A27		B27	TP49
TP10	A28		B28	TP50
GND	A29		B29	GND
TP11	A30		B30	TP51
TP12	A31		B31	TP52
AIO3	A32		B32	AIO19
AIO4	A33		B33	AIO20
TP13	A34		B34	TP53
TP14	A35		B35	TP54
GND	A36		B36	GND
TP15	A37		B37	TP55
TP16	A38		B38	TP56
GND	A39		B39	GND
TP17	A40		B40	TP57
TP18	A41		B41	TP58
AIO5	A42		B42	AIO21
AIO6	A43		B43	AIO22
TP19	A44		B44	TP59
TP20	A45		B45	TP60
GND	A46		B46	GND
AIO7	A47		B47	AIO23
AIO8	A48		B48	AIO24
INT	A49		B49	GND

Figure 6. Interaction Connectors Pinout Map

2. Functional Blocks Description

2.1 User Interface

The Go Configure Development Board is intended to be used only with the Go Configure Software Hub. All functions are supported and managed internally and controlled through the standard interface elements in the software.

However, the board contains several onboard interface components that are available for the end user and gives an access to minimum required service functions and simplified board status indication.

The following elements can be considered as the user interface:

- Indication LEDs. Show current board status, available power modes, errors, and active running sequences (Emulation and/or Programming).
- RESET button. Provides a possibility to start a Reset sequence or put the GCDB into a BOOT mode.
- USER button. Macro button with the user-programmable functionality.

2.1.1 Indication LEDs

There are three onboard colored LEDs that indicate current board status:

- PWR MODE (Power mode). Green/orange LED, represents detected power configuration and indicates BOOT mode.
- STS (Status). Blue LED, active during data transfer or during Emulation or Programming sequence.
- PWR (Power indicator). Red LED, indicates possible errors, fails, and other.

Figure 7. LED Indication Block

List of indication modes is given in Table 1.

Table 1. Indication LEDs Status

LED Status	Description
PWR MODE: GREEN **STS:** OFF **PWR:** ON	Normal operation. Board is connected and passed self-tests.
PWR MODE: YELLOW **STS:** OFF **PWR:** ON	Normal operation. Board is connected and passed self-tests. One of the high-power modes is detected and available.

LED Status	Description
PWR MODE: GREEN **STS:** ON, fast blink **PWR:** ON	Normal operation. Procedure of Read, Emulation, or Programming is in active state. Do not disconnect board during this operation.
PWR MODE: GREEN, blink **STS:** - **PWR:** -	BOOT mode. Board is ready for firmware update.
PWR MODE: Yellow, fast blink **STS:** - **PWR:** -	▪ Reverse polarity at DC INPUT is detected, fault mode, non-operational. ▪ Short circuit at DC INPUT is detected, fault mode, non-operational.
PWR MODE: - **STS:** - **PWR:** Slow blink	▪ Error in power configuration during self-test is detected. ▪ Abnormal values at input/output power lines. ▪ Overcurrent condition is detected.

1. "-" equal to either ON or OFF state, depending on other conditions.

2.1.2 USER Button

The USER button is a macro button that can be used for custom features available in the Go Configure Software Hub. Among them are:

- Enabling analog/digital generators
- Starting pre-programmed sequences.

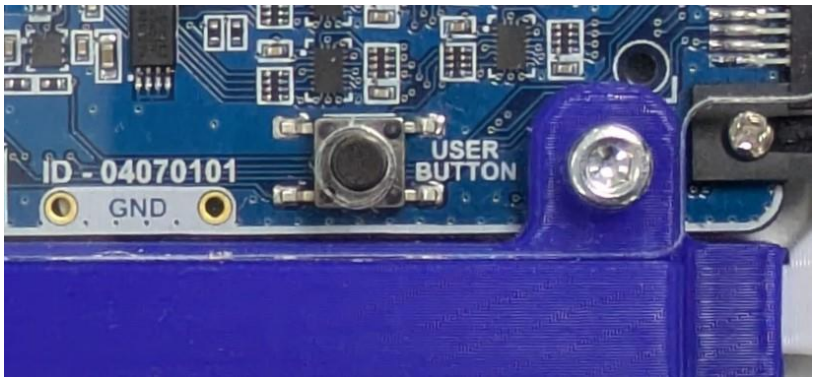


Figure 8. USER Button

2.1.3 RESET Button

The RESET button is available on the side panel of the GCDB, alongside the USB and DC INPUT connectors, and is covered with a flexible plastic fixture to prevent uncontrolled pushes.

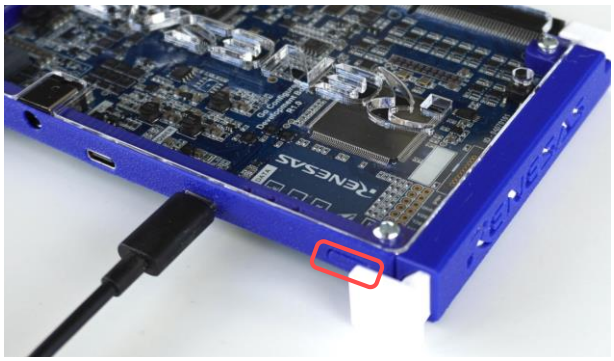


Figure 9. RESET Button

The flowchart of the RESET button algorithm is shown in Figure 10, and the detailed description is given below.

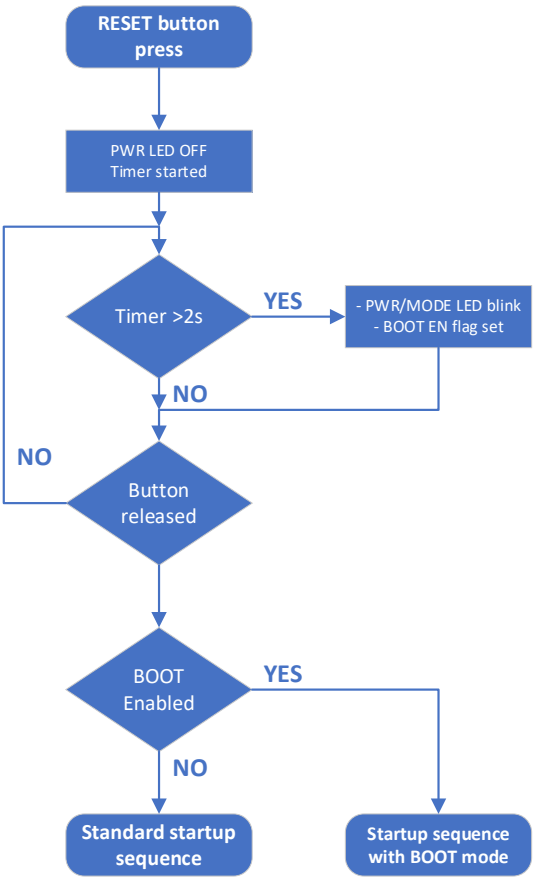


Figure 10. RESET Button Operation Flowchart

RESET is a two-function button, used for cases, when an unexpected and uncontrolled board behavior is met.

Short button press (less than 2 seconds) initiates board reset sequence with complete re-initialization. Sequence stops current work session, clears all the user data, and interrupts Emulation and Programming procedures.

Warning: *If the RESET button is accidently used during the Programming procedure, this action can bring the target OTP device into non-working conditions and lock any further actions with it.*

During normal operation, the GCDB initiates firmware version check each time it is connected to PC, and if necessary, automatically performs the update procedure. However, in some cases, situations that will require update for the GCDB low-level firmware are only possible in the BOOT mode.

Long button press (more than 2 seconds) leads to the reset sequence with an automatic start in a special BOOT mode. After the button is pressed for pre-programmed time, the corresponding indication through the PWR MODE LED will become active (blinking green color), showing that the BOOT mode is selected. After that, the RESET button can be released.

In the BOOT mode, the board is not available for normal operation through the Go Configure Software Hub and can be used only for firmware update.

Warning: *If the RESET button is accidently pressed during firmware update, the development board can be switched to non-working conditions. In the BOOT mode, do not interrupt initiated firmware update procedure and disconnect it from the host PC.*

After firmware update, the board requires manual Reset initiation to exit from the BOOT mode. It is possible either by short press on the RESET button or through changes in power configuration – connecting or disconnecting USB POWER or DC INPUT connectors.

2.2 Power Management and Power Distribution

Internal structure of the GCDB provides the end user with a flexible setup of providing power to V_{DD1}, V_{DD2}, V_{DDC} lines, possibility of interconnecting power lines and using externally supplied voltages.

Figure 11 shows simplified power distribution scheme. It is important to consider the series resistance over the active power path for all the user applications, where high currents are expected during normal operation.

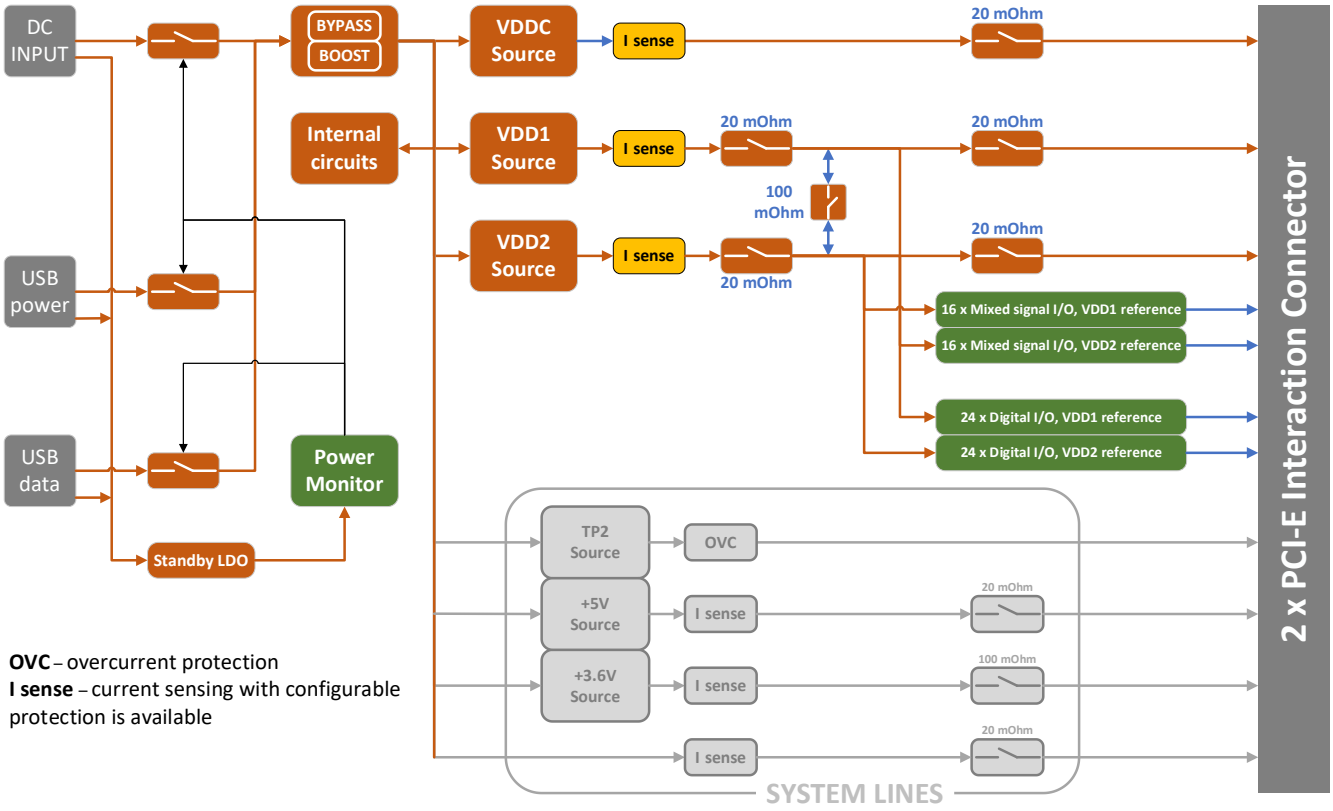
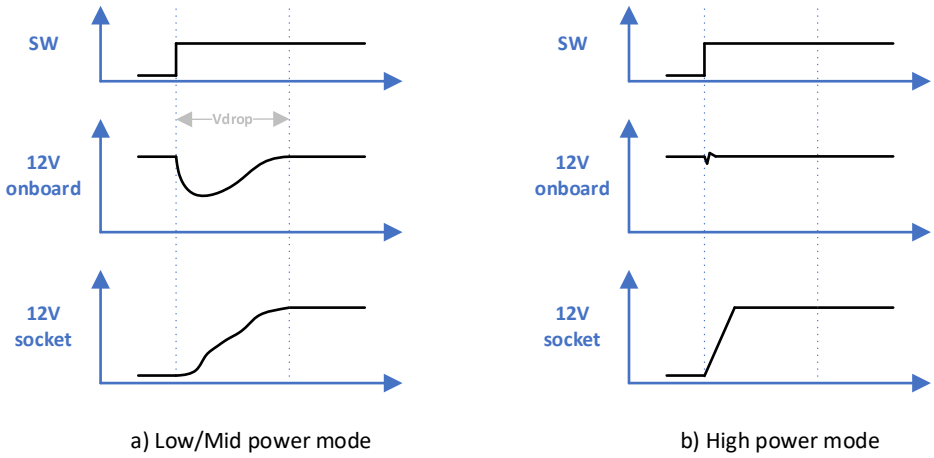


Figure 11. Simplified Power Distribution Diagram

Onboard power sources shown in grayscale are designed for internal usage and may be available on specific Socket Cards or other Extension boards. Check documentation for each mating board for more information.

Note: Because of supporting multiple power sources and operation modes, the GCDB contains inrush current control scheme that implements active input current limiting for input power sources. This adds restrictions to a maximum capacitive load and pulsed current consumption for all power lines exposed to Interaction Connectors, if the GCDB is used with USB DATA connection only.

Exceeding rated values for output capacitance or building setups with high pulse currents (Emulation of HVPAK family products with active V_{DD2}, motor control schemes, and others) may cause unexpected behavior – during Emulation start, possible voltage drops at internal lines (Figure 12, a) that can lead to unstable operation or board reset conditions.



a) Low/Mid power mode b) High power mode

Figure 12. Internal Power Line Sag

To avoid such situations, it is strongly recommended to use a good quality USB PD power source or DC INPUT connection for any applications, where high inrush currents or pulse current consumption are expected. In this case, the onboard power path will automatically switch to a bypass mode, where all current spikes are handled by an external power source (Figure 12, b).

USB adapters with supported 9 V at 2 A, 12 V at 1.5 A, 12 V at 3 A PD profiles are acceptable.

In case if DC INPUT is used – a regulated laboratory power supply with a voltage from 9 V to 14 V (12 V nominal) and rated current ≥ 2 A is acceptable and recommended. Physical interface for DC INPUT is a standard 5.5 mm x 2.0 mm barrel connector with a “+” on central terminal.

Warning: *Correct behavior with USB DATA connection only is not guaranteed if the GCDB is used for work with the FPGA devices and/or any of the Power GreenPAK products.*

2.2.1 Power Modes

The GCDB can work in several configurations (power modes) that are defined by a combination of USB DATA, USB POWER, and DC INPUT connections.

Figure 13 represents power mode selection algorithm during a standard startup sequence. This functionality is automatically managed by an onboard power monitor and applied during the board startup or any reset sequence.

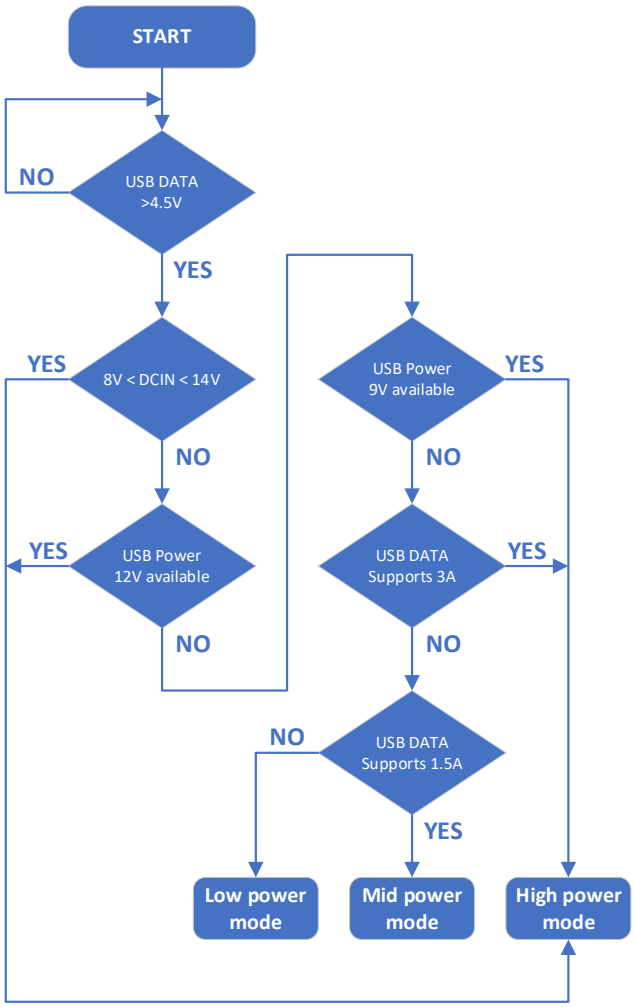


Figure 13. Power Mode Selection Algorithm

Power modes affect current limit per V_{DDx} power source and the ability of connecting additional devices to the GCDB through the Universal Extension Card or Socket Cards (power limitations over the internal lines). For the end user, limits are visible in the **Current Limits** dialog window – corresponding spin-boxes contain pre-defined maximum allowable current per power mode. In High Power mode, this interface allows the user to define custom limits below pre-defined maximum level.

Any change in power configuration (connecting and/or disconnecting cables, removing power from power supply, and others), reset condition caused by the RESET button, or abnormal operation of the GCDB (overcurrent, power fails, and others) leads to an automatic board reset and re-initialization in one of available power modes.

During initialization, the GCDB always selects the highest available power mode and keeps it active during normal operation up to any RESET condition. Detailed description is given below.

Low Power mode is a basic configuration with only USB DATA connection to the host PC. This operation mode is enough for working with all GreenPAK products (Emulation, Programming) and without connecting any extra load to the Extension Card or to PMOD connectors at the Socket Card.

The mode is active if the GCDB is connected through the USB A – USB Type C cable or if the USB Type C – USB Type C cable is used, but the downstream port supports only 500 mA or 1 A current rating.

Current limits in Low Power mode are set to pre-defined minimum values and not accessible through the user interface.

It is not recommended to use the GCDB with any of the FPGA products, while working in Low Power mode. In this mode, software reduces maximum output current on V_{DDx} lines, that may cause unexpected power fails.

Mid Power mode becomes active in two possible scenarios:

1. USB DATA input is connected through the USB Type C – USB Type C cable and the host PC supports 1.5 A current rating on its USB port.
2. USB POWER input is used, and corresponding power supply unit (PSU) is detected with active support of 9 V USB PD Profile.

High Power mode is available in three possible scenarios:

1. USB DATA input is connected through the USB Type C – USB Type C cable and the host PC supports available 3 A current rating on its USB port.
2. USB POWER input is used, and corresponding power supply unit (PSU) is detected with active support of 12 V USB PD Profile.
3. Power source with a voltage within rated specifications is connected to DC INPUT.

Both Mid Power and High Power modes are recommended for work with all supported Renesas FPGA products and all Power GreenPAK ICs.

Note 1: The GCDB provides a possibility to power Power GreenPAK products directly from the onboard power lines, if used in Mid Power and High Power (preferred) modes of operation. However, this functionality is given for test purposes only and available only in setups with specialized Socket Cards with a limited current rating on power lines. For the best user experience, an external power supply should be used if possible. Check documentation for each specific Socket Card for more information.

Note 2: The GCDB firmware calculates current limits according to input power source capabilities. If used power sources are limited in performance or have their parameters different from those listed below, this may lead to an incorrect behavior of active current limits. By default, it is assumed that:

1. USB POWER source with active 9 V USB PD profile is capable of sourcing at least 1 A output current.
2. USB POWER source with active 12 V USB PD profile is capable of sourcing at least 1.25 A output current.
3. When used, DC INPUT power source is capable of sourcing at least 1.5 A output current within rated input voltage range.

2.2.2 V_{DD1}, V_{DD2}, V_{DDC} Sources

The Go Configure Development Board includes three programmable power sources – V_{DDC}, V_{DD1}, V_{DD2}, that provide flexible configuration for prototyping dual supply Renesas products, as well as FPGA with a separate core power input and dual V_{IO} supply configuration.

Each power source consists of a configurable power module with integrated software control and monitoring. During operation, the system automatically applies voltage and current limits based on the active power configuration and the selected target device.

Figure 14 shows a simplified block scheme for all V_{DDC}, V_{DD1}, V_{DD2} sources.

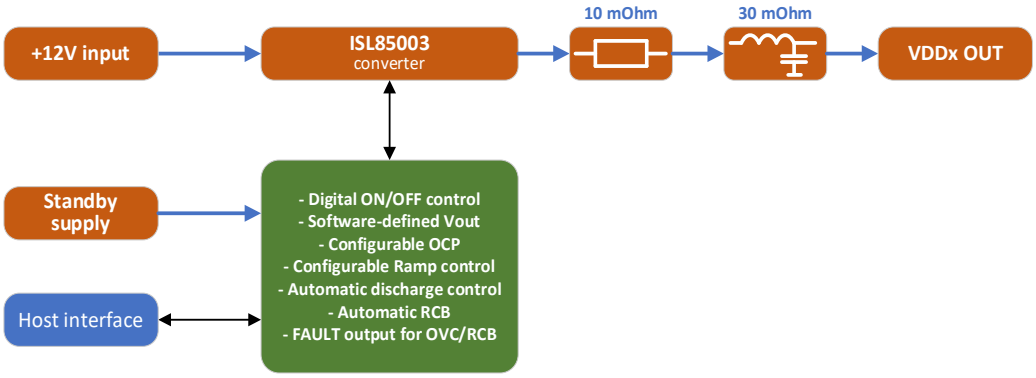


Figure 14. V_{DDC}, V_{DD1}, V_{DD2} Power Supply Structure

Current sensing elements (shunt) and output LC filter define output resistance for each V_{DDx} power source. In combination with interconnection power switches (see section 2.2 Power Management and Power Distribution), it should be considered for the user setups, where high load currents are expected.

Total output resistance from source to Interaction Connectors is expected to be within the range:

- V_{DDC} source: 45-60 mΩ
- V_{DD1} and V_{DD2} source: 65-80 mΩ.

All main electrical parameters (DC + AC) are listed in Table 2.

Ramp mode

All V_{DDx} power sources can work in Normal mode and Ramp mode. In Normal mode, rise time (slew-rate) is fixed at the level of 2 V/ms for all output voltages within rated specifications.

Ramp mode is used to simulate power source with software definable slew-rate, where Ramp-up and Ramp-down time (slew-rate) is user-defined in the range from 2 V/ms (Figure 15, a) to 40 mV/s (Figure 15, b).

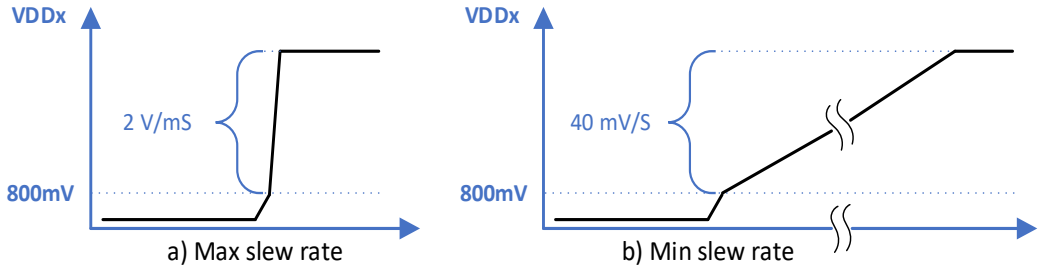


Figure 15. Ramp Mode Variations

If Ramp mode is used, output voltage during ON sequence will automatically reach the target value in two steps:

1. Up to the level of ~800 mV with constant slew-rate of 0.28 V/ms.
2. From the level of ~800 mV and up to the user-defined level with defined slew-rate.

Output voltage during OFF sequence will follow the same steps but in reverse direction:

1. From the user-defined target voltage down to the level of ~800 mV with defined slew-rate.
2. From the level of ~800 mV to 0 mV (if corresponding channel is turned OFF) – exponential fall with 10 Ω discharge resistor.

Overcurrent protection

For safety reasons and to support different modes of operation (power modes) – each V_{DDx} power source includes current sensing circuit with software-defined limits. During normal operation, after reaching limits, an automatic Reset sequence will be initiated with Power Fail indication (see Table 1). In some cases, OCP can lead to a full board Reset with complete re-initialization.

Reverse current blocking

Among other implemented features, all V_{DDx} lines contain Reverse Current Blocking (RCB) option – dedicated circuit detects conditions when negative current is injected into the V_{DDx} channel.

In the case of Reverse Current detection, an automatic power OFF sequence is initialized, and corresponding message will appear in the Go Configure Software Hub.

For most cases, internal logic will correctly manage all power interconnections according to setup defined by the user and abnormal conditions connected with RCB can arise only in some specific situations, for example:

1. The user selects one of the internal V_{DDx} channels as power source and applies to it an external power supply in runtime (Figure 16, a).
2. The user develops a design for dual V_{IO} target device and connects two GPIOs (Output → Input OR Output → Output) from different GPIO banks with different V_{IO} values through a jumper. In this case, the same sequence of turning off power switches will be initialized (Figure 16, b).

Figure 16 shows both cases.

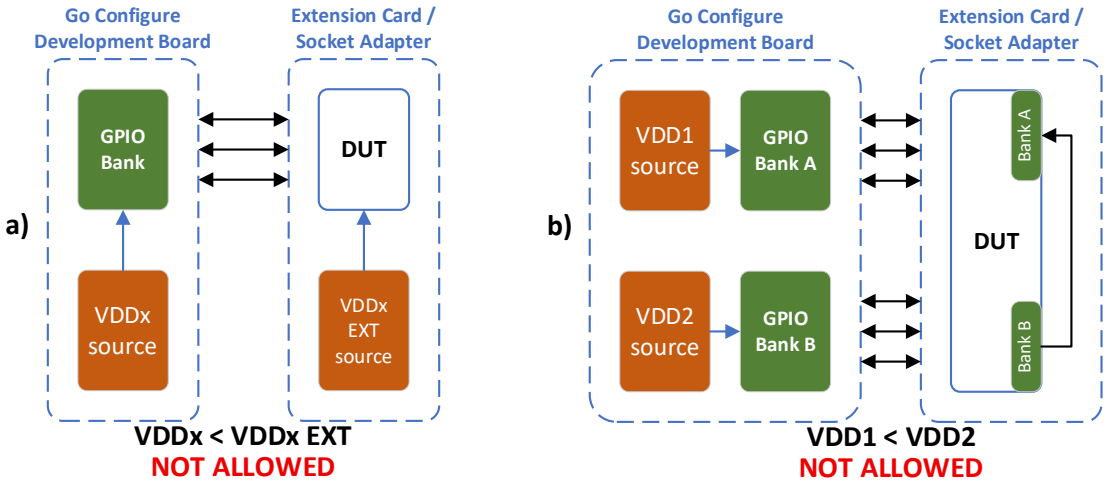


Figure 16. Reverse Current Cases

To avoid any unexpected behavior, the user should carefully define power settings when working with target devices with multiple V_{IO} lines and avoid any changes during operations of chip detection, Emulation and Programming.

During operation, it is not allowed to apply any external power sources to the Socket Adapter or Extension Card, attach or detach jumpers in power lines. All settings related to power configuration should be done before starting the Emulation or Programming procedure.

Table 2. V_{DD1}, V_{DD2}, V_{DDC} Power Sources Parameters

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage (Target Device) [1]	V_{OUT}	I_{OUT} = 100 mA	0.8	-	5.5	V
Output Voltage Regulation Step	V_{STEP}	$V_{OUT(MIN)} \le V_{OUT} \le V_{OUT(MAX)}$	-	10	-	mV
Output Voltage DC Error [1] [2]	ΔV_{OUT}	$I_{OUT} \le I_{OUT(MAX)}$	-1	-	1	%
Output Current	I_{OUT}		0	-	1734	mA
V_{OUT} Slew-Rate	SR	$I_{OUT} \le I_{OUT(MAX)}$	1.8	2	2.2	V/ms
V_{OUT} Slew-Rate	SR_{RM_max}	$I_{OUT} \le I_{OUT(MAX)}$, Ramp mode	2	-	-	V/ms
V_{OUT} Slew-Rate	SR_{RM_min}	$I_{OUT} \le I_{OUT(MAX)}$, Ramp mode	40	-	-	mV/S
Output Capacitance	C_{OUT}		8	10	12	µF
I Meas Resolution	I_{MEAS_VDDx}		-	1	-	mA
I Meas Accuracy			-0.5	-	0.5	%
Discharge Resistance	R_{dsch}		-	10	-	Ω
Discharge Pulse Duration	T_{dsch}		-	50.4	-	ms

1. Measured at Interaction Connector.
2. Measured in High Power mode with certified USB PD power supply.

2.2.3 Internal Power Sources 3.3 V, 5 V, 12 V

The GCDB incorporates three onboard power sources (3.3 V, 5 V, 12 V) that are used for internal circuits and exposed to main Interaction Connectors. Each source contains built-in current monitoring circuits with software-definable limits and controllable switch for external connections. Current limits are automatically applied according to the active input power configuration and not accessible for modifications by the end user.

Availability of 3.3 V, 5 V, 12 V power sources depend on the used target board that is attached to the GCDB. In case if no separate header or jumper selector is available on the target Socket Card or Socket Adapter – lines

remain connected to internal circuits only. Refer to the documentation for the used Socket Adapter or Socket Card for more information.

Warning:

1. *Onboard 12 V line will follow DC INPUT while its value is greater than 11.7 V and stays within rated specifications. The user should consider this fact when working with target boards that have 12 V line exposed to an external connector.*
2. *If the GCDB is used in Low Power mode, do not attach the Extension Card or Socket Adapters with capacitive load outside the specified range. Refer to section 2.2 Power Management and Power Distribution for more information.*

Table 3. Onboard +5 V Power Supply Parameters

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage [1]	V_{OUT_5V}	I_{OUT} = 100 mA	5.05	5.1	5.15	V
Maximum Output Current	I_{OUT_5V}		0	-	96	mA
V_{OUT} Slew-Rate	SR_{5V}	I_{OUT} = 100 mA	1.8	2	2.2	V/ms
Output Capacitance	C_{OUT_5V}		-	44	-	µF
Load Capacitance	C_{LOAD_5V}		0	-	22	µF
Output Ripple [1]	V_{RIPPLE_5V}	I_{OUT} = 100 mA	-	10	-	mV_{p-p}
I Meas Resolution	I_{MEAS_5V}		-	1	-	mA

1. Measured at Interaction Connector.

Table 4. Onboard +3.4 V Power Supply Parameters

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage [1]	$V_{OUT\_3.3V}$	I_{OUT} = 100 mA	3.4	3.42	3.45	V
Maximum Output Current	$I_{OUT\_3.3V}$		0	-	96	mA
V_{OUT} Slew-Rate	$SR\_{3.3V}$	I_{OUT} = 100 mA	1.8	2	2.2	V/ms
Output Capacitance	$C_{OUT\_3.3V}$		-	44	-	µF
Load Capacitance	$C_{LOAD\_3.3V}$		0	-	22	µF
Output Ripple [1]	$V_{RIPPLE\_3.3V}$	I_{OUT} = 100 mA	-	12	-	mV_{p-p}
I Meas Resolution	$I_{MEAS\_3.3V}$		-	1	-	mA

1. Measured at Interaction Connector.

Table 5. Onboard +12 V Power Supply Parameters

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage [1] [2]	V_{OUT_12V}	I_{OUT} = 100 mA	11.5	11.7	14	V
Maximum Output Current	I_{OUT_12V}		0	-	96	mA
V_{OUT} Slew-Rate	SR_{12V}	I_{OUT} = 100 mA	1.8	2	2.2	V/ms
Output Capacitance	C_{OUT_12V}		-	22	-	µF
Load Capacitance	C_{LOAD_12V}		0	-	22	µF
Output Ripple [1] [2]	V_{RIPPLE_12V}	I_{OUT} = 100 mA	-	22	-	mV_{p-p}
I Meas Resolution	I_{MEAS_12V}		-	1	-	mA

1. Measured at Interaction Connector.
2. Output ripple voltage is defined by DC INPUT power source parameters, while its value stays within the range of +11.8 V to +14 V.

2.3 Interaction Connectors GPIOs

For work with the target device, two Interaction Connectors are used as a single physical interface. Their pins are divided into several groups:

Power management – all configurable power sources (V_{DD1}, V_{DD2}, V_{DDC}) are exposed to Interaction Connectors and used for powering the target device or as a power path for setups with external power supplies. Internal service lines like +5 V or +12 V are present at Interaction Connectors but normally are not available for the end user, except for application-specific Socket Cards designed for the GreenPAK devices (for example, HVPAK, Power GreenPAK, and others). Refer to the documentation for the used Socket Card or Extension Card for more information.

GPIOs – all digital and analog Inputs/Outputs that are available in the GCDB:

- TP1 to TP16 – multifunctional mixed-signal GPIOs with ADC functionality and configurable port structures. By default, the group refers to V_{DD1} power source.
- TP41 to TP56 – multifunctional mixed-signal GPIOs with ADC functionality and configurable port structures. By default, the group refers to V_{DD2} power source.
- TP17 to TP40 – multifunctional digital IO pins with configurable input/output ports and selectable pull-up or pull-down resistors. By default, the group refers to V_{DD1} power source.
- TP57 to TP80 – multifunctional digital IO pins with configurable input/output ports and selectable pull-up or pull-down resistors. By default, the group refers to V_{DD2} power source.

Analog IOs – pins with available analog functions, like ADC and DAC:

- AIO1 to AIO8, AIO17 to AIO24 – Analog Output pins with DAC functionality. All pins within the group have an option of Analog Generators. See section 2.6 Analog Generators, Table 8, and Table 9 for more details.
- AIO9 to AIO16, AIO25 to AIO32 – Analog Inputs with ADC functionality.

Service IOs – special pins intended for internal usage only and marked RSRV in Figure 6. These pins are not available for the end user.

2.4 Read, Programming, Emulation Sequencer

Read, Programming, Emulation sequencer is a virtual module that is used for work with all supported mixed-signal products of Renesas in Emulation or Programming modes. It contains two groups of mixed-signal configurable GPIOs with rich analog and digital functions. All GPIOs are divided into groups and refer to a separate V_{DDx} power source:

- TP1-TP16 refer to V_{DD1} source
- TP41-TP56 refer to V_{DD2} source.

For single supply devices, all GPIOs can be connected to either V_{DD1} or V_{DD2} line, according to the user's setup.

Work with a module is supported through target boards connected to Interaction Connectors. For example, the GreenPAK Extension Card in a combination with the Socket Adapter.

The port structure of each individual IO within the module is shown in Figure 17. Electrical parameters are listed in Table 6.

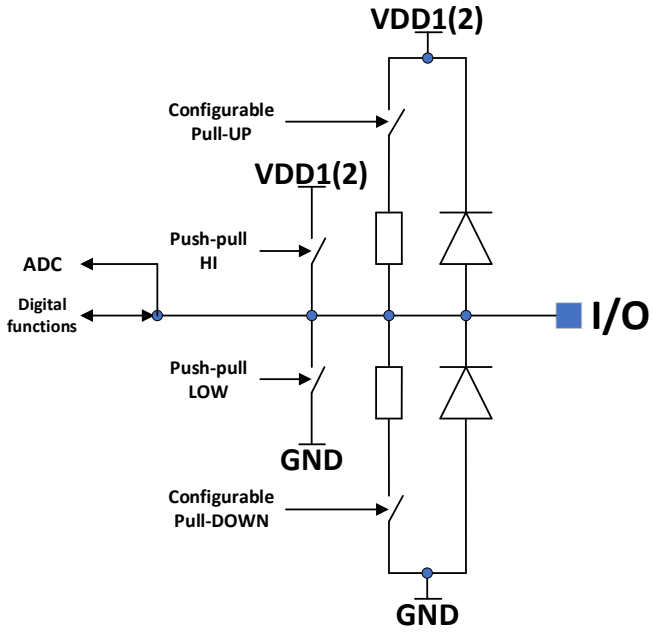


Figure 17. Mixed-Signal IO Structure

Table 6. GPIO Electrical Parameters, GreenPAK Programming Module

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
GPIO Banks Voltage Supply	V_{DDIO}	V_{DD1}, V_{DD2}	1.71	-	5.5	V
Output Voltage Level Range	V_O	I_{OH}, I_{OL} = 0 mA	0	-	V_{DDIO}	V
HIGH-level Output Voltage	V_{OH}	I_{OH} = 4 mA, V_{DDIO} = 3.3 V	V_{ddIO} – 0.6	-	-	V
		I_{OH} = 1 mA, V_{DDIO} = 1.8 V	V_{ddIO} – 0.5	-	-	V
LOW-level Output Voltage	V_{OL}	I_{OH} = 8 mA, V_{DDIO} = 3.3 V	-	-	0.6	V
		I_{OH} = 4 mA, V_{DDIO} = 3.3 V	-	-	0.4	V
		I_{OH} = 1 mA, V_{DDIO} = 1.8 V	-	-	0.6	V
HIGH-level Output Current	I_{OH}	V_{OL} = 2.4 V, Strong-LOW setup	11.5	24	-	mA
LOW-level Output Current	I_{OL}	V_{OL} = 0.4 V, Strong-LOW setup	9.75	16.5	-12	mA
Input Voltage Level Range	V_I		0	-	V_{DD}	V
Input Voltage Level Range (ABS Max)	$V_{I\,max}$	V_{DD} = V_{DD1} or V_{DD2}	-0.5 V	-	V_{DD}+ 0.5V	V
HIGH-level Input Voltage	V_{IH}		0.7 x V_{DD}	-	-	V
LOW-level Input Voltage	V_{IL}		-	-	0.3 x V_{DD}	V
Schmitt Trigger Input Hysteresis	V_{HYS}		0.29	0.62	0.94	V
Input Leakage Current	I_{LKG}		-	-	2	nA
Pull-Up, Pull-Down Resistor	R_{PU}/R_{PD}	Digital IN setup	3.5	5.6	8.5	kΩ
Input Capacitance	C_{IN}		-	17	-	pF

1. V_{DD1} = 1.71 V to 5.5 V, V_{DD2} = 1.71 V to 5.5 V, T_A = 25 °C, unless otherwise noted.

2.5 ForgeFPGA Programmer

ForgeFPGA Programmer is a virtual module inside the GCDB that provides a functionality of emulating FPGA products and programming their OTP memory, as well as programming onboard FLASH memory.

Work with the target device is supported through Socket Cards, compatible with specific parts or packages. Check the documentation for the used Socket Card for more information about pin mapping and available onboard resources.

Communication between the GCDB and target Socket Cards is possible through 48 multifunctional configurable Digital GPIOs (see section 2.3 Interaction Connectors GPIOs for more information) divided into two banks:

- TP17-TP40 refer to V_{DD1} voltage
- TP57-TP80 refer to V_{DD2} voltage.

The GCDB supports both configurations, with internal and external power supply connections. If the user selects an option of external power source, onboard power supplies (V_{DDC}, V_{DD1}, V_{DD2} lines) will become disconnected and the power management scheme will automatically follow the external power source value.

Note: The user is responsible for not exceeding absolute maximum ratings for the target device in setups, where an external power source is used. Internal protection circuits implemented in the GCDB will disconnect onboard power lines when reaching maximum values, but DUT and communication lines may still be damaged.

Table 7. GPIO Electrical Parameters, ForgeFPGA Programming Module

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage Level Range	V_O	I_{OH} = I_{OL} = 0 mA	0	-	V_{DD}	V
HIGH-level Output Voltage	V_{OH}	I_{OH} = 3 mA, Strong-HI setup	2.87	3.21	-	V
LOW-level Output Voltage	V_{OL}	I_{OL} = 3 mA, Strong-LOW setup	-	0.06	0.11	V
HIGH-level Output Current	I_{OH}	V_{OL} = 2.4 V, Strong-HI setup	11.5	24	-	mA
LOW-level Output Current	I_{OL}	V_{OL} = 0.4 V, Strong-LOW setup	9.75	16.5	-12	mA
Input Voltage Level Range	V_I		0	-	V_{DD}	V
Input Voltage Level Range (ABS Max)	$V_{I\,max}$		-0.5 V	-	V_{DD}+ 0.5 V	V
HIGH-level Input Voltage	V_{IH}		0.7 x V_{DD}	-	-	V
LOW-level Input Voltage	V_{IL}		-	-	0.3 x V_{DD}	V
Schmitt Trigger Input Hysteresis	V_{HYS}		0.29	0.62	0.94	V
Input Leakage Current	I_{LKG}		-	2	2000	nA
Pull-Up, Pull-Down Resistor	R_{PU}/R_{PD}	Digital IN setup	-	4.7	-	kΩ
Input Capacitance	C_{IN}		-	20	-	pF

1. V_{DD1} = 1.71 V to 3.45 V, V_{DD2} = 1.71 V to 3.45 V, T_A = 25 °C, unless otherwise noted.

2.6 Analog Generators

The GCDB has 16 built-in Analog Waveform Generator (AWG) channels. On the Interaction Connectors pin map, (Figure 6) the Analog Waveform Generators are shown as AIO1-AIO8 and AIO17-AIO24.

Analog generators are driven by onboard DA/AD converters and their states on all channels are simultaneously updated at the speed of 10 kS/s. The waveform of each channel is defined as a set of “points”. Each single “point” contains the channel state configuration (Hi-Z state, zero voltage, voltage level, and either add or subtract the voltage level from the current one) and its time that defines the number of consecutive samples for which this point is applied (in the range from 1 to 65535 samples) every 100 µs. A single channel can have up to 60 points, each with the available point time range, meaning that the duration of a single waveform can vary from 100 µs to up to 6.553 s.

Each AWG channel can be controlled independently (start, pause, and stop operations) and each supports the repeating function for the waveform (up to 255 repetitions or repeats until a stop command is received). Before the repeating waveform begins, it is possible to define initial state for the selected channel (pre-start state),

which is applied before the start of the points sequence and is not included in the regular, repeated part of the waveform, as shown in Figure 18.

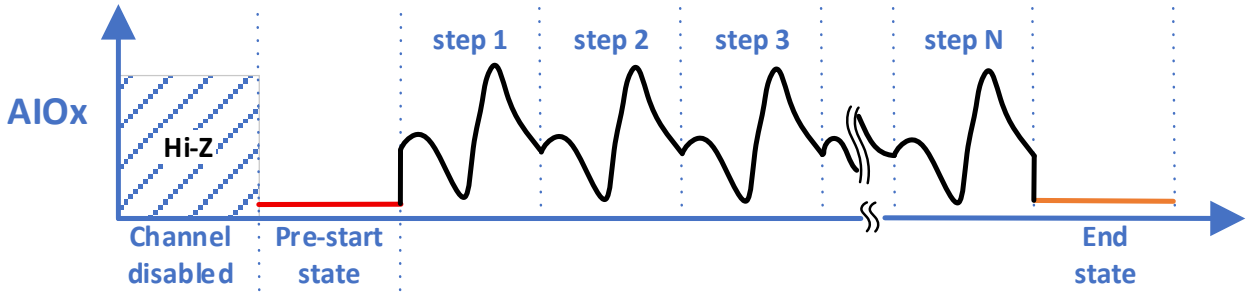


Figure 18. Analog Waveform Generator Cycle

The states of the analog waveform channels are configurable before the pattern generation starts (pre-start state), during the pause (pause state), and after the generation is complete (end state). Available options and other Analog Waveform Generator parameters can be found in Table 8.

Table 8. Analog Waveform Generator Specifications

Parameter	Description
Sample Rate	10 kS/s
Number of channels	16
Number of points	60
Minimum point duration	100 µs
Maximum point duration	3.276 s
Features	Configurable constant voltage source, pre-start waveform, regular (repeated) waveform, configurable pre-start, pause, end states
Repeat Functions	One-shot, Cyclic
Repeat Count	1-255 (repeats until stop if counter set to 0)
Output Type	Rail-to-Rail
Pre-start state options	Hi-Z, zero voltage, first point state
Pause state options	Hi-Z, zero voltage, first point state, keep last state
End state options	First point state, keep last state
Waveform type	Arbitrary

Analog Waveform Generator DC and AC characteristics are described in Table 9.

Table 9. Analog Waveform Generator Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage Range [1]	V_{OUT}		0	-	5500	mV
Output Voltage Resolution	1 LSB	10 mV ≤ V_{OUT} ≤ 5540 mV	-	1.354	-	mV
Output Voltage Accuracy	ΔV_{OUT}	10 mV ≤ V_{OUT} ≤ 5540 mV	-2.708	-	2.708	mV
Zero Code Error			-	0.65	2	mV
Settling Time	T_{settle}	From 25 % to 75 % full scale with 1LSB accuracy	-	6	-	µs
Slew-Rate			-	1.25	-	V/µs

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Impedance	Z_O		-	25 [1]	-	Ω
Output Resistive Load [1]	R_{L_RES}	Within 10 % to 90 % full scale	1	-	-	kΩ
Output Capacitive Load [1]	R_{L_CAP}	R_{L_RES} = ∞	-	-	2	nF
		R_{L_RES} = 1 kΩ	-	-	10	nF
Short-Circuit Current [1]			-	-	25	mA
Off State Leakage Current	I_{LKG}		-	1	-	µA

1. Defined by DAC internal structure, not limited inside the GCDB. Exceeding maximum values may damage the board.

2.7 Digital Generators

The GCDB has a built-in Digital Generator module with 32 independent channels that are mapped to TP1-TP16 and TP41-TP56 pins on Interaction Connectors.

All channels can generate logic patterns – set of “points”, where each point represents a combination of pin state and its duration in time (number of minimum time steps) per defined state. Generated patterns share the same global start point, are synchronized in time and updated with a resolution of 100 µs (10 kS/s).

The way how the pattern is generated is similar to AWG (see section 2.6 Analog Generators) but with a possible number of points equal to 181.

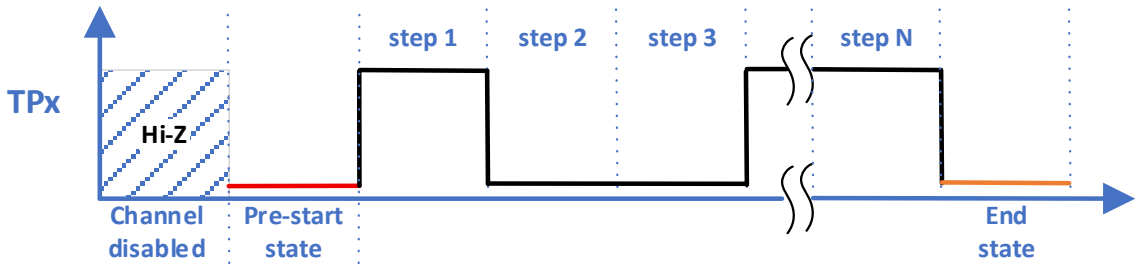


Figure 19. Digital Waveform Generator Cycle

All main parameters of the Digital Generator module are listed in Table 10.

Table 10. Digital Generator Specifications

Parameter	Description
Number of channels	32
Sample Rate	10 kS/s
Number of points	181
Minimum point duration	100 µs
Maximum point duration	3.276 s
Repeat Functions	One-shot, Cyclic
Repeat Count	1-255 (repeats until stop if counter set to 0)
Output Type	Push-pull, Hi-Z, Open-drain NMOS, Open-drain PMOS, Pull-up, Pull-down
Pre-start state options	Hi-Z, zero voltage, first point state
Pause state options	Hi-Z, zero voltage, first point state, keep last state
End state options	First point state, keep last state

3. Schematic Circuits

Note: All schematic circuits in this section are for information purposes only. Refer to official web resources for more information about all pointed components (Datasheets, Evaluation Boards, Reference Designs, and others).

This section shows schematic diagrams with detailed description for some of the GCDB functional blocks that are available to the end user.

3.1 V_{DDC}, V_{DD1}, V_{DD2} Power Sources

All three onboard power sources are built around the ISL85003AFRZ – Renesas synchronous buck converter. As control and monitoring unit used the SLG47003V – configurable mixed-signal IC from the GreenPAK family. Its internal analog and digital modules provide rich functionality for controlling external power converters. The overall scheme for V_{DDC}, V_{DD1}, V_{DD2} power converters is shown in Figure 20.

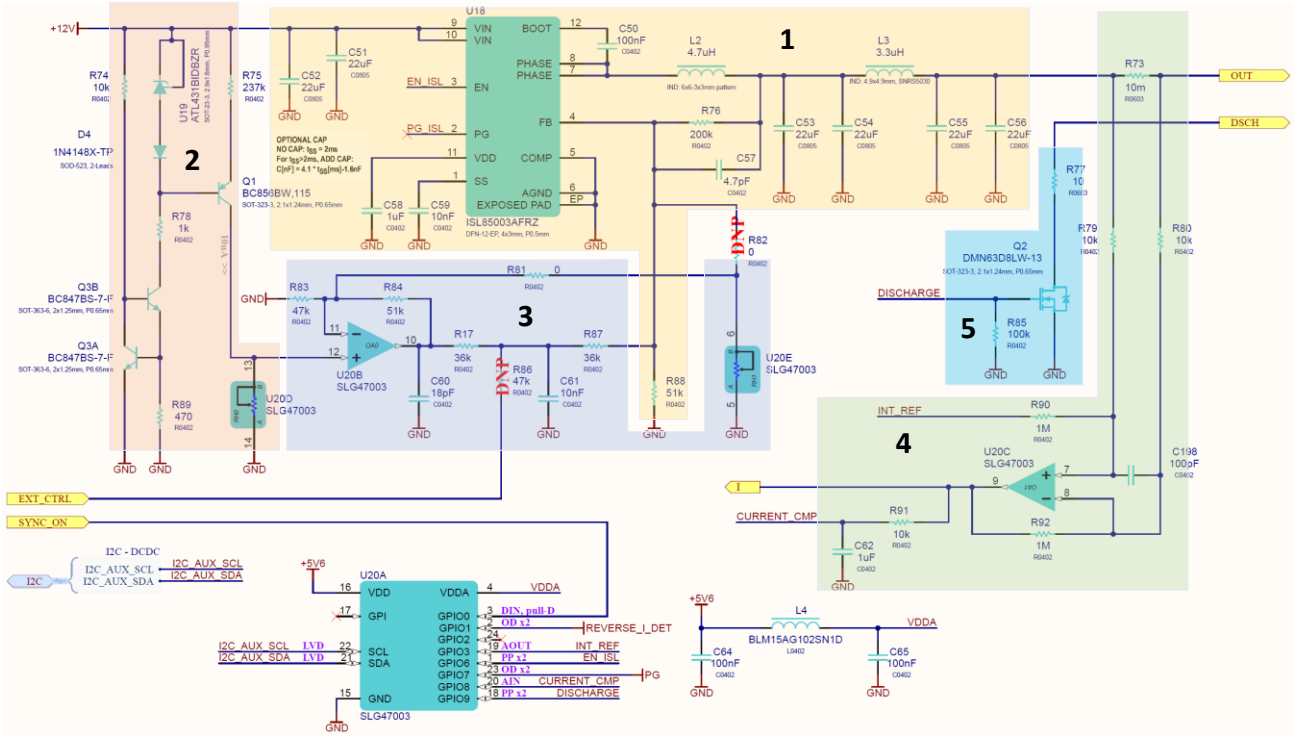


Figure 20. V_{DDC}, V_{DD1}, V_{DD2} Power Source Scheme

The main functional blocks are:

1. Synchronous buck converter with output LC filter.
2. Software-controlled voltage source (DAC) built around Digital Rheostat module inside the SLG47003V and constant current source.
3. Feedback control. Matching circuit between DAC and feedback of the ISL85003AFRZ. Used for setting output voltage and factory calibration process. Based on the SLG47003V OpAmp and Rheostat modules.
4. Differential amplifier with programmable offset for current measurement, OCP, RCB. Based on the SLG47003V OpAmp module.
5. Discharge circuit.

Warning: *In provided design, the SLG47003V is powered close to its maximum allowable V_{IN} range and beyond the recommended operation conditions. Do not use the shown example as any kind of reference for new designs. Refer to the official documentation for more information: SLG47003V.*

3.2 Power Switches

In total the GCDB contains 13 bidirectional power switches, based on a combination of the SLG55021-200010V gate driver and two MOSFETs with a common-source connection, see section 2.2 Power Management and Power Distribution for more details.

The SLG55021-200010V is a standalone, cost-effective gate driver from Renesas. With a help of additional independent supply source, it allows simple implementation of a “floating” MOSFET connection for realization of power commutation blocks with a possibility of disconnecting the load without any possible reverse current issues.

Another useful feature of the SLG55021-200010V is dual control inputs with logic “AND” behavior. It allows to build power distribution schemes with independent OFF signal that overrides input control.

All power switches share the same schematic (Figure 21) but differ in discrete components (MOSFETs) used to match the output requirements:

1. Blocks used for main power lines commutation, like V_{DDx} or internal service power lines, utilize parts with ~8 mΩ (or better) static ON resistance. Total output resistance per switch, including thermal derating, is expected to be within the range of ~20 mΩ maximum.
2. All auxiliary power lines or lines where voltage drop across the switch is not critical utilize parts with ~35 mΩ (or better) static ON resistance. Total output resistance per switch, including thermal derating, is expected to be within the range of ~100 mΩ maximum.

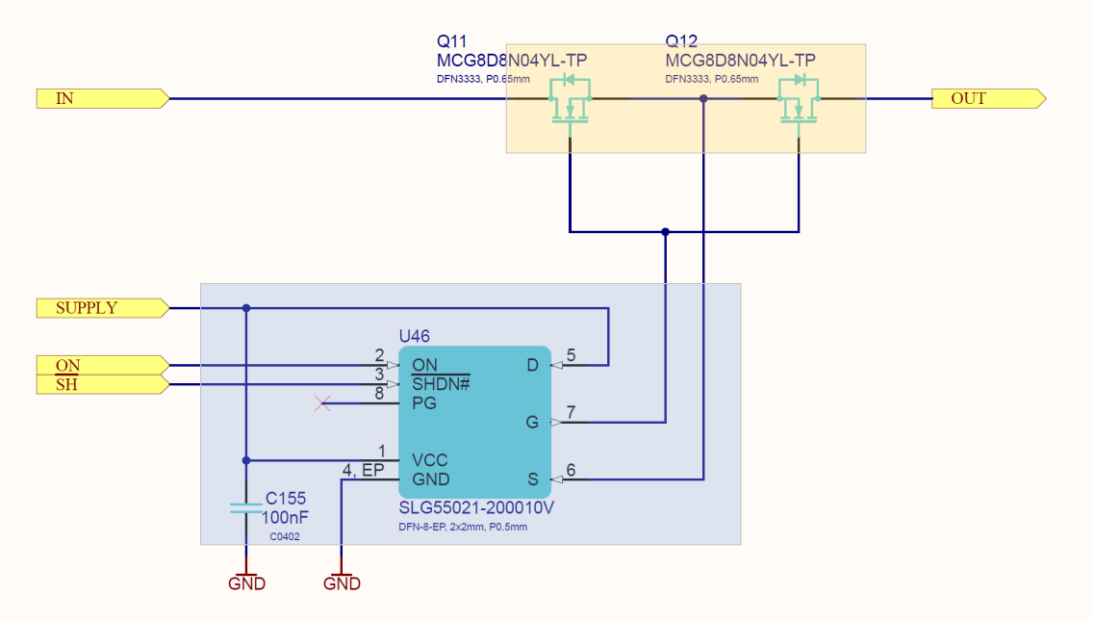


Figure 21. Power Switch Schematic Diagram

Note: According to the documentation, in standard configuration, input pin D (№ 5) of the SLG55021-200010 should be connected to Drain terminal of the controlled MOSFET. In designs where a separate power supply is available and connected to pin D, it should be turned on before applying any voltage to Drain terminal of the controlled MOSFET. Refer to the official documentation for more information: SLG55021-200010V.

3.3 Mixed-Signal Port Connections

As a component for work with mixed-signal target devices, like the GreenPAK ICs, the CY8C5868AXI-LP035 MCU is used.

All TPs are divided into two banks are powered from V_{DD1} and V_{DD2} power sources and directly exposed to Interaction Connectors. Figure 22 shows the correspondence between this MCU and Interaction Connectors pinouts. Internal structure of all IOs and other information are described in sections 2.3 Interaction Connectors GPIOs and 2.4 Read, Programming, Emulation Sequencer.

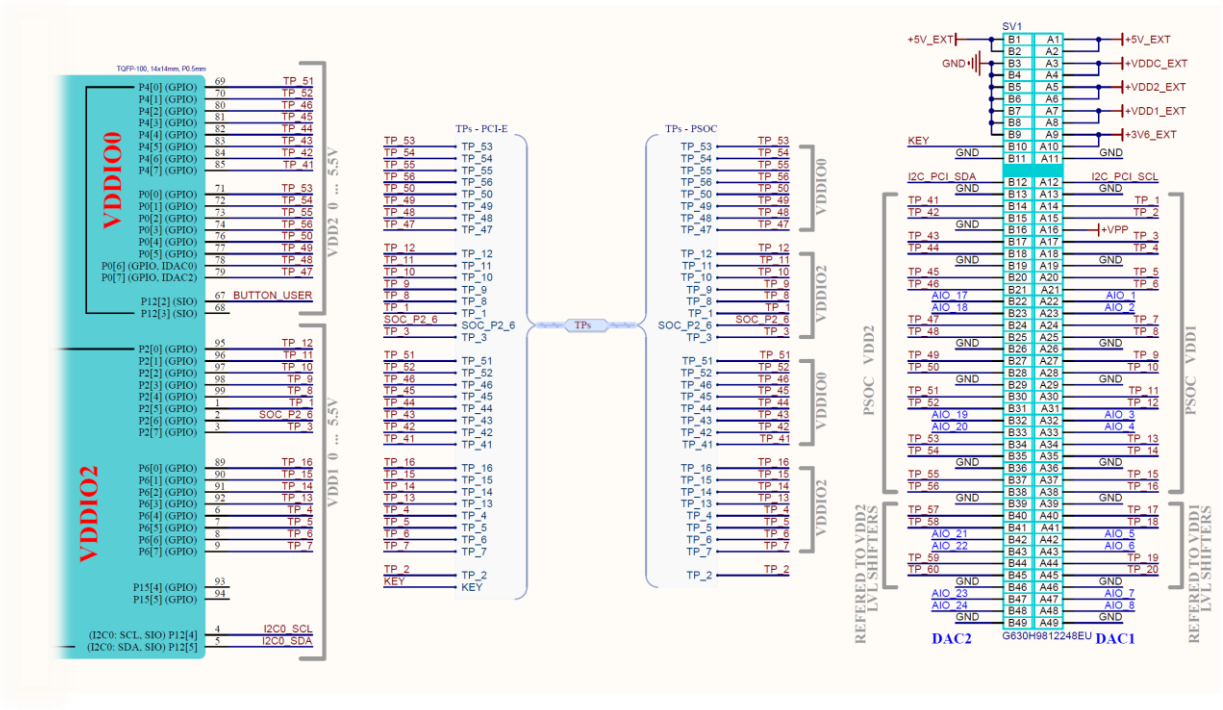


Figure 22. Simplified Representation of Mixed-Signal Test Points Connection

Power input pins related to IO banks with TPs are connected to V_{DD1} and V_{DD2} power sources through the software-controlled communication scheme (see Figure 11), allowing to configure either internal or external power for supplying banks. The correspondence between TPs and power sources is the following:

1. Input/Output signals for TP1-TP20 are limited by current V_{DD1} value.
2. Input/Output signals for TP41-TP56 are limited by current V_{DD2} value.

Warning: *The CY8C5868AXI-LP035 device is ESD sensitive. The GCDB itself does not contain any additional built-in protection against ESD impact or abnormal voltage spikes on IO lines and power rails.*

3.4 Digital Port Connections

For work with ForgeFPGA and to support digital functions of all other products – a set of 48 Digital TPs is used. Similar to what is described in the previous section, TPs from this group are divided into two banks with a connection to V_{DD1} and V_{DD2} power sources. To support variable supply voltage and isolate main controller from target devices, custom level-shifters are used. Simplified schematic is shown in Figure 23 (Note 1). The SLG46538V, dual supply programmable IC from Renesas, is used as a main component. Thanks to its internal structure and two independent V_{IO} power rails, it allows for a seamless level translation between the main controller and the target device.

Internal communication lines connected to IO port of the SLG46538V with a fixed 3.42 V power supply input (1). Series resistors are used to prevent a short circuit during unexpected conditions.

IO port exposed to Interaction Connectors is powered from V_{DD1} or V_{DD2} (Note 2) power source (2). Each TP has a connection to two IO ports of the SLG46538V – direct connection and connection through the 4.7 kΩ series resistor. Such connection type in a combination with the custom design built for the SLG46538V allows to implement complex output port structures in addition to such standard options as Open-drain PMOS/NMOS, controllable Pull-up, Pull-down, and others. See section 2.7 Digital Generators for more information.

Power connection is done with a help of MOSFET switches (3). It provides a possibility to disconnect supply voltage from output port of level shifters in cases when V_{DD1} and V_{DD2} lines stay outside the allowable minimum and maximum ranges for the SLG46538V.

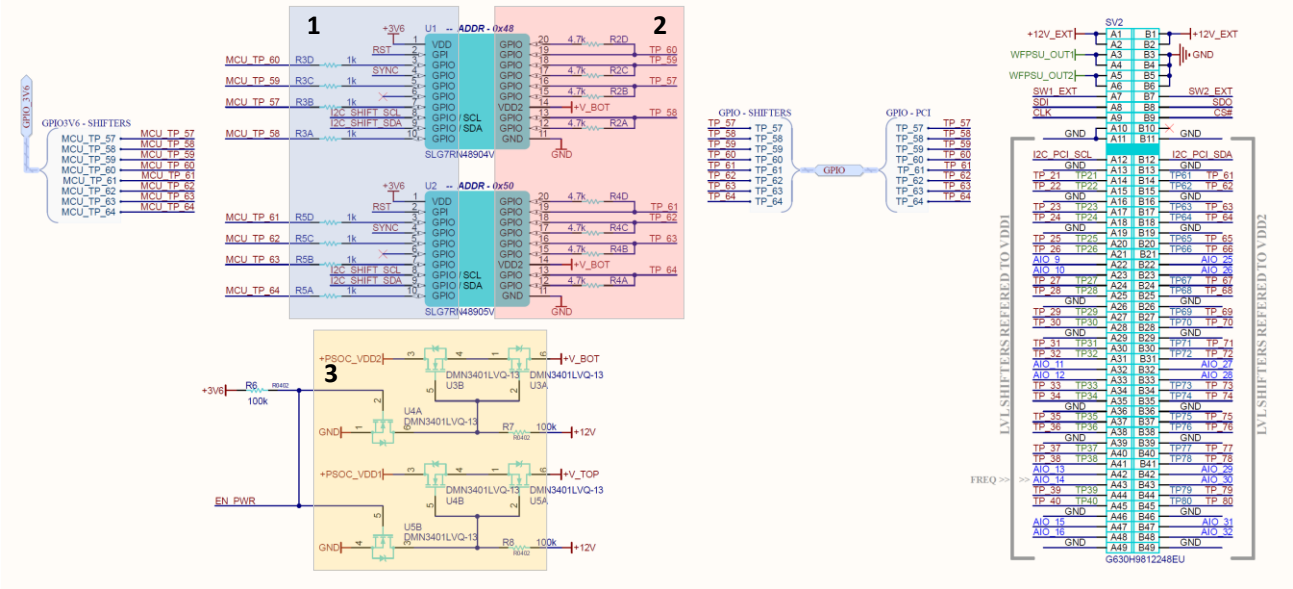


Figure 23. Simplified Schematic Diagram of Digital Test Points Level Translators

Note 1: Part of the overall scheme is shown for demonstration purposes only.

Note 2: For dual-supply mixed-signal ICs, limitations are applied to both supply rails of the device. Check the documentation for more information: SLG46538.

3.5 Analog Waveform Generators Connections

Analog Waveform Generators module is bult from two identical blocks, with eight output channels for each. Simplified (Note) schematic diagram for one block is shown in Figure 24.

The block is built around the integrated DAC IC AD5592RBCPZ (1) from Analog Devices. The SLG47910V (2) from Renesas ForgeFPGA family is used as a control element. In current design, it is used as a small configurable interface converter with additional custom functionality.

Outputs from two AWG blocks are directly (Warning) routed to Interaction Connector, see Figure 6 for a complete pinout.

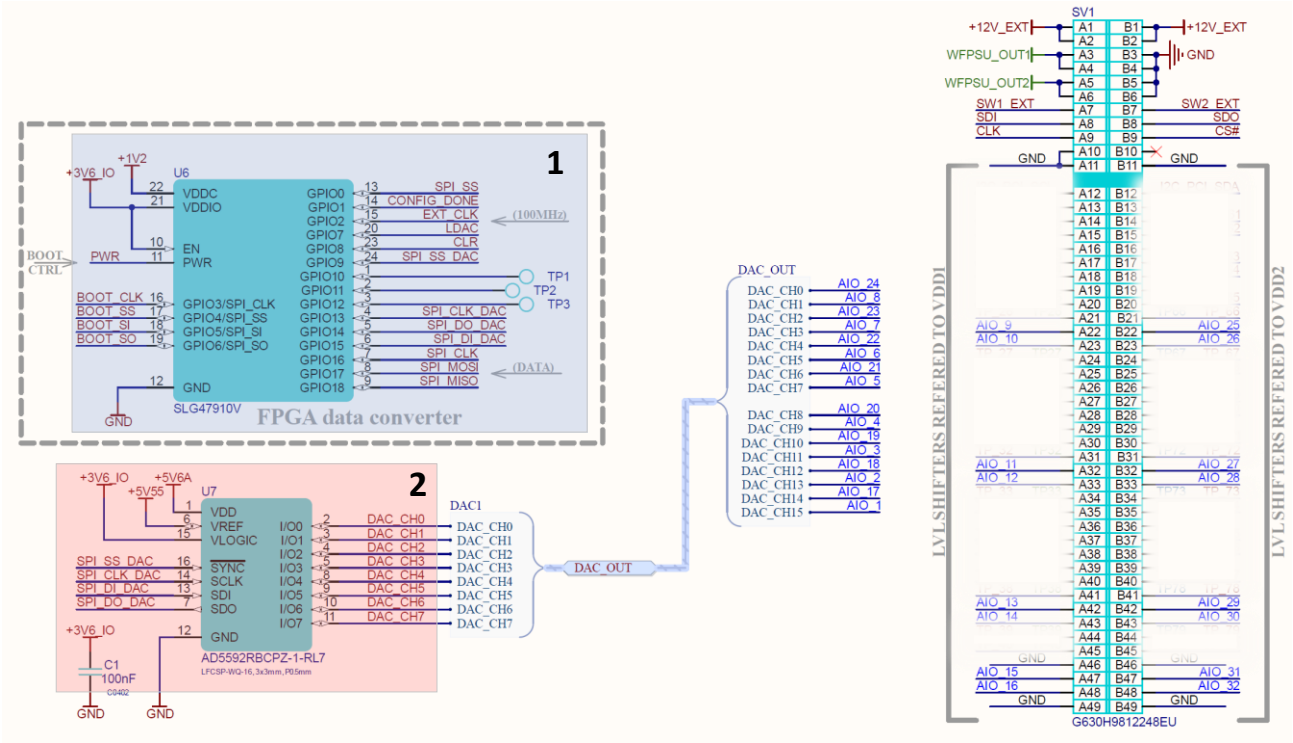


Figure 24. Analog Waveform Generators Output Circuit

Note: Control circuits for two blocks, Boot FLASH IC, data line multiplexer, and power circuits are not shown in the schematic diagram.

Warning: *The AD5592RBCPZ-1 is ESD sensitive. The GCDB itself does not contain any additional built-in protection on all AWG channels.*

4. Electrical Characteristics

Table 11. Main Operation Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Voltage Applied to DC INPUT Connector [1]	V_{DCIN}	9	12	14	V
Required Current for DC INPUT Connector [2]	I_{DCIN}	1.5	-	-	A
Data USB Input Voltage [3]	V_{USB}	4.5	5	5.5	V
Data USB Input Current	I_{USB}	0.5	-	3	A
PWR USB Input Voltage [4]	V_{USB}	9	12	14	V
PWR USB Input Current	I_{USB}	1.5	-	-	A
Operating Ambient Temperature	T_A	15	-	45	°C
Board Dimensions		122 x 164 x 16.5			mm
Weight		190			g

1. Internal +12 V bus will follow input voltage value at DC INPUT connector in the range of +11.8 V to +14 V.
2. To support High Power mode.
3. Connecting the GCDB through the long or poor-quality USB cables may lead to an unstable work because of voltage drop inside the cable.
4. 9 V and 12 V USB PD profiles are supported. Attaching USB source with 5 V output voltage to USB POWER port will not damage the GCDB.

5. Ordering Information

Part Number	Description
SLG4DVKGOCONF	Go Configure Development Board (GCDB-04070101), USB-A to USB-C cable, USB-C to USB-C cable, Wall mount power supply (USA and EU plug).

6. Terms and Definitions

ADC	Analog to Digital Converter
AWG	Analog Waveform Generator
DAC	Digital to Analog Converter
DUT	Device Under Test
GCDB	Go Configure Development Board
GPIO	General Purpose Input/Output
IO	Input/Output
LED	Light Emitting Diode
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
OCP	Overcurrent Protection
OpAmp	Operational Amplifier
OVP	Overvoltage Protection
PC	Personal Computer
PD	Power Delivery
RCB	Reverse Current Blocking
TP	Test Point

7. Revision History

Revision	Date	Description
1.00	Dec 10, 2025	Initial release