ForgeFPGA Socket Card #5

ForgeFPGA™ Socket Card #5 is a development board designed for emulation and prototyping of ForgeFPGA integrated circuits.

Specifications

The "ForgeFPGA Socket Card #5" provides a connection between the pins of a ForgeFPGA and a Development Board. This board can be used for design prototyping with various boot modes. The Socket Card supports the PMOD standard, allowing the connection of different PMOD adapters.

Board Contents

Includes ForgeFPGA Socket Card #5 board.

Features

- Programming and Emulation
- Standalone Boot Option
- Onboard 4-Mbit SPI Flash
- PMOD Connectors
- Clock Generator from 2.5 kHz to 200 MHz
- Standalone Power Connectors

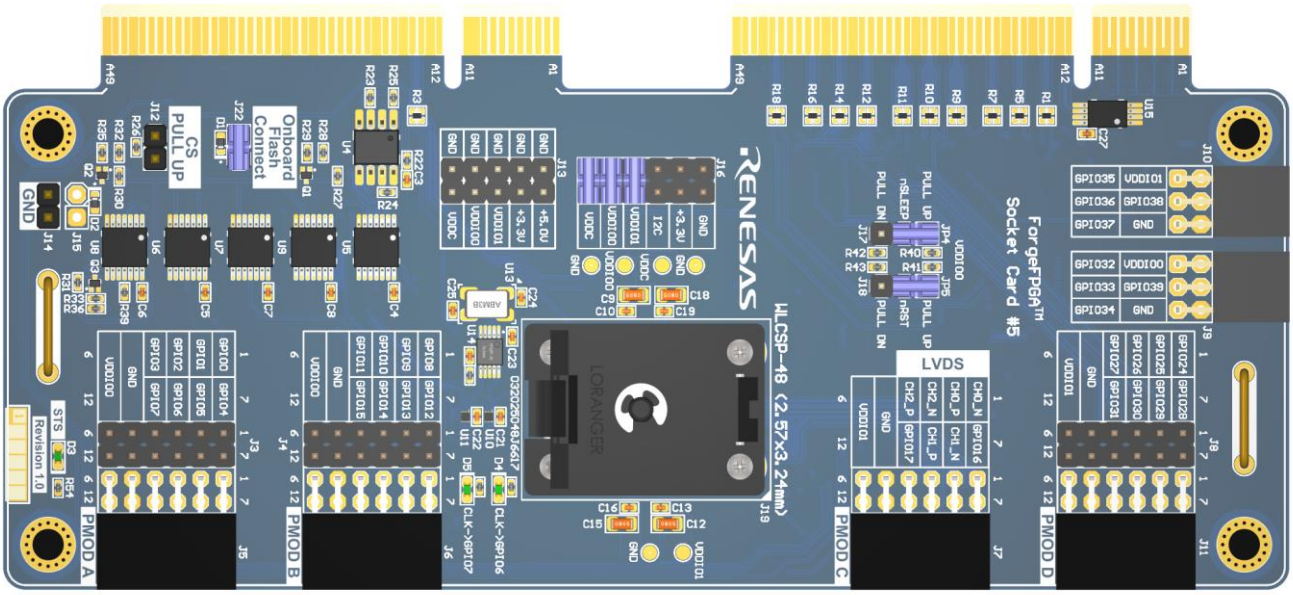


Figure 1. ForgeFPGA Socket Card #5

Contents

Figures

1. Functional Description

The figure below shows the board view and identifies its main components. This board can be used in conjunction with the Go Configure Development Board via the Dual Interaction Connector to transmit and process signals. It can also operate as a standalone unit. The chip can be powered either by the Development Board or through the External Power connector, and signals on the GPIO are accessible through the 12-pin GPIO connectors or PMOD connectors.

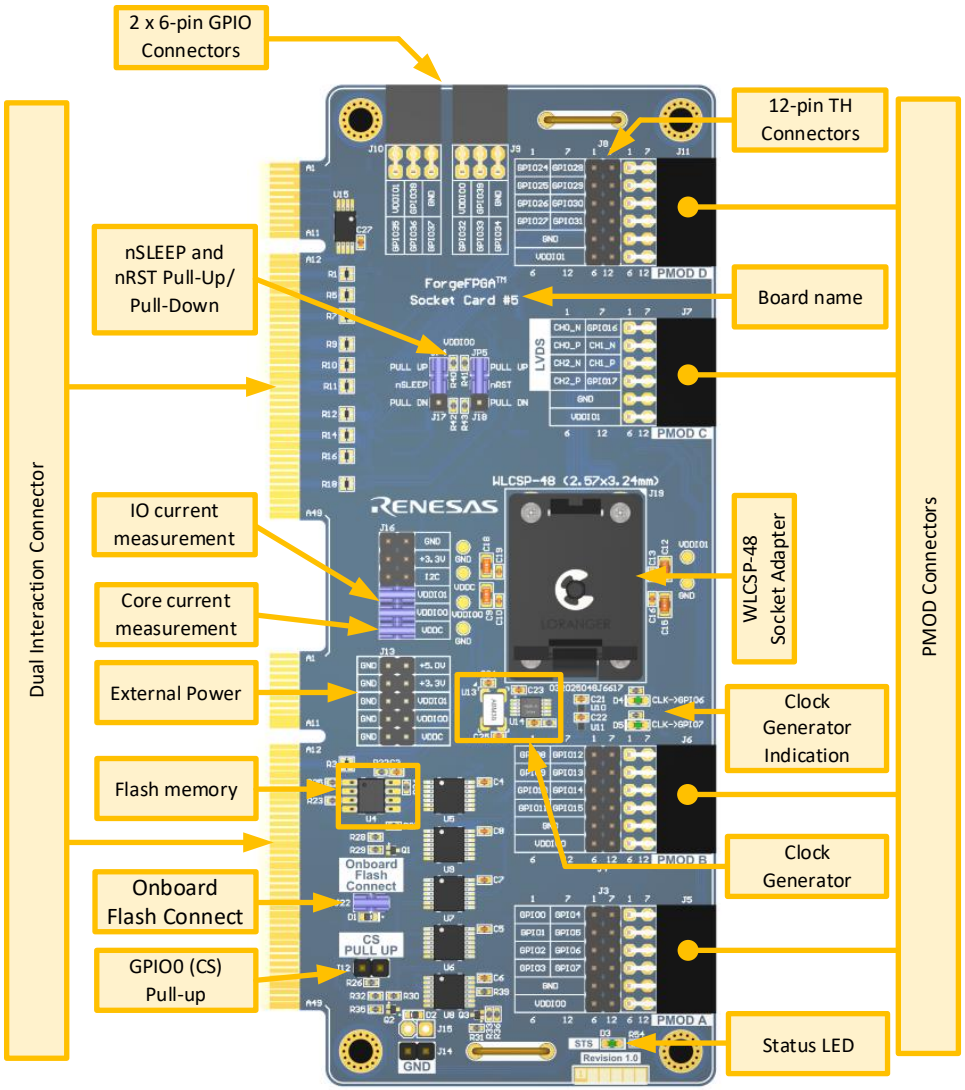
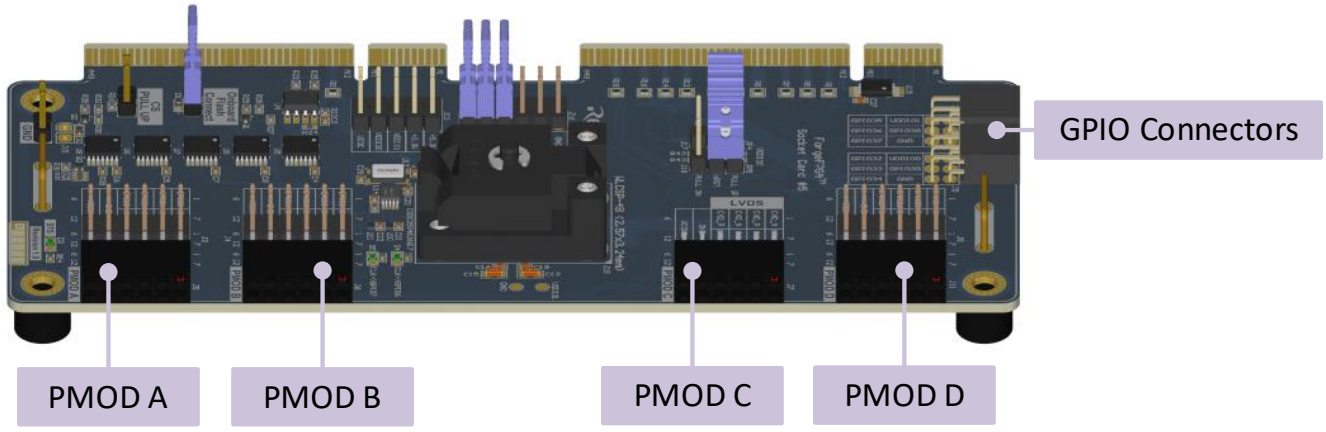


Figure 2. ForgeFPGA Socket Card #5 Components

1.1 PMOD and GPIO Connectors

Access to the socket pins is provided through the GPIO and PMOD connectors, both of which share the same pinout. Note that programming signals from the Interaction Connector to the GPIO/PMOD are gated during programming and emulation entry sequences.



6	5	4	3	2	1
12	11	10	9	8	7

Figure 3. PMOD and GPIO Connector

Table 1. PMOD A-C and External Connectors Pinout

GPIO/PMOD A	
PMOD PIN #	GPIO #
1	GPIO0
2	GPIO1
3	GPIO2
4	GPIO3
5	GND
6	VDDIO0
7	GPIO4
8	GPIO5
9	GPIO6
10	GPIO7
11	GND
12	VDDIO0

GPIO/PMOD B	
PMOD PIN #	GPIO #
1	GPIO8
2	GPIO9
3	GPIO10
4	GPIO11
5	GND
6	VDDIO0
7	GPIO12
8	GPIO13
9	GPIO14
10	GPIO15
11	GND
12	VDDIO0

GPIO/PMOD C	
PMOD PIN #	GPIO #
1	LVDS_0_N/GPIO18
2	LVDS_0_P/GPIO19
3	LVDS_2_N/GPIO22
4	LVDS_2_P/GPIO23
5	GND
6	VDDIO1
7	GPIO16
8	LVDS_1_N/GPIO20
9	LVDS_1_P/GPIO21
10	GPIO17
11	GND
12	VDDIO1

Table 2. PMOD D and External Connectors Pinout / GPIO Connectors Pinout

GPIO/PMOD D	
PMOD PIN #	GPIO #
1	GPIO24
2	GPIO25
3	GPIO26

GPIO CONN J9	
CONN PIN #	GPIO #
1	GPIO32
2	GPIO33
3	GPIO34

GPIO CONN J10	
CONN PIN #	GPIO #
1	GPIO35
2	GPIO36
3	GPIO37

4	GPIO27
5	GND
6	VDDIO1
7	GPIO28
8	GPIO29
9	GPIO30
10	GPIO31
11	GND
12	VDDIO1

4	VDDIO0
5	GPIO39
6	GND

4	VDDIO1
5	GPIO38
6	GND

Table 3. GPIO and PMOD Connector Characteristics

Parameter	Description	Min	Typ	Max	Unit
I_L	Input leakage current	-	2	-	µA
C_{IO}	Input-Output Pin Capacitance	-	7	-	pF
R_{ON}	Series Resistance	-	25	52	Ω
V_{IN}	Input Voltage	-0.5	-	VDDIO	V

1.2 ForgeFPGA Current Measuring

ForgeFPGA Socket Card #5 also includes an option for measuring IC power consumption. To perform this measurement, remove the jumpers (as shown in **Figure 4**) and connect a current meter in their place. The typical load should not exceed 200 mA. Under normal operation, when current measurement is not required, the jumpers should remain installed on the board.

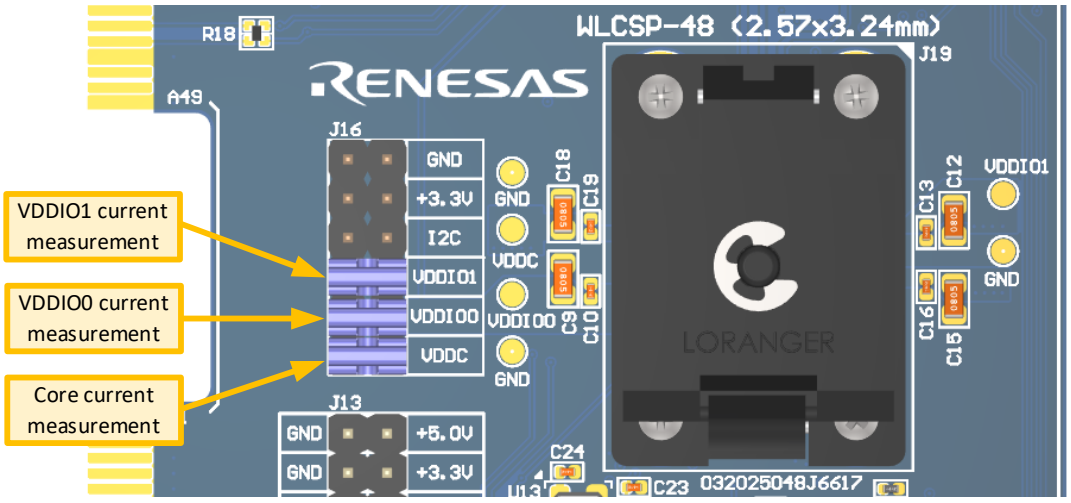


Figure 4. ForgeFPGA Current Measurement Setup

1.3 SPI Interface between ForgeFPGA and Flash Memory

Figure 5 shows the SPI flash interface connection between ForgeFPGA IC and Flash Memory.

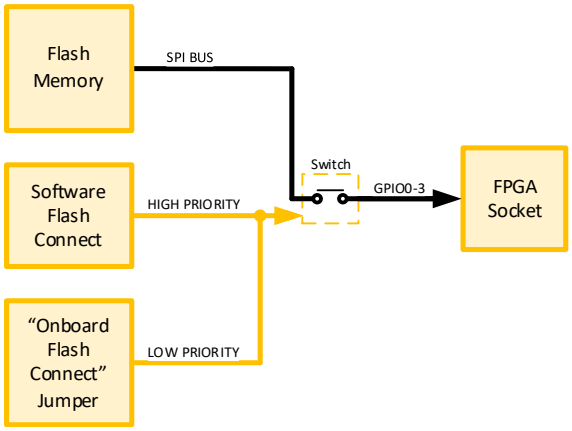
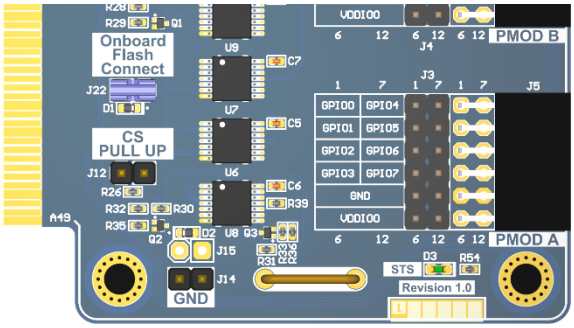


Figure 5. SPI Interface Connection

The "Onboard Flash Connect" and "CS PULL UP" jumpers should be installed when using the board with the Development Board. Note that jumper removal or configuration changes are overridden and controlled by the Development Board. The table in **Figure 6** shows the correct jumper setup for standalone operation.



Mode	Onboard Flash Connect	CS PULL UP
Internal OTP Memory	0	0
SPI FLASH Memory	1	X
EXT Flash Memory	0	1

Figure 6. Memory Selection Table for Boot Configuration

External Flash Memory can be connected to Socket Card by using PMOD A.

Figure 7 shows how to connect External Flash Memory to PMOD A.

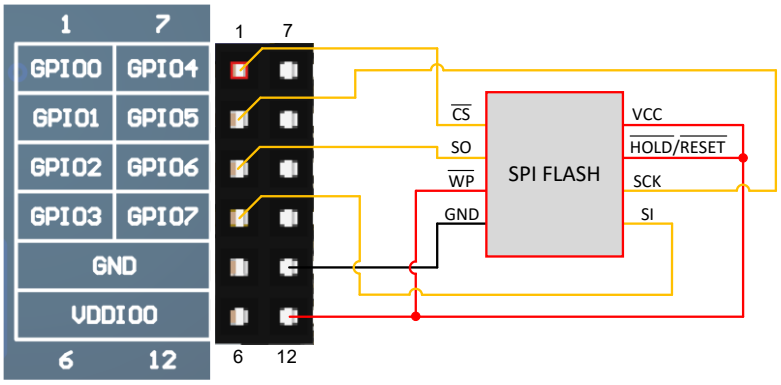


Figure 7. Connection of External Flash Memory to PMOD A

1.4 "External Power" Connector

ForgeFPGA Socket Card #5 can also operate with an external power supply. In this case, five separate power supply channels must be connected to the "External Power" (J13) connector (shown in **Figure 8**). The voltage

and current levels for VDDIO0, VDDIO1, and VDDC must comply with the ForgeFPGA IC specifications. The “5.0V” terminal should be supplied with 5.0 V to power the commutation switches. The external power supply option can only be used when the Socket Card is not connected to the Go Configure Development Board.

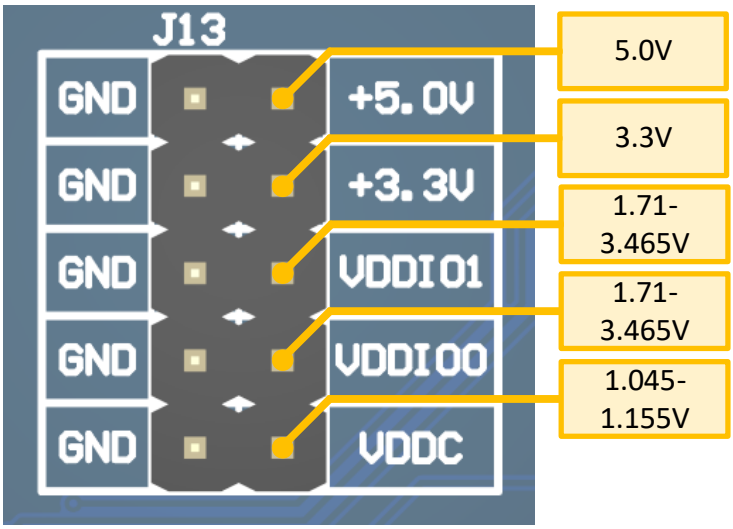


Figure 8. External Power Connector Pinout

1.5 Clock Generator

ForgeFPGA Socket Card #5 has I2C Programmable CMOS Clock Generator – Si5351A-B-GTR.

It used for drive PLL inputs of ForgeFPGA – GPIO6 and GPIO7.

Table 4 shows main characteristics of Clock Generator.

Table 4. Main Characteristics of Clock Generator

Parameter	Description	Min	Typ	Max	Unit
F_{CLK}	Frequency Range	0.0025	-	200	MHz
J_{PER}	Period Jitter	-	70	155	ps, pk-pk
V_{DDOx}	Output Buffer Voltage	-	VDDIO0	-	V
I_{DDOx}	Output Buffer Supply Current (Per Output)	-	2.2	5.6	mA

1.6 Status LED

The status LED indicates the current operation being performed on the chip

Chip Standard operations:

- **Read**
- **Program**

Flash operations:

- **Read**
- **Program**

- **Emulation**
- **Test Mode**
- **Erase**
- **Test Mode**

The position of Status LED (D3) is shown on **Figure 9**.

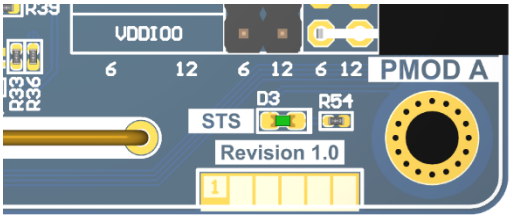


Figure 9. Status LED

2. Working with ForgeFPGA Products

To start working with ForgeFPGA products using the Socket Card, two methodologies are available:

- Using the Go Configure Development Board.
- In standalone mode, where the ForgeFPGA configuration is downloaded from the onboard SPI flash.

2.1 Standalone Working Mode

As previously described, ForgeFPGA can boot from onboard flash as an SPI host. There are two ways of programming onboard flash: program with the Development Board or program the flash IC manually. The programming pins for the flash chip are accessible through the PMOD A connector. To program manually, the Socket Card must be powered via the “EXT Power” connector. If the VDDIO voltage is equal to or greater than 3.0 V, the “5V” and “VDDIO” pins can be powered from the same source.

During this operation, the ForgeFPGA must be disabled by applying logic LOW (0) to the “PWR” pin. Additionally, the “Onboard Flash Connect” and “CS PULL UP” jumpers must be installed. If the SPI flash is programmed correctly, setting logic HIGH (1) to both the PWR and EN pins will allow the ForgeFPGA to boot from the SPI flash.

2.2 Configuration with Go Configure Development Board

To begin working with ForgeFPGA products, connect the platform to a PC using a USB Type-C cable and apply power.
Important: The USB cable should be connected directly to the PC. Avoid using USB hubs or docking stations.
Ensure the Socket Card is properly connected to the Go Configure Development Board as shown in **Figure 10**.

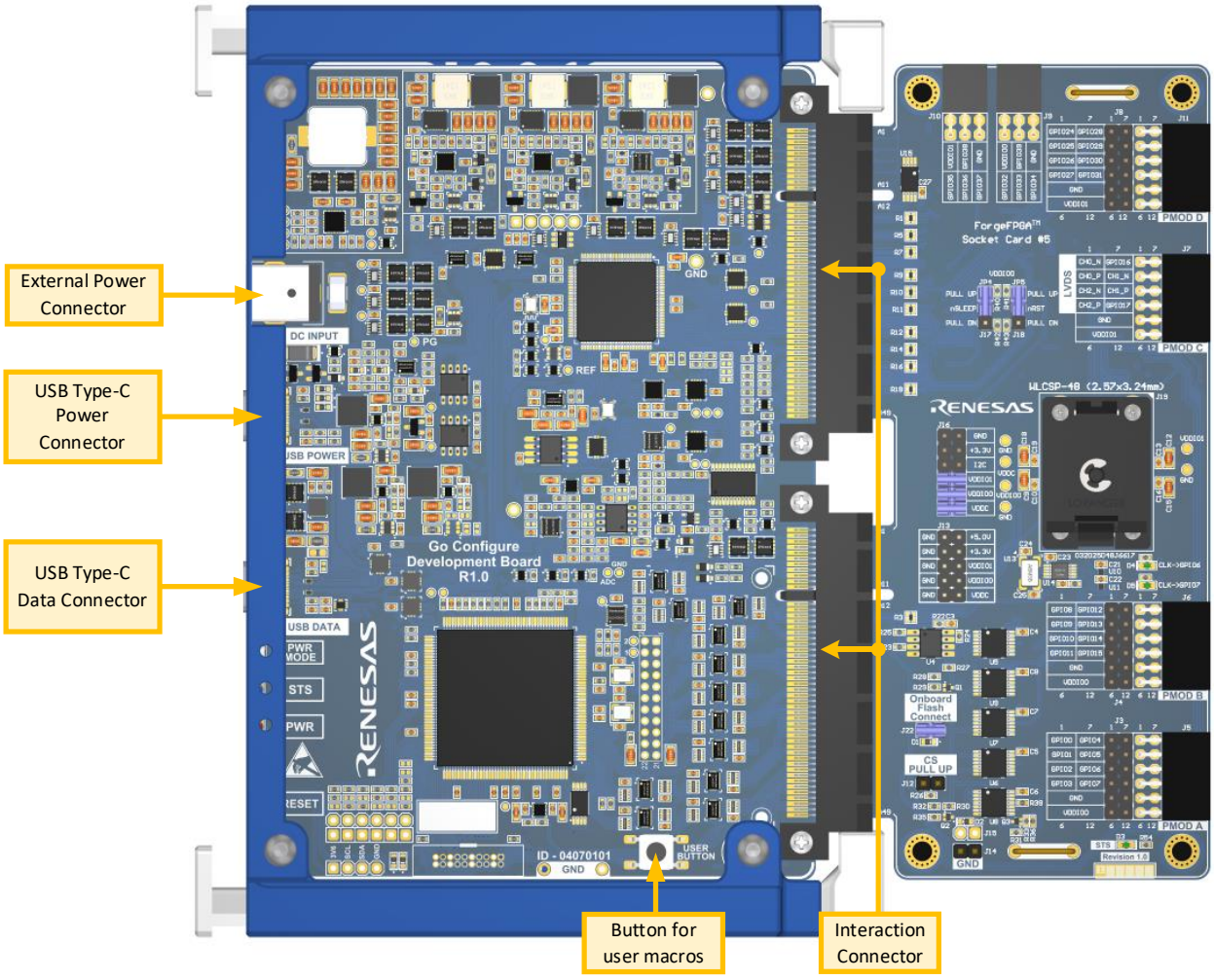


Figure 10. Development Kit

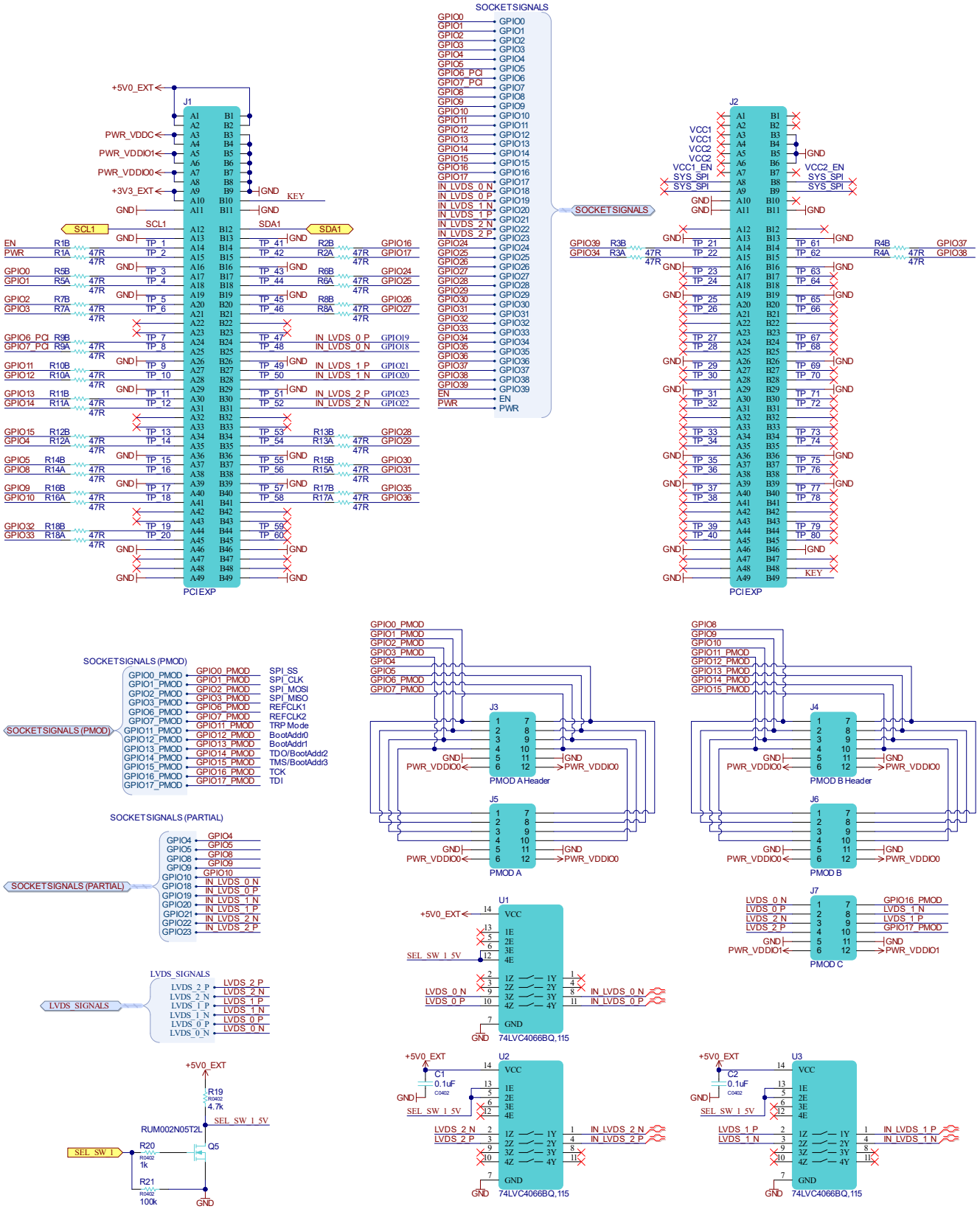
If all the connections are correct, then the red LED (PWR) will automatically turn on. After selecting “Go Configure Development Board” in Go Configure “Debug” tab, the blue LED will blink several times, and the “HW-FW” version will appear in the bottom-left corner of the debugging control window.

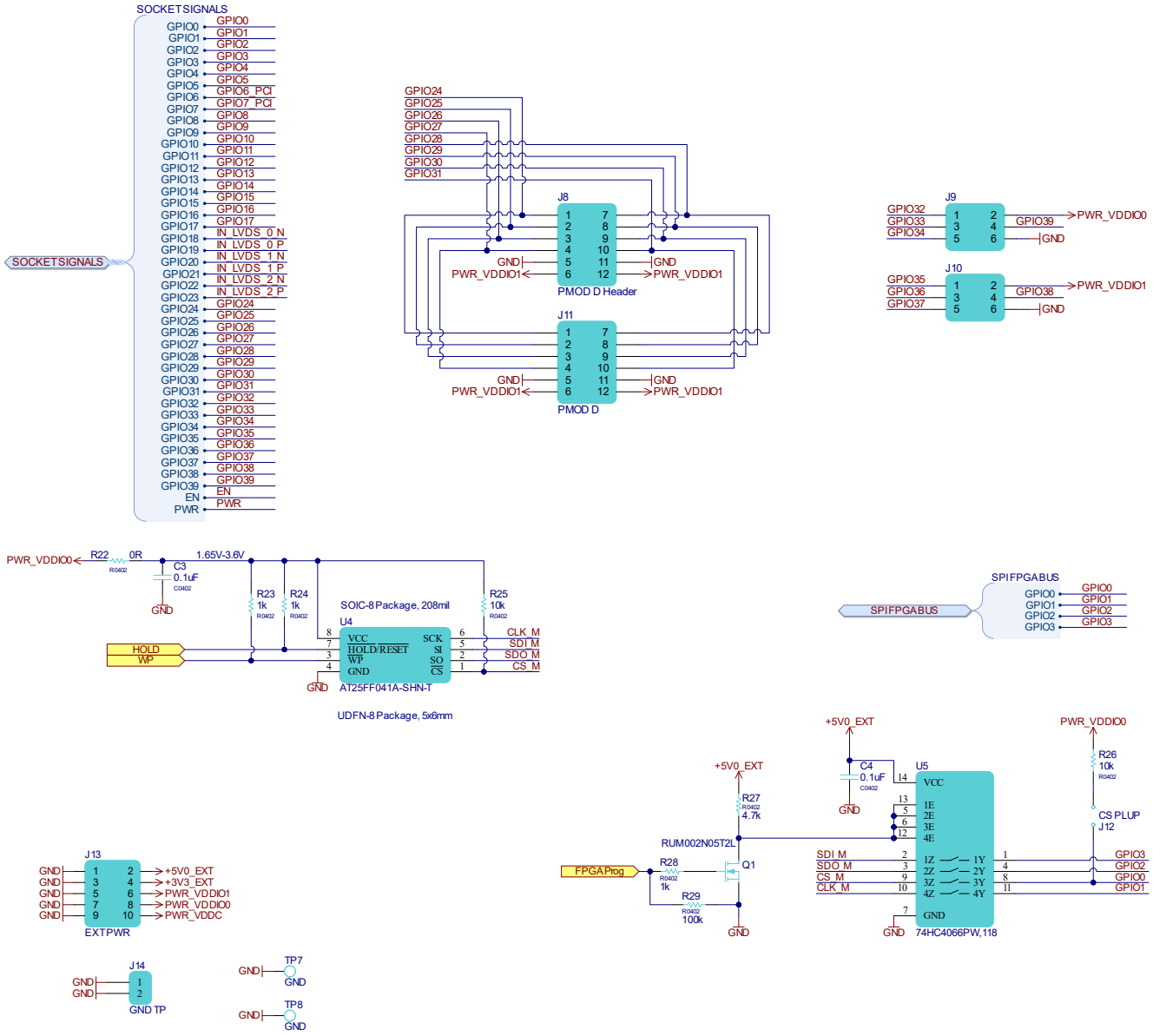
The following debug options are available:

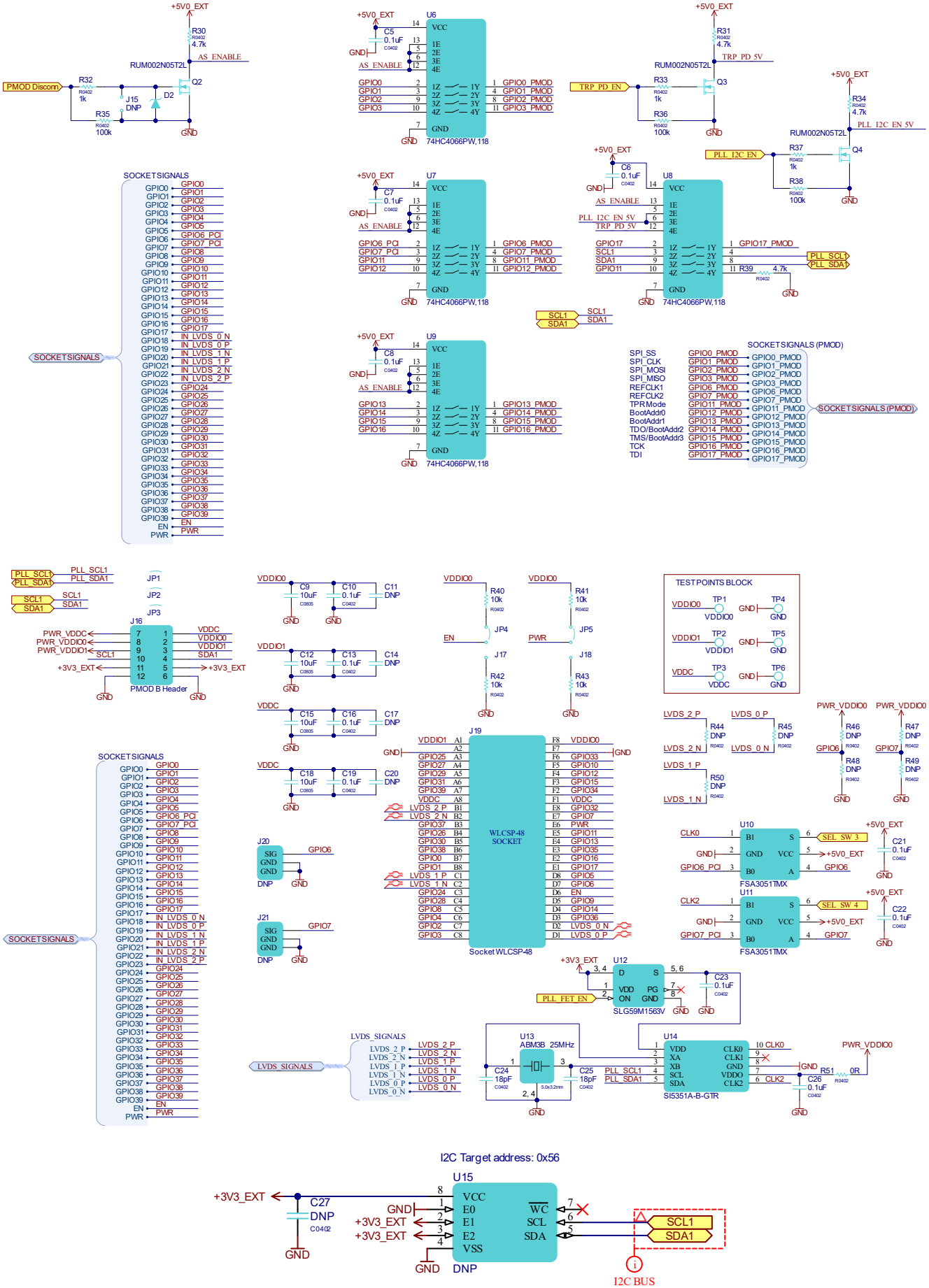
- Emulation – allows debugging of the current project. This mode is available only after synthesis and bitstream generation in the FPGA Editor.
- Test Mode – enables debugging of a programmed project.
- Test Mode* – used to debug a project loaded from SPI Flash.
- Read – reads the configuration from the programmed chip and opens the project in a new software instance or in the “Project Data” window of the current instance.
- Program – programs the chip with the current project.
- TP Map – displays the test point map in the workspace, reflecting the physical test points on the development platform.

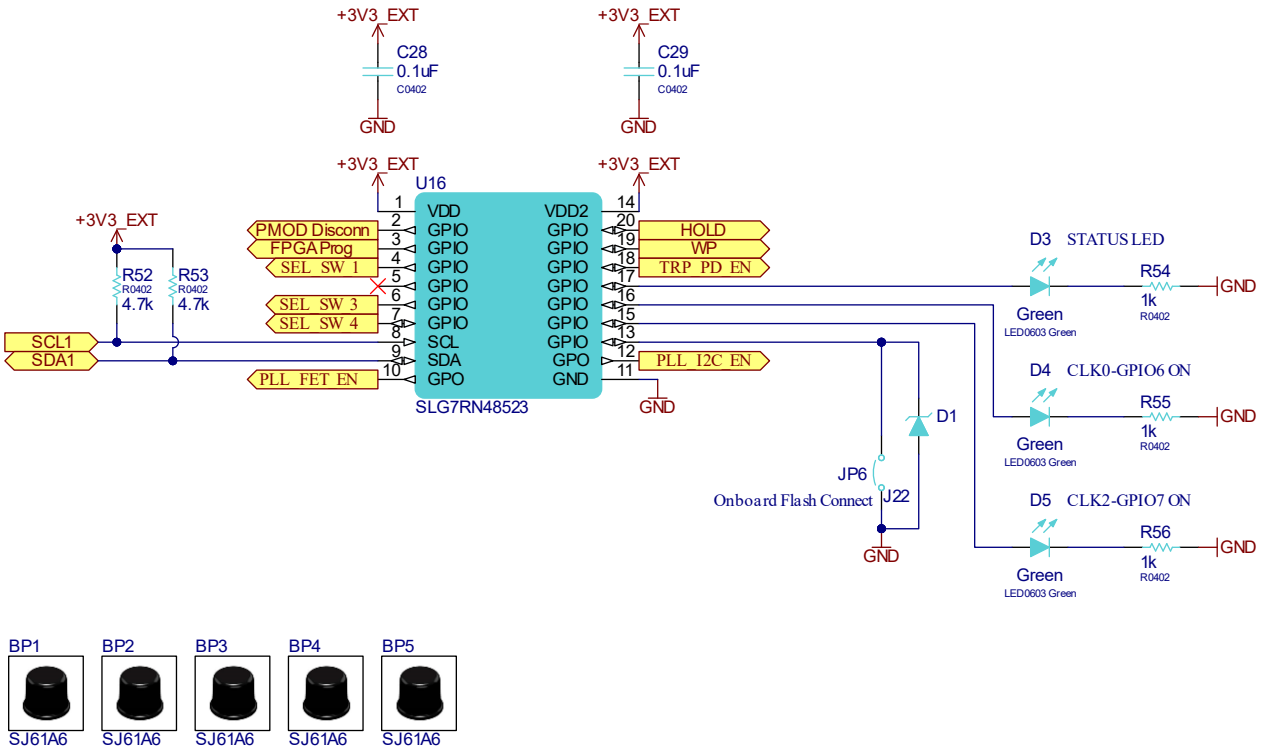
The more detailed information about Go Configure software can be found in Go Configure™ Software Hub User Guide.

3. Schematic Diagram




SOCKETSIGNALS
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6_PCI
GPIO7_PCI
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
IN_LVDS_0_N
IN_LVDS_0_P
IN_LVDS_1_N
IN_LVDS_1_P
IN_LVDS_2_N
IN_LVDS_2_P
GPIO24
GPIO25
GPIO26
GPIO27
GPIO28
GPIO29
GPIO30
GPIO31
GPIO32
GPIO33
GPIO34
GPIO35
GPIO36
GPIO37
GPIO38
GPIO39
EN
PWR
J8
PMOD D Header
J11
PMOD D
J9
J10
PWR_VDDIO0
PWR_VDDIO1
GND
PWR_VDDIO00
R22
0R
1.65V-3.6V
C3
0.1uF
R23
1k
R24
1k
R25
10k
U4
SOIC-8 Package, 208mil
UDFN-8 Package, 5x6mm
AT25FF041A-SHN-T
HOLD
WP
CLK_M
SDI_M
SDO_M
CS_M
SPIFPGABUS
J13
EXTPWR
+5V0_EXT
+3V3_EXT
PWR_VDDC
J14
GND TP
TP7
TP8
R27
4.7k
R28
1k
R29
100k
Q1
RUM002N05T2L
FPGAProg
C4
0.1uF
U5
74HC4066PW,118
R26
10k
CS PLUP
J12


+5V0_EXT
R30
4.7k
AS_ENABLE
RUM002N05T2L
Q2
PMOD Discon
R32
1k
J15
DNP
D2
R35
100k
GND
U6
74HC4066PW,118
GPIO0_PMOD
GPIO1_PMOD
GPIO2_PMOD
GPIO3_PMOD
TRP_PD_5V
TRP_PD_EN
R31
R33
R36
Q3
PLL_I2C_EN_5V
R34
Q4
R37
R38
PLL_I2C_EN
U7
U8
GPIO6_PMOD
GPIO7_PMOD
GPIO11_PMOD
GPIO12_PMOD
GPIO17_PMOD
SCL1
SDA1
PLL_SCL
PLL_SDA
U9
GPIO13_PMOD
GPIO14_PMOD
GPIO15_PMOD
GPIO16_PMOD
SOCKET SIGNALS
SOCKET SIGNALS (PMOD)
SPI_SS
SPI_CLK
SPI_MOSI
SPI_MISO
REFCLK1
REFCLK2
TPR Mode
BootAddr0
BootAddr1
TDO/BootAddr2
TMS/BootAddr3
TCK
TDI
JP1
JP2
JP3
J16
PMOD B Header
PWR_VDDC
PWR_VDDIO0
PWR_VDDIO1
VDDC
VDDIO0
VDDIO1
+3V3_EXT
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
10uF
0.1uF
DNP
R40
R41
R42
R43
10k
JP4
JP5
J17
J18
TEST POINTS BLOCK
TP1
TP2
TP3
TP4
TP5
TP6
J19
WLCSP-48 SOCKET
Socket WLCSP-48
J20
J21
SIG
DNP
R44
R45
R46
R47
R48
R49
R50
LVDS_2_P
LVDS_2_N
LVDS_1_P
LVDS_1_N
LVDS_0_P
LVDS_0_N
U10
U11
FSA3051TMX
SEL_SW_3
SEL_SW_4
C21
C22
U12
SLG59M1563V
PLL_FET_EN
C23
LVDS_SIGNALS
U13
ABM3B 25MHz
C24
C25
18pF
U14
SI5351A-B-GTR
CLK0
CLK2
R51
0R
C26
I2C Target address: 0x56
U15
VCC
E0
E1
E2
VSS
WC
SCL
SDA
C27
I2C BUS


+3V3_EXT
C28
0.1uF
C0402
GND
+3V3_EXT
C29
0.1uF
C0402
GND
+3V3_EXT
U16
+3V3_EXT
R52
R0402
4.7k
R53
R0402
4.7k
SCL1
SDA1
PMOD Disconn
FPGAProg
SEL_SW_1
SEL_SW_3
SEL_SW_4
PLL_FET_EN
1 VDD
2 GPIO
3 GPIO
4 GPIO
5 GPIO
6 GPIO
7 GPIO
8 SCL
9 SDA
10 GPO
VDD2 14
GPIO 20
GPIO 19
GPIO 18
GPIO 17
GPIO 16
GPIO 15
GPIO 13
GPIO 12
GPO 11
GND
HOLD
WP
TRP_PD_EN
PLL_I2C_EN
SLG7RN48523
GND
D3 STATUS LED
R54
1k
R0402
GND
Green
LED0603 Green
D4 CLK0-GPIO6 ON
R55
1k
R0402
GND
Green
LED0603 Green
D5 CLK2-GPIO7 ON
R56
1k
R0402
GND
Green
LED0603 Green
D1
JP6
Onboard Flash Connect
J22
GND

BP1
BP2
BP3
BP4
BP5
SJ61A6
SJ61A6
SJ61A6
SJ61A6
SJ61A6

4. Bill Of Materials

#	Designator	Manufacturer Part Number	Manufacturer	Quantity
1	BP1, BP2, BP3, BP4, BP5	SJ61A6	3M	5
2	C1-C8, C10, C13, C16, C19, C23, C26, C28, C29	GCM155R71C104KA55D	Murata	16
3	C9, C12, C15, C18	GRM21BR61C106KE15L	Murata	4
4	C11, C14, C17, C20, C27	DNP	DNP	5
5	C21, C22	GCM155R71C104KA55D	Murata	2
6	C24, C25	CL05C180JB5NNNC	Samsung	2
7	D1, D2	DESD5V0U1BB-7	Diodes	2
8	D3, D4, D5	150060GS75000	Wurth Electronics	3
9	J3, J4, J8, J16	67996-212HLF	Amphenol ICC / FCI	4
10	J5, J6, J7, J11	PPPC062LJBN-RC	Sullins	4
11	J9, J10	PPPC032LJBN-RC	Sullins	2
12	J12, J22	68000102HLF	Amphenol ICC / FCI	2
13	J13	67997210HLF	Amphenol ICC / FCI	1
14	J14	68000102HLF	Amphenol ICC / FCI	1
15	J15	DNP	DNP	1
16	J17, J18	HTSW-103-07-T-S	Samtec	2
17	J19	060SQ049J6618C	Renesas Electronics	1
18	J20, J21	DNP	DNP	2
19	JP1, JP2, JP3, JP4, JP5, JP6	NPC02SXON-RC	Sullins	6
20	Q1, Q2, Q3, Q4	RUM002N05T2L	Rohm	4
21	Q5	RUM002N05T2L	Rohm	1
22	R1- R18	S41X043470JP	CTS	18
23	R19	RC0402JR-074K7L	Yageo	1
24	R20	RC0402JR-071KL	Yageo	1
25	R21	RC0402JR-07100KL	Yageo	1
26	R22, R51	RC0402JR-070RL	Yageo	2
27	R23, R24, R28, R32, R33, R37, R54, R55, R56	RC0402JR-071KL	Yageo	9
28	R25, R26, R40, R41, R42, R43	RC0402JR-0710KL	Yageo	6
29	R27, R30, R31, R34, R39, R52, R53	RC0402JR-074K7L	Yageo	7
30	R29, R35, R36, R38	RC0402JR-07100KL	Yageo	4
31	R44-R50	DNP	DNP	7
32	U1, U2, U3	74LVC4066BQ,115	Nexperia	3
33	U4	AT25FF041A-SHN-T	Renesas	1
34	U5, U6, U7, U8, U9	74HC4066PW,118	Nexperia	5
35	U10, U11	FSA3051TMX	ON Semiconductor / Fairchild	2
36	U12	SLG59M1563V	Renesas Electronics America Inc	1
37	U13	ABM3B-25.000MHZ-D2Y-T	Abracon	1
38	U14	SI5351A-B-GTR	Skyworks Solutions	1
39	U15	DNP	DNP	1
40	U16	SLG7RN48523	Renesas Electronics America Inc	1

5. Ordering Information

Part Number	Description
SLG7SC5	ForgeFPGA Socket Card #5 (ID-06110101)
SLG47921C-SKT	ForgeFPGA Socket Card #5 (part number SLG7SC5), 20 Samples of SLG47921C and SLG479PMODLED Adapter
SLG47912C-SKT	ForgeFPGA Socket Card #5 (part number SLG7SC5), 20 Samples of SLG47912C and SLG479PMODLED Adapter

6. Certifications

The ForgeFPGA Socket Card #5 complies with the following certifications/standards.

6.1 EMC/EMI Standards

- FCC Notice (Class A)

This device complies with FCC 47 CFR part 15, subpart B. Operation is subject to the following two conditions:
(1) The equipment should be handled using standard CMOS device precautions. The user must take all precautions to avoid the build-up of static electricity while working with this equipment. All test and measurement tools, including the workbench, must be grounded. The user/operator must be grounded using the wrist strap. The connectors and/or device pins should not be touched with bare fingers.

(2) This Class A digital device complies with the FCC rules outlined in 47 CFR Part 15. This equipment may cause radio frequency noise when used in a residential area. In such cases, the user/operator of the equipment may be required to take appropriate countermeasures at their own responsibility.

- CE Class B (EMC)

This product is in conformity with the following Directive(s) of the European Parliament and of the Council on the harmonisation of the laws of the Member States relating to Electromagnetic Compatibility 2014/30/EU (EMC Directive). The equipment can be operated under the following conditions:

(1) The equipment should be handled using standard CMOS device precautions. The user must take all precautions to avoid the build-up of static electricity while working with this equipment. All test and measurement tools, including the workbench, must be grounded. The user/operator must be grounded using the wrist strap. The connectors and/or device pins should not be touched with bare fingers.

(2) This is a ‘Class B’ (EN 55032:2015) device. This equipment may cause radio frequency noise when used in a residential area. In such cases, the user/operator of the equipment may be required to take appropriate countermeasures at their own responsibility.

- UKCA Class B (EMC)

This product conforms to the following relevant UK Statutory Instrument(s) (and their amendments): 2016 No. 1091 Electromagnetic Compatibility Regulations 2016. The equipment can be operated under the following conditions:

(1) The equipment should be handled using standard CMOS device precautions. The user must take all precautions to avoid the build-up of static electricity while working with this equipment. All test and measurement tools, including the workbench, must be grounded. The user/operator must be grounded using the wrist strap. The connectors and/or device pins should not be touched with bare fingers.

(2) This is a ‘Class B’ (BS EN 55032:2015) equipment. This equipment may cause radio frequency noise when used in a residential area. In such cases, the user/operator of the equipment may be required to take appropriate countermeasures at their own responsibility.

6.2 Material Selection, Waste, Recycling, and Disposal Standards

- 2011/65/EU Restriction of Hazardous Substances (RoHS Directive) + amendment (EU) 2015/863 (RoHS3)
- 2012/19/EU Waste Electrical and Electronic Equipment (WEEE Directive)
- 2012 No. 3032 The Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment Regulations
- 2013 No. 3113 Waste Electrical and Electronic Equipment Regulations

7. Revision History

Revision	Date	Description
1.02	Mar 19, 2026	Fixed typos
1.01	Mar 5, 2026	Added Certifications section
1.00	Nov 10, 2025	Initial release.