Connectivity Production Line Tool

This document describes the Renesas Connectivity Production Line Tool. The Connectivity PLT hardware, as well as various software applications, are explained in detail. The purpose of this document is to guide users in the setup and operation of the tool. Please add functional and/or application names in keywords in Advanced Properties of the Word file.

Contents

Figures

Tables

1. Terms and Definitions

BDA	Bluetooth® Device Address
Bluetooth LE	Bluetooth® Low Energy
BT Classic	Bluetooth® Classic
CS	Configuration Script (a Renesas DA14xxx devices memory area related to production testing)
DMM	Digital Multi Meter
DIP Switch	Dual in-line package switches
DUT	Device Under Test
HCI	Host Controller Interface
PLT	Production Line Tool
RF	Radio Frequency
RFTU	Radio Frequency Test Unit

2. References

[1] DA14531 Datasheet, Renesas Electronics.

[2] DA14535 USB kit - DA14535-00FXDEVKT-U.

[3] DA14695 USB kit - DA14695-00HQDEVKT-U.

[4] https://www.microchip.com/en-us/development-tool/sam-ba-in-system-programmer

[5] https://www.ni.com/en/support/downloads/drivers/download.ni-visa.html#565016

Note 1 References are for the latest published version, unless otherwise indicated.

3. Introduction

The Renesas Connectivity PLT is designed to test, calibrate, and perform memory operations for multiple devices under test (DUTs) in parallel. Specifically, up to four Connectivity PLT boards with eight test sites each can be daisy chained to achieve 32 test sites.

The following parts are delivered with the tool:

- Hardware:
  - Main board (Figure 1)
  - Power cable
- Software:
  - Installation package for Windows environment
- Documents
  - User manual
  - Electrical schematics
  - Gerber files
  - Bill of Materials.

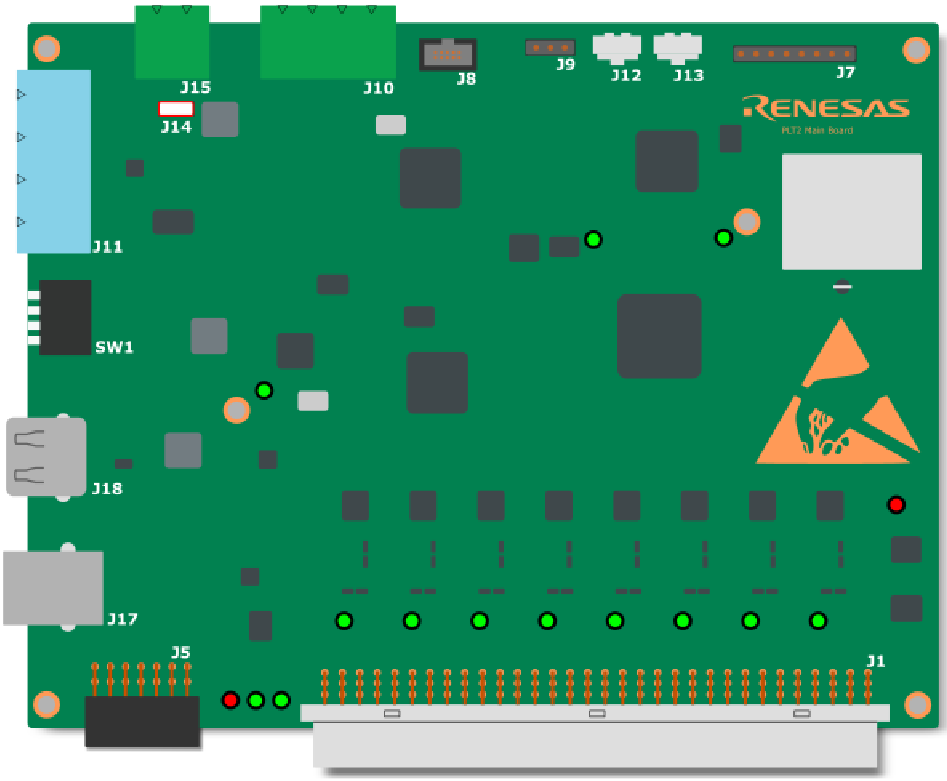


Figure 1. Main board

4. System Overview

4.1 Typical Setup

The Connectivity PLT is a configurable tool that can be adapted to the needs of the production line. Figure 2 shows a simple configuration that consists of a single Connectivity PLT board with eight connected DUT's powered by an external power supply. The host PC is connected to the Connectivity PLT board and to an RF test unit (in this case the SmartBond™ DA14695 Bluetooth® Low Energy 5.2 USB Development Kit). The host has a connected screen so it can run the Connectivity PLT execution application.

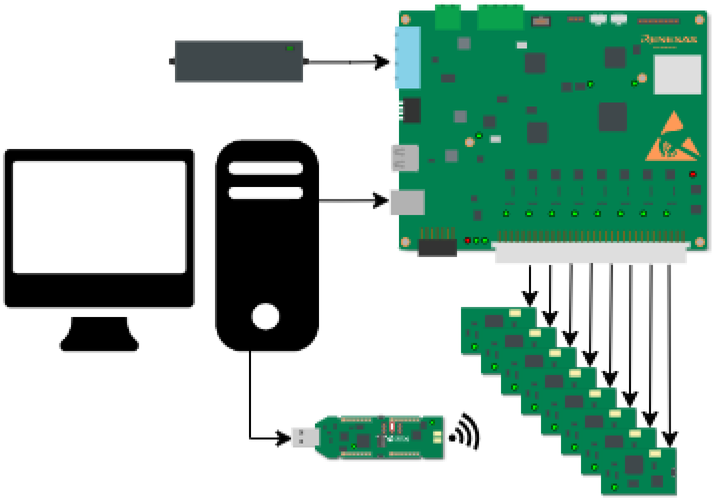


Figure 2. Basic setup

4.2 Typical Test Sequence

The tool performs the following actions:

1. The production test firmware is downloaded to the DUT.
2. Factory timestamp is read from OTP.
3. Automatic crystal (XTAL) trimming is performed.
4. RF RSSI RX tests are performed.
5. Advertise scan test is performed.
6. Flash programmer firmware is downloaded to RAM
7. The (customer) application firmware is downloaded (into OTP, QSPI flash).
8. The OTP Configuration Script and Header are written to OTP.
9. OTP and Flash memory are read back for verification.
10. DUTs are powered down.

All actions are performed at the same time on all DUTs up to 32 devices.

5. Hardware Setup

5.1 Power Supply Connections

The Connectivity PLT is designed for use with an external power supply connected to J11. The type of connector is a four-pin terminal block (TBP01R1W-508-04BE). Table 1 shows the requirements for this power supply, and Figure 3 shows the pinout of J11, indicating that the power connector allows for daisy chaining.

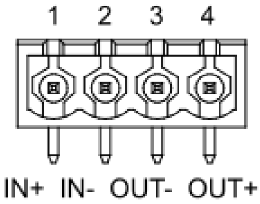


Figure 3. Power Connector J11

Table 1. Power supply characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IN}	Input supply voltage		11	12	15	V
I_{IN}	Input supply current	Single Connectivity PLT board	2			A
I_{IDLE}	IDLE current draw	Single Connectivity PLT board		200		mA

5.2 DUT Connections

The DUT connector is an interface for up to eight application boards that can be connected. The type of connector is a 96pin DIN 41612 male connector from Amphenol (86093967113745ELF). Mating parts can be found on the producer’s website. The power and the signals to the application board go through this connector. The connector is divided into eight sections, one section per DUT (Figure 4). The pin layout of each section is the same and can be found in Figure 5.

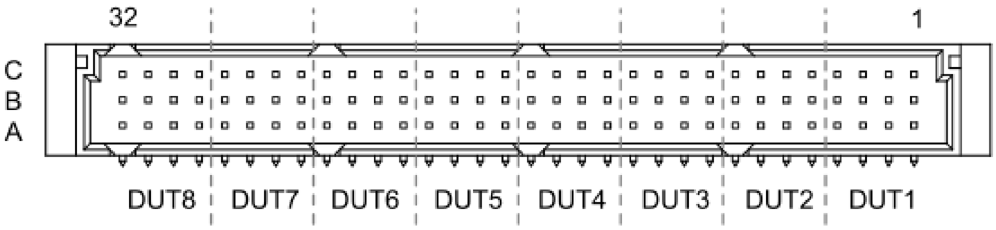
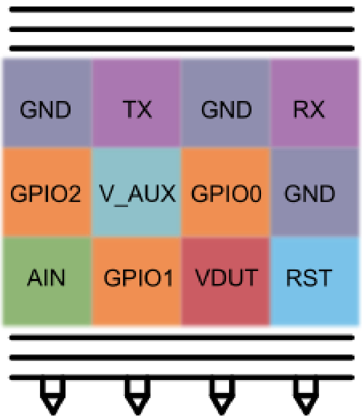


Figure 4. DUT connector



GND	TX	GND	RX
GPIO2	V_AUX	GPIO0	GND
AIN	GPIO1	VDUT	RST

Figure 5. DUT connector pin layout

Table 2. DUT connection characteristics

Parameter	Description	Conditions	Min	Typical	Max	Unit
V_{DUT}	Configurable DUT supply voltage		1.1		5.0	V
I_{DUT}	DUT current	Independent of V_{DUT}			300	mA
V_{AUX}	Configurable Auxiliary voltage		0		5.0	V
I_{AUX}		1 kΩ series resistor			1	mA
AIN	Analog input voltage		0		5.0	V
	Input impedance			830		kΩ
	ADC resolution (LSB)			1.25		mV
V_{GPIO}	Configurable GPIO voltage		1.2		3.3	V
V_{GPIO_OUT}	GPIO out high voltage	Percentage of V_{GPIO}	70			%
	GPIO out low voltage	Percentage of V_{GPIO}			30	%
I_{GPIO_OUT}	GPIO output current	Depends on FPGA setting				mA
V_{GPIO_IN}	GPIO in high threshold	Percentage of V_{GPIO}	70			%
	GPIO in low threshold	Percentage of V_{GPIO}			30	%
	GPIO in voltage range		0		3.3	V
V_{TX}	TX high voltage	Percentage of V_{GPIO}	70			%
	TX low voltage	Percentage of V_{GPIO}			30	%
	Configurable reset voltage	Percentage of V_{GPIO}	70			%

5.3 GPIO Connections

The GPIO connector is an optional galvanically isolated interface to external test equipment such as the testing fixture. The connector consists of one general purpose input and one general purpose output. The output does not supply its own power, it must be externally powered. The type of connector is a 4pin WR-TBL terminal block from Würth Elektronik (691313510004).

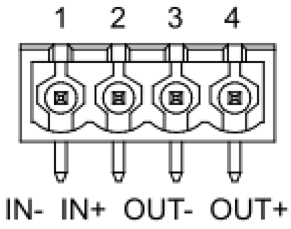


Figure 6. GPIO connector J10

Table 3. GPIO characteristics

Parameter	Description	Min	Typical	Max	Unit
V_{OUTPUT}	General purpose output voltage		24	80	V
I_{OUTPUT}	General purpose output current			5	mA
V_{INPUT}	General purpose input voltage	2		24	V

5.4 Daisy Chaining

The Connectivity PLT allows for up to four Connectivity PLT mainboards to be connected in a chain. Each Connectivity PLT board has a USB in (J17) and a USB out (J18). Each output connects to the next board's input, up to a maximum of four boards, see Figure 7. The USB must be chained from board to board and cannot be connected in any other way (such as through a hub). The power may however be connected as desired, if the requirements mentioned in Section 5.1 are met. Figure 8 shows an example of alternative power connections.

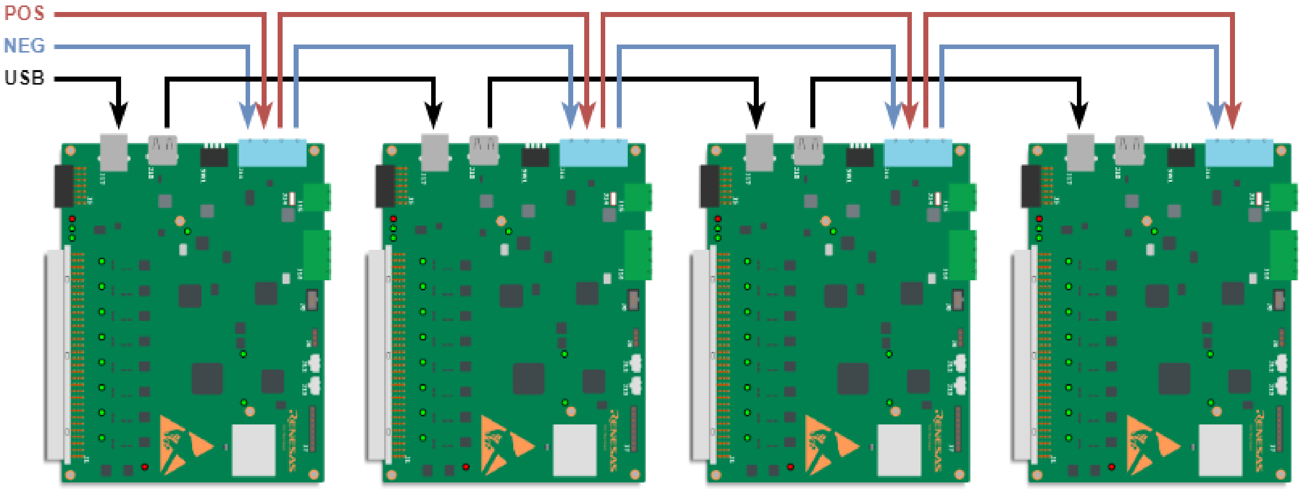


Figure 7. Connectivity PLT chain

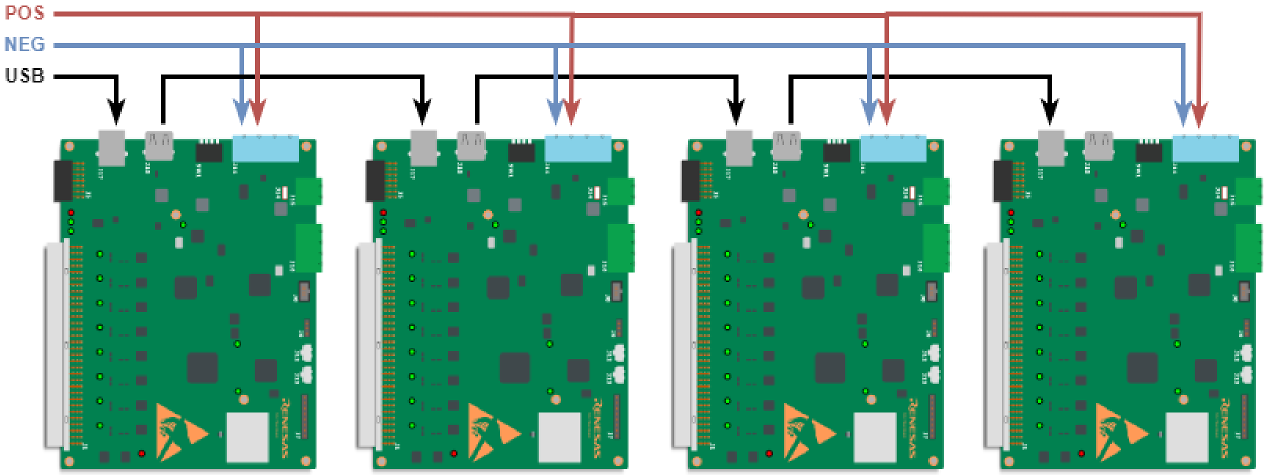


Figure 8. Connectivity PLT chain alternative

5.4.1 Addressing

When using multiple Connectivity PLT boards, the address on each of the boards needs to be set using DIP switches SW1. The switches are numbered, and the ON position is marked on the switch housing. The addressing is in binary format and switch number 1 is the least significant bit. For example, to set board number 3, switches 1 and 2 should be ON, and switches 3 and 4 should be OFF.

5.4.2 Sleep Current Measurement Using External DMM

Using externally connected current measurement equipment on J15, the Connectivity PLT can provide precise sleep current measurements for the DUTs. The current measurement is done on the VDUT rail so all DUT's are measured simultaneously. A jumper on J14 is used to bypass the external current measurement.

To set up the sleep current measurement with an external instrument, jumper J14 must be removed and a connection between J15 and the instrument needs to be made. Two wires from the positive and negative current measurement connections of the DMM must be connected to the terminal block for J15. The instrument must be NI VISA compatible through a USB connection or through a GPIB interface. The implemented protocol is compatible with Agilent/Keysight 3440x common among many DMMs.

The NI VISA drivers and software also need to be installed, see Section 6.4.

5.4.3 RFTUs

Radio Frequency Test Unit can be connected directly to PLT board on USB port.

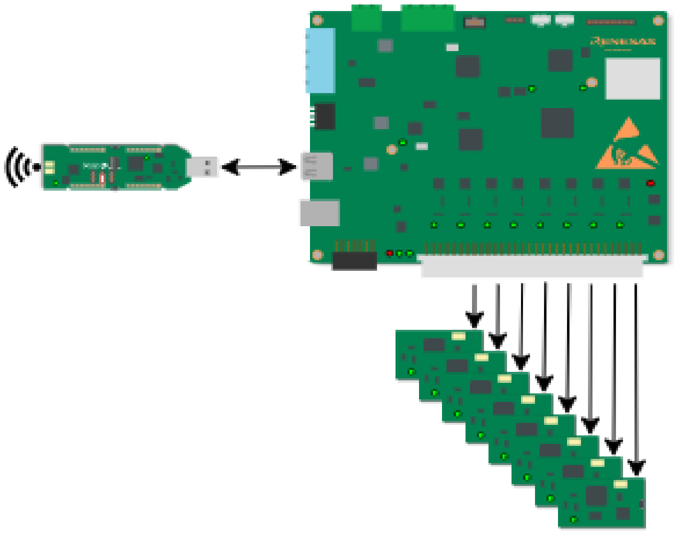


Figure 9. RFTU connected on PLT Board

If chaining is used, the RFTU can be connected to the last PLT board.

For combo devices, that support multiple protocols (for example, Wi-Fi and Bluetooth LE) different RFTUs are needed for each protocol. See an example of RFTU connections in Section 5.5.

5.5 Production Line Setup

To deploy the Connectivity PLT in a production environment, there are some considerations that must be made regarding the RF environment. If any RF tests are to be performed by the Connectivity PLT, there should be minimal background noise and interference. The recommended way to achieve this in any production environment is to place the Connectivity PLT main board(s), DUT's, and RF testing unit in a shielded box. Figure 10 shows a single board and single RFTU setup, and Figure 13. When multiple PLT main boards and multiple RFTUs are used, they can be set up in multiple shieled boxes (Figure 12) or a single shielded box (Figure 13).

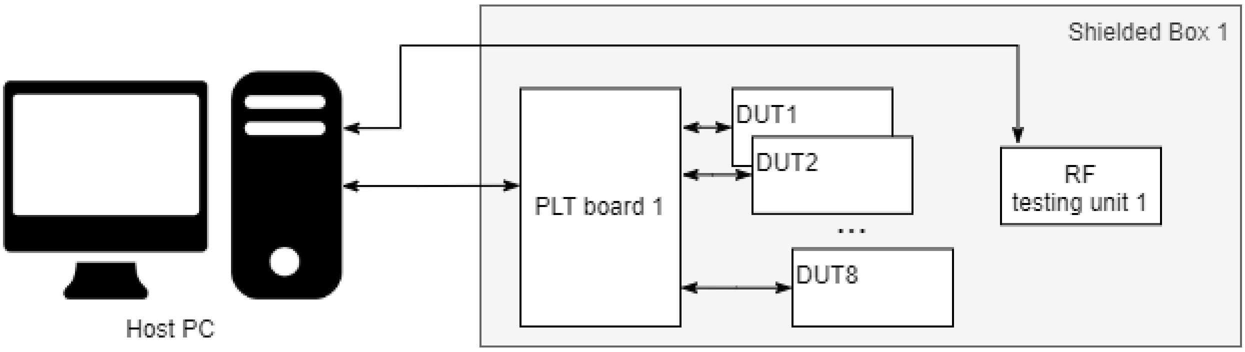


Figure 10. Connectivity PLT in a shielded box

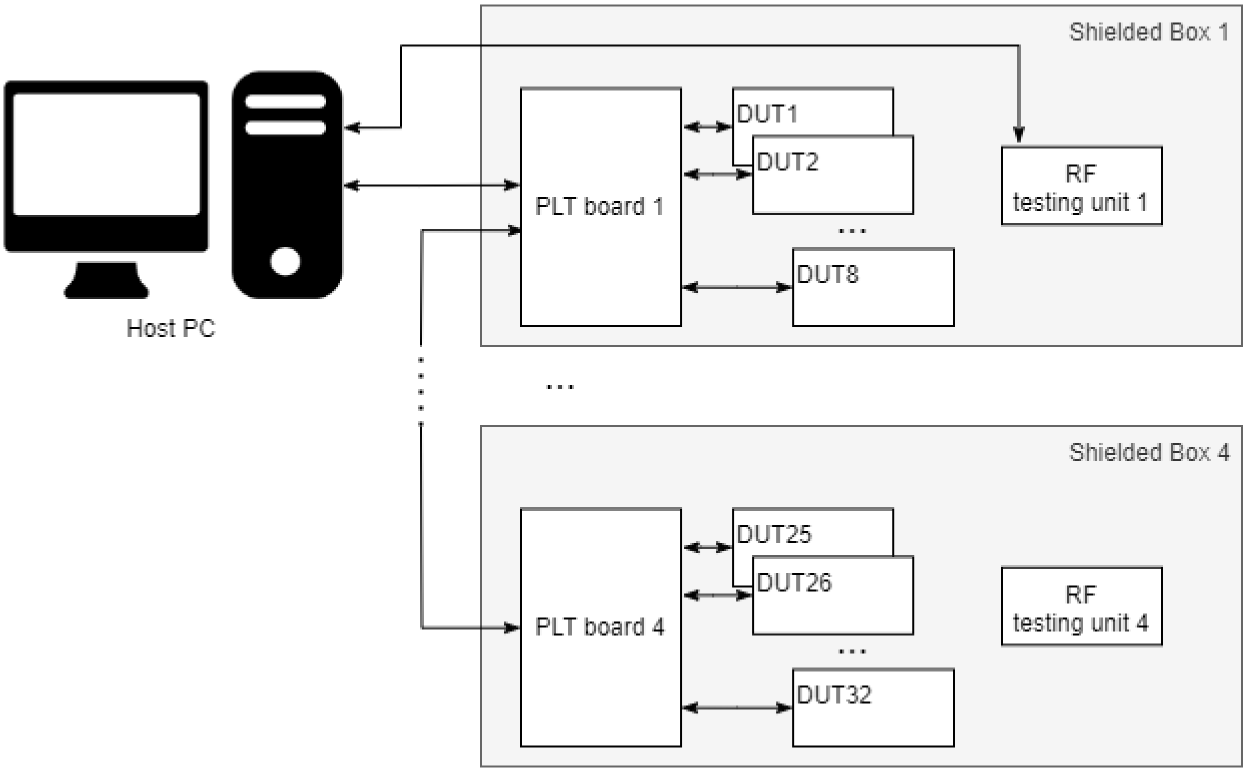


Figure 11. Connectivity PLT chain in multiple shielded boxes

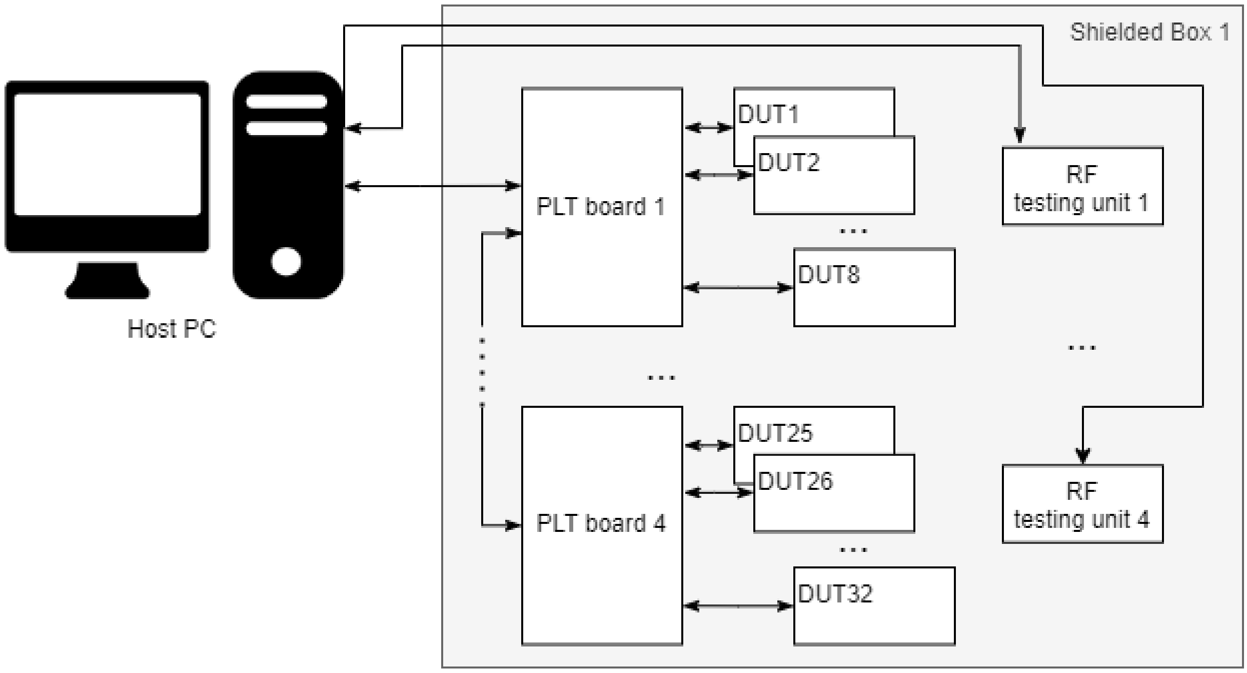


Figure 12. Connectivity PLT chain in single shielded box with multiple RF testing units

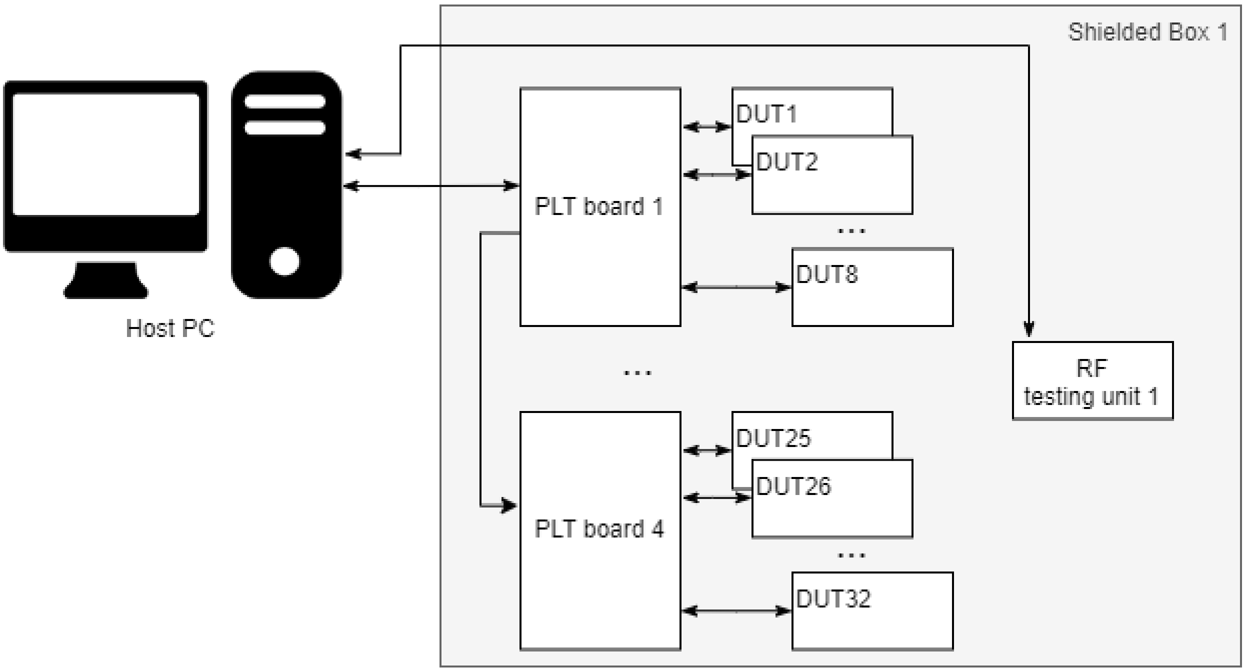


Figure 13. Connectivity PLT chain in single shielded box

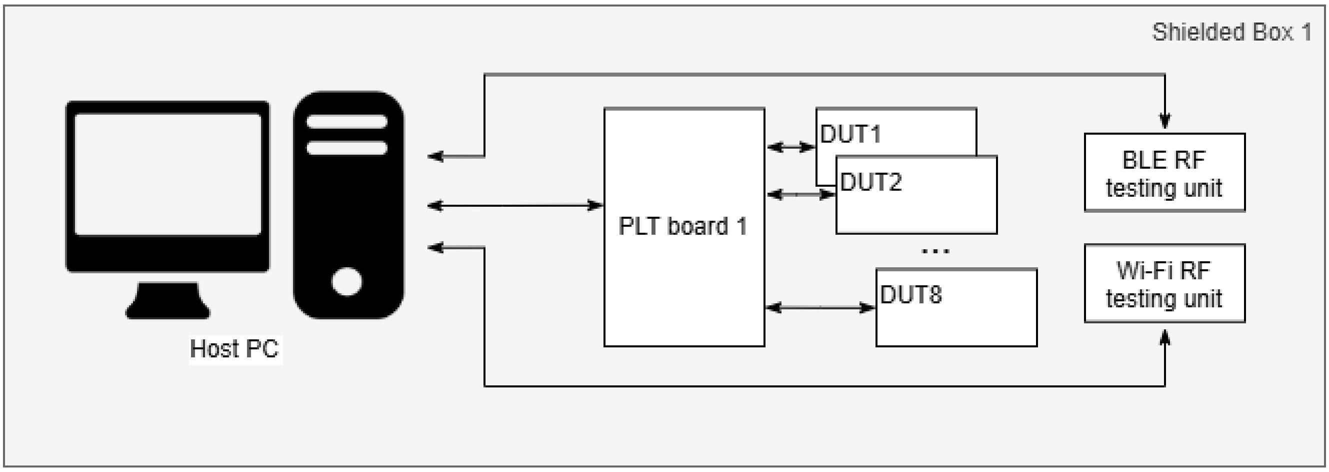


Figure 14. Connectivity PLT with Bluetooth LE and Wi-Fi RF testing units

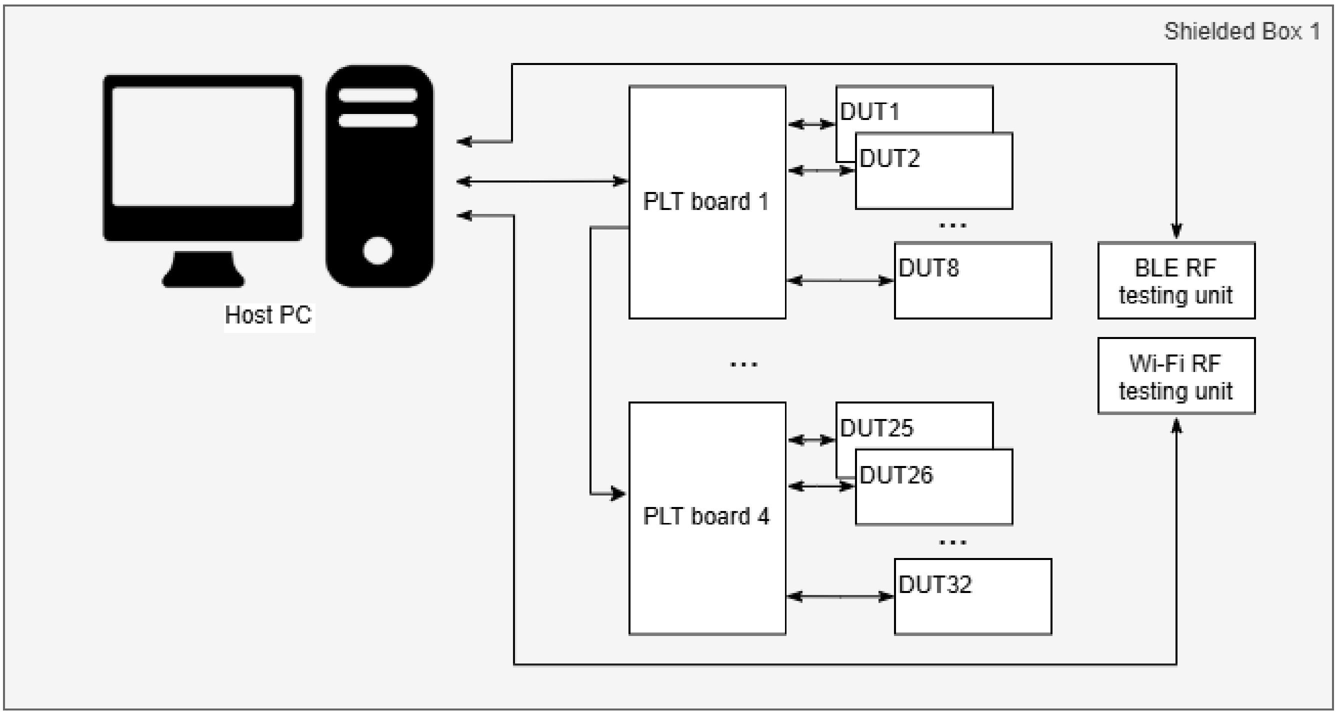


Figure 15. Connectivity PLT chain with Bluetooth LE and Wi-Fi RF testing units

6. Installation

6.1 Introduction

This section provides information on how to install the Connectivity PLT software. The Connectivity PLT is not a single application but a group of services and applications that can be installed on a single host or multiple networked machines. The installation process differs depending on the individual setup of the production line.

A single installer is used for all types of installation.

6.2 Architecture and Different Setup Strategies

The Connectivity PLT is split into two services and a few user interface applications, see Figure 16.

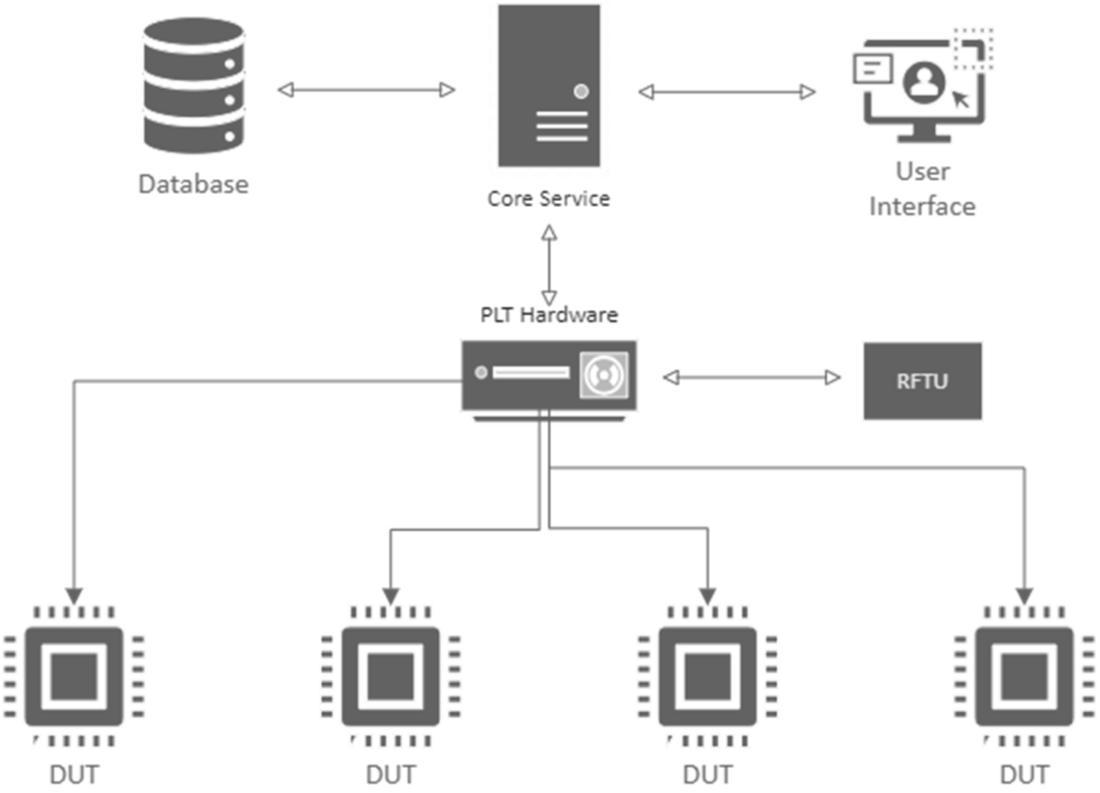


Figure 16. Connectivity PLT Architecture

6.2.1 PLT Services

The Connectivity PLT installer can install two Windows services:

- **The Renesas Connectivity PLT Database Service** – a host service for the main database that holds all the production related data such as serial numbers, BD addresses, test logs and results.
- **The Renesas Connectivity PLT Core Service** –the main service responsible for executing all operations at the host machine which has **a physical connection to the PLT hardware**.

These services can either be installed and run as windows services or can be manually started to run in a shell window and can be installed on the same system or on separate networked machines.

6.2.2 PLT Applications

- **Connectivity PLT** – the main application which provides the user interface to the Connectivity PLT execution. This application can run on a separate but networked system to the core service or locally at the same system.
- **Connectivity PLT CLI** – a command line interface with similar functionality to the main application but without a graphical user interface. This application can run on a separate but networked system to the core service or locally at the same system.
- **Connectivity PLT Configuration** – an application providing a user interface to configure every aspect of the PLT operation, including setup, tests, and programming. This application needs to run on the same system as the core service.
- **Connectivity PLT Service Agent** – a tray application providing access to the Core Service log when it is running as a windows service as well as a simple way to start and stop the windows service. This application needs to run on the same system as the core service.
- **Connectivity PLT Firmware Update** – an application providing an interface to update the Connectivity PLT firmware. This application needs to run on the same system that the hardware is connected to.

6.3 Installation

6.3.1 Standard Installation

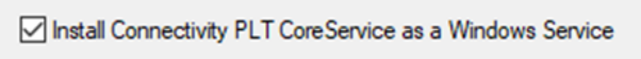
To install all applications and services of the Connectivity PLT on a single host system, run the installer with default selections and with the **Install Connectivity PLT CoreService as a Windows Service** checkbox selected.

It is strongly recommended to keep the installation folder in the default location. However, if it is necessary to change it, select a folder that does not require special permissions, for example, user folders or application folders. The windows services are executed from the SYSTEM account that does not have access to users' or some other special folders.

6.3.2 Remote System Installation

Installation of Core Service, Database Service, and Application can be installed on two or three separate remote systems.

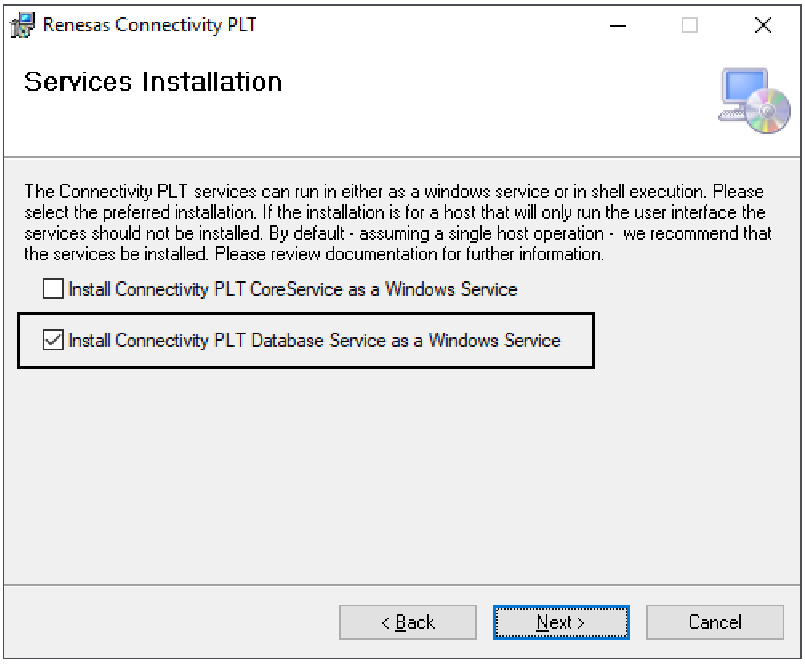
- **CoreService System** – this should be installed in the system that is physically connected to the Connectivity PLT hardware. The service can be installed by enabling the Renesas Connectivity PLT Core Service windows service checkbox in the installation wizard Figure 17. Take note of the IP address of the system, it is needed for the configuration of the Connectivity PLT application.



☑ Install Connectivity PLT CoreService as a Windows Service

Figure 17. CoreService Windows Service installation

- **Database Service System** – to use another host only as the database service, complete the installation enabling the Renesas Connectivity PLT Database Service Windows service during the installation and disabling the CoreService installation (Figure 18). Remember the IP address of this host as well.
  For the CoreService to communicate with the database on separate host, the configuration should be updated with the correct IP address or host name as shown in Figure 19.



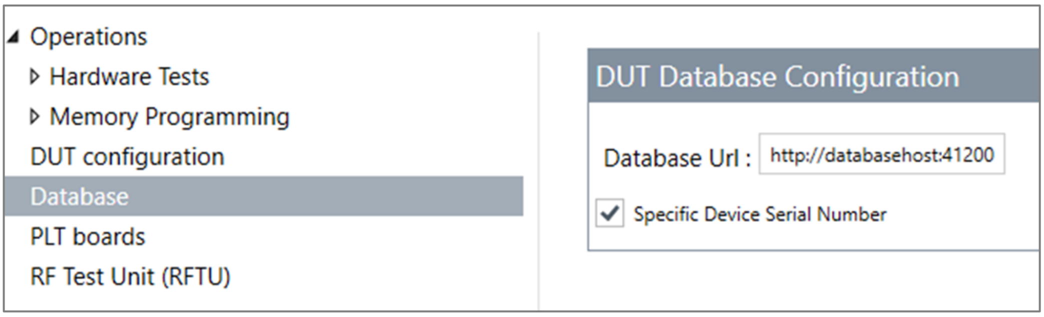
Services Installation

The Connectivity PLT services can run in either as a windows service or in shell execution. Please select the preferred installation. If the installation is for a host that will only run the user interface the services should not be installed. By default - assuming a single host operation - we recommend that the services be installed. Please review documentation for further information.

□ Install Connectivity PLT CoreService as a Windows Service

☑ Install Connectivity PLT Database Service as a Windows Service

Figure 18. Database Service Installation



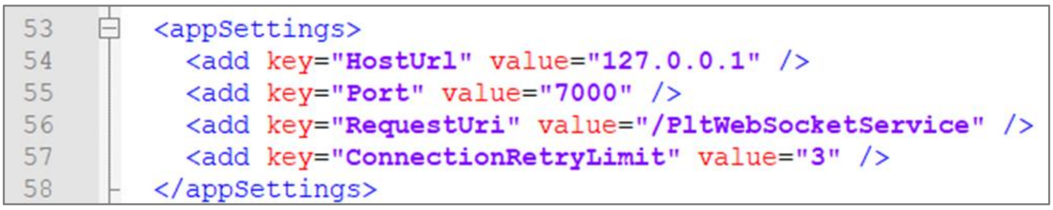
Database Url : http://databasehost:41200

☑ Specific Device Serial Number

Figure 19. Database Host configuration

- **Connectivity PLT Application** (main application system) – the third system can be used as an operators' console which is, for example, located further away from the hardware. For this instance, during the installation, no services should be selected.

  To set up the system in a distributed architecture, the configuration needs to be updated of the main application to use the correct IP address of the CoreService. Go to the `C:\Renesas Electronics\Renesas Connectivity PLT\ Renesas_Connectivity_PLT.exe.config` file and update the `HostUrl` value to the correct IP address of the CoreService host as shown in Figure 20.



```
<appSettings>
  <add key="HostUrl" value="127.0.0.1" />
  <add key="Port" value="7000" />
  <add key="RequestUri" value="/PltWebSocketService" />
  <add key="ConnectionRetryLimit" value="3" />
</appSettings>
```

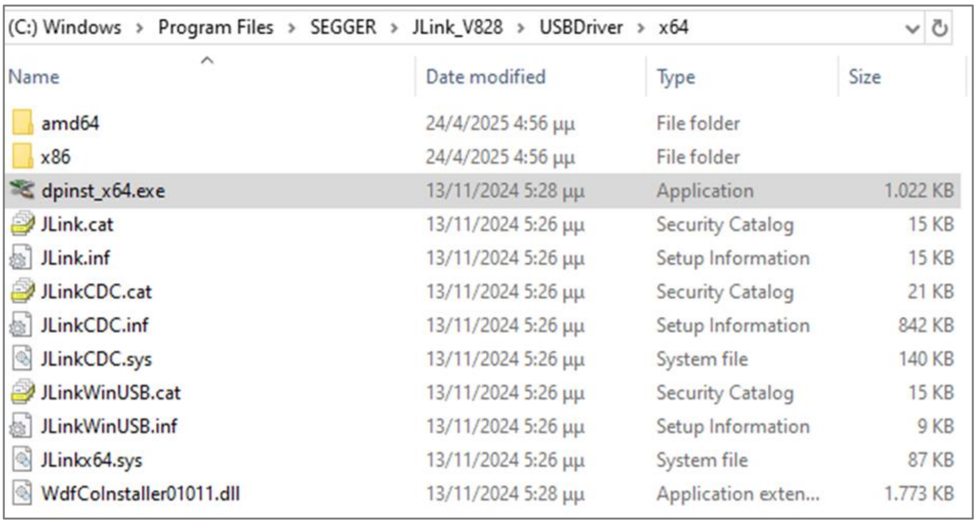
Figure 20. Main Application CoreService Host configuration

6.4 Install Necessary Drivers

Due to licensing restrictions, some drivers cannot be included in the installation package. You need to manually download and install these drivers.

- **Segger J-Link driver** – can be installed as part of the Segger J-Link Application installation. You can download the driver from https://www.segger.com/downloads/jlink/.

If the installer is launched from a restricted account, you need to run the driver installer manually as an administrator. The driver installer is in the installation folder of the JLink application. (Figure 21).



(C:) Windows › Program Files › SEGGER › JLink_V828 › USBDriver › x64

Name	Date modified	Type	Size
amd64	24/4/2025 4:56 μμ	File folder	
x86	24/4/2025 4:56 μμ	File folder	
dpinst_x64.exe	13/11/2024 5:28 μμ	Application	1.022 KB
JLink.cat	13/11/2024 5:26 μμ	Security Catalog	15 KB
JLink.inf	13/11/2024 5:26 μμ	Setup Information	15 KB
JLinkCDC.cat	13/11/2024 5:26 μμ	Security Catalog	21 KB
JLinkCDC.inf	13/11/2024 5:26 μμ	Setup Information	842 KB
JLinkCDC.sys	13/11/2024 5:26 μμ	System file	140 KB
JLinkWinUSB.cat	13/11/2024 5:26 μμ	Security Catalog	15 KB
JLinkWinUSB.inf	13/11/2024 5:26 μμ	Setup Information	9 KB
JLinkx64.sys	13/11/2024 5:26 μμ	System file	87 KB
WdfCoInstaller01011.dll	13/11/2024 5:28 μμ	Application exten...	1.773 KB

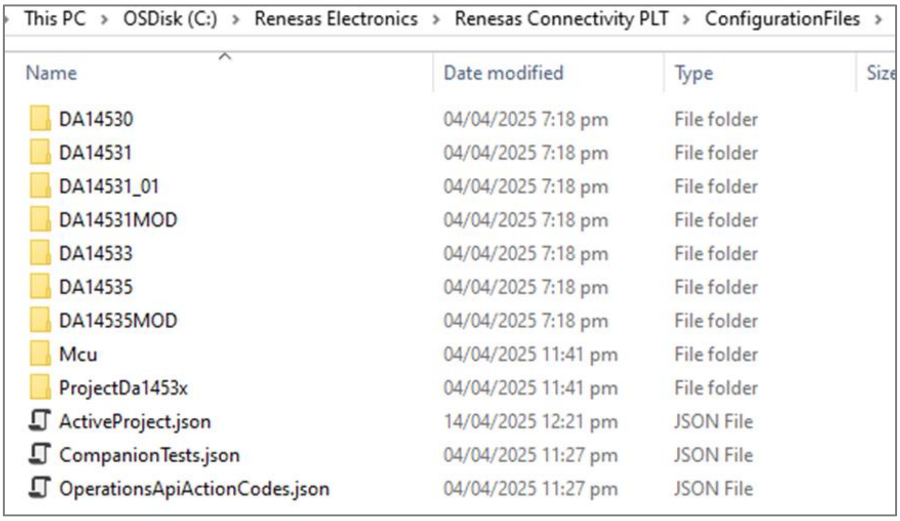
Figure 21. Jlink driver installer

- **NI Visa drivers** - if an external DMM or other instruments are used for tests, then NI Visa drivers are required. You can download the drivers from https://www.ni.com/en/support/downloads/drivers/download.ni-visa.html#558610.
- **Microchip SAM-BA driver** – used for updating the firmware of the connectivity PLT hardware. You can download the driver from https://www.microchip.com/en-us/development-tool/sam-ba-in-system-programmer.

6.5 Update and Uninstall

To update to the newest version of the Connectivity PLT, first uninstall the previous version, and then install the needed version.

The pre-generated project files are not removed from the installation folder during the uninstall process. However, remember to keep a backup of the Configuration files, when new configuration files are introduced during the installation the old ones are going to be deleted. Figure 22 shows an example of configuration files and folders that should be backed up.



This PC › OSDisk (C:) › Renesas Electronics › Renesas Connectivity PLT › ConfigurationFiles ›

Name	Date modified	Type	Size
DA14530	04/04/2025 7:18 pm	File folder	
DA14531	04/04/2025 7:18 pm	File folder	
DA14531_01	04/04/2025 7:18 pm	File folder	
DA14531MOD	04/04/2025 7:18 pm	File folder	
DA14533	04/04/2025 7:18 pm	File folder	
DA14535	04/04/2025 7:18 pm	File folder	
DA14535MOD	04/04/2025 7:18 pm	File folder	
Mcu	04/04/2025 11:41 pm	File folder	
ProjectDa1453x	04/04/2025 11:41 pm	File folder	
ActiveProject.json	14/04/2025 12:21 pm	JSON File	
CompanionTests.json	04/04/2025 11:27 pm	JSON File	
OperationsApiActionCodes.json	04/04/2025 11:27 pm	JSON File	

Figure 22. Configuration files

7. Database Service

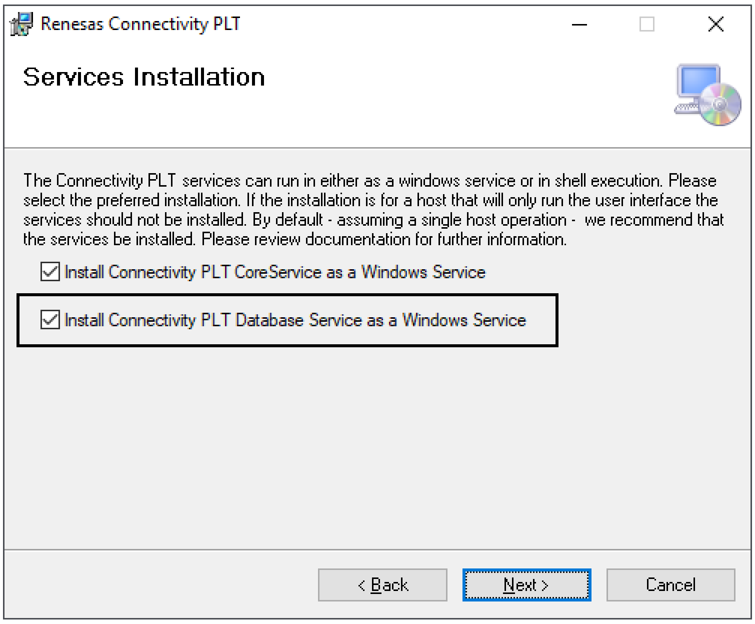
The Renesas Connectivity PLT Database Service provides access to the database holding the product information as well as other details through a network interface (web service). It is used by the Connectivity PLT to identify serial numbers matched to BD addresses, store information about the test process and results, and retrieve data that is required to be written to the DUTs storage (eFlash, OTP, external Flash, EEprom).

7.1 Installation

Installation of the Renesas Connectivity PLT Database Service, can be achieved using the same Connectivity PLT Installer.

The database service can be installed as a Windows service, using the same Connectivity PLT installer, and run in the background. Alternatively, it can be executed from a shell window with administrator privileges. It can be installed on the same host system as the one that executes the core service or on a remote system, if it is accessible over the network.

It is strongly recommended that it is installed as a service, in which instance no interaction with the user is required to access the database, it automatically starts during power up in the background with the correct privileges.



The Connectivity PLT services can run in either as a windows service or in shell execution. Please select the preferred installation. If the installation is for a host that will only run the user interface the services should not be installed. By default - assuming a single host operation - we recommend that the services be installed. Please review documentation for further information.

☑ Install Connectivity PLT CoreService as a Windows Service

☑ Install Connectivity PLT Database Service as a Windows Service

Figure 23. Database Service Installation

By default, the entire Connectivity PLT folder structure is installed on `C:\Renesas Electronics\Renesas Connectivity PLT`. The `database.db` file is in the `Database` folder in the root folder of the installation, and the database service is configured to locate the database at this location.

If you have changed the installation folder or want to move the database to another location, do the following:

1. Open the `DatabaseService\bin\Renesas_Connectivity_Plt_Database_Service.exe.config` file using a text editor.
2. Locate the following entry

```
<connectionStrings>
        <add name="DevicesDatabase" providerName="System.Data.SQLite" connectionString="Data Source=C:\Renesas Electronics\Renesas Connectivity PLT\Database\DevicesDatabase.db; Integrated Security=True" />
 </connectionStrings>
```

   and then change the `DataSource` property to the correct location of the database file.

3. Save the file and restart the service.

7.2 Database Structure

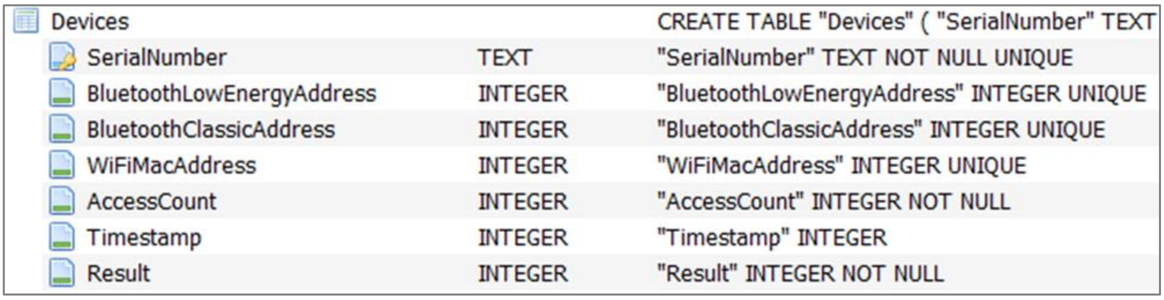
The database contains a few different tables to hold all the necessary information.

7.2.1 Devices Table

The Devices table is the main table storing the list of serial numbers and corresponding BD addresses. After the installation, the database already contains some data for testing and demonstration purposes. Before going into production, you need to replace this data with the serial numbers and board addresses range based on your specific needs.

To manage the database directly, use SQLite tool (https://sqlitebrowser.org/).

Figure 24 shows the database devices table structure in the SQLite tool.



Devices		CREATE TABLE "Devices" ("SerialNumber" TEXT
SerialNumber	TEXT	"SerialNumber" TEXT NOT NULL UNIQUE
BluetoothLowEnergyAddress	INTEGER	"BluetoothLowEnergyAddress" INTEGER UNIQUE
BluetoothClassicAddress	INTEGER	"BluetoothClassicAddress" INTEGER UNIQUE
WiFiMacAddress	INTEGER	"WiFiMacAddress" INTEGER UNIQUE
AccessCount	INTEGER	"AccessCount" INTEGER NOT NULL
Timestamp	INTEGER	"Timestamp" INTEGER
Result	INTEGER	"Result" INTEGER NOT NULL

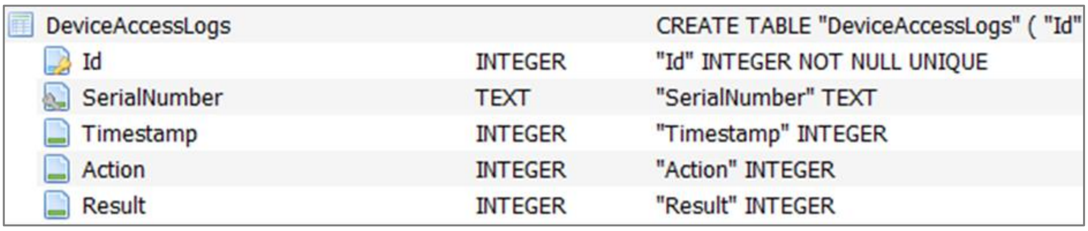
Figure 24. Database Devices table structure

- Serial Number - text field, must contain text representing the serial number, it must be unique, is the index
- BluetoothLowEnergyAddress - integer field, contains the entire Bluetooth LE address as a 64-bit integer
- BluetoothClassAddress - integer field, contains the entire Bluetooth Classic address as a 64bit integer. (only used in devices that support classic Bluetooth)
- WiFiMacAddress - integer filed, contains the entire MAC address as a 64-bit integer (only used in devices that support Wi-Fi).
- AccessCount - integer filed, contains a counter signifying how many times this entry is accessed by the Connectivity PLT
- Timestamp - integer field, a timestamp of the last access represented in unix timestamp format
- Result - integer filed, represents the results of the last test run on the Connectivity PLT.

7.2.2 Device Access Logs Table

The DeviceAccessLogs table holds information about every time the Connectivity PLT has accessed each device entry based on the serial number (index). This table should not be changed by any external processes or manually.

Figure 25 shows the Device Access Logs table structure in the SQLite tool.



DeviceAccessLogs		CREATE TABLE "DeviceAccessLogs" ("Id"
Id	INTEGER	"Id" INTEGER NOT NULL UNIQUE
SerialNumber	TEXT	"SerialNumber" TEXT
Timestamp	INTEGER	"Timestamp" INTEGER
Action	INTEGER	"Action" INTEGER
Result	INTEGER	"Result" INTEGER

Figure 25. Database Device Access Logs table structure

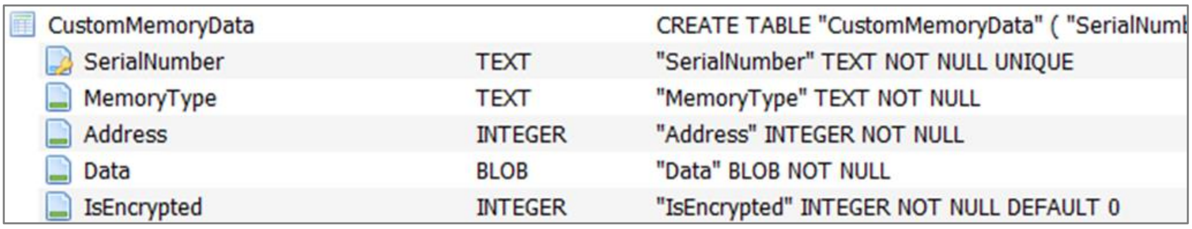
- Id - integer field, a unique ID of the entry (index)
- SerialNumber - text field, Reference to the Devices Table of the entry
- Timestamp - integer field, a timestamp at the time of access represented in unix timestamp format
- Action - integer field, an enumeration of the Connectivity PLT action log entry.

- Result - integer field, the result of the action.

7.2.3 Custom Memory Data Table

The CustomMemoryData table contains data to be stored on the DUT tied to a specific serial number. This can be useful, for example, to store the serial number and other information that is unique to each device. For every continuous sequence of data a new entry should be made, multiple entries can exist for each serial number, each entry is programmed at the specified memory type and address specified. The write process is enabled during the configuration of the testing.

Figure 26 shows the Custom Memory Data table structure in the SQLite tool.



CustomMemoryData		CREATE TABLE "CustomMemoryData" ("SerialNumb
SerialNumber	TEXT	"SerialNumber" TEXT NOT NULL UNIQUE
MemoryType	TEXT	"MemoryType" TEXT NOT NULL
Address	INTEGER	"Address" INTEGER NOT NULL
Data	BLOB	"Data" BLOB NOT NULL
IsEncrypted	INTEGER	"IsEncrypted" INTEGER NOT NULL DEFAULT 0

Figure 26. Database Custom Memory data table

- SerialNumber - text, Reference to the Devices Table of the entry
- Memory Type - text, specifies the type of memory that the data should be stored at
  - SpiFlash
  - Otp
- Address - integer, the memory address at which the data should begin to be stored
- Data - blob, the data stored in binary format.
- IsEncrypted - integer, specifies if the data entry is encrypted (1) or not (0).

Example of storing:

- Data of a random 32 bit number at adress 0x10000 of the SPI Flash
- and the serial number at address 0x200000.

Entry 1

- SerialNumber: 0x12345678
- MemoryType: SpiFlash
- Address: 0x10000
- Data: [random number in binary blob]
- IsEncrypted: 0

Entry 2

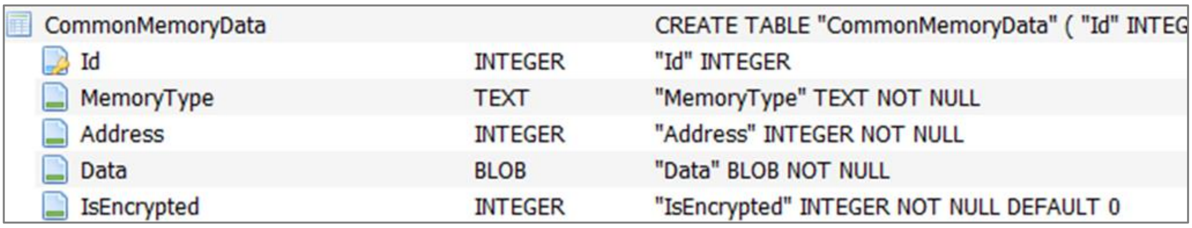
- SerialNumber: 0x12345678
- MemoryType: SpiFlash
- Address: 0x200000
- Data: [serial number in binary blob]
- IsEncrypted: 0

Another example of a different binary file loaded to the OTP for each serial number:

- SerialNumber: 0x12345678
- MemoryType: Otp
- Address: 0x1000
- Data: [0x12345678.bin]
- IsEncrypted: 0

7.2.4 Common Memory Data Table

The CommonMemoryData table contains data to be stored on every DUT. This can be useful for storing data for all the devices regardless of their serial number. For every continuous sequence of data a new entry should be made, each entry is programmed at the specified memory type and address specified. The write process is enabled during the configuration of the testing.



CommonMemoryData		CREATE TABLE "CommonMemoryData" ("Id" INTEG
Id	INTEGER	"Id" INTEGER
MemoryType	TEXT	"MemoryType" TEXT NOT NULL
Address	INTEGER	"Address" INTEGER NOT NULL
Data	BLOB	"Data" BLOB NOT NULL
IsEncrypted	INTEGER	"IsEncrypted" INTEGER NOT NULL DEFAULT 0

Figure 27. Database Common Memory Data table structure

- Memory Type - Text, specifies the type of memory that the data should be stored at
  - SpiFlash
  - OTP
- Address - Integer, the memory address at which the data should begin to be stored
- Data - Blob, the data stored in binary format.
- IsEncrypted - Integer, specifies if the data entry is encrypted (1) or not (0).

Example of setting that is common on all devices stored in SPI flash:

- MemoryType: SpiFlash
- Address: 0x10000
- Data: [0x01 0x02 0x03 0x04]
- IsEncrypted: 0

7.3 Data Encryption

A basic encryption method is implemented for the data stored in the database. The data should be encrypted before storing them into the database.

The encryption method is AES on a 256-bit key.

The key for decryption is stored in `C:\Renesas Electronics\Renesas Connectivity PLT\DatabaseService\bin\ Renesas_Connectivity_Plt_Database_Service.exe.config`.

In the appSettings section, entry: <add key="decryptionKey" value="1234567" />

This should be changed to the key used for the encryption for the PLT to be able to decrypt and store the data.

8. Connectivity PLT Configuration

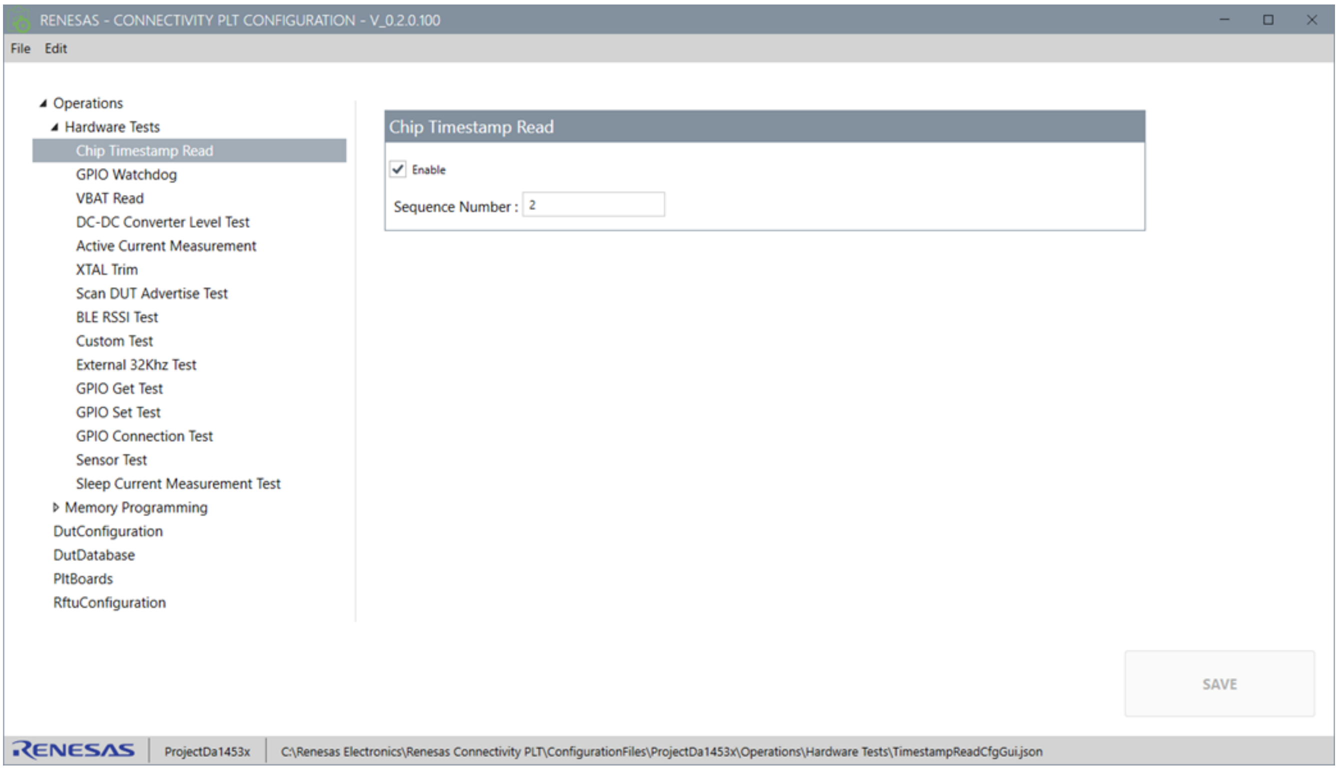
The Renesas Connectivity PLT Configuration is used to set up the system according to the device hardware options and select the required tests and memory actions to be performed.

The Connectivity PLT Configuration application (`Renesas_Connectivity_PLT_Configuration.exe`) is an application, which is used to appropriately configure the tests and memory operations the tool performs. Depending on the selected device chipset and the enabled actions, only appropriate options are enabled and shown. Any change made is validated before being saved to the JSON file. This prevents erroneous values from being stored in the JSON file that would harm the production procedure.

8.1 Connectivity PLT Configuration Window

The tree list in the side navigation is automatically created based on the folder structure in `ConfigurationFiles` folder in the application folder. Folders become parent items, and the contents (JSON configuration files) become child items. Clicking on a tree item either expands the contents of the folder or displays the configuration parameters of the file. If there is an error in any of the configuration JSON files, a warning message is shown indicating which of the parameters has an error.

Figure 28 shows the initial Connectivity PLT Configuration window with the first configuration item in the tree menu on the left.



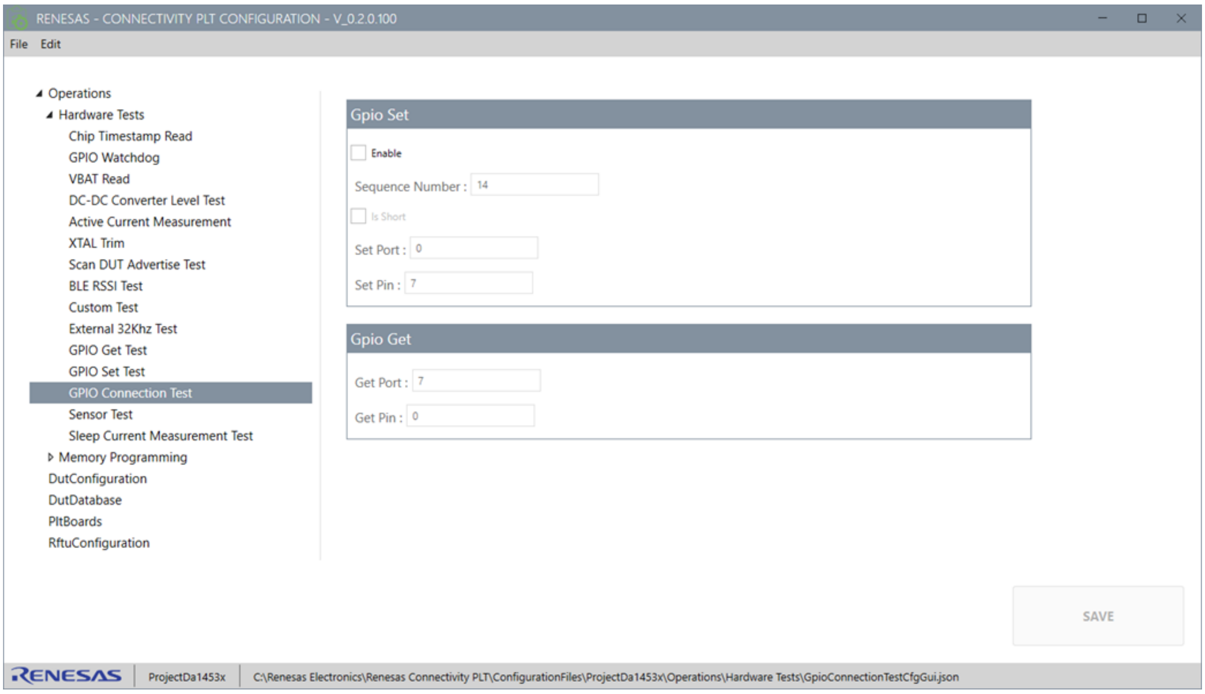
☑ Enable

Sequence Number : 2

ProjectDa1453x

C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\ProjectDa1453x\Operations\Hardware Tests\TimestampReadCfgGui.json

Figure 28. Start window



Gpio Set

□ Enable

Sequence Number : 14

□ Is Short

Set Port : 0

Set Pin : 7

Gpio Get

Get Port : 7

Get Pin : 0

ProjectDa1453x

C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\ProjectDa1453x\Operations\Hardware Tests\GpioConnectionTestCfgGui.json

Figure 29. Tree menu

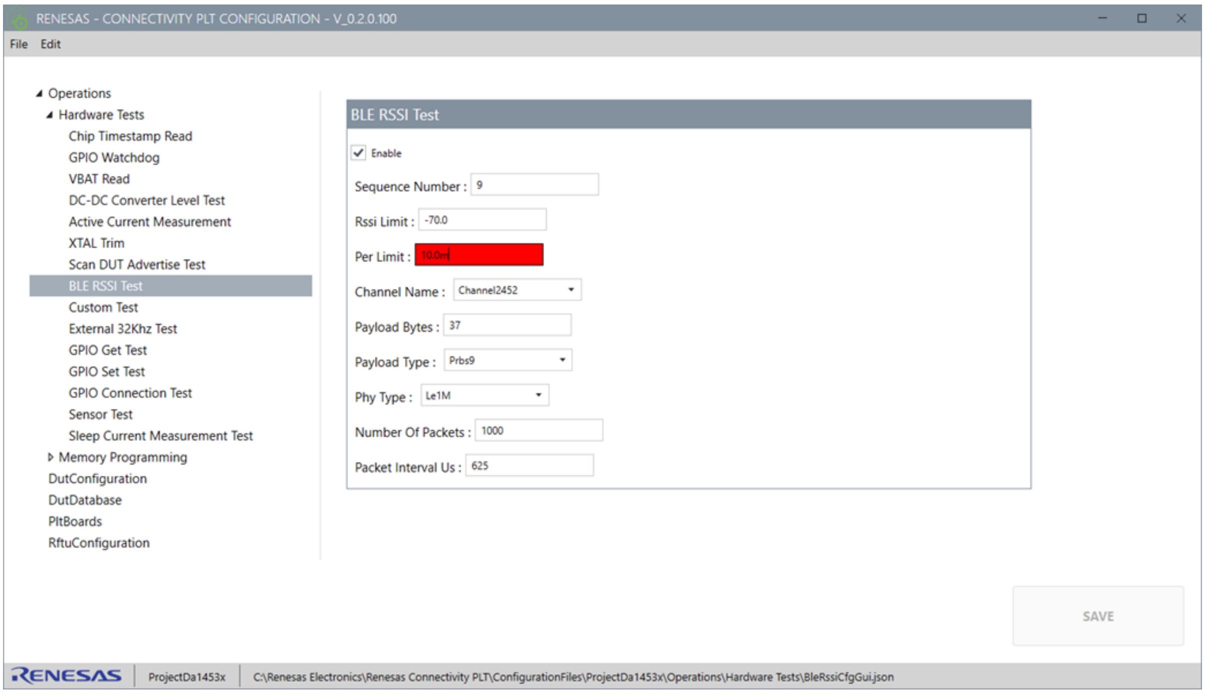
You can use menu options to manage projects: create new ones, open, save, reload or edit.

At the bottom of the window, you can see the location path of the current selected JSON configuration file.

The save button is disabled on startup. After you make a change in any field in JSON configuration files, the save button turns red with an asterisk and the option to save the changes is available. An asterisk also appears on title bar and on windows taskbar. You must save your changes before opening another file.

The parameter fields have a tooltip describing the field and the expected values.

All the parameter fields are protected by regex validation customized to the contents of each field. If an unsupported value or character is inserted, the field turns red and the save button is disabled again until a valid value is entered, Figure 30.



BLE RSSI Test

☑ Enable

Sequence Number : 9

Rssi Limit : -70.0

Per Limit : 10.0m

Channel Name : Channel2452

Payload Bytes : 37

Payload Type : Prbs9

Phy Type : Le1M

Number Of Packets : 1000

Packet Interval Us : 625

ProjectDa1453x

C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\ProjectDa1453x\Operations\Hardware Tests\BleRssiCfgGui.json

Figure 30. Input error

8.2 Configurations

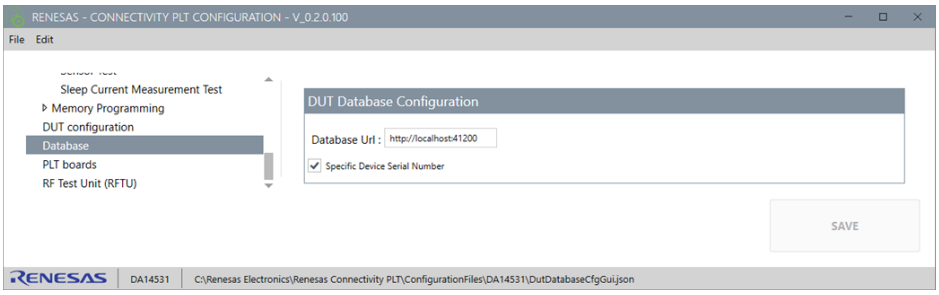
8.2.1 Project Configuration

You can save information into projects to easily switch between different test procedures or devices in the Connectivity PLT. Each project is a set of configuration files stored in a separate folder named as the project. By default, when Connectivity PLT is installed, a few projects representing different ICs are created automatically.

To create a new project configuration, go to **File**> **Create New Project**. In the **Create New Project** dialog, select a base project that is used as a starting point, and add project name. All the necessary files are copied to the new project folder under `ConfigurationFiles` folder and side navigation refreshes displaying the new project.

8.2.2 Database Configuration

Database configuration is used to store serial numbers, Bluetooth LE addresses, BT classic addresses, Wi-Fi mac addresses; information used in testing, such as common memory data and custom memory data, and statistics like passed/failed tests, access count, timestamps. If the Connectivity PLT Database Service is installed on a separate machine you need to set the correct URL and port to point to this machine.



RENESAS - CONNECTIVITY PLT CONFIGURATION - V_0.2.0.100

DUT Database Configuration

Database Url : http://localhost:41200

☑ Specific Device Serial Number

DA14531

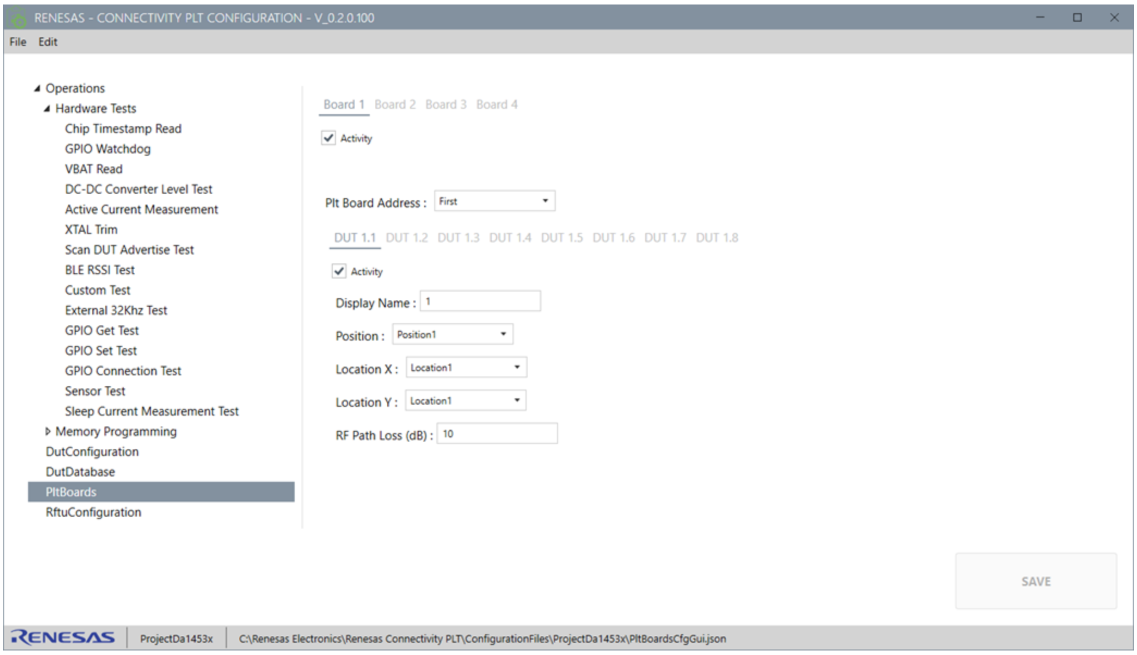
C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531\DutDatabaseCfgGui.json

Figure 31. Database configuration

The Connectivity PLT used the database to assign BD addresses based on serial numbers previously entered in the database. The option to have Specific Device Serial Number enables a dialog to appear at the beginning of the test procedure to enter the serial number of the first DUT. This is usually done using a barcode scanner. For more details, see Section 7.

8.2.3 PLT Boards Configuration

The Connectivity PLT boards configuration has four available Connectivity PLT boards, and you can enable them and assign a location in the chain, see Figure 32. For each Connectivity PLT board, there are eight available test positions. For the minimum configuration, you must enable at least one Connectivity PLT board and one DUT.



☑ Activity

Plt Board Address : First

☑ Activity

Display Name : 1

Position : Position1

Location X : Location1

Location Y : Location1

RF Path Loss (dB) : 10

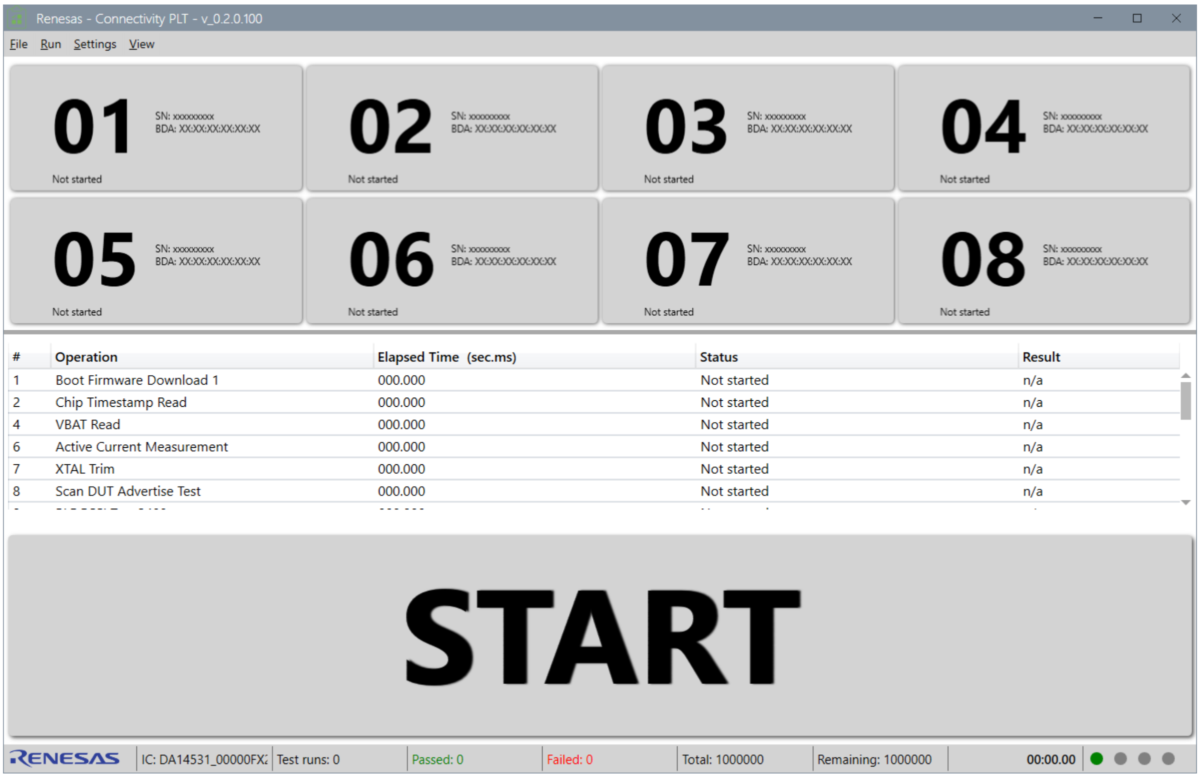
ProjectDa1453x | C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\ProjectDa1453x\PltBoardsCfgGui.json

Figure 32. PltBoards configuration

Table 4. PltBoards parameters

Parameter	Description
PLT Board	
Activity	Enables or disables the usage of the specific PLT Board.
PLT Board Number	Sets the PLT Board number (Zero, First, Second, Third).
PLT Board Address	Sets the address of the PLT Board (First, Second, Third, Fourth).
DUT	
Activity	Enables or disables the usage of the specific DUT.
Display Name	The name of each DUT in the testing environment.
Position	The position of each DUT on the PLT Board.
Location X	The location of each DUT, in X axis, in the testing environment grid.
Location Y	The location of each DUT, in Y axis, in the testing environment grid.
RF Path Loss (db)	The value to be used in RF Path Loss, in dBm.

Location X/Y adjusts the view of the DUT tiles in the testing environment to simulate the actual hardware layout. Each DUT can be placed wherever needed in the Execution GUI grid. Figure 33 and Figure 34 show examples of two different views on the testing environment by adjusting Position X and Position Y.

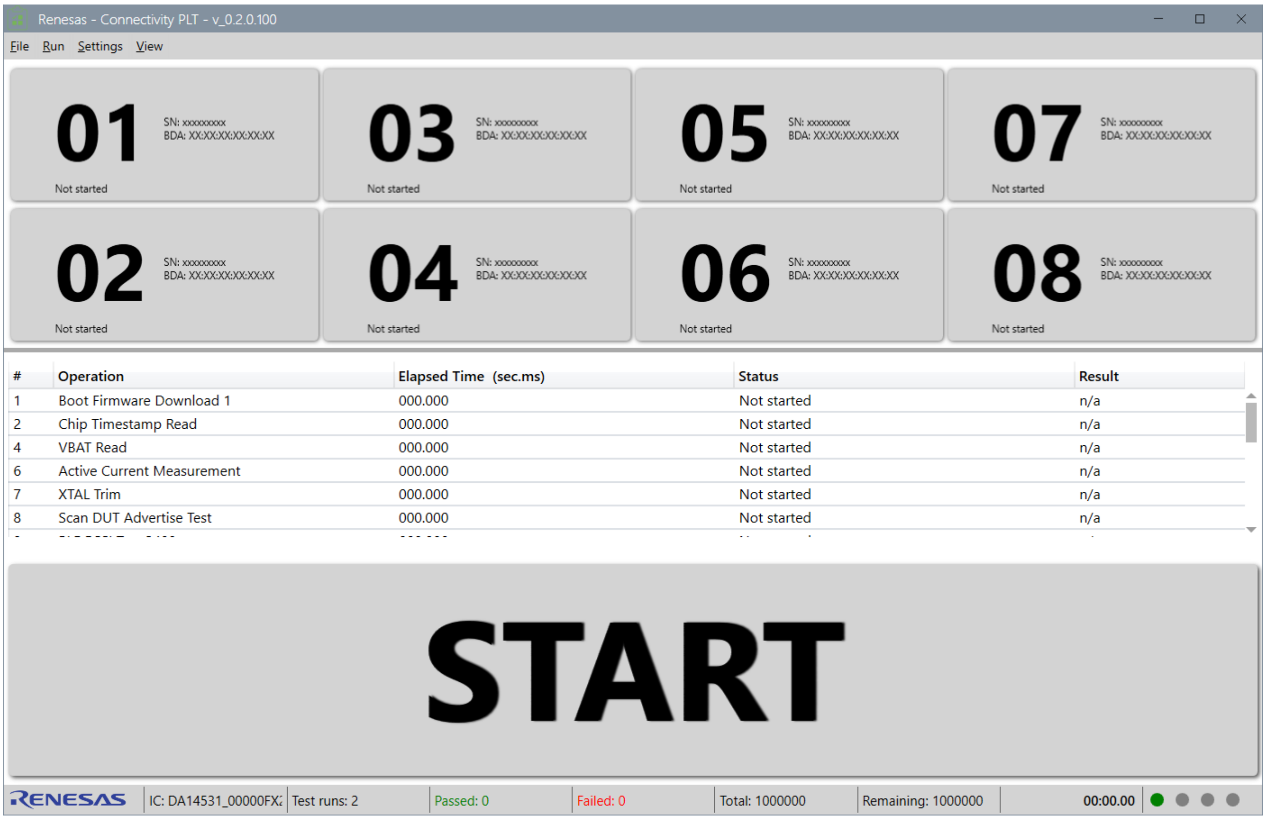


01 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started
02 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started
03 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started
04 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started
05 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started
06 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started
07 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started
08 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started

#	Operation	Elapsed Time (sec.ms)	Status	Result
1	Boot Firmware Download 1	000.000	Not started	n/a
2	Chip Timestamp Read	000.000	Not started	n/a
4	VBAT Read	000.000	Not started	n/a
6	Active Current Measurement	000.000	Not started	n/a
7	XTAL Trim	000.000	Not started	n/a
8	Scan DUT Advertise Test	000.000	Not started	n/a

IC: DA14531_00000FX | Test runs: 0 | Passed: 0 | Failed: 0 | Total: 1000000 | Remaining: 1000000 | 00:00.00

Figure 33. Default tile configuration



01 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started
03 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started
05 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started
07 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started
02 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started
04 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started
06 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started
08 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started

#	Operation	Elapsed Time (sec.ms)	Status	Result
1	Boot Firmware Download 1	000.000	Not started	n/a
2	Chip Timestamp Read	000.000	Not started	n/a
4	VBAT Read	000.000	Not started	n/a
6	Active Current Measurement	000.000	Not started	n/a
7	XTAL Trim	000.000	Not started	n/a
8	Scan DUT Advertise Test	000.000	Not started	n/a

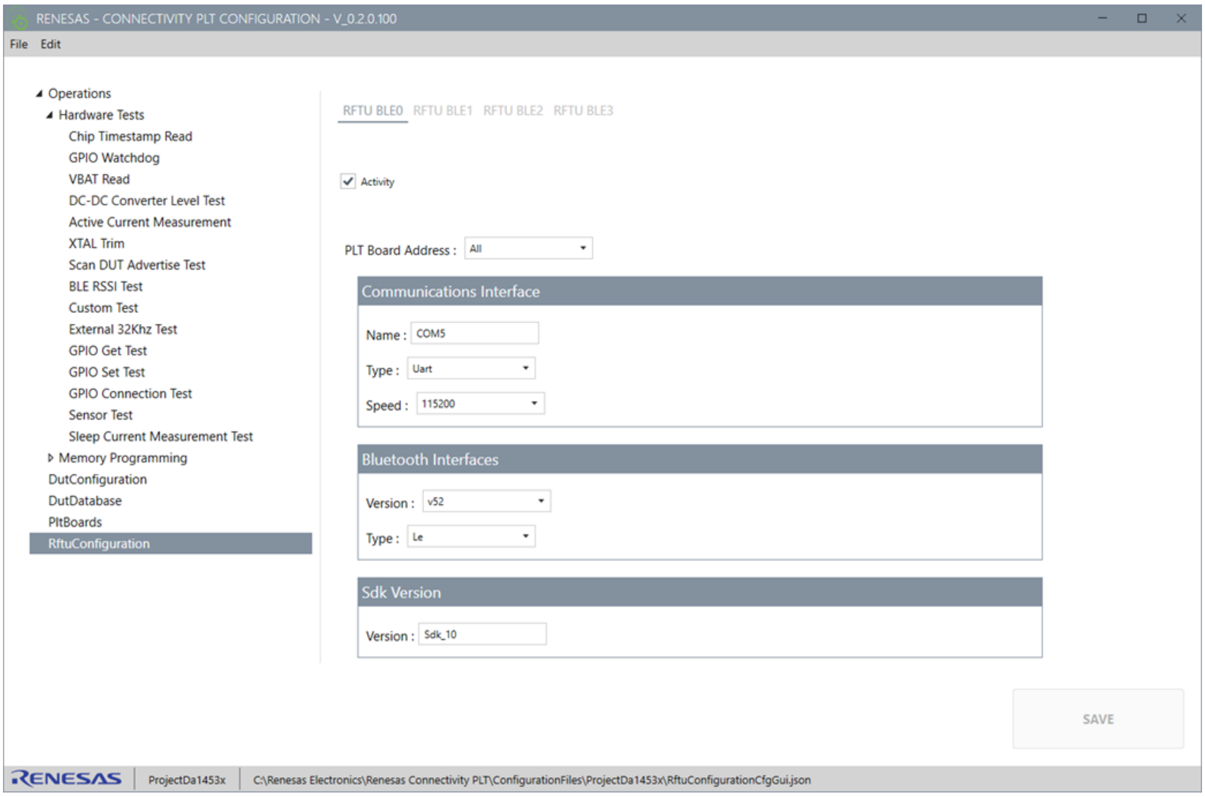
IC: DA14531_00000FX | Test runs: 2 | Passed: 0 | Failed: 0 | Total: 1000000 | Remaining: 1000000 | 00:00.00

Figure 34. 2-row tile configuration

8.2.4 RFTU Bluetooth LE Configuration

The Connectivity PLT system can be configured to use one or multiple RFTUs. Multiple RTFUs can be used for cases when the multiple boards exist on the chain and are separated by distance or other RF blocking methods.

Different RFTU configurations are available. At a minimum one RFTU is necessary when RF tests are going to be performed during the test process. Figure 35 demonstrates the default and minimum RFTU configuration. The communications Interface name be se set to empty to be automatically detected.



☑ Activity

PLT Board Address : All

Communications Interface

Name : COM5

Type : Uart

Speed : 115200

Bluetooth Interfaces

Version : v52

Type : Le

Sdk Version

Version : Sdk_10

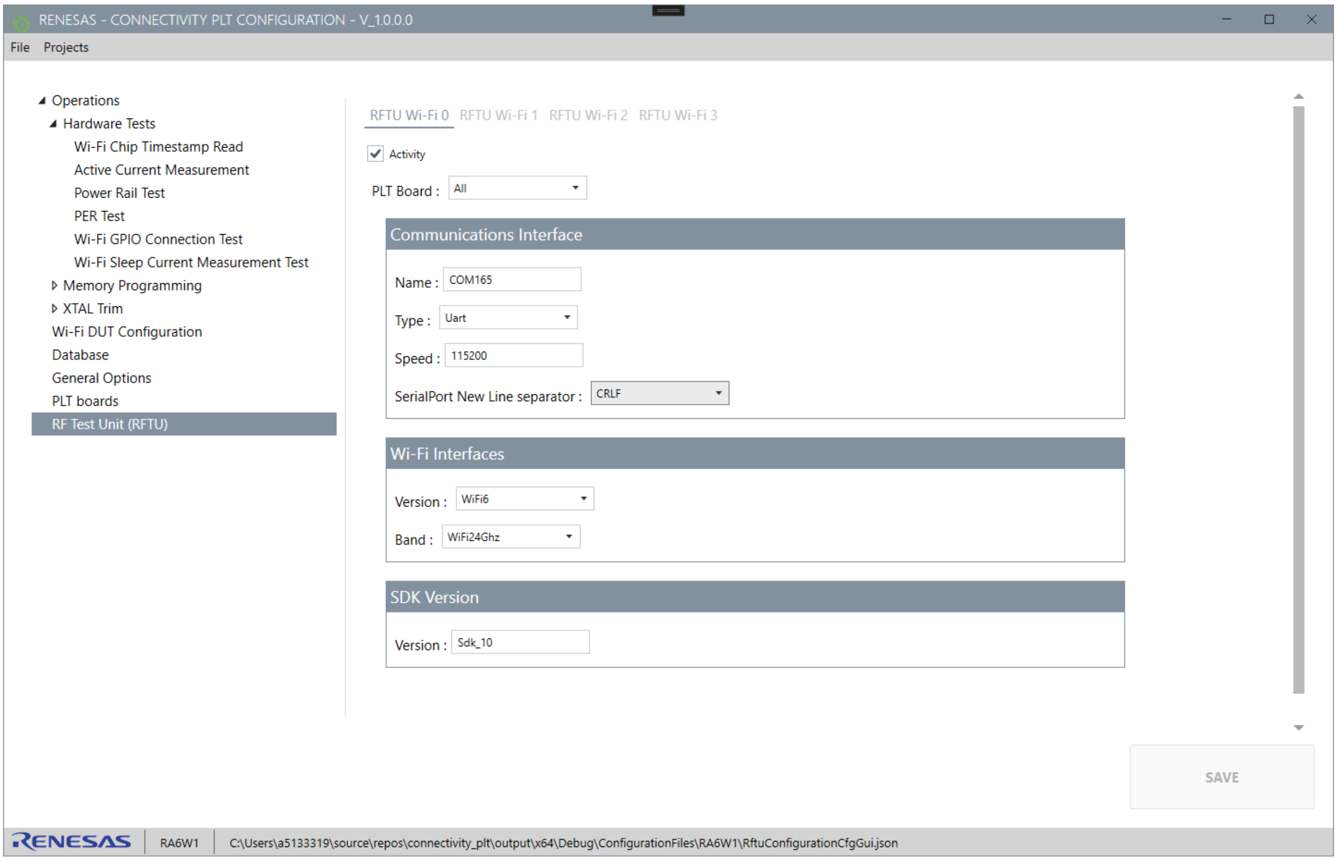
ProjectDa1453x | C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\ProjectDa1453x\RftuConfigurationCfgGui.json

Figure 35. RFTU Bluetooth LE configuration

Table 5. RFTU configurations options

Option	Description
RFTU BLE	
Activity	Enables or disables the usage of the specific RFTU.
Number	RFTU number starting from 0 (first, second, third, fourth).
Plt Board Address	All if the specific RFTU is used for all PLT boards. Otherwise, the address (through the DIP switches) of the associated PLT board to be tested with the specific RFTU (first, second, third, fourth).
Communications Interface	
Name	Assigns a name to the communications interface.
Type	Defines the specific interface (UART, SingleWireUART, SPI, JTAG, SWD)
Speed	Defines speed of the communication interface, for example 115200.
Bluetooth Interfaces	
Version	Version of the Bluetooth interface (v40, v41, v42, v50, v51, v52, v53)..
Type	Type of the Bluetooth interface (Classic, LE).
Sdk Version	
Version	The version of the SDK used.

8.2.5 RFTU Wi-Fi Configuration



☑ Activity

PLT Board : All

Name : COM165

Type : Uart

Speed : 115200

SerialPort New Line separator : CRLF

Version : WiFi6

Band : WiFi24Ghz

Version : Sdk_10

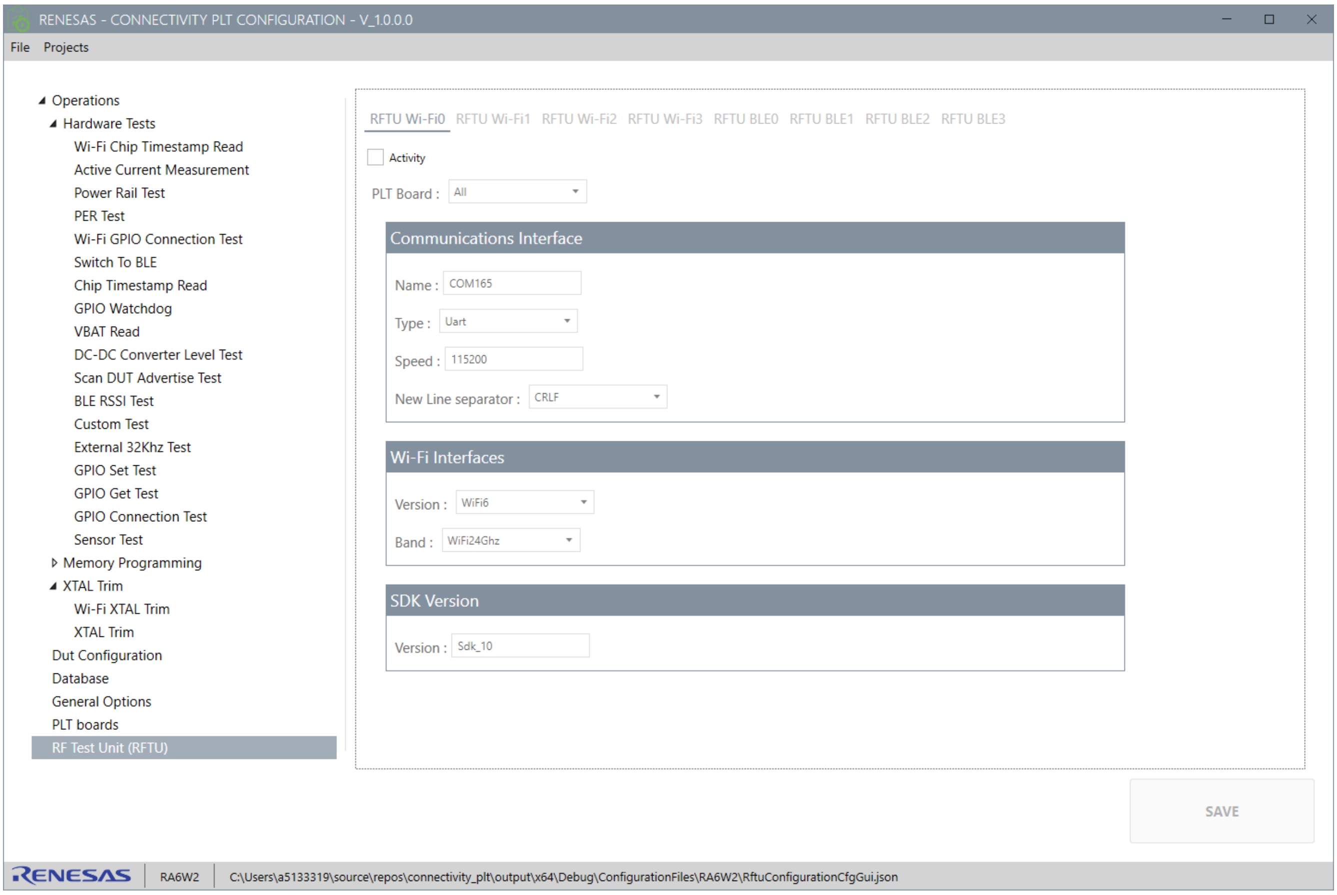
C:\Users\a5133319\source\repos\connectivity_plt\output\x64\Debug\ConfigurationFiles\RA6W1\RftuConfigurationCfgGui.json

Figure 36. RFTU Wi-Fi Configuration

Table 6. RFTU Wi-Fi Configuration

Option	Description
RFTU Wi-Fi	
Activity	Enables or disables the usage of the specific RFTU.
Number	RFTU number starting from 0 (first, second, third, fourth).
Plt Board	All if the specific RFTU is used for all PLT boards. Otherwise, the address (through the DIP switches) of the associated PLT board to be tested with the specific RFTU (first, second, third, fourth).
Communications Interface	
Name	Assigns a name to the communications interface.
Type	Defines the specific interface (UART, SingleWireUART, SPI, JTAG, SWD).
Speed	Defines speed of the communication interface, for example 115200.
NewLine Separator	CRLF, CF, LF
Wi-Fi Interfaces	
Wi-Fi Version	Version of the Wi-Fi interface (WiFi1, WiFi2, WiFi3, WiFi4, WiFi5, WiFi6).
Wi-Fi Band	The band of the Wi-Fi interface (WiFi24Ghz, WiFi5Ghz, WiFiAllBands).
SDK Version	The version of the SDK used.

8.2.6 RFTU Bluetooth LE Wi-Fi Configuration



□ Activity

PLT Board : All

Communications Interface

Name : COM165

Type : Uart

Speed : 115200

New Line separator : CRLF

Wi-Fi Interfaces

Version : WiFi6

Band : WiFi24Ghz

SDK Version

Version : Sdk_10

RA6W2 | C:\Users\a5133319\source\repos\connectivity_plt\output\x64\Debug\ConfigurationFiles\RA6W2\RftuConfigurationCfgGui.json

Figure 37 Bluetooth LE Wi-Fi RFTU configuration

Table 7. RFTU Bluetooth LE/Wi-Fi Configuration

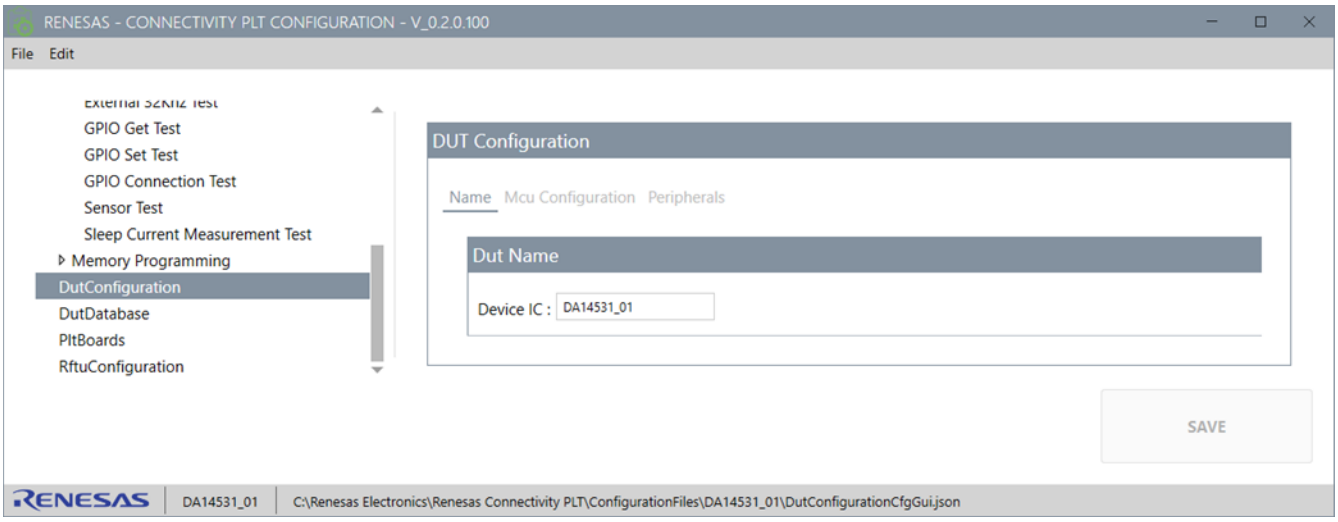
Option	Description
RFTU Wi-Fi	
Activity	Enables or disables the usage of the specific RFTU.
Number	RFTU number starting from 0 (first, second, third, fourth).
Plt Board	All if the specific RFTU is used for all PLT boards. Otherwise, the address (through the DIP switches) of the associated PLT board to be tested with the specific RFTU (first, second, third, fourth).
Communications Interface	
Name	Assigns a name to the communications interface.
Type	Defines the specific interface (UART, SingleWireUART, SPI, JTAG, SWD)
Speed	Defines speed of the communication interface, for example 115200.
NewLine Separator	CRLF, CF, LF
Wi-Fi Interfaces	
Wi-Fi Version	Version of the Wi-Fi interface (WiFi1, WiFi2, WiFi3, WiFi4, WiFi5, WiFi6).
Wi-Fi Band	The band of the Wi-Fi interface (WiFi24Ghz, WiFi5Ghz, WiFiAllBands).
SDK Version	The version of the SDK used.

8.2.7 DUT Configuration

The DUT Configuration section is dedicated to parameters specific to the actual devices that are under test. There are numerous parameters to describe the hardware properties, communication interfaces and so on.

8.2.7.1 DUT Configuration – Device IC

The Device IC under Dut Name is the generic type of the IC used.



RENESAS - CONNECTIVITY PLT CONFIGURATION - V_0.2.0.100

DUT Configuration

Dut Name

Device IC : DA14531_01

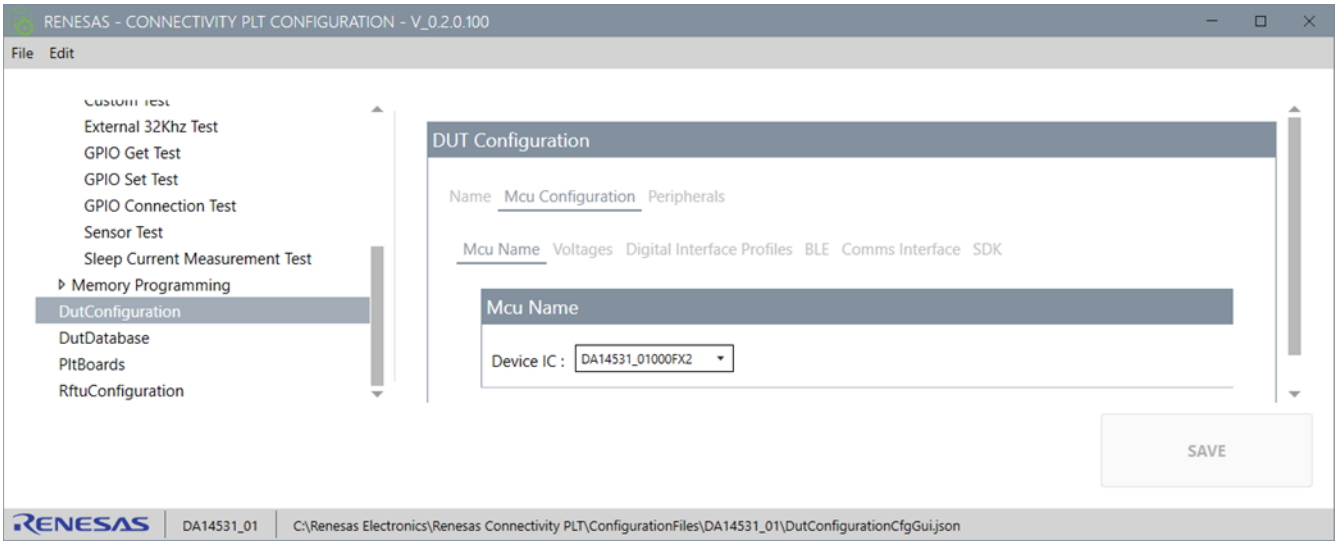
DA14531_01 | C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\DutConfigurationCfgGui.json

Figure 38. Dut configuration

8.2.7.2 MCU Configuration

The MCU configuration section sets all the parameters specific to the MCU being used by the DUT.

- Mcu Name – the exact part number of the MCU used for the DUT.



RENESAS - CONNECTIVITY PLT CONFIGURATION - V_0.2.0.100

DUT Configuration

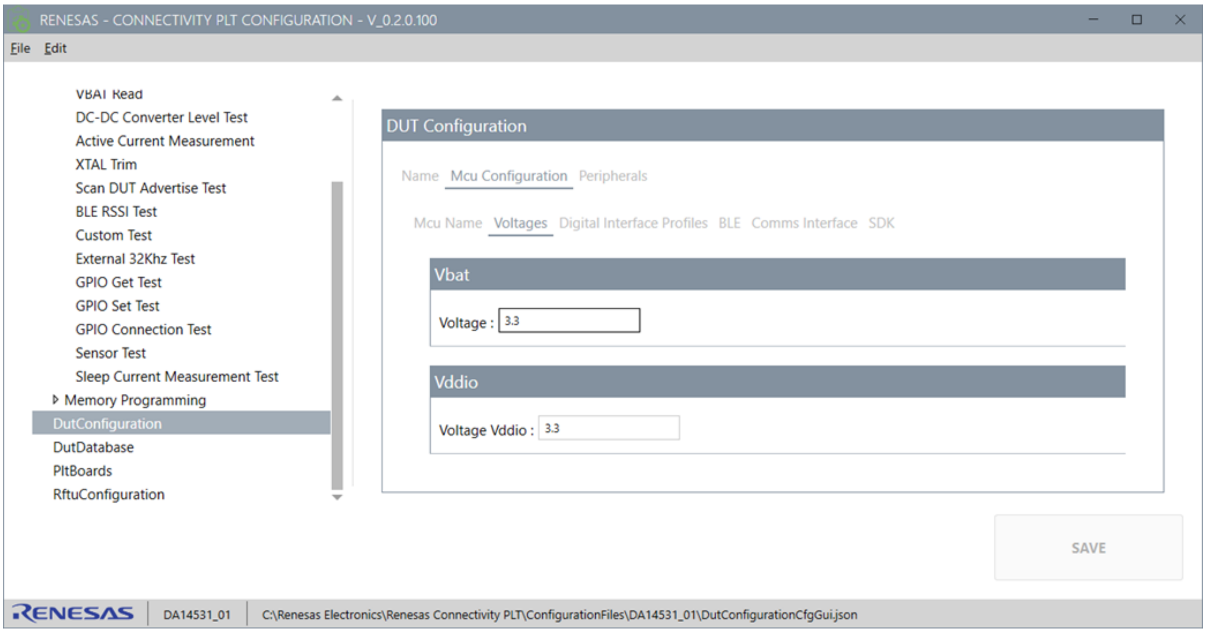
Mcu Name

Device IC : DA14531_01000FX2

DA14531_01 | C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\DutConfigurationCfgGui.json

Figure 39. MCU name configuration

- Voltages
  - Vbat is the voltage that the Connectivity PLT board supplies to the DUT.
  - Vddio is the voltage of the digital interface.



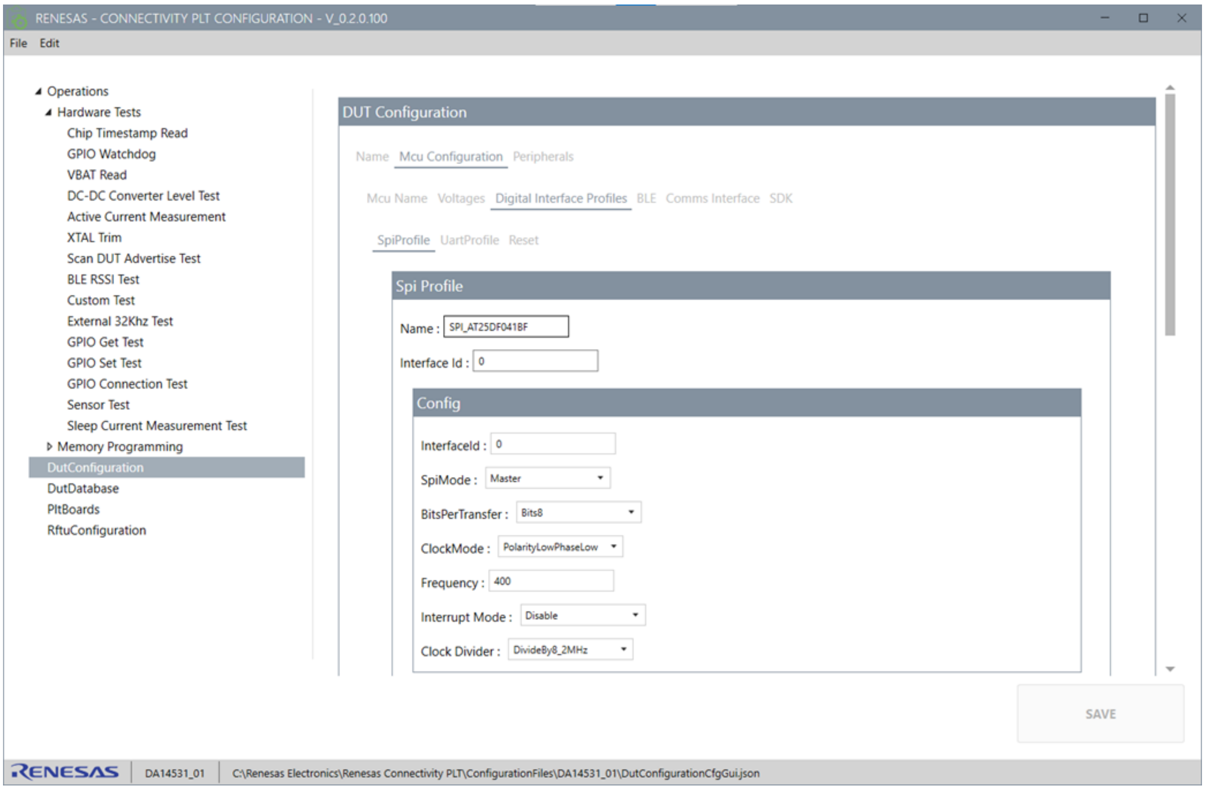
Voltage : 3.3

Voltage Vddio : 3.3

DA14531_01 C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\DutConfigurationCfgGui.json

Figure 40. Voltages configuration

- Digital Interface Profiles
  - **SpiProfile** groups a set of parameters for the SPI interface commonly used for flash memory and sensors. This is a primary configuration of the interface that is used if no further profile is defined for the specific peripheral.



Name : SPI_AT25DF041BF

Interface Id : 0

InterfaceId : 0

SpiMode : Master

BitsPerTransfer : Bits8

ClockMode : PolarityLowPhaseLow

Frequency : 400

Interrupt Mode : Disable

Clock Divider : DivideBy8_2MHz

DA14531_01 C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\DutConfigurationCfgGui.json

Figure 41. SpiProfile configuration

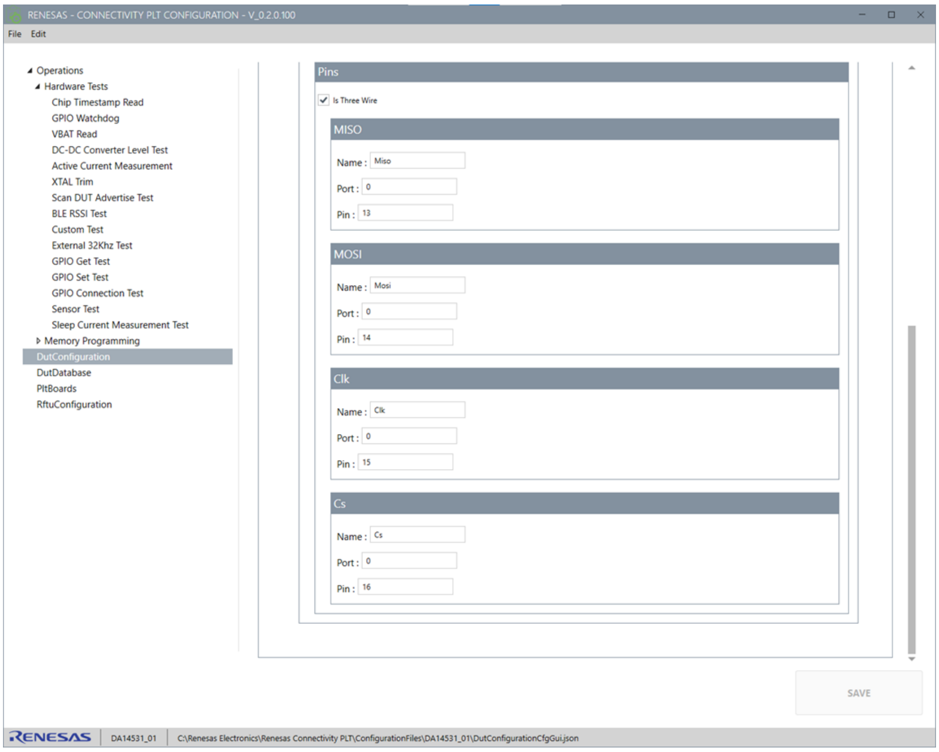
Table 8. SPI profile options

Option	Description
Config	

Option	Description
InterfaceId	The ID of the interface used
BitsPerTransfer	Bits8, Bits16
ClockMode	PolarityLowPhaseLow, PolarityLowPhaseHigh, PolarityHighPhaseLow, PolarityHighPhaseHigh
Frequency	For example, 400
Interrupt Mode	Enable/Disable
Clock Divider	DivideBy8_2MHz, DivideBy4_4MHz, DivideBy2_8MHz, DivideBy14_16MHz

Table 9. SPI profile pin options

Option	Description
Miso	
Port	MISO GPIO port
Pin	MISO GPIO pin
Mosi	
Port	MOSI GPIO port
Pin	MOSI GPIO pin
Sclk	
Port	SCLK GPIO port
Pin	SCLK GPIO pin
Cs	
Port	CS GPIO port
Pin	CS GPIO pin



Pins

☑ Is Three Wire

MISO

Name : Miso
Port : 0
Pin : 13

MOSI

Name : Mosi
Port : 0
Pin : 14

Clk

Name : Clk
Port : 0
Pin : 15

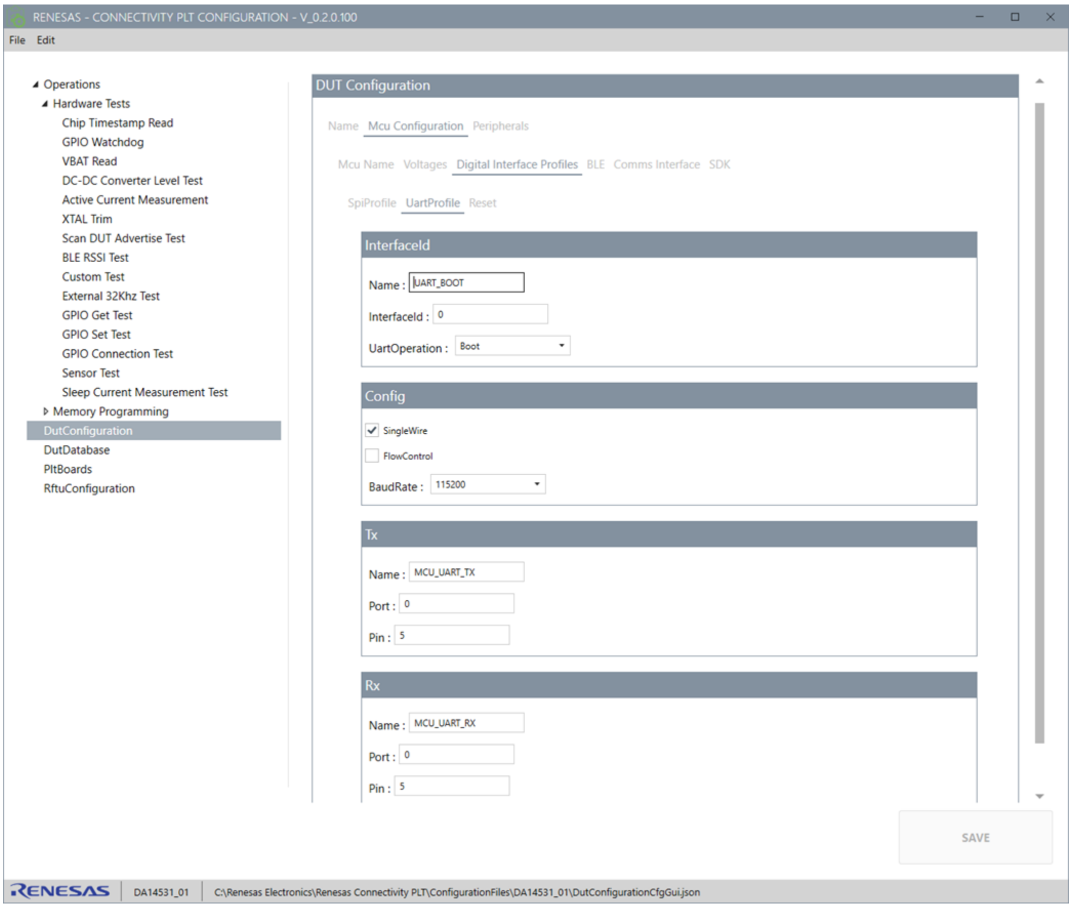
Cs

Name : Cs
Port : 0
Pin : 16

DA14531_01 | C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\DutConfigurationCfgGui.json

Figure 42. Pin configuration

- **UART Profile** (Figure 43)



InterfaceId

Name : UART_BOOT

InterfaceId : 0

UartOperation : Boot

Config

☑ SingleWire

□ FlowControl

BaudRate : 115200

Tx

Name : MCU_UART_TX

Port : 0

Pin : 5

Rx

Name : MCU_UART_RX

Port : 0

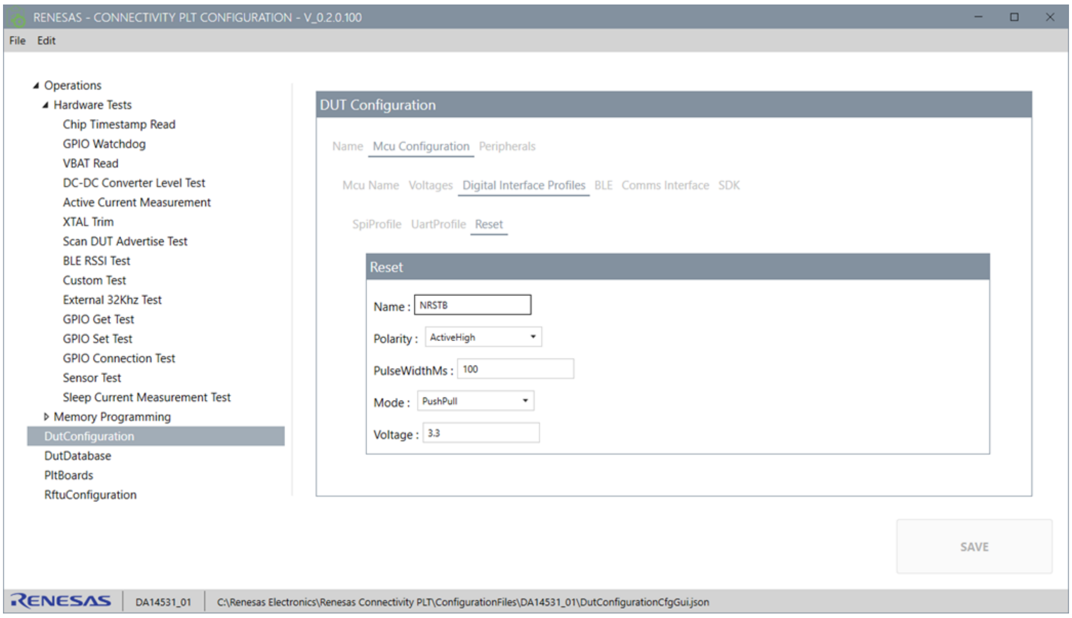
Pin : 5

Figure 43. UART profile configuration

Table 10. UART options

Option	Description
Name	The name of the interface
InterfaceId	The id of the interface used
UartOperation	(Boot, Peripheral, Debug)
Single Wire	-
Flow Control	-
Baud Rate	(1200, 2400, 4800, 9600,19200, 38400, 57600, 76800, 115200, 230400, 460800, 576000, 921600, 1M, 2M, 3M, 4M, 5M, 6M)
Name	MCU_UART_TX
Port	Tx Gpio port
Pin	Tx Gpio pin
Name	MCU_UART_RX
Port	Rx Gpio port
Pin	Rx Gpio pin

- **Reset**



Name : NRSTB
Polarity : ActiveHigh
PulseWidthMs : 100
Mode : PushPull
Voltage : 3.3

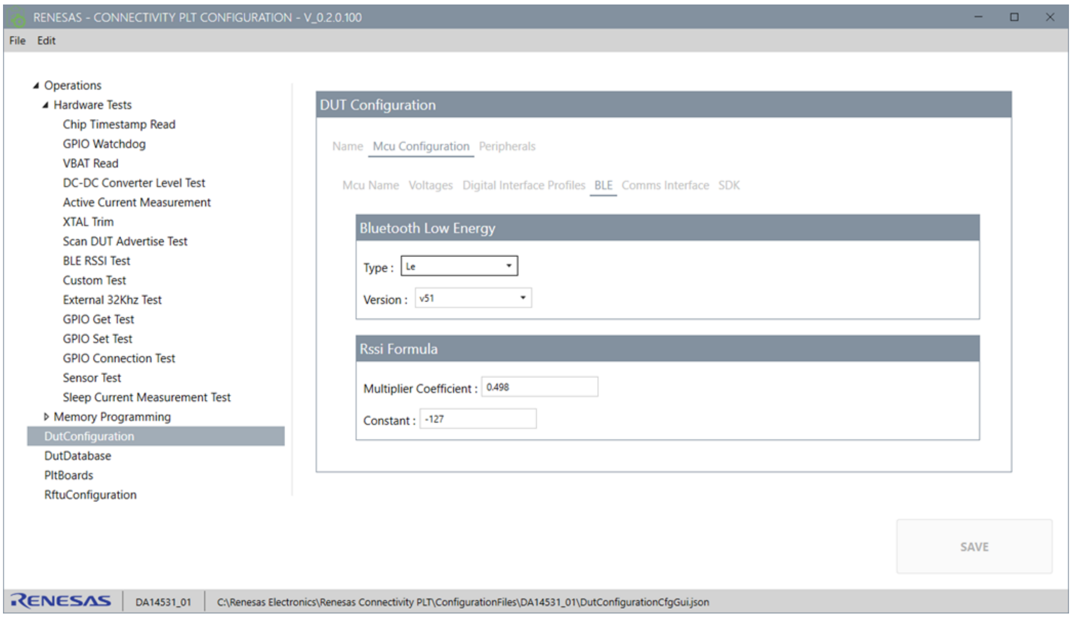
C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\DutConfigurationCfgGui.json

Figure 44. Reset configuration

Table 11. Reset options

Option	**Description**
Config	
Name	NRSTB
Polarity	ActiveHigh, ActiveLow
Pulse Width Ms	100
Mode	PushPull, OpenDrain
Voltage	3.3

- **Bluetooth LE**



Type : Le
Version : v51
Multiplier Coefficient : 0.498
Constant : -127

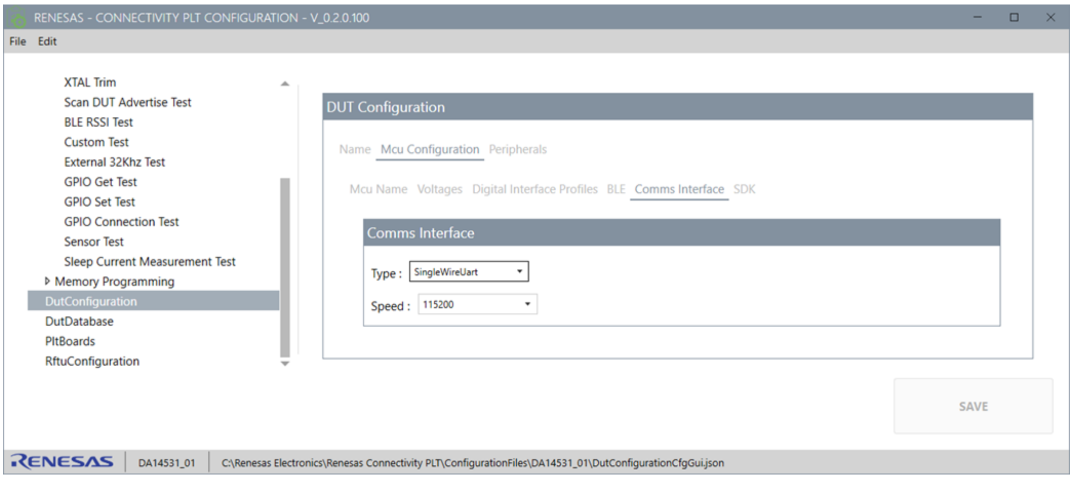
C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\DutConfigurationCfgGui.json

Figure 45. Bluetooth LE configuration

Table 12. Bluetooth LE options

Option	Description
Bluetooth Low Energy	
Type	Type of the Bluetooth Interface (Classic, Le)
Version	Version of the Bluetooth interface (v40, v41, v42, v50, v51, v52, v53)
Rssi Formula	
Multiplier Coefficient	The coefficient used in the calculation of the RSSI (Conversion factor)
Constant	The constant used in the calculation of the RSSI (Noise floor)

- **Comms Interface** (Figure 46)



Type : SingleWireUart

Speed : 115200

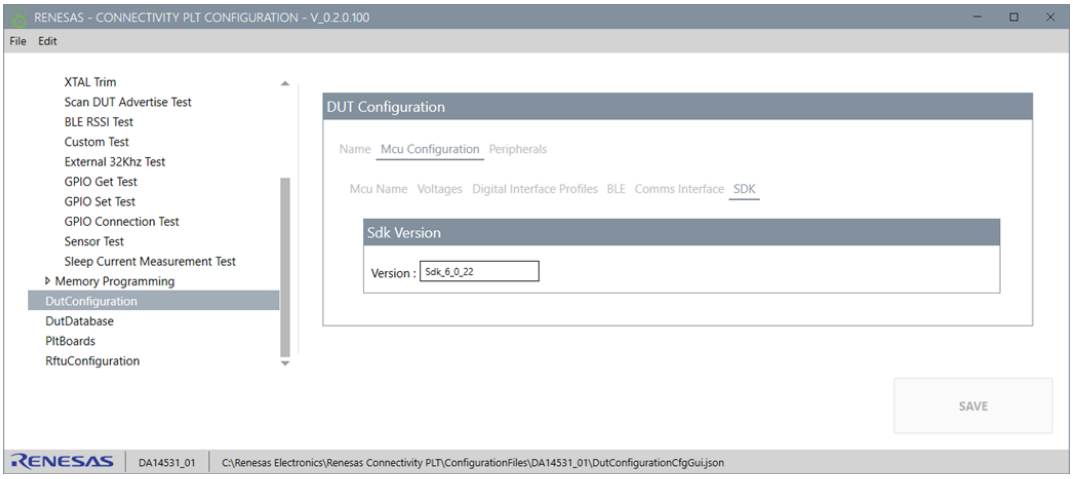
C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\DutConfigurationCfgGui.json

Figure 46. Comms interface configuration

Table 13. Comms interface options

Option	Description
Config	
Type	Uart, SingleWireUart, Spi, Jtag, Swd, Usb
Baud Rate	(1200, 2400, 4800, 9600,19200, 38400, 57600, 76800, 115200, 230400, 460800, 576000, 921600, 1M, 2M, 3M, 4M, 5M, 6M)

- **SDK**



Version : Sdk_6_0_22

C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\DutConfigurationCfgGui.json

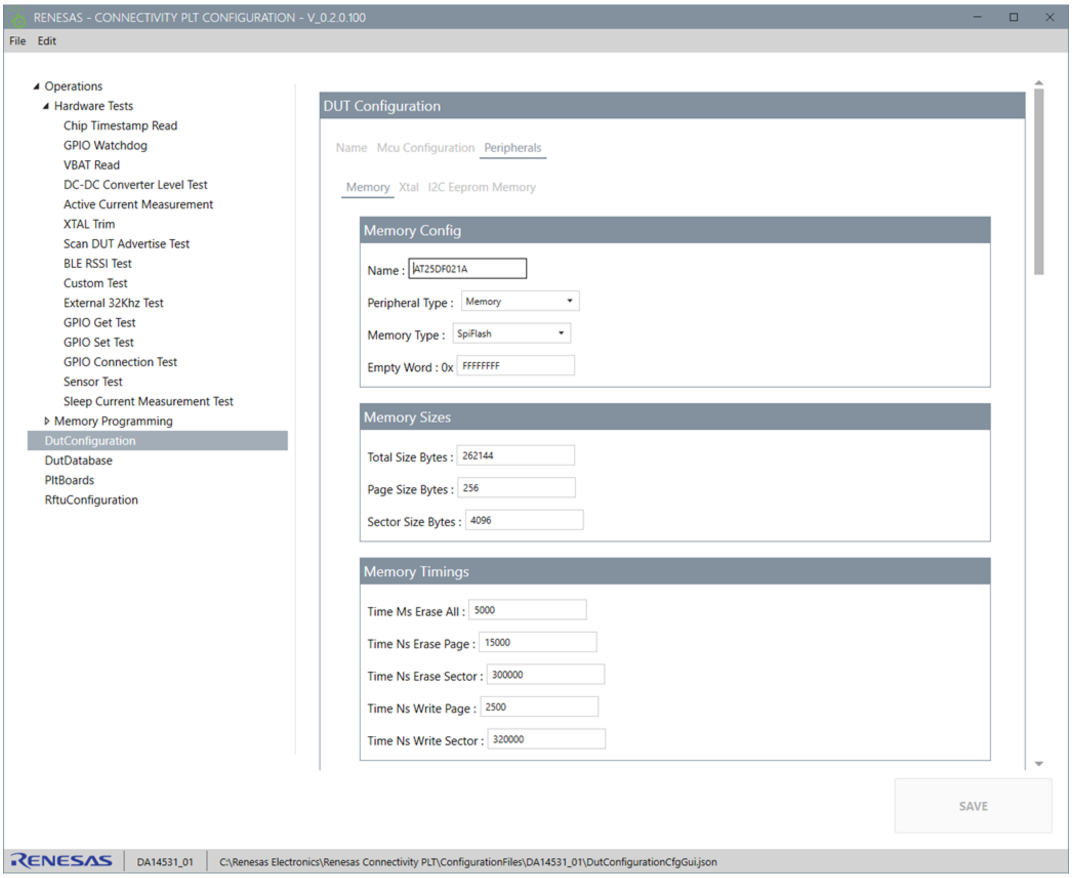
Figure 47. SDK configuration

Table 14. SDK version

Option	Description
Sdk Version	
Version	The SDK version

8.2.7.3 Peripherals

- **Memory**



Name : AT25DF021A

Peripheral Type : Memory

Memory Type : SpiFlash

Empty Word : 0x FFFFFFFF

Total Size Bytes : 262144

Page Size Bytes : 256

Sector Size Bytes : 4096

Time Ms Erase All : 5000

Time Ns Erase Page : 15000

Time Ns Erase Sector : 300000

Time Ns Write Page : 2500

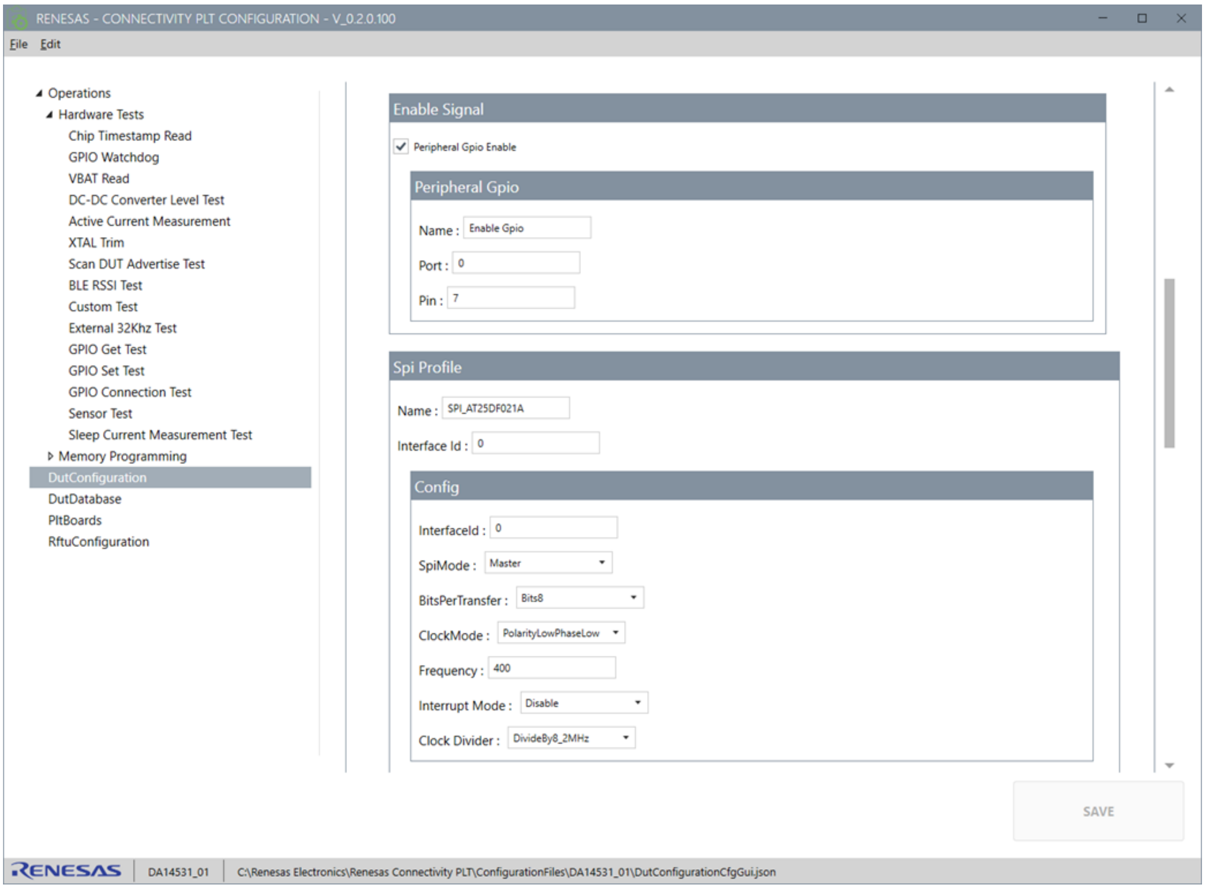
Time Ns Write Sector : 320000

Figure 48. Memory configuration 1

Table 15. Memory configuration

Option	Description
Memory Config	
Name	The name of the configuration
Peripheral Type	(Memory, Sensor, Antenna, Led, Button, Switch, Ftdi, Fpga, Dac, Adc, UsbHub, I2cGeneric, SpiGeneric, AddressSwitch, VoltageController, DutController, Nex74CB3Q3253, Ammeter, Xtal)
Memory Type	(SpiFlash, QspiFlash, OspiFlash, I2cEeprom, Otp, EmbeddedFlash, Rom, SpiEeprom)
Empty Word	Content of empty flash: 0xFFFFFFFF
Option	Description
Memory Sizes	
Total Size Bytes	Total memory size in bytes
Page Size bytes	Page size in Bytes
Sector Size Bytes	Sector size in Bytes

Option	Description
Option	Description
Memory Timings	
Time Ms Erase All	Time to erase all (chip erase) in milliseconds
Time Ns Erase Page	Time to erase a single page in nanoseconds
Time Ns Erase Sector	Time to erase a single sector in nanoseconds
Time Ns Write Page	Minimum time to write a single page in nanoseconds
Time Ns Write Sector	Minimum time to write a single sector in nanoseconds



Enable Signal

☑ Peripheral Gpio Enable

Peripheral Gpio

Name : Enable Gpio

Port : 0

Pin : 7

Spi Profile

Name : SPI_AT25DF021A

Interface Id : 0

Config

InterfaceId : 0

SpiMode : Master

BitsPerTransfer : Bits8

ClockMode : PolarityLowPhaseLow

Frequency : 400

Interrupt Mode : Disable

Clock Divider : DivideBy8_2MHz

DA14531_01 C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\DutConfigurationCfgGui.json

Figure 49. Memory configuration

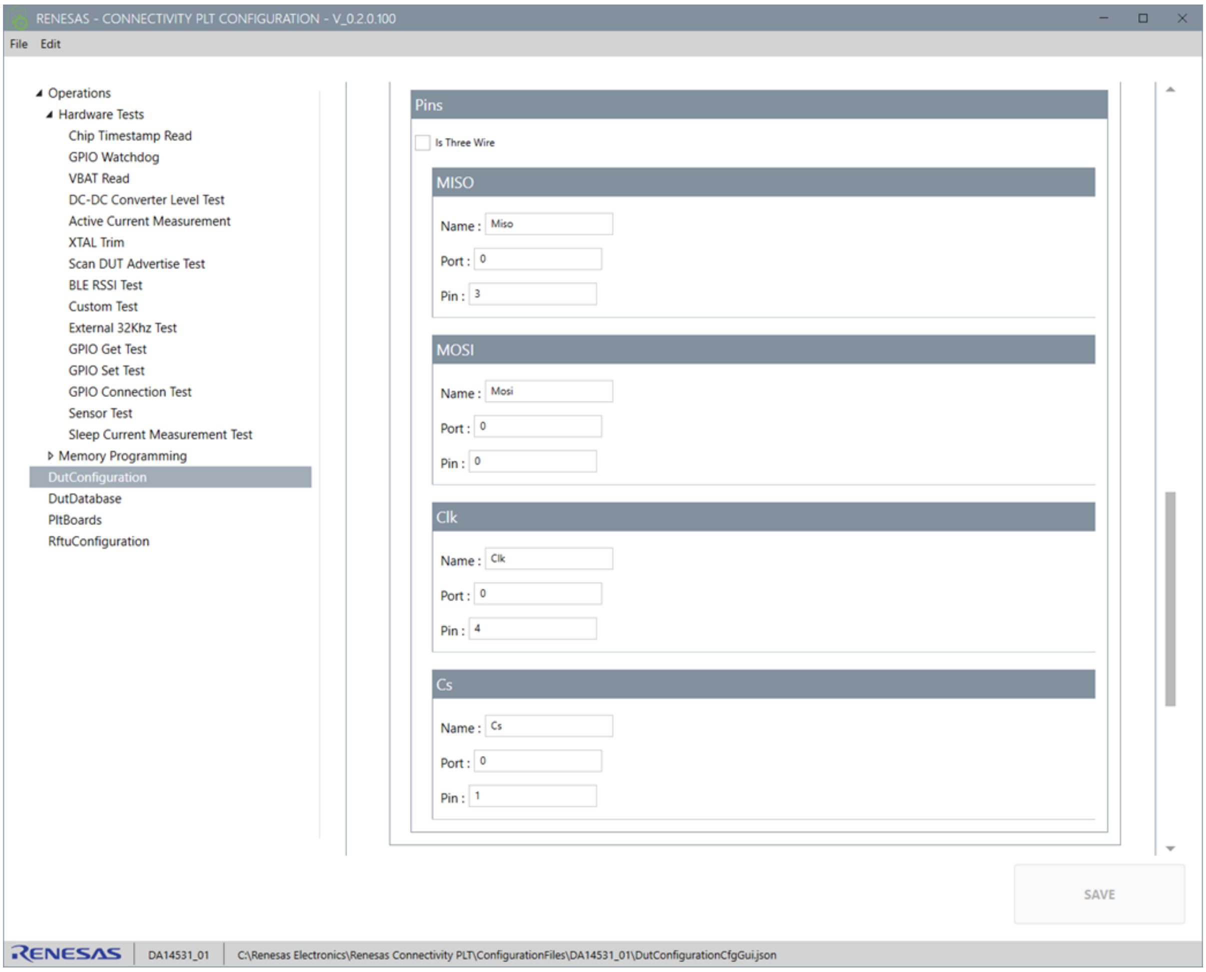
Table 16. Peripheral GPIO

Option	Description
Enable Signal	
Peripheral GPIO Enable	Enable the peripheral GPIO
Name	Name of Peripheral GPIO
Port	GPIO Port
Pin	GPIO Pin

Table 17. SPI profile

Option	Description
Spi Profile	
Name	Name of Spi profile

Option	Description
Interface Id	Interface Id
Option	Description
Config	
Interface Id	Interface Id
Bits Per Transfer	(Bits8, Bits16)
Clock Mode	(PolarityLowPhaseLow, PolarityLowPhaseHigh, PolarityHighPhaseLow, PolarityHighPhaseHigh)
Frequency	Frequency
Interrupt Mode	Enable or disable Interrupt Mode (Enable, Disable)
Clock Divider	(DivideBy8_2MHz, DivideBy4_4MHz, DivideBy2_8MHz, DivideBy14_16MHz)



Pins

☐ Is Three Wire

MISO

Name : Miso

Port : 0

Pin : 3

MOSI

Name : Mosi

Port : 0

Pin : 0

Clk

Name : Clk

Port : 0

Pin : 4

Cs

Name : Cs

Port : 0

Pin : 1

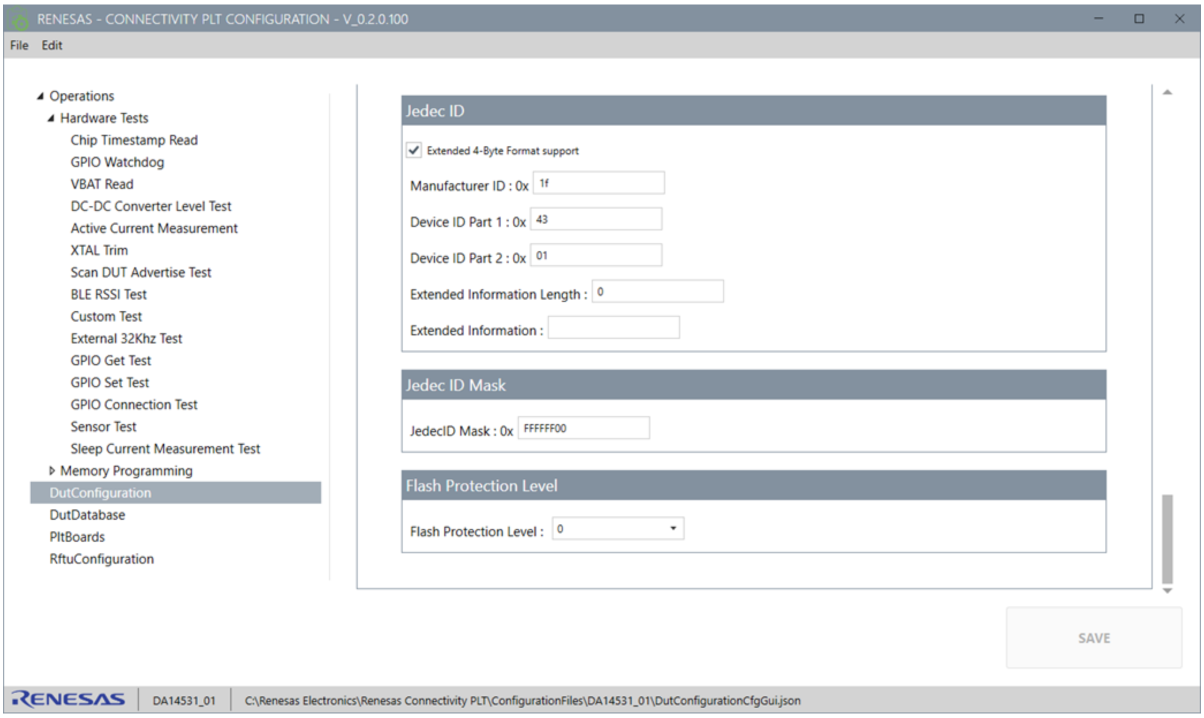
DA14531_01 | C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\DutConfigurationCfgGui.json

Figure 50. Pins configuration

Table 18. Pins configuration

Option	Description
Is Three Wire	Enable three wire communication
Miso	
Name	Name of Miso configuration
Port	Miso Gpio port
Pin	Miso Gpio pin
Mosi	

Option	Description
Name	Name of Mosi configuration
Port	Mosi Gpio port
Pin	Mosi Gpio pin
Sclk	
Name	Name of Sclk configuration
Port	Sclk Gpio port
Pin	Sclk Gpio pin
Cs	
Name	Name of Cs configuration
Port	Cs Gpio port
Pin	Cs Gpio pin



Jedec ID

☑ Extended 4-Byte Format support

Manufacturer ID : 0x 1f

Device ID Part 1 : 0x 43

Device ID Part 2 : 0x 01

Extended Information Length : 0

Extended Information :

Jedec ID Mask

JedecID Mask : 0x FFFFFF00

Flash Protection Level

Flash Protection Level : 0

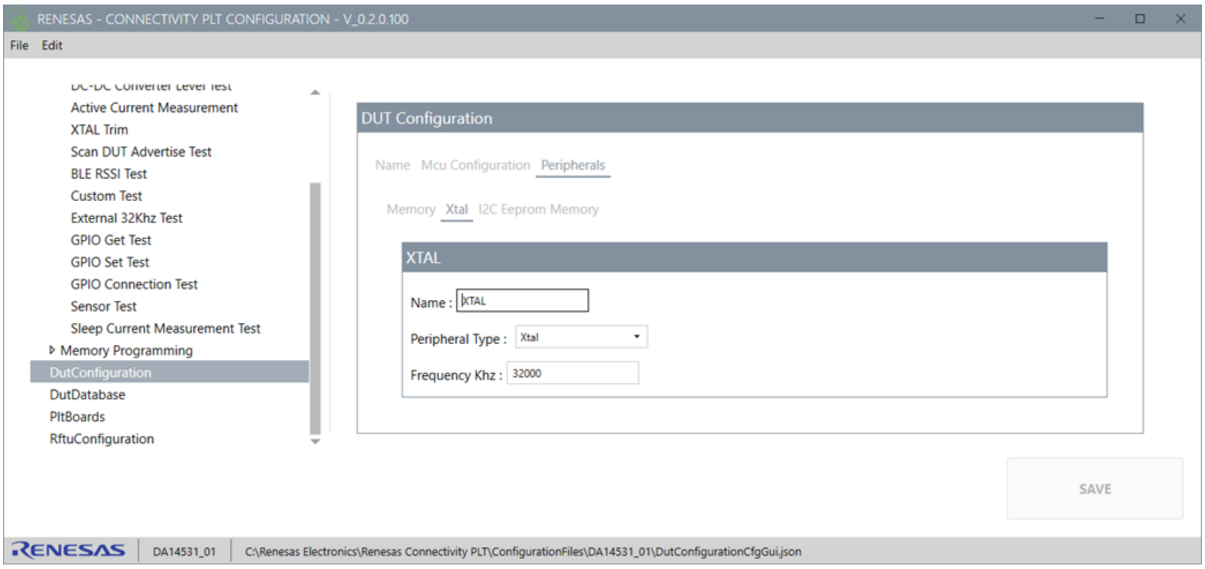
Figure 51. Memory configuration

Table 19. Jedec configuration

Option	Description
Jedec ID	
Extended 4-byte Format Support	Enable/Disable 4-byte format support
Manufacturer ID	Part of Jedec ID
Device ID Part1	Part of Jedec ID
Device ID Part2	Part of Jedec ID
Extended Information Length	Number of bytes of extended information
Extended Information	Jedec Id extended information
Jedec ID Mask	
Jedec ID Mask	Jedec Id mask to ignore bytes

Option	Description
Flash Protection Level	
Flash Protection Level	(0-15)

- **Xtal**



Name : XTAL

Peripheral Type : Xtal

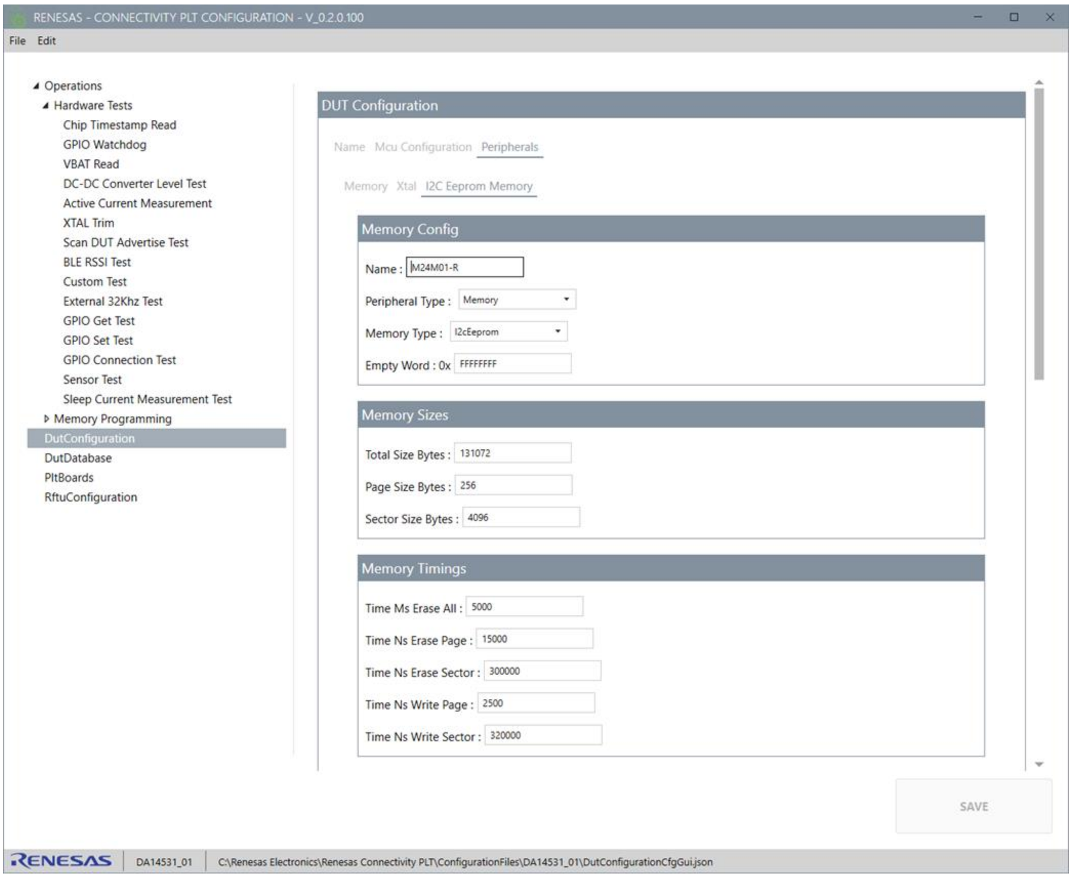
Frequency Khz : 32000

Figure 52. Xtal configuration

Table 20. XTAL configuration

Option	Description
XTAL	
Name	Name of Xtal
Peripheral Type	(Memory, Sensor, Antenna, Led, Button, Switch, Ftdi, Fpga, Dac, Adc, UsbHub, I2cGeneric, SpiGeneric, AddressSwitch, VoltageController, DutController, Nex74CB3Q3253, Ammeter, Xtal)
Frequency kHz	XTAL Frequency in kHz

- **I2C Eeprom Memory**



Memory Config

Name : M24M01-R

Peripheral Type : Memory

Memory Type : I2cEeprom

Empty Word : 0x FFFFFFFF

Memory Sizes

Total Size Bytes : 131072

Page Size Bytes : 256

Sector Size Bytes : 4096

Memory Timings

Time Ms Erase All : 5000

Time Ns Erase Page : 15000

Time Ns Erase Sector : 300000

Time Ns Write Page : 2500

Time Ns Write Sector : 320000

Figure 53. I2C Eeprom configuration 1

Table 21. I2C configuration

Option	**Description**
Memory Config	
Name	Name of memory configuration
Peripheral Type	(Memory, Sensor, Antenna, Led, Button, Switch, Ftdi, Fpga, Dac, Adc, UsbHub, I2cGeneric, SpiGeneric, AddressSwitch, VoltageController, DutController, Nex74CB3Q3253, Ammeter, Xtal)
Memory Type	(SpiFlash, QspiFlash, OspiFlash, I2cEeprom, Otp, EmbeddedFlash, Rom, SpiEeprom)
Empty Word	Content of empty eeprom: 0xFFFFFFFF

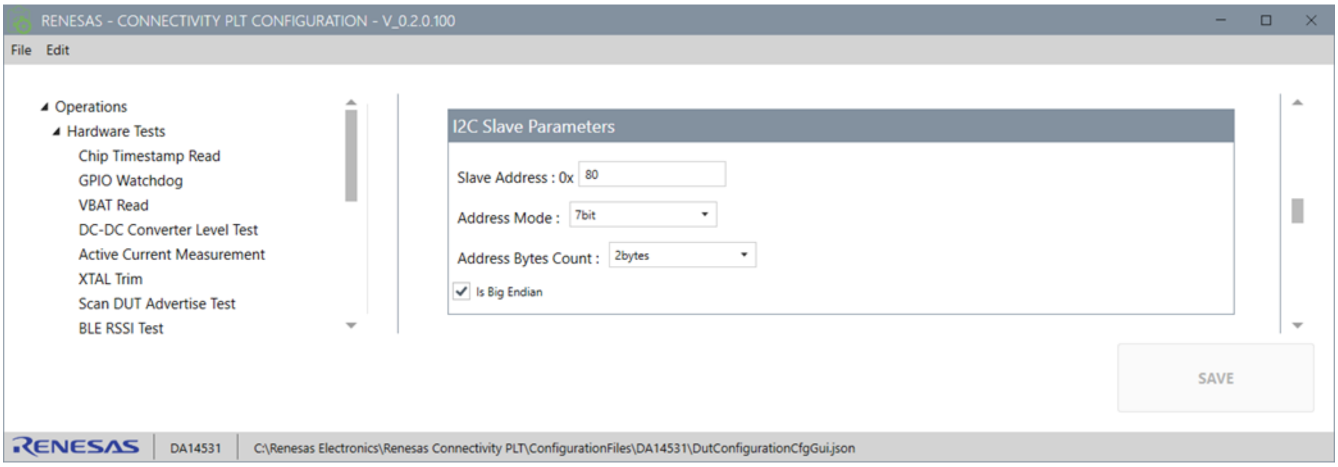
Table 22. I2C size

Option	**Description**
Memory Sizes	
Total Size Bytes	Memory total size in Bytes
Page Size bytes	Memory page size in Bytes
Sector Size Bytes	Memory sector size in Bytes

Table 23. I2C timings

Option	**Description**
Memory Timings	
Time Ms Erase All	Time to erase all (chip erase) in milliseconds
Time Ns Erase Page	Time to erase a single page in nanoseconds

Option	Description
Time Ns Erase Sector	Time to erase a single sector in nanoseconds
Time Ns Write Page	Minimum time to write a single page in nanoseconds
Time Ns Write Sector	Minimum time to write a single sector in nanoseconds


RENESAS - CONNECTIVITY PLT CONFIGURATION - V_0.2.0.100
File
Edit
Operations
Hardware Tests
Chip Timestamp Read
GPIO Watchdog
VBAT Read
DC-DC Converter Level Test
Active Current Measurement
XTAL Trim
Scan DUT Advertise Test
BLE RSSI Test
SAVE
RENESAS
DA14531
C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531\DutConfigurationCfgGui.json

I2C Slave Parameters

Slave Address : 0x 80

Address Mode : 7bit

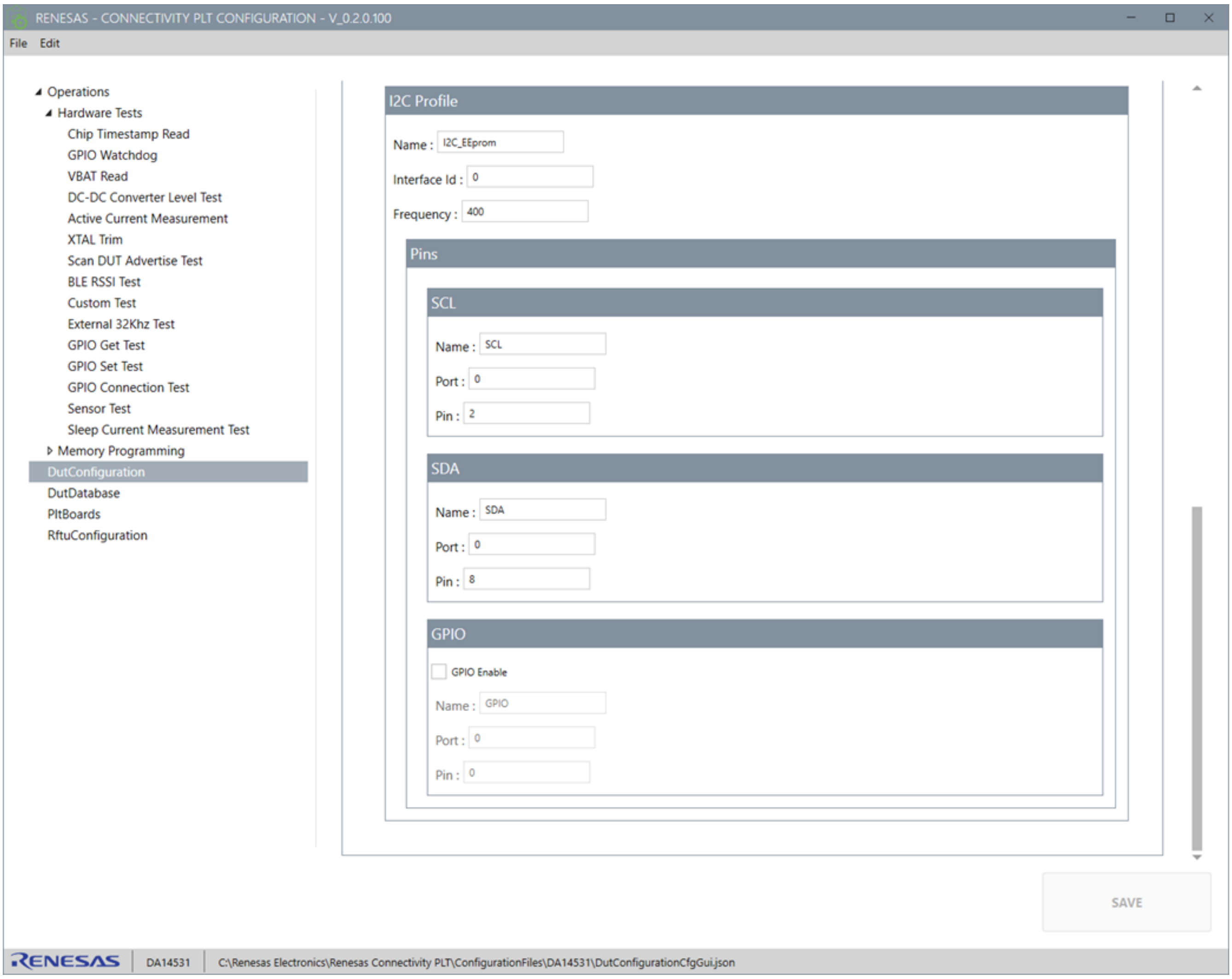
Address Bytes Count : 2bytes

☑ Is Big Endian

Figure 54. I2C slave parameters

Table 24. I2C slave configuration

Option	Description
I2C Slave Parameters	
Slave Address	Slave address in hex
Address Mode	(7bit, 10bit)
Address Byte Count	(1byte, 2bytes, 3bytes)
Is Big Endian	Set if Big Endian



I2C Profile

Name : I2C_EEprom

Interface Id : 0

Frequency : 400

Pins

SCL

Name : SCL

Port : 0

Pin : 2

SDA

Name : SDA

Port : 0

Pin : 8

GPIO

□ GPIO Enable

Name : GPIO

Port : 0

Pin : 0

Figure 55. I2C profile

Table 25. I2C profile configuration

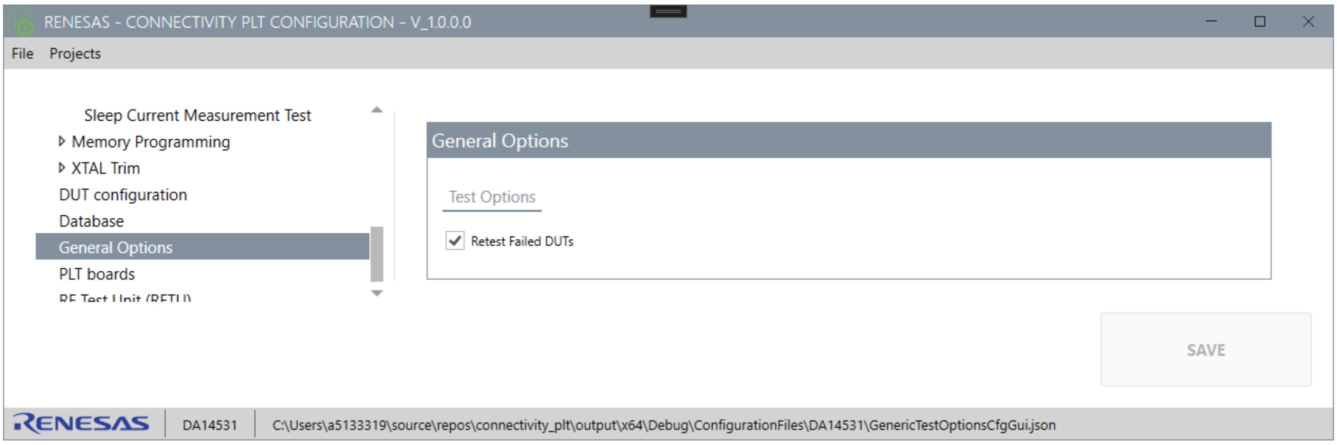
Option	Description
I2C Profile	
Name	Profile name
Interface Id	Interface Id
Frequency	Profile frequency

Table 26. I2C pins configuration

Option	Description
SCL	
Name	SCL name
Port	Scl Gpio port
Pin	Scl Gpio pin
SDA	
Name	SDA name
Port	Sda Gpio port
Pin	Sda Gpio pin

Option	Description
GPIO	
Gpio Enable	Enable Gpio
Name	Gpio name
Port	Gpio port
Pin	Gpio pin

8.2.8 General Options



General Options

Test Options

☑ Retest Failed DUTs

DA14531 C:\Users\a5133319\source\repos\connectivity_plt\output\x64\Debug\ConfigurationFiles\DA14531\GenericTestOptionsCfgGui.json

Figure 56. General Options

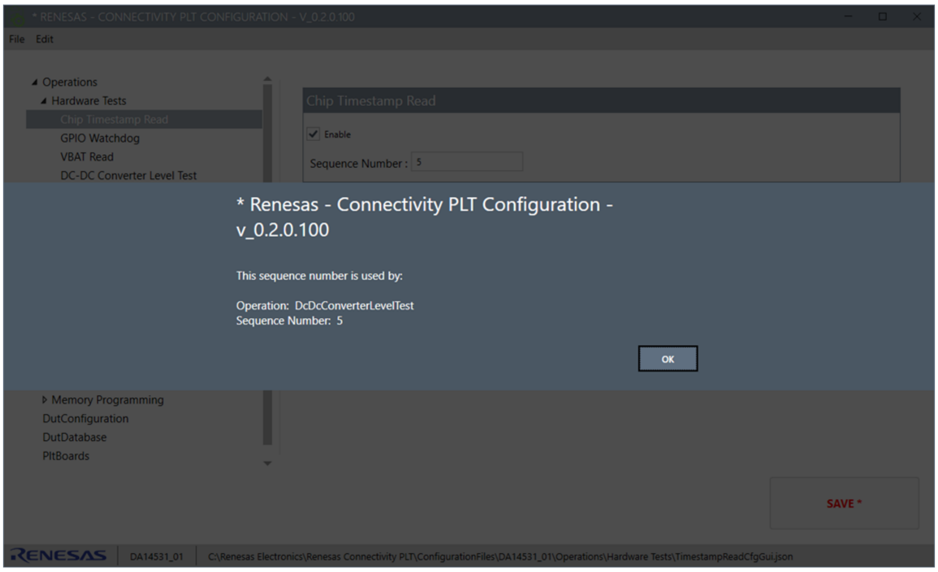
Table 27. General Options

Option	Description
General Options	
Retest Failed DUTs	Automatically retests only the failed DUTs.

8.2.9 Configure Sequence Number

A sequence number is assigned to every test and represents the order in which the tests are executed. The order is reflected in the side navigation panel. You can edit the sequence number.

If the sequence number is duplicated, an error message is displayed informing that the specific sequence number is in use and the test name that uses it, Figure 57.


* RENESAS - CONNECTIVITY PLT CONFIGURATION - V_0.2.0.100
File
Edit
Operations
Hardware Tests
Chip Timestamp Read
GPIO Watchdog
VBAT Read
DC-DC Converter Level Test
Memory Programming
DutConfiguration
DutDatabase
PltBoards
Chip Timestamp Read
OK
SAVE *
RENESAS
DA14531_01
C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\Operations\Hardware Tests\TimestampReadCfgGui.json

☑ Enable

Sequence Number : 5

* Renesas - Connectivity PLT Configuration - v_0.2.0.100

This sequence number is used by:

Operation: DcDcConverterLevelTest
Sequence Number: 5

Figure 57. Sequence number configuration

8.3 Hardware Tests Configurations

This section groups all the tests that are not related to memory programming, see Table 28. Typically, each test represents a hardware function and has defined pass and fail criteria.

Table 28. Type of hardware tests

Operation type	Description
Chip Timestamp Read	Not an actual test but is used mainly to log the information that was stored in the CS area of the OTP during factory programming. See Section 0.
GPIO Watchdog	Enables a periodic pulse at a specific CPU pin that can be utilized by the specific product as an external watchdog monitor. See Section 8.3.2.
VBAT Read	Sends a command to the DUTs to measure their VBAT using their internal ADC. See Section 8.3.3.
DC-DC Converter Level Test	Used to measure the output of the on-board DC-DC converter. See Section 8.3.4. A lower and upper limit are used to define the pass/fail criteria.
Active Current Measurement	Measures the current consumed by the DUT at this stage of testing. In most cases this is the current consumption of the entire product. See Section 8.3.5.
XTAL Trim	Calculates the correct crystal oscillator trim value. The trim value of the crystal is important to achieve accurate frequency of the Bluetooth LE radio. See Section 8.3.6.
Scan Dut Advertise	Tests the transmission of Bluetooth LE advertising packets for each DUT. See Section 8.3.8.
Bluetooth LE RSSI Test	Tests the reception of Bluetooth LE signals by the DUTs. See Section 8.3.9.
Custom Test	Used for vendor specific operations. These tests are developed within the production test firmware and follow a specific format. The tests are initiated by a single byte HCI command and report back a byte indicating the status of the test. See Section 8.3.10.
External 32 kHz Test	Checks if the 32 kHz crystal is present and operated correctly. See Section 8.3.11.
GPIO Get Test	Evaluates the state of a specific pin. This test is commonly used to check interoperability between other devices and the CPU in the customers' product; and can also be used to check for short circuit between pins. See Section 8.3.12.
GPIO Set Test	Sets a CPU pin to a specific state. It is commonly used for interoperability between other devices and the CPU in the customers' product; and can also be used to check for short circuit between pins in conjunction with a GPIO get Test. See Section 8.3.13.

Operation type	Description
GPIO Connection Test	Combines set and get GPIO operations to check connectivity between CPU pins. See Section 8.3.14.
Sensor Test	Tests interoperability between the CPU and attached sensors to the I2C or SPI bus. See Section 8.3.15.
Sleep Current Measurement Test	Measures the current consumption of the DUTs during sleep mode. Due to the extremely low currents, an external DMM instrument is required for this operation to make very accurate measurements. The measurement is performed on the VDUT power supply of the Connectivity PLT and is cumulative of the current from all DUTs. The result is divided by the number of active DUTs, report and compared to pass/fail criteria. See Section 8.3.16.

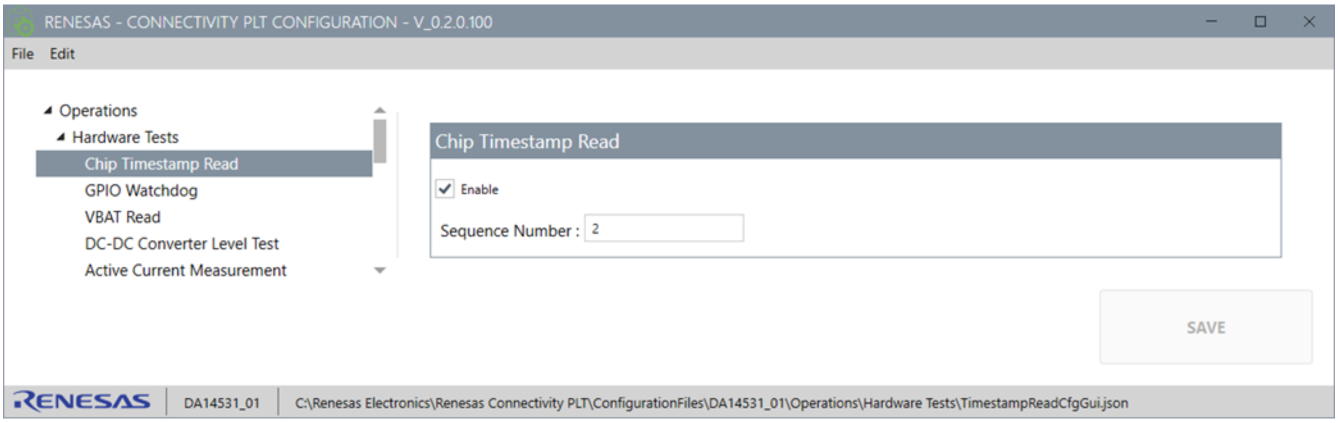
Table 29. Tests and Projects applicability

Hardware Tests	DA14530, DA14531, DA14531MOD, DA14531-01, DA14533, DA14535, DA14530MOD	RA6W1, RRQ6100x	RA6W2, RRQ6105x
Hardware Tests			
Active Current Measurement	✓	✓	✓
Chip Timestamp Read	✓		✓
GPIO Watchdog	✓		✓
VBAT Read	✓		✓
DC-DC Converter Level Test	✓		✓
Scan DUT Advertise Test	✓		✓
BLE RSSI Test	✓		✓
Custom Test	✓		✓
External 32Khz Test	✓		✓
GPIO Get Test	✓		✓
GPIO Set Test	✓		✓
GPIO Connection Test	✓	✓	✓
Sensor Test	✓		✓
Sleep Current Measurement Test	✓		✓
Power Rail Test		✓	✓
Packet Error Rate Test		✓	✓
Memory Programming			
UART Baud Rate Set	✓		
SPI Flash Init	✓		
SPI Flash Erase All	✓		
SPI Flash Erase Bock	✓		
SPI Flash Write Binary	✓		
Spi Flash Read	✓		
EEPROM Memory Write	✓		
EEPROM Memory Read	✓		
OTP Memory Read	✓	✓	✓
OTP Memory Write	✓	✓	✓
OTP Encryption Key Write	✓		
Custom Memory Data Write	✓	✓	✓
Common Memory Data Write	✓	✓	✓

Hardware Tests	DA14530, DA14531, DA14531MOD, DA14531-01, DA14533, DA14535, DA14530MOD	RA6W1, RRQ6100x	RA6W2, RRQ6105x
Configuration Script Write	✓	✓	
Header Write	✓	✓	
QSPI Flash Block Erase		✓	✓
QSPI Flash Direct Write Binary		✓	✓
QSPI Flash Read		✓	✓
QSPI Flash Erase All		✓	✓
QSPI Test		✓	✓
Wi-Fi Configuration Script Write		✓	✓
XTAL Trim			
XTAL Trim	✓		✓
XTAL Trim Wi-Fi		✓	✓

8.3.1 Chip Timestamp Read

Chip Timestamp Read test is available in DA14530, DA14531, DA14531MOD, DA14531_1, DA14533, DA14535, DA14530MOD, RA6W2, and can be useful for traceability and quality control.


RENESAS - CONNECTIVITY PLT CONFIGURATION - V_0.2.0.100
File
Edit
Operations
Hardware Tests
Chip Timestamp Read
GPIO Watchdog
VBAT Read
DC-DC Converter Level Test
Active Current Measurement
SAVE
RENESAS

Chip Timestamp Read

☑ Enable

Sequence Number : 2

DA14531_01 C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\Operations\Hardware Tests\TimestampReadCfgGui.json

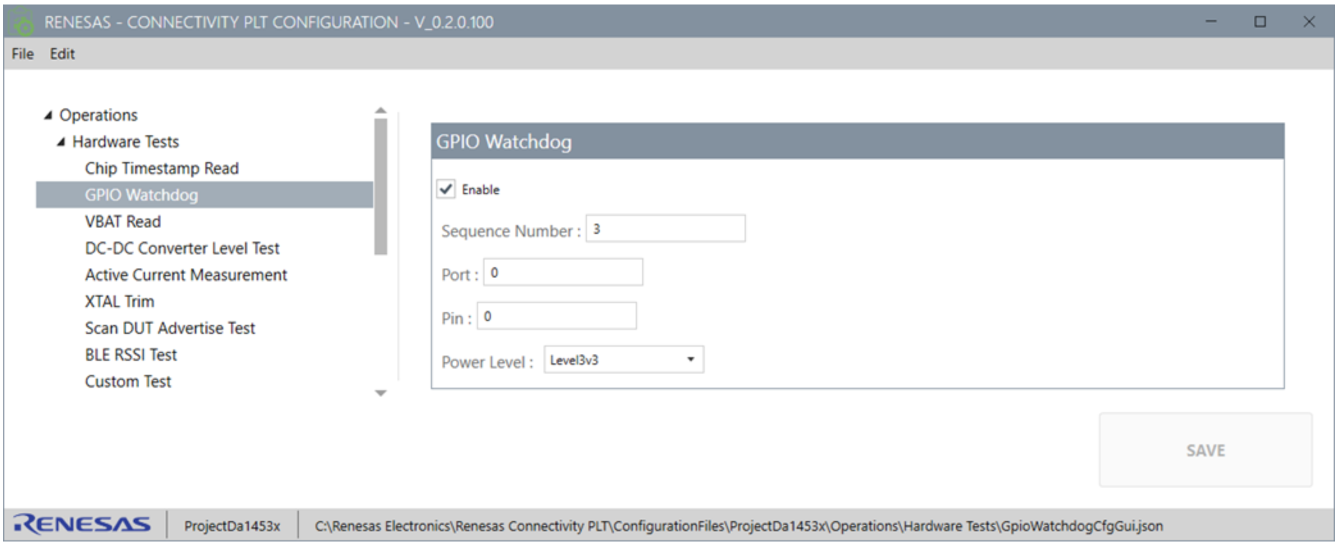
Figure 58. Chip timestamp configuration

8.3.2 GPIO Watchdog

GPIO Watchdog is available in DA1453x, RA6W2, RRQ6105x.

The pin output toggles throughout the entire test process except for the firmware download process. Following the firmware download process the watchdog output resumes.

The pulse on the GPIO has approximately 0.75% duty cycle and 0.5 Hz frequency.



☑ Enable

Sequence Number : 3

Port : 0

Pin : 0

Power Level : Level3v3

ProjectDa1453x

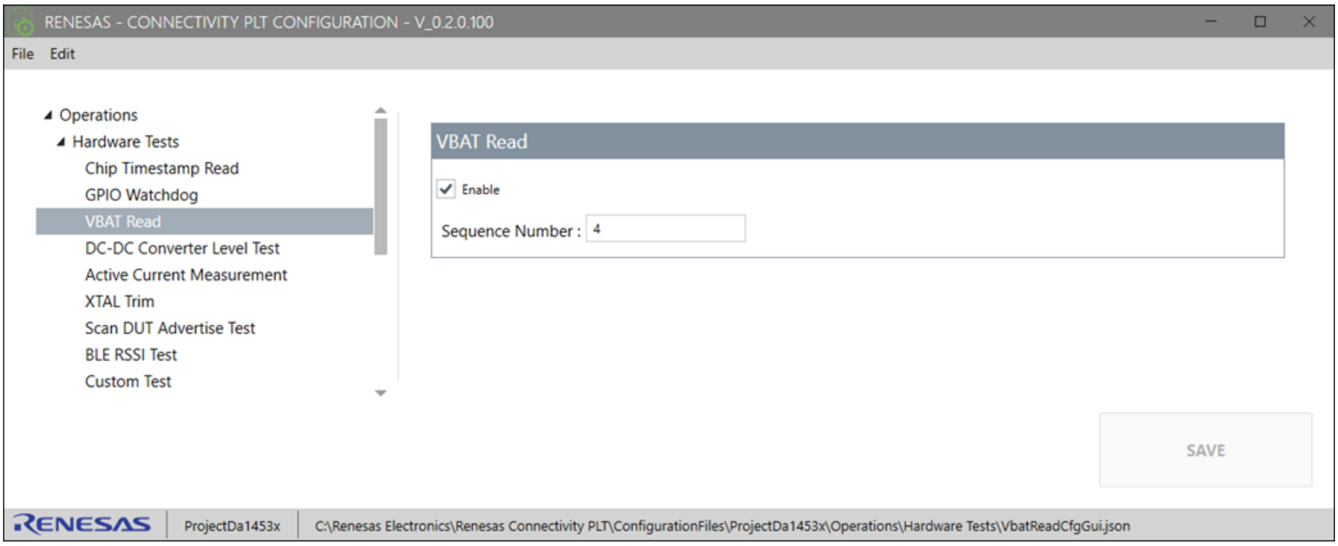
C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\ProjectDa1453x\Operations\Hardware Tests\GpioWatchdogCfgGui.json

Figure 59. GPIO watchdog configuration

8.3.3 VBAT Read

VBAT Read is available in DA14530, DA14531, DA14531MOD, DA14531_1, DA14533, DA14535, DA14530MOD, RA6W2, RRQ6105x.

This is a very useful tool to verify the operation and accuracy of the internal ADC. The VBAT level is further logged for traceability or any other purpose.



☑ Enable

Sequence Number : 4

ProjectDa1453x

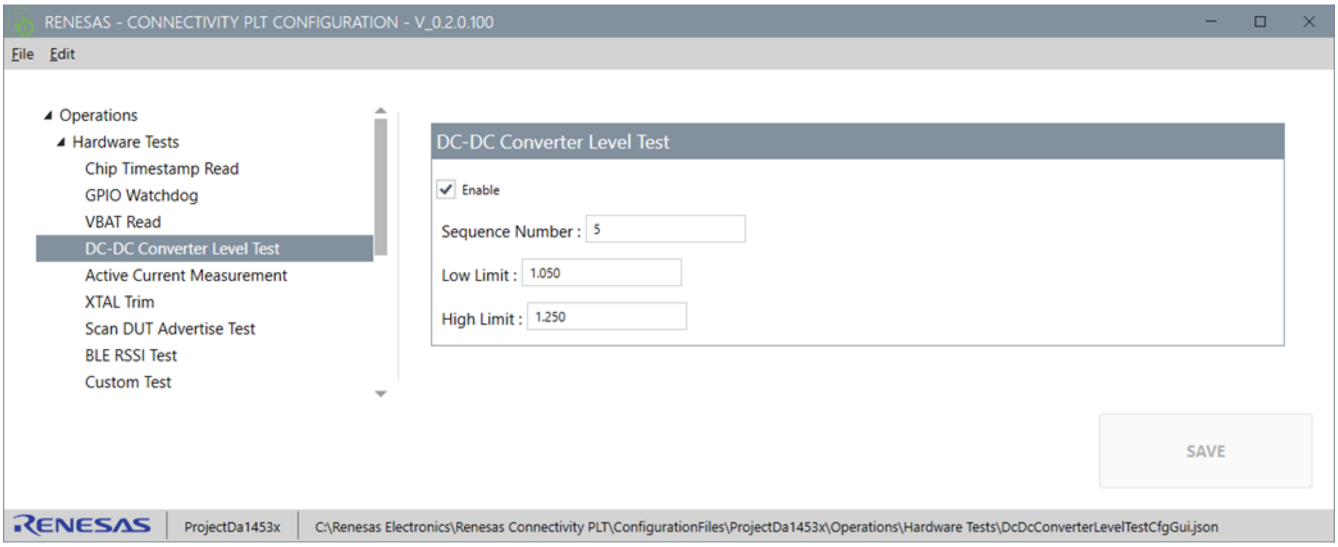
C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\ProjectDa1453x\Operations\Hardware Tests\VbatReadCfgGui.json

Figure 60. VBAT read configuration

8.3.4 DC-DC Converter Level Test

DC-DC Converter Level Test is available in DA1453x, RA6W2, RRQ6105x.

This is a useful test to check the operation of this function of the MCU and log its operating characteristics. A lower and upper limit are used to define the pass/fail criteria.


RENESAS - CONNECTIVITY PLT CONFIGURATION - V_0.2.0.100
File Edit
Operations
Hardware Tests
Chip Timestamp Read
GPIO Watchdog
VBAT Read
DC-DC Converter Level Test
Active Current Measurement
XTAL Trim
Scan DUT Advertise Test
BLE RSSI Test
Custom Test
SAVE
RENESAS
ProjectDa1453x
C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\ProjectDa1453x\Operations\Hardware Tests\DcDcConverterLevelTestCfgGui.json

DC-DC Converter Level Test

☑ Enable

Sequence Number : 5

Low Limit : 1.050

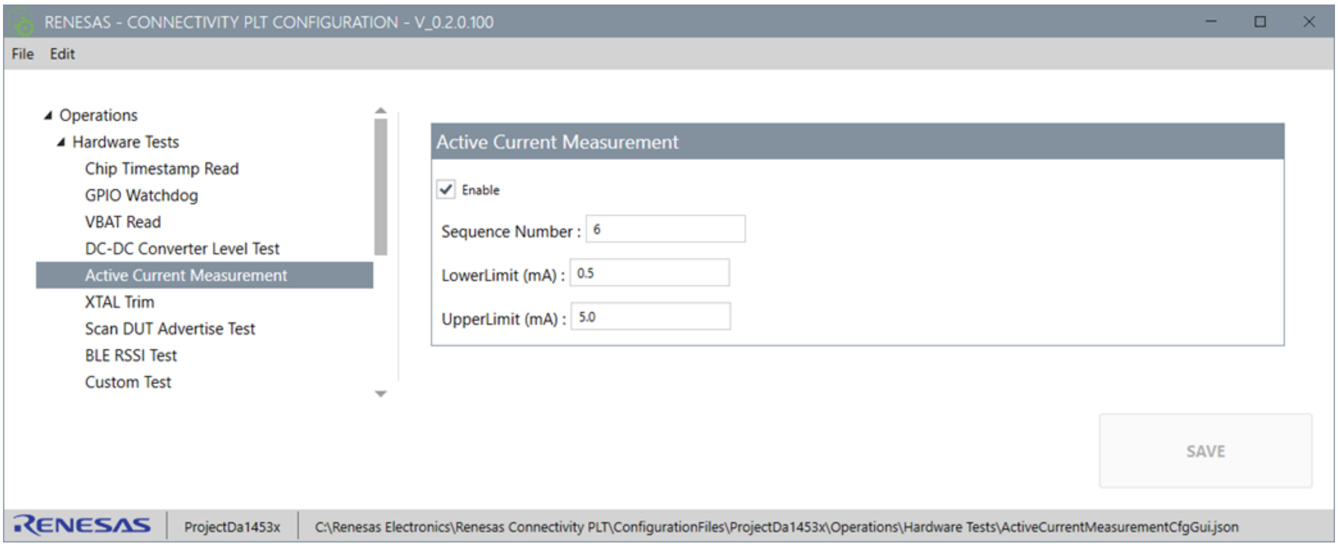
High Limit : 1.250

Figure 61. DC-DC converter configuration

8.3.5 Active Current Measurement

Active Current Measurement is available in DA1453x, RA6W1, RA6W2, RRQ6100x, RRQ6105x.

This is an extremely useful diagnostic test as the current consumption can be a significant indicator of the DUT product. An upper and lower limit are used to define the pass/fail criteria.


RENESAS - CONNECTIVITY PLT CONFIGURATION - V_0.2.0.100
File Edit
Operations
Hardware Tests
Chip Timestamp Read
GPIO Watchdog
VBAT Read
DC-DC Converter Level Test
Active Current Measurement
XTAL Trim
Scan DUT Advertise Test
BLE RSSI Test
Custom Test
SAVE
RENESAS
ProjectDa1453x
C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\ProjectDa1453x\Operations\Hardware Tests\ActiveCurrentMeasurementCfgGui.json

Active Current Measurement

☑ Enable

Sequence Number : 6

LowerLimit (mA) : 0.5

UpperLimit (mA) : 5.0

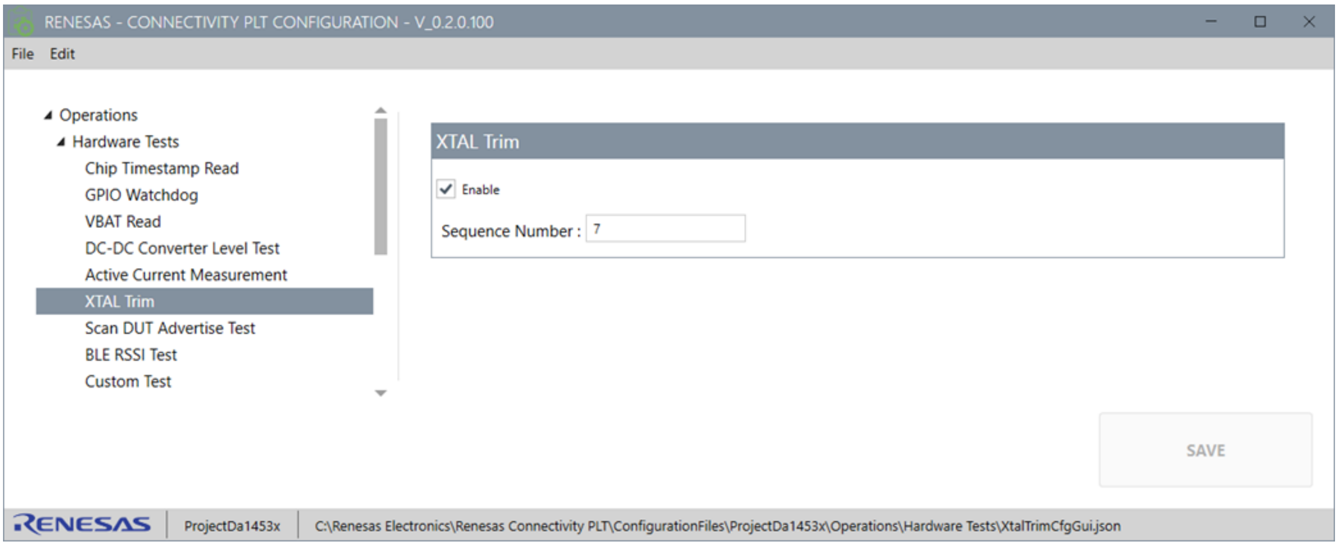
Figure 62. Active current measurement configuration

8.3.6 XTAL Trim

XTAL Trim is available in DA1453x, RA6W2, RRQ6105x.

It is recommended that all devices with RF radio go through the trim process to maintain their frequency offset to minim PPM deviation. The XTAL trim process is completed using a combination of the Connectivity PLT

Hardware clock signal and an internal calibration method of the DUT. For this process, a pin of the MCU is used to receive the calibration pulse. By default, configuration this pin is the UART RX pin.



XTAL Trim

☑ Enable

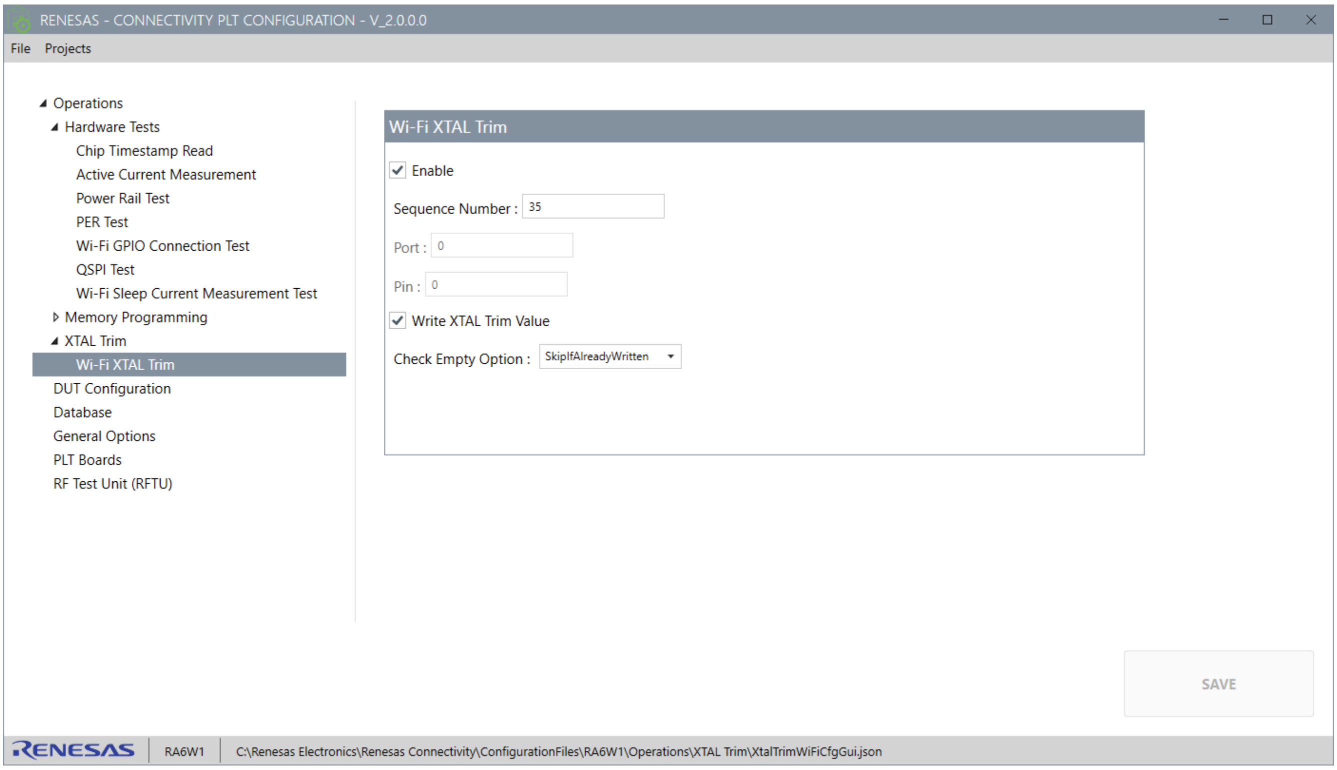
Sequence Number : 7

ProjectDa1453x | C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\ProjectDa1453x\Operations\Hardware Tests\XtalTrimCfgGui.json

Figure 63. XTAL configuration

8.3.7 XTAL Trim Wi-Fi

XTAL Trim Wi-Fi is available in RA6W, RRQ6100x.



Wi-Fi XTAL Trim

☑ Enable

Sequence Number : 35

Port : 0

Pin : 0

☑ Write XTAL Trim Value

Check Empty Option : SkipIfAlreadyWritten

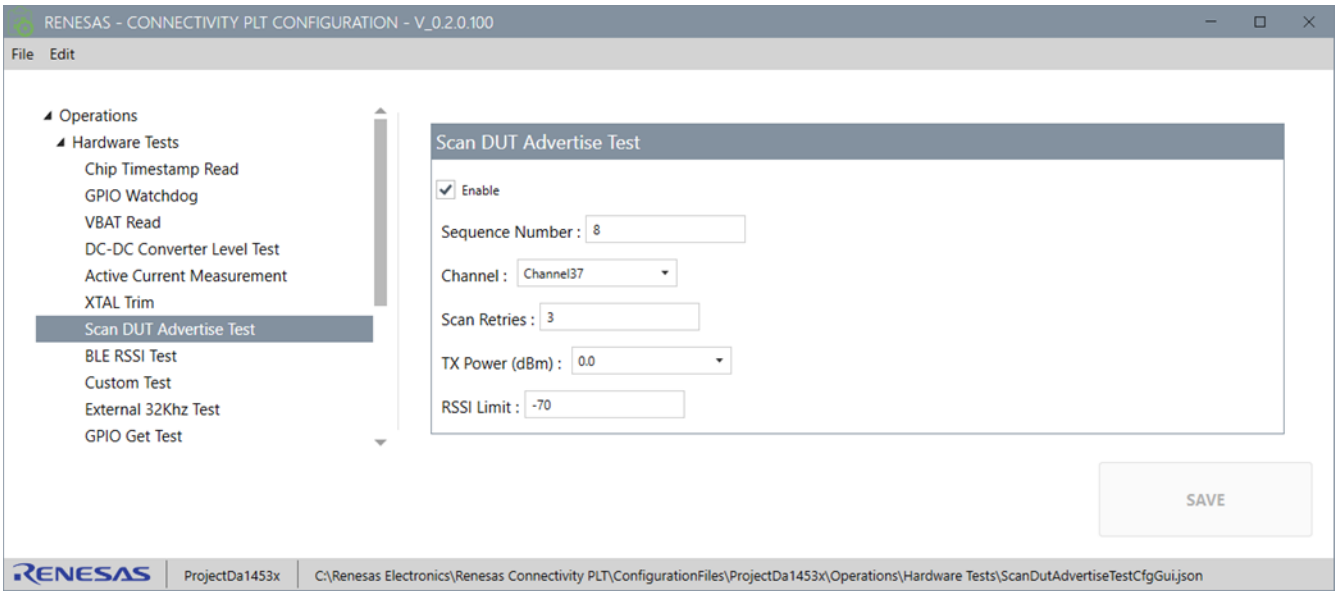
RA6W1 | C:\Renesas Electronics\Renesas Connectivity\ConfigurationFiles\RA6W1\Operations\XTAL Trim\XtalTrimWiFiCfgGui.json

Figure 64. XTAL Trim Wi-Fi

8.3.8 Scan Dut Advertise

Scan Dut Advertise is available in DA1453x, RA6W2, RRQ6105x.

This is a core test of the RF functionality of DUT. All DUTs are set in Bluetooth LE advertising mode through standard HCI commands whilst the RFTU is set in reception mode looking to capture all the BD addresses that are advertising. During the initiation of the test temporary BD addresses are issued for the DUTs, these addresses are then compared to the received ones. The pass/fail criterial is the actual reception of the advertising packet and the RSSI (signal strength) of it.



Scan DUT Advertise Test

☑ Enable

Sequence Number : 8

Channel : Channel37

Scan Retries : 3

TX Power (dBm) : 0.0

RSSI Limit : -70

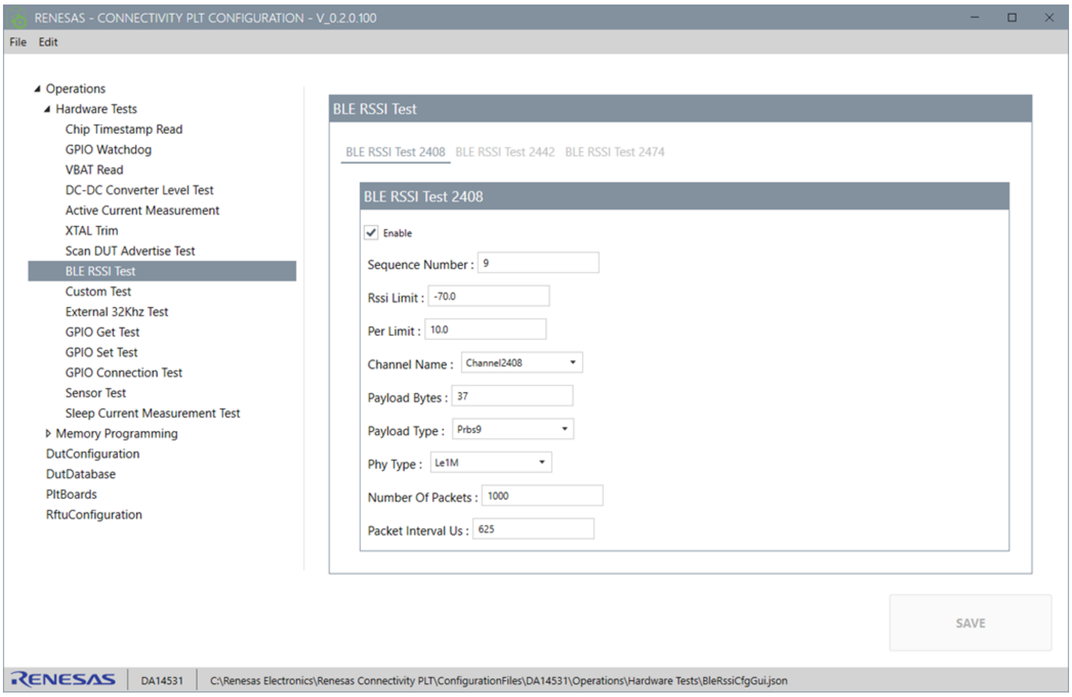
ProjectDa1453x | C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\ProjectDa1453x\Operations\Hardware Tests\ScanDutAdvertiseTestCfgGui.json

Figure 65. Scan DUT advertise configuration

8.3.9 Bluetooth LE RSSI Test

Bluetooth LE RSSI Test is available in DA1453x, RA6W2, RRQ6105x.

A set of packets is transmitted by the RTFU using the specified settings and received by all the DUTs. The metrics of the received packets are used to determine if the reception is within the acceptable range. The set metrics tested are the average RSSI and the total PER.



BLE RSSI Test

BLE RSSI Test 2408

☑ Enable

Sequence Number : 9

Rssi Limit : -70.0

Per Limit : 10.0

Channel Name : Channel2408

Payload Bytes : 37

Payload Type : Prbs9

Phy Type : Le1M

Number Of Packets : 1000

Packet Interval Us : 625

DA14531 | C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531\Operations\Hardware Tests\BleRssiCfgGui.json

Figure 66. Bluetooth LE RSSI configuration

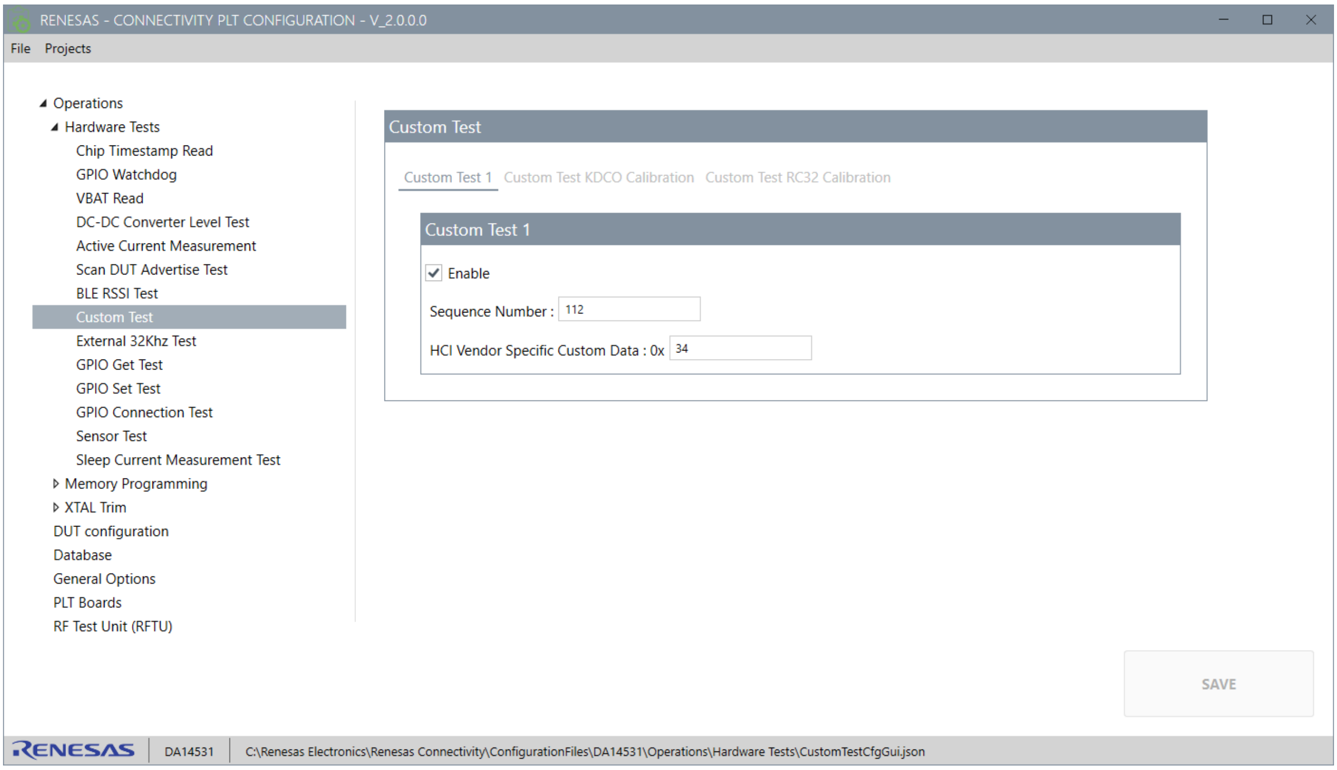
The RSSI Limit is the lowest acceptable level for the DUT to pass the test. The result is calculated by averaging the RSSI measurement of all packets.

The PER Limit if the highest acceptable level for the DUT to pass the test The result is calculated by the total packet errors.

8.3.10 Custom Test

Custom Test is available in DA1453x, RA6W2, RRQ6105x.

The tests are commonly used for extended sensor test procedures that require more than a single read-write operation. By default, a return value same as the command value indicates a pass status.



☑ Enable

Sequence Number : 112

HCI Vendor Specific Custom Data : 0x 34

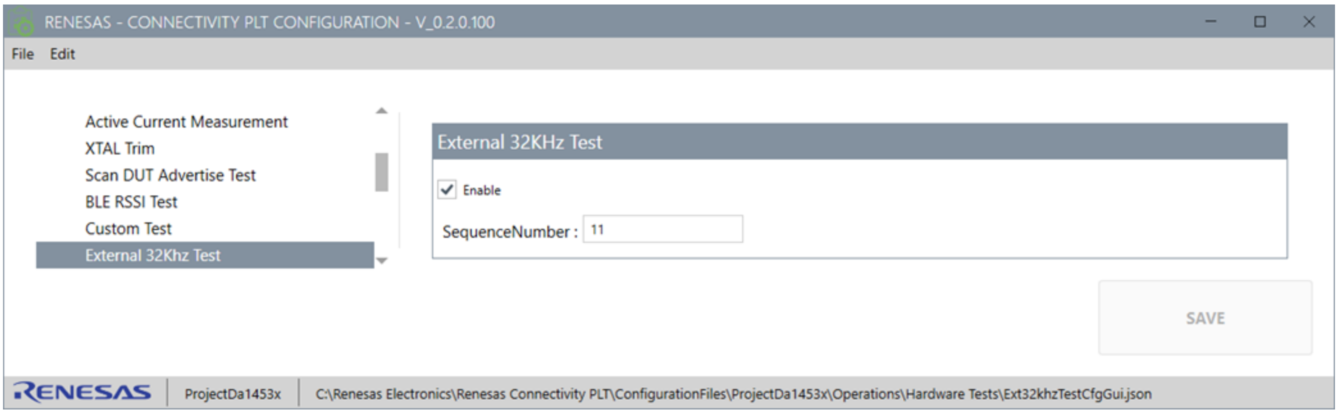
DA14531 | C:\Renesas Electronics\Renesas Connectivity\ConfigurationFiles\DA14531\Operations\Hardware Tests\CustomTestCfgGui.json

Figure 67. Custom test configuration

8.3.11 External 32-kHz Test

External 32-kHz Test is available in DA1453x, RA6W2, RRQ6105x.

Its frequency is measured against the main clock source of the DUT. This test is only applicable on devices that support secondary oscillators.



☑ Enable

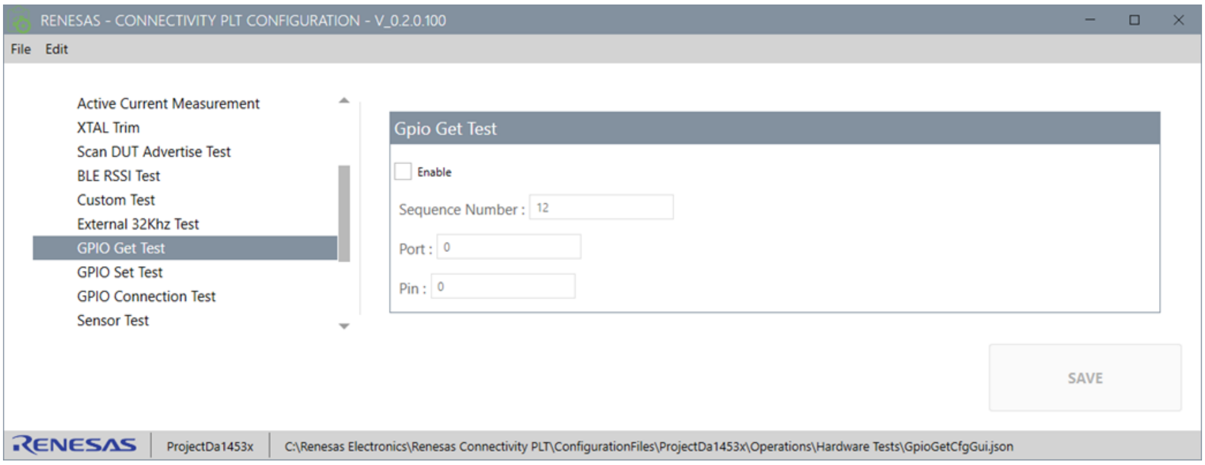
SequenceNumber : 11

ProjectDa1453x | C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\ProjectDa1453x\Operations\Hardware Tests\Ext32khzTestCfgGui.json

Figure 68. Ext32kHz crystal test configuration

8.3.12 GPIO Get Test

GPIO Get Test is available in DA1453x, RA6W2, RRQ6105x.



Gpio Get Test

□ Enable

Sequence Number : 12

Port : 0

Pin : 0

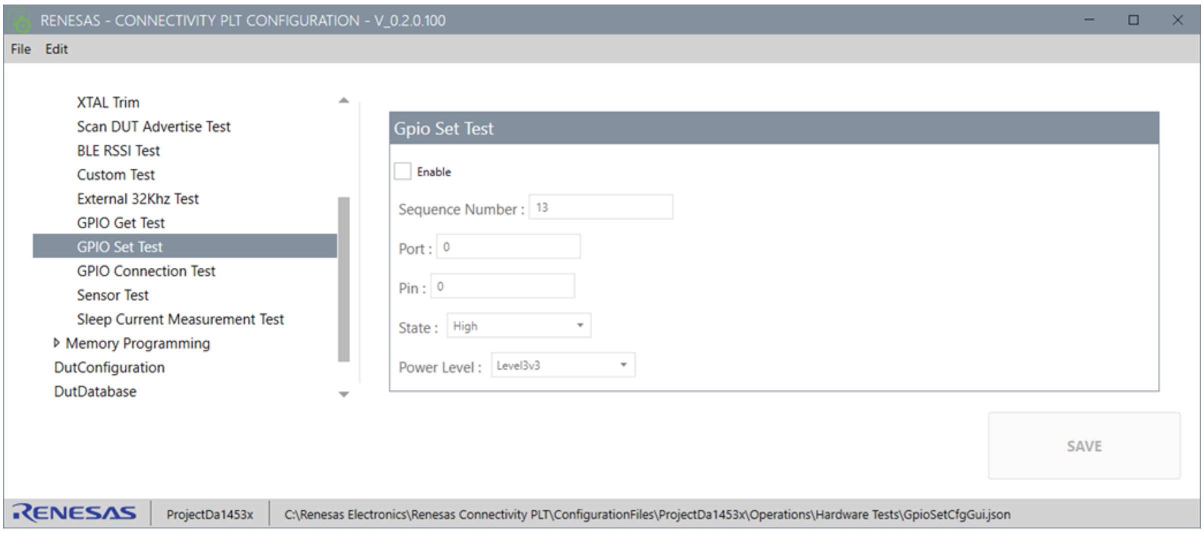
ProjectDa1453x

C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\ProjectDa1453x\Operations\Hardware Tests\GpioGetCfgGui.json

Figure 69. GPIO get configuration

8.3.13 GPIO Set Test

GPIO Set Test is available in DA1453x, RA6W2, RRQ6105x.



Gpio Set Test

□ Enable

Sequence Number : 13

Port : 0

Pin : 0

State : High

Power Level : Level3v3

ProjectDa1453x

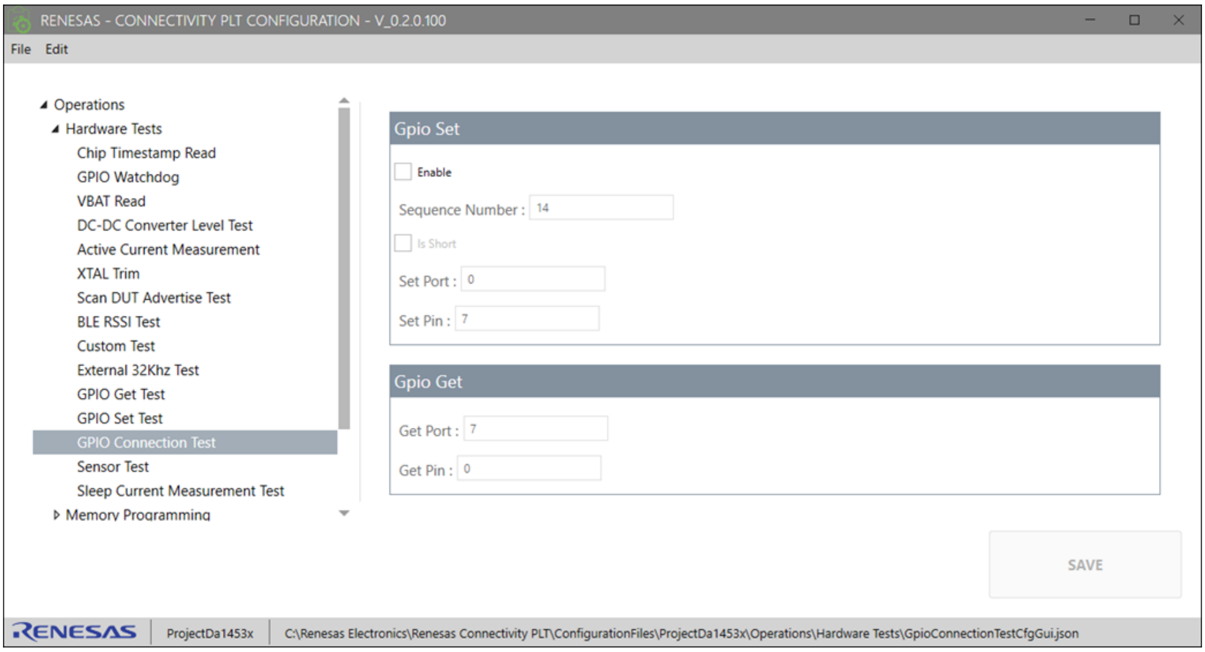
C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\ProjectDa1453x\Operations\Hardware Tests\GpioSetCfgGui.json

Figure 70. GPIO set configuration

8.3.14 GPIO Connection Test

GPIO Connection Test is available in DA1453x, RA6W1, RA6W2, RRQ6100x , RRQ6105x.

If the **Is Short** option is enabled, the operation checks whether **Set Pin** has the same level as **Get Pin** for all retries. Alternatively, the operation checks whether **Get Pin** is always low no matter what the **Set Pin** level is.


RENESAS - CONNECTIVITY PLT CONFIGURATION - V_0.2.0.100
File
Edit
Operations
Hardware Tests
Chip Timestamp Read
GPIO Watchdog
VBAT Read
DC-DC Converter Level Test
Active Current Measurement
XTAL Trim
Scan DUT Advertise Test
BLE RSSI Test
Custom Test
External 32Khz Test
GPIO Get Test
GPIO Set Test
GPIO Connection Test
Sensor Test
Sleep Current Measurement Test
Memory Programming
SAVE
ProjectDa1453x
C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\ProjectDa1453x\Operations\Hardware Tests\GpioConnectionTestCfgGui.json

Gpio Set

☐ Enable

Sequence Number : 14

☐ Is Short

Set Port : 0

Set Pin : 7

Gpio Get

Get Port : 7

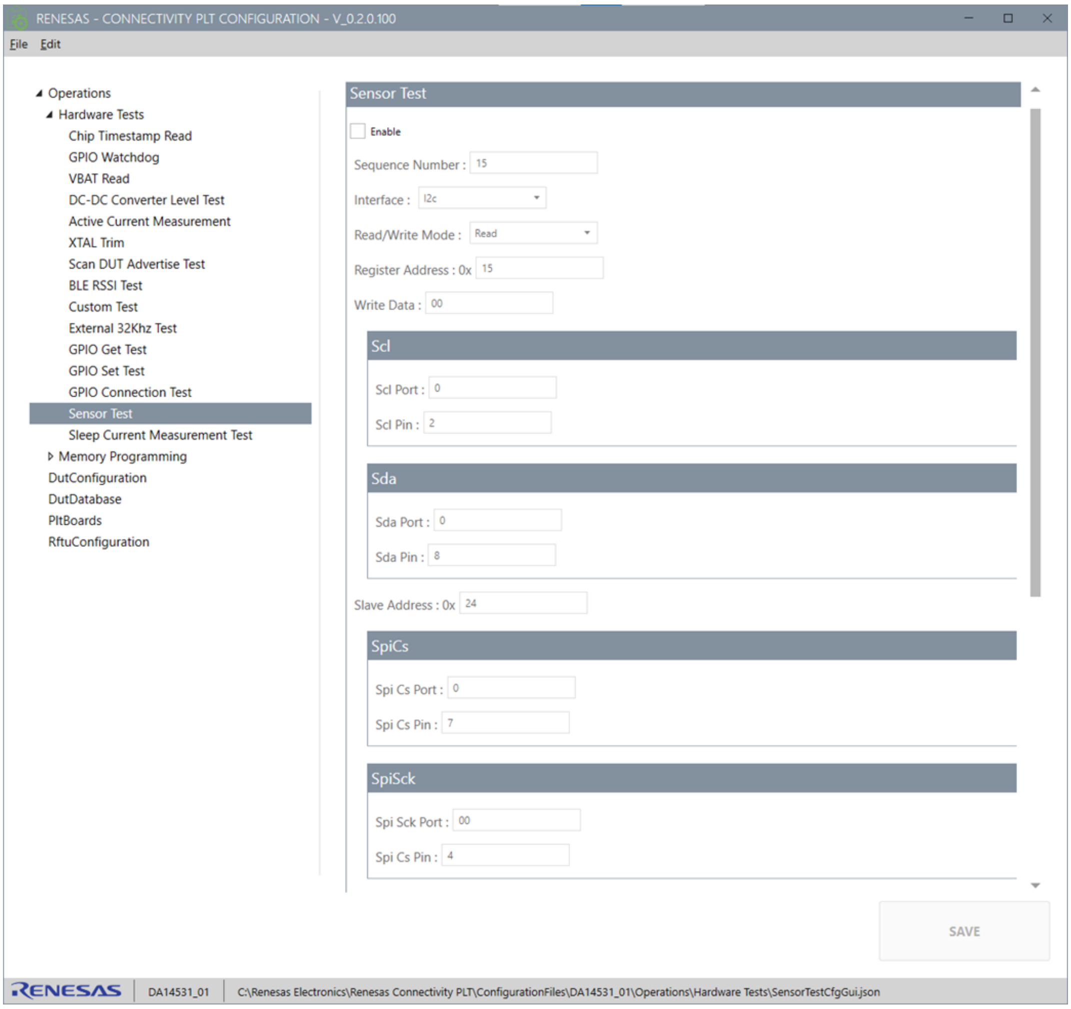
Get Pin : 0

Figure 71. GPIO connection configuration

8.3.15 Sensor Test

Sensor Test is available in DA1453x, RA6W2, RRQ6105x.

The operation can perform read and write functions to the sensor at a specified register address. In the case of I2C devices the I2C address needs to be specified in 7-bit format. If the read function is used the **Expected Data** field is compared with the result to determine the success of the test. When the write function is used, it is followed by a read test to verify that the value written is correct, this determines the test result.



Sensor Test

□ Enable

Sequence Number : 15

Interface : I2c

Read/Write Mode : Read

Register Address : 0x 15

Write Data : 00

Scl

Scl Port : 0

Scl Pin : 2

Sda

Sda Port : 0

Sda Pin : 8

Slave Address : 0x 24

SpiCs

Spi Cs Port : 0

Spi Cs Pin : 7

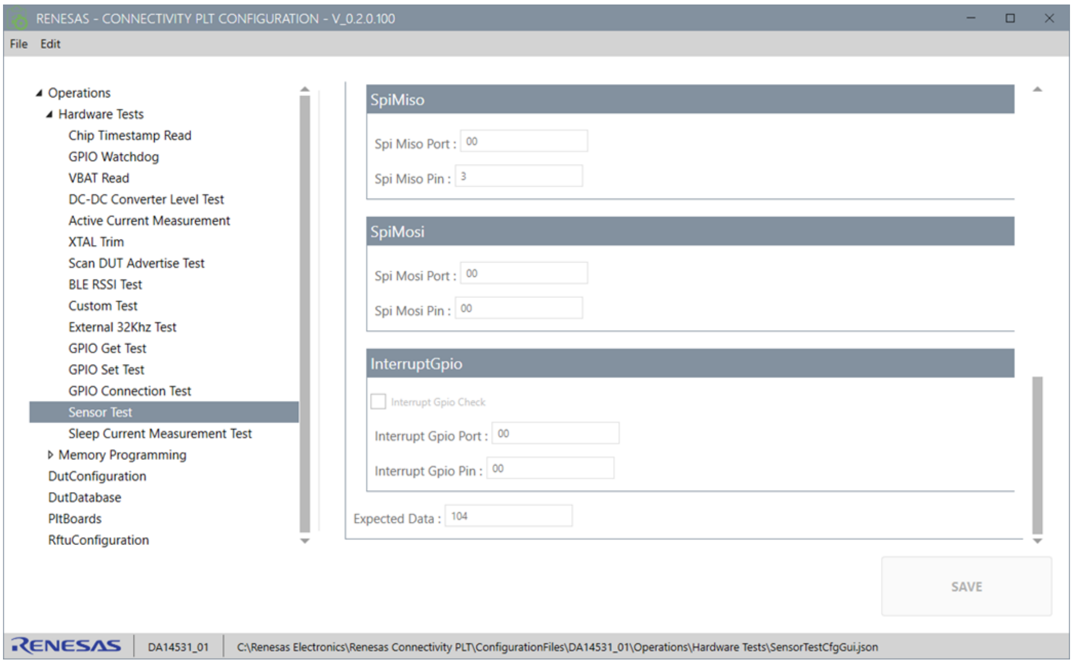
SpiSck

Spi Sck Port : 00

Spi Cs Pin : 4

DA14531_01 | C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\Operations\Hardware Tests\SensorTestCfgGui.json

Figure 72. Sensor test configuration 1



SpiMiso

Spi Miso Port : 00

Spi Miso Pin : 3

SpiMosi

Spi Mosi Port : 00

Spi Mosi Pin : 00

InterruptGpio

□ Interrupt Gpio Check

Interrupt Gpio Port : 00

Interrupt Gpio Pin : 00

Expected Data : 104

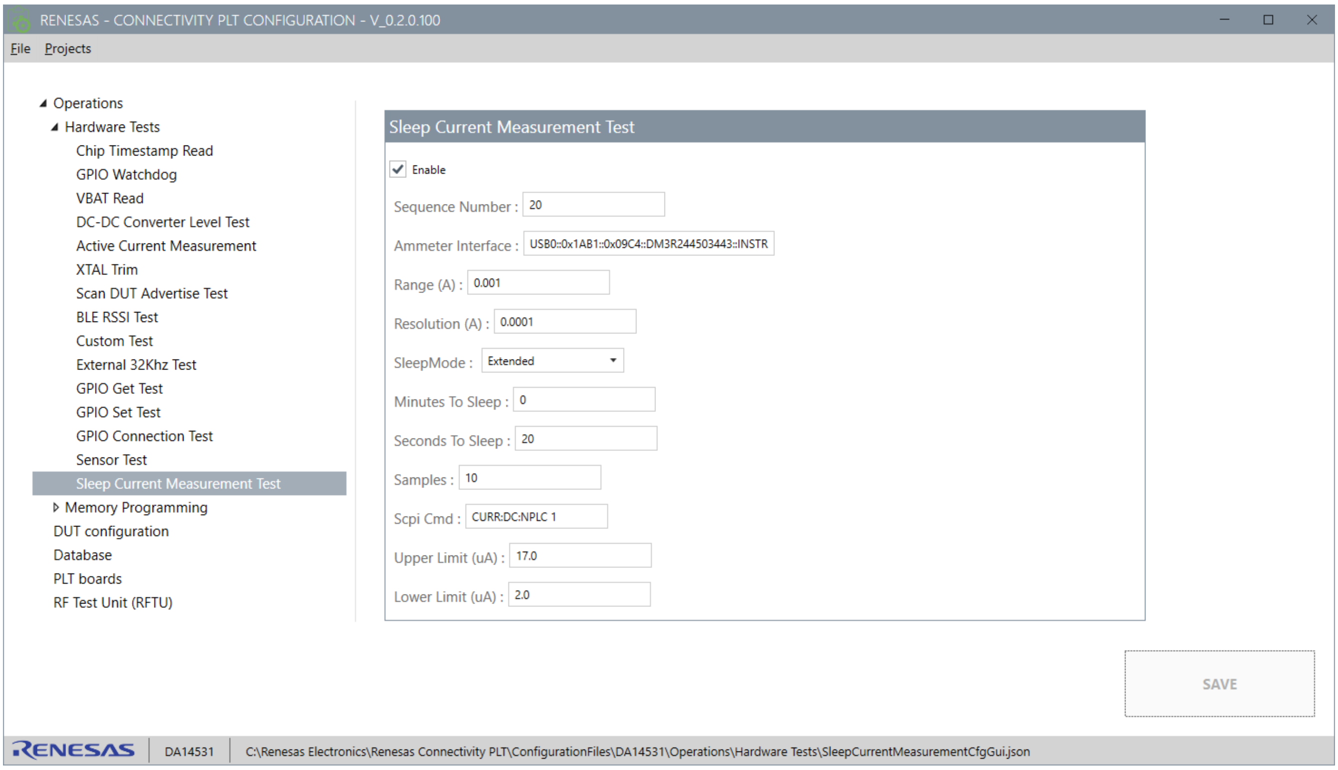
DA14531_01 | C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\Operations\Hardware Tests\SensorTestCfgGui.json

Figure 73. Sensor test configuration 2

8.3.16 Sleep Current Measurement Test

Sleep Current Measurement Test is available in DA1453x.

Due to the extremely low currents, an external DMM instrument is required for this operation to make very accurate measurements. For details on the instrument and connectivity, see Section 5.4.2. The measurement is performed on the VDUT power supply of the Connectivity PLT and is cumulative of the current from all DUTs. The result is divided by the number of active DUTs, report and compared to pass/fail criteria.



Sleep Current Measurement Test

☑ Enable

Sequence Number : 20

Ammeter Interface : USB0::0x1AB1::0x09C4::DM3R244503443::INSTR

Range (A) : 0.001

Resolution (A) : 0.0001

SleepMode : Extended

Minutes To Sleep : 0

Seconds To Sleep : 20

Samples : 10

Scpi Cmd : CURR:DC:NPLC 1

Upper Limit (uA) : 17.0

Lower Limit (uA) : 2.0

DA14531 | C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531\Operations\Hardware Tests\SleepCurrentMeasurementCfgGui.json

Figure 74. Sleep current measurement configuration

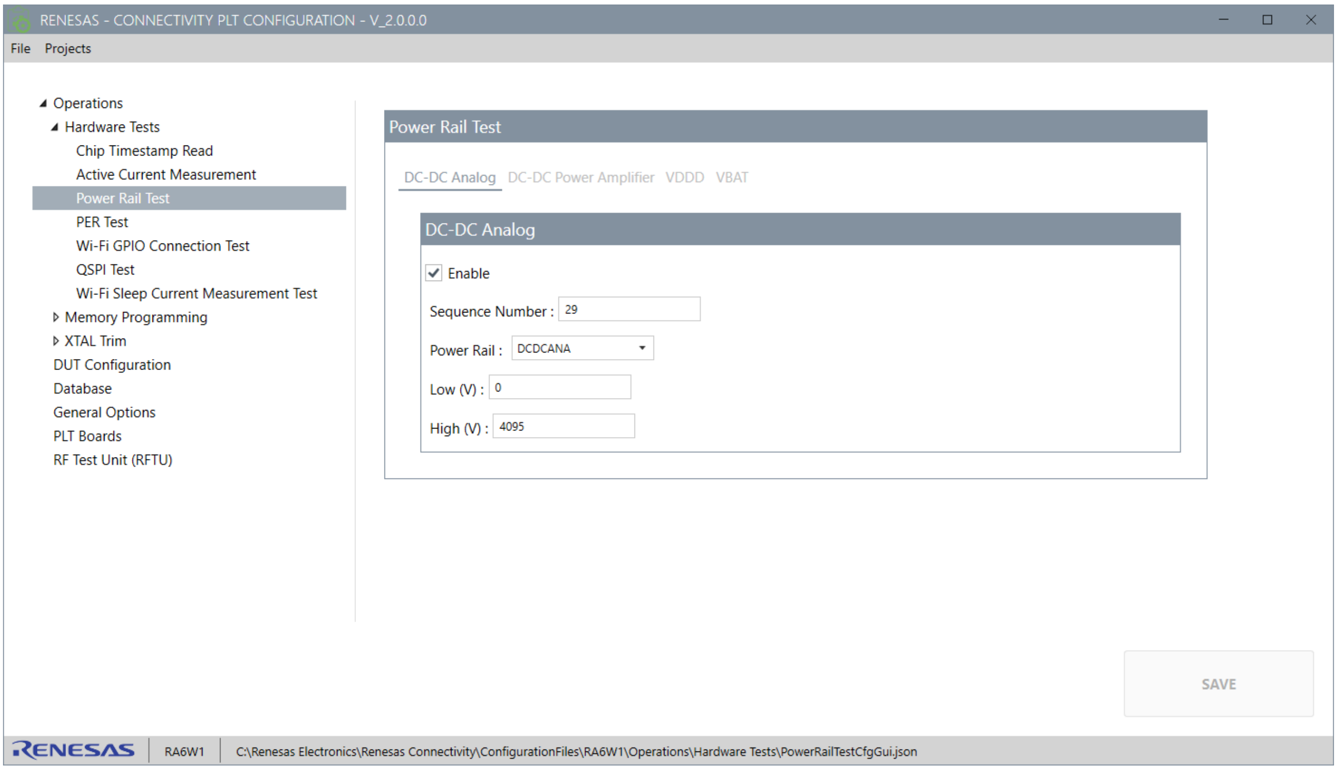
Configuration details:

- Ammeter Interface: the NI VISA address of the instrument (can be obtained by the NI Max application).
- Range: the set range of the instrument. The actual range values depends on the instrument. Typical values are 1 µA, 10 µ A, 100 µ A, 1 mA, 10 mA, 100 mA, 1 A, 3 A, 10 A. The value must be entered in ampere. Default value is 1 mA. This range must be able to accommodate the sleep current of all DUTs connected to a single Connectivity PLT board.
- Resolution: the set resolution for the instrument. The actual resolution depends on the instrument. The acceptable values are between 0 and 7 decimal places. Note that many instruments do not use this command and the range sets the resolution as well.
- Sleep mode: Sleep mode depends on the CPU supported modes, typically an active, extended and deep sleep mode is support. Current consumption differs between these modes.
- Minutes/Seconds to sleep: the time the device is set to wake up after switching to sleep mode. The CPU of the DUTs uses a timer interrupt to wake up since for the sleep operation most I/O is commonly disabled including the reset pin. These settings also determine the length of time after which the measurement is made which happens just before the device wakes up.
- Sample: the number of samples to be taken and averaged.
- SCPI CMD: additional SCPI command, usually specific to the instrument used. The default CURR:DC:NPLC 1 sets the sampling type to one NPLC cycle.
- Upper/Lower limits: sets the pass/fail criterial for the sleep current value per DUT.

8.3.17 Power Rail Test

Power Rail Test is available in RA6W1, RA6W2, RRQ6100x, RRQ6105x.
The aim of this test is to verify that the power supplies of the chip function properly. There are seven power domains: VDDIO1, VDDIO2, VDDIO_FDIO, VBAT, VDDD, DCDC_PA_OUT, and DCDC_ANA_OUT.

8.3.17.1 DC-DC Analog



☑ Enable

Sequence Number : 29

Power Rail : DCDCANA

Low (V) : 0

High (V) : 4095

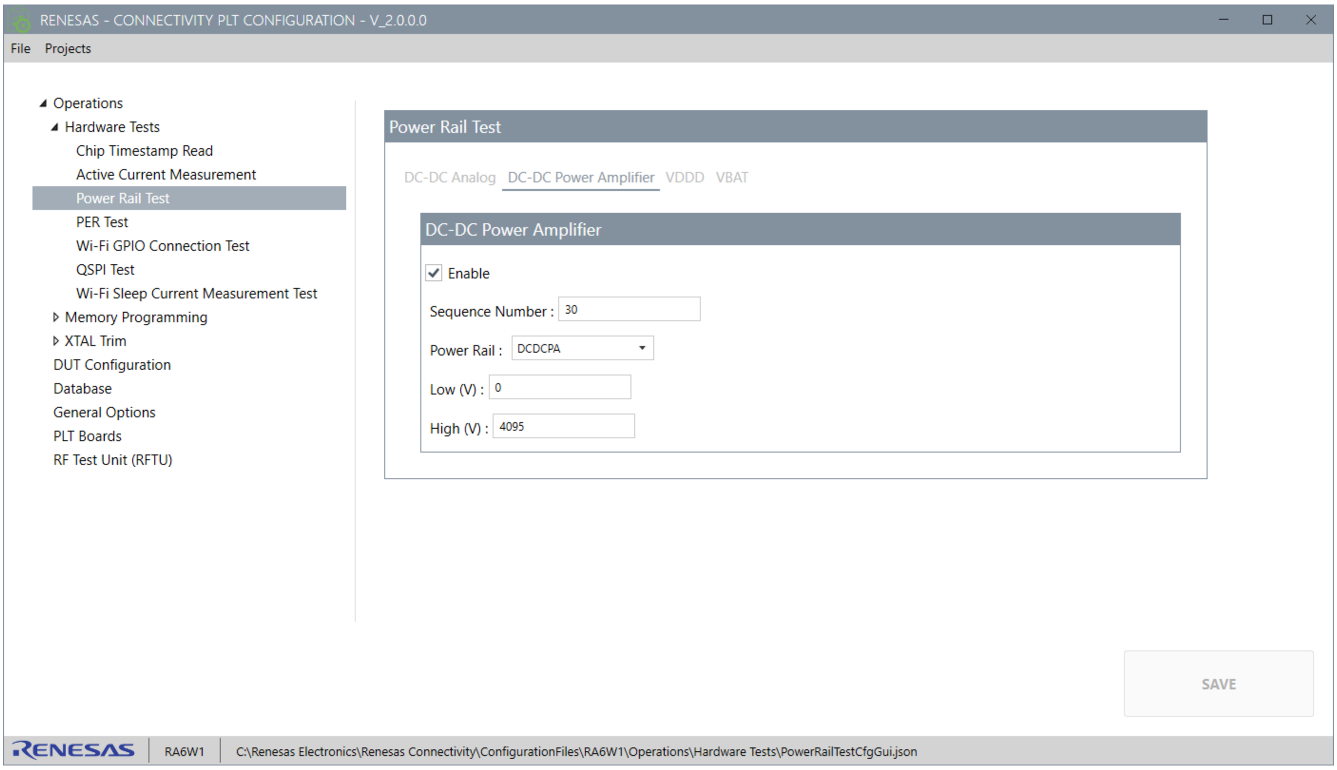
C:\Renesas Electronics\Renesas Connectivity\ConfigurationFiles\RA6W1\Operations\Hardware Tests\PowerRailTestCfgGui.json

Figure 75. DC-DC Analog Configuration

Table 30. DC-DC Analog

Option	Description
Enable	This enables the specific memory reading operation.
Sequence Number	The order in which the test is run in execution.
Power Rail	Select the rail to configure.
ADC Value Read – Min Limit	Minimum accepted value of ADC.
ADC Value Read – Max Limit	Maximum accepted value of ADC

8.3.17.2 DC-DC Power Amplifier



☑ Enable

Sequence Number : 30

Power Rail : DCDCPA

Low (V) : 0

High (V) : 4095

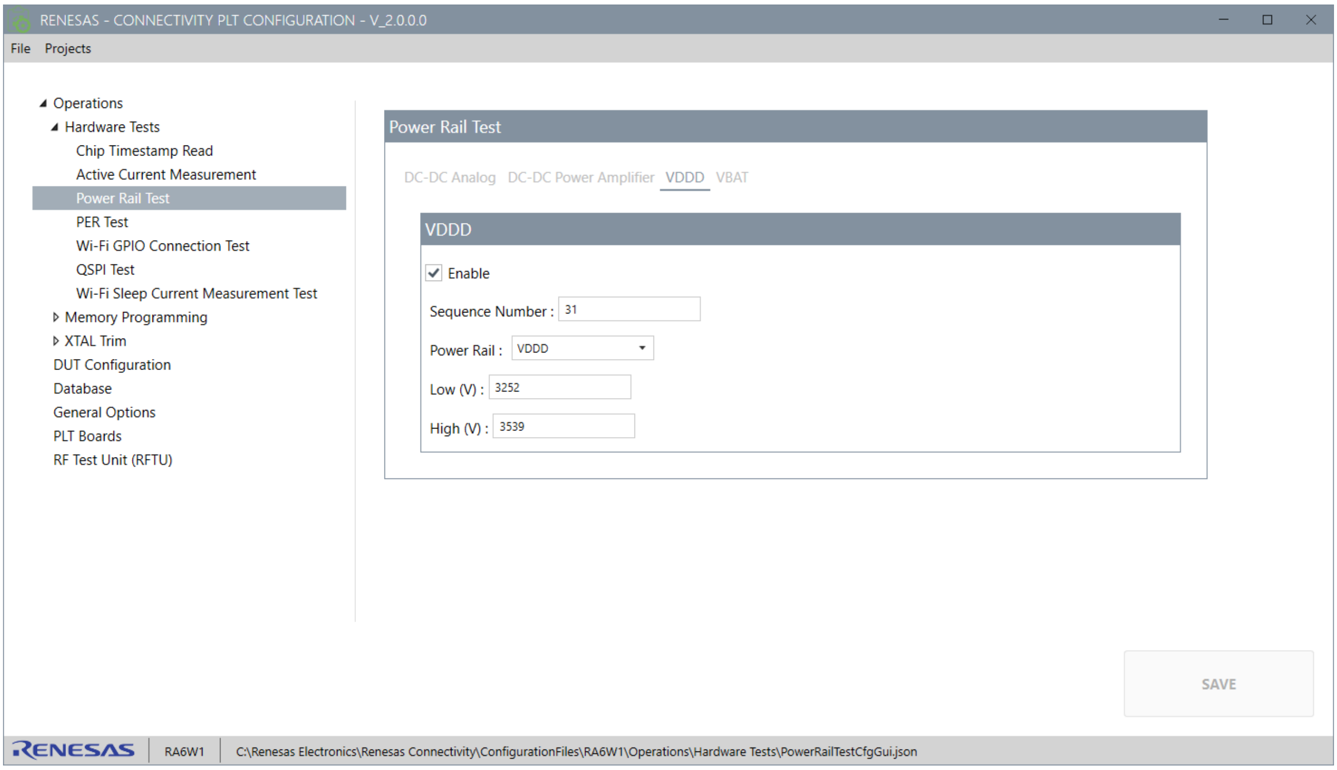
C:\Renesas Electronics\Renesas Connectivity\ConfigurationFiles\RA6W1\Operations\Hardware Tests\PowerRailTestCfgGui.json

Figure 76. DC-DC Power Amplifier

Table 31. DC-DC Poer Amplifier

Option	Description
Enable	This enables the specific memory reading operation.
Sequence Number	The order in which the test is run in execution.
Power Rail	Select the rail to configure.
ADC Value Read – Min Limit	Minimum accepted value of ADC.
ADC Value Read – Max Limit	Maximum accepted value of ADC

8.3.17.3 DC-DC VDD



☑ Enable

Sequence Number : 31

Power Rail : VDDD

Low (V) : 3252

High (V) : 3539

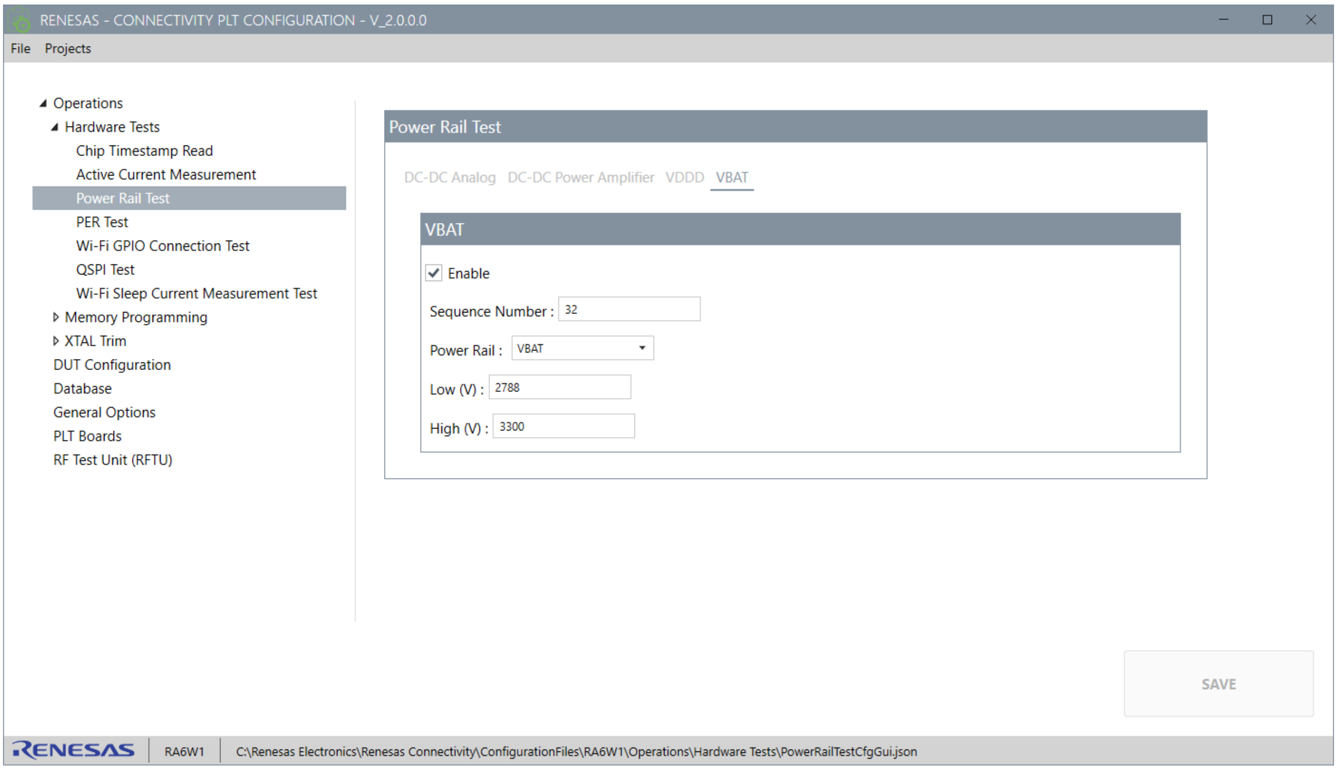
C:\Renesas Electronics\Renesas Connectivity\ConfigurationFiles\RA6W1\Operations\Hardware Tests\PowerRailTestCfgGui.json

Figure 77. DC-DC VDD

Table 32. DC-DC VDD

Option	Description
Enable	This enables the specific memory reading operation.
Sequence Number	The order in which the test is run in execution.
Power Rail	Select the rail to configure.
ADC Value Read – Min Limit	Minimum accepted value of ADC.
ADC Value Read – Max Limit	Maximum accepted value of ADC.

8.3.17.4 DC-DC VBAT


RENESAS - CONNECTIVITY PLT CONFIGURATION - V_2.0.0.0
File
Projects
Operations
Hardware Tests
Chip Timestamp Read
Active Current Measurement
Power Rail Test
PER Test
Wi-Fi GPIO Connection Test
QSPI Test
Wi-Fi Sleep Current Measurement Test
Memory Programming
XTAL Trim
DUT Configuration
Database
General Options
PLT Boards
RF Test Unit (RFTU)
Power Rail Test
DC-DC Analog
DC-DC Power Amplifier
VDDD
VBAT
VBAT
SAVE
RENESAS
RA6W1
C:\Renesas Electronics\Renesas Connectivity\ConfigurationFiles\RA6W1\Operations\Hardware Tests\PowerRailTestCfgGui.json

☑ Enable

Sequence Number : 32

Power Rail : VBAT

Low (V) : 2788

High (V) : 3300

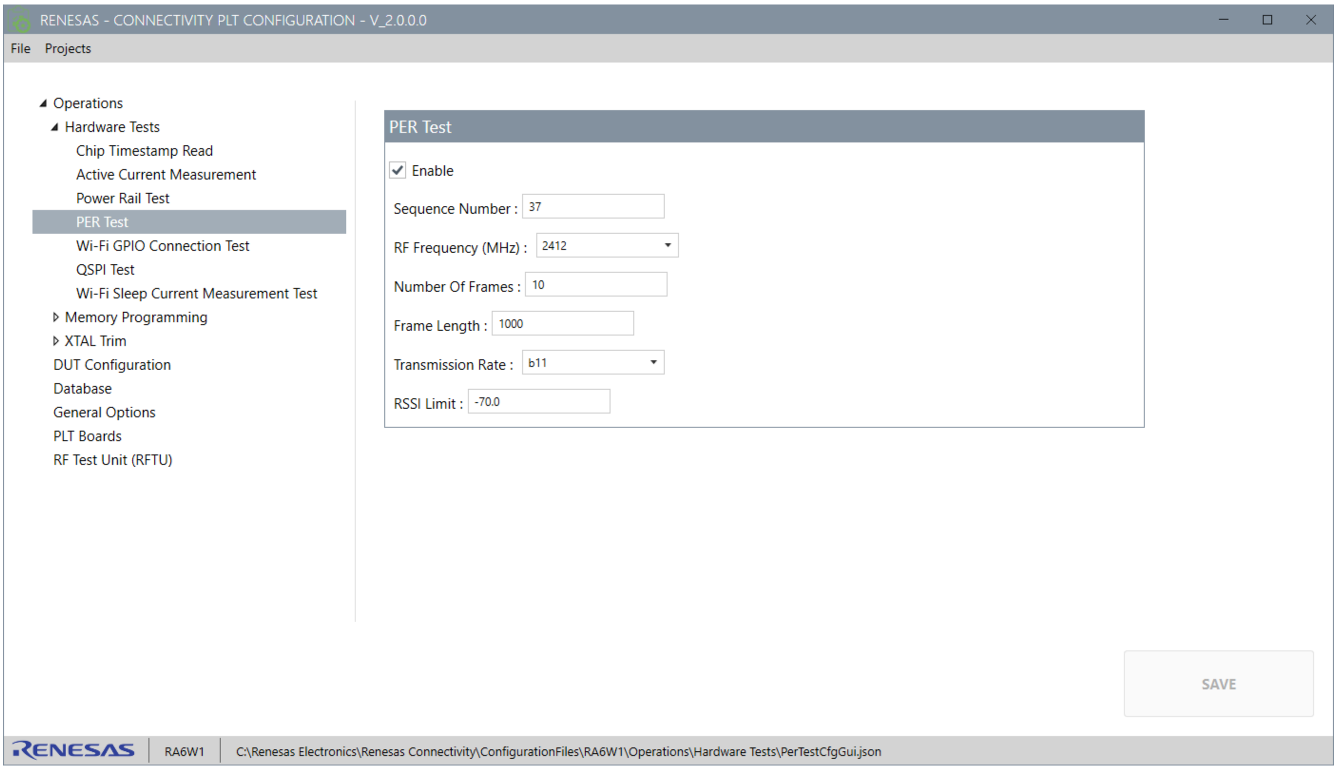
Figure 78. DC-DC VBAT

Table 33. DC-DC VBAT

Option	Description
Enable	This enables the specific memory reading operation.
Sequence Number	The order in which the test is run in execution.
Power Rail	Select the rail to configure.
ADC Value Read – Min Limit	Minimum accepted value of ADC.
ADC Value Read – Max Limit	Maximum accepted value of ADC

8.3.18 Packet Error Rate (PER) Test

Packet Error Rate (PER) Test is available in RA6W1, RA6W2, RRQ6100x, RRQ6105x



☑ Enable

Sequence Number : 37

RF Frequency (MHz) : 2412

Number Of Frames : 10

Frame Length : 1000

Transmission Rate : b11

RSSI Limit : -70.0

C:\Renesas Electronics\Renesas Connectivity\ConfigurationFiles\RA6W1\Operations\Hardware Tests\PerTestCfgGui.json

Figure 79. PER Test

Table 34. PER Test

Option	Description
Enable	This enables the specific memory reading operation.
Rf Frequency (MHz)	The Rf frequency in MHz.
Number of frames	The number of frames.
Frame Length	The length of the frame.
Transmission Rate	Transmission Rate.
RSSI Limit	RSSI limit

8.4 Memory Programming Configuration

The memory programming group contains operations for reading and writing to different types of memories internal and external to the MCU. In addition to simple binary read/write operations special memory areas can be configured and programmed.

Table 35 summarizes all memory programing operations.

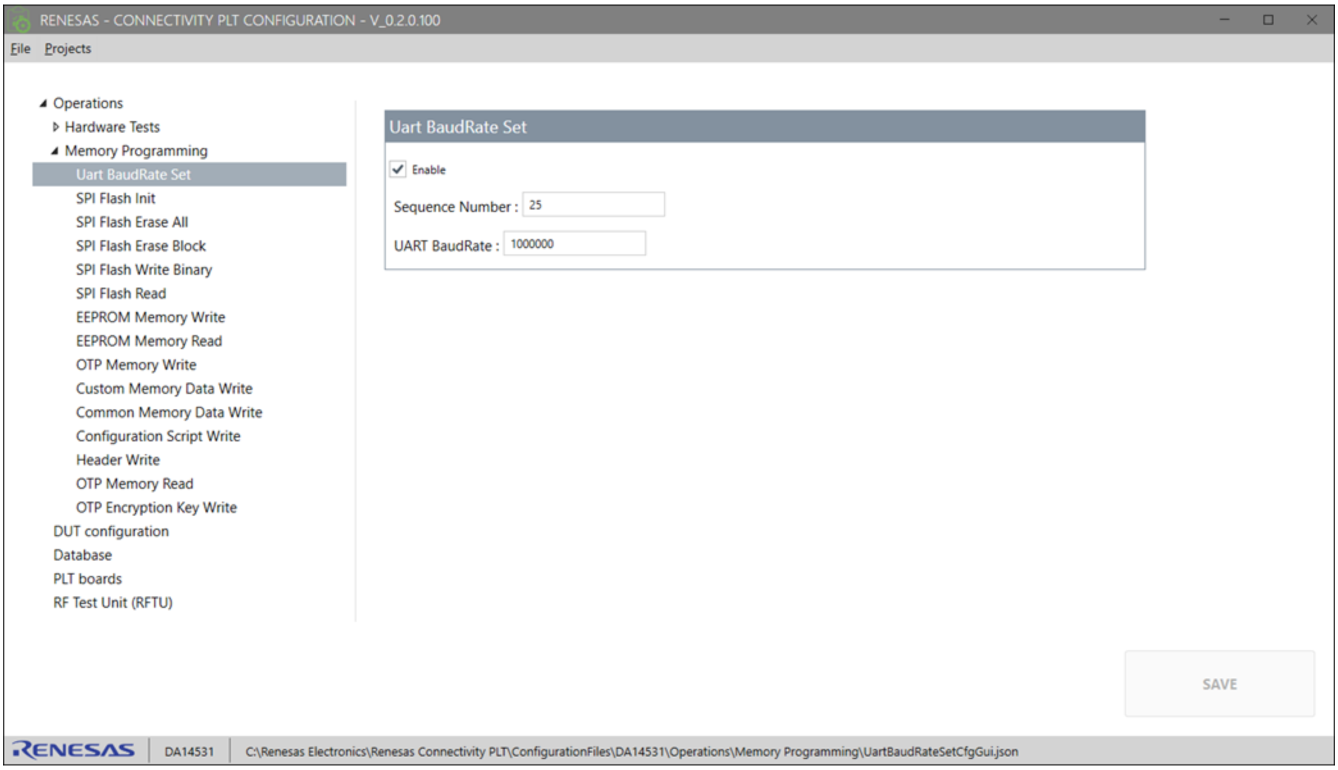
Table 35. Types of memory tests

Operation type	Description
UART BaudRate Set	Sets the baud rate of the UART for all memory operations. See Section 8.4.1.
SPI Flash Init	Initializes the external flash memory controller which internally defines the pins used and other settings as configured in the peripheral configuration page. See Section 8.4.2.
SPI Flash Erase All	Performs a chip erase on the flash memory. See Section 8.4.3.

Operation type	Description
SPI Flash Erase Block	Erases specific memory blocks. See Section 8.4.4.
SPI Flash Write Binary	Writes an entire binary to flash memory. See Section 8.4.5.
SPI Flash Read	Reads the flash memory with the specified settings. See Section 8.4.6.
Eeprom Memory Write	Writes an entire binary to an external EERPOM memory. See Section 8.4.7.
Eeprom Memory Read	Reads data from external EEPROM memory. See Section 8.4.8.
OTP Memory Write	Writes an entire binary to the OTP memory. See Section 8.4.9.
OTP Memory Read	Reads data from the OTP memory. See Section 8.4.10.
Header Write	Writes in the special memory area of OTP Header. See Section 8.4.11.
Configuration Script Write	Writes entries to the configuration script area of the OTP. See Section 8.4.12.
Custom Memory Data Write	Writes data to Flash or OTP memory that are stored in the devices database and are specific for each serial number. See Section 8.4.13.
Common Memory Data Write	Writes data to Flash or OTP memory that are stored in the devices database. See Section 8.4.14.
QSPI Flash Block Erase	Erases specific QSPI flash memory blocks. See Section 8.4.15
QSPI Flash Write Binary	Writes an entire binary to QSPI flash memory. See Section 8.4.16
QSPI Flash Read	Reads the QSPI flash memory with the specified settings. See Section 8.4.17
QSPI Flash Erase All	Performs a chip erase on the QSPI flash memory. See Section 8.4.18
QSPI Test	Gets the JEDEC ID from QSPI flash Memory. See Section 8.4.19
Wi-Fi Configuration Script Write	Writes entries to the configuration script area of the OTP. See Section 8.4.20

8.4.1 Uart BaudRate Set

Uart BaudRate Set is available in DA1453x.



☑ Enable

Sequence Number : 25

UART BaudRate : 1000000

DA14531 | C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531\Operations\Memory Programming\UartBaudRateSetCfgGui.json

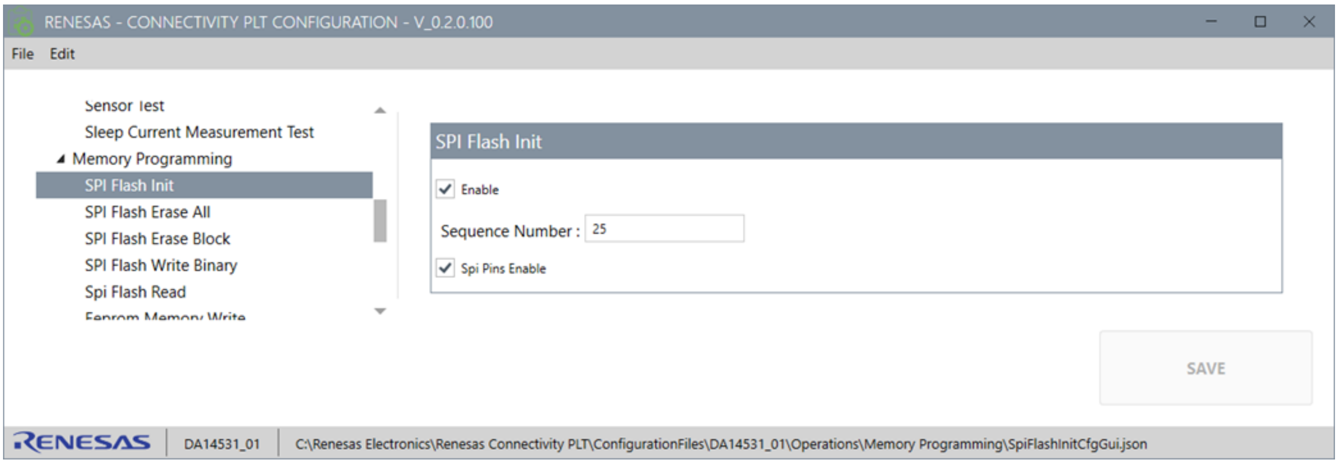
Figure 80. Uart BaudRate Set configuration

Table 36. Uart BaudRate Set configuration

Option	Description
Enable	This enables the UART Set baud rate operation.
Sequence Number	The order in which the test is run in execution
UART BaudRate	The baud rate to set up in bps 9600, 19200, 57600, 115200, 1000000 Note: if the default 115200 the operation doesn't need to be enabled.

8.4.2 SPI Flash Init

SPI Flash Init is available in DA1453x.



SPI Flash Init

☑ Enable

Sequence Number : 25

☑ Spi Pins Enable

DA14531_01 C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\Operations\Memory Programming\SpiFlashInitCfgGui.json

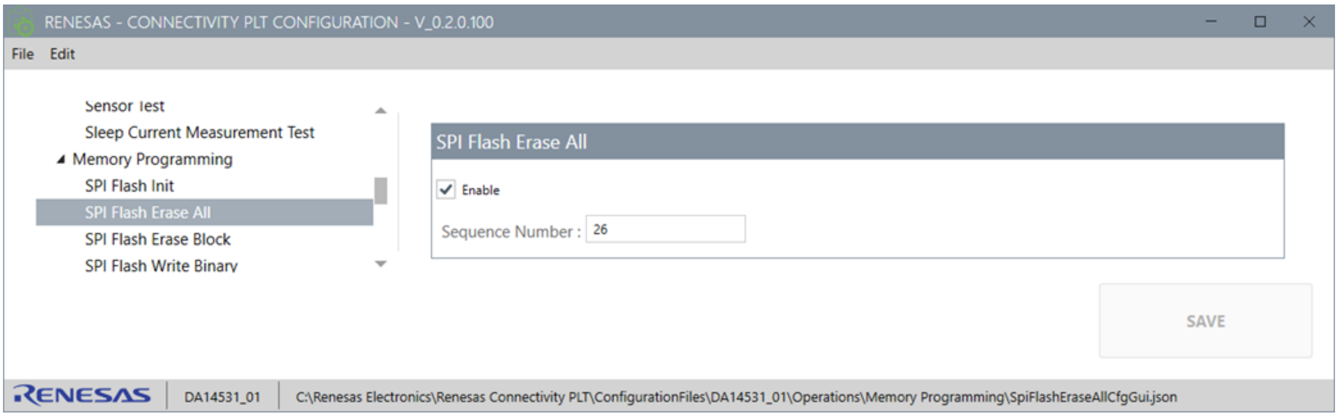
Figure 81. SPI Flash Init configuration

Table 37. SPI Flash Init configuration

Option	Description
Enable	This enables the SPI Flash Init operation.
Sequence Number	The order in which the test is run in execution
Spi Pins Enable	Enables the SPI pins

8.4.3 SPI Flash Erase All

SPI Flash Erase All is available in DA1453x.



SPI Flash Erase All

☑ Enable

Sequence Number : 26

DA14531_01 C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\Operations\Memory Programming\SpiFlashEraseAllCfgGui.json

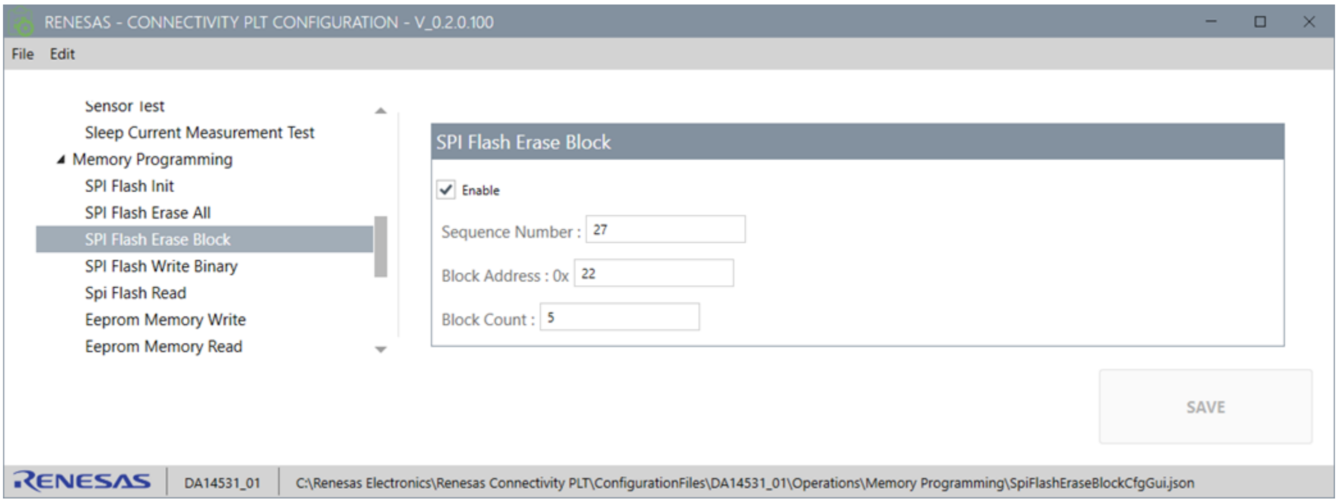
Figure 82. SPI Flash Erase All configuration

Table 38. SPI Flash Erase All configuration

Option	Description
Enable	This enables the SPI flash chip erase operation.
Sequence Number	The order in which the test is run in execution.

8.4.4 SPI Flash Erase Block

SPI Flash Erase Block is available in DA1453x.



☑ Enable

Sequence Number : 27

Block Address : 0x 22

Block Count : 5

DA14531_01 C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\Operations\Memory Programming\SpiFlashEraseBlockCfgGui.json

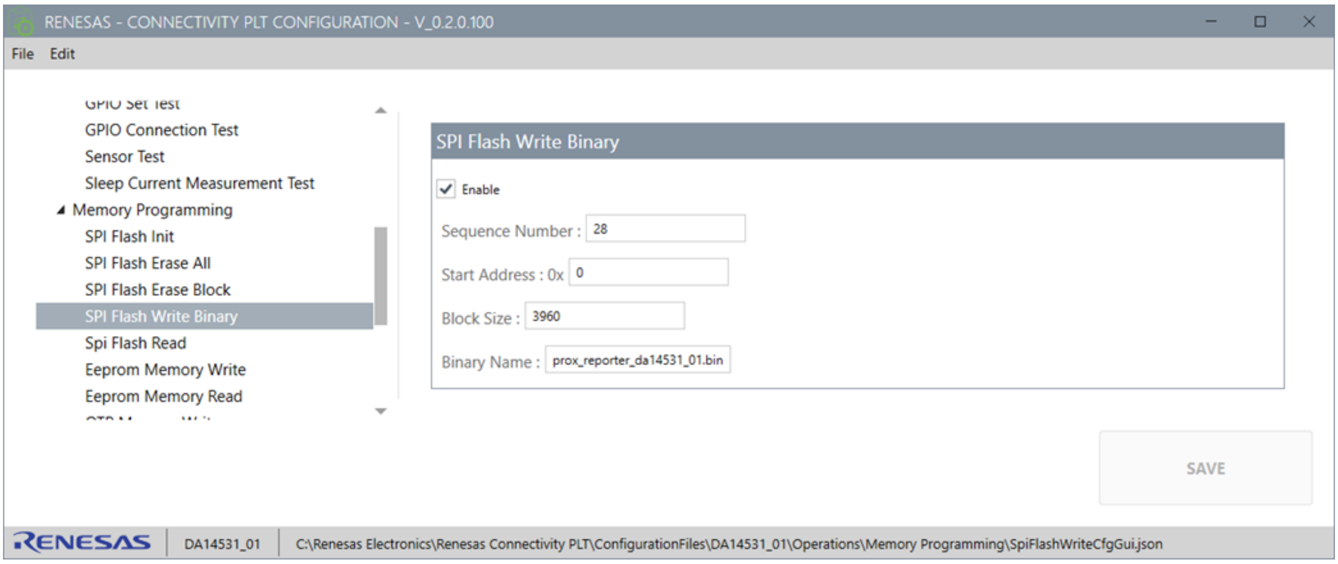
Figure 83. SPI Flash Erase Block configuration

Table 39. Flash erase block configuration

Option	Description
Enable	This enables the specific memory erase test.
Sequence Number	The order in which the test is run in execution.
Block Address	Configures the address of the first block.
Block Count	Number of memory blocks to erase

8.4.5 SPI Flash Write Binary

SPI Flash Write Binary is available in DA1453x.



SPI Flash Write Binary

☑ Enable

Sequence Number : 28

Start Address : 0x 0

Block Size : 3960

Binary Name : prox_reporter_da14531_01.bin

DA14531_01 C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\Operations\Memory Programming\SpiFlashWriteCfgGui.json

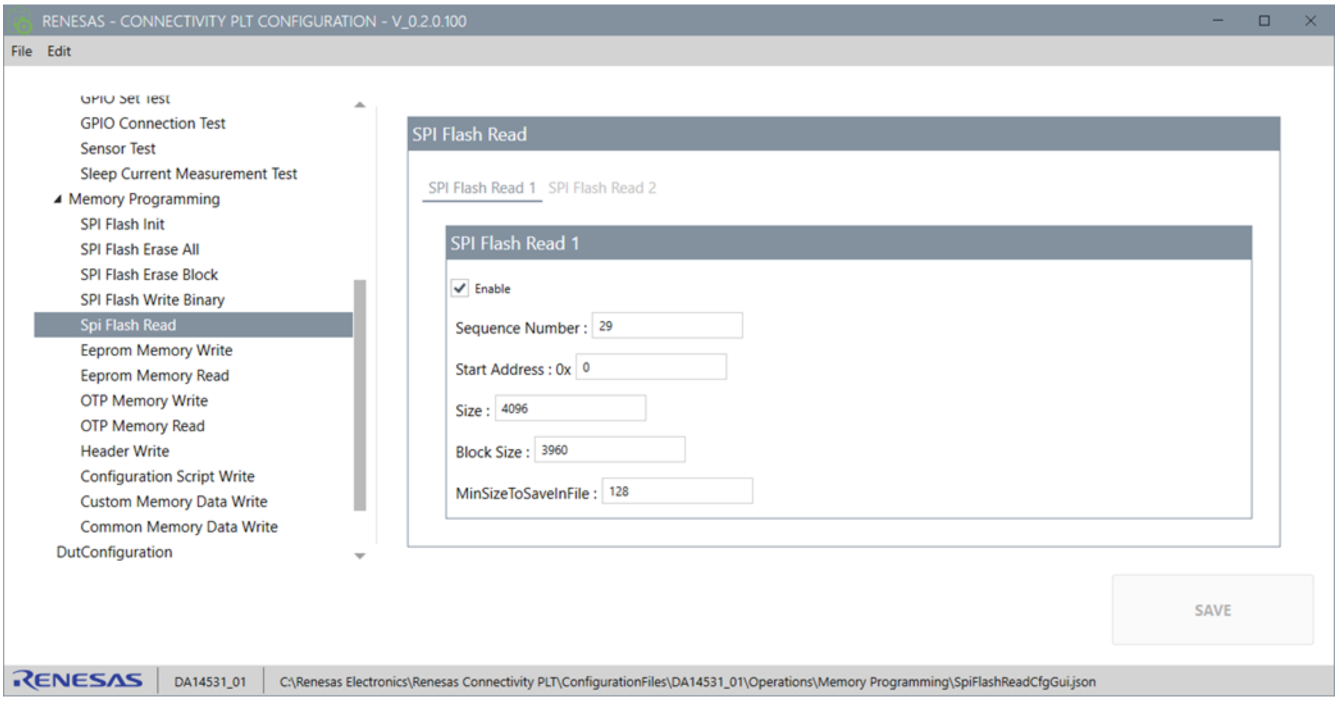
Figure 84. SPI Flash Write configuration

Table 40. Flash write configuration

Option	Description
Enable	This enables specific flash image programming operation.
Sequence Number	The order in which the test is run in execution
Start address	Configures the flash start address the image is written to.
Block Size	The chunk size for writing.
Binary Name	The filename of the binary to be written. Note: All binary files need to be stored in the Firmware folder under the installation folder and registered in the specific MCU JSON file.

8.4.6 Spi Flash Read

Spi Flash Read is available in DA1453x.



☑ Enable

Sequence Number : 29

Start Address : 0x 0

Size : 4096

Block Size : 3960

MinSizeToSaveInFile : 128

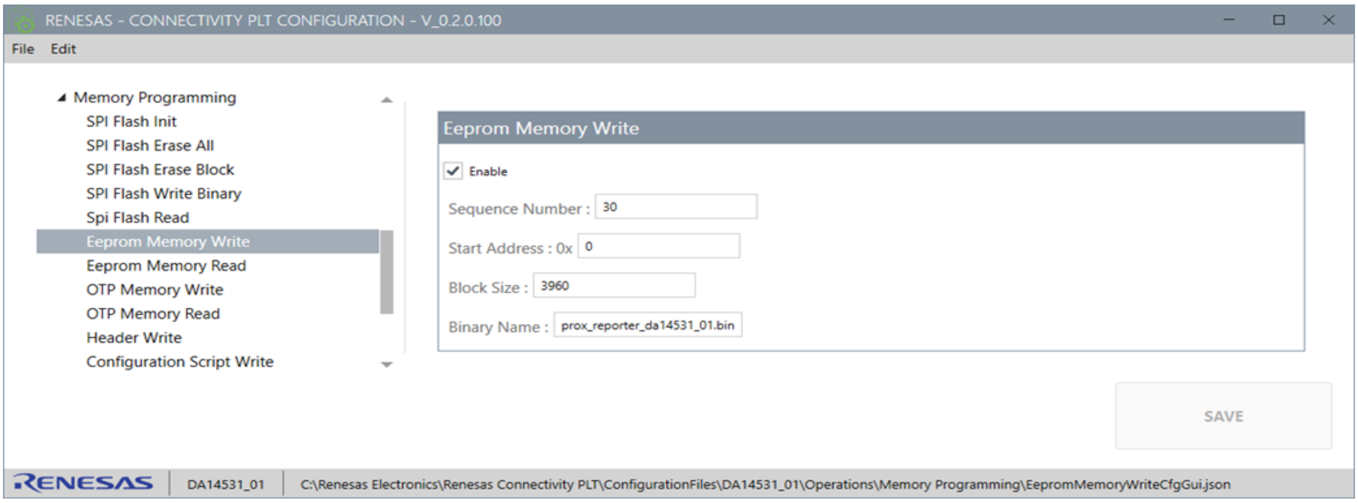
Figure 85. SPI Flash Read configuration

Table 41. SPI Flash Read configuration

Option	Description
Enable	This enables specific memory reading operation.
Sequence Number	The order in which the test is run in execution.
Start address	Configures the address the read operation begins from.
Size	Number of bytes to read, up to 64 MB. If data to be read are greater than
Block Size	The size of the chunk the data is split during reading.
MinSizeToSaveInFile	Minimum number of bytes required for the read operation to create a file. The file is stored under logs\folder mem_read_test in the Connectivity PLT installation folder. If no file is created the data is available in the logs files.

8.4.7 Eeprom Memory Write

Eeprom Memory Write is available in DA1453x,



Eeprom Memory Write

☑ Enable

Sequence Number : 30

Start Address : 0x 0

Block Size : 3960

Binary Name : prox_reporter_da14531_01.bin

DA14531_01 | C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\Operations\Memory Programming\EepromMemoryWriteCfgGui.json

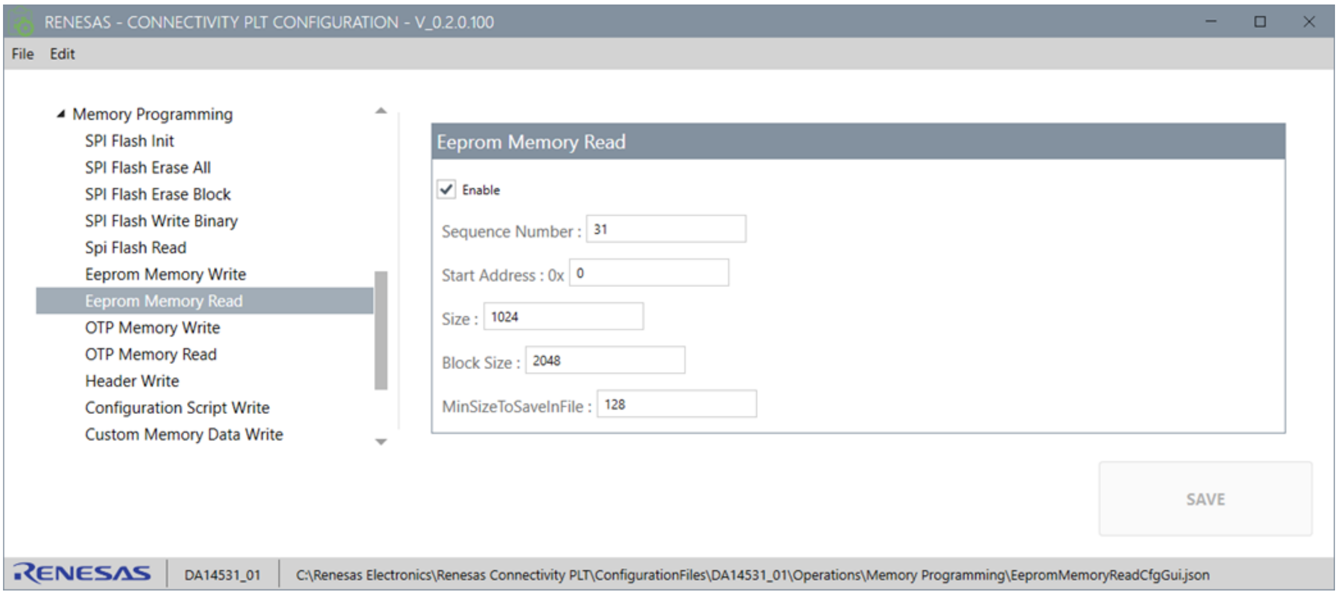
Figure 86. Eeprom Memory Write configuration

Table 42. Eeprom Memory Write configuration

Option	Description
Enable	This enables the specific memory reading operation.
Sequence Number	The order in which the test is run in execution.
Start address	Configures the start address.
Block Size	The size of the chunk the data is split during writing.
Binary Name	The filename of the binary file. Note: All binary files need to be stored in the Firmware folder under the installation folder and registered in the specific MCU JSON file.

8.4.8 Eeprom Memory Read

Eeprom Memory Read is available in DA1453x.



Eeprom Memory Read

☑ Enable

Sequence Number : 31

Start Address : 0x 0

Size : 1024

Block Size : 2048

MinSizeToSaveInFile : 128

DA14531_01 | C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\Operations\Memory Programming\EepromMemoryReadCfgGui.json

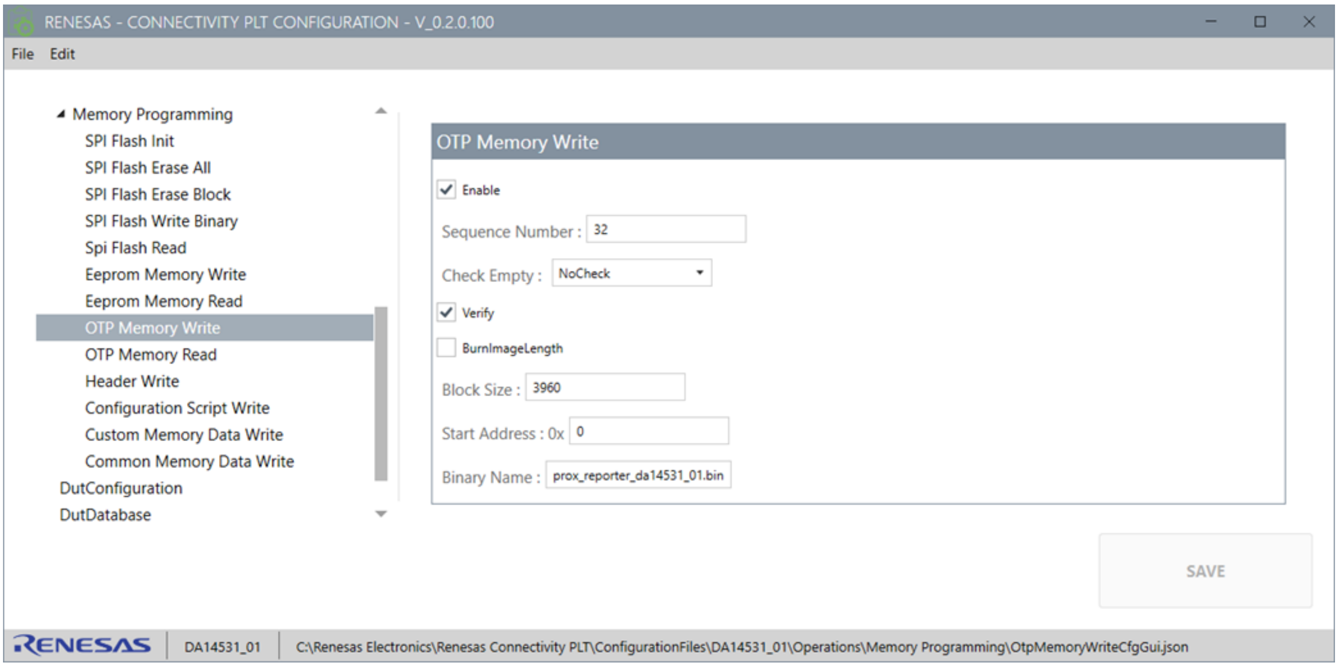
Figure 87. Eeprom Memory Read configuration

Table 43. Eeprom Memory Read configuration

Option	Description
Enable	This enables the specific memory reading operation.
Sequence Number	The order in which the test is run in execution.
Start address	Configures the start address.
Size	Number of bytes to read, up to 64 MB.
Block Size	The size of the chunk the data is split during reading.
MinSizeToSaveInFile	Minimum number of bytes required for the read operation to create a file. The file is stored under logs\folder mem_read_test in the Connectivity PLT installation folder. If no file is created the data is available in the logs files.

8.4.9 OTP Memory Write

OTP Memory Write is available in DA1453x, RA6W1, RA6W2, RRQ6100x, RRQ6105x.



☑ Enable

Sequence Number : 32

Check Empty : NoCheck

☑ Verify

□ BurnImageLength

Block Size : 3960

Start Address : 0x 0

Binary Name : prox_reporter_da14531_01.bin

DA14531_01 C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\Operations\Memory Programming\OtpMemoryWriteCfgGui.json

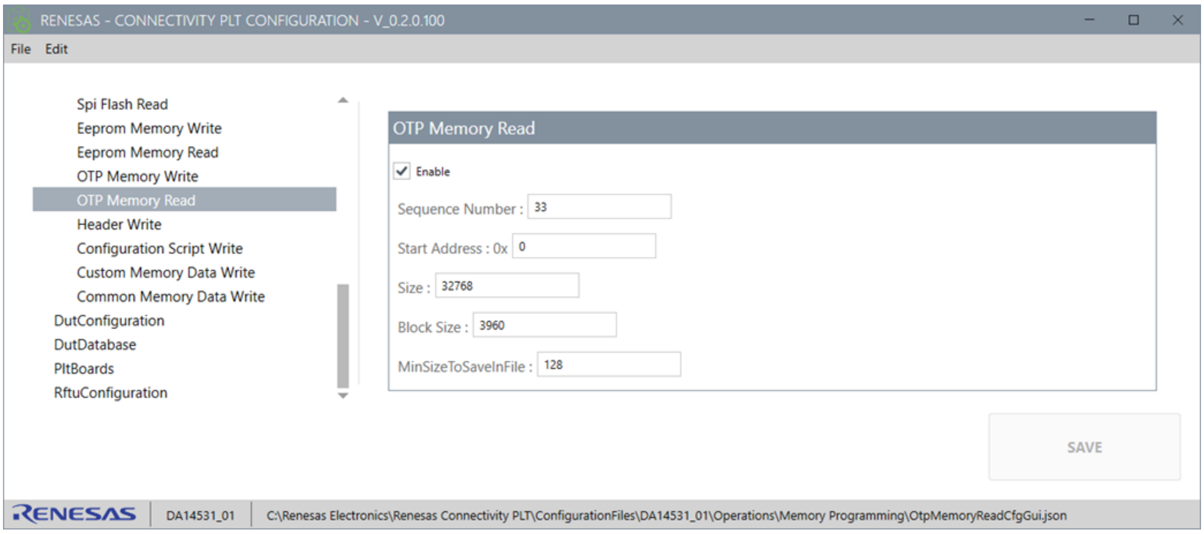
Figure 88. OTP Memory Write configuration

Table 44. OTP Memory Write configuration

Option	Description
Enable	This enables the specific memory reading operation.
Sequence Number	The order in which the test is run in execution
Check Empty	▪ NoCheck writes the data without reading first. ▪ ErrorIfNotEmpty fails the operation if the OTP area to be written is not empty. ▪ PassifNotEmpty skips the writing and report the operation as pass. ▪ PassifMatch fails the operation if the contents of the OTP differ from the binary file.
Verify	By selecting this option, the PLT software reads back the contents of the OTP memory and compares them to the original image file. If these do not match, the operation fails.
BurnImageLength	This option writes the size of the image written to the OTP Header.
Block Size	The size of the chunk the data is split during the operation.

8.4.10 OTP Memory Read

OTP Memory Read is available in DA1453x, RA6W1, RA6W2, RRQ6100x, RRQ6105x.



☑ Enable

Sequence Number : 33

Start Address : 0x 0

Size : 32768

Block Size : 3960

MinSizeToSaveInFile : 128

DA14531_01 C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\Operations\Memory Programming\OtpMemoryReadCfgGui.json

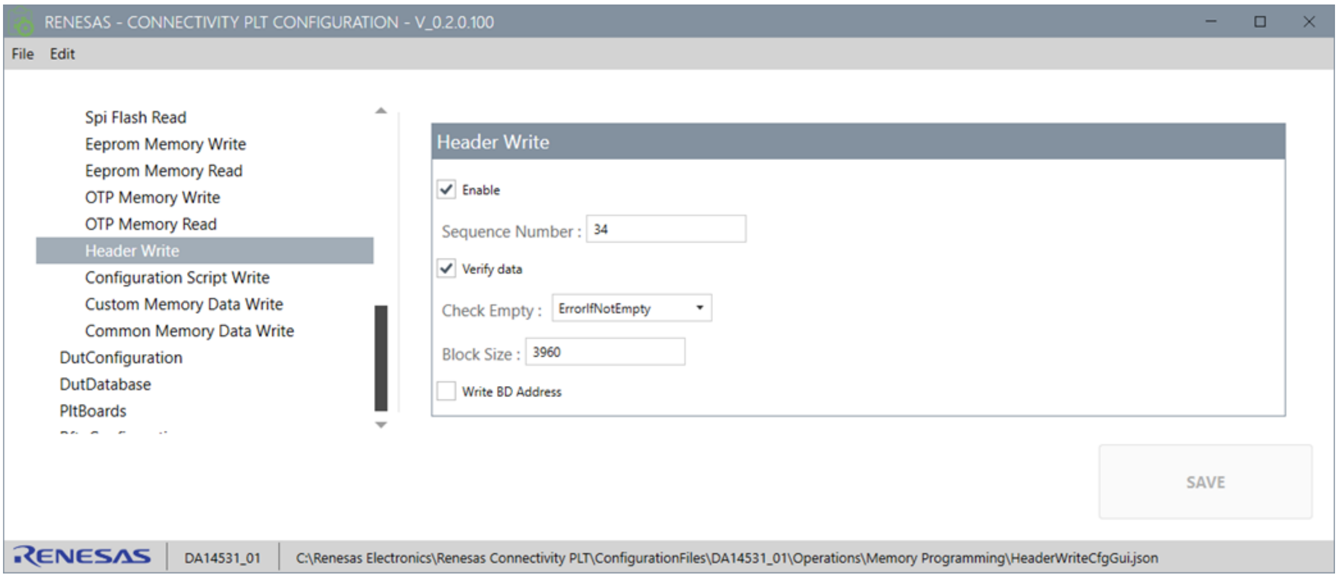
Figure 89. OTP Memory Read configuration

Table 45. OTP Memory Read configuration

Option	Description
Enable	This enables the specific memory reading operation.
Sequence Number	The order in which the test is run in execution.
Start address	Configures the start address.
Size	Number of bytes to read, up to 64 MB.
Block Size	The size of the chunk the data is split during the operation.
MinSizeToSaveInFile	Minimum number of bytes required for the read operation to create a file. The file is stored under logs\folder mem_read_test in the Connectivity PLT installation folder. If no file is created the data is available in the logs files.

8.4.11 Header Write

Header Write is available in DA1453x, RA6W1, RRQ6100x.



☑ Enable

Sequence Number : 34

☑ Verify data

Check Empty : ErrorIfNotEmpty

Block Size : 3960

☐ Write BD Address

DA14531_01 C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\Operations\Memory Programming\HeaderWriteCfgGui.json

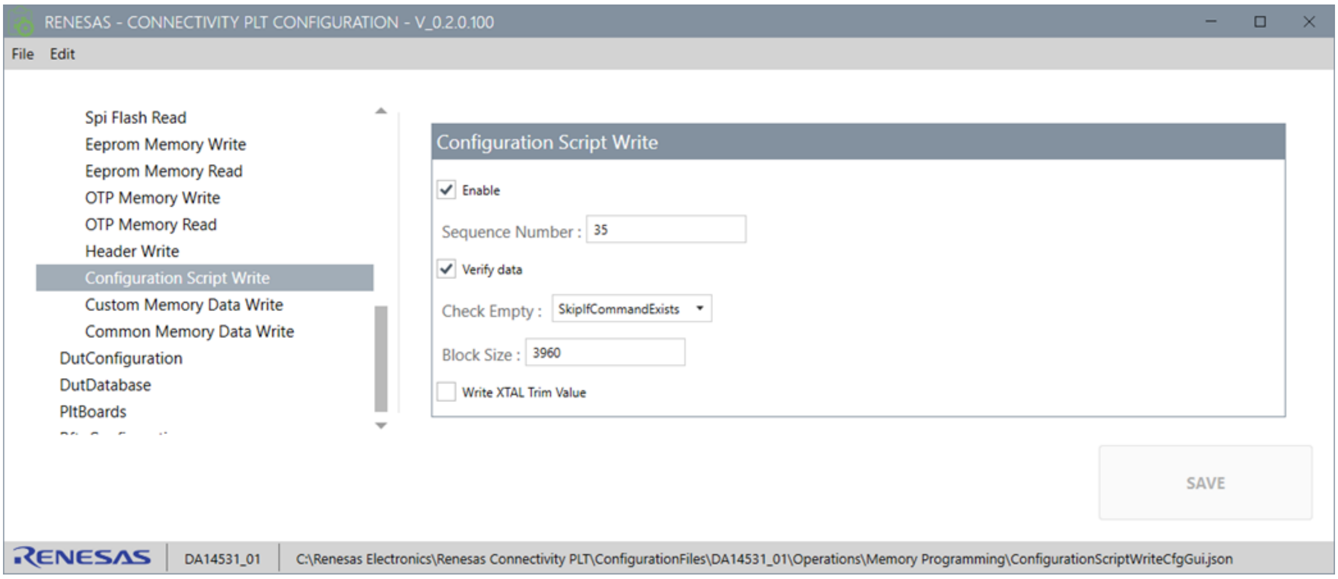
Figure 90. Header Write configuration

Table 46. Header Write configuration

Option	Description
Enable	This enables the header write operation.
Sequence Number	The order in which the test is run in execution.
Verify Data	By selecting this option, the PLT software reads back the contents of the flash memory and compares them to the original image file. If these do not match, the memory programming fails.
Check Empty	▪ NoCheck writes the data without reading first. ▪ ErrorIfNotEmpty fails the operation if the OTP area to be written is not empty. ▪ PassifNotEmpty skips the writing and report the operation as pass. ▪ PassifMatch fails the operation if the contents of the OTP differ from the one set to write.
Block Size	The size of the chunk the data is split during the operation.

8.4.12 Configuration Script Write

Configuration Script Write is available in DA1453x, RA6W1, RRQ6100x.



Configuration Script Write

☑ Enable

Sequence Number : 35

☑ Verify data

Check Empty : SkipIfCommandExists

Block Size : 3960

☐ Write XTAL Trim Value

DA14531_01 | C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\Operations\Memory Programming\ConfigurationScriptWriteCfgGui.json

Figure 91. Configuration Script Write

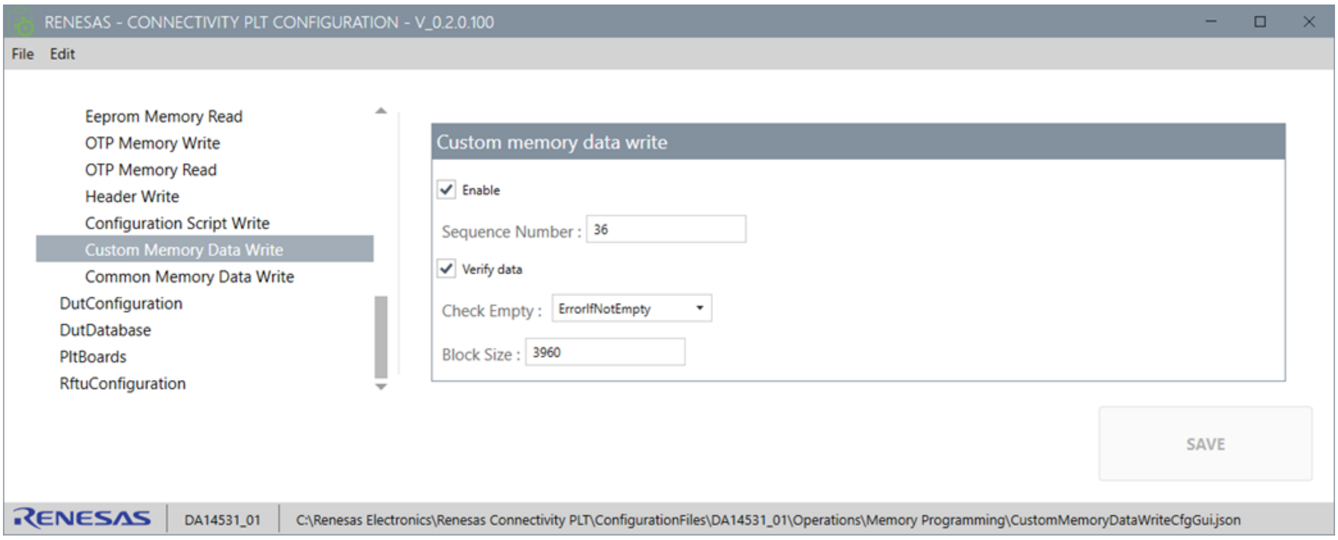
Table 47. Configuration Script Write

Option	Description
Enable	This enables the Configuration Script write operation.
Sequence Number	The order in which the test is run in execution.
Verify Data	By selecting this option, the PLT software reads back the contents of the flash memory and compares them to the original image file. If these do not match, the memory programming fails.
Check Empty	▪ No Check writes the data without reading first ▪ ErrorIfCommandExists fails the operation if the CS entry command already exists in the CS area. ▪ SkipIfCommandExists skips the command-value set if it already exists in the CS area. ▪ SkipIfTotalMatch fails the operation if the command-value set doesn’t match what is already stored in CS area.
Block Size	The size of the chunk the data is split during the operation.
Write XTAL Trim Value	Write the XTAL Trim Value (acquired from XTAL trim test).
Write KDCO Calibration Value	Write the KDCO calibration value (acquired from the KDCO calibration test).

Option	Description
Write RC32 Calibration Value	Write the RC32 calibration value (acquired from the RC32 calibration test).

8.4.13 Custom Memory Data Write

Custom Memory Data Write is available in DA1453x, RA6W1, RA6W2, RRQ6100x, RRQ6105x.



☑ Enable

Sequence Number : 36

☑ Verify data

Check Empty : ErrorIfNotEmpty

Block Size : 3960

C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\Operations\Memory Programming\CustomMemoryDataWriteCfgGui.json

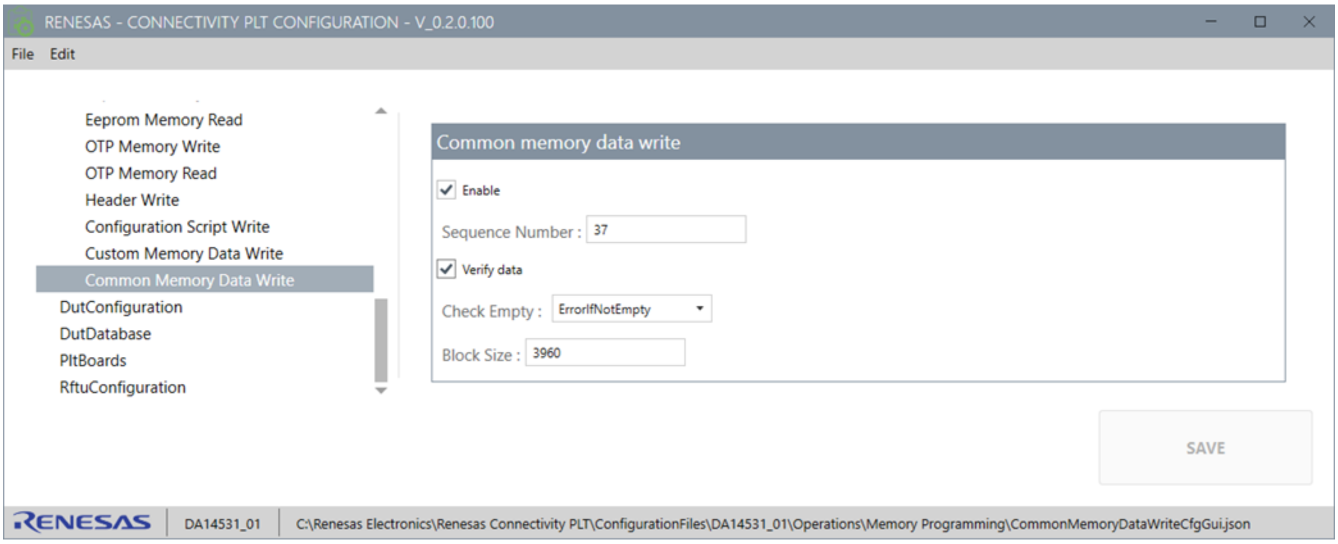
Figure 92. Custom Memory Write configuration

Table 48. Custom Memory Write configuration

Option	Description
Enable	This enables custom memory data write operation.
Sequence Number	The order in which the test is run in execution.
Verify Data	By selecting this option, the PLT software reads back the contents of the flash memory and compares them to the original image file. If these do not match, the memory programming fails.
OTP Check Empty	Not implemented for this operation – Set to No Check.
Block Size	The size of the chunk the data is split during the operation.

8.4.14 Common Memory Data Write

Common Memory Data Write is available in DA1453x, RA6W1, RA6W2, RRQ6100x, RRQ6105x.



☑ Enable

Sequence Number : 37

☑ Verify data

Check Empty : ErrorIfNotEmpty

Block Size : 3960

C:\Renesas Electronics\Renesas Connectivity PLT\ConfigurationFiles\DA14531_01\Operations\Memory Programming\CommonMemoryDataWriteCfgGui.json

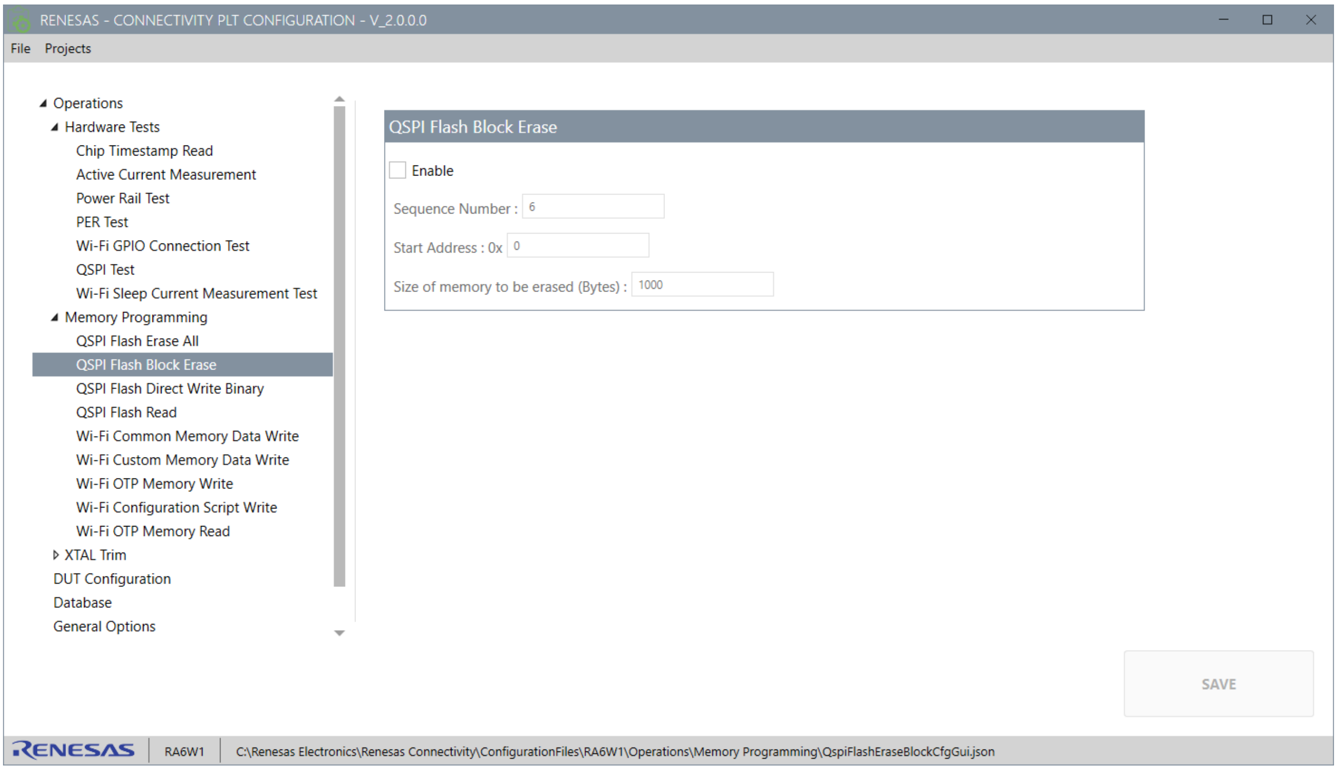
Figure 93. Common Memory Write configuration

Table 49. Common Memory Write configuration

Option	Description
Enable	This enables common memory data write operation.
Sequence Number	The order in which the test is run in execution.
Verify Data	By selecting this option, the PLT software reads back the contents of the flash memory and compares them to the original image file. If these do not match, the memory programming fails.
Check Empty	Not implemented for this operation – Set to No Check.
Block Size	The size of the chunk the data is split during the operation.

8.4.15 QSPI Flash Block Erase

QSPI Flash Block Erase is available in RA6W1, RA6W2, RRQ6100x, RRQ6105x.



QSPI Flash Block Erase

☐ Enable

Sequence Number : 6

Start Address : 0x 0

Size of memory to be erased (Bytes) : 1000

RA6W1 | C:\Renesas Electronics\Renesas Connectivity\ConfigurationFiles\RA6W1\Operations\Memory Programming\QspiFlashEraseBlockCfgGui.json

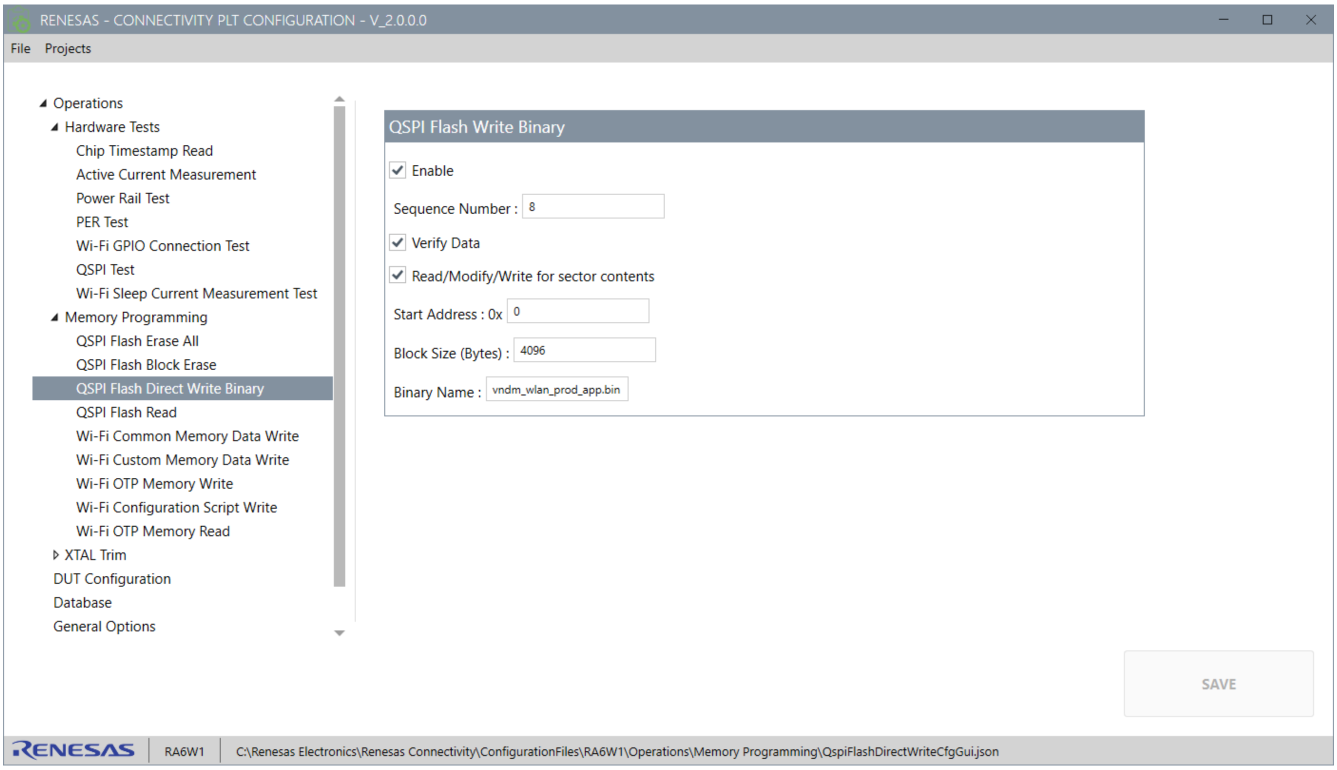
Figure 94. QSPI Flash Block Erase

Table 50. QSPI Flash Block Erase

Option	Description
Enable	This enables common memory data write operation.
Sequence Number	The order in which the test is run in execution.
Start Address	Start address in Hex.
Start of memory to be erased in bytes	

8.4.16 QSPI Flash Write Binary

QSPI Flash Write Binary is available in RA6W1, RA6W2, RRQ6100x, RRQ6105x.



QSPI Flash Write Binary

☑ Enable

Sequence Number : 8

☑ Verify Data

☑ Read/Modify/Write for sector contents

Start Address : 0x 0

Block Size (Bytes) : 4096

Binary Name : vndm_wlan_prod_app.bin

RA6W1 | C:\Renesas Electronics\Renesas Connectivity\ConfigurationFiles\RA6W1\Operations\Memory Programming\QspiFlashDirectWriteCfgGui.json

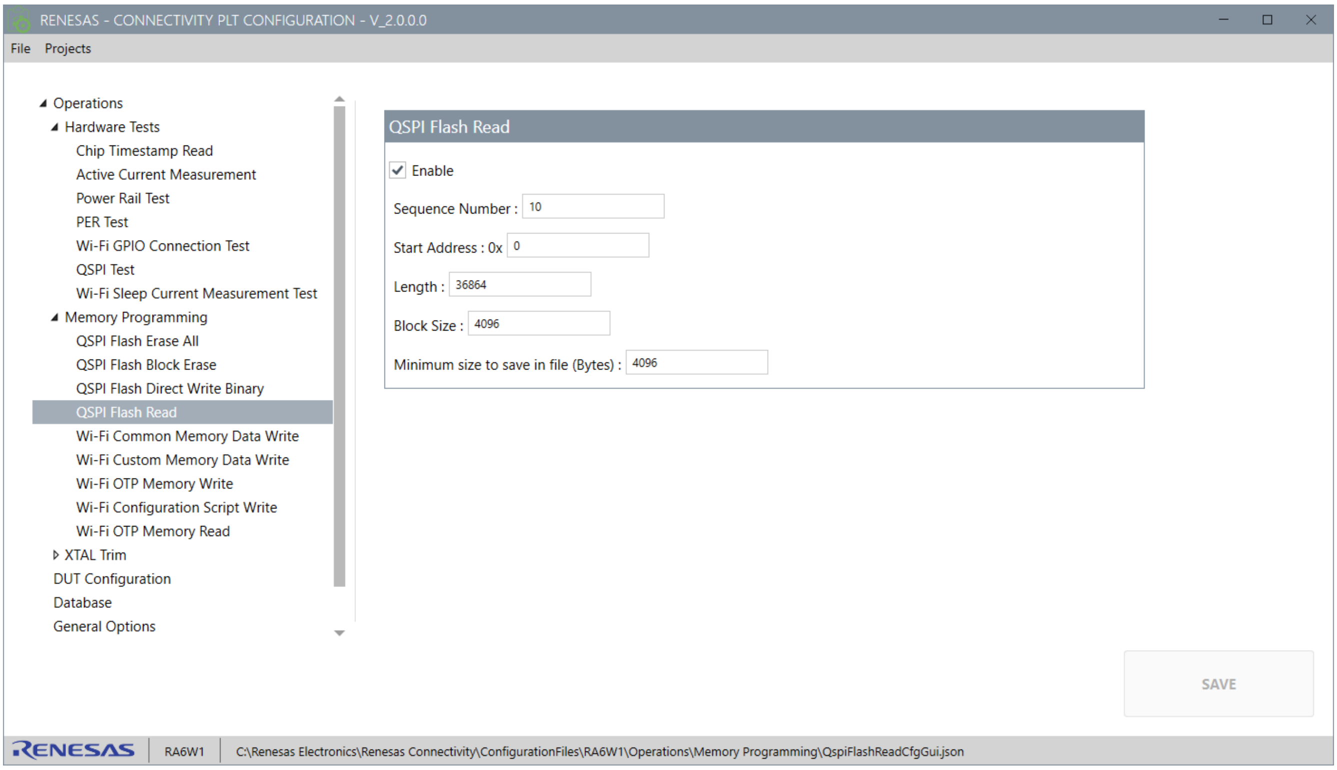
Figure 95. QSPI Write

Table 51. QSPI Flash Write

Option	Description
Enable	This enables common memory data write operation.
Sequence Number	The order in which the test is run in execution.
Data Verify	Verify or not written data.
Read Modify Write for Sector contents	Add Read/Write/Modify to sector contents.
Start Address	Start address in Hex.
Block Size	Block size in bytes.
Binary Name	Binary name.

8.4.17 QSPI Flash Read

QSPI Flash Read is available in RA6W1, RA6W2, RRQ6100x, RRQ6105x.



QSPI Flash Read

☑ Enable

Sequence Number : 10

Start Address : 0x 0

Length : 36864

Block Size : 4096

Minimum size to save in file (Bytes) : 4096

RA6W1 C:\Renesas Electronics\Renesas Connectivity\ConfigurationFiles\RA6W1\Operations\Memory Programming\QspiFlashReadCfgGui.json

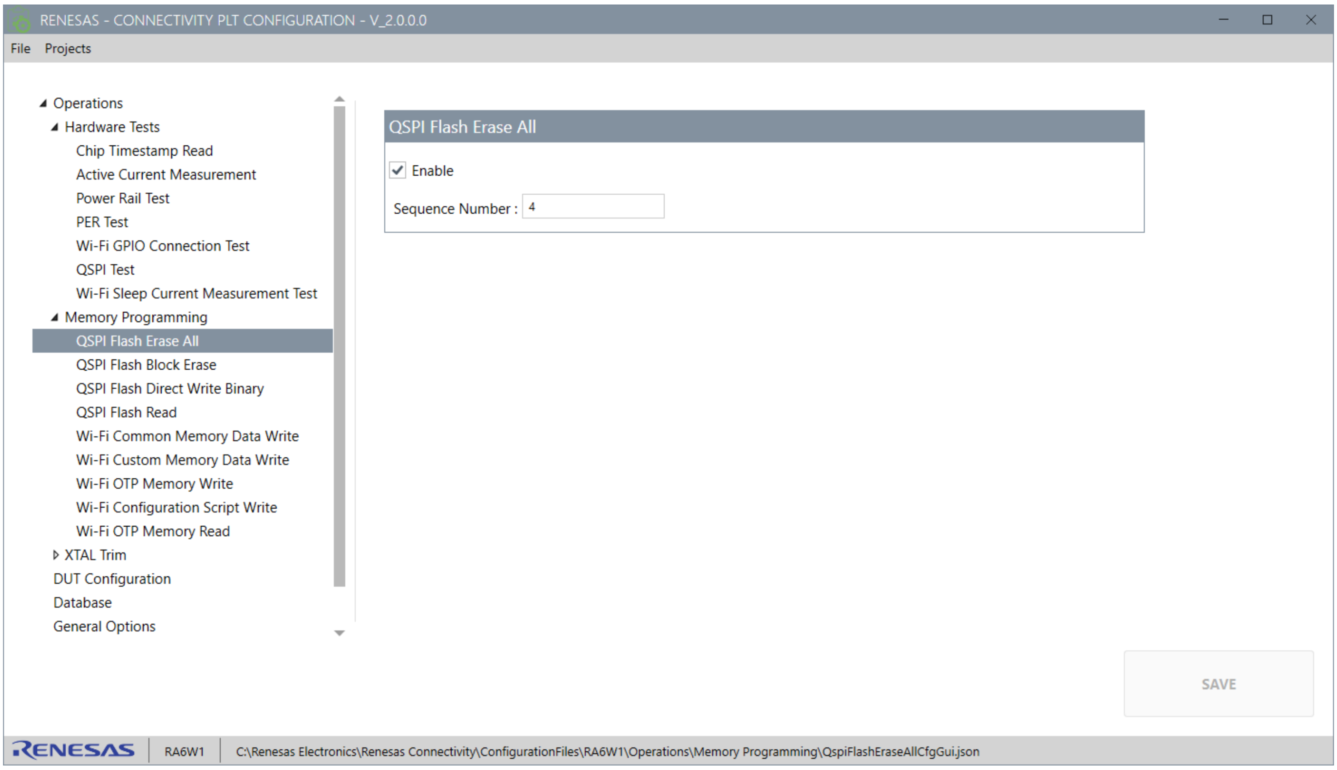
Figure 96. QSPI Flash Read

Table 52. QSPI Flash Read

Option	Description
Enable	This enables common memory data write operation.
Sequence Number	The order in which the test is run in execution.
Start Address	Start address in Hex.
Length	Length of read.
Block Size	Block size in bytes.
Minimum Size To Save In File	Minimum size in bytes.

8.4.18 QSPI Flash Erase All

QSPI Flash Erase All is available in RA6W1, RA6W2, RRQ6100x, RRQ6105x.



RENESAS - CONNECTIVITY PLT CONFIGURATION - V_2.0.0.0

QSPI Flash Erase All

☑ Enable

Sequence Number : 4

RA6W1 | C:\Renesas Electronics\Renesas Connectivity\ConfigurationFiles\RA6W1\Operations\Memory Programming\QspiFlashEraseAllCfgGui.json

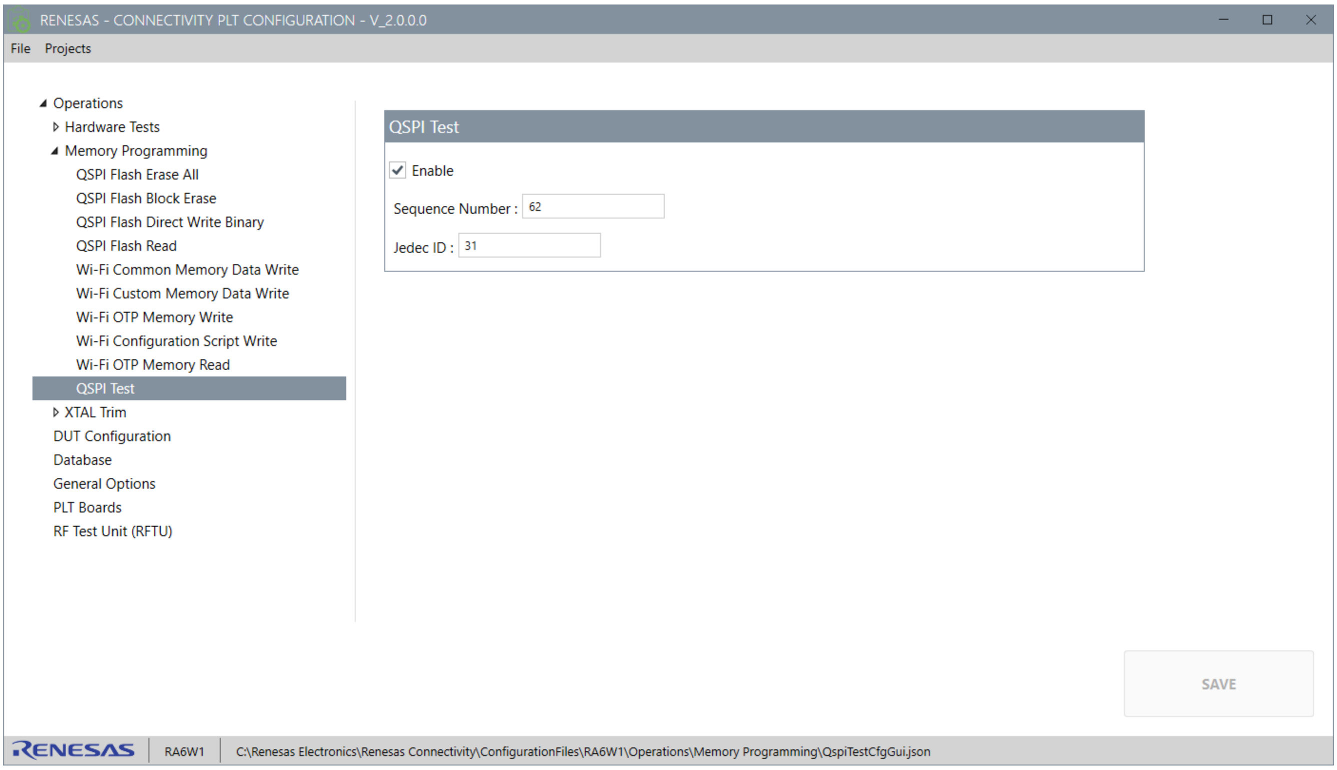
Figure 97. QSPI Flash Erase All

Table 53. QSPI Erase All

Option	Description
Enable	This enables common memory data write operation.
Sequence Number	The order in which the test is run in execution.

8.4.19 QSPI Test

QSPI Test is available in RA6W1, RA6W2, RRQ6100x, RRQ6105x.



QSPI Test

☑ Enable

Sequence Number : 62

Jedec ID : 31

RA6W1 | C:\Renesas Electronics\Renesas Connectivity\ConfigurationFiles\RA6W1\Operations\Memory Programming\QspiTestCfgGui.json

Figure 98. QSPI Test

Table 54. QSPI Test

Option	Description
Enable	This enables common memory data write operation.
Sequence Number	The order in which the test is run in execution.
Jedec ID	Jedec ID.

8.4.20 Wi-Fi Configuration Script Write

Wi-Fi Configuration Script Write is available in RA6W1, RA6W2, RRQ6100x, RRQ6105x.

Figure 99. Wi-Fi Configuration Script

Table 55. Wi-Fi Configuration Script Write

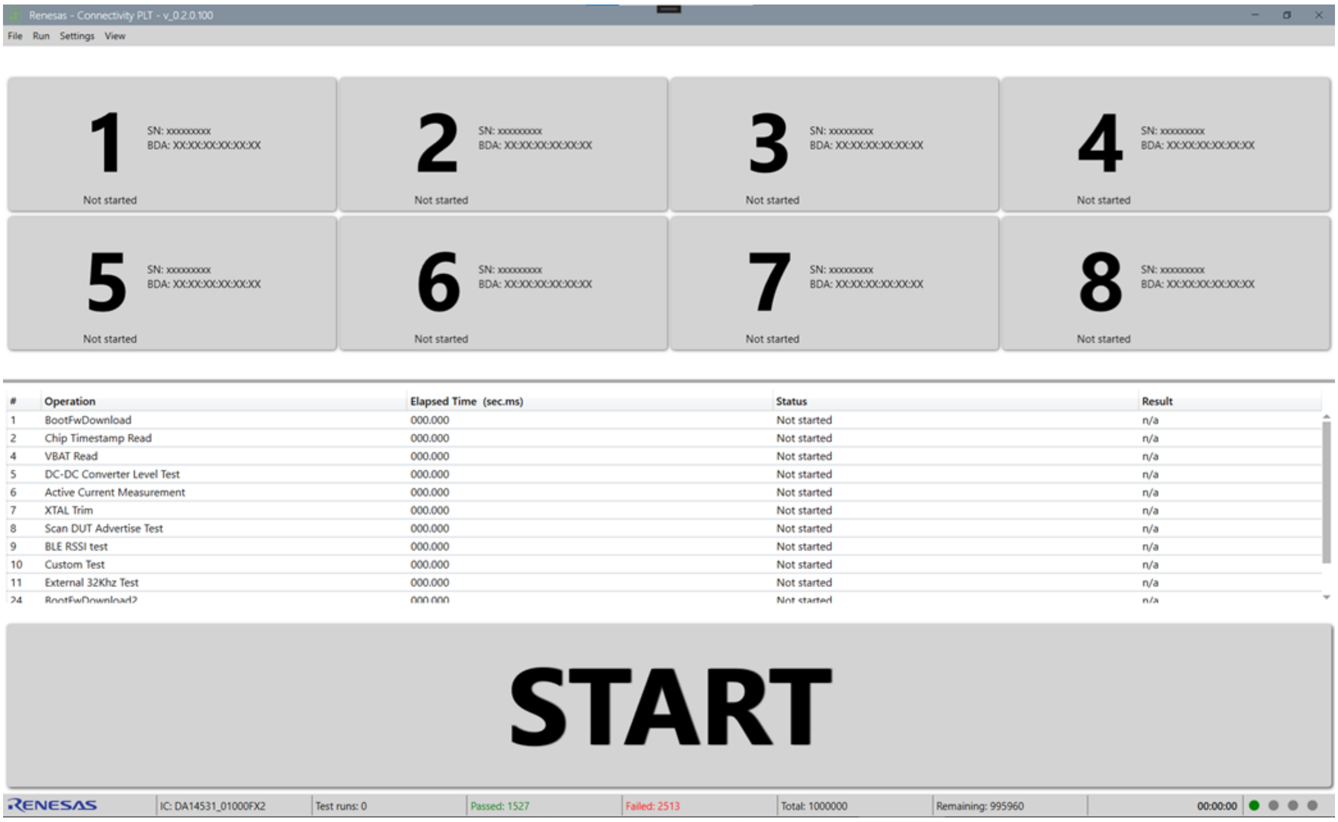
Option	Description
Enable	This enables common memory data write operation.
Verify Dara	Verify Written data.
Check Empty	Jedec ID.
Block Size	Block size in bytes.

9. Connectivity PLT Application

The Renesas Connectivity PLT application serves as the primary graphical user interface for executing tests and programming tasks. It provides operators with a console to initiate and monitor the testing process. The application connects remotely to the Connectivity PLT Core service and functions as the front end of the PLT system. It can be launched either from the Windows Start menu or by directly running the executable file located in the installation directory. (`Renesas_Connectivity_PLT.exe`).

9.1 Connectivity PLT Application Main Execution Window

The main application window consists of tiles, each representing a DUT and its status, as well as a list of operations and their status, a start/finish button, and several other information fields. Figure 100 shows an example of a setup of a single Connectivity PLT board with 8 DUTs.



1 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started

2 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started

3 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started

4 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started

5 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started

6 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started

7 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started

8 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started

#	Operation	Elapsed Time (sec.ms)	Status	Result
1	BootFwDownload	000.000	Not started	n/a
2	Chip Timestamp Read	000.000	Not started	n/a
4	VBAT Read	000.000	Not started	n/a
5	DC-DC Converter Level Test	000.000	Not started	n/a
6	Active Current Measurement	000.000	Not started	n/a
7	XTAL Trim	000.000	Not started	n/a
8	Scan DUT Advertise Test	000.000	Not started	n/a
9	BLE RSSI test	000.000	Not started	n/a
10	Custom Test	000.000	Not started	n/a
11	External 32Khz Test	000.000	Not started	n/a
24	BootFwDownload2	000.000	Not started	n/a

IC: DA14531_01000FX2 | Test runs: 0 | Passed: 1527 | Failed: 2513 | Total: 1000000 | Remaining: 995960 | 00:00:00 ● ● ● ●

Figure 100. Test execution start window

You can configure the testing using the menu items at the top of window. Brief testing results are displayed at the bottom of the window, including the four LEDs for RFTU status (grey for not enabled, green for enabled and detected, and red for enabled but not detected).

Information tiles with numbers represent DUTs in your setup (Figure 101) and can accommodate from one to four Connectivity PLT boards consisting of one to thirty-two DUT tiles (one to eight DUTS per Connectivity PLT board). The layout is configured using X/Y axis in PLT boards Configuration, see Section 8.2.3.

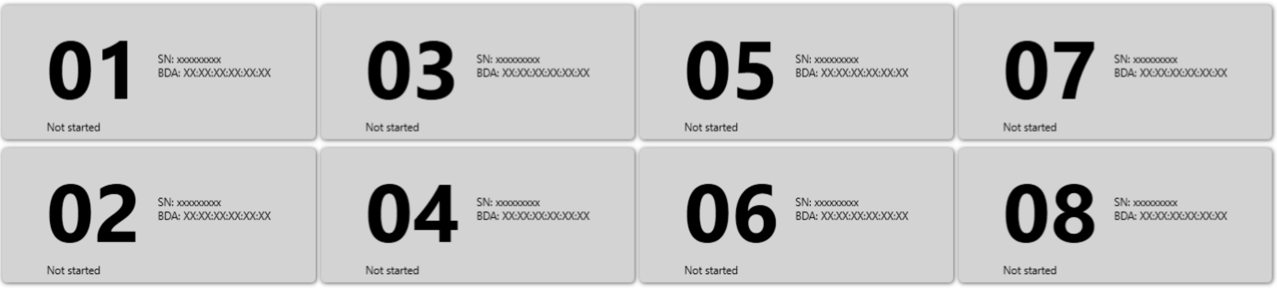


Figure 101. DUTs grid

Each DUT tile contains the following:

- a – Display name (for example, 01) as configured in Connectivity PLT boards settings.
- b – Acquired Serial Number either automatically or from the initial dialog. (only while tests are running)
- c – Acquired board address as fetched automatically form the devices database (either based on entered serial number or automatic base on next available) (only while tests are running)
- d – Current operation executing (only while tests are running), see Figure 102. If any of the DUTs fails, the current command field indicates the failed test command.

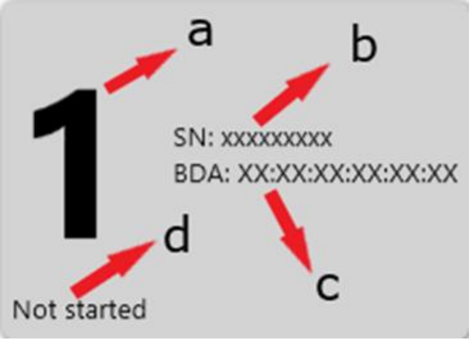
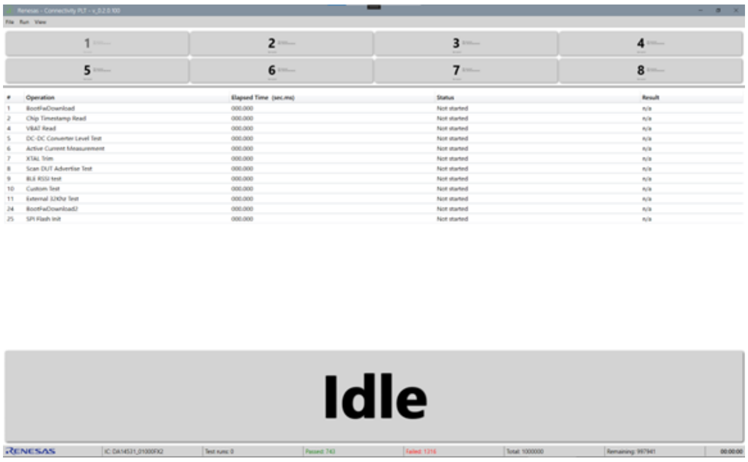


Figure 102. Single DUT tile

A splitter control allows the display area to be maximized for showing more of the operations table or more tile space depending on the user needs.



#	Operation	Elapsed Time (sec.ms)	Status	Result
1	BootFwDownload	000.000	Not started	n/a
2	Chip Timestamp Read	000.000	Not started	n/a
4	VBAT Read	000.000	Not started	n/a
5	DC-DC Converter Level Test	000.000	Not started	n/a
6	Active Current Measurement	000.000	Not started	n/a
7	XTAL Trim	000.000	Not started	n/a
8	Scan DUT Advertise Test	000.000	Not started	n/a
9	BLE RSSI test	000.000	Not started	n/a
10	Custom Test	000.000	Not started	n/a
11	External 32Khz Test	000.000	Not started	n/a
24	BootFwDownload2	000.000	Not started	n/a
25	SPI Flash Init	000.000	Not started	n/a

IC: DA14531_01000FX2 | Test runs: 0 | Passed: 743 | Failed: 1316 | Total: 1000000 | Remaining: 997941 | 00:00:00

Figure 103. Grid splitter top position

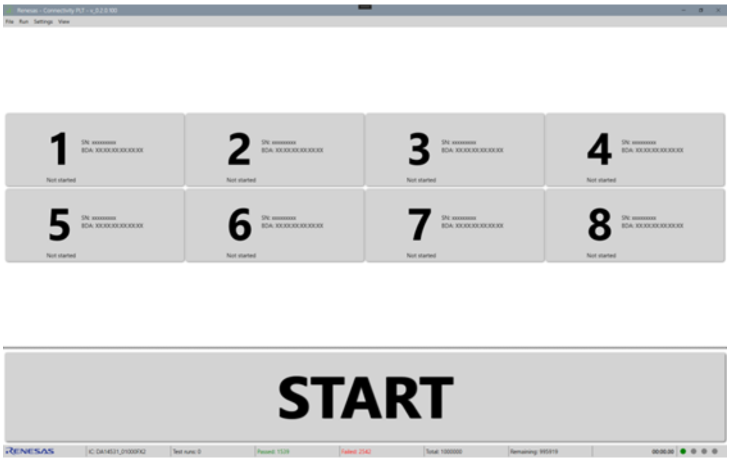
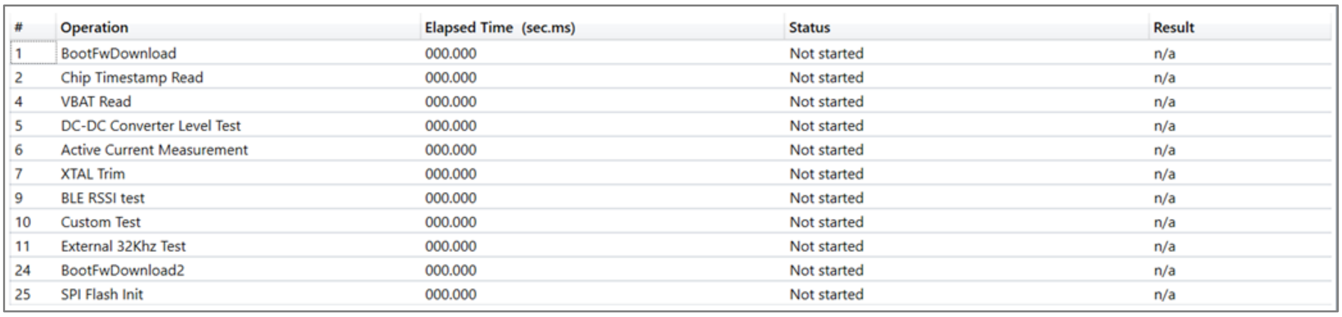


Figure 104. Grid splitter bottom position

The operations grid is the table that shows the operations that are enabled to run. This table provides data about execution time, status, and results (Figure 105).



#	Operation	Elapsed Time (sec.ms)	Status	Result
1	BootFwDownload	000.000	Not started	n/a
2	Chip Timestamp Read	000.000	Not started	n/a
4	VBAT Read	000.000	Not started	n/a
5	DC-DC Converter Level Test	000.000	Not started	n/a
6	Active Current Measurement	000.000	Not started	n/a
7	XTAL Trim	000.000	Not started	n/a
9	BLE RSSI test	000.000	Not started	n/a
10	Custom Test	000.000	Not started	n/a
11	External 32Khz Test	000.000	Not started	n/a
24	BootFwDownload2	000.000	Not started	n/a
25	SPI Flash Init	000.000	Not started	n/a

Figure 105. Operations grid

Start button has four states:

- **Idle** – grey and enabled; right click the button or press space bar to start testing.
- **Enter Device Serial Number** – at this state a dialog is displayed requesting to enter the serial number
- **Running** – blue and disabled; testing is in process.
- **Finish** – green if testing is successful or red if testing failed.

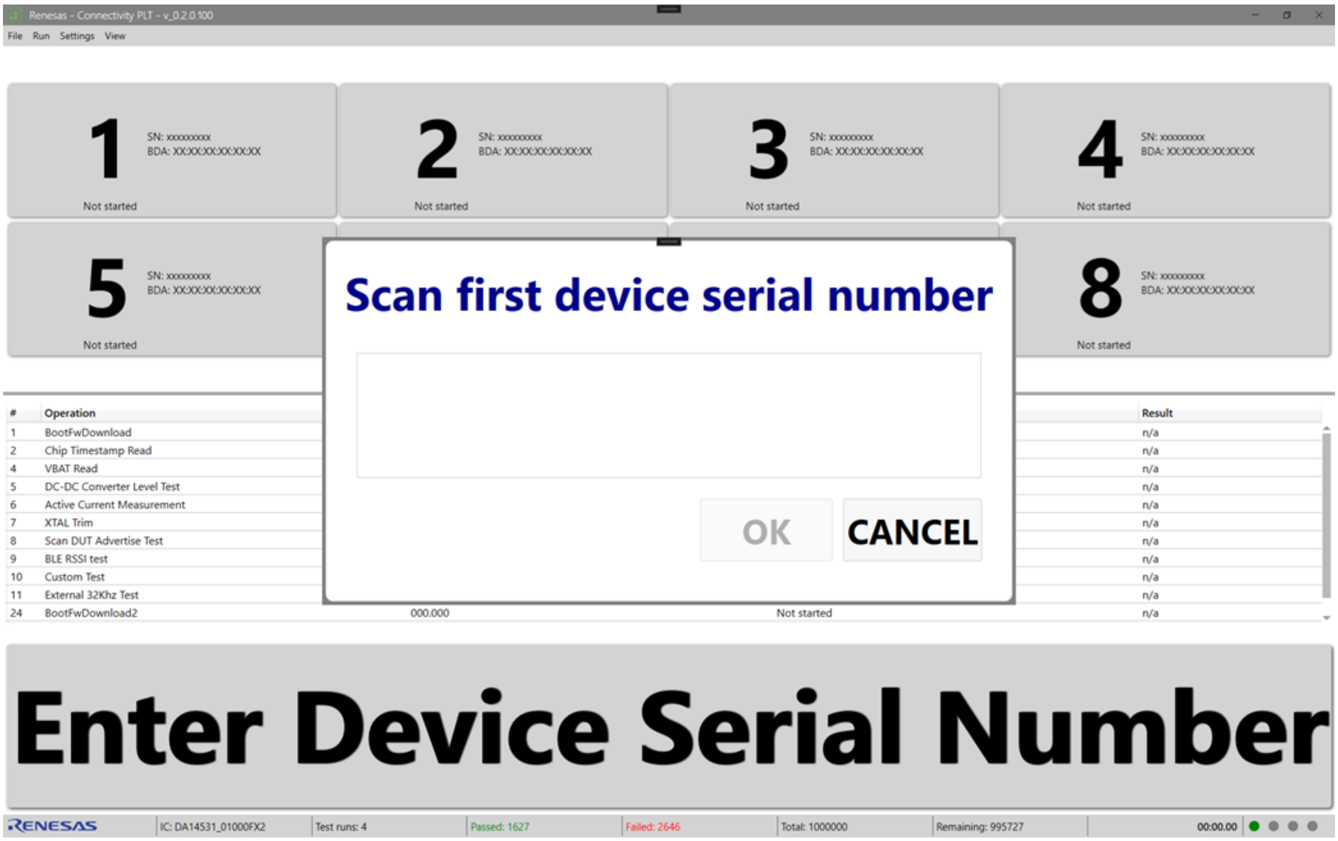
You can also use keyboard shortcuts: to start testing, select S or the Spacebar; and to finish testing, select F.

9.2 Test Execution

The test execution process has the following stages:

1. **Serial numbers assignment (optional)**

   If the Device Specific Serial Number option was enabled a dialog to enter the first serial number is displayed when the test process is initiated, see Figure 106.



1 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started

2 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started

3 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started

4 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started

5 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started

8 SN: xxxxxxxxx BDA: XX:XX:XX:XX:XX:XX Not started

Scan first device serial number

#	Operation			Result
1	BootFwDownload			n/a
2	Chip Timestamp Read			n/a
4	VBAT Read			n/a
5	DC-DC Converter Level Test			n/a
6	Active Current Measurement			n/a
7	XTAL Trim			n/a
8	Scan DUT Advertise Test			n/a
9	BLE RSSI test			n/a
10	Custom Test			n/a
11	External 32Khz Test			n/a
24	BootFwDownload2	000.000	Not started	n/a

Enter Device Serial Number

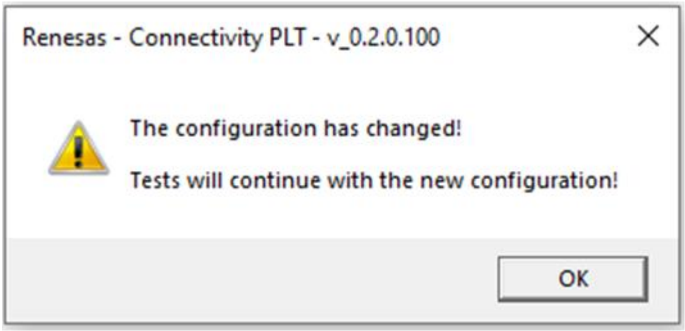
IC: DA14531_01000FX2 | Test runs: 4 | Passed: 1627 | Failed: 2646 | Total: 1000000 | Remaining: 995727

Figure 106. Enter serial number screen

   After the serial number is entered, all DUTs are assigned with a sequential serial number retrieved from the database along with the corresponding Bluetooth address.

2. **Configuration**

   Connectivity PLT fetches the latest configuration available in the current project. If changes are made to the configuration, reload is required to apply these changes (go to **File** >**Reload Configuration** or press F5). Even if manual reload is not executed the configuration is going to be reloaded at the beginning of the test process and a warning message appears, see Figure 107.



Renesas - Connectivity PLT - v_0.2.0.100

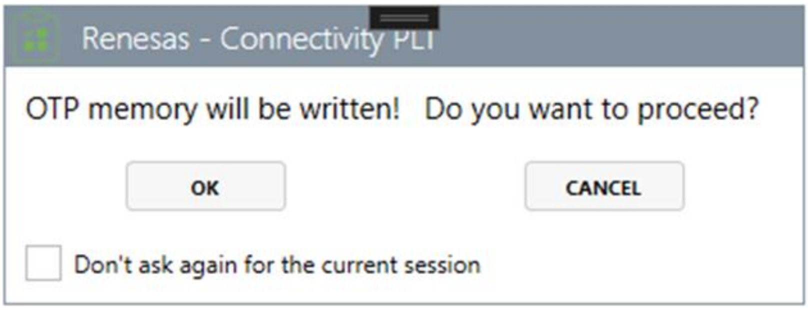
The configuration has changed!

Tests will continue with the new configuration!

Figure 107. Configuration reload warning

3. **OTP Write Warning**

If any operation includes writing to the OTP memory, a warning is displayed at the start of the test process to avoid accidental writes since the OTP cannot be re-written. The warning can be suppressed for future runs from the same dialog by checking the Don’t ask again for the current session checkbox.



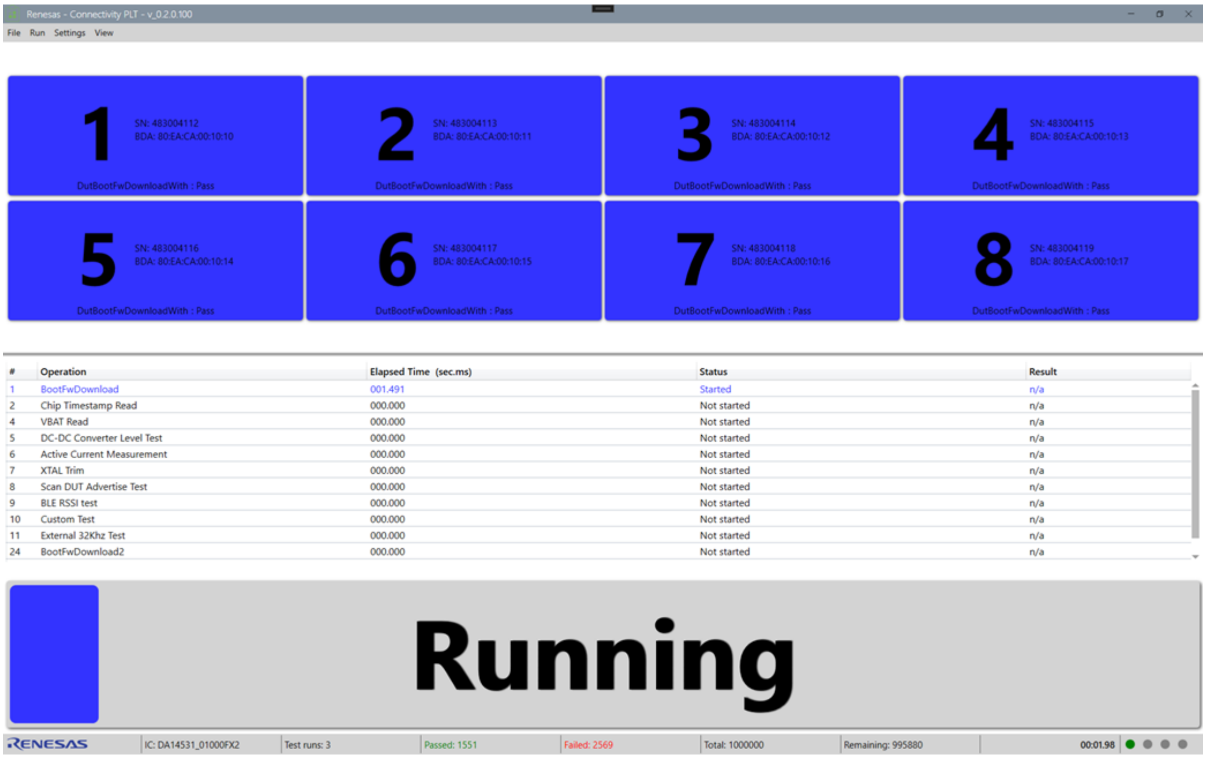
OTP memory will be written! Do you want to proceed?

□ Don't ask again for the current session

Figure 108. OTP write warning message

4. **Tests Execution**

When the test process starts, the background color of DUT tiles changes to blue to indicate the in progress status. The active operation row text color changes to blue also to indicate in progress while also the dedicated test timer starts. The start button is disabled but serves as a progress bar colored blue while executing and green or red depending on the result, see Figure 109.



1 SN: 483004112 BDA: 80:EA:CA:00:10:10 DutBootFwDownloadWith : Pass

2 SN: 483004113 BDA: 80:EA:CA:00:10:11 DutBootFwDownloadWith : Pass

3 SN: 483004114 BDA: 80:EA:CA:00:10:12 DutBootFwDownloadWith : Pass

4 SN: 483004115 BDA: 80:EA:CA:00:10:13 DutBootFwDownloadWith : Pass

5 SN: 483004116 BDA: 80:EA:CA:00:10:14 DutBootFwDownloadWith : Pass

6 SN: 483004117 BDA: 80:EA:CA:00:10:15 DutBootFwDownloadWith : Pass

7 SN: 483004118 BDA: 80:EA:CA:00:10:16 DutBootFwDownloadWith : Pass

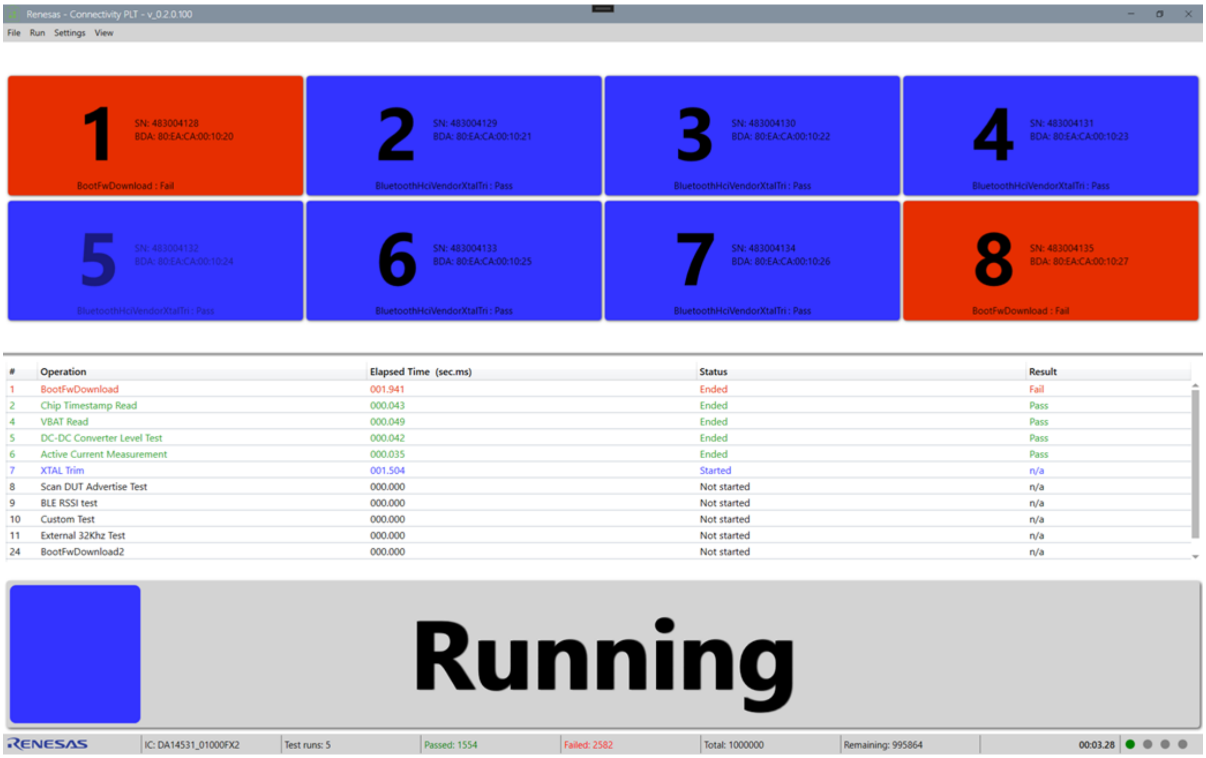
8 SN: 483004119 BDA: 80:EA:CA:00:10:17 DutBootFwDownloadWith : Pass

#	Operation	Elapsed Time (sec.ms)	Status	Result
1	BootFwDownload	001.491	Started	n/a
2	Chip Timestamp Read	000.000	Not started	n/a
4	VBAT Read	000.000	Not started	n/a
5	DC-DC Converter Level Test	000.000	Not started	n/a
6	Active Current Measurement	000.000	Not started	n/a
7	XTAL Trim	000.000	Not started	n/a
8	Scan DUT Advertise Test	000.000	Not started	n/a
9	BLE RSSI test	000.000	Not started	n/a
10	Custom Test	000.000	Not started	n/a
11	External 32Khz Test	000.000	Not started	n/a
24	BootFwDownload2	000.000	Not started	n/a

IC: DA14531_01000FX2 | Test runs: 3 | Passed: 1551 | Failed: 2569 | Total: 1000000 | Remaining: 995880 | 00:01.98

Figure 109. Test execution

If any DUT fails on any operation, the tile background becomes red, the failed command is displayed at the bottom of the tile, and the operation row text color changes to red to indicate that at least one DUT failed this test.



1
SN: 483004128
BDA: 80:EA:CA:00:10:20
BootFwDownload : Fail

2
SN: 483004129
BDA: 80:EA:CA:00:10:21
BluetoothHciVendorXtalTri : Pass

3
SN: 483004130
BDA: 80:EA:CA:00:10:22
BluetoothHciVendorXtalTri : Pass

4
SN: 483004131
BDA: 80:EA:CA:00:10:23
BluetoothHciVendorXtalTri : Pass

5
SN: 483004132
BDA: 80:EA:CA:00:10:24
BluetoothHciVendorXtalTri : Pass

6
SN: 483004133
BDA: 80:EA:CA:00:10:25
BluetoothHciVendorXtalTri : Pass

7
SN: 483004134
BDA: 80:EA:CA:00:10:26
BluetoothHciVendorXtalTri : Pass

8
SN: 483004135
BDA: 80:EA:CA:00:10:27
BootFwDownload : Fail

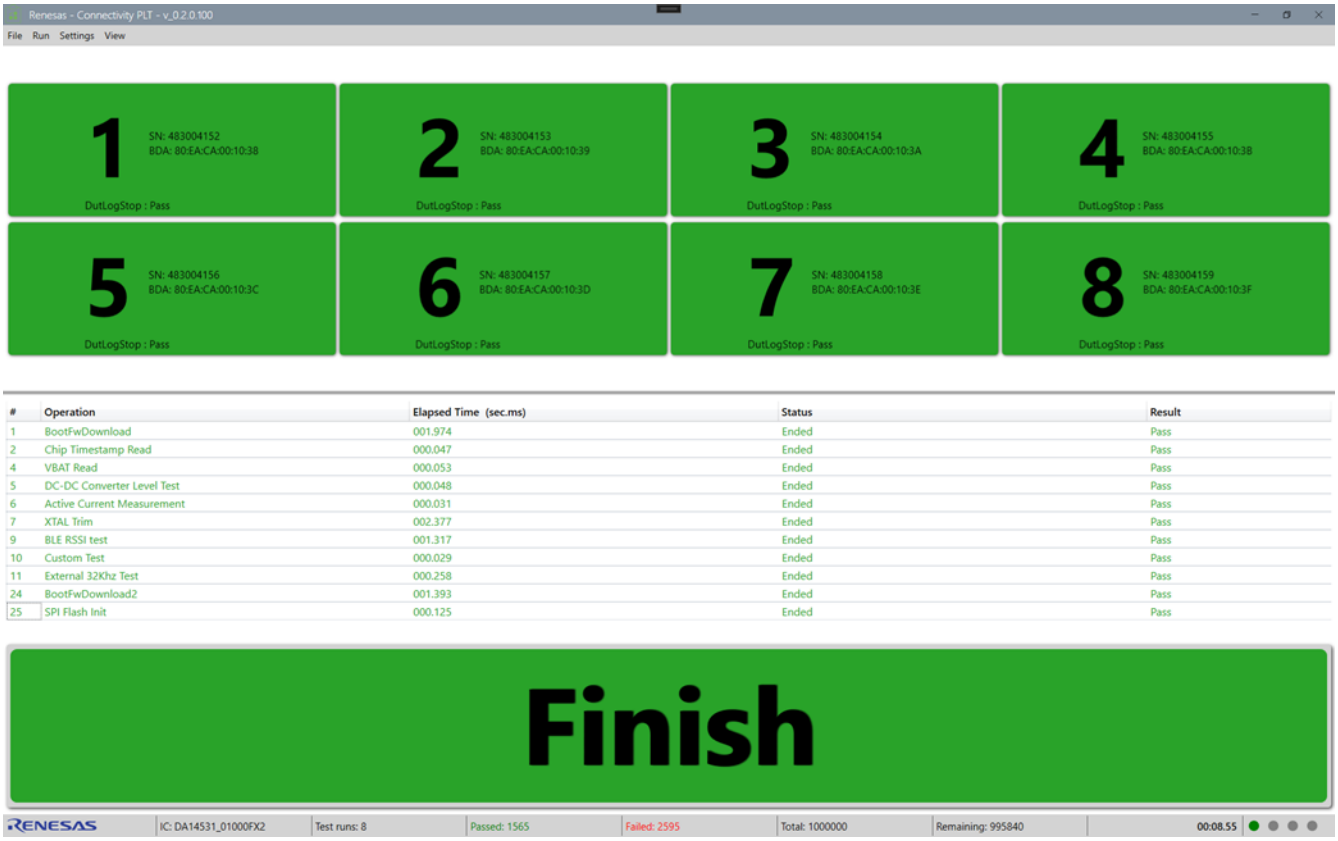
#	Operation	Elapsed Time (sec.ms)	Status	Result
1	BootFwDownload	001.941	Ended	Fail
2	Chip Timestamp Read	000.043	Ended	Pass
4	VBAT Read	000.049	Ended	Pass
5	DC-DC Converter Level Test	000.042	Ended	Pass
6	Active Current Measurement	000.035	Ended	Pass
7	XTAL Trim	001.504	Started	n/a
8	Scan DUT Advertise Test	000.000	Not started	n/a
9	BLE RSSI test	000.000	Not started	n/a
10	Custom Test	000.000	Not started	n/a
11	External 32Khz Test	000.000	Not started	n/a
24	BootFwDownload2	000.000	Not started	n/a

IC: DA14531_01000FX2 | Test runs: 5 | Passed: 1554 | Failed: 2582 | Total: 1000000 | Remaining: 995864 | 00:03.28

Figure 110. DUTs fail during execution

5. **Test process completion**

- Successful completion – if all operations were successful (Pass) for all the DUTs tiles, lines in the operations table, and the start button are green.



1
SN: 483004152
BDA: 80:EA:CA:00:10:38
DutLogStop : Pass

2
SN: 483004153
BDA: 80:EA:CA:00:10:39
DutLogStop : Pass

3
SN: 483004154
BDA: 80:EA:CA:00:10:3A
DutLogStop : Pass

4
SN: 483004155
BDA: 80:EA:CA:00:10:38
DutLogStop : Pass

5
SN: 483004156
BDA: 80:EA:CA:00:10:3C
DutLogStop : Pass

6
SN: 483004157
BDA: 80:EA:CA:00:10:3D
DutLogStop : Pass

7
SN: 483004158
BDA: 80:EA:CA:00:10:3E
DutLogStop : Pass

8
SN: 483004159
BDA: 80:EA:CA:00:10:3F
DutLogStop : Pass

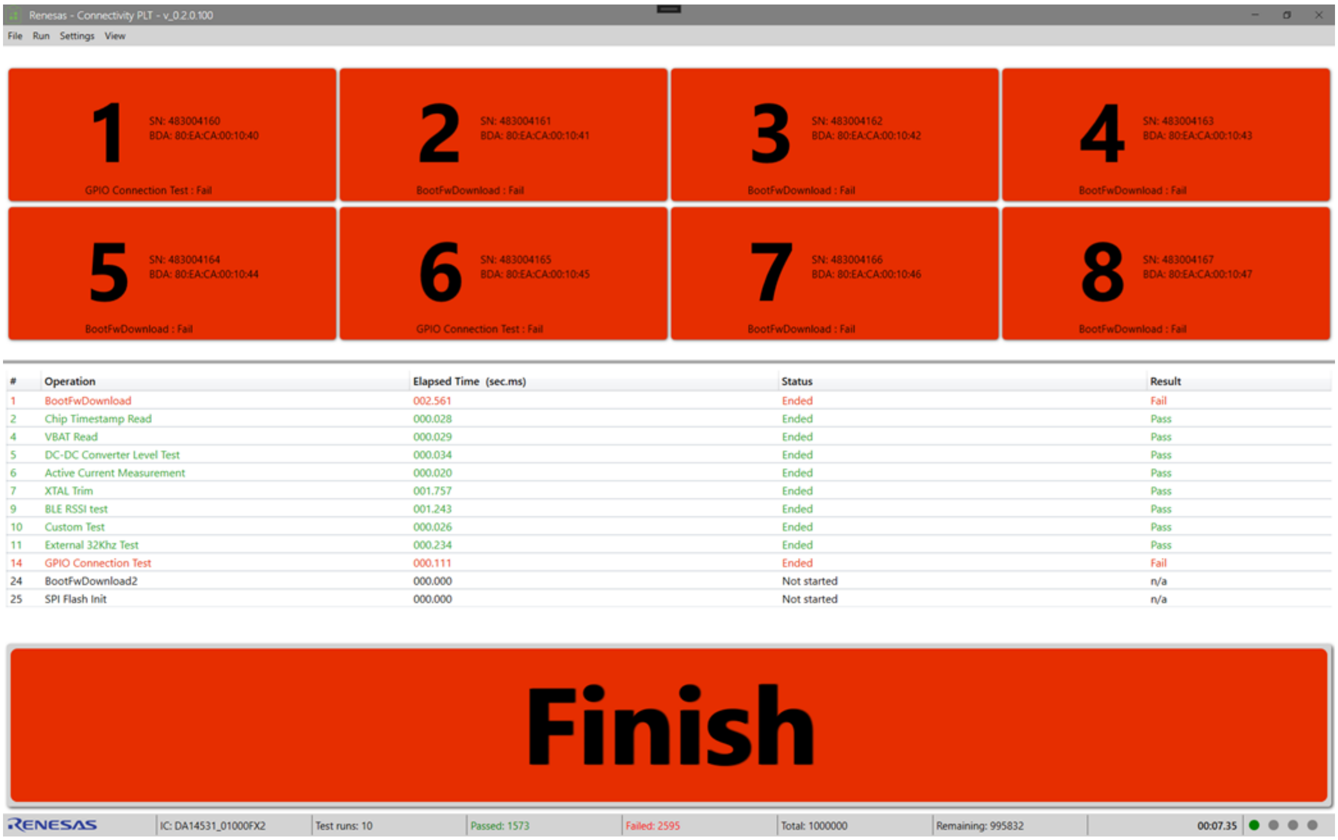
#	Operation	Elapsed Time (sec.ms)	Status	Result
1	BootFwDownload	001.974	Ended	Pass
2	Chip Timestamp Read	000.047	Ended	Pass
4	VBAT Read	000.053	Ended	Pass
5	DC-DC Converter Level Test	000.048	Ended	Pass
6	Active Current Measurement	000.031	Ended	Pass
7	XTAL Trim	002.377	Ended	Pass
9	BLE RSSI test	001.317	Ended	Pass
10	Custom Test	000.029	Ended	Pass
11	External 32Khz Test	000.258	Ended	Pass
24	BootFwDownload2	001.393	Ended	Pass
25	SPI Flash Init	000.125	Ended	Pass

IC: DA14531_01000FX2 | Test runs: 8 | Passed: 1565 | Failed: 2595 | Total: 1000000 | Remaining: 995840 | 00:08.55

Figure 111. Successful test sequence

- Incomplete testing due to failures.

  If during the test process all DUTs have at least one test that failed, then the test process stops as no more DUTs are available to continue. For this case, all DUT tiles are red whilst the operations table displays in red all the operations that failed for at least one DUT. Figure 112 shows that DUTs 1 and 6 failed on GPIO Connection Test and DUTs 2,3,4,5,7, and 8 failed in BootFwDownload. Failed command is indicated on each DUT tile.



1 SN: 483004160 BDA: 80:EA:CA:00:10:40
GPIO Connection Test : Fail

2 SN: 483004161 BDA: 80:EA:CA:00:10:41
BootFwDownload : Fail

3 SN: 483004162 BDA: 80:EA:CA:00:10:42
BootFwDownload : Fail

4 SN: 483004163 BDA: 80:EA:CA:00:10:43
BootFwDownload : Fail

5 SN: 483004164 BDA: 80:EA:CA:00:10:44
BootFwDownload : Fail

6 SN: 483004165 BDA: 80:EA:CA:00:10:45
GPIO Connection Test : Fail

7 SN: 483004166 BDA: 80:EA:CA:00:10:46
BootFwDownload : Fail

8 SN: 483004167 BDA: 80:EA:CA:00:10:47
BootFwDownload : Fail

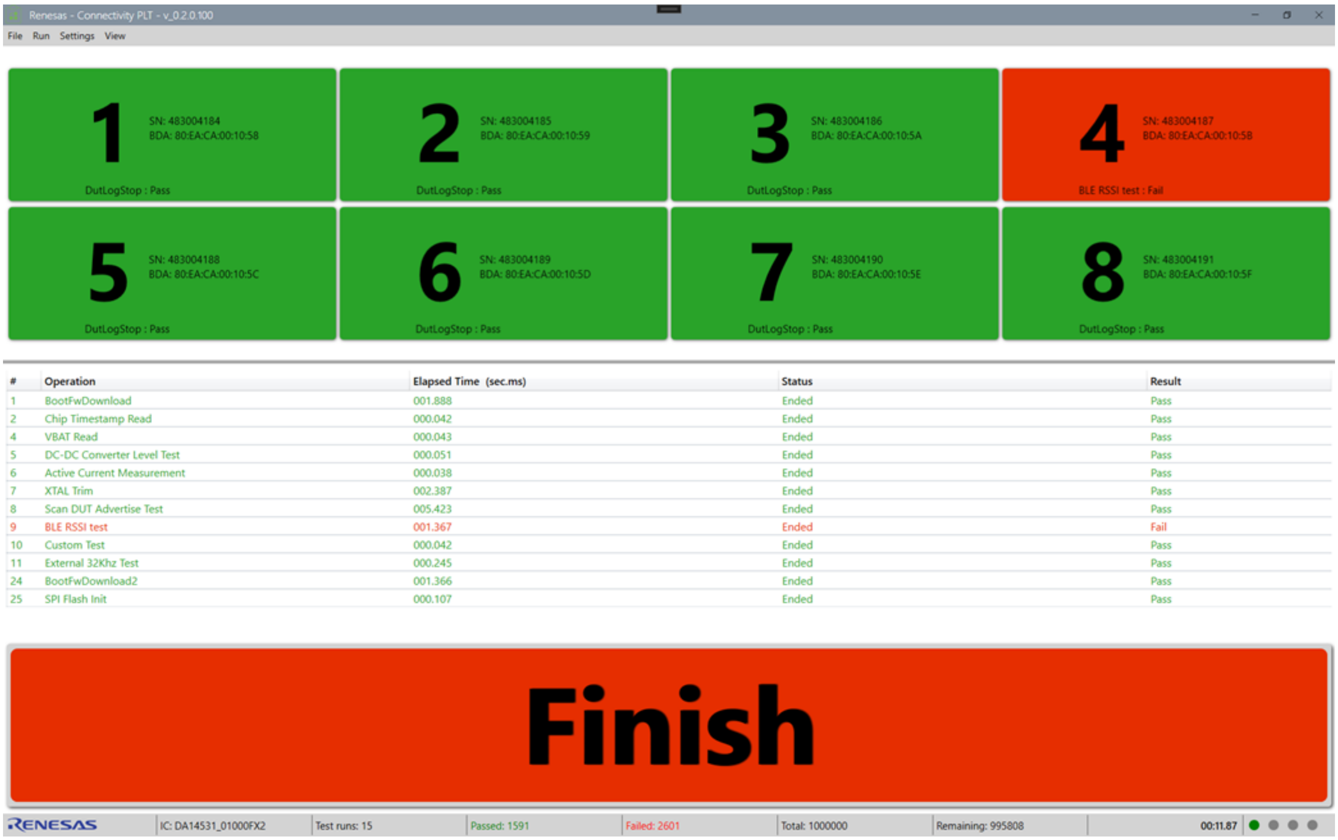
#	Operation	Elapsed Time (sec.ms)	Status	Result
1	BootFwDownload	002.561	Ended	Fail
2	Chip Timestamp Read	000.028	Ended	Pass
4	VBAT Read	000.029	Ended	Pass
5	DC-DC Converter Level Test	000.034	Ended	Pass
6	Active Current Measurement	000.020	Ended	Pass
7	XTAL Trim	001.757	Ended	Pass
9	BLE RSSI test	001.243	Ended	Pass
10	Custom Test	000.026	Ended	Pass
11	External 32Khz Test	000.234	Ended	Pass
14	GPIO Connection Test	000.111	Ended	Fail
24	BootFwDownload2	000.000	Not started	n/a
25	SPI Flash Init	000.000	Not started	n/a

IC: DA14531_01000FX2 | Test runs: 10 | Passed: 1573 | Failed: 2595 | Total: 1000000 | Remaining: 995832 | 00:07.35

Figure 112. Failed test sequence

- Partially successful completion

  The testing is considered partially successful when there are both passed and failed DUTs. Figure 113 shows that DUT 4 failed on BLE RSSI test but 1,2,3,5,6,7,8 passed the test sequence. Successful DUTs are green, failed are red, failed operation and start button is red.



1
SN: 483004184
BDA: 80:EA:CA:00:10:58
DutLogStop : Pass

2
SN: 483004185
BDA: 80:EA:CA:00:10:59
DutLogStop : Pass

3
SN: 483004186
BDA: 80:EA:CA:00:10:5A
DutLogStop : Pass

4
SN: 483004187
BDA: 80:EA:CA:00:10:5B
BLE RSSI test : Fail

5
SN: 483004188
BDA: 80:EA:CA:00:10:5C
DutLogStop : Pass

6
SN: 483004189
BDA: 80:EA:CA:00:10:5D
DutLogStop : Pass

7
SN: 483004190
BDA: 80:EA:CA:00:10:5E
DutLogStop : Pass

8
SN: 483004191
BDA: 80:EA:CA:00:10:5F
DutLogStop : Pass

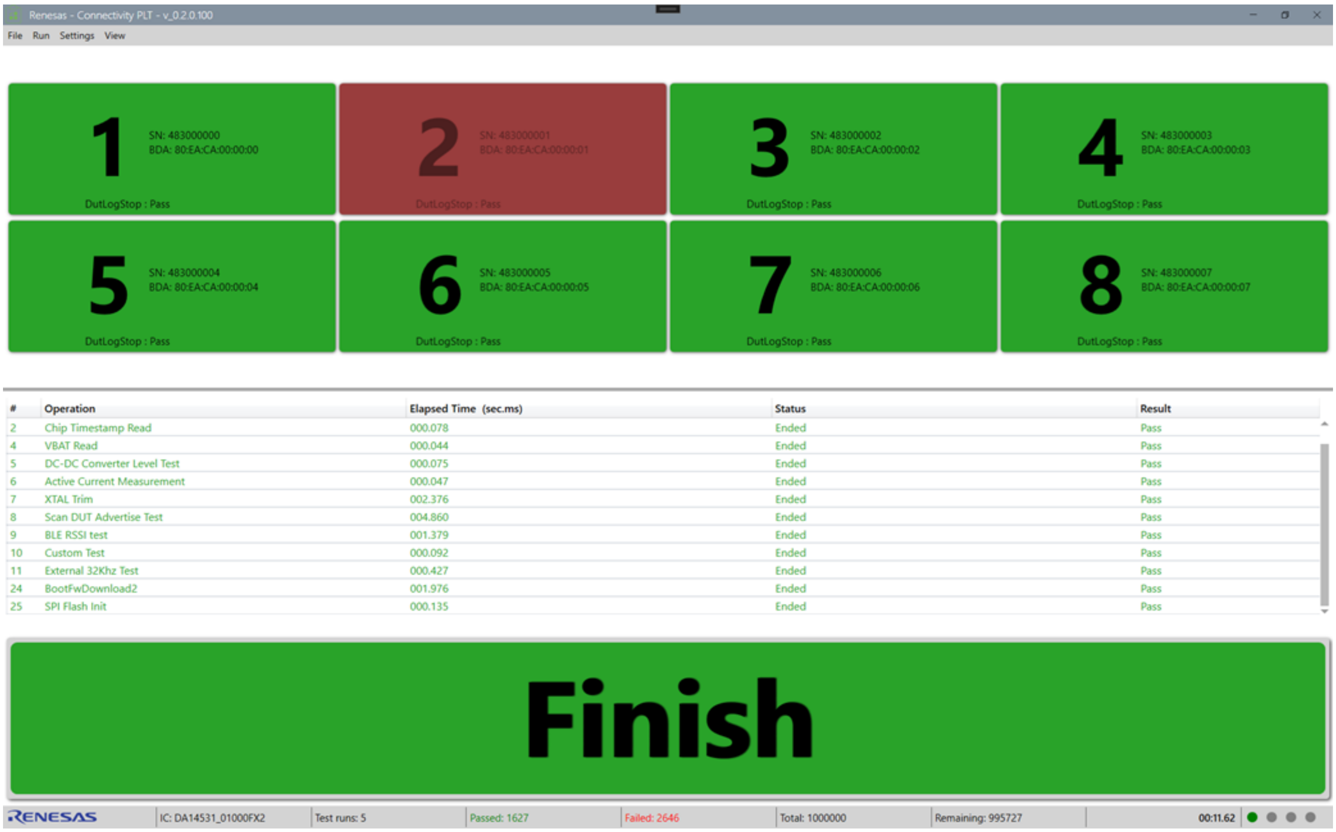
#	Operation	Elapsed Time (sec.ms)	Status	Result
1	BootFwDownload	001.888	Ended	Pass
2	Chip Timestamp Read	000.042	Ended	Pass
4	VBAT Read	000.043	Ended	Pass
5	DC-DC Converter Level Test	000.051	Ended	Pass
6	Active Current Measurement	000.038	Ended	Pass
7	XTAL Trim	002.387	Ended	Pass
8	Scan DUT Advertise Test	005.423	Ended	Pass
9	BLE RSSI test	001.367	Ended	Fail
10	Custom Test	000.042	Ended	Pass
11	External 32Khz Test	000.245	Ended	Pass
24	BootFwDownload2	001.366	Ended	Pass
25	SPI Flash Init	000.107	Ended	Pass

IC: DA14531_01000FX2 | Test runs: 15 | Passed: 1591 | Failed: 2601 | Total: 1000000 | Remaining: 995808 | 00:11.87

Figure 113. Partially successful test sequence

6. **Test Logs viewing**

   After the termination of the test sequence, clicking any tile brings up the log file for the specific DUT (Figure 114) or by opening the logs folder under the installation folder. (Figure 115).



1 SN: 483000000 BDA: 80:EA:CA:00:00:00 DutLogStop : Pass

2 SN: 483000001 BDA: 80:EA:CA:00:00:01 DutLogStop : Pass

3 SN: 483000002 BDA: 80:EA:CA:00:00:02 DutLogStop : Pass

4 SN: 483000003 BDA: 80:EA:CA:00:00:03 DutLogStop : Pass

5 SN: 483000004 BDA: 80:EA:CA:00:00:04 DutLogStop : Pass

6 SN: 483000005 BDA: 80:EA:CA:00:00:05 DutLogStop : Pass

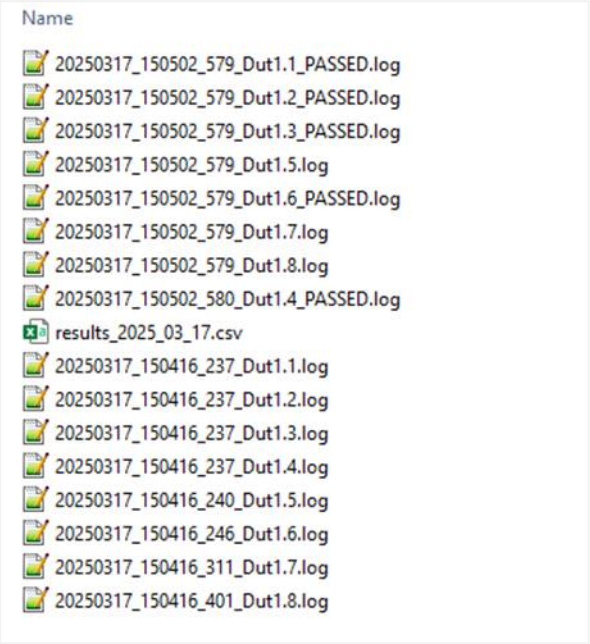
7 SN: 483000006 BDA: 80:EA:CA:00:00:06 DutLogStop : Pass

8 SN: 483000007 BDA: 80:EA:CA:00:00:07 DutLogStop : Pass

#	Operation	Elapsed Time (sec.ms)	Status	Result
2	Chip Timestamp Read	000.078	Ended	Pass
4	VBAT Read	000.044	Ended	Pass
5	DC-DC Converter Level Test	000.075	Ended	Pass
6	Active Current Measurement	000.047	Ended	Pass
7	XTAL Trim	002.376	Ended	Pass
8	Scan DUT Advertise Test	004.860	Ended	Pass
9	BLE RSSI test	001.379	Ended	Pass
10	Custom Test	000.092	Ended	Pass
11	External 32Khz Test	000.427	Ended	Pass
24	BootFwDownload2	001.976	Ended	Pass
25	SPI Flash Init	000.135	Ended	Pass

IC: DA14531_01000FX2 | Test runs: 5 | Passed: 1627 | Failed: 2646 | Total: 1000000 | Remaining: 995727 | 00:11.62

Figure 114. Click on DUT tile



Name

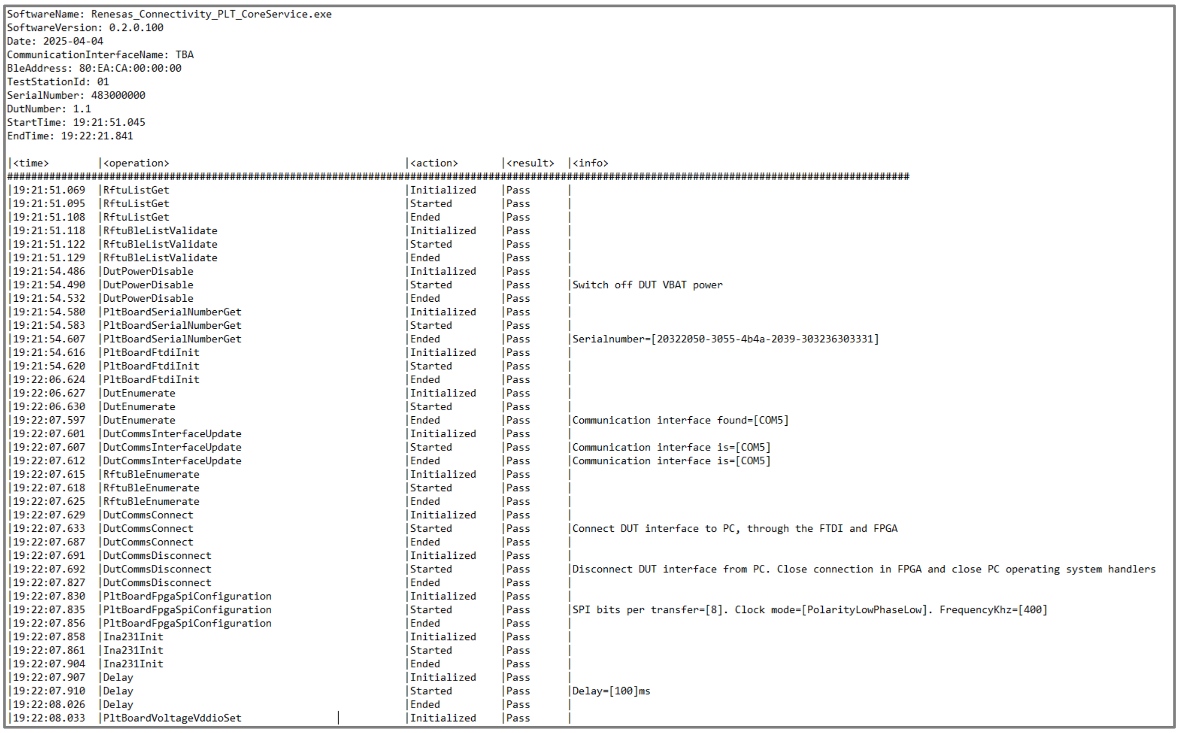
20250317_150502_579_Dut1.1_PASSED.log
20250317_150502_579_Dut1.2_PASSED.log
20250317_150502_579_Dut1.3_PASSED.log
20250317_150502_579_Dut1.5.log
20250317_150502_579_Dut1.6_PASSED.log
20250317_150502_579_Dut1.7.log
20250317_150502_579_Dut1.8.log
20250317_150502_580_Dut1.4_PASSED.log
results_2025_03_17.csv
20250317_150416_237_Dut1.1.log
20250317_150416_237_Dut1.2.log
20250317_150416_237_Dut1.3.log
20250317_150416_237_Dut1.4.log
20250317_150416_240_Dut1.5.log
20250317_150416_246_Dut1.6.log
20250317_150416_311_Dut1.7.log
20250317_150416_401_Dut1.8.log

Figure 115. Example of the log folder contents

7. DUT Log viewing

The log file for each DUT contains a detailed log of the test process and the test results. It can be found in the logs folder or by clicking the DUT tile at the completion of the test process.

A header is included in the log file providing details about connectivity PLT hardware and the software. It includes the firmware and software versions, the station name and test dates and times. It also provides information about DUT, such as the physical connection to the Connectivity PLT hardware and the virtual COM port used, the serial number and BD address assigned. See Figure 116.



```
SoftwareName: Renesas_Connectivity_PLT_CoreService.exe
SoftwareVersion: 0.2.0.100
Date: 2025-04-04
CommunicationInterfaceName: TBA
BleAddress: 80:EA:CA:00:00:00
TestStationId: 01
SerialNumber: 483000000
DutNumber: 1.1
StartTime: 19:21:51.045
EndTime: 19:22:21.841

|<time>        |<operation>                                      |<action>       |<result>  |<info>
#####################################################################################################################################################
|19:21:51.069  |RftuListGet                                      |Initialized    |Pass      |
|19:21:51.095  |RftuListGet                                      |Started        |Pass      |
|19:21:51.108  |RftuListGet                                      |Ended          |Pass      |
|19:21:51.118  |RftuBleListValidate                              |Initialized    |Pass      |
|19:21:51.122  |RftuBleListValidate                              |Started        |Pass      |
|19:21:51.129  |RftuBleListValidate                              |Ended          |Pass      |
|19:21:54.486  |DutPowerDisable                                  |Initialized    |Pass      |
|19:21:54.490  |DutPowerDisable                                  |Started        |Pass      |Switch off DUT VBAT power
|19:21:54.532  |DutPowerDisable                                  |Ended          |Pass      |
|19:21:54.580  |PltBoardSerialNumberGet                          |Initialized    |Pass      |
|19:21:54.583  |PltBoardSerialNumberGet                          |Started        |Pass      |
|19:21:54.607  |PltBoardSerialNumberGet                          |Ended          |Pass      |Serialnumber=[20322050-3055-4b4a-2039-303236303331]
|19:21:54.616  |PltBoardFtdiInit                                 |Initialized    |Pass      |
|19:21:54.620  |PltBoardFtdiInit                                 |Started        |Pass      |
|19:22:06.624  |PltBoardFtdiInit                                 |Ended          |Pass      |
|19:22:06.627  |DutEnumerate                                     |Initialized    |Pass      |
|19:22:06.630  |DutEnumerate                                     |Started        |Pass      |
|19:22:07.597  |DutEnumerate                                     |Ended          |Pass      |Communication interface found=[COM5]
|19:22:07.601  |DutCommsInterfaceUpdate                          |Initialized    |Pass      |
|19:22:07.607  |DutCommsInterfaceUpdate                          |Started        |Pass      |Communication interface is=[COM5]
|19:22:07.612  |DutCommsInterfaceUpdate                          |Ended          |Pass      |Communication interface is=[COM5]
|19:22:07.615  |RftuBleEnumerate                                 |Initialized    |Pass      |
|19:22:07.618  |RftuBleEnumerate                                 |Started        |Pass      |
|19:22:07.625  |RftuBleEnumerate                                 |Ended          |Pass      |
|19:22:07.629  |DutCommsConnect                                  |Initialized    |Pass      |
|19:22:07.633  |DutCommsConnect                                  |Started        |Pass      |Connect DUT interface to PC, through the FTDI and FPGA
|19:22:07.687  |DutCommsConnect                                  |Ended          |Pass      |
|19:22:07.691  |DutCommsDisconnect                               |Initialized    |Pass      |
|19:22:07.692  |DutCommsDisconnect                               |Started        |Pass      |Disconnect DUT interface from PC. Close connection in FPGA and close PC operating system handlers
|19:22:07.827  |DutCommsDisconnect                               |Ended          |Pass      |
|19:22:07.830  |PltBoardFpgaSpiConfiguration                     |Initialized    |Pass      |
|19:22:07.835  |PltBoardFpgaSpiConfiguration                     |Started        |Pass      |SPI bits per transfer=[8]. Clock mode=[PolarityLowPhaseLow]. FrequencyKhz=[400]
|19:22:07.856  |PltBoardFpgaSpiConfiguration                     |Ended          |Pass      |
|19:22:07.858  |Ina231Init                                       |Initialized    |Pass      |
|19:22:07.861  |Ina231Init                                       |Started        |Pass      |
|19:22:07.904  |Ina231Init                                       |Ended          |Pass      |
|19:22:07.907  |Delay                                            |Initialized    |Pass      |
|19:22:07.910  |Delay                                            |Started        |Pass      |Delay=[100]ms
|19:22:08.026  |Delay                                            |Ended          |Pass      |
|19:22:08.033  |PltBoardVoltageVddioSet                          |Initialized    |Pass      |
```

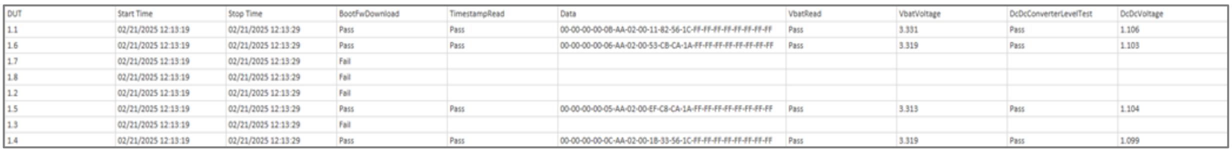
Figure 116. DUT log example

For the DUTs that have passed all tests, the log file is renamed with the word "_PASSED" at the end for easier retrieval.

The Log file is created at the beginning of each test, containing only the header and all information available at the time of creation. As the device testing progresses, the file is updated with the status of each test including information about the DUT and a timestamp of the event. After the tests finish the header is updated with the end time of the test and the firmware versions, which were retrieved during testing.

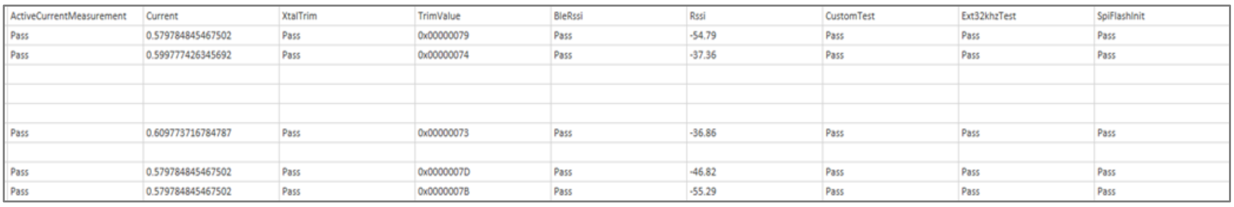
8. **CSV Log viewing**

   In addition to the individual DUT logs all results are summarized in a continuous CSV log file. The CSV logs are located in the same folder as the DUT logs and are rotated in a daily basis. Every CSV file has a filename indicating the date created, for example "results_2024_10_15.csv".



DUT	Start Time	Stop Time	BootFwDownload	TimestampRead	Data	VbatRead	VbatVoltage	DcDcConverterLevelTest	DcDcVoltage
1.1	02/21/2025 12:13:19	02/21/2025 12:13:29	Pass	Pass	00-00-00-00-08-AA-02-00-11-82-56-1C-FF-FF-FF-FF-FF-FF-FF-FF	Pass	3.331	Pass	1.106
1.6	02/21/2025 12:13:19	02/21/2025 12:13:29	Pass	Pass	00-00-00-00-06-AA-02-00-53-CB-CA-1A-FF-FF-FF-FF-FF-FF-FF-FF	Pass	3.319	Pass	1.103
1.7	02/21/2025 12:13:19	02/21/2025 12:13:29	Fail						
1.8	02/21/2025 12:13:19	02/21/2025 12:13:29	Fail						
1.2	02/21/2025 12:13:19	02/21/2025 12:13:29	Fail						
1.5	02/21/2025 12:13:19	02/21/2025 12:13:29	Pass	Pass	00-00-00-00-05-AA-02-00-EF-C8-CA-1A-FF-FF-FF-FF-FF-FF-FF-FF	Pass	3.313	Pass	1.104
1.3	02/21/2025 12:13:19	02/21/2025 12:13:29	Fail						
1.4	02/21/2025 12:13:19	02/21/2025 12:13:29	Pass	Pass	00-00-00-00-0C-AA-02-00-1B-33-56-1C-FF-FF-FF-FF-FF-FF-FF-FF	Pass	3.319	Pass	1.099

Figure 117. CSV log example (part 1)

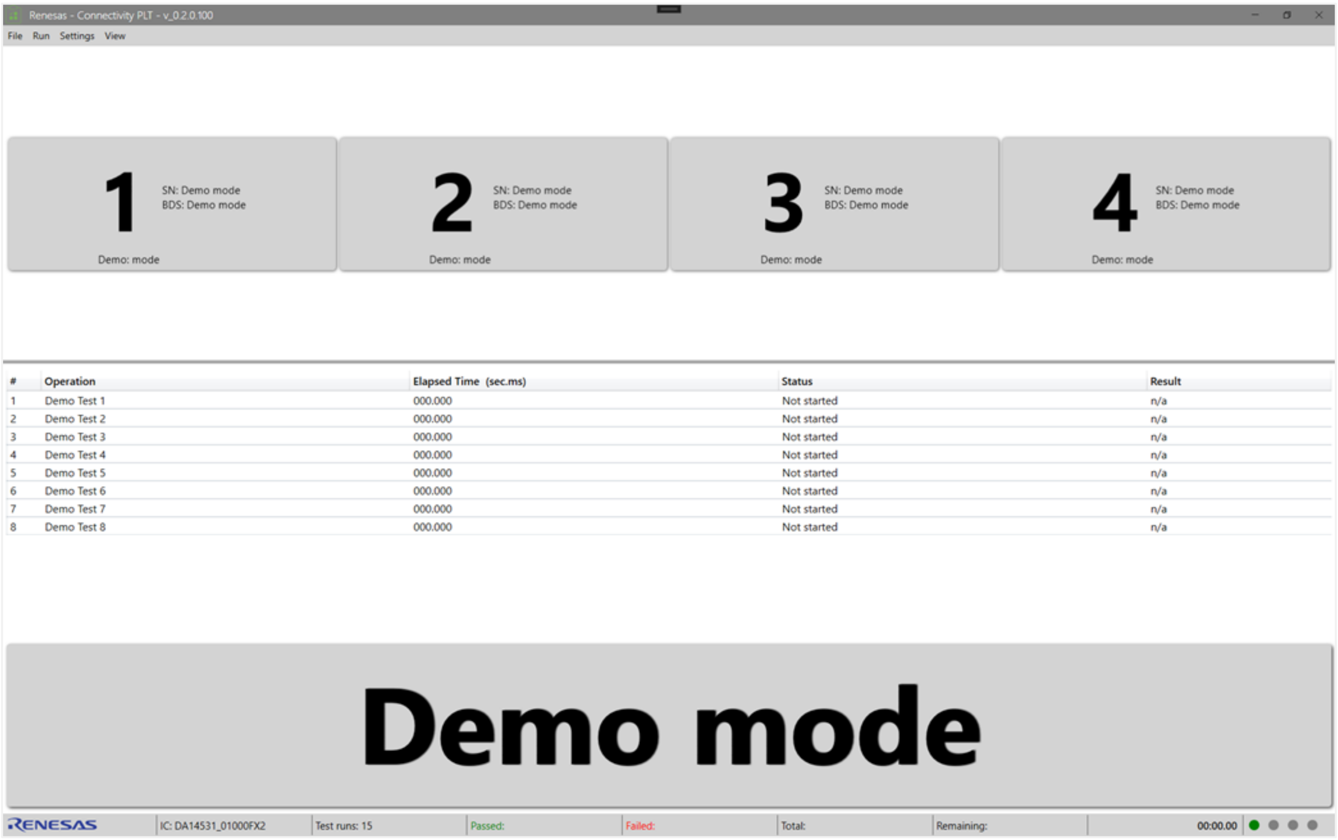


ActiveCurrentMeasurement	Current	XtalTrim	TrimValue	BleRssi	Rssi	CustomTest	Ext32khzTest	SpiFlashInit
Pass	0.579784845467502	Pass	0x00000079	Pass	-54.79	Pass	Pass	Pass
Pass	0.599777426345692	Pass	0x00000074	Pass	-37.36	Pass	Pass	Pass
Pass	0.609773716784787	Pass	0x00000073	Pass	-36.86	Pass	Pass	Pass
Pass	0.579784845467502	Pass	0x0000007D	Pass	-46.82	Pass	Pass	Pass
Pass	0.579784845467502	Pass	0x0000007B	Pass	-55.29	Pass	Pass	Pass

Figure 118. CSV log example (part 2)

9.3 Error Handling

Connectivity PLT switched to a demo mode when various configuration and hardware issues occur. Demo mode has no functionality, it only displays a basic setup screen, Figure 119.



1 SN: Demo mode
BDS: Demo mode
Demo: mode

2 SN: Demo mode
BDS: Demo mode
Demo: mode

3 SN: Demo mode
BDS: Demo mode
Demo: mode

4 SN: Demo mode
BDS: Demo mode
Demo: mode

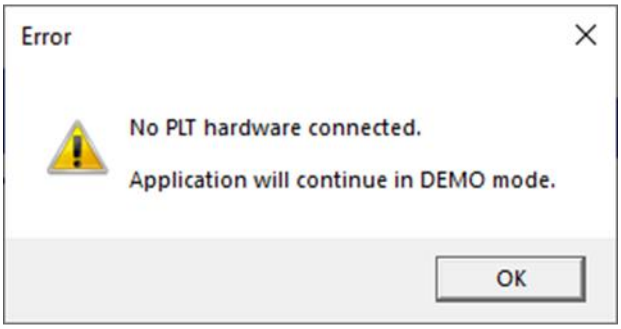
#	Operation	Elapsed Time (sec.ms)	Status	Result
1	Demo Test 1	000.000	Not started	n/a
2	Demo Test 2	000.000	Not started	n/a
3	Demo Test 3	000.000	Not started	n/a
4	Demo Test 4	000.000	Not started	n/a
5	Demo Test 5	000.000	Not started	n/a
6	Demo Test 6	000.000	Not started	n/a
7	Demo Test 7	000.000	Not started	n/a
8	Demo Test 8	000.000	Not started	n/a

Demo mode

IC: DA14531_01000FX2 | Test runs: 15 | Passed: | Failed: | Total: | Remaining: | 00:00.00 ● ● ● ●

Figure 119. Demo mode

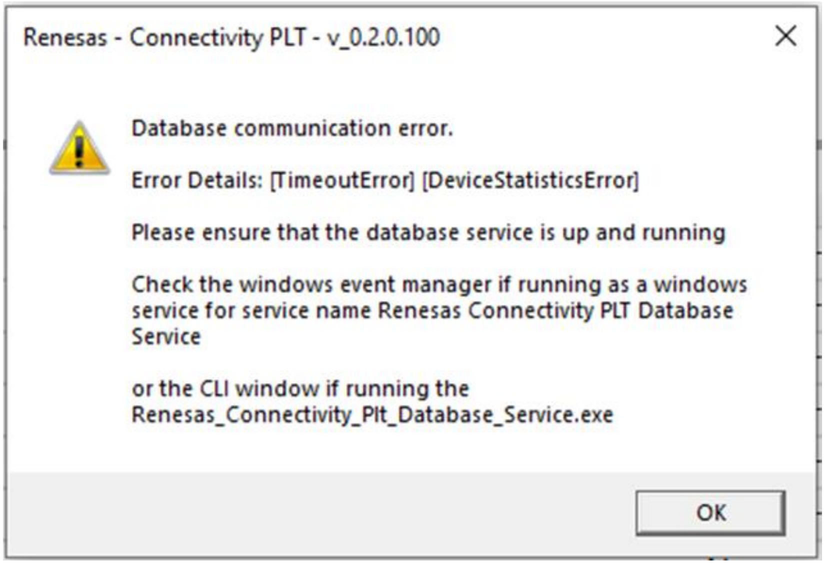
In some cases where there are issues in the initialization, a reload of the configuration might help resolve them. To reload the configuration, go to **File**> **Reload Configuration** or by press F5. Common causes of a failed initialization are communication errors between the different services that can happen on the first run of the application or connectivity issues with hardware. If a reload of the configuration doesn’t solve the issue, check hardware connectivity and that the Connectivity PLT Core Service and Connectivity PLT Database Service are running.



No PLT hardware connected.

Application will continue in DEMO mode.

Figure 120. Hardware communication error



Database communication error.

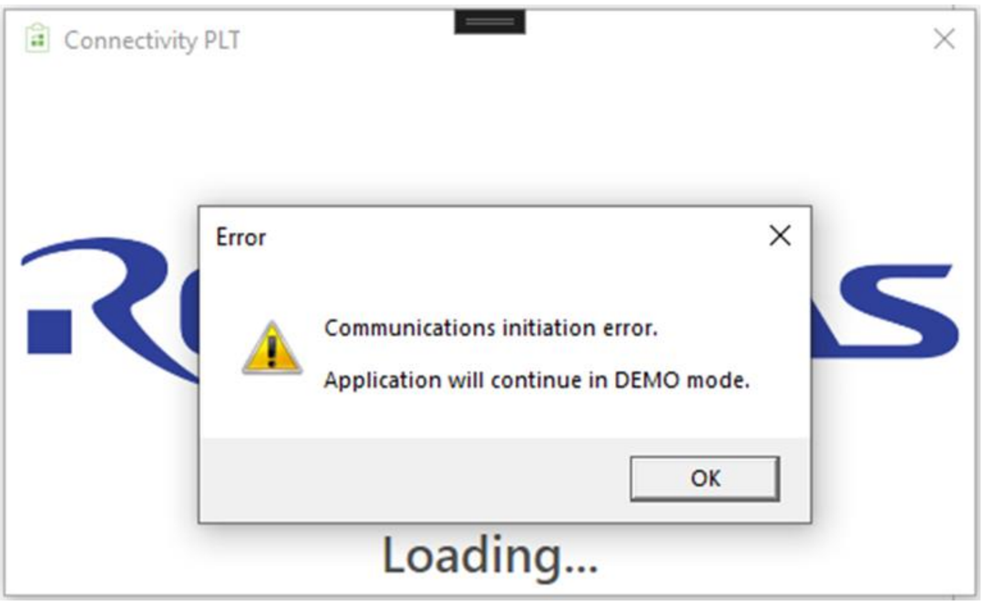
Error Details: [TimeoutError] [DeviceStatisticsError]

Please ensure that the database service is up and running

Check the windows event manager if running as a windows service for service name Renesas Connectivity PLT Database Service

or the CLI window if running the Renesas_Connectivity_Plt_Database_Service.exe

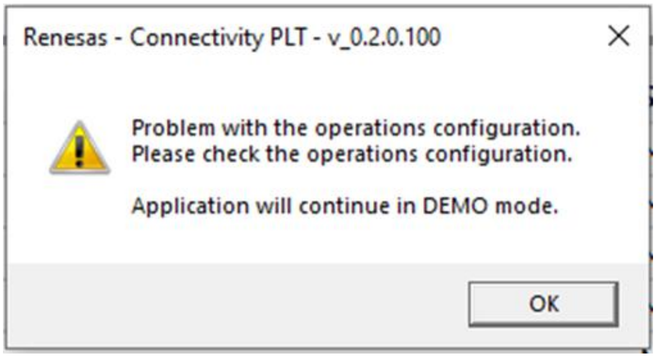
Figure 121. Database communication error



Communications initiation error.

Application will continue in DEMO mode.

Figure 122. Core Service communication error



Problem with the operations configuration. Please check the operations configuration.

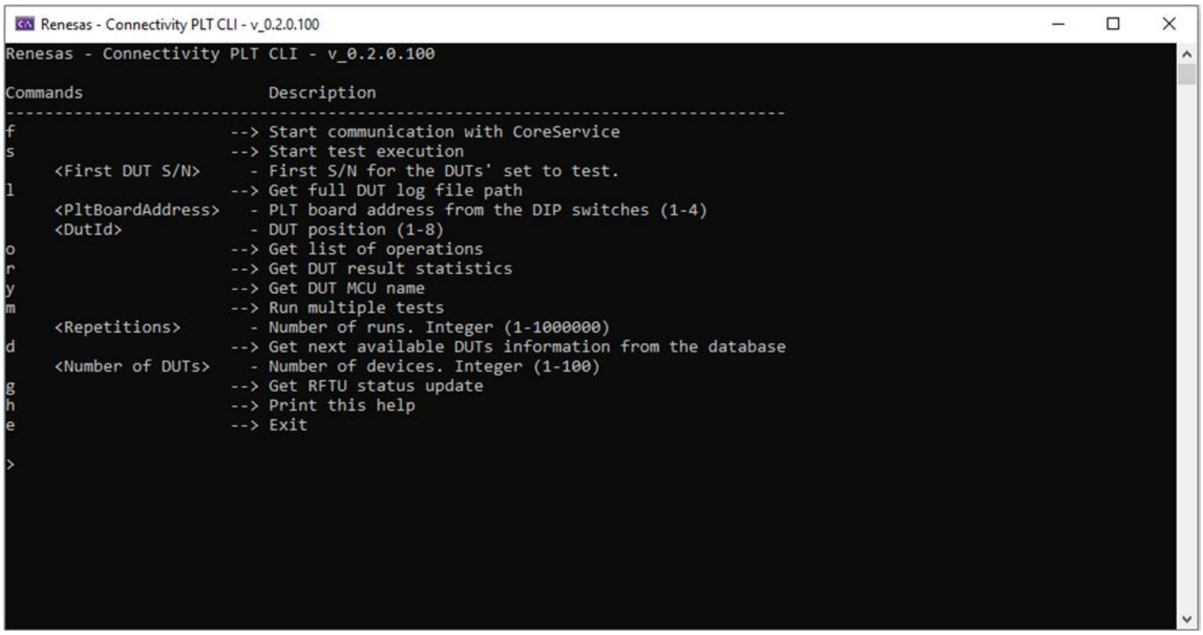
Application will continue in DEMO mode.

Figure 123. Operations configuration error

10. Connectivity PLT CLI Application

The Connectivity PLT CLI application (`Renesas_Connectivity_PLT_Cli.exe`) is a command line Interface application with functionality and features similar to the Connectivity PLT Application. In addition to the standard tasks for starting and monitoring the test process – based on the same configuration structure – there are additional commands available that can aid interoperability with other applications.

The application can be started from the start menu shortcut or by executing `Renesas_Connectivity_PLT_Cli.exe` in the installation folder. A command menu is displayed when the application is started with no parameters Figure 124. All the commands stated in this menu can also be used as parameters to automatically execute from the command line.



```
Renesas - Connectivity PLT CLI - v_0.2.0.100

Commands                   Description
--------------------------------------------------------------------------------
f                       --> Start communication with CoreService
s                       --> Start test execution
     <First DUT S/N>      - First S/N for the DUTs' set to test.
l                       --> Get full DUT log file path
     <PltBoardAddress>    - PLT board address from the DIP switches (1-4)
     <DutId>              - DUT position (1-8)
o                       --> Get list of operations
r                       --> Get DUT result statistics
y                       --> Get DUT MCU name
m                       --> Run multiple tests
     <Repetitions>        - Number of runs. Integer (1-1000000)
d                       --> Get next available DUTs information from the database
     <Number of DUTs>     - Number of devices. Integer (1-100)
g                       --> Get RFTU status update
h                       --> Print this help
e                       --> Exit

>
```

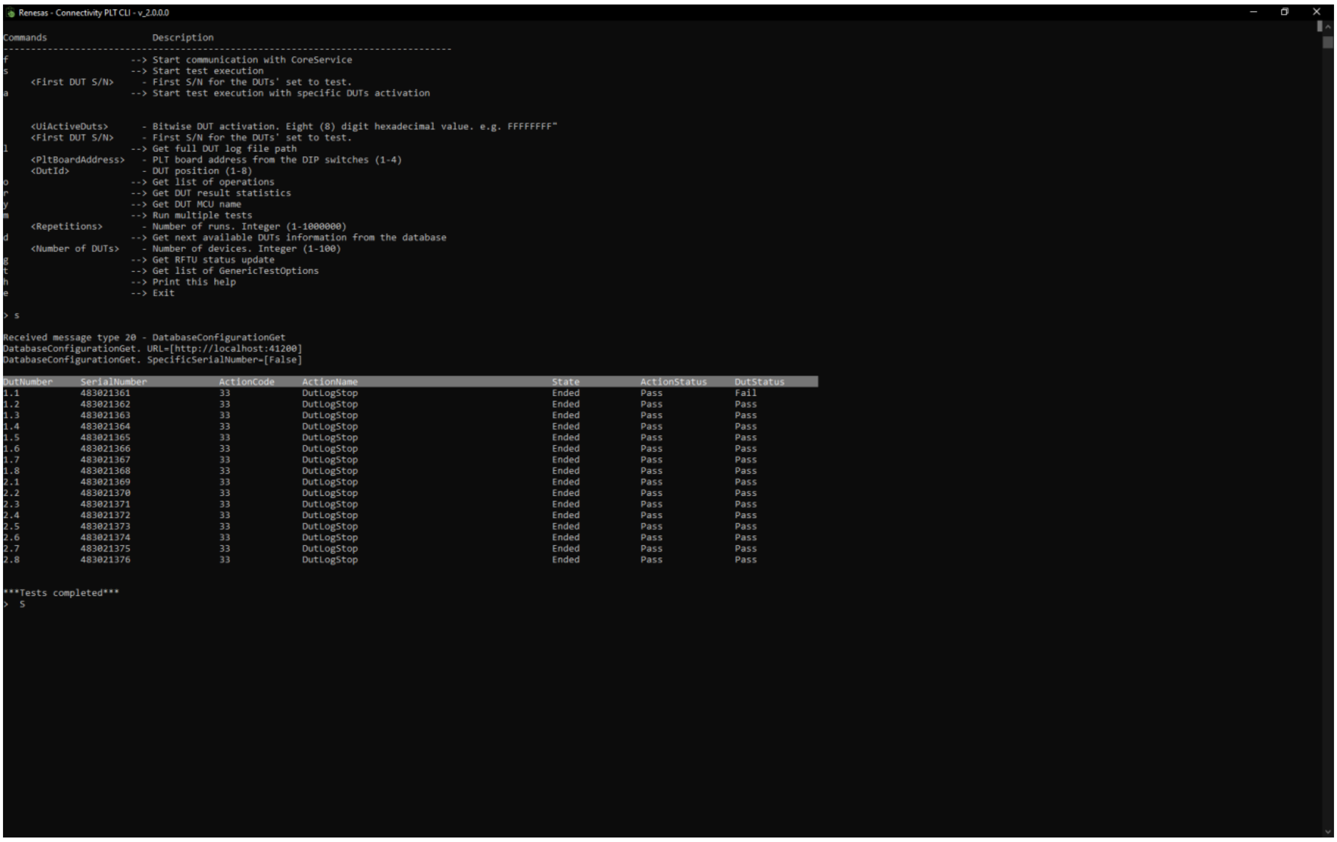
Figure 124. Execution CLI start screen

Table 56. CLI commands

Command	Arguments	Description
`f`	-	Establishes communication with CoreService.
`s`	First DUT serial number	Starts the test sequence.
`l`	<PltBoardAddress> <DutId>	Returns the full log file path of a specific DUT. Log files are accessible only after running the test sequence.
`o`	-	Returns the operations test sequence. The operations list can be configured on Renesas_Connectivity_PLT_Configuration.
`r`	-	Returns the overall statistics: total devices, remaining devices, passed and failed DUTs.
`y`	-	Returns the MCU name.
`m`	<Repetitions>	Runs the test sequence on repeat, according to the number of repetitions entered.
`d`	<Number of DUTs>	Gets the next available DUT information from the database (S/N and BD Address).
`g`	-	Gets the RFTU status (name, type, activity, connection).
`h`	-	Returns the menu options.
`e`	-	Exits the application.

10.1 CLI Test Execution

The following is an example CLI test run result.



```
Commands                   Description
--------------------------------------------------------------------------------
f                      --> Start communication with CoreService
s                      --> Start test execution
     <First DUT S/N>     - First S/N for the DUTs' set to test.
a                      --> Start test execution with specific DUTs activation


     <UiActiveDuts>      - Bitwise DUT activation. Eight (8) digit hexadecimal value. e.g. FFFFFFFF"
     <First DUT S/N>     - First S/N for the DUTs' set to test.
l                      --> Get full DUT log file path
     <PltBoardAddress>   - PLT board address from the DIP switches (1-4)
     <DutId>             - DUT position (1-8)
o                      --> Get list of operations
r                      --> Get DUT result statistics
y                      --> Get DUT MCU name
m                      --> Run multiple tests
     <Repetitions>       - Number of runs. Integer (1-1000000)
d                      --> Get next available DUTs information from the database
     <Number of DUTs>    - Number of devices. Integer (1-100)
g                      --> Get RFTU status update
t                      --> Get list of GenericTestOptions
h                      --> Print this help
e                      --> Exit

> s

Received message type 20 - DatabaseConfigurationGet
DatabaseConfigurationGet. URL=[http://localhost:41200]
DatabaseConfigurationGet. SpecificSerialNumber=[False]

DutNumber     SerialNumber             ActionCode     ActionName                                   State          ActionStatus     DutStatus
1.1           483021361                33             DutLogStop                                   Ended          Pass             Fail
1.2           483021362                33             DutLogStop                                   Ended          Pass             Pass
1.3           483021363                33             DutLogStop                                   Ended          Pass             Pass
1.4           483021364                33             DutLogStop                                   Ended          Pass             Pass
1.5           483021365                33             DutLogStop                                   Ended          Pass             Pass
1.6           483021366                33             DutLogStop                                   Ended          Pass             Pass
1.7           483021367                33             DutLogStop                                   Ended          Pass             Pass
1.8           483021368                33             DutLogStop                                   Ended          Pass             Pass
2.1           483021369                33             DutLogStop                                   Ended          Pass             Pass
2.2           483021370                33             DutLogStop                                   Ended          Pass             Pass
2.3           483021371                33             DutLogStop                                   Ended          Pass             Pass
2.4           483021372                33             DutLogStop                                   Ended          Pass             Pass
2.5           483021373                33             DutLogStop                                   Ended          Pass             Pass
2.6           483021374                33             DutLogStop                                   Ended          Pass             Pass
2.7           483021375                33             DutLogStop                                   Ended          Pass             Pass
2.8           483021376                33             DutLogStop                                   Ended          Pass             Pass


***Tests completed***
>  S
```

Figure 125 CLI Test Execution

11. Connectivity PLT Core Service

The Connectivity PLT Core Service is the central component of the PLT system and hosts a WebSocket service used by client applications, including the Connectivity PLT application and the Connectivity PLT CLI.

This service must be installed on the Windows machine that is directly connected to the Connectivity PLT hardware through USB. The Core Service can operate in two modes:

- **As a Windows Service** – runs in the background automatically with no user interaction required.
- **As a CLI Application** – runs in a command-line interface for manual control and special functions.

Under normal circumstances, the service runs silently in the background, requiring no user interaction. However, for advanced tasks or special operations within the Connectivity PLT system, the service must be run in CLI mode to provide an interface for these functions.

11.1 Operation in Service Mode

In Service mode, the Connectivity PLT Core Service acts as the link between the hardware and the user applications, while also serving as the executor for all operations. When a request is received from a client application, the service loads the relevant configuration files that define the parameters for the requested operation.

In addition to handling direct communication with the hardware, the service is responsible for the detection, configuration, and initialization of Connectivity PLT boards, RFTUs, and DUTs.

The Core Service remains idle until a client connects and begins issuing commands. Once a request is received, the Core Service executes the required operations, providing real-time updates to the client throughout the process. Upon completion, it returns the results to the client. The operations' sequences depends on the parameters and commands listed in the configuration files and does not depend on the continued commands form the client.

The Connectivity PLT Core Service communicates to the user front end (graphical or CLI) using messages.

Both request and reply messages consist of the Message Type ID field and parameters field. The Type Id field is an integer number, identifying the type of data. This field has the same value for both request and reply to messages.

Table 57 shows the requests and the corresponding reply messages supported by the Core Service.

Table 57. Core service messages

Message type	Message type ID	Description
Start Test	2	CoreService starts test execution
Dut Status Update	10	DUT status update info is sent to the Client
Rftu Status Update	11	RFTUs' status update info is sent to the Client
PltBoard Configuration	14	PLT Boards Configuration info is sent to the Client
Dut Log FilePath	15	DUT log file path info is sent to the Client
Operations	16	Operations list info is sent to the Client
Device Statistics	17	Device Statistics info from the Database is sent to the Client
Dut Mcu Name	18	The name of the DUT's MCU is sent to the Client
Device Info	19	Device info list from the Database is sent to the Client

Table 58 shows a list of error messages.

Table 58. Core service error messages

Error message	Error ID	Description
NoError	0	Successful request, no error returned from CoreService.
NoPltBoardError	1	No connected PLT board found.
PltBoardNumberError	2	Error in the number of PLT boards connected.
PltBoardAddressingError	3	Error in PLT Boards addressing. Probably a misconfiguration of the PLT boards' DIP switches.
DutDatabaseError	4	Error of the Database communication.
UsbChainError	5	Error in the PLT board daisy chaining setup.
DutLogFilePathError	6	Error in retrieving the DUT log file path.
OperationsError	7	Error in getting the Operations list.
StartTestsError	8	Error when attempting test execution.
TimeoutError	9	Timeout error in the communication between the client and the server.
CommsInitError	10	Error of CoreService - PLT Client application connection.
DeviceStatisticsError	11	Error in retrieving Device Statistics from the Database.
DutMcuNameError	12	Error when attempting to get the MCU name of a DUT.
DeviceInfoError	14	Error in retrieving Device Info from the Database.
RftuConfigurationError	15	Error in the configuration of the RFTUs.
RftuConnectionError	16	Error of RFTU connection.
SerialNumberNotFoundError	17	Error in getting a given Serial Number from the Database.
OtherError	13	Other error cases, not described above in this table.

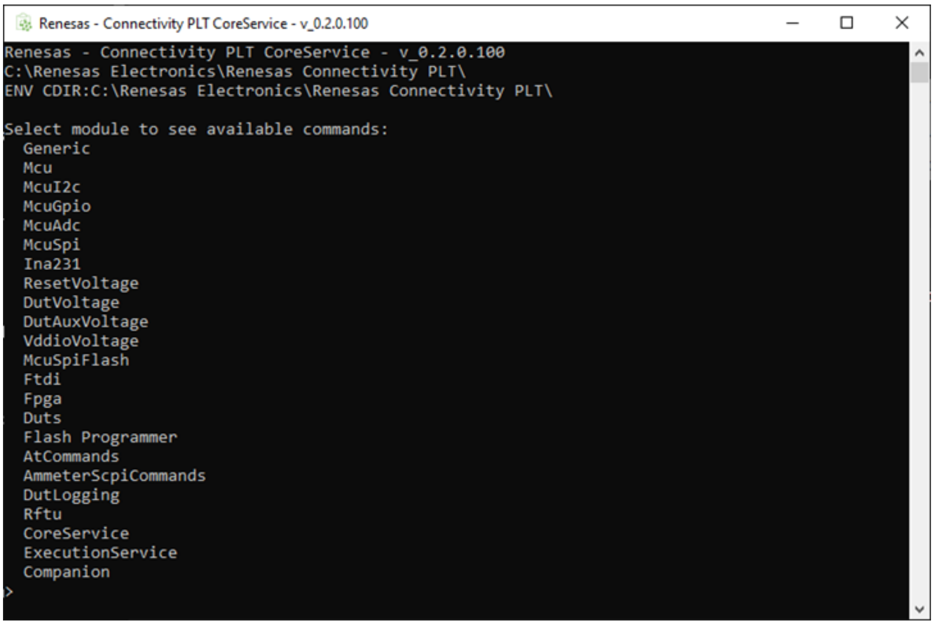
11.2 Operation in CLI Mode

If the Connectivity PLT Core Service is installed as a windows service (see Section 6.2) it is required to stop the windows service before starting it in CLI mode. This can be done through the Connectivity PLT Service Agent or any other of the standard Windows methods of starting and stopping services (Services Application, PowerShell, Command prompt). The service name is **Renesas Connectivity PLT CoreService.**

The Core Service can be started through the shortcut in the start menu or by launching command prompt and executing `Renesas_Connectivity_PLT_CoreService.exe CLI` within the installation folder, note the additional parameter CLI.

Note that while in IDLE state, a client can connect to the Core Service same as if it was running in the background service, Figure 126.

Many of the functions at this stage fall outside the scope of this user manual as they are mainly used for development purposes. All the user functionality can be accessed through the dedicated Connectivity PLT CLI application (see Section 10).



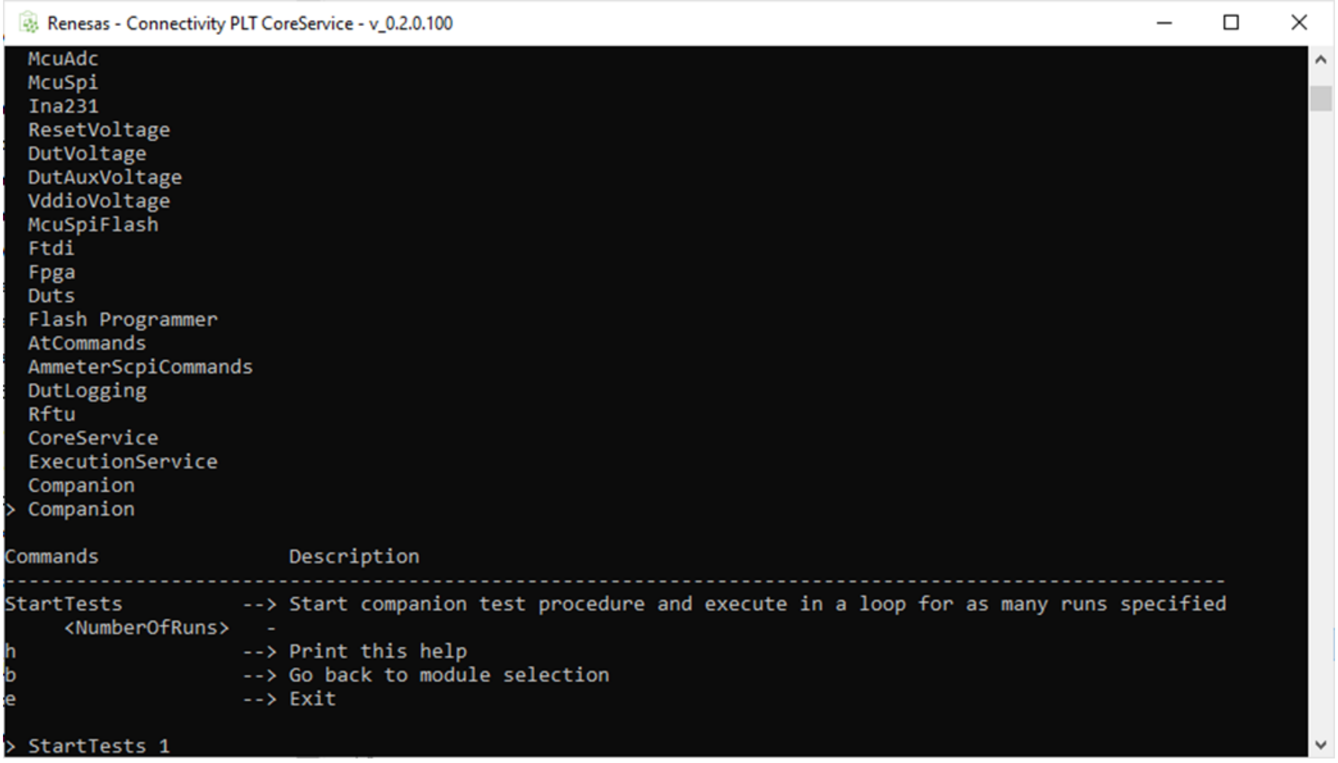
```
Renesas - Connectivity PLT CoreService - v_0.2.0.100
C:\Renesas Electronics\Renesas Connectivity PLT\
ENV CDIR:C:\Renesas Electronics\Renesas Connectivity PLT\

Select module to see available commands:
  Generic
  Mcu
  McuI2c
  McuGpio
  McuAdc
  McuSpi
  Ina231
  ResetVoltage
  DutVoltage
  DutAuxVoltage
  VddioVoltage
  McuSpiFlash
  Ftdi
  Fpga
  Duts
  Flash Programmer
  AtCommands
  AmmeterScpiCommands
  DutLogging
  Rftu
  CoreService
  ExecutionService
  Companion
>
```

Figure 126. Core Service in CLI mode initial screen

Running the Core Service in CLI mode allows attaching a dedicated companion board to each Connectivity PLT main board to perform self-testing and calibration. Once the companion board is attached the test process can be initiated by the Core Service in CLI mode.

Following the main screen, type Companion to enter the companion boards test menu. Following this type StartTests 1 to start the test process. The parameter 1 is the number of iterations to perform, Figure 127.



```
  McuAdc
  McuSpi
  Ina231
  ResetVoltage
  DutVoltage
  DutAuxVoltage
  VddioVoltage
  McuSpiFlash
  Ftdi
  Fpga
  Duts
  Flash Programmer
  AtCommands
  AmmeterScpiCommands
  DutLogging
  Rftu
  CoreService
  ExecutionService
  Companion
> Companion

Commands                Description
---------------------------------------------------------------------------------------------------------
StartTests          --> Start companion test procedure and execute in a loop for as many runs specified
     <NumberOfRuns>   -
h                   --> Print this help
b                   --> Go back to module selection
e                   --> Exit

> StartTests 1
```

Figure 127. Companion board tests

The Core Service runs through a number of tests as defined in the `CompanionTests.json` in the configuration files folder. Following the completion of the test process a pass/fail message is displayed. The pass/fail criteria can be adjusted depending on the standards of the production line.

12. Connectivity PLT Service Agent

The Connectivity PLT Service Agent is a small application designed to be present in the system tray to provide a quick way to start and stop the Connectivity PLT windows services as well as offer a live real time log of the Connectivity PLT Core Service execution. The application is installed automatically, and a shortcut is placed in the windows all-users start-up folder, so that it automatically starts after a reboot of the system.

The Service Agent can be started manually from the start menu or automatically during windows start. The tray icon is located either directly on the visible tray or on the extended tray which can be shown by clicking the tray icon expansion arrow, Figure 128.

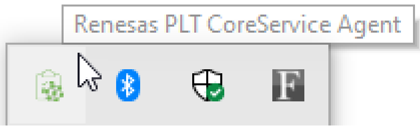


Figure 128. Service Agent icon

By clicking the icon, the Service Agent menu appears where the Core Service and Database services can be started and stopped, as well as a live view of the Core Service Log can be started, Figure 129.

The Core Service Console can be used to monitor the communication between the Connectivity PLT application and the Core Service as well as the status of the operations, Figure 130.

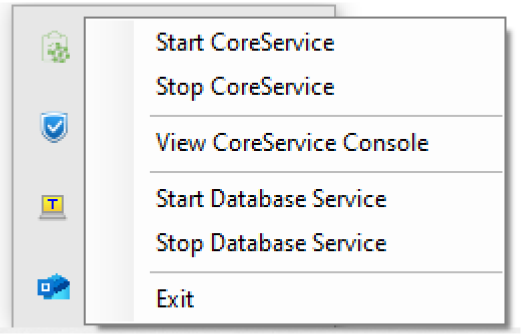
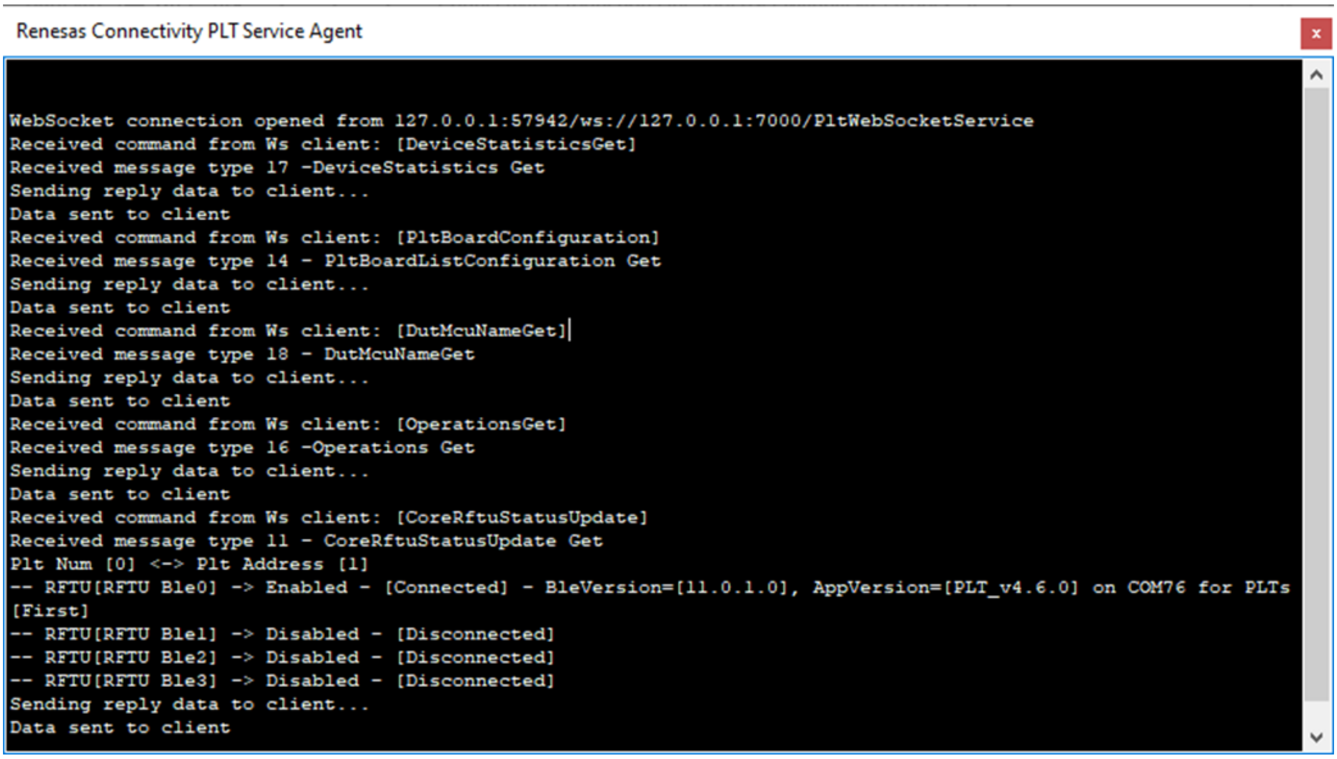


Figure 129. Service Agent menu



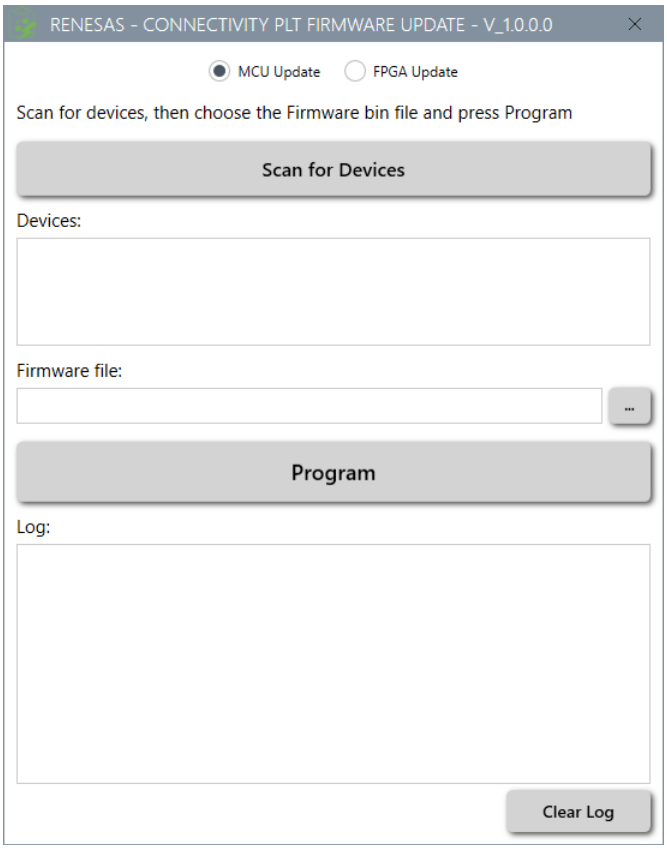
```
WebSocket connection opened from 127.0.0.1:57942/ws://127.0.0.1:7000/PltWebSocketService
Received command from Ws client: [DeviceStatisticsGet]
Received message type 17 -DeviceStatistics Get
Sending reply data to client...
Data sent to client
Received command from Ws client: [PltBoardConfiguration]
Received message type 14 - PltBoardListConfiguration Get
Sending reply data to client...
Data sent to client
Received command from Ws client: [DutMcuNameGet]
Received message type 18 - DutMcuNameGet
Sending reply data to client...
Data sent to client
Received command from Ws client: [OperationsGet]
Received message type 16 -Operations Get
Sending reply data to client...
Data sent to client
Received command from Ws client: [CoreRftuStatusUpdate]
Received message type 11 - CoreRftuStatusUpdate Get
Plt Num [0] <-> Plt Address [1]
-- RFTU[RFTU Ble0] -> Enabled - [Connected] - BleVersion=[11.0.1.0], AppVersion=[PLT_v4.6.0] on COM76 for PLTs
[First]
-- RFTU[RFTU Ble1] -> Disabled - [Disconnected]
-- RFTU[RFTU Ble2] -> Disabled - [Disconnected]
-- RFTU[RFTU Ble3] -> Disabled - [Disconnected]
Sending reply data to client...
Data sent to client
```

Figure 130. Service Agent Core Service log view

13. Connectivity PLT Firmware Update Application

The Connectivity PLT Firmware Update application (`Renesas_Connectivity_PLT_Firmware_Update.exe`) is a tool to update the SPI Flash memory of the MCU and the FPGA.

NOTE
For PLT Firmware Update Application to work, the SAM-Ba driver should be installed. See Section 6.4.



RENESAS - CONNECTIVITY PLT FIRMWARE UPDATE - V_1.0.0.0

● MCU Update ○ FPGA Update

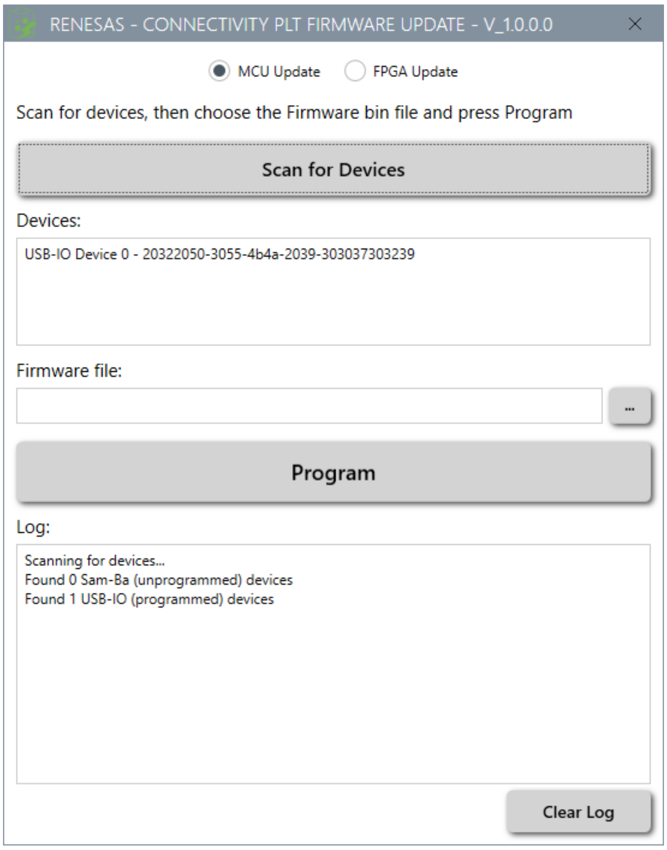
Scan for devices, then choose the Firmware bin file and press Program

Figure 131. Firmware update application initial screen

13.1 MCU Update

To update MCU firmware:

1. In the top of **Renesas – Connectivity PLT Firmware Update** window, select **MCU Update**, and then click **Scan for Devices** (Figure 131).
2. If the hardware is connected correctly, you should see from one to four USB-IO devices corresponding to each connected PLT board, see Figure 132.



RENESAS - CONNECTIVITY PLT FIRMWARE UPDATE - V_1.0.0.0

● MCU Update ○ FPGA Update

Scan for devices, then choose the Firmware bin file and press Program

Devices:

USB-IO Device 0 - 20322050-3055-4b4a-2039-303037303239

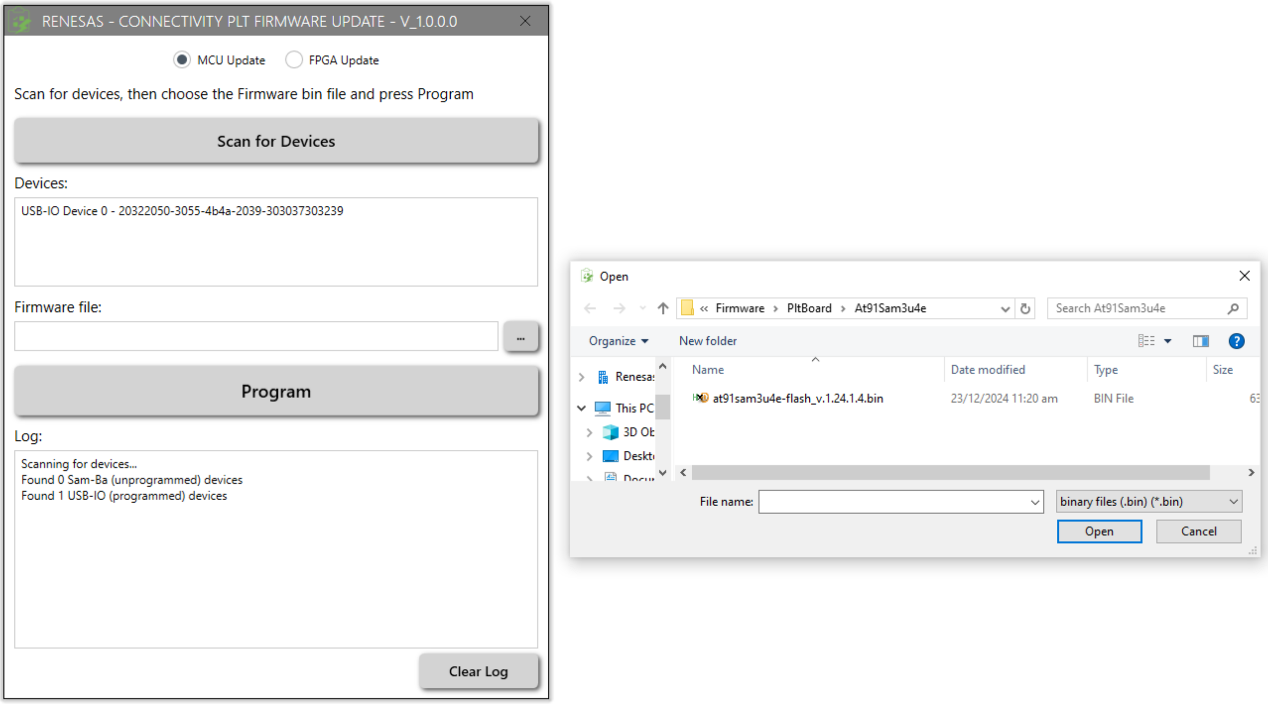
Firmware file:

Log:

```
Scanning for devices...
Found 0 Sam-Ba (unprogrammed) devices
Found 1 USB-IO (programmed) devices
```

Figure 132. Device detection

3. Next specify the **Firmware file**, click the browse button (three dots), and select the appropriate file to flash, see Figure 133.



RENESAS - CONNECTIVITY PLT FIRMWARE UPDATE - V_1.0.0.0

● MCU Update ○ FPGA Update

Scan for devices, then choose the Firmware bin file and press Program

Devices:

USB-IO Device 0 - 20322050-3055-4b4a-2039-303037303239

Firmware file:

Log:

```
Scanning for devices...
Found 0 Sam-Ba (unprogrammed) devices
Found 1 USB-IO (programmed) devices
```

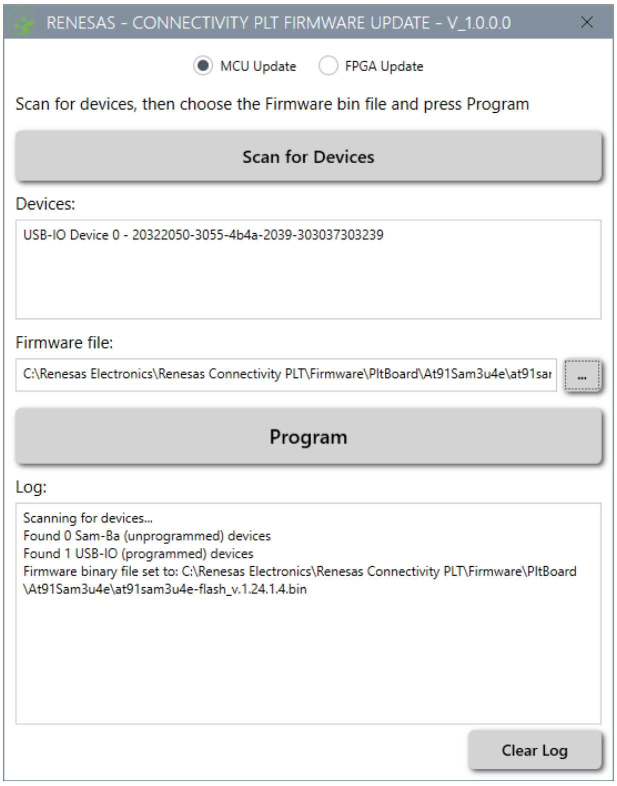
Name	Date modified	Type	Size
at91sam3u4e-flash_v.1.24.1.4.bin	23/12/2024 11:20 am	BIN File	63

File name:

binary files (.bin) (*.bin)

Figure 133. Firmware update file browse

4. Click **Program**. See Figure 134 and Figure 135.



● MCU Update ○ FPGA Update

Scan for devices, then choose the Firmware bin file and press Program

Devices:

USB-IO Device 0 - 20322050-3055-4b4a-2039-303037303239

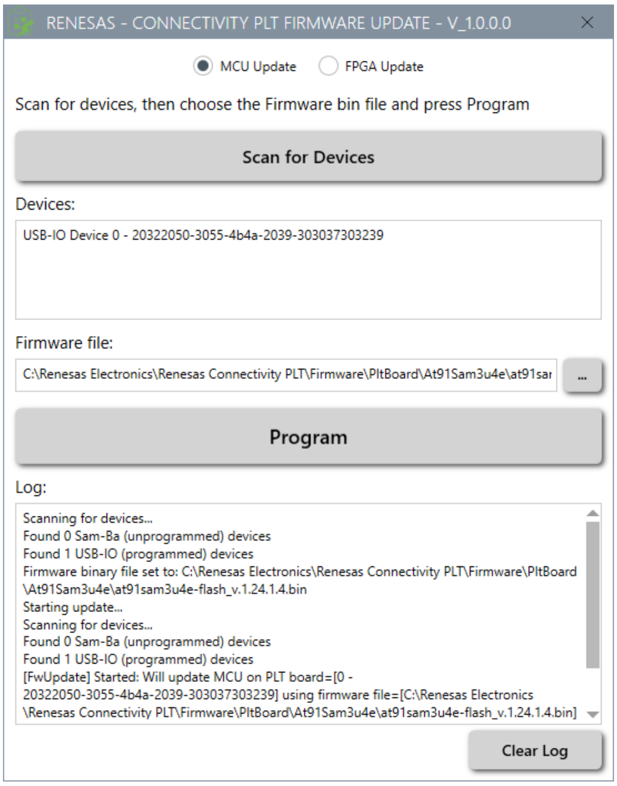
Firmware file:

C:\Renesas Electronics\Renesas Connectivity PLT\Firmware\PltBoard\At91Sam3u4e\at91sar

Log:

```
Scanning for devices...
Found 0 Sam-Ba (unprogrammed) devices
Found 1 USB-IO (programmed) devices
Firmware binary file set to: C:\Renesas Electronics\Renesas Connectivity PLT\Firmware\PltBoard
\At91Sam3u4e\at91sam3u4e-flash_v.1.24.1.4.bin
```

Figure 134. Firmware update - .bin file loading



● MCU Update ○ FPGA Update

Scan for devices, then choose the Firmware bin file and press Program

Devices:

USB-IO Device 0 - 20322050-3055-4b4a-2039-303037303239

Firmware file:

C:\Renesas Electronics\Renesas Connectivity PLT\Firmware\PltBoard\At91Sam3u4e\at91sar

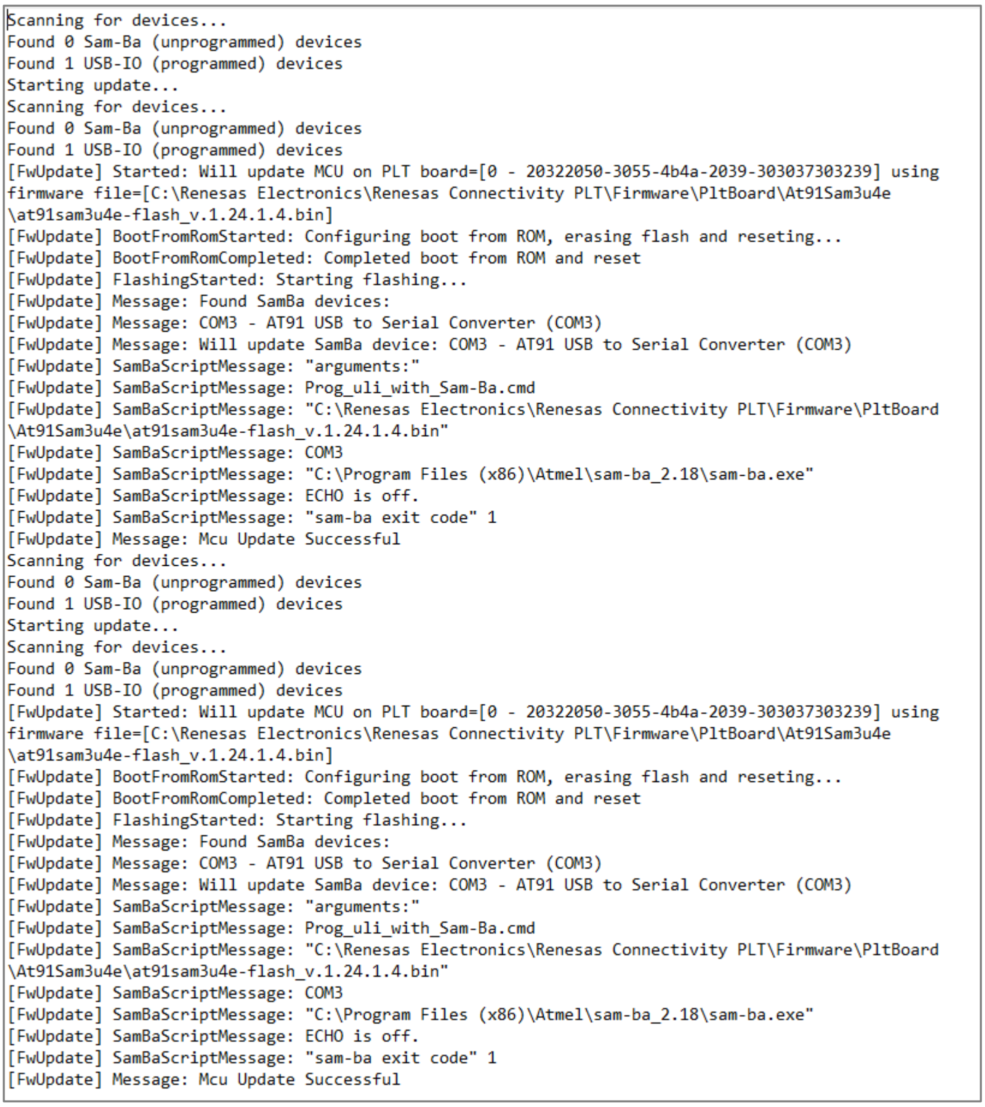
Log:

```
Scanning for devices...
Found 0 Sam-Ba (unprogrammed) devices
Found 1 USB-IO (programmed) devices
Firmware binary file set to: C:\Renesas Electronics\Renesas Connectivity PLT\Firmware\PltBoard
\At91Sam3u4e\at91sam3u4e-flash_v.1.24.1.4.bin
Starting update...
Scanning for devices...
Found 0 Sam-Ba (unprogrammed) devices
Found 1 USB-IO (programmed) devices
[FwUpdate] Started: Will update MCU on PLT board=[0 -
20322050-3055-4b4a-2039-303037303239] using firmware file=[C:\Renesas Electronics
\Renesas Connectivity PLT\Firmware\PltBoard\At91Sam3u4e\at91sam3u4e-flash_v.1.24.1.4.bin]
```

Figure 135. Firmware update - Programing

5. Check the log for errors.

Figure 136 shows the example log.



```
Scanning for devices...
Found 0 Sam-Ba (unprogrammed) devices
Found 1 USB-IO (programmed) devices
Starting update...
Scanning for devices...
Found 0 Sam-Ba (unprogrammed) devices
Found 1 USB-IO (programmed) devices
[FwUpdate] Started: Will update MCU on PLT board=[0 - 20322050-3055-4b4a-2039-303037303239] using
firmware file=[C:\Renesas Electronics\Renesas Connectivity PLT\Firmware\PltBoard\At91Sam3u4e
\at91sam3u4e-flash_v.1.24.1.4.bin]
[FwUpdate] BootFromRomStarted: Configuring boot from ROM, erasing flash and reseting...
[FwUpdate] BootFromRomCompleted: Completed boot from ROM and reset
[FwUpdate] FlashingStarted: Starting flashing...
[FwUpdate] Message: Found SamBa devices:
[FwUpdate] Message: COM3 - AT91 USB to Serial Converter (COM3)
[FwUpdate] Message: Will update SamBa device: COM3 - AT91 USB to Serial Converter (COM3)
[FwUpdate] SamBaScriptMessage: "arguments:"
[FwUpdate] SamBaScriptMessage: Prog_uli_with_Sam-Ba.cmd
[FwUpdate] SamBaScriptMessage: "C:\Renesas Electronics\Renesas Connectivity PLT\Firmware\PltBoard
\At91Sam3u4e\at91sam3u4e-flash_v.1.24.1.4.bin"
[FwUpdate] SamBaScriptMessage: COM3
[FwUpdate] SamBaScriptMessage: "C:\Program Files (x86)\Atmel\sam-ba_2.18\sam-ba.exe"
[FwUpdate] SamBaScriptMessage: ECHO is off.
[FwUpdate] SamBaScriptMessage: "sam-ba exit code" 1
[FwUpdate] Message: Mcu Update Successful
Scanning for devices...
Found 0 Sam-Ba (unprogrammed) devices
Found 1 USB-IO (programmed) devices
Starting update...
Scanning for devices...
Found 0 Sam-Ba (unprogrammed) devices
Found 1 USB-IO (programmed) devices
[FwUpdate] Started: Will update MCU on PLT board=[0 - 20322050-3055-4b4a-2039-303037303239] using
firmware file=[C:\Renesas Electronics\Renesas Connectivity PLT\Firmware\PltBoard\At91Sam3u4e
\at91sam3u4e-flash_v.1.24.1.4.bin]
[FwUpdate] BootFromRomStarted: Configuring boot from ROM, erasing flash and reseting...
[FwUpdate] BootFromRomCompleted: Completed boot from ROM and reset
[FwUpdate] FlashingStarted: Starting flashing...
[FwUpdate] Message: Found SamBa devices:
[FwUpdate] Message: COM3 - AT91 USB to Serial Converter (COM3)
[FwUpdate] Message: Will update SamBa device: COM3 - AT91 USB to Serial Converter (COM3)
[FwUpdate] SamBaScriptMessage: "arguments:"
[FwUpdate] SamBaScriptMessage: Prog_uli_with_Sam-Ba.cmd
[FwUpdate] SamBaScriptMessage: "C:\Renesas Electronics\Renesas Connectivity PLT\Firmware\PltBoard
\At91Sam3u4e\at91sam3u4e-flash_v.1.24.1.4.bin"
[FwUpdate] SamBaScriptMessage: COM3
[FwUpdate] SamBaScriptMessage: "C:\Program Files (x86)\Atmel\sam-ba_2.18\sam-ba.exe"
[FwUpdate] SamBaScriptMessage: ECHO is off.
[FwUpdate] SamBaScriptMessage: "sam-ba exit code" 1
[FwUpdate] Message: Mcu Update Successful
```

Figure 136. Example for firmware update log

13.2 FPGA Update

To update FPGA, follow the same steps as for the MCU update but instead select **FPGA Update** and the appropriate .bin file.

Appendix A Conformity Assessment

Connectivity PLT conforms to laws and regulations that are described in the following subsections.

A.1 FCC Notice (Applicable to Evaluation Kits not FCC-Approved)

This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

A.2 CE – UKCA (Europe-UK)

The Connectivity PLT is tested and found to comply with **EMC Directive (2014/30/EU)** for electromagnetic compatibility. Applicable standards are the following:

- **EN 55032 (2015)/AC (2016)/A11 (2020) & EN 55035 (2017)/A11 (2020).**

Simplified Declaration of Conformity
Hereby, Renesas Design Netherlands B.V. declares that The Connectivity PLT is in compliance with **EMC Directive (2014/30/EU)**. The full texts of the EU declaration of conformity are available at the following internet address: www.renesas.com

A.3 WEEE Directive (2012/19/EU)

The Waste Electrical and Electronic Equipment Regulations 2013

For customers in the UK and European Union

The WEEE (Waste Electrical and Electronic Equipment)

regulations put responsibilities on producers for the collection and recycling or disposal of electrical and electronic waste. Return of WEEE under these regulations is applicable in the UK and European Union.

This equipment (including all accessories) is not intended for household use. After use, the equipment cannot be disposed of as household waste, and the WEEE must be treated, recycled, and disposed of in an environmentally sound manner.

Renesas Electronics Europe GmbH can take back the end of line equipment. Register for this service at https://www.renesas.com/eu/en/support/regional-customer-support/weee.

A.4 RoHS Compliance

Renesas Electronics' suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

Table 59. Product standards

Revision	Description
ELOT EN 55032 E2:2015 +A11:2020	Electromagnetic compatibility of multimedia equipment - Emission Requirements
ELOT EN 55035 E1:2017 +A11:2020	Electromagnetic compatibility of multimedia equipment - Immunity Requirements

Table 60. Test standards

Revision	Description
ELOT EN 61000-4-2 E2:2009	Electromagnetic compatibility (EMC) -- Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test
ELOT EN IEC 61000-4-3 E4:2020	Electromagnetic compatibility (EMC) -- Part 4-3: Testing and measurement techniques - Radiated, radio-frequency, electromagnetic field immunity test
ELOT EN 61000-4-8 E2:2010	Electromagnetic compatibility (EMC) -- Part 4-8: Testing and measurement techniques - Power frequency magnetic field immunity test

14. Revision History

Revision	Date	Description
01.03	Nov 20, 2025	Added section about RFTUs. Added figures for Bluetooth LE and Wi-Fi testing unit setup. Updated section Connectivity PLT Configuration with new information.
01.02	Sept 12, 2025	Fixed J11 pinout.
01.01	Aug 14, 2025	Added Compliance information (Appendix A).
01.00	June 3, 2025	First version.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

ROHS Compliance

Renesas Electronics' suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

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