User's Manual

RZ/G1H

User's Manual: Hardware

for Rich Graphics Applications
RZ/G Series

ARM®

Specifications of Individual RZ/G Series Product

Renesas Electronics
www.renesas.com

Rev.1.00 Sep 2016

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
3. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from such alteration, modification, copy or otherwise misappropriation of Renesas Electronics product.
5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The recommended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.

   “Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots etc.

   “High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; and safety equipment etc.

   Renesas Electronics products are neither intended nor authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems, surgical implantations etc.), or may cause serious property damages (nuclear reactor control systems, military equipment etc.). You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application for which it is not intended. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for which the product is not intended by Renesas Electronics.
6. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You should not use Renesas Electronics products or technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. When exporting the Renesas Electronics products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the contents and conditions set forth in this document, Renesas Electronics assumes no responsibility for any losses incurred by you or third parties as a result of unauthorized use of Renesas Electronics products.
11. This document may not be reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(2012.4)

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of hardware, pin assignments, pin multiplexing, and pin function controller.

For the rest of the sections on other on-chip peripheral functions, see the RZ/G Series User's Manual: Hardware.

> Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

> The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

We provide the following three types of user's manual for RZ/G series products.

Make sure to refer to the latest versions of these documents.

Document Type	Description	Document Title	Document No.
User's manual for specifications of individual RZ/G series product	Overview of hardware, pin assignments, pin multiplexing, and pin function controller	RZ/G1H User's Manual: Hardware	R01UH0627EJ0100 Rev.1.00 (This user's manual)
User's manual for specifications common to RZ/G series products	Hardware specifications (address map, general-purpose I/O port pins, clock, reset, core functions, graphics, video processing, sound processing, and network modules, serial interfaces, storage, timers, other on-chip peripheral functions, testing, and debugging) and descriptions of operation	RZ/G Series User's Manual: Hardware	R01UH0543EJ0100 Rev.1.00
User's manual for electrical characteristics	Electrical characteristics of the RZ/G series products	Provided as separate technical information.	

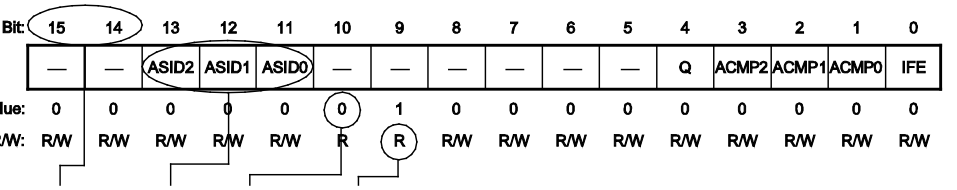
2. Notation of Numbers and Symbols

Bit notation:	Bits are shown in high-to-low order from left to right.
Number notation:	Binary numbers are given as B'XXXX, hexadecimal numbers are given as H'XXXX, and decimal numbers are given as XXXX.
Signal notation:	A number sign (#) after the name indicates that a signal or pin is active-low, unless otherwise specified. Example: PRESET#

3. Register Notation

Each register description includes a bit chart, illustrating the arrangement of bits, and a table of bits, describing the meanings of the bit settings.

[Bit Chart]



[Table of Bits]

(1) (2) (3) (4) (5)

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved
14	—	0	R	These bits are always read as 0.
13 to 11	ASID2 to ASID0	All 0	R/W	Address Identifier These bits enable or disable the pin function.
10	—	0	R	Reserved This bit is always read as 0.
9	—	1	R	Reserved This bit is always read as 1.
	—	0		

Note: The bit names and sentences in the above figure are examples, and have nothing to do with the contents of this manual.

(1) Bit
Indicates the bit number or numbers.
In the case of a 32-bit register, the bits are arranged in order from 31 to 0. In the case of a 16-bit register, the bits are arranged in order from 15 to 0.

(2) Bit name
Indicates the name of the bit or bit field.
When the number of bits has to be clearly indicated in the field, appropriate notation is included (e.g., ASID[3:0]).
A reserved bit is indicated by "–".
Certain kinds of bits, such as those of timer counters, are not assigned bit names. In such cases, the entry under Bit Name is blank.

(3) Initial value
Indicates the value of each bit immediately after a power-on reset, i.e., the initial value.
0: The initial value is 0.
1: The initial value is 1.
–: The initial value is undefined

(4) R/W
For each bit and bit field, this entry indicates whether the bit or field is readable or writable, or both writing to and reading from the bit or field are impossible.
The notation is as follows:

R/W: The bit or field is readable and writable.
R/(W): The bit or field is readable and writable.
However, writing is only performed to flag clearing.
R/WC0: The bit or field is readable and writable. Writing 0 to the bit initializes the bit.
Writing 1 to the bit is ignored.
R/WC1: The bit or field is readable and writable. Writing 1 to the bit initializes the bit.
Writing 0 to the bit is ignored.
R: The bit or field is readable.
"R" is indicated for all reserved bits. When writing to the register, write the value under Initial Value in the bit chart to reserved bits or fields.
W: The bit or field is writable.
Note that values read from write-only bits are not guaranteed, unless they are specified in the chart of bits.

(5) Description
Describes the function of the bit or field and specifies the values for writing.

Contents

1. Overview

1.1 Introduction

The RZ/G1H is that features the basic functions for Rich Graphics Applications.

The RZ/G1H includes:

- Four 1.4-GHz ARM Cortex®-A15 MPCore® cores,
- Four 780-MHz ARM Cortex®-A7 MPCore® cores,
- Memory controller for DDR3-SDRAM (DDR3-1600) with 32 bits × two channels,
- Two- and three-dimensional graphics engines,
- Video processing units,
- 3 channels Display Output,
- 4 channels Video Input,
- Sound processing units,,
- SD card host interface,
- USB3.0 and USB2.0 interfaces,
- PCI Express interface,
- Serial ATA interface, and
- CAN interface.

Also, a full implementation of the extremely expandable and Internal AXI bus has been adopted for the RZ/G1H.

This bus structure is optimized for maximum system performance, leading to the realization of high-performance and cost-effective premium in-vehicle infotainment systems.

Notes: 1. ARM is a registered trademark and Cortex is a trademark of ARM Limited. All other brands or product names are the property of their respective holders.

1.2 System Configuration Diagram

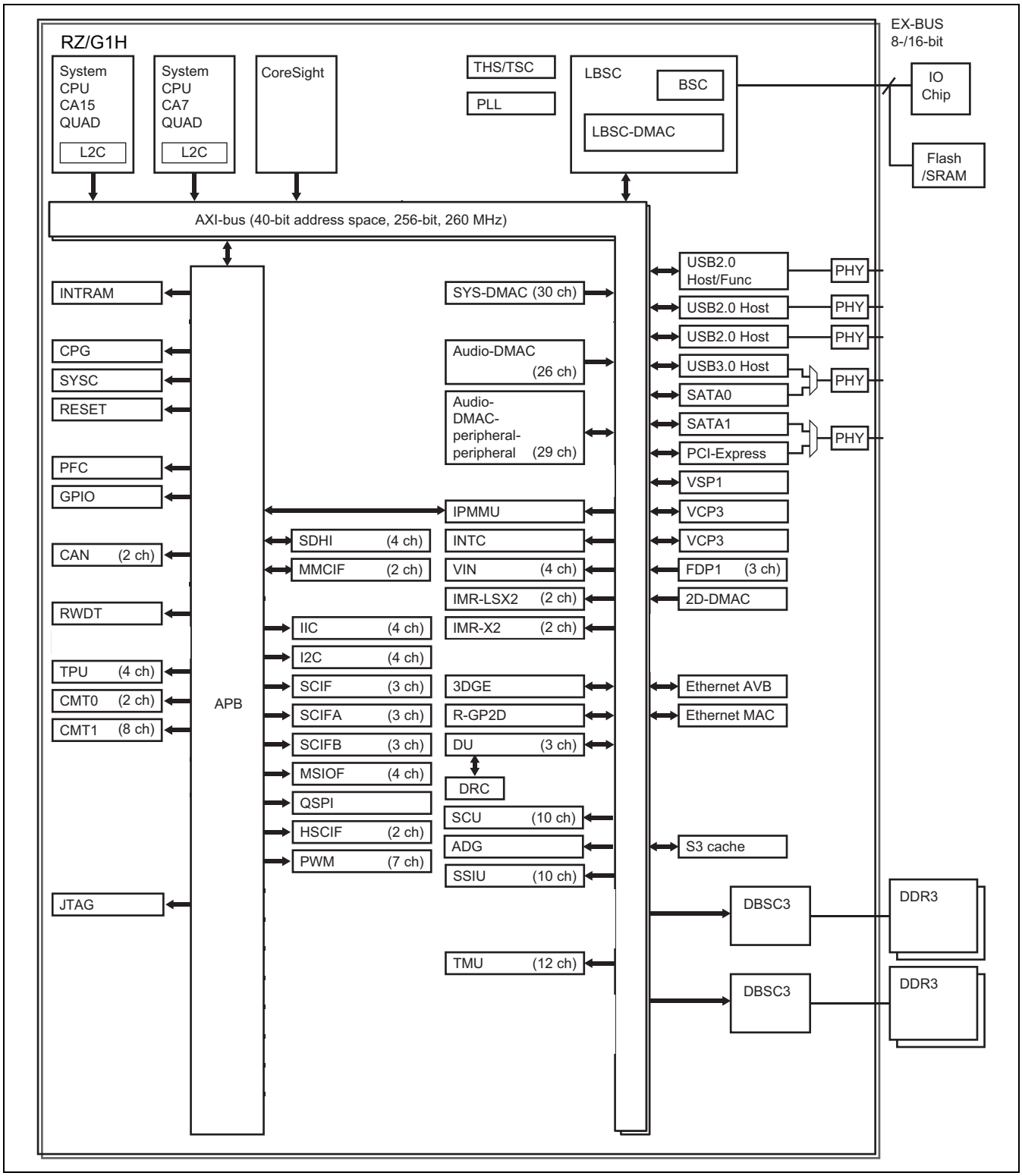


Figure 1.1 RZ/G1H System Configuration

1.3 List of Specifications

1.3.1 ARM Core

Item	Description
System CPU Cortex-A15	• ARM Cortex-A15 Quad MPCore 1.4 GHz • L1 I/D cache 32/32 KBytes, L2 cache 2 MBytes • NEON™/VFPv4 supported • Security extension supported
System CPU Cortex-A7	• ARM Cortex-A7 Quad MPCore 780 MHz • L1 I/D cache 32/32 KBytes, L2 cache 512 KBytes • NEON™/VFPv4 supported • Security extension supported
ARM debugger (CoreSight)	• CoreSight system compliant • JTAG/SWD I/F supported • CoreSight PTM-A15/A7 supported (each CPU) • CoreSight ETR 16 Kbytes for program flow trace • CoreSight ETR 4 Kbytes for system trace

1.3.2 CPU Core Peripherals

Item	Description
Operating clock pulse generation circuit (CPG)	• Generates the clocks from external clock (EXTAL1). — Maximum Cortex-A15 clock: 1.4 GHz — Maximum Cortex-A7 clock: 780 MHz — Maximum AXI-bus clock: 260 MHz — Maximum SDRAM bus clock: 800 MHz (DDR3-1600), 666 MHz (DDR3-1333) — Maximum media clock: 260 MHz — Maximum peripheral clock (HPϕ): 130 MHz • System-CPU shut down mode control supported • Module-standby mode supported • Includes module reset registers to control reset operation of individual on-chip peripheral modules
System controller (SYSC)	• Shuts down and restores power to target modules. Target modules: — Cortex-A15 (with independent shutting down of CPUs 0, 1, 2, 3, and SCU + L2 cache)* — Cortex-A7 (with independent shutting down of CPUs 0, 1, 2, 3, and SCU + L2 cache)* — 3DGE Note: * SCU and L2 cache are treated as one power-domain. When CPU is working, SCU + L2 cache can't be powered off.
Reset (RST)	• Includes one reset-signal external output port for external modules • Includes boot address register etc.
Pin function controller (PFC)	• Setting multiplexed pin functions for LSI pins Function of the RZ/G1H pin selectable by setting the registers in the PFC module. • Module selection Enable and disable the functions of RZ/G1H LSI pins to which pin functions from multiple pin groups are assigned by setting the registers in the PFC module. • Pull-up control for each LSI pin On/off of the pull-up resistor on each LSI pin can be controlled by setting the registers in the PFC module. • Control of SDIO functions SDIO functions, including the driving ability of pins for the SDIF, can be controlled by setting registers of the PFC.
General-purpose I/O (GPIO)	• General-purpose I/O ports: 188 ports • Supports GPIO interrupts.
Thermal sensor (THS/TSC)	• Single channel of thermal sensor • Programmable 4 temperature level for the sensor, to indicate the temperature level • Selectable operation (Interrupt/Reset) when the temperature reaches programmed

1.3.3 External Bus Module

Item	Description
Local bus state controller (LBSC)	• EX-BUS interface: max. 16-bit bus • Frequency: 65 MHz or 43.3 MHz • External area divided into several areas and managed — Allocation to space of area 0, area 1, and area 6 or allocation to space of area 0 only is selected at startup time. — Area 0 supports 128-Mbyte memory space (startup mode). — Space of area 6 is divided into up to six areas (capacity of each area variable) and managed — I/F settings, bus width settings, and wait state insertion are possible for each area • SRAM interface — Wait states can be inserted through register settings — Period of waiting is set in cycle unit, and the maximum value is 15. — EX_WAIT pin can be used for wait state insertion — Connectable bus widths: 16 bits or 8 bits • Burst ROM interface — Wait states can be inserted through register settings — Number of bursts can be set through register settings — Connectable bus widths: 16 bits or 8 bits • Byte-control SRAM interface (available with areas 1 and 6 only) — Byte-control SRAM interface — Wait states can be inserted through register settings — EX_WAIT pin can be used for wait state insertion — Connectable bus widths: 16 bits or 8 bits • ATA interface (two ports) — Wait states can be inserted through register settings — Supports PIO modes 0 through 4 — Supports multi-word modes 0 through 2 — Supports Ultra DMA modes 0 through 4 (Ultra ATA66) — Ready timeout detection (detection time (ns) = EX-BUS operating frequency (ns) × 100 clock cycles) • Supports external buffer enable/direction control

Item	Description
LBSC-DMAC	• Three channels • Address space: Physical address space • Transfer direction: Peripheral to memory (AXI-bus), memory (AXI-bus) to peripheral • Data packing for peripheral read data: Memory write data length is selectable as transfer data length to memory side. • Transfer data length: Peripheral (APB-bus) side: 1, 2, 4 bytes Memory (AXI-bus) side: 4 or 16 (channel 2), 32 (channel 0 and 1) bytes • Transfer burst length: 1, 8 (transfer with a burst length of 8 supported only for LBSCDMAC00, 01) • Number of transfers — Maximum number of transfers: 16 M (16,777,216 transfers), 64M (67,108,864 transfers), (64 M transfers supported only for LBSC-DMAC00) — Minimum number of transfers: 1 • Address mode: Dual address mode • Transfer modes: Single transfer mode, continuous transfer mode • Transfer end interrupt: Occurs at the end of the number of transfers specified in the register
External bus controller for DDR3-SDRAM (DBSC3)	• Two channels (32-bit bus mode) or single channel (64-bit bus mode) • DDR3-SDRAM can be connected directly. • Memory Size: Up to 8 Gbytes (8-Gbit memory × 8) • Data bus width: 32 bits × 2 or 64 bits × 1 • Auto-refresh/self-refresh/partial array self-refresh supported • Deep-power-down mode supported • Auto precharge mode/bank active mode • DDR back up supported
Memory connections	DDR3-SDRAM compliant to JEDEC JESD79-3E Supports from 512-Mbit to 8-Gbit memory unit configurations 32-bit DDR3-1600 (four units with 8-bit width)

1.3.4 Internal Bus Module

Item	Description
AXI-bus	• On-chip main bus — Bus protocol : AXI3 with QoS control — Frequency: 260 MHz — Bus width: 256 bits/128 bits • On-chip CPU & GPU main bus — Corelink™ CCI-400 Cache Coherent Interconnect - r0p3 — Bus protocol: AMBA®4 ACE™ and ACE-Lite™ — Frequency: 520 MHz — Bus width: 128 bits

Item	Description
S3 cache (S3CTRL)	• 2 MBytes cache memory for system
Direct memory access controller for system (SYS-DMAC)	• 30 channels for ARM domain • Address space: 4 Gbytes on architecture • Data transfer length: Byte, word (2 bytes), longword (4 bytes), 8 bytes, 16 bytes, 32 bytes, and 64 bytes • Maximum number of transfer times: 16,777,216 • Transfer request: Selectable from on-chip peripheral module request and auto request • Bus mode: Selectable from normal mode and slow mode • Priority: Selectable from fixed channel priority mode and round-robin mode • Interrupt request: Supports interrupt request to CPU at the end of data transfer • Repeat function: Automatically resets the transfer source, destination, and count at the end of DMA transfer (by descriptor function) • Descriptor function (each channel) supported • MMU (each channel) supported • Channel bandwidth arbiter (each channel)
Direct memory access controller for Audio (Audio-DMAC)	• 26 channels for Audio domain • Address space: 4 Gbytes on architecture • Data transfer length: Byte, word (2 bytes), longword (4 bytes), 8 bytes, 16 bytes, 32 bytes, and 64 bytes • Maximum number of transfer times: 16,777,216 • Transfer request: Selectable from on-chip peripheral module request and auto request • Bus mode: Selectable from normal mode and slow mode • Priority: Selectable from fixed channel priority mode and round-robin mode • Interrupt request: Supports interrupt request to CPU at the end of data transfer • Repeat function: Automatically resets the transfer source, destination, and count at the end of DMA transfer (by descriptor function) • Descriptor function (each channel) supported • MMU (each channel) supported • Channel bandwidth arbiter (each channel)
Direct memory access controller (Audio-DMAC-Peripheral-Peripheral)	Audio-DMAC (for transfer from Peripheral to Peripheral) • 29 channels for audio domain • Data transfer length: longword (4 bytes) • Transfer count: Transfer count is not specified (DMA transfer is made from the transfer-start to transfer-stop settings.) • Transfer request: Selectable from on-chip audio peripheral module request • Priority: round-robin mode • Interrupt request: not supports interrupt request to CPU at the end of data transfer
IPMMU	An IPMMU is a memory management unit (MMU) which provides address translation and access protection functionalities to processing units and interconnect networks.

Item	Description	
Interrupt controller (INTC)	INTC-SYS	— Four interrupt pins which can detect external interrupts — Fall/rise/high level/low level detection is selectable — On-chip peripheral interrupts: Priority can be specified for each module — Max. 384 shared peripheral interrupts supported — 16 software interrupts that have been generated and 6 private peripheral interrupts supported — 32-level priority selectable — Trust Zone supported

1.3.5 Local Memory

Item	Description
INTRAM	• RAM0 of 72 Kbytes • RAM1 of 4 Kbytes • RAM2 of 256 Kbytes

1.3.6 Graphics Units

Item	Description
3D graphics engine (3DGE)	• Imagination Technologies PowerVR Series6 G6400 • Max. Freq. 520 MHz • Most comprehensive IP core family and roadmap in the industry • Universal Scalable Shader Engine (USSE) • Programmable architecture • Latency tolerant architecture • Internal True Color • Support APIs: OGLES2.0, Halti, (Dx10), (OpenCL 1.1e)

Item	Description	
Graphics engine basic functions (R-GP2D)（option）	Maximum operating clock frequency	AXI: 260 MHz APB: 65 MHz
	Drawing functions	Four-vertex surface drawing, polygon drawing, line drawing, highly-functional thick line drawing, anti-aliasing, BitBLT with raster operations/α blending, α blended lines
	Coordinate transformation functions	4 × 4 matrix operations + perspective W-division performed
	Color display	8-bit index, RGB565, ARGB1555, ARGB8888
	Screen coordinates	• X direction: 0 to 4095 • Y direction: 0 to 4095
	Register settings	• Current point setting [MOVE/RMOVE] • Local offset setting [LCOFS/RLCOFS] • Specific address mapped register setting [WPR] • Local coordinates conversion offset setting [RGTOFS]
	Sequence control	• Vsync wait [VBKEM] • Jump [JUMP] • Subroutine [GOSUB] (nesting level: 1, 8)
	Anti-aliased fonts	8 bits/pixel color format, anti-aliased font drawing
	Multiple source blending with α map reference values	Supports 8 bits/pixel color format α maps
	Thick line customizing	Borders at which thickness direction is switched can be set [BDS], jaggy reduction [WLM]
	New anti-aliased line	Anti-aliasing for vertical, horizontal and 45-degree oblique lines is possible. [NAA]
	Loop function	Draws a closed figure by connecting the start and end points. [LOOP]

Item	Description	
Display unit (DU)	Display channel	Three independently controllable channels
	Interface	• LVDS output: Four lanes × two channels (One of channels (two lanes × 2)) • Digital RGB : Single channel (8-bit precision for each RGB color)
	LVDS interface (2 ch)	• Output: compliant with TIA/EIA-644; five pairs of differential output (four pairs of data and one pair of clock) • Operating frequency: Dotclk 148.5 MHz • Selectable eight output formats
	Screen size and number of composite planes	• Maximum screen size: 4095 × 2047 • Number of planes specifiable: 8 Note that possibility number of combined display depends on DCLK; 1-plane @DCLK > 75 MHz 2-plane @75 MHz ≥ DCLK > 38 MHz 3-plane @38 MHz ≥ DCLK Note: The above applies to RGB non-multiplexed output. • For DU0 and DU1: Maximum number of planes: 8 (When two output systems are used, a total of up to eight planes may be used.) Maximum number of 'α' planes: 2 (When two output systems are used, a total of up to two planes may be used.) • For DU2: Maximum number of planes: 8 Maximum number of 'α' planes: 2
	CRT scanning method	Non-interlaced, interlaced sync, interlaced sync & video
	Synchronization method	Master, TV sync
	Internal color palette	Includes four color palette planes which can display 256 of 260 thousands colors at the same time.
	Digital RGB	• Three output channel • Output on rising and falling edges of the synchronizing signal (resolution for the same display) • 8-bit precision for each RGB color
	Blending ratio settings	Number of color palette planes with blending ratio: 4
	Dot clock	Switchable between external input and internal clock
	Color management	• γ correction, gain correction • Applies correction of color (skin color adjustment and color correction set in memory) in terms of color phase, brightness, and chromaticity for a specified range of colors or for the full range of colors

Item	Description	
Dynamic range compression (DRC)	• Single channel • Contrast correction • Optimal contrast extension processing for every domain of a picture. • A higher contrast expansion effect can be acquired compared with the system which controls the whole screen uniformly.	
Video input (VIN)	Input interface	• Four channels (RGB/YCbCr: (channel 0,1,2), YCbCr only: (channel 3)) • ITU-R BT.601 interface: 8-, 10- (same size only (not scaling)), or 12-bit (same size only (not scaling)) YCbCr422, RGB666, 24-bit RGB888, and 12-bit RGB888 • ITU-R BT.656 interface: 8-, 10- (same size only (not scaling)), or 12-bit (same size only (not scaling)) YCbCr422 • ITU-R BT.1358 interface: 16-, 20- (same size only (not scaling)), or 24-bit (same size only (not scaling)) • YCbCr422 • ITU-R BT.709 interface: RGB666, 24-bit RGB888, and 12-bit RGB888,YCbCr422
	Input data format	• 8-, 10-, or 12-bit YCbCr422 (CbYCrY format) • 8-bit YCbCr422 (4 bits (Cb)/4 bits (Y)/4 bits (Cr)/4 bits (Y) format) (double edge clock transfer mode) • 16-bit YCbCr422 (8 bits (Y) + 8 bits (CbCr) format) • 16-bit YCbCr422 (8 bits (Y)/8 bits (CbCr) format) (double edge clock transfer mode) • 20-bit YCbCr422 (10 bits (Y) + 10 bits (CbCr) format) • 24-bit YCbCr422 (12 bits (Y) + 12 bits (CbCr) format) • 18-bit RGB666 • 24-bit RGB888 • 12-bit RGB888 (double edge clock transfer mode)
	Clipping function	Up to 2048 × 2048
	Horizontal scaling	Uses a 9-tap multi-phase filter. Up to two times, but only scaling down is possible for HD1080i or HD720P data.
	Vertical scaling	Scaling by linear interpolation Up to three times, but only scaling down is possible for HD1080i or HD720P data.
	Output format	RGB-565, ARGB-1555, YCbCr422, RGB888 (for channels 0, 1, and 2), YC separation, and extraction of the Y component
IMR-LX2（option）	• Two channels • Pixel pipelines internally operate at the 260-MHz clock frequency (pixels are generated and distortion is corrected at one pixel per cycle). • Reads data from the external memory or from the path directly connected to VIN and outputs data in which distortion was corrected to the external memory. • Access to the AXI-Bus is at the 260-MHz clock frequency. • Includes a dedicated destination cache (8 KBytes) and line memory (1280 pixels × 8). • Image data format: 16 bpp (YCbCr422 (Y: 8 bpp, 10 bpp, CbCr: 8 bpp))	

Item	Description
IMR-X2（option）	• Two channels • Pixel pipelines internally operate at the 260-MHz clock frequency (pixels are generated and distortion is corrected at one pixel per two cycles). • Reads data from the external memory, corrects distortion in the data, then outputs the corrected data to the external memory. • Access to the AXI-Bus is at the 260-MHz clock frequency. • Includes a dedicated destination cache (2 KBytes) and source cache (4 KBytes). • Image data format: YCbCr 422, YCbCr 420 (Y: 8 bpp, 10 bpp, CbCr: 8 bpp), ARGB1555, RGB565 (16 bpp)

1.3.7 Video Processing

Item	Description
Video signal processor 1 (VSP1)	The VSP1 is the successor IP of Renesas' VIO6-IP series, and has the following features. (1) Supports various data formats and conversion — Supports YCbCr444/422/420, RGB, αRGB, αplane — Color space conversion and changes to the number of colors by dithering — Color keying (2) Full HD video processing — Up and down scaling with arbitrary scaling ratio — Super resolution processing — Blending of four picture layers and raster operations (ROPs) (3) Full HD picture quality/color correction with 1D/3D look up table (LUT) — Dynamic γ correction and gain correction — Correction of color (to adjust skin tones or colors in memory) — Hue, brightness, and saturation adjustment — 1D and 2D histogram (4) Direct connection to display module — Display unit (DU) supported
Video processing unit (VCP3)	The VCP3 is a multi-codec module which provides encoding and decoding capabilities on the basis of multiple video coding schemes, e.g., H.264/AVC, MPEG-4, MPEG-2 and VC-1. This IP (Intellectual Property) is a multi codec that processes the frame or each field by controlling software for VCP3 executed on host CPU. The VCP3 has the following features: • Two channels • Support for multiple codecs — H.264/MPEG-4 AVC HP (High Profile) and MVC SHP (Stereo High Profile) encoding and decoding — H.262/MPEG-2 MP (Main Profile) decoding — MPEG-4 ASP (Advanced Simple Profile) decoding — VC-1 SP/MP/AP (Simple, Main, Advanced Profile) decoding — H.263 Baseline decoding — VP8 decoding • Support for HDTV resolutions — 1920 pixels × 1080 lines × 60 frames/second × two channels — Maximum performance will change with securable bus bandwidth. • Data handling on a picture-by-picture basis — Encodes/decodes data one picture (frame or field) at a time. • High picture quality — Supports the H.264 high-efficiency coding tools (CABAC, 8 × 8 frequency conversion, and quantization matrix). — High-efficiency motion vector detection by a combination of discrete search and trace search — Highly efficient real-time intra-prediction by Prediction from Original Image (POI) — Optimal-mode selection by Rate-Distortion (RD) cost evaluation — Picture quality control based on activity analysis results which match visual models • Low power dissipation — Dynamically disables the clocks for the entire VCP3. — Dynamically disables the clocks for individual submodules. • Includes its own dedicated 64-KByte cache

Item	Description
Fine display processor 1 (FDP1)	The FDP1 is the de-interlacing module which converts the interlaced video to progressive video, and has the following features. (1) Supports three channels (2) Supports various data formats — Input: YCbCr444/422/420 — Output: YCbCr444/422/420 and RGB/αRGB (3) Full HD video processing performance (4) High image quality de-interlacing algorithm — Motion adaptive de-interlacing — Accurate still detection — Diagonal line interpolation (DLI)
Image extraction direct memory access controller (2D-DMAC)	• Eight channels • Supports conversion between various RGB formats. • Image extraction function: Capable of extracting an image and storing it as a separate image in the RAM. • Image rotation/reversal function: Reverses an image vertically/horizontally or rotates it by 90°/270°. • Simple scaling function: Capable of scaling an image two times in the X or Y direction. • Format conversion • Supports conversion from RGB to RGB and from YCbCr to YCbCr.

1.3.8 Sound Interface

Item	Description	
Sampling rate converter unit (SCU)	Overall specification	• Includes ten SRC modules — Supports the quality suitable for audio sound (THD+N -132dB): six modules — Supports the quality suitable for voice sound (THD+N -96dB): four modules • The SRC module is capable of correcting phase change and delay (timing jitter) generated during data transfer over external memories or external devices. • The channel count conversion unit (CTU), mixer (MIX), and digital mute and volume function (DVC) can be used on two fixed output channels.
	Sampling rate conversion (SRC)	• Capable of asynchronous sampling rate conversion • Supports resolutions up to 24 bits • Two kinds of filter type for SRC. — Supports the quality suitable for audio sound (THD+N -132dB): Realized the filter by passband -1dB@0.4575FS, cutoff -18dB@0.5FS. — Supports the quality suitable for voice sound (THD+N -96dB): Realized the filter by passband -1dB@0.4561FS, cutoff -72dB@0.5FS (Characteristics of each filter is written in the equivalent/up-sampling cases). • Automatically generates antialiasing filter coefficients • For monaural to eight-channel sound sources
	Channel count conversion unit (CTU)	• Downmixing and splitter functions — Conversion of eight input channels into four output channels — Conversion of six input channels into two output channels — Conversion of two input channels into four sets of two output channels — Conversion of one input channel into eight sets of one output channel — No conversion
	Mixer (MIX)	• Mixing (adds) two to four sources into one • Ratio for adding sources is selectable • Ratio is dynamically changeable • Mixing with volume ramp is available (ramp period is selectable)
	Digital volume and mute function (DVC)	• Volume control function including digital volume, volume ramp, and zero-crossing mute • The digital volume function is specified by a 24-bit fixed-point value within the range from 0 to 8 times (mute, or -120 to 18 dB) • The volume ramp function can be used for soft mute, fade-in, fade-out, or desired volume adjustment • The volume ramp period can be changed within the sampling range from the 0th to 23rd power of 2 • The zero-crossing mute function silences the sound at the zero-crossing point of the audio data

Item	Description	
Serial sound interface unit (SSIU)	Overall specification	• Includes ten SSI modules functioning as interfaces with external devices. — Supports short and long formats — Supports TDM format (six modules of ten modules can be used for this function) • Up to four independent stereo sound sources in a TDM format can be distributed to each course. Up to four independent stereo sound sources can be combined output in TDM format.
	Serial sound interface (SSI)	• 10 channels • Operating mode: non-compressed mode (Not support compressed mode) • Supports versatile serial audio formats (I2S/left justified/right justified) • Supports master/slave functions • Programmable word clock, bit clock generation functions • Multichannel format functions (up to four channels) • Supports 8-/16-/18-/20-/22-/24-/32-bit data formats • Supports TDM mode • Supports WS continue mode • The DMA controller or interrupts control the transfer of data to and from the SSI module. • Supports short and long frames for monaural data (valid data lengths are 8 and 16 bits) • Up to nine independent clock signals can be input.
Audio clock generator (ADG)	Selection or division of audio clock signals	

1.3.9 Storage

Item	Description
USB2.0 host & function module (USB2.0)	• Three channels (Host only two channel/Host-Function one channel selected)* • PHY integrated • USB Host (EHCI/OHCI) 2LINK • Compliance with USB2.0 • USB Function 1LINK • Compliance with USB2.0 (High-Speed) • Interrupt request • Internal dedicated DMA Note: * A USB2.0 PHY is used as USB3.0 host HS/FS. USB2.0: Three channels/USB2.0: Two channels + USB3.0: Single channel
USB 3.0 host module (USB3.0)	• USB 3.0 host single channel* • Supports SS/HS/FS/LS. xHCI • Not support FUNCTION and OTG Note: * A USB2.0 PHY is used as USB3.0 HOST HS/FS. USB2.0: Three channels/USB2.0: Two channels + USB3.0: Single channel
Serial-ATA	• Serial ATA Standard Rev.3.1 supported • 3.0-Gbps (Gen2) transfer rate supported — Single-channel PHY for USB3.0 and SATA (channel 0) — Single-channel PHY for PCIEC and SATA (channel 1)
SD host interface (SDHI)	• Four interfaces — Interfaces 0 and 1: Support SDR104 class transfer rate at max. 97.5 Mbytes/s@ 195 MHz, and SDXC. Does not support CPRM. — Interfaces 2 and 3: Support SDR50 class transfer rate at max. 48 Mbytes/s@ 97.5 MHz, and SDXC. Does not support CPRM. • Supports SD memory/SDIO interface (1-/4-bit SD buses). • Error check function: CRC7 (command/response), CRC16 (data) • Card detection function • Supports write protection
Multi-media card interface (MMCIF)	• Two channels • MMC 4.41 base • eMMC controllable • Data bus: 1/4/8-bit MMC mode (not support SPI mode) • Support block transfer (not support stream transfer) • Block size in multi-block transfer: 512 bytes

1.3.10 Network

Item	Description
CAN interface (CAN)	• Two interfaces • Supports CAN specification 2.0B • ISO-11898-1 compliant • Maximum bit rate: 1 Mbps • Message box — Normal mode: 32 receive-only mailboxes and 32 mailboxes for transmission/reception — FIFO mode: 32 receive-only mailboxes and 24 mailboxes for transmission/reception, 4-stage FIFO for transmission, and 4-stage FIFO for reception • Reception — Data frame and remote frame can be received. — Selectable receiving ID format — Selectable overwrite mode (message overwritten) or overrun mode (message discarded) • Acceptance filter — Mask can be enabled or disabled for each mailbox. • Transmission — Data frame and remote frame can be transmitted. — Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) — Selectable ID priority mode or mailbox number priority mode • Sleep mode for reducing power consumption
PCI-Express Controller (PCIEC)	• PCI Express Base Specification Revision 2.0 • Single channel • PHY integrated
Ethernet AVB	• Supports IEEE802.1BA, IEEE802.1AS, IEEE802.1Qav and IEEE1722 functions • Supports transfer at 1000 Mbps and 100 Mbps • Magic packet detection • Supports Reception Filtering to separate streaming frames from different sources • Supports interface conforming to IEEE802.3 PHY GMII (Gigabit Media Independent Interface) and MII (Media Independent Interface)
Ethernet MAC	• IEEE802.3u MAC (Ether) function • Supports transfer at 10 and 100 Mbps • Flow control conforming to IEEE802.3x or back pressure system • Supports interface conforming to IEEE802.3u • Magic packet detection • Includes DMAC • Supports RMII (Reduced Media Independent Interface)

1.3.11 Timer

Item	Description
Watchdog timer (RWDT)	• Single channel • Internal 16-bit watchdog timer operated by RCLK • Programmable overflow time-period: more than 1 hour count capable

Item	Description
Timer pulse unit (TPU)	• 4-channels • 16-bit timers • Each channel outputs PWM
Compare match timer 0 (CMT0)	• Two channels • 32-bit timer (16 bits/32 bits can be selected) • Source clock: RCLK clock • Compare match function provided • Interrupt requests
Compare match timer 1 (CMT1)	• Eight channels • 48-bit timer (16 bits/32 bits/48 bits can be selected) • Source clock: RCLK/system clock • Compare match function provided • Interrupt requests
Timer unit (TMU)	• 12 channels • 32-bit timer • Auto-reload type 32-bit down counter • Internal prescaler • Interrupt request • Two channels for input capture

1.3.12 Peripheral Module

Item	Description
I2C bus interface (IIC)	• Four channels • One of channel (Channel3) for DVFS • Supports single master transmission/reception • Interrupt request • DMAC request • IIC pins switchable with I2C pins (just below)
Multi-master I2C bus interface (I2C)	• Four channels • Philips I2C bus interface method supported • Master/slave functions • Multi-master functions • Transfer rate up to 400 kbps supported • Programmable clock generation from the system clock • Two channels for buffers with a slew rate (channel 0 and 3 for dedicated buffers), two channels for LVTTL buffers (channel 1 and 2 for ordinary buffers) • I2C pins switchable with IIC pins(just above)
Serial communication interface with FIFO (SCIFA)	• Three channels • Internal 64-byte transmit/receive FIFOs • High-speed UART • Internal prescaler • Clock synchronous serial communications possible • Support edge selection function • Interrupt request, DMAC request and DMA multi-Byte transfer supported • Asynchronous mode (modem control is enabled) • Clock synchronous mode
Serial communication interface with FIFO (SCIFB)	• Three channels • Internal 256-byte transmit/receive FIFOs • High-speed UART • Internal prescaler • Clock synchronous serial communications possible • Support edge selection function • Interrupt request, DMAC request and DMA multi-Byte transfer supported • Asynchronous mode (modem control is enabled) • Clock synchronous mode

Item	Description	
Serial communication interface with FIFO (SCIF)	Overall specification	• Three channels • Asynchronous, clock-synchronized modes • Asynchronous serial communication mode The SCIF performs serial data communication based on a character-by-character asynchronous system. This feature enables serial data communication with standard asynchronous communication chips that support Universal Asynchronous Receiver/Transmitter (UART) or Asynchronous Communication Interface Adapter (ACIA). There is a choice of eight serial data transfer formats. — Data length: 7 bits or 8 bits — Stop bits: 1 bit or 2 bits — Parity: Even/odd/none — Receive error detection: Parity, framing, and overrun errors — Break detection: A break is detected when a framing error lasts for more than 1 frame length at space 0 (low level). When a framing error occurs, a break can also be detected by reading the RX pin level directly from the serial port register (SCSPTR). • Clock synchronous serial communication mode The SCIF performs serial data communication synchronized with a clock. This feature enables serial data communication with other LSIs that support synchronous communication. There is a single serial data communication format for clock synchronous serial communication. — Data length: 8 bits — Receive error detection: Overrun errors • Full-duplex communication capability The SCIF has an independent transmitter and receiver that enable simultaneous transmission and reception. The transmitter and receiver both have a 16-stage FIFO buffer structure, enabling continuous serial data transmission and reception. • On-chip baud rate generator, enabling any bit rate to be selected The SCIF enables choice of a clock source for transmission/reception: a clock from the on-chip baud rate generator based on the internal clock or an external clock. • Eight interrupt sources The SCIF has eight types of interrupt sources: receive-data-ready, receive-FIFO-data-full, break, transmit-FIFO-data-empty, transmit-end, receive-error, overrun-error and time-out and enables any of them to be requested independently. • DMA data transfer When the transmit FIFO register is empty or the receive FIFO register has received data, issuing a DMA transfer request activates the DMA controller (DMAC) to execute a data transfer. • In asynchronous mode using channels 0 and 1, modem control functions (RTS and CTS) are stored. • The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available. • In asynchronous mode, a receive data ready (DR) or a timeout error (TO) can be detected during reception.

Item	Description
Clock-synchronized serial interface with FIFO (MSIOF)	• Four channels • Max. speed: 26 MHz (ch 2 only), 13 MHz (ch 0, 1, and 3) • Internal 64-byte transmit FIFOs/internal 256-byte receive FIFOs • Supports master and slave modes • Internal prescaler • Supports serial formats: IIS, SPI (master and slave modes) • Interrupt request, DMAC request
QSPI	• Single channel • Single/Dual/Quad-SPI • Supports master mode • SPICLK clock rate: 1 to 4080 in master mode; Max. 78 MHz
High-speed serial communication interface with FIFO (HSCIF)	• Two channels • Asynchronous serial communication mode • Capable of full-duplex communication • On-chip baud rate generator, enabling any bit rate to be selected • Eight interrupt sources • DMA data transfer • Modem control functions (HRTS and HCTS) are stored. • The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available. • A receive data ready (DR) or a timeout error (TO) can be detected during reception.
PWM timer (PWM)	• Seven channels • High-level width (10 bits) of PWM output can be set. • High-level periods (10 bits) of PWM can be set. • Periods in the range from two to 2^{24} × 1024 cycles of the Pϕ clock can be set. • Continuous pulse or single pulse output selectable
Boot Function (Booting)	• System startup with selectable boot mode at power-on reset • The external boot device can be selected as either external ROM (area 0) or on-chip ROM by the levels on the MD3 to MD1 pins. • Booting from the serial flash ROM connected to the QSPI is supported. • Autorun function for the downloaded program

Others

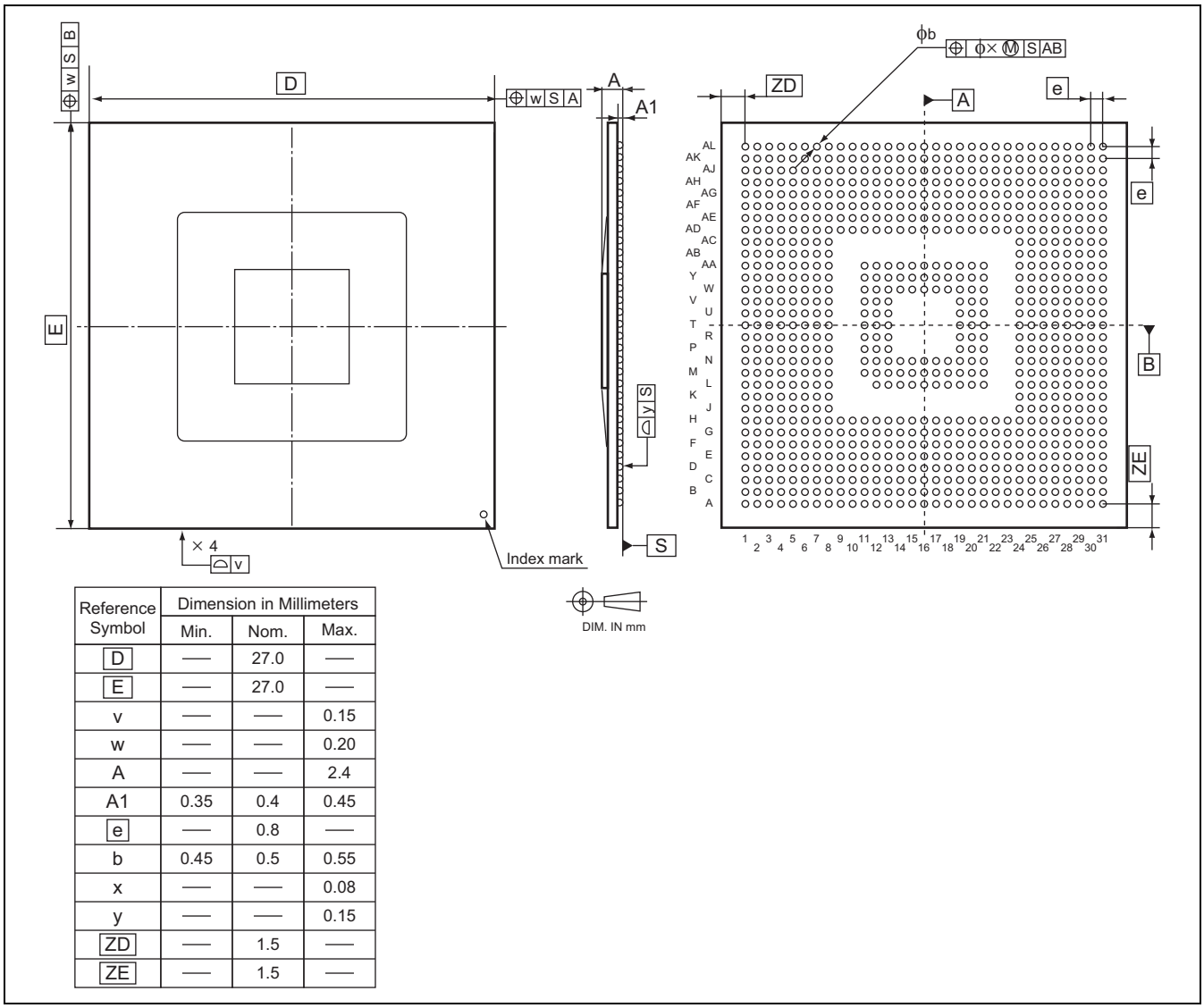
Item	Description
JTAG	JTAG interface for CoreSight
Process	28-nm Si-CMOS
Package	FC-BGA2727-831

1.4 Power Supply Voltages and Temperature Range

- Power supply voltage (typ.)
  1.8 V: (ETM, SDHI, DDR3_GPIO, LVCMOS I/F, Xtal, JTAG, and RST)
  1.03 V: (Core, SATA/USB3.0/PCI Express-I/O)
  1.5 V: (DDR3-I/O SSTL mode: DDR3)
  3.3 V: (Others)

- Temperature range
  Ta = –40°C to +85°C
  Tc = –40°C to +105°C

1.5 Package



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	27.0	—
E	—	27.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	2.4
A1	0.35	0.4	0.45
e	—	0.8	—
b	0.45	0.5	0.55
x	—	—	0.08
y	—	—	0.15
ZD	—	1.5	—
ZE	—	1.5	—

Figure 1.2 Package Outline

2. Area Map

See section 2, Area Map in the RZ/G Series User's Manual: Hardware.

3. Pin Assignment

3.1 Top View (Left)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	VDDQ_ M1	M1DQ31	M1DQ29	M1DM3	M1DQ28	VDDQ_ M1	M1DQ17	M1DQ21	VSS	M1DQ3	M1DM0	VDDQ_ M1	M1DQ8	M1DQ9	M1DQ15	M0A8
B	M1A0	VSS	M1DQ24	VSS	M1DQ30	M1DQ16	VSS	M1DQ19	M1DQ23	VSS	M1DQ1	M1DQ0	VSS	M1DQ11	M1DQ13	M0A14
C	M1BA1	M1A12	VSS	M1DQ26	M1DQ27	VSS	M1DM2	M1DQ18	VSS	M1DQ6	M1DQ4	VSS	M1DM1	M1DQ12	VDDQ_ M0	M0BA1
D	M1A5	VSS	M1RAS#	VSS	M1DQ25	M1DQ22	VSS	M1DQ20	VSS	M1DQ5	M1DQ7	M1DQ2	VSS	M1DQ10	M1DQ14	M0A5
E	M1A4	M1A2	M1WE#	M1CAS#	VSS	M1 DQS3#	M1DQS3	M1DQS2	M1 DQS2#	VSS	M1 DQS0#	M1DQS0	M1 DQS1#	M1DQS1	VSS	M0A12
F	VDDQ_ M1A	M1CS0#	VSS	M1ODT0	M1CKE0	VSS	VDDQ_ M1	VSS	VSSQ_ M1DPLL2	VDDQ_ M1DPLL2	VSS	VSSQ_ M1DPLL1	VDDQ_ M1DPLL1	VSS	VSS_ CPGPLL1	VDD_ CPGPLL1
G	M1CS1#	VSS	M1CKE1	VSS	M1 RESET#	VDDQ_ M1BKUP	VSS	M1VREF DQ1	VSSQ_ M1DPLL3	VDDQ_ M1DPLL3	VSS	VSSQ_ M1DPLL0	VDDQ_ M1DPLL0	M1VREF DQ0	VSS_ CPGPLL2	M0VREF CA (VSS)
H	M1A7	M1A1	M1BA2	M1ODT1	M1CK0#	VSS	M1VREF CA	VSS	VSS	VDDQ_ M1	VSS	VSS	VDDQ_ M1	VSS	VDD_ CPGPLL2	M0ZQ
J	VSS	M1A9	M1BA0	VSS	M1CK0	VDDQ_ M1A	M1BKP RST#	VSS								
K	M1A11	M1A6	M1A15	VSS	M1CK1#	VSSQ_ M1MPLL	VSSQ_ M1APLL	VSS								
L	M1A13	VDDQ_ M1A	M1A10	VSS	M1CK1	VDDQ_ M1MPLL	VDDQ_ M1APLL	M1ZQ				VDD	VDD_ DVFS	VSS	VDD_ DVFS	VSS
M	M1A8	M1A14	M1A3	VSS	VSS	VSS	VSS	VDDQ_ M1A			VSS	VSS	VDD_ DVFS	VSS	VDD_ DVFS	VSS
N	VSS	VSS	VSS	VDD_ CPGPLL0	VSS_ CPGPLL0	VSS_ CPGPLL3	VDD_ CPGPLL3	VSS			VDD	VDD	VSS	VSS	VDD_ DVFS	VSS
P	SD3_ CLK	VSS	SD3_ DAT3	SD3_ DAT2	SD3_ CMD	SD3_ CD	SD3_ WP	VCCQ_ SD3			VSS	VSS	VSS			
R	SD2_ CLK	VSS	SD2_ DAT2	SD2_ DAT1	SD2_ DAT0	SD3_ DAT1	SD3_ DAT0	VSS			VDD_ DVFS	VDD_ DVFS	VDD_ DVFS			
T	VSS	SD2_ CD	SD2_ WP	SD2_ CMD	SD2_ DAT3	SD1_ CMD	SD1_ DAT3	VCCQ_ SD2			VSS	VSS	VSS			
U	SD1_ CLK	VSS	SD1_ DAT2	SD1_ DAT1	VSS	SD1_ DAT0	SD1_ CD	VCCQ_ SD1			VDD_ DVFS	VDD_ DVFS	VDD_ DVFS			
V	SD0_ CLK	VSS	SD1 WP	SD0_ CMD	SD0_ DAT3	SD0_ DAT2	SD0_ DAT1	VSS			VSS	VSS	VSS			
W	VSS	SD0_ DAT0	SD0_ CD	SD0_ WP	VSS	VI0_ DATA5/ VI0_B5	VI0_ DATA4/ VI0_B4	VCCQ_ SD0			VDD	VDD	VSS	VSS	VDD_ DVFS	VSS
Y	VI0_ CLK	VSS	VI0_ DATA3/ VI0_B3	VI0_ DATA2/ VI0_B2	VI0_ DATA1/ VI0_B1	VI0_ DATA0/ VI0_B0	VTH SENSE0	VCCQ			VSS	VSS	VDD_ DVFS	VSS	VDD_ DVFS	VSS
AA	VI1_ DATA7/ VI1_B7	VI1_ DATA6/ VI1_B6	VI1_ DATA1/ VI1_B1	VI1_ DATA0/ VI1_B0	VI0_ DATA7/ VI0_B7	VI0_ DATA6/ VI0_B6	VTH REF0	VSS			VDD	VDD	VDD_ DVFS	VSS	VDD_ DVFS	VSS
AB	VI1_ CLK	VSS	VI1_ DATA5/ VI1_B5	VI1_ DATA4/ VI1_B4	VCCQ18	VI1_ DATA3/ VI1_B3	VI1_ DATA2/ VI1_B2	VCCQ								
AC	EX_CS0#	EX_CS1#	EX_CS2#	EX_CS3#	DREQ0	DACK0	VCCQ	VSS								
AD	CS0#	RD/WR#	RD#/ MD16	DACK1	DREQ1	DACK2	DREQ2	VSS	VCCQ	VSS	VCCQ	VSS	VSS	VCCQ18	VSS	VCCQ18
AE	CLKOUT	VSS	EX_CS4#	EX_CS5#	BS#/ MD13	A25	VSS	VSS	ETH_ MDC/ MD8	ETH_ TXD0/ MD9	ETH_ RXD1	PWM0/ MD7	BSMODE	TCK	MPMD0	VCCQ_ ISO
AF	A20	A21	A22	A23	A24	VSS	D12	D6	D0	ETH_ MAGIC/ MD10	ETH_ RXD0	EXREFIN (VSS)	ACK	TMS	IIC0_SDA	PRESET#
AG	A16/ MD18	A17/ MD17	A18/ MD15	A19/ MD14	VSS	A1/ MD27	D13	D7	D1	ETH_ TX_EN/ MD11	ETH_ RX_ER	NMI	VSS	VCCQ18	IIC0_SCL	TRST#
AH	WE0#	WE1#	A15/ MD19	VSS	A5/ MD23	A2/ MD26	VSS	D8	D2	ETH_ TXD1/ MD12	ETH_ CRS_DV	TDO	DU_ DOT CLKIN1	TDI	IIC3_SDA (DVFS)	VSS
AJ	PRESET OUT#	CS1#/A26	VSS	A9	A6/ MD22	A3/ MD25	D14	D9	D3	ETH_ MDIO	PWM2	DU DOT CLKIN2	DU DOT CLKIN0	MPMD1	IIC3_SCL (DVFS)	DU_ LVDS0_ CH3_N
AK	EX_ WAIT0	VSS	A12	A10	A7/ MD21	VCCQ	D15	D10	D4	ETH_ LINK	PWM1/ MD6	VSS	VSS	VSS	VSS	VSS
AL	VSS	A14/ MD20	A13	A11	A8	A4/ MD24	A0/ MD28	D11	D5	ETH_ REF_CLK	VSS	EXTAL	XTAL	USB_ EXTAL	USB_ XTAL	VSS
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

3.2 Top View (Right)

17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
M0A13	M0A11	M0CS1#	VDDQ_ M0	M0A4	M0A2	VSS	M0DQ9	M0DQ15	VDDQ_ M0	M0DQ0	M0DM0	M0DQ3	M0DQ7	VDDQ_ M0	A
M0A6	M0A9	VSS	M0CS0#	M0A7	M0A1	M0DQ8	M0DQ14	VSS	M0DQ12	M0DQ4	VSS	M0DQ5	VSS	M0DQ19	B
VSS	M0A10	M0CKE1	VSS	M0BA0	M0CAS#	VSS	M0DQ10	M0DM1	VSS	M0DQ6	M0DQ1	VSS	M0DQ17	M0DQ21	C
M0A3	M0A15	VSS	M0ODT0	M0BA2	M0RAS#	VSS	M0DQ11	VSS	M0DQ13	M0DQ2	VSS	M0DQ23	VSS	M0DM2	D
M0A0	M0ODT1	M0 RESET#	VDDQ_ M0	M0WE#	VSS	M0DQS1	M0DQS1#	M0DQS0#	M0DQS0	VSS	M0DQ22	M0DQ18	M0DQ20	M0DQ16	E
VSS	VSS	VSS	M0CKE0	VSS	VDDQ_ M0DPLL1	VSSQ_ M0DPLL1	VSS	VDDQ_ M0	VSS	M0DQS2	M0DQ24	VSS	M0DQ26	VDDQ_ M0	F
M0CK1	M0CK1#	M0CK0#	M0CK0	VDDQ_ M0APLL	VDDQ_ M0DPLL0	VSSQ_ M0DPLL0	M0VREF DQ0	VSS	VDDQ_ M0	M0DQS2#	VSS	M0DM3	VSS	M0DQ25	G
VDDQ_ M0	M0BKP RST#	VDDQ_ M0BKUP	VSS	VSSQ_ M0APLL	VDDQ_ M0	VSS	VSS	M0VREF DQ1	VSS	M0DQS3#	M0DQ28	M0DQ30	M0DQ27	M0DQ31	H
							VDDQ_ M0	VSSQ_ M0DPLL2	VSSQ_ M0DPLL3	M0DQS3	VSS	VSS	M0DQ29	VSS	J
							VSS	VDDQ_ M0DPLL2	VDDQ_ M0DPLL3	VSS	VCCQ18_ MLBP	VCCQ33_ MLBP	VSS	NC	K
VDD_ DVFS	VSS	VDD_ DVFS	VDD	VDD			VDDQ_ M0	VDD_ MLBP PLL0	VDD_ MLBP PLL1	VSS	NC	NC	VSS	NC	L
VDD_ DVFS	VSS	VDD_ DVFS	VSS	VSS			VSS	VSS_ MLBP PLL0	VSS_ MLBP PLL1	VSS	NC	NC	VSS	NC	M
VDD_ DVFS	VSS	VSS	VDD	VDD			VCCQ	VSS	VSS	VSS	VCCQ18_ MLBP	VCCQ33_ MLBP	VSS	NC	N
		VSS	VSS	VSS			VSS	VSS	SSI_ SDATA5	SSI_ SDATA1	VSS	SSI_ SDATA0	SSI_ WS0129	SSI_ SCK0129	P
		VDD_ DVFS	VDD_ DVFS	VDD_ DVFS			VCCQ	SSI_ SDATA9	SSI_ SDATA2	SSI_ SDATA3	SSI_ WS34	SSI_ SDATA4	VSS	SSI_ SCK34	R
		VSS	VSS	VSS			VSS	SSI SDATA6	SSI SDATA7	VCCQ	SSI SDATA8	SSI WS4	VSS	SSI SCK4	T
		VDD_ DVFS	VDD_ DVFS	VDD_ DVFS			VCCQ	HRTS0#	HCTS0#	SSI WS6	SSI WS78	SSI SCK6	SSI WS5	SSI SCK5	U
		VSS	VSS	VSS			VSS	MSIOF0_ SYNC	HRX0	HTX0/ MD1	HSCK0	SSI_ SCK78	VSS	AUDIO_ CLKA	V
VDD_ DVFS	VSS	VSS	VDD	VDD			VCCQ	SCIFA0 CTS#	MSIOF0_ SS2/ MDT0	MSIOF0_ RXD	MSIOF0_ SS1/ MD0	MSIOF0_ TXD/ MDT1	VCCQ	AUDIO CLKB	W
VDD_ DVFS	VSS	VDD_ DVFS	VSS	VSS			VSS	SCIFA1 CTS#	SCIFA1_ RTS#/ MD2	SCIFA1_ TXD/ MD3	SCIFA1 RXD	SCIFA0_ RTS#/ MD4	SCIFA0_ TXD/ MD5	MSIOF0 SCK	Y
VDD_ DVFS	VSS	VDD_ DVFS	VDD	VDD			VCCQ	AVS1	VSS_ MLBPLL	VDD_ MLBPLL	VCCQ18	SCIFA0_ RXD	SCIFA0_ SCK	NC	AA
							AVDD	VD181	AVS2	SCIFA2_ TXD	SCIFA2_ SCK	NC	VSS	NC	AB
							AVSS	AVDD	VD181	SCIFA2_ RXD	USB0_ PWEN	USB1_ PWEN	USB2_ OVC	NC	AC
VSS	VDDQ_ LVDS	DU_ LVDS0_ PLL1_VSS	DU_ LVDS1_ PLL1_VCC	DU_ LVDS1_ PLL1_VSS	VDDQ_ LVDS	VSS_ SATA1	VSS_ SATA0	AVSS	AVDD	VD181	USB0_ OVC/VBUS	USB1_ OVC	USB2_ PWEN	VSS	AD
VSS	VDDQ_ LVDS	VSS	DU_ LVDS0_ PLL1_VCC	VSS	VDDQ_ LVDS	VSS_ SATA1	VSS_ SATA1	VSS_ SATA0	AVSS	AVDD	VD331	VD331	VSS	USB0_ DM	AE
VSS	VDDQ_ LVDS	VSS	VSS	VSS	VDDQ_ LVDS	VDDD SATA1	VDDA SATA1	VSS SATA0	VSS SATA0	AVSS	AVSS	USB0_ RREF	VSS	USB0_ DP	AF
DU_ LVDS0_ CLK_P	DU_ LVDS0_ CLK_N	DU_ LVDS0_ CH1_P	DU_ LVDS0_ CH1_N	DU_ LVDS1_ CH3_N	DU_ LVDS1_ CH3_P	VDDD_ SATA1	VDDA_ SATA1	VDDD_ SATA0	VDDA_ SATA0	VSS_ SATA0	AVSS	USB1_ RREF	VSS	USB1_ DM	AG
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDD_ SATA1	VDDD_ SATA0	VDDD_ SATA0	VDDA_ SATA0	VSS_ SATA0	USB2_ RREF	VSS	USB1_ DP	AH
DU_ LVDS0_ CH3_P	DU_ LVDS0_ CH0_P	DU_ LVDS0_ CH0_N	DU_ LVDS1_ CH2_P	DU_ LVDS1_ CH2_N	DU_ LVDS1_ CH0_N	DU_ LVDS1_ CH0_P	VSS_ SATA1	CICREF N1_SATA	CICREF P1_SATA	CICREF N0_SATA	CICREF P0_SATA	VSS_ SATA0	VSS	USB2_ DM	AJ
VSS	VSS	VSS	VSS	VSS	VSS	VSS SATA1	VSS SATA1	VSS SATA1	VSS SATA1	VSS SATA0	VSS SATA0	VSS SATA0	VSS SATA0	USB2_ DP	AK
DU_ LVDS0_ CH2_N	DU_ LVDS0_ CH2_P	DU_ LVDS1_ CLK_P	DU_ LVDS1_ CLK_N	DU_ LVDS1_ CH1_P	DU_ LVDS1_ CH1_N	RIDP1 SATA	RIDN1 SATA	TODP1 SATA	TODN1 SATA	RIDP0 SATA	RIDN0 SATA	TODP0 SATA	TODN0 SATA	VSS_ SATA0	AL
17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	

: Multiplexed pin that function is selected by the Pin Function Controller (PFC) register and mode pin setting.

: Mode pin assigned.

3.3 Mode Pin Settings

Input fixed values for the MPMD0, MPMD1, and BSMODE pins. These values cannot be changed after power is supplied. The values of pins MD0 to MD28, MDT0 and MDT1 are input upon power-on reset using the PRESET# pin. Power-on reset results in switching to a different function.

Legend: "0" means logic low level input, "1" means logic high level input.
"—" means either "0" or "1", but its level must be fixed.

MPMD1	MPMD0	MP Mode Switching
0	0	Normal operation
0	1	Setting prohibited
1	0	Setting prohibited
1	1	Setting prohibited

BSMODE	JTAG Pin Operating Mode Switching
0	Normal operation
1	Operates in boundary scan mode. When PRESET# is at low level, pin IO control is disabled.

MD0	Free-Running Mode or Step-Up Mode
0	Free-running mode
1	Step-up mode

MD3	MD2	MD1	Boot Device Selection
0	0	0	Area 0 boot (boot from the external mask ROM)
0	1	0	QSPI (high speed/16 Kbytes)
0	0	1	Reserved
0	1	1	Reserved
1	0	0	QSPI (low speed/16 Kbytes)
1	1	0	QSPI (low speed/4 Kbytes)
1	0	1	Reserved
1	1	1	Reserved

MD4	Area Division
0	Area 0: 64 Mbytes
1	Area 0: 128 Mbytes

MD5	Reserved, fixed to 1

MD7	MD6	Master Boot Processor Selection
0	0	CA15 boot
0	1	CA7 boot
1	0	Setting prohibited
1	1	Setting prohibited

MD8	EXBUS Area 0 Data Bus Width
0	8-bit
1	16-bit

MD9	EXTAL/XTAL Pin Setting
0	Inputs an external clock to the EXTAL pin.
1	Connects a crystal resonator to the EXTAL/XTAL pin.

MD12	MD10	MD21, 20	MD11	MDT [1:0]	JTAG	SDHI0	SDHI1
0	0	00	—	—	Boundary scan	Normal	Normal
		01	—	—	Reserved	Reserved	Reserved
		10	0	—	CoreSight debug port	Normal	Normal
			1	00		Reserved	Normal
				01		Reserved	Normal
				10		Normal	Reserved
				11		Normal	Reserved
		11	0	—	Reserved	Normal	Normal
			1	00		CoreSight debug port	Normal
				01	Reserved	Reserved	Reserved
				1-			
	1	00	—	—	Reserved	Reserved	Reserved
		01	0	—	CoreSight debug port	Normal	Normal
			1	00		Reserved	Normal
				01		Reserved	Normal
				1-	Reserved	Reserved	Reserved
		10	—	—	Reserved	Reserved	Reserved
		11	—	—	Reserved	Reserved	Reserved
1	—	—	—	—	Reserved	Reserved	Reserved

Note: For normal operation, set MD12, MD10 and MD[21:20] to 0000 and TRST# pin must be pulled-down (MD11 and MDT[1:0]: don't care, but which level must be fixed at a power-on reset).

MD14	MD13	Internal Clock	External Clock	PLL1	PLL0	PLL3/ MD19: DDR3-1600	PLL3/ MD19: DDR3-1333
0	0	15 MHz	× 1/1*1	× 208*3	× 172	× 106 (VCO = 1590 MHz)	× 88 (VCO = 1320 MHz)
	1	20 MHz	× 1/1*1	× 156*3	× 130	× 80 (VCO = 1600 MHz)	× 66 (VCO = 1320 MHz)
1	0	26 MHz	× 1/2*2	× 240*3	× 200	× 122 (VCO = 1586 MHz)	× 102 (VCO = 1326 MHz)
	1	30 MHz	× 1/2*2	× 208*3	× 172	× 106 (VCO = 1590 MHz)	× 88 (VCO = 1320 MHz)

Note: 1. Do not input the clock frequency of less than 12 MHz when the input division ratio is × 1/1.
2. Do not input the clock frequency of less than 24 MHz when the input division ratio is × 1/2.
3. VCO = 3120 MHz

MD15	Reserved, fixed to 0

MD16	Power Off Control
0	Setting prohibited
1	Normal: Power off control enabled

MD18	External Bus Clock
0	65 MHz
1	43.3 MHz

MD19	DDR3-SDRAM Bus Clock
0	DDR3-1600 mode
1	DDR3-1333 mode

MD28	MD27	MD22	MD17	DDR 64 Bits or 32 Bits	Remarks
0	0	0	0	DDR 64 bits × single channel	Reserved
			1		Reserved
		1	0		Reserved
			1		Reserved
	1	0	0		Reserved
			1		Reserved
		1	0		DDR3_GPIO (29-bit)
1	0	0	0	DDR 32 bits × single channel	Reserved
			1		Reserved
		1	0		Reserved
			1		Reserved
	1	0	0		Reserved
			1		Reserved
		1	0		DDR3_GPIO (29-bit)
—	1	1	1	DDR 32 bits × two channels	(No DDR3_GPIO)

MD23	ComboPHY1 Function Selection
0	SATA-0
1	USB3.0

MD24	ComboPHY0 Function Selection
0	SATA-1
1	PCI express

MD26 and MD25	Reserved, fixed to 00

4. Pin Multiplexing

4.1 List of Multiplexed Pin Functions

Table 4.1 lists the multiplexed pin functions of the RZ/G1H.

The default pin function of each pin after power-on reset is "Function 1" respectively, unless otherwise mentioned in each table note.

For details on pin function control, refer to section 3.3, Mode Pin Settings and section 5, Pin Function Controller (PFC).

[Legend]

No.: Serial number, Pin No.: BGA package ball grid number, Mode Pin (only for corresponding pin): Mode pin is assigned, Function n (n=1, 2, 3, ...)/GPIO: Module or GPIO, Module: Module abbreviation except for GPIO, Pin Name: Module or GPIO pin name, I/O: Input or output

"Reserved" in module column is assigned internal function and "-" in module column is undefined, they must not be specified.

During POR: Pin state during power-on reset (PRESET# pin input is low-level).

V/|IOH|: Pin voltage and output drive current (nominal value respectively).

Pull-up: Internal pull-up control function is available or not from a power-on reset.

"On": Pull-up control function is available and default state is pulled-up.
(No.292, ACK pin is available for internal pull-down function.)
"Off": Pull-up control function is available and default state is not pulled-up.
"-": Pull-up control function is not available.
For details of pull-up control function, refer to PUPR0 through PUPR6 registers in section 5, Pin Function Controller (PFC).

I: Input, I(S): Schmitt input, IO: Input and output, IO (OD): Input and open drain output, O: Output, P: Power supply pin.

(H)/(L)/(X)/(Z) in I/O row: Default pin state (only for default pin, except for clock or analog output)

H: High level output, L: Low level output, X: Undefined value output, Z: High impedance

Notes:

1. All power supply pins and ground pins must be supplied suitable power supply and GND respectively.
2. All mode pins must be used during power-on reset.
3. Pin name that has an identifier for example "XXXX_B", "XXXX_C" etc. are mirror pins of the XXXX pin. Only one pin out of the XXXX pin or its mirror pins can be used. When using mirror pin, specify the suite of pin that has the same identifier for the selected module. It is prohibited to use a suite of pin as mixed two or more identifiers for a selected module.
4. Do not use any pins that of unused modules.
5. Unused pins must be handled as described in section 4.3, Handling of Unused Pins.
6. The terminal state after the reset cancellation has been described as a premise not using the BKPRST (BKRST#=H(fixed)).

Table 4.1 List of Multiplexed Pin Functions

DBSC3 channel 0 (No.1 to 60): Single Function

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V/|IOH|
	I/O	Pull-up
1	DBSC3 channel 0	O
F20	M0CKE0	1.5V/-
	O(L)	-
2	DBSC3 channel 0	O
C19	M0CKE1	1.5V/-
	O(L)	-
3	DBSC3 channel 0	P
G16	M0VREFCA*(VSS)	-
	P	-
4	DBSC3 channel 0	I
H18	M0BKPRST#	1.5V/-
	I	-
5	DBSC3 channel 0	H
E19	M0RESET#	1.5V/-
	O(H to L)	-
6	DBSC3 channel 0	X
G20	M0CK0	1.5V/-
	O	-
7	DBSC3 channel 0	X
G19	M0CK0#	1.5V/-
	O	-
8	DBSC3 channel 0	X
G17	M0CK1	1.5V/-
	O	-
9	DBSC3 channel 0	X
G18	M0CK1#	1.5V/-
	O	-
10	DBSC3 channel 0	H
B20	M0CS0#	1.5V/-
	O(H)	-
11	DBSC3 channel 0	H
A19	M0CS1#	1.5V/-
	O(H)	-
12	DBSC3 channel 0	L
D20	M0ODT0	1.5V/-
	O(L)	-
13	DBSC3 channel 0	L
E18	M0ODT1	1.5V/-
	O(L)	-
14	DBSC3 channel 0	IO
H16	M0ZQ	-
	IO	-
15	DBSC3 channel 0	H
E21	M0WE#	1.5V/-
	O(H)	-
16	DBSC3 channel 0	H
D22	M0RAS#	1.5V/-
	O(H)	-
17	DBSC3 channel 0	H
C22	M0CAS#	1.5V/-
	O(H)	-
18	DBSC3 channel 0	L
E17	M0A0	1.5V/-
	O(L)	-
19	DBSC3 channel 0	L
B22	M0A1	1.5V/-
	O(L)	-
20	DBSC3 channel 0	L
A22	M0A2	1.5V/-
	O(L)	-

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V/|IOH|
	I/O	Pull-up
21	DBSC3 channel 0	L
D17	M0A3	1.5V/-
	O(L)	-
22	DBSC3 channel 0	L
A21	M0A4	1.5V/-
	O(L)	-
23	DBSC3 channel 0	L
D16	M0A5	1.5V/-
	O(L)	-
24	DBSC3 channel 0	L
B17	M0A6	1.5V/-
	O(L)	-
25	DBSC3 channel 0	L
B21	M0A7	1.5V/-
	O(L)	-
26	DBSC3 channel 0	L
A16	M0A8	1.5V/-
	O(L)	-
27	DBSC3 channel 0	L
B18	M0A9	1.5V/-
	O(L)	-
28	DBSC3 channel 0	L
C18	M0A10	1.5V/-
	O(L)	-
29	DBSC3 channel 0	L
A18	M0A11	1.5V/-
	O(L)	-
30	DBSC3 channel 0	L
E16	M0A12	1.5V/-
	O(L)	-
31	DBSC3 channel 0	L
A17	M0A13	1.5V/-
	O(L)	-
32	DBSC3 channel 0	L
B16	M0A14	1.5V/-
	O(L)	-
33	DBSC3 channel 0	L
D18	M0A15	1.5V/-
	O(L)	-
34	DBSC3 channel 0	L
C21	M0BA0	1.5V/-
	O(L)	-
35	DBSC3 channel 0	L
C16	M0BA1	1.5V/-
	O(L)	-
36	DBSC3 channel 0	L
D21	M0BA2	1.5V/-
	O(L)	-
37	DBSC3 channel 0	P
G21	VDDQ_M0APLL	-
	P	-
38	DBSC3 channel 0	P
H21	VSSQ_M0APLL	-
	P	-
39	DBSC3 channel 0	Z
A27	M0DQ0	1.5V/-
	IO(Z)	-
40	DBSC3 channel 0	Z
C28	M0DQ1	1.5V/-
	IO(Z)	-

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V/|IOH|
	I/O	Pull-up
41	DBSC3 channel 0	Z
D27	M0DQ2	1.5V/-
	IO(Z)	-
42	DBSC3 channel 0	Z
A29	M0DQ3	1.5V/-
	IO(Z)	-
43	DBSC3 channel 0	Z
B27	M0DQ4	1.5V/-
	IO(Z)	-
44	DBSC3 channel 0	Z
B29	M0DQ5	1.5V/-
	IO(Z)	-
45	DBSC3 channel 0	Z
C27	M0DQ6	1.5V/-
	IO(Z)	-
46	DBSC3 channel 0	Z
A30	M0DQ7	1.5V/-
	IO(Z)	-
47	DBSC3 channel 0	Z**
E26	M0DQS0	1.5V/-
	IO(Z**)	-
48	DBSC3 channel 0	Z**
E25	M0DQS0#	1.5V/-
	IO(Z**)	-
49	DBSC3 channel 0	Z
A28	M0DM0	1.5V/-
	O(Z)	-
50	DBSC3 channel 0	P
G22	VDDQ_M0DPLL0	-
	P	-
51	DBSC3 channel 0	P
G23	VSSQ_M0DPLL0	-
	P	-
52	DBSC3 channel 0	P
G24	M0VREFDQ0	-
	P	-
53	DBSC3 channel 0	Z
B23	M0DQ8	1.5V/-
	IO(Z)	-
54	DBSC3 channel 0	Z
A24	M0DQ9	1.5V/-
	IO(Z)	-
55	DBSC3 channel 0	Z
C24	M0DQ10	1.5V/-
	IO(Z)	-
56	DBSC3 channel 0	Z
D24	M0DQ11	1.5V/-
	IO(Z)	-
57	DBSC3 channel 0	Z
B26	M0DQ12	1.5V/-
	IO(Z)	-
58	DBSC3 channel 0	Z
D26	M0DQ13	1.5V/-
	IO(Z)	-
59	DBSC3 channel 0	Z
B24	M0DQ14	1.5V/-
	IO(Z)	-
60	DBSC3 channel 0	Z
A25	M0DQ15	1.5V/-
	IO(Z)	-

1/2 (DBSC3 channel 0)

Note: * (No.3): Must be fixed to VSS.

DBSC3 channel 0 (No.61 to 93): Single Function

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V/|IOH|
	I/O	Pull-up
61	DBSC3 channel 0	Z**
E23	M0DQS1	1.5V/-
	IO(Z**)	-
62	DBSC3 channel 0	Z**
E24	M0DQS1#	1.5V/-
	IO(Z**)	-
63	DBSC3 channel 0	Z
C25	M0DM1	1.5V/-
	O(Z)	-
64	DBSC3 channel 0	P
F22	VDDQ_M0DPLL1	-
	P	-
65	DBSC3 channel 0	P
F23	VSSQ_M0DPLL1	-
	P	-
66	DBSC3 channel 0	Z
E31	M0DQ16	1.5V/-
	IO(Z)	-
67	DBSC3 channel 0	Z
C30	M0DQ17	1.5V/-
	IO(Z)	-
68	DBSC3 channel 0	Z
E29	M0DQ18	1.5V/-
	IO(Z)	-
69	DBSC3 channel 0	Z
B31	M0DQ19	1.5V/-
	IO(Z)	-
70	DBSC3 channel 0	Z
E30	M0DQ20	1.5V/-
	IO(Z)	-
71	DBSC3 channel 0	Z
C31	M0DQ21	1.5V/-
	IO(Z)	-

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V/|IOH|
	I/O	Pull-up
72	DBSC3 channel 0	Z
E28	M0DQ22	1.5V/-
	IO(Z)	-
73	DBSC3 channel 0	Z
D29	M0DQ23	1.5V/-
	IO(Z)	-
74	DBSC3 channel 0	Z**
F27	M0DQS2	1.5V/-
	IO(Z**)	-
75	DBSC3 channel 0	Z**
G27	M0DQS2#	1.5V/-
	IO(Z**)	-
76	DBSC3 channel 0	Z
D31	M0DM2	1.5V/-
	O(Z)	-
77	DBSC3 channel 0	P
K25	VDDQ_M0DPLL2	-
	P	-
78	DBSC3 channel 0	P
J25	VSSQ_M0DPLL2	-
	P	-
79	DBSC3 channel 0	P
H25	M0VREFDQ1	-
	P	-
80	DBSC3 channel 0	Z
F28	M0DQ24	1.5V/-
	IO(Z)	-
81	DBSC3 channel 0	Z
G31	M0DQ25	1.5V/-
	IO(Z)	-
82	DBSC3 channel 0	Z
F30	M0DQ26	1.5V/-
	IO(Z)	-

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V/|IOH|
	I/O	Pull-up
83	DBSC3 channel 0	Z
H30	M0DQ27	1.5V/-
	IO(Z)	-
84	DBSC3 channel 0	Z
H28	M0DQ28	1.5V/-
	IO(Z)	-
85	DBSC3 channel 0	Z
J30	M0DQ29	1.5V/-
	IO(Z)	-
86	DBSC3 channel 0	Z
H29	M0DQ30	1.5V/-
	IO(Z)	-
87	DBSC3 channel 0	Z
H31	M0DQ31	1.5V/-
	IO(Z)	-
88	DBSC3 channel 0	Z**
J27	M0DQS3	1.5V/-
	IO(Z**)	-
89	DBSC3 channel 0	Z**
H27	M0DQS3#	1.5V/-
	IO(Z**)	-
90	DBSC3 channel 0	Z
G29	M0DM3	1.5V/-
	O(Z)	-
91	DBSC3 channel 0	P
K26	VDDQ_M0DPLL3	-
	P	-
92	DBSC3 channel 0	P
J26	VSSQ_M0DPLL3	-
	P	-
93	DBSC3 channel 0	P
H19	VDDQ_M0BKUP	-
	P	-

2/2 (DBSC3 channel 0)

Note for DBSC3 channel 0 DQS/DQS# states. ** (No.47/48, 61/62, 74/75, 88/89):

The drivers output states are both high-impedance (Z), and the internal circuit controls pin levels as low-level for the M0DQSx pins and high-level for the M0DQSx# pins respectively.

DBSC3 channel 1 (32-bit)/DBSC3 channel 0 (64-bit)/DDR3 GPIO (No.94 to 113): Up to 3-Function Multiplexed

Pin state during power-on reset and default pin function are defined by the MD28, MD 27, MD22 and MD17 pins setting, which function cannot be changed after power-on reset by software.

Function	1	2	3	
Mode Pin settings	(MD28, MD27, MD22, MD17) = (0/1, 1, 1, 1)	= (0, 1, 1, 0)	= (1, 1, 1, 0)	
No.	Module			During POR
Pin No.	Pin Name			V/|IOH|
	I/O			Pull-up
94	DBSC3 channel 1	GPIO	GPIO	O/X(GPIO)
F5	M1CKE0	GP_DDR1	GP_DDR1	1.5V/1.8V(GPIO)/-
	O(L)	O	O	-
95	DBSC3 channel 1	GPIO	GPIO	O/X(GPIO)
G3	M1CKE1	GP_DDR2	GP_DDR2	1.5V/1.8V(GPIO)/-
	O(L)	O	O	-
96	DBSC3 channel 1	Unused	Unused	P
H7	M1VREFCA	(M1VREFCA)	(M1VREFCA)	-
	P	P	P	-
97	DBSC3 channel 1	Unused	Unused	I
J7	M1BKPRST#	(M1BKPRST#)	(M1BKPRST#)	1.5V/-
	I	I	I	-
98	DBSC3 channel 1	GPIO	GPIO	H/X(GPIO)
G5	M1RESET#	GP_DDR3	GP_DDR3	1.5V/1.8V(GPIO)/-
	O(H to L)	O	O	-
99	DBSC3 channel 1	Reserved*	Reserved*	X
J5	M1CK0	-	-	1.5V/-
	O	-	-	-
100	DBSC3 channel 1	Reserved*	Reserved*	X
H5	M1CK0#	-	-	1.5V/-
	O	-	-	-
101	DBSC3 channel 1	Reserved*	Reserved*	X
L5	M1CK1	-	-	1.5V/-
	O	-	-	-
102	DBSC3 channel 1	Reserved*	Reserved*	X
K5	M1CK1#	-	-	1.5V/-
	O	-	-	-
103	DBSC3 channel 1	GPIO	GPIO	H/I
F2	M1CS0#	GP_DDR5	GP_DDR5	1.5V/1.8V(GPIO)/-
	O(H)	I	I	-
104	DBSC3 channel 1	GPIO	GPIO	H/I
G1	M1CS1#	GP_DDR8	GP_DDR8	1.5V/1.8V(GPIO)/-
	O(H)	I	I	-
105	DBSC3 channel 1	GPIO	GPIO	L/I
F4	M1ODT0	GP_DDR6	GP_DDR6	1.5V/1.8V(GPIO)/-
	O(L)	I	I	-
106	DBSC3 channel 1	GPIO	GPIO	L/I
H4	M1ODT1	GP_DDR10	GP_DDR10	1.5V/1.8V(GPIO)/-
	O(L)	I	I	-
107	DBSC3 channel 1	Unused	Unused	IO
L8	M1ZQ	(M1ZQ)	(M1ZQ)	1.5V/-
	IO	IO	IO	-
108	DBSC3 channel 1	GPIO	GPIO	H/Z
E3	M1WE#	GP_DDR9	GP_DDR9	1.5V/1.8V(GPIO)/-
	O(H)	O(Z)	O(Z)	-
109	DBSC3 channel 1	GPIO	GPIO	H/Z
D3	M1RAS#	GP_DDR12	GP_DDR12	1.5V/1.8V(GPIO)/-
	O(H)	O(Z)	O(Z)	-
110	DBSC3 channel 1	GPIO	GPIO	H/I
E4	M1CAS#	GP_DDR4	GP_DDR4	1.5V/1.8V(GPIO)/-
	O(H)	I	I	-
111	DBSC3 channel 1	GPIO	GPIO	L/Z
B1	M1A0	GP_DDR7	GP_DDR7	1.5V/1.8V(GPIO)/-
	O(L)	O(Z)	O(Z)	-
112	DBSC3 channel 1	GPIO	GPIO	L/I
H2	M1A1	GP_DDR13	GP_DDR13	1.5V/1.8V(GPIO)/-
	O(L)	I	I	-
113	DBSC3 channel 1	GPIO	GPIO	L/Z
E2	M1A2	GP_DDR15	GP_DDR15	1.5V/1.8V(GPIO)/-
	O(L)	O(Z)	O(Z)	-

1/5 (DBSC3 channel 1)

Note: * Reserved pins in function 2 and 3 should be opened.

DBSC3 channel 1 (32-bit)/DBSC3 channel 0 (64-bit)/DDR3 GPIO (No.114 to 133): Up to 3-Function Multiplexed

Pin state during power-on reset and default pin function are defined by the MD28, MD 27, MD22 and MD17 pins setting, which function cannot be changed after power-on reset by software.

Function	1	2	3	
Mode Pin settings	(MD28, MD27, MD22, MD17) = (0/1, 1, 1, 1)	= (0, 1, 1, 0)	= (1, 1, 1, 0)	
No.	Module			During POR
Pin No.	Pin Name			V/|IOH|
	I/O			Pull-up
114	DBSC3 channel 1	GPIO	GPIO	L/I
M3	M1A3	GP_DDR23	GP_DDR23	1.5V/1.8V(GPIO)/-
	O(L)	I	I	-
115	DBSC3 channel 1	GPIO	GPIO	L/Z
E1	M1A4	GP_DDR17	GP_DDR17	1.5V/1.8V(GPIO)/-
	O(L)	O(Z)	O(Z)	-
116	DBSC3 channel 1	GPIO	GPIO	L/Z
D1	M1A5	GP_DDR11	GP_DDR11	1.5V/1.8V(GPIO)/-
	O(L)	O(Z)	O(Z)	-
117	DBSC3 channel 1	GPIO	GPIO	L/Z
K2	M1A6	GP_DDR24	GP_DDR24	1.5V/1.8V(GPIO)/-
	O(L)	O(Z)	O(Z)	-
118	DBSC3 channel 1	GPIO	GPIO	L/I
H1	M1A7	GP_DDR14	GP_DDR14	1.5V/1.8V(GPIO)/-
	O(L)	I	I	-
119	DBSC3 channel 1	GPIO	GPIO	L/I
M1	M1A8	GP_DDR25	GP_DDR25	1.5V/1.8V(GPIO)/-
	O(L)	I	I	-
120	DBSC3 channel 1	GPIO	GPIO	L/Z
J2	M1A9	GP_DDR26	GP_DDR26	1.5V/1.8V(GPIO)/-
	O(L)	O(Z)	O(Z)	-
121	DBSC3 channel 1	GPIO	GPIO	L/I
L3	M1A10	GP_DDR22	GP_DDR22	1.5V/1.8V(GPIO)/-
	O(L)	I	I	-
122	DBSC3 channel 1	GPIO	GPIO	L/Z
K1	M1A11	GP_DDR21	GP_DDR21	1.5V/1.8V(GPIO)/-
	O(L)	O(Z)	O(Z)	-
123	DBSC3 channel 1	GPIO	GPIO	L/Z
C2	M1A12	GP_DDR16	GP_DDR16	1.5V/1.8V(GPIO)/-
	O(L)	O(Z)	O(Z)	-
124	DBSC3 channel 1	GPIO	GPIO	L/I
L1	M1A13	GP_DDR27	GP_DDR27	1.5V/1.8V(GPIO)/-
	O(L)	I	I	-
125	DBSC3 channel 1	GPIO	GPIO	L/I
M2	M1A14	GP_DDR28	GP_DDR28	1.5V/1.8V(GPIO)/-
	O(L)	I	I	-
126	DBSC3 channel 1	GPIO	GPIO	L/Z
K3	M1A15	GP_DDR29	GP_DDR29	1.5V/1.8V(GPIO)/-
	O(L)	O(Z)	O(Z)	-
127	DBSC3 channel 1	GPIO	GPIO	L/Z
J3	M1BA0	GP_DDR20	GP_DDR20	1.5V/1.8V(GPIO)/-
	O(L)	O(Z)	O(Z)	-
128	DBSC3 channel 1	GPIO	GPIO	L/Z
C1	M1BA1	GP_DDR19	GP_DDR19	1.5V/1.8V(GPIO)/-
	O(L)	O(Z)	O(Z)	-
129	DBSC3 channel 1	GPIO	GPIO	L/I
H3	M1BA2	GP_DDR18	GP_DDR18	1.5V/1.8V(GPIO)/-
	O(L)	I	I	-
130	DBSC3 channel 1	DBSC3 channel 1	DBSC3 channel 1	P
L7	VDDQ_M1APLL	VDDQ_M1APLL	VDDQ_M1APLL	-
	P	P	P	-
131	DBSC3 channel 1	DBSC3 channel 1	DBSC3 channel 1	P
K7	VSSQ_M1APLL	VSSQ_M1APLL	VSSQ_M1APLL	-
	P	P	P	-
132	DBSC3 channel 1	DBSC3 channel 1	DBSC3 channel 1	P
L6	VDDQ_M1MPLL	VDDQ_M1MPLL	VDDQ_M1MPLL	-
	P	P	P	-
133	DBSC3 channel 1	DBSC3 channel 1	DBSC3 channel 1	P
K6	VSSQ_M1MPLL	VSSQ_M1MPLL	VSSQ_M1MPLL	-
	P	P	P	-

2/5 (DBSC3 channel 1)

DBSC3 channel 1 (32-bit)/DBSC3 channel 0 (64-bit)/DDR3 GPIO (No.134 to 153): Up to 3-Function Multiplexed

Pin state during power-on reset and default pin function are defined by the MD28, MD 27, MD22 and MD17 pins setting, which function cannot be changed after power-on reset by software.

Function	1	2	3	
Mode Pin settings	(MD28, MD27, MD22, MD17) = (0/1, 1, 1, 1)	= (0, 1, 1, 0)	= (1, 1, 1, 0)	
No.	Module			During POR
Pin No.	Pin Name			V/|IOH|
	I/O			Pull-up
134	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
B12	M1DQ0	M0DQ32	-	1.5V/-
	IO(Z)	IO(Z)	-	-
135	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
B11	M1DQ1	M0DQ33	-	1.5V/-
	IO(Z)	IO(Z)	-	-
136	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
D12	M1DQ2	M0DQ34	-	1.5V/-
	IO(Z)	IO(Z)	-	-
137	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
A10	M1DQ3	M0DQ35	-	1.5V/-
	IO(Z)	IO(Z)	-	-
138	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
C11	M1DQ4	M0DQ36	-	1.5V/-
	IO(Z)	IO(Z)	-	-
139	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
D10	M1DQ5	M0DQ37	-	1.5V/-
	IO(Z)	IO(Z)	-	-
140	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
C10	M1DQ6	M0DQ38	-	1.5V/-
	IO(Z)	IO(Z)	-	-
141	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
D11	M1DQ7	M0DQ39	-	1.5V/-
	IO(Z)	IO(Z)	-	-
142	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z**
E12	M1DQS0	M0DQS4	-	1.5V/-
	IO(Z**)	IO(Z**)	-	-
143	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z**
E11	M1DQS0#	M0DQS4#	-	1.5V/-
	IO(Z**)	IO(Z**)	-	-
144	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
A11	M1DM0	M0DM4	-	1.5V/-
	O(Z)	O(Z)	-	-
145	DBSC3 channel 1	DBSC3 channel 0	DBSC3 channel 0	P
G13	VDDQ_M1DPLL0	VDDQ_M0DPLL4	VDDQ_M0DPLL4	-
	P	P	P	-
146	DBSC3 channel 1	DBSC3 channel 0	DBSC3 channel 0	P
G12	VSSQ_M1DPLL0	VSSQ_M0DPLL4	VSSQ_M0DPLL4	-
	P	P	P	-
147	DBSC3 channel 1	DBSC3 channel 0	DBSC3 channel 0	P
G14	M1VREFDQ0	M0VREFDQ2	M0VREFDQ2	-
	P	P	P	-
148	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
A13	M1DQ8	M0DQ40	-	1.5V/-
	IO(Z)	IO(Z)	-	-
149	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
A14	M1DQ9	M0DQ41	-	1.5V/-
	IO(Z)	IO(Z)	-	-
150	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
D14	M1DQ10	M0DQ42	-	1.5V/-
	IO(Z)	IO(Z)	-	-
151	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
B14	M1DQ11	M0DQ43	-	1.5V/-
	IO(Z)	IO(Z)	-	-
152	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
C14	M1DQ12	M0DQ44	-	1.5V/-
	IO(Z)	IO(Z)	-	-
153	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
B15	M1DQ13	M0DQ45	-	1.5V/-
	IO(Z)	IO(Z)	-	-

3/5 (DBSC3 channel 1)

Note: * Reserved pins in function 3 should be opened.

DBSC3 channel 1 (32-bit)/DBSC3 channel 0 (64-bit)/DDR3 GPIO (No.154 to 173): Up to 3-Function Multiplexed

Pin state during power-on reset and default pin function are defined by the MD28, MD 27, MD22 and MD17 pins setting, which function cannot be changed after power-on reset by software.

Function	1	2	3	
Mode Pin settings	(MD28, MD27, MD22, MD17) = (0/1, 1, 1, 1)	= (0, 1, 1, 0)	= (1, 1, 1, 0)	
No.	Module			During POR
Pin No.	Pin Name			V/|IOH|
	I/O			Pull-up
154	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
D15	M1DQ14	M0DQ46	-	1.5V/-
	IO(Z)	IO(Z)	-	-
155	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
A15	M1DQ15	M0DQ47	-	1.5V/-
	IO(Z)	IO(Z)	-	-
156	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z**
E14	M1DQS1	M0DQS5	-	1.5V/-
	IO(Z**)	IO(Z**)	-	-
157	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z**
E13	M1DQS1#	M0DQS5#	-	1.5V/-
	IO(Z**)	IO(Z**)	-	-
158	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
C13	M1DM1	M0DM5	-	1.5V/-
	O(Z)	O(Z)	-	-
159	DBSC3 channel 1	DBSC3 channel 0	DBSC3 channel 0	P
F13	VDDQ_M1DPLL1	VDDQ_M0DPLL5	VDDQ_M0DPLL5	-
	P	P	P	-
160	DBSC3 channel 1	DBSC3 channel 0	DBSC3 channel 0	P
F12	VSSQ_M1DPLL1	VSSQ_M0DPLL5	VSSQ_M0DPLL5	-
	P	P	P	-
161	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
B6	M1DQ16	M0DQ48	-	1.5V/-
	IO(Z)	IO(Z)	-	-
162	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
A7	M1DQ17	M0DQ49	-	1.5V/-
	IO(Z)	IO(Z)	-	-
163	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
C8	M1DQ18	M0DQ50	-	1.5V/-
	IO(Z)	IO(Z)	-	-
164	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
B8	M1DQ19	M0DQ51	-	1.5V/-
	IO(Z)	IO(Z)	-	-
165	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
D8	M1DQ20	M0DQ52	-	1.5V/-
	IO(Z)	IO(Z)	-	-
166	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
A8	M1DQ21	M0DQ53	-	1.5V/-
	IO(Z)	IO(Z)	-	-
167	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
D6	M1DQ22	M0DQ54	-	1.5V/-
	IO(Z)	IO(Z)	-	-
168	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
B9	M1DQ23	M0DQ55	-	1.5V/-
	IO(Z)	IO(Z)	-	-
169	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z**
E8	M1DQS2	M0DQS6	-	1.5V/-
	IO(Z**)	IO(Z**)	-	-
170	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z**
E9	M1DQS2#	M0DQS6#	-	1.5V/-
	IO(Z**)	IO(Z**)	-	-
171	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
C7	M1DM2	M0DM6	-	1.5V/-
	O(Z)	O(Z)	-	-
172	DBSC3 channel 1	DBSC3 channel 0	DBSC3 channel 0	P
F10	VDDQ_M1DPLL2	VDDQ_M0DPLL6	VDDQ_M0DPLL6	-
	P	P	P	-
173	DBSC3 channel 1	DBSC3 channel 0	DBSC3 channel 0	P
F9	VSSQ_M1DPLL2	VSSQ_M0DPLL6	VSSQ_M0DPLL6	-
	P	P	P	-

4/5 (DBSC3 channel 1)

Note: * Reserved pins in function 3 should be opened.

DBSC3 channel 1 (32-bit)/DBSC3 channel 0 (64-bit)/DDR3 GPIO (No.174 to 188): Up to 3-Function Multiplexed

Pin state during power-on reset and default pin function are defined by the MD28, MD 27, MD22 and MD17 pins setting, which function cannot be changed after power-on reset by software.

Function	1	2	3	
Mode Pin settings	(MD28, MD27, MD22, MD17) = (0/1, 1, 1, 1)	= (0, 1, 1, 0)	= (1, 1, 1, 0)	
No.	Module			During POR
Pin No.	Pin Name			V/|IOH|
	I/O			Pull-up
174	DBSC3 channel 1	DBSC3 channel 0	DBSC3 channel 0	P
G8	M1VREFDQ1	M0VREFDQ3	M0VREFDQ3	-
	P	P	P	-
175	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
B3	M1DQ24	M0DQ56	-	1.5V/-
	IO(Z)	IO(Z)	-	-
176	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
D5	M1DQ25	M0DQ57	-	1.5V/-
	IO(Z)	IO(Z)	-	-
177	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
C4	M1DQ26	M0DQ58	-	1.5V/-
	IO(Z)	IO(Z)	-	-
178	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
C5	M1DQ27	M0DQ59	-	1.5V/-
	IO(Z)	IO(Z)	-	-
179	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
A5	M1DQ28	M0DQ60	-	1.5V/-
	IO(Z)	IO(Z)	-	-
180	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
A3	M1DQ29	M0DQ61	-	1.5V/-
	IO(Z)	IO(Z)	-	-
181	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
B5	M1DQ30	M0DQ62	-	1.5V/-
	IO(Z)	IO(Z)	-	-
182	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
A2	M1DQ31	M0DQ63	-	1.5V/-
	IO(Z)	IO(Z)	-	-
183	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z**
E7	M1DQS3	M0DQS7	-	1.5V/-
	IO(Z**)	IO(Z**)	-	-
184	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z**
E6	M1DQS3#	M0DQS7#	-	1.5V/-
	IO(Z**)	IO(Z**)	-	-
185	DBSC3 channel 1	DBSC3 channel 0	Reserved*	Z
A4	M1DM3	M0DM7	-	1.5V/-
	O(Z)	O(Z)	-	-
186	DBSC3 channel 1	DBSC3 channel 0	DBSC3 channel 0	P
G10	VDDQ_M1DPLL3	VDDQ_M0DPLL7	VDDQ_M0DPLL7	-
	P	P	P	-
187	DBSC3 channel 1	DBSC3 channel 0	DBSC3 channel 0	P
G9	VSSQ_M1DPLL3	VSSQ_M0DPLL7	VSSQ_M0DPLL7	-
	P	P	P	-
188	DBSC3 channel 1	DBSC3 channel 0	DBSC3 channel 0	P
G6	VDDQ_M1BKUP	VDDQ_M1BKUP	VDDQ_M1BKUP	-
	P	P	P	-

5/5 (DBSC3 channel 1)

Note: * Reserved pins in function 3 should be opened.

Note for DBSC3 channel 1 DQS/DQS# states. ** (No.142/143, 156/157, 169/170, 183/184):

The drivers output states are both high-impedance (Z), and the internal circuit controls pin levels as low-level for the M1DQSx pins and high-level for the M1DQSx# pins respectively.

CPG, RESET, SYSTEM, AVS, POWER ISO and GPIO (No.189 to 207): Up to 2-Function Multiplexed

	Function 1	GPIO	
No.	Module		During POR
Pin No.	Pin Name		V/|IOH|
	I/O		Pull-up
189	CPG	-	I
AL12	EXTAL	-	1.8V/-
	I	-	-
190	CPG	-	O
AL13	XTAL	-	1.8V/-
	O	-	-
191	CPG	-	I
AF12	EXREFIN*1	-	1.8V/-
	I	-	-
192	PLL	-	P
F16	VDD_CPGPLL1	-	-
	P	-	-
193	PLL	-	P
F15	VSS_CPGPLL1	-	-
	P	-	-
194	PLL	-	P
H15	VDD_CPGPLL2	-	-
	P	-	-
195	PLL	-	P
G15	VSS_CPGPLL2	-	-
	P	-	-
196	PLL	-	P
N4	VDD_CPGPLL0	-	-
	P	-	-
197	PLL	-	P
N5	VSS_CPGPLL0	-	-
	P	-	-
198	PLL	-	P
N7	VDD_CPGPLL3	-	-
	P	-	-
199	PLL	-	P
N6	VSS_CPGPLL3	-	-
	P	-	-
200	RESET	-	I(S)
AF16	PRESET#	-	1.8V/-
	I(S)	-	-
201	RESET	-	L
AJ1	PRESETOUT#	-	3.3V/4mA
	O(L to H)	-	-
202	SYSTEM	-	I(S)
AE15	MPMD0	-	1.8V/-
	I(S)	-	-
203	SYSTEM	-	I(S)
AJ14	MPMD1	-	1.8V/-
	I(S)	-	-
204	SYSTEM	-	I(S)
AE13	BSMODE	-	1.8V/-
	I(S)	-	-
205	AVS		L
AA25	AVS1	GP5_24	3.3V/4mA
	O(H/L)*2	IO	Off
206	AVS		L
AB26	AVS2	GP5_25	3.3V/4mA
	O(H/L)*2	IO	Off
207	POWER ISO	-	P
AE16	VCCQ_ISO	-	-
	P	-	-

Notes: 1. (No.191): Must be fixed to VSS.
2. (No.205 and 206): Output value of the AVS[2:1] pins depends on each product.

LBSC, MSIOF, VIN, SCIFB, SCIF, IIC, I2C, TMU, EtherAVB and GPIO (No.208 to 223): Up to 10-Function Multiplexed

Default pin function (function 1 or GPIO) after power-on reset is defined by MD[3:1] pins setting.

Function	1	2	3	4	5	6	7	8	9	10	GPIO	
MD[3:1]	= 000										≠ 000	
No.	Module											During POR
Pin No.	Pin Name											V/|IOH|
	I/O											Pull-up
208	LBSC	MSIOF3	VIN3	VIN0	VIN0	Reserved	Reserved	-	-	-		I(GPIO)
AF9	D0	MSIOF3_SCK_B	VI3_DATA0	VI0_G4	VI0_G4_B	-	-	-	-	-	GP0_0	3.3V/8mA
	IO(I)	IO	I	I	I	-	-	-	-	-	IO(I)	On
209	LBSC	MSIOF3	VIN3	VIN0	VIN0	Reserved	Reserved	-	-	-		I(GPIO)
AG9	D1	MSIOF3_SYNC_B	VI3_DATA1	VI0_G5	VI0_G5_B	-	-	-	-	-	GP0_1	3.3V/8mA
	IO(I)	IO	I	I	I	-	-	-	-	-	IO(I)	On
210	LBSC	MSIOF3	VIN3	VIN0	VIN0	Reserved	Reserved	-	-	-		I(GPIO)
AH9	D2	MSIOF3_RXD_B	VI3_DATA2	VI0_G6	VI0_G6_B	-	-	-	-	-	GP0_2	3.3V/8mA
	IO(I)	I	I	I	I	-	-	-	-	-	IO(I)	On
211	LBSC	MSIOF3	VIN3	VIN0	VIN0	Reserved	Reserved	-	-	-		I(GPIO)
AJ9	D3	MSIOF3_TXD_B	VI3_DATA3	VI0_G7	VI0_G7_B	-	-	-	-	-	GP0_3	3.3V/8mA
	IO(I)	O	I	I	I	-	-	-	-	-	IO(I)	On
212	LBSC	SCIFB1	SCIFB0	VIN3	VIN0	VIN0	SCIF0	Reserved	Reserved	-		I(GPIO)
AK9	D4	SCIFB1_RXD_F	SCIFB0_RXD_C	VI3_DATA4	VI0_R0	VI0_R0_B	RX0_B	-	-	-	GP0_4	3.3V/8mA
	IO(I)	I	I	I	I	I	I	-	-	-	IO(I)	On
213	LBSC	SCIFB1	SCIFB0	VIN3	VIN0	VIN0	SCIF0	Reserved	Reserved	-		I(GPIO)
AL9	D5	SCIFB1_TXD_F	SCIFB0_TXD_C	VI3_DATA5	VI0_R1	VI0_R1_B	TX0_B	-	-	-	GP0_5	3.3V/8mA
	IO(I)	O	O	I	I	I	O	-	-	-	IO(I)	On
214	LBSC	IIC2	VIN3	VIN0	VIN0	I2C2	-	Reserved	Reserved	-		I(GPIO)
AF8	D6	IIC2_SCL_C	VI3_DATA6	VI0_R2	VI0_R2_B	I2C2_SCL_C	-	-	-	-	GP0_6	3.3V/8mA
	IO(I)	IO	I	I	I	IO	-	-	-	-	IO(I)	On
215	LBSC	Reserved	IIC2	VIN3	VIN0	VIN0	I2C2	TMU	Reserved	Reserved		I(GPIO)
AG8	D7	-	IIC2_SDA_C	VI3_DATA7	VI0_R3	VI0_R3_B	I2C2_SDA_C	TCLK1	-	-	GP0_7	3.3V/8mA
	IO(I)	-	IO	I	I	I	IO	I	-	-	IO(I)	On
216	LBSC	SCIFA1	EtherAVB	Reserved	VIN0	VIN0	VIN2	Reserved	Reserved	-		I(GPIO)
AH8	D8	SCIFA1_SCK_C	AVB_TXD0	-	VI0_G0	VI0_G0_B	VI2_DATA0/VI2_B0	-	-	-	GP0_8	3.3V/8mA
	IO(I)	O	O	-	I	I	I	-	-	-	IO(I)	On
217	LBSC	SCIFA1	EtherAVB	Reserved	VIN0	VIN0	VIN2	Reserved	Reserved	-		I(GPIO)
AJ8	D9	SCIFA1_RXD_C	AVB_TXD1	-	VI0_G1	VI0_G1_B	VI2_DATA1/VI2_B1	-	-	-	GP0_9	3.3V/8mA
	IO(I)	I	O	-	I	I	I	-	-	-	IO(I)	On
218	LBSC	SCIFA1	EtherAVB	Reserved	VIN0	VIN0	VIN2	Reserved	Reserved	-		I(GPIO)
AK8	D10	SCIFA1_TXD_C	AVB_TXD2	-	VI0_G2	VI0_G2_B	VI2_DATA2/VI2_B2	-	-	-	GP0_10	3.3V/8mA
	IO(I)	O	O	-	I	I	I	-	-	-	IO(I)	On
219	LBSC	SCIFA1	EtherAVB	Reserved	VIN0	VIN0	VIN2	Reserved	Reserved	-		I(GPIO)
AL8	D11	SCIFA1_CTS#_C	AVB_TXD3	-	VI0_G3	VI0_G3_B	VI2_DATA3/VI2_B3	-	-	-	GP0_11	3.3V/8mA
	IO(I)	I	O	-	I	I	I	-	-	-	IO(I)	On
220	LBSC	SCIFA1	EtherAVB	VIN0	VIN0	VIN2	Reserved	Reserved	-	-		I(GPIO)
AF7	D12	SCIFA1_RTS#_C	AVB_TXD4	VI0_HSYNC#	VI0_HSYNC#_B	VI2_DATA4/VI2_B4	-	-	-	-	GP0_12	3.3V/8mA
	IO(I)	O	O	I	I	I	-	-	-	-	IO(I)	On
221	LBSC	EtherAVB	VIN0	VIN0	VIN2	Reserved	Reserved	-	-	-		I(GPIO)
AG7	D13	AVB_TXD5	VI0_VSYNC#	VI0_VSYNC#_B	VI2_DATA5/VI2_B5	-	-	-	-	-	GP0_13	3.3V/8mA
	IO(I)	O	I	I	I	-	-	-	-	-	IO(I)	On
222	LBSC	SCIFB1	EtherAVB	SCIF1	VIN0	VIN0	VIN2	Reserved	Reserved	-		I(GPIO)
AJ7	D14	SCIFB1_RXD_C	AVB_TXD6	RX1_B	VI0_CLKENB	VI0_CLKENB_B	VI2_DATA6/VI2_B6	-	-	-	GP0_14	3.3V/8mA
	IO(I)	I	O	I	I	I	I	-	-	-	IO(I)	On
223	LBSC	SCIFB1	EtherAVB	SCIF1	VIN0	VIN0	VIN2	Reserved	Reserved	-		I(GPIO)
AK7	D15	SCIFB1_TXD_C	AVB_TXD7	TX1_B	VI0_FIELD	VI0_FIELD_B	VI2_DATA7/VI2_B7	-	-	-	GP0_15	3.3V/8mA
	IO(I)	O	O	O	I	I	I	-	-	-	IO(I)	On

LBSC, PWM, MSIOF, TPU, SCIFA, ADG, SSI, VIN, SCIFB, SCIF and GPIO (No.224 to 237): Up to 11-Function Multiplexed and Mode Pins assigned (No.224 to 231)

Default pin function (function 1 or GPIO) after power-on reset is defined by MD[3:1] pins setting.

Function	1	2	3	4	5	6	7	8	9	10	GPIO	
MD[3:1]	= 000										≠ 000	
No.	Module											During POR
Pin No.	Pin Name											V/|IOH|
Mode Pin	I/O											Pull-up
224	LBSC	PWM3	Reserved	Reserved	-	-	-	-	-	-		I(Mode Pin)
AL7	A0	PWM3	-	-	-	-	-	-	-	-	GP0_16	3.3V/8mA
MD28	O(L)	O	-	-	-	-	-	-	-	-	IO(I)	Off
225	LBSC	PWM4	Reserved	Reserved	-	-	-	-	-	-		I(Mode Pin)
AG6	A1	PWM4	-	-	-	-	-	-	-	-	GP0_17	3.3V/8mA
MD27	O(L)	O	-	-	-	-	-	-	-	-	IO(I)	Off
226	LBSC	PWM5	MSIOF1	Reserved	Reserved	-	-	-	-	-		I(Mode Pin)
AH6	A2	PWM5	MSIOF1_SS1_B	-	-	-	-	-	-	-	GP0_18	3.3V/8mA
MD26	O(L)	O	O	-	-	-	-	-	-	-	IO(I)	Off
227	LBSC	PWM6	MSIOF1	Reserved	Reserved	-	-	-	-	-		I(Mode Pin)
AJ6	A3	PWM6	MSIOF1_SS2_B	-	-	-	-	-	-	-	GP0_19	3.3V/8mA
MD25	O(L)	O	O	-	-	-	-	-	-	-	IO(I)	Off
228	LBSC	MSIOF1	TPU	Reserved	Reserved	-	-	-	-	-		I(GPIO)
AL6	A4	MSIOF1_TXD_B	TPU0TO0	-	-	-	-	-	-	-	GP0_20	3.3V/8mA
MD24	O(L)	O	O	-	-	-	-	-	-	-	IO(I)	Off
229	LBSC	SCIFA1	TPU	Reserved	Reserved	-	-	-	-	-		I(GPIO)
AH5	A5	SCIFA1_TXD_B	TPU0TO1	-	-	-	-	-	-	-	GP0_21	3.3V/8mA
MD23	O(L)	O	O	-	-	-	-	-	-	-	IO(I)	Off
230	LBSC	SCIFA1	TPU	Reserved	Reserved	-	-	-	-	-		I(GPIO)
AJ5	A6	SCIFA1_RTS#_B	TPU0TO2	-	-	-	-	-	-	-	GP0_22	3.3V/8mA
MD22	O(L)	O	O	-	-	-	-	-	-	-	IO(I)	Off
231	LBSC	SCIFA1	ADG	TPU	Reserved	Reserved	-	-	-	-		I(GPIO)
AK5	A7	SCIFA1_SCK_B	AUDIO_CLKOUT_B	TPU0TO3	-	-	-	-	-	-	GP0_23	3.3V/8mA
MD21	O(L)	O	O	O	-	-	-	-	-	-	IO(I)	Off
232	LBSC	SCIFA1	SSI	VIN0	VIN0	SCIFB2	SCIF2	VIN2	Reserved	Reserved		I(GPIO)
AL5	A8	SCIFA1_RXD_B	SSI_SCK5_B	VI0_R4	VI0_R4_B	SCIFB2_RXD_C	RX2_B	VI2_DATA0_B/VI2_B0_B	-	-	GP0_24	3.3V/8mA
	O(L)	I	IO	I	I	I	I	I	-	-	IO(I)	On
233	LBSC	SCIFA1	SSI	VIN0	VIN0	SCIFB2	SCIF2	VIN2	Reserved	Reserved		I(GPIO)
AJ4	A9	SCIFA1_CTS#_B	SSI_WS5_B	VI0_R5	VI0_R5_B	SCIFB2_TXD_C	TX2_B	VI2_DATA1_B/VI2_B1_B	-	-	GP0_25	3.3V/8mA
	O(L)	I	IO	I	I	O	O	I	-	-	IO(I)	On
234	LBSC	SSI	MSIOF2	VIN0	VIN0	VIN2	Reserved	Reserved	-	-		I(GPIO)
AK4	A10	SSI_SDATA5_B	MSIOF2_SYNC	VI0_R6	VI0_R6_B	VI2_DATA2_B/VI2_B2_B	-	-	-	-	GP0_26	3.3V/8mA
	O(L)	IO	IO	I	I	I		-	-	-	IO(I)	On
235	LBSC	SCIFB2	MSIOF2	VIN1	VIN1	VIN2	VIN2	Reserved	Reserved	-		I(GPIO)
AL4	A11	SCIFB2_CTS#_B	MSIOF2_SCK	VI1_R0	VI1_R0_B	VI2_G0	VI2_DATA3_B/VI2_B3_B	-	-	-	GP0_27	3.3V/8mA
	O(L)	I	IO	I	I	I	I	-	-	-	IO(I)	On
236	LBSC	SCIFB2	MSIOF2	VIN1	VIN1	VIN2	VIN2	Reserved	Reserved	-		I(GPIO)
AK3	A12	SCIFB2_RXD_B	MSIOF2_TXD	VI1_R1	VI1_R1_B	VI2_G1	VI2_DATA4_B/VI2_B4_B	-	-	-	GP0_28	3.3V/8mA
	O(L)	I	O	I	I	I	I	-	-	-	IO(I)	On
237	LBSC	SCIFB2	LBSC	MSIOF2	VIN1	VIN1	VIN2	VIN2	Reserved	Reserved		I(GPIO)
AL3	A13	SCIFB2_RTS#_B	EX_WAIT2	MSIOF2_RXD	VI1_R2	VI1_R2_B	VI2_G2	VI2_DATA5_B/VI2_B5_B	-	-	GP0_29	3.3V/8mA
	O(L)	O	I	I	I	I	I	I	-	-	IO(I)	On

LBSC, PWM, MSIOF, TPU, SCIFA, ADG, SSI, VIN, SCIFB, SCIF and GPIO (No.238 to 255): Up to 9-Function Multiplexed and Mode Pin Assigned (No.238 to 243)

Default pin function (function 1 or GPIO) after power-on reset is defined by MD[3:1] pins setting except for No.253 to 255.

Function	1	2	3	4	5	6	7	8	GPIO	
MD[3:1]	= 000								≠ 000	
No.	Module									During POR
Pin No.	Pin Name									V/|IOH|
Mode Pin	I/O									Pull-up
238	LBSC	SCIFB2	LBSC	MSIOF2	Reserved	Reserved	-	-		I(Mode Pin)
AL2	A14	SCIFB2_TXD_B	ATACS11#	MSIOF2_SS1	-	-	-	-	GP0_30	3.3V/8mA
MD20	O(L)	O	O	O	-	-	-	-	IO(I)	Off
239	LBSC	SCIFB2	LBSC	MSIOF2	Reserved	Reserved	-	-		I(Mode Pin)
AH3	A15	SCIFB2_SCK_B	ATARD1#	MSIOF2_SS2	-	-	-	-	GP0_31	3.3V/8mA
MD19	O(L)	O	O	O	-	-	-	-	IO(I)	Off
240	LBSC	LBSC	Reserved	Reserved	-	-	-	-		I(Mode Pin)
AG1	A16	ATAWR1#	-	-	-	-	-	-	GP1_0	3.3V/8mA
MD18	O(L)	O	-	-	-	-	-	-	IO(I)	Off
241	LBSC	Reserved	LBSC	Reserved	Reserved	-	-	-		I(Mode Pin)
AG2	A17	-	ATADIR1#	-	-	-	-	-	GP1_1	3.3V/8mA
MD17	O(L)	-	O	-	-	-	-	-	IO(I)	Off
242	LBSC	Reserved	LBSC	Reserved	Reserved	-	-	-		I(Mode Pin)
AG3	A18	-	ATAG1#	-	-	-	-	-	GP1_2	3.3V/8mA
MD15	O(L)	-	O	-	-	-	-	-	IO(I)	Off
243	LBSC	Reserved	LBSC	LBSC	Reserved	Reserved	-	-		I(Mode Pin)
AG4	A19	-	ATACS01#	EX_WAIT0_B	-	-	-	-	GP1_3	3.3V/8mA
MD14	O(L)	-	O	I	-	-	-	-	IO(I)	Off
244	LBSC	QSPI*[1]	VIN1	VIN1	VIN2	Reserved	Reserved	-		I(GPIO)
AF1	A20	SPCLK	VI1_R3	VI1_R3_B	VI2_G4	-	-	-	GP1_4	3.3V/8mA
	O(L)	IO	I	I	I	-	-	-	IO(I)	On
245	LBSC	QSPI*[1]	VIN1	VIN1	VIN2	Reserved	Reserved	-		I(GPIO)
AF2	A21	MOSI/IO0	VI1_R4	VI1_R4_B	VI2_G5	-	-	-	GP1_5	3.3V/8mA
	O(L)	IO	I	I	I	-	-	-	IO(I)	On
246	LBSC	QSPI*[1]	VIN1	VIN1	VIN2	Reserved	Reserved	-		I(GPIO)
AF3	A22	MISO/IO1	VI1_R5	VI1_R5_B	VI2_G6	-	-	-	GP1_6	3.3V/8mA
	O(L)	IO	I	I	I	-	-	-	IO(I)	On
247	LBSC	QSPI*[1]	VIN1	VIN1	VIN2	Reserved	Reserved	-		I(GPIO)
AF4	A23	IO2	VI1_G7	VI1_G7_B	VI2_G7	-	-	-	GP1_7	3.3V/8mA
	O(L)	IO	I	I	I	-	-	-	IO(I)	On
248	LBSC	QSPI*[1]	VIN1	VIN1	VIN2	VIN2	Reserved	Reserved		I(GPIO)
AF5	A24	IO3	VI1_R7	VI1_R7_B	VI2_CLKENB	VI2_CLKENB_B	-	-	GP1_8	3.3V/8mA
	O(L)	IO	I	I	I	I	-	-	IO(I)	On
249	LBSC	QSPI*[1]	VIN1	VIN1	VIN2	VIN2	-	-		I(GPIO)
AE6	A25	SSL	VI1_G6	VI1_G6_B	VI2_FIELD	VI2_FIELD_B	-	-	GP1_9	3.3V/8mA
	O	IO	I	I	I	I	-	-	IO(I)	On
250	LBSC	-	-	-	-	-	-	-	-	O
AE1	CLKOUT	-	-	-	-	-	-	-	-	3.3V/8mA
	O	-	-	-	-	-	-	-	-	-
251	LBSC	VIN1	VIN1	VIN2	MSIOF0	-	-	-		I(GPIO)
AD1	CS0#	VI1_R6	VI1_R6_B	VI2_G3	MSIOF0_SS2_B	-	-	-	GP1_10	3.3V/4mA
	O(H)	I	I	I	O	-	-	-	IO(I)	On
252	LBSC	Reserved	VIN0	VIN0	VIN2	VIN2	-	-		I(GPIO)
AJ2	CS1#/A26	-	VI0_R7	VI0_R7_B	VI2_CLK	VI2_CLK_B	-	-	GP1_11	3.3V/4mA
	O(H or L)*[1]	-	I	I	I	I	-	-	IO(I)	On
253*[2]	LBSC	HSCIF1	VIN1	VIN1	VIN2	HSCIF0	MSIOF0	-		I(GPIO)
AC1	EX_CS0#	HRX1_B	VI1_G5	VI1_G5_B	VI2_R0	HTX0_B	MSIOF0_SS1_B	-	GP1_12	3.3V/4mA
	O	I	I	I	I	O	O	-	IO(I)	On
254*[2]	LBSC	Reserved	HSCIF1	VIN1	VIN1	VIN2	-	-		I(GPIO)
AC2	EX_CS1#	-	HCTS1#_B	VI1_FIELD	VI1_FIELD_B	VI2_R1	-	-	GP1_13	3.3V/4mA
	O	-	IO	I	I	I	-	-	IO(I)	On
255*[2]	LBSC	Reserved	HSCIF1	VIN3	VIN1	VIN1	VIN2	-		I(GPIO)
AC3	EX_CS2#	-	HRTS1#_B	VI3_CLKENB	VI1_G0	VI1_G0_B	VI2_R2	-	GP1_14	3.3V/4mA
	O	-	IO	I	I	I	I	-	IO(I)	On

Notes: 1. (No.252): Output value of CS1#/A26 pin after power-on reset is 'H' when MD4 = 0, 'L' when MD4 = 1.

2. (No.253 to 255): These pins are set for GPIO after power-on reset even if MD[3:1] = 000. For details, refer to GPSR1 register in section 5, Pin Function Controller (PFC).

LBSC, PWM, MSIOF, TPU, SCIFA, ADG, SSI, VIN, SCIFB, SCIF and GPIO (No.256 to 270): Up to 9-Function Multiplexed and Mode Pin Assigned (No.259 and 260)

Default pin function (function 1 or GPIO) after power-on reset is defined by MD[3:1] pins setting except for No.256 to 258, 261 and No.265 to 270.

Function	1	2	3	4	5	6	7	8	9	10	GPIO	
MD[3:1]	= 000										≠ 000	
No.	Module											During POR
Pin No.	Pin Name											V/|IOH|
Mode Pin	I/O											Pull-up
256*	LBSC	Reserved	VIN3	VIN1	VIN1	VIN2	-	-	-	-		I(GPIO)
AC4	EX_CS3#	-	VI3_FIELD	VI1_G1	VI1_G1_B	VI2_R3	-	-	-	-	GP1_15	3.3V/4mA
	O	-	I	I	I	I	-	-	-	-	IO(I)	On
257*	LBSC	MSIOF1	VIN3	VIN2	IIC1	VIN2	Reserved	I2C1	-	-		I(GPIO)
AE3	EX_CS4#	MSIOF1_SCK_B	VI3_HSYNC#	VI2_HSYNC#	IIC1_SCL	VI2_HSYNC#_B	-	I2C1_SCL	-	-	GP1_16	3.3V/8mA
	O	IO	I	I	IO	I	-	IO	-	-	IO(I)	On
258*	LBSC	RCAN0	MSIOF1	VIN3	VIN1	VIN1	VIN2	IIC1	Reserved	I2C1		I(GPIO)
AE4	EX_CS5#	CAN0_RX	MSIOF1_RXD_B	VI3_VSYNC#	VI1_G2	VI1_G2_B	VI2_R4	IIC1_SDA	-	I2C1_SDA	GP1_17	3.3V/4mA
	O	I	I	I	I	I	I	IO	-	IO	IO(I)	On
259	LBSC	Reserved	HSCIF1	RCAN1	LBSC	Reserved	-	-	-	-		I(Mode Pin)
AE5	BS#	-	HTX1_B	CAN1_TX	DRACK0	-	-	-	-	-	GP1_18	3.3V/4mA
MD13	O(H)	-	O	O	O	-	-	-	-	-	IO(I)	Off
260	LBSC	RCAN0	SCIFA0	-	-	-	-	-	-	-		I(Mode Pin)
AD3	RD#	CAN0_TX	SCIFA0_SCK_B	-	-	-	-	-	-	-	GP1_19	3.3V/4mA
MD16	O(H)	O	O	-	-	-	-	-	-	-	IO(I)	Off
261*	LBSC	VIN1	VIN1	VIN2	SCIFA0	Reserved	-	-	-	-		I(GPIO)
AD2	RD/WR#	VI1_G3	VI1_G3_B	VI2_R5	SCIFA0_RXD_B	-	-	-	-	-	GP1_20	3.3V/4mA
	O	I	I	I	I	-	-	-	-	-	IO(I)	On
262	LBSC	Reserved	RCAN	VIN2	SCIFA0	VIN2	-	-	-	-		I(GPIO)
AH1	WE0#	-	CAN_CLK	VI2_VSYNC#	SCIFA0_TXD_B	VI2_VSYNC#_B	-	-	-	-	GP1_21	3.3V/4mA
	O(H)	-	I	I	O	I	-	-	-	-	IO(I)	On
263	LBSC	Reserved	RCAN1	VIN1	VIN1	VIN2	SCIFA0	Reserved	-	-		I(GPIO)
AH2	WE1#	-	CAN1_RX	VI1_G4	VI1_G4_B	VI2_R6	SCIFA0_CTS#_B	-	-	-	GP1_22	3.3V/4mA
	O(H)	-	I	I	I	I	I	-	-	-	IO(I)	On
264	LBSC	INTC	Reserved	VIN3	SCIFA0	HSCIF0	MSIOF0	-	-	-		I(GPIO)
AK1	EX_WAIT0	IRQ3	-	VI3_CLK	SCIFA0_RTS#_B	HRX0_B	MSIOF0_SCK_B	-	-	-	GP1_23	3.3V/8mA
	I(I)	I	-	I	O	I	IO	-	-	-	IO(I)	On
265*	LBSC	VIN1	VIN1	VIN2	SSI	SSI	-	-	-	-		I(GPIO)
AC5	DREQ0	VI1_HSYNC#	VI1_HSYNC#_B	VI2_R7	SSI_SCK78_C	SSI_WS78_B	-	-	-	-	GP1_24	3.3V/4mA
	I	I	I	I	IO	IO	-	-	-	-	IO(I)	On
266*	LBSC	INTC	Reserved	SSI	VIN1	VIN1	SSI	-	-	-		I(GPIO)
AC6	DACK0	IRQ0	-	SSI_SCK6_B	VI1_VSYNC#	VI1_VSYNC#_B	SSI_WS78_C	-	-	-	GP1_25	3.3V/4mA
	O	I	-	IO	I	I	IO	-	-	-	IO(I)	On
267*	LBSC	VIN1	VIN1	SSI	SSI	-	-	-	-	-		I(GPIO)
AD5	DREQ1	VI1_CLKENB	VI1_CLKENB_B	SSI_SDATA7_C	SSI_SCK78_B	-	-	-	-	-	GP1_26	3.3V/4mA
	I	I	I	IO	IO	-	-	-	-	-	IO(I)	On
268*	LBSC	INTC	Reserved	SSI	SSI	-	-	-	-	-		I(GPIO)
AD4	DACK1	IRQ1	-	SSI_WS6_B	SSI_SDATA8_C	-	-	-	-	-	GP1_27	3.3V/4mA
	O	I	-	IO	IO	-	-	-	-	-	IO(I)	On
269*	LBSC	HSCIF1	HSCIF0	MSIOF0	-	-	-	-	-	-		I(GPIO)
AD7	DREQ2	HSCK1_B	HCTS0#_B	MSIOF0_TXD_B	-	-	-	-	-	-	GP1_28	3.3V/4mA
	I	IO	IO	O	-	-	-	-	-	-	IO(I)	On
270*	LBSC	INTC	Reserved	SSI	HSCIF0	MSIOF0	-	-	-	-		I(GPIO)
AD6	DACK2	IRQ2	-	SSI_SDATA6_B	HRTS0#_B	MSIOF0_RXD_B	-	-	-	-	GP1_29	3.3V/4mA
	O	I	-	IO	IO	I	-	-	-	-	IO(I)	On

Note: * (No.256 to 258, 261 and No.265 to 270): These pins are set for GPIO after power-on reset even if MD[3:1] = 000. For details, refer to GPSR1 register in section 5, Pin Function Controller (PFC).

EtherMAC, IIC, I2C, SCIFB, SCIF, HSCIF, SCIFA and GPIO (No.271 to 285): Up to 10-Function Multiplexed and Mode Pin Assigned (No.278 to 284)

These pins are set for GPIO after power-on reset. For details, refer to GPSR2 and GPSR5 registers in section 5, Pin Function Controller (PFC).

Function	1	2	3	4	5	6	7	8	9	GPIO	
No.	Module										During POR
Pin No.	Pin Name										V/|IOH|
Mode Pin	I/O										Pull-up
271	EtherMAC	Reserved	Reserved	Reserved	Reserved	IIC2	I2C2	-	-		I(GPIO)
AH11	ETH_CRS_DV	-	-	-	-	IIC2_SCL_E	I2C2_SCL_E	-	-	GP2_18	3.3V/4mA
	I	-	-	-	-	IO	IO	-	-	IO(I)	On
272	EtherMAC	Reserved	Reserved	Reserved	Reserved	IIC2	I2C2	-	-		I(GPIO)
AG11	ETH_RX_ER	-	-	-	-	IIC2_SDA_E	I2C2_SDA_E	-	-	GP2_19	3.3V/4mA
	I	-	-	-	-	IO	IO	-	-	IO(I)	On
273	EtherMAC	Reserved	Reserved	Reserved	Reserved	SCIFB1	SCIF1	-	-		I(GPIO)
AF11	ETH_RXD0	-	-	-	-	SCIFB1_SCK_G	SCK1_E	-	-	GP2_20	3.3V/4mA
	I	-	-	-	-	O	IO	-	-	IO(I)	On
274	EtherMAC	Reserved	HSCIF0	Reserved	Reserved	Reserved	SCIFB1	SCIF1	-		I(GPIO)
AE11	ETH_RXD1	-	HRX0_E	-	-	-	SCIFB1_RXD_G	RX1_E	-	GP2_21	3.3V/4mA
	I	-	I	-	-	-	I	I	-	IO(I)	On
275	EtherMAC	Reserved	HSCIF0	Reserved	SCIFB1	SCIF1	-	-	-		I(GPIO)
AK10	ETH_LINK	-	HTX0_E	-	SCIFB1_TXD_G	TX1_E	-	-	-	GP2_22	3.3V/4mA
	I	-	O	-	O	O	-	-	-	IO(I)	On
276	EtherMAC	Reserved	HSCIF0	Reserved	HSCIF0	-	-	-	-		I(GPIO)
AL10	ETH_REF_CLK	-	HCTS0#_E	-	HRX0_F	-	-	-	-	GP2_23	3.3V/4mA
	I	-	IO	-	I	-	-	-	-	IO(I)	On
277	EtherMAC	Reserved	HSCIF0	Reserved	HSCIF0	-	-	-	-		I(GPIO)
AJ10	ETH_MDIO	-	HRTS0#_E	-	HCTS0#_F	-	-	-	-	GP2_24	3.3V/4mA
	IO	-	IO	-	IO	-	-	-	-	IO(I)	On
278	EtherMAC	Reserved	HSCIF0	Reserved	Reserved	-	-	-	-		I(Mode Pin)
AH10	ETH_TXD1	-	HTX0_F	-	-	-	-	-	-	GP2_25	3.3V/4mA
MD12	O	-	O	-	-	-	-	-	-	IO(I)	Off
279	EtherMAC	Reserved	Reserved	HSCIF0	-	-	-	-	-		I(Mode Pin)
AG10	ETH_TX_EN	-	-	HRTS0#_F	-	-	-	-	-	GP2_26	3.3V/4mA
MD11	O	-	-	IO	-	-	-	-	-	IO(I)	Off
280	EtherMAC	Reserved	Reserved	-	-	-	-	-	-		I(Mode Pin)
AF10	ETH_MAGIC	-	-	-	-	-	-	-	-	GP2_27	3.3V/4mA
MD10	O	-	-	-	-	-	-	-	-	IO(I)	Off
281	EtherMAC	Reserved	Reserved	Reserved	Reserved	-	-	-	-		I(Mode Pin)
AE10	ETH_TXD0	-	-	-	-	-	-	-	-	GP2_28	3.3V/4mA
MD9	O	-	-	-	-	-	-	-	-	IO(I)	Off
282	EtherMAC	Reserved	Reserved	Reserved	Reserved	-	-	-	-		I(Mode Pin)
AE9	ETH_MDC	-	-	-		-	-	-	-	GP2_29	3.3V/4mA
MD8	O	-	-	-	-	-	-	-	-	IO(I)	Off
283	PWM0	SCIFA2	Reserved	Reserved	Reserved	-	-	-	-		I(Mode Pin)
AE12	PWM0	SCIFA2_SCK_C	-	-	-	-	-	-	-	GP5_29	3.3V/4mA
MD7	O	O	-	-	-	-	-	-	-	IO(I)	Off
284	PWM1	SCIFA2	Reserved	Reserved	Reserved	Reserved	-	-	-		I(Mode Pin)
AK11	PWM1	SCIFA2_TXD_C	-	-	-	-	-	-	-	GP5_30	3.3V/4mA
MD6	O	O	-	-	-	-	-	-	-	IO(I)	Off
285	PWM2	Reserved	SCIFA2	Reserved	Reserved	-	-	-	-		I(GPIO)
AJ11	PWM2	-	SCIFA2_RXD_C	-	-	-	-	-	-	GP5_31	3.3V/4mA
	O	-	I	-	-	-	-	-	-	IO(I)	On

INTC and Debugging Function (No.286 to 292): Single Function

	Function 1	
No.	**Module**	**During POR**
Pin No.	**Pin Name**	**V/|IOH|**
	I/O	**Pull-up**
286	INTC	I(S)
AG12	NMI	1.8V/-
	I(S)	-
287	DBG	I
AG16	TRST#	1.8V/-
	I	On
288	DBG	I
AE14	TCK	1.8V/-
	I	On
289	DBG	I
AF14	TMS	1.8V/4mA
	IO(I)	On
290	DBG	I
AH14	TDI	1.8V/-
	I	On
291	DBG	Z
AH12	TDO	1.8V/8mA
	O(Z)	-
292	DBG	I
AF13	ACK	1.8V/4mA
	IO(I)	On(pull-down)

Note: For details of debugging function, refer to section 62, CoreSight.

DU_LVDS0, DU_LVDS1 and GPIO (No.293 to 318): Up to 2-Function Multiplexed

These pins are set for Function 1 except for No.303.

	Function 1	GPIO	
No.	Module		During POR
Pin No.	Pin Name		V/|IOH|
	I/O		Pull-up
293	DU_LVDS0	-	Z
AG17	DU_LVDS0_CLK_P	-	1.8V/-
	O(Z)	-	-
294	DU_LVDS0	-	Z
AG18	DU_LVDS0_CLK_N	-	1.8V/-
	O(Z)	-	-
295	DU_LVDS0	-	Z
AJ18	DU_LVDS0_CH0_P	-	1.8V/-
	O(Z)	-	-
296	DU_LVDS0	-	Z
AJ19	DU_LVDS0_CH0_N	-	1.8V/-
	O(Z)	-	-
297	DU_LVDS0	-	Z
AG19	DU_LVDS0_CH1_P	-	1.8V/-
	O(Z)	-	-
298	DU_LVDS0	-	Z
AG20	DU_LVDS0_CH1_N	-	1.8V/-
	O(Z)	-	-
299	DU_LVDS0	-	Z
AL18	DU_LVDS0_CH2_P	-	1.8V/-
	O(Z)	-	-
300	DU_LVDS0	-	Z
AL17	DU_LVDS0_CH2_N	-	1.8V/-
	O(Z)	-	-
301	DU_LVDS0	-	Z
AJ17	DU_LVDS0_CH3_P	-	1.8V/-
	O(Z)	-	-
302	DU_LVDS0	-	Z
AJ16	DU_LVDS0_CH3_N	-	1.8V/-
	O(Z)	-	-
303*	DU		I(GPIO)
AJ13	DU_DOTCLKIN0	GP5_26	1.8V/4mA
	I	IO(I)	On
304	DU_LVDS0	-	P
AD18	VDDQ_LVDS	-	-
	P	-	-
305	DU_LVDS0	-	P
AE18	VDDQ_LVDS	-	-
	P	-	-
306	DU_LVDS0	-	P
AF18	VDDQ_LVDS	-	-
	P	-	-
307	DU_LVDS0	-	P
AE20	DU_LVDS0_PLL1_VCC	-	-
	P	-	-
308	DU_LVDS0	-	P
AD19	DU_LVDS0_PLL1_VSS	-	-
	P	-	-

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V/|IOH|
	I/O	Pull-up
309	DU_LVDS1	Z
AL19	DU_LVDS1_CLK_P	1.8V/-
	O(Z)	-
310	DU_LVDS1	Z
AL20	DU_LVDS1_CLK_N	1.8V/-
	O(Z)	-
311	DU_LVDS1	Z
AJ23	DU_LVDS1_CH0_P	1.8V/-
	O(Z)	-
312	DU_LVDS1	Z
AJ22	DU_LVDS1_CH0_N	1.8V/-
	O(Z)	-
313	DU_LVDS1	Z
AL21	DU_LVDS1_CH1_P	1.8V/-
	O(Z)	-
314	DU_LVDS1	Z
AL22	DU_LVDS1_CH1_N	1.8V/-
	O(Z)	-
315	DU_LVDS1	Z
AJ20	DU_LVDS1_CH2_P	1.8V/-
	O(Z)	-
316	DU_LVDS1	Z
AJ21	DU_LVDS1_CH2_N	1.8V/-
	O(Z)	-
317	DU_LVDS1	Z
AG22	DU_LVDS1_CH3_P	1.8V/-
	O(Z)	-
318	DU_LVDS1	Z
AG21	DU_LVDS1_CH3_N	1.8V/-
	O(Z)	-

Note: * (No.303): This pin is set for GPIO after power-on reset. For details, refer to GPSR5 register in section5, Pin Function Controller (PFC).

DU, DU_LVDS1, ADG, VIN, LBSC, EtherAVB and GPIO (No.319 to 334): Up to 5-Function Multiplexed

These pins are set for GPIO except for No.320 to 325. For details, refer to GPSR5 and GPSR2 registers in section 5, Pin Function Controller (PFC).

Function	1	2	3	4	GPIO	
No.	Module					During POR
Pin No.	Pin Name					V/|IOH|
	I/O					Pull-up
319	DU	ADG	ADG	-		I(GPIO)
AH13	DU_DOTCLKIN1	AUDIO_CLKC	AUDIO_CLKOUT_C	-	GP5_27	1.8V/4mA
	I	I	O	-	IO(I)	On
320	DU_LVDS1	-	-	-	-	P
AD22	VDDQ_LVDS	-	-	-	-	-
	P	-	-	-	-	-
321	DU_LVDS1	-	-	-	-	P
AE22	VDDQ_LVDS	-	-	-	-	-
	P	-	-	-	-	-
322	DU_LVDS1	-	-	-	-	P
AF22	VDDQ_LVDS	-	-	-	-	-
	P	-	-	-	-	-
323	DU_LVDS1	-	-	-	-	P
AD20	DU_LVDS1_PLL1_VCC	-	-	-	-	-
	P	-	-	-	-	-
324	DU_LVDS1	-	-	-	-	P
AD21	DU_LVDS1_PLL1_VSS	-	-	-	-	-
	P	-	-	-	-	-
325	DU	-	-	-		I(DU)
AJ12	DU_DOTCLKIN2	-	-	-	GP5_28	1.8V/4mA
	I(I)	-	-	-	IO	On
326	VIN0	LBSC	EtherAVB	Reserved		I(GPIO)
Y1	VI0_CLK	ATACS00#	AVB_RXD1	-	GP2_0	3.3V/4mA
	I	O	I	-	IO(I)	On
327	VIN0	LBSC	EtherAVB	Reserved		I(GPIO)
Y6	VI0_DATA0/VI0_B0	ATACS10#	AVB_RXD2	-	GP2_1	3.3V/4mA
	I	O	I	-	IO(I)	On
328	VIN0	LBSC	EtherAVB	Reserved		I(GPIO)
Y5	VI0_DATA1/VI0_B1	ATARD0#	AVB_RXD3	-	GP2_2	3.3V/4mA
	I	O	I	-	IO(I)	On
329	VIN0	LBSC	EtherAVB	-		I(GPIO)
Y4	VI0_DATA2/VI0_B2	ATAWR0#	AVB_RXD4	-	GP2_3	3.3V/4mA
	I	O	I	-	IO(I)	On
330	VIN0	LBSC	EtherAVB	-		I(GPIO)
Y3	VI0_DATA3/VI0_B3	ATADIR0#	AVB_RXD5	-	GP2_4	3.3V/4mA
	I	O	I	-	IO(I)	On
331	VIN0	LBSC	EtherAVB	-		I(GPIO)
W7	VI0_DATA4/VI0_B4	ATAG0#	AVB_RXD6	-	GP2_5	3.3V/4mA
	I	O	I	-	IO(I)	On
332	VIN0	LBSC	EtherAVB	-		I(GPIO)
W6	VI0_DATA5/VI0_B5	EX_WAIT1	AVB_RXD7	-	GP2_6	3.3V/4mA
	I	I	I	-	IO(I)	On
333	VIN0	EtherAVB	Reserved	-		I(GPIO)
AA6	VI0_DATA6/VI0_B6	AVB_RX_ER	-	-	GP2_7	3.3V/4mA
	I	I	-	-	IO(I)	On
334	VIN0	EtherAVB	Reserved	-		I(GPIO)
AA5	VI0_DATA7/VI0_B7	AVB_RX_CLK	-	-	GP2_8	3.3V/4mA
	I	I	-	-	IO(I)	On

VIN, EtherAVB, SCIFA, SDHI0, SCIFB and GPIO (No.335 to 349): Up to 5-Function Multiplexed

These pins are set for GPIO after power-on reset. For details, refer to GPSR2 and GPSR3 registers in section 5, Pin Function Controller (PFC).

Function	1	2	3	4	GPIO	
No.	Module					During POR
Pin No.	Pin Name					V/|IOH|
	I/O					Pull-up
335	VIN1	EtherAVB	Reserved	-		I(GPIO)
AB1	VI1_CLK	AVB_RX_DV	-	-	GP2_9	3.3V/4mA
	I	I	-	-	IO(I)	On
336	VIN1	SCIFA1	EtherAVB	Reserved		I(GPIO)
AA4	VI1_DATA0/VI1_B0	SCIFA1_SCK_D	AVB_CRS	-	GP2_10	3.3V/8mA
	I	O	I	-	IO(I)	On
337	VIN1	SCIFA1	EtherAVB	Reserved		I(GPIO)
AA3	VI1_DATA1/VI1_B1	SCIFA1_RXD_D	AVB_MDC	-	GP2_11	3.3V/8mA
	I	I	O	-	IO(I)	On
338	VIN1	SCIFA1	EtherAVB	Reserved		I(GPIO)
AB7	VI1_DATA2/VI1_B2	SCIFA1_TXD_D	AVB_MDIO	-	GP2_12	3.3V/8mA
	I	O	IO	-	IO(I)	On
339	VIN1	SCIFA1	EtherAVB	-		I(GPIO)
AB6	VI1_DATA3/VI1_B3	SCIFA1_CTS#_D	AVB_GTX_CLK	-	GP2_13	3.3V/8mA
	I	I	O	-	IO(I)	On
340	VIN1	SCIFA1	EtherAVB	Reserved		I(GPIO)
AB4	VI1_DATA4/VI1_B4	SCIFA1_RTS#_D	AVB_MAGIC	-	GP2_14	3.3V/8mA
	I	O	O	-	IO(I)	On
341	VIN1	EtherAVB	-	-		I(GPIO)
AB3	VI1_DATA5/VI1_B5	AVB_PHY_INT	-	-	GP2_15	3.3V/4mA
	I	I	-	-	IO(I)	On
342	VIN1	EtherAVB	-	-		I(GPIO)
AA2	VI1_DATA6/VI1_B6	AVB_GTXREFCLK	-	-	GP2_16	3.3V/4mA
	I	I	-	-	IO(I)	On
343	VIN1	-	-	-		I(GPIO)
AA1	VI1_DATA7/VI1_B7	-	-	-	GP2_17	3.3V/4mA
	I	-	-	-	IO(I)	On
344	SDHI0	VIN1	-	-		I(GPIO)/Z(DBG)*1
V1	SD0_CLK	VI1_DATA0_B/VI1_B0_B	-	-	GP3_0	1.8/3.3V*2/16mA
	O	I	-	-	IO(I)	Off/-*1
345	SDHI0	SCIFB1	VIN1	-		I(GPIO)/I(DBG)*1
V4	SD0_CMD	SCIFB1_SCK_B	VI1_DATA1_B/VI1_B1_B	-	GP3_1	1.8/3.3V*2/16mA
	IO	O	I	-	IO(I)	Off/-*1
346	SDHI0	SCIFB1	VIN1	-		I(GPIO)/I(DBG)*1
W2	SD0_DAT0	SCIFB1_RXD_B	VI1_DATA2_B/VI1_B2_B	-	GP3_2	1.8/3.3V*2/16mA
	IO	I	I	-	IO(I)	Off/-*1
347	SDHI0	SCIFB1	VIN1	-		I(GPIO)/I(DBG)*1
V7	SD0_DAT1	SCIFB1_TXD_B	VI1_DATA3_B/VI1_B3_B	-	GP3_3	1.8/3.3V*2/16mA
	IO	O	I	-	IO(I)	Off/-*1
348	SDHI0	SCIFB1	VIN1	-		I(GPIO)/I(DBG)*1
V6	SD0_DAT2	SCIFB1_CTS#_B	VI1_DATA4_B/VI1_B4_B	-	GP3_4	1.8/3.3V*2/16mA
	IO	I	I	-	IO(I)	Off/-*1
349	SDHI0	SCIFB1	VIN1	-		I(GPIO)/I(DBG)*1
V5	SD0_DAT3	SCIFB1_RTS#_B	VI1_DATA5_B/VI1_B5_B	-	GP3_5	1.8/3.3V*2/16mA
	IO	O	I	-	IO(I)	Off/-*1

Notes: 1. (No.344 to 349): Debugging function is assigned. For details of debugging function, refer to section 62, CoreSight. The default pin state after power-on reset depends on MD[21:20], MD[12:10] and MDT[1:0] pins setting. For details of mode pin settings, refer to section 3.3, Mode Pin Settings. Default pull-up state of No.344 to 349 is "-" only in debugging operation.

2. (No.344 to 349): Pin voltage is selectable (3.3 V: default). For details, refer to IOCTRL6 register in section 5, Pin Function Controller (PFC).

SDHI0/1, MMC, USB2.0, VIN, IIC, I2C, EtherAVB, SCIFB and GPIO (No.350 to 361): Up to 11-Function Multiplexed

These pins are set for GPIO after power-on reset. For details, refer to GPSR2 and GPSR3 registers in section 5, Pin Function Controller (PFC).

Function	1	2	3	4	5	6	7	8	9	10	GPIO	
No.	Module											During POR
Pin No.	Pin Name											V/|IOH|
	I/O											Pull-up
350	SDHI0	MMC0	Reserved	Reserved	Reserved	VIN1	IIC1	I2C1	VIN2	-		I(GPIO)
W3	SD0_CD	MMC0_D6	-	-	-	VI1_DATA6_B/VI1_B6_B	IIC1_SCL_B	I2C1_SCL_B	VI2_DATA6_B/VI2_B6_B	-	GP3_6	1.8/3.3V*2/16 mA
	I	IO	-	-	-	I	IO	IO	I	-	IO(I)	Off
351	SDHI0	MMC0	Reserved	Reserved	Reserved	VIN1	IIC1	I2C1	VIN2	-		I(GPIO)
W4	SD0_WP	MMC0_D7	-	-	-	VI1_DATA7_B/VI1_B7_B	IIC1_SDA_B	I2C1_SDA_B	VI2_DATA7_B/VI2_B7_B	-	GP3_7	1.8/3.3V*2/16 mA
	I	IO	-	-	-	I	IO	IO	I	-	IO(I)	Off
352	SDHI0	-	-	-	-	-	-	-	-	-	-	P
W8	VCCQ_SD0	-	-	-	-	-	-	-	-	-	-	-
	P	-	-	-	-	-	-	-	-	-	-	-
353	SDHI1	EtherAVB	Reserved	-	-	-	-	-	-	-		I(GPIO)/Z(DBG)*1
U1	SD1_CLK	AVB_TX_EN	-	-	-	-	-	-	-	-	GP3_8	1.8/3.3V*2/16 mA
	O	O	-	-	-	-	-	-	-	-	IO(I)	Off/-*1
354	SDHI1	EtherAVB	Reserved	SCIFB0	-	-	-	-	-	-		I(GPIO)/Z(DBG)*1
T6	SD1_CMD	AVB_TX_ER	-	SCIFB0_SCK_B	-	-	-	-	-	-	GP3_9	1.8/3.3V*2/16 mA
	IO	O	-	O	-	-	-	-	-	-	IO(I)	Off/-*1
355	SDHI1	EtherAVB	Reserved	SCIFB0	-	-	-	-	-	-		I(GPIO)/Z(DBG)*1
U6	SD1_DAT0	AVB_TX_CLK	-	SCIFB0_RXD_B	-	-	-	-	-	-	GP3_10	1.8/3.3V*2/16 mA
	IO	I	-	I	-	-	-	-	-	-	IO(I)	Off/-*1
356	SDHI1	EtherAVB	Reserved	SCIFB0	-	-	-	-	-	-		I(GPIO)/Z(DBG)*1
U4	SD1_DAT1	AVB_LINK	-	SCIFB0_TXD_B	-	-	-	-	-	-	GP3_11	1.8/3.3V*2/16 mA
	IO	I	-	O	-	-	-	-	-	-	IO(I)	Off/-*1
357	SDHI1	EtherAVB	Reserved	SCIFB0	-	-	-	-	-	-		I(GPIO)/Z(DBG)*1
U3	SD1_DAT2	AVB_COL	-	SCIFB0_CTS#_B	-	-	-	-	-	-	GP3_12	1.8/3.3V*2/16 mA
	IO	I	-	I	-	-	-	-	-	-	IO(I)	Off/-*1
358	SDHI1	EtherAVB	Reserved	SCIFB0	-	-	-	-	-	-		I(GPIO)/Z(DBG)*1
T7	SD1_DAT3	AVB_RXD0	-	SCIFB0_RTS#_B	-	-	-	-	-	-	GP3_13	1.8/3.3V*2/16 mA
	IO	I	-	O	-	-	-	-	-	-	IO(I)	Off/-*1
359	SDHI1	MMC1	Reserved	Reserved	Reserved	VIN0	IIC2	I2C2	Reserved	VIN3		I(GPIO)/Z(DBG)*1
U7	SD1_CD	MMC1_D6	-	-	-	VI0_CLK_B	IIC2_SCL_D	I2C2_SCL_D	-	VI3_CLK_B	GP3_14	1.8/3.3V*2/16 mA
	I	IO	-	-	-	I	IO	IO	-	I	IO(I)	Off
360	SDHI1	MMC1	Reserved	Reserved	Reserved	VIN1	IIC2	I2C2	Reserved	-		I(GPIO)/Z(DBG)*1
V3	SD1_WP	MMC1_D7	-	-	-	VI1_CLK_B	IIC2_SDA_D	I2C2_SDA_D	-	-	GP3_15	1.8/3.3V*2/16 mA
	I	IO	-	-	-	I	IO	IO	-	-	IO(I)	Off
361	SDHI1	-	-	-	-	-	-	-	-	-	-	P
U8	VCCQ_SD1	-	-	-	-	-	-	-	-	-	-	-
	P	-	-	-	-	-	-	-	-	-	-	-

Notes: 1. (No.353 to 358): Debugging function is assigned. For details of debugging function, refer to section 62, CoreSight. The default pin state after power-on reset depends on MD[21:20], MD[12:10] and MDT[1:0] pins setting. For details of mode pin settings, refer to section 3.3, Mode Pin Settings. Default pull-up state of No.353 to 358 is "-" only in debugging operation.

2. (No.350, 351 and No.353 to 358): Pin voltage is selectable (3.3 V: default). For details, refer to IOCTRL6 register in section 5, Pin Function Controller (PFC).

SDHI2, MMC, VIN, SCIFB, SCIF, HSCIF, USB2.0 and GPIO (No.362 to 370): Up to 11-Function Multiplexed

These pins are set for GPIO after power-on reset. For details, refer to GPSR3 register in section 5, Pin Function Controller (PFC).

Function	1	2	3	4	5	6	7	8	9	10	GPIO	
No.	Module											During POR
Pin No.	Pin Name											V/|IOH|
	I/O											Pull-up
362	SDHI2	MMC0	Reserved	VIN0	Reserved	Reserved	VIN3	-	-	-		I(GPIO)
R1	SD2_CLK	MMC0_CLK	-	VI0_DATA0_B/VI0_B0_B		-	VI3_DATA0_B	-	-	-	GP3_16	1.8/3.3V*/16mA
	O	O	-	I		-	I	-	-	-	IO(I)	Off
363	SDHI2	MMC0	Reserved	VIN0	SCIFB1	SCIF1	Reserved	Reserved	VIN3	-		I(GPIO)
T4	SD2_CMD	MMC0_CMD	-	VI0_DATA1_B/VI0_B1_B	SCIFB1_SCK_E	SCK1_D	-	-	VI3_DATA1_B	-	GP3_17	1.8/3.3V*/16mA
	IO	IO	-	I	O	IO	-	-	I	-	IO(I)	Off
364	SDHI2	MMC0	Reserved	VIN0	SCIFB1	SCIF1	Reserved	Reserved	VIN3	-		I(GPIO)
R5	SD2_DAT0	MMC0_D0	-	VI0_DATA2_B/VI0_B2_B	SCIFB1_RXD_E	RX1_D	-	-	VI3_DATA2_B	-	GP3_18	1.8/3.3V*/16mA
	IO	IO	-	I	I	I	-	-	I	-	IO(I)	Off
365	SDHI2	MMC0	Reserved	Reserved	VIN0	SCIFB1	SCIF1	Reserved	Reserved	VIN3		I(GPIO)
R4	SD2_DAT1	MMC0_D1	-	-	VI0_DATA3_B/VI0_B3_B	SCIFB1_TXD_E	TX1_D	-	-	VI3_DATA3_B	GP3_19	1.8/3.3V*/16mA
	IO	IO	-	-	I	O	O	-	-	I	IO(I)	Off
366	SDHI2	MMC0	Reserved	Reserved	VIN0	HSCIF0	Reserved	Reserved	VIN3	-		I(GPIO)
R3	SD2_DAT2	MMC0_D2	-	-	VI0_DATA4_B/VI0_B4_B	HRX0_D	-	-	VI3_DATA4_B	-	GP3_20	1.8/3.3V*/16mA
	IO	IO	-	-	I	I	-	-	I	-	IO(I)	Off
367	SDHI2	MMC0	Reserved	VIN0	HSCIF0	Reserved	Reserved	VIN3	-	-		I(GPIO)
T5	SD2_DAT3	MMC0_D3	-	VI0_DATA5_B/VI0_B5_B	HTX0_D	-	-	VI3_DATA5_B	-	-	GP3_21	1.8/3.3V*/16mA
	IO	IO	-	I	O	-	-	I	-	-	IO(I)	Off
368	SDHI2	MMC0	Reserved	Reserved	Reserved	VIN0	HSCIF0	Reserved	Reserved	VIN3		I(GPIO)
T2	SD2_CD	MMC0_D4	-	-	-	VI0_DATA6_B/VI0_B6_B	HCTS0#_D	-	-	VI3_DATA6_B	GP3_22	1.8/3.3V*/16mA
	I	IO	-	-	-	I	IO	-	-	I	IO(I)	Off
369	SDHI2	MMC0	Reserved	Reserved	Reserved	VIN0	HSCIF0	Reserved	Reserved	VIN3		I(GPIO)
T3	SD2_WP	MMC0_D5	-	-	-	VI0_DATA7_B/VI0_B7_B	HRTS0#_D	-	-	VI3_DATA7_B	GP3_23	1.8/3.3V*/16mA
	I	IO	-	-	-	I	IO	-	-	I	IO(I)	Off
370	SDHI2	-	-	-	-	-	-	-	-	-	-	P
T8	VCCQ_SD2	-	-	-	-	-	-	-	-	-	-	-
	P	-	-	-	-	-	-	-	-	-	-	-

Note: * (No.362 to 369): Pin voltage is selectable (3.3 V: default). For details, refer to IOCTRL6 register in section 5, Pin Function Controller (PFC).

SDHI3, MMC and GPIO (No.371 to 379): Up to 11-Function Multiplexed

These pins are set for GPIO after power-on reset. For details, refer to GPSR3 register in section 5, Pin Function Controller (PFC).

Function	1	2	3	4	5	6	7	8	9	10	GPIO	
No.	Module											During POR
Pin No.	Pin Name											V/|IOH|
	I/O											Pull-up
371	SDHI3	MMC1	-	-	-	-	-	-	-	-		I(GPIO)
P1	SD3_CLK	MMC1_CLK	-	-	-	-	-	-	-	-	GP3_24	1.8/3.3V/16mA
	O	O	-	-	-	-	-	-	-	-	IO(I)	Off
372	SDHI3	MMC1	Reserved	-	-	-	-	-	-	-		I(GPIO)
P5	SD3_CMD	MMC1_CMD	-	-	-	-	-	-	-	-	GP3_25	1.8/3.3V/16mA
	IO	IO	-	-	-	-	-	-	-	-	IO(I)	Off
373	SDHI3	MMC1	Reserved	-	-	-	-	-	-	-		I(GPIO)
R7	SD3_DAT0	MMC1_D0	-	-	-	-	-	-	-	-	GP3_26	1.8/3.3V/16mA
	IO	IO	-	-	-	-	-	-	-	-	IO(I)	Off
374	SDHI3	MMC1	Reserved	-	-	-	-	-	-	-		I(GPIO)
R6	SD3_DAT1	MMC1_D1	-	-	-	-	-	-	-	-	GP3_27	1.8/3.3V/16mA
	IO	IO	-	-	-	-	-	-	-	-	IO(I)	Off
375	SDHI3	MMC1	Reserved	-	-	-	-	-	-	-		I(GPIO)
P4	SD3_DAT2	MMC1_D2	-	-	-	-	-	-	-	-	GP3_28	1.8/3.3V/16mA
	IO	IO	-	-	-	-	-	-	-	-	IO(I)	Off
376	SDHI3	MMC1	Reserved	-	-	-	-	-	-	-		I(GPIO)
P3	SD3_DAT3	MMC1_D3	-	-	-	-	-	-	-	-	GP3_29	1.8/3.3V/16mA
	IO	IO	-	-	-	-	-	-	-	-	IO(I)	Off
377	SDHI3	MMC1	Reserved	Reserved	Reserved	Reserved	-	-	-	-		I(GPIO)
P6	SD3_CD	MMC1_D4	-	-	-	-	-	-	-	-	GP3_30	1.8/3.3V/16mA
	I	IO	-	-	-	-	-	-	-	-	IO(I)	Off
378	SDHI3	MMC1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved		I(GPIO)
P7	SD3_WP	MMC1_D5	-	-	-	-	-	-	-	-	GP3_31	1.8/3.3V/16mA
	I	IO	-	-	-	-	-	-	-	-	IO(I)	Off
379	SDHI3	-	-	-	-	-	-	-	-	-	-	P
P8	VCCQ_SD3	-	-	-	-	-	-	-	-	-	-	-
	P	-	-	-	-	-	-	-	-	-	-	-

No.380 to 392: Single Function

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V/|IOH|
	I/O	Pull-up
380	Reserved	Z
L31	-	1.8/3.3V/-
	-	-
381	Reserved	Z
K31	-	1.8/3.3V/-
	-	-
382	Reserved	Z
N31	-	1.8/3.3V/-
	-	-
383	Reserved	Z
M31	-	1.8/3.3V/-
	-	-
384	Reserved	Z
L29	-	1.8/3.3V/-
	-	-
385	Reserved	Z
L28	-	1.8/3.3V/-
	-	-
386	Reserved	Z
M29	-	1.8/3.3V/-
	-	-
387	Reserved	Z
M28	-	1.8/3.3V/-
	-	-

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V/|IOH|
	I/O	Pull-up
388	-	P
N28	VCCQ18_MLBP	-
	P	-
389	-	P
L25	VDD_MLBPPLL0	-
	P	-
390	-	P
M25	VSS_MLBPPLL0	-
	P	-
391	-	P
L26	VDD_MLBPPLL1	-
	P	-
392	-	P
M26	VSS_MLBPPLL1	-
	P	-

IIC, I2C, SCIFB, SCIF, RCAN, SSI, MSIOF and GPIO (No.393 to 409): Up to 7-Function Multiplexed

These pins are set for GPIO after power-on reset except for No.396 to 398. For details, refer to GPSR4 register in section 5, Pin Function Controller (PFC).

Function	1	2	3	4	5	6	GPIO	
No.	Module							During POR
Pin No.	Pin Name							V/|IOH|
	I/O							Pull-up
393	Reserved	IIC2	I2C2	-	-	-		I(GPIO)
AB31	-	IIC2_SCL_B	I2C2_SCL_B	-	-	-	GP4_0	3.3V/16mA
	-	IO	IO	-	-	-	IO(I)	-
394	Reserved	SCIFB1	SCIF1	IIC2	I2C2	-		I(GPIO)
AC31	-	SCIFB1_RXD_D	RX1_C	IIC2_SDA_B	I2C2_SDA_B	-	GP4_1	3.3V/16mA
	-	I	I	IO	IO	-	IO(I)	-
395	Reserved	Reserved	SCIFB1	SCIF1	Reserved	Reserved		I(GPIO)
AA31	-	-	SCIFB1_TXD_D	TX1_C	-	-	GP4_2	3.3V/16mA
	-	-	O	O	-	-	IO(I)	-
396	Reserved	-	-	-	-	-	-	IO(MLB)
AB29	-	-	-	-	-	-	-	3.3V/16mA
	-	-	-	-	-	-	-	-
397	-	-	-	-	-	-	-	P
AA27	VDD_MLBPLL	-	-	-	-	-	-	-
	P	-	-	-	-	-	-	-
398	-	-	-	-	-	-	-	P
AA26	VSS_MLBPLL	-	-	-	-	-	-	-
	P	-	-	-	-	-	-	-
399	SSI	RCAN	Reserved	-	-	-		I(GPIO)
P31	SSI_SCK0129	CAN_CLK_B	-	-	-	-	GP4_3	3.3V/8mA
	IO	I	-	-	-	-	IO(I)	On
400	SSI	RCAN0	Reserved	-	-	-		I(GPIO)
P30	SSI_WS0129	CAN0_TX_B	-	-	-	-	GP4_4	3.3V/8mA
	IO	O	-	-	-	-	IO(I)	On
401	SSI	RCAN0	Reserved	-	-	-		I(GPIO)
P29	SSI_SDATA0	CAN0_RX_B	-	-	-	-	GP4_5	3.3V/8mA
	IO	I	-	-	-	-	IO(I)	On
402	SSI	RCAN1	Reserved	-	-	-		I(GPIO)
P27	SSI_SDATA1	CAN1_TX_B	-	-	-	-	GP4_6	3.3V/8mA
	IO	O	-	-	-	-	IO(I)	On
403	SSI	RCAN1	SSI	Reserved	-	-		I(GPIO)
R26	SSI_SDATA2	CAN1_RX_B	SSI_SCK1	-	-	-	GP4_7	3.3V/8mA
	IO	I	IO	-	-	-	IO(I)	On
404	SSI	Reserved	SCIFB0	MSIOF1	Reserved	-		I(GPIO)
R31	SSI_SCK34	-	SCIFB0_SCK	MSIOF1_SCK	-	-	GP4_8	3.3V/8mA
	IO	-	O	IO	-	-	IO(I)	On
405	SSI	Reserved	SCIFB0	MSIOF1	Reserved	-		I(GPIO)
R28	SSI_WS34	-	SCIFB0_RXD	MSIOF1_SYNC	-	-	GP4_9	3.3V/8mA
	IO	-	I	IO	-	-	IO(I)	On
406	SSI	Reserved	SCIFB0	MSIOF1	Reserved	-		I(GPIO)
R27	SSI_SDATA3	-	SCIFB0_TXD	MSIOF1_SS1	-	-	GP4_10	3.3V/8mA
	IO	-	O	O	-	-	IO(I)	On
407	SSI	Reserved	SCIFB0	MSIOF1	SSI	Reserved		I(GPIO)
T31	SSI_SCK4	-	SCIFB0_CTS#	MSIOF1_SS2	SSI_SCK5_C	-	GP4_11	3.3V/8mA
	IO	-	I	O	IO	-	IO(I)	On
408	SSI	Reserved	SCIFB0	MSIOF1	SSI	Reserved		I(GPIO)
T29	SSI_WS4	-	SCIFB0_RTS#	MSIOF1_TXD	SSI_WS5_C	-	GP4_12	3.3V/8mA
	IO	-	O	O	IO	-	IO(I)	On
409	SSI	Reserved	MSIOF1	Reserved	-	-		I(GPIO)
R29	SSI_SDATA4	-	MSIOF1_RXD	-	-	-	GP4_13	3.3V/8mA
	IO	-	I	-	-	-	IO(I)	On

SSI, SCIFB, DU, RCAN, SCIF, SCIFA, TMU, ADG, SCU and GPIO (No.410 to 422): Up to 13-Function Multiplexed

These pins are set for GPIO after power-on reset. For details, refer to GPSR4 register in section 5, Pin Function Controller (PFC).

Function	1	2	3	4	5	6	7	8	9	10	11	12	GPIO	
No.	Module													During POR
Pin No.	Pin Name													V/|IOH|
	I/O													Pull-up
410	SSI	SCIFB1	Reserved	DU	Reserved	Reserved	-	-	-	-	-	-		I(GPIO)
U31	SSI_SCK5	SCIFB1_SCK	-	DU_EXHSYNC/DU_HSYNC	-	-	-	-	-	-	-	-	GP4_14	3.3V/8mA
	IO	O	-	IO	-	-	-	-	-	-	-	-	IO(I)	On
411	SSI	SCIFB1	Reserved	DU	Reserved	Reserved	-	-	-	-	-	-		I(GPIO)
U30	SSI_WS5	SCIFB1_RXD	-	DU_EXVSYNC/DU_VSYNC	-	-	-	-	-	-	-	-	GP4_15	3.3V/8mA
	IO	I	-	IO	-	-	-	-	-	-	-	-	IO(I)	On
412	SSI	SCIFB1	Reserved	DU	Reserved	Reserved	-	-	-	-	-	-		I(GPIO)
P26	SSI_SDATA5	SCIFB1_TXD	-	DU_DR2	-	-	-	-	-	-	-	-	GP4_16	3.3V/8mA
	IO	O	-	O	-	-	-	-	-	-	-	-	IO(I)	On
413	SSI	SCIFB1	Reserved	Reserved	DU	Reserved	Reserved	Reserved	Reserved	-	-	-		I(GPIO)
U29	SSI_SCK6	SCIFB1_CTS#	-	-	DU_DR3	-	-	-	-	-	-	-	GP4_17	3.3V/8mA
	IO	I	-	-	O	-	-	-	-	-	-	-	IO(I)	On
414	SSI	SCIFB1	RCAN0	DU	Reserved	Reserved	-	-	-	-	-	-		I(GPIO)
U27	SSI_WS6	SCIFB1_RTS#	CAN0_TX_D	DU_DR4	-	-	-	-	-	-	-	-	GP4_18	3.3V/8mA
	IO	O	O	O	-	-	-	-	-	-	-	-	IO(I)	On
415	SSI	Reserved	Reserved	DU	Reserved	Reserved	-	-	-	-	-	-		I(GPIO)
T25	SSI_SDATA6	-	-	DU_DR5	-	-	-	-	-	-	-	-	GP4_19	3.3V/8mA
	IO	-	-	O	-	-	-	-	-	-	-	-	IO(I)	On
416	SSI	Reserved	SCIF1	SCIFA1	DU	Reserved	Reserved	-	-	-	-	-		I(GPIO)
V29	SSI_SCK78	-	SCK1	SCIFA1_SCK	DU_DR6	-	-	-	-	-	-	-	GP4_20	3.3V/8mA
	IO	-	IO	O	O	-	-	-	-	-	-	-	IO(I)	On
417	SSI	Reserved	SCIFB2	SCIFA2	DU	Reserved	Reserved	-	-	-	-	-		I(GPIO)
U28	SSI_WS78	-	SCIFB2_SCK	SCIFA2_CTS#	DU_DR7	-	-	-	-	-	-	-	GP4_21	3.3V/8mA
	IO	-	O	I	O	-	-	-	-	-	-	-	IO(I)	On
418	SSI	Reserved	SCIFB2	SCIFA2	TMU	Reserved	Reserved	Reserved	Reserved	SSI	Reserved	Reserved		I(GPIO)
T26	SSI_SDATA7	-	SCIFB2_RXD	SCIFA2_RTS#	TCLK2	-	-	-	-	SSI_SDATA7_B	-	-	GP4_22	3.3V/8mA
	IO	-	I	O	I	-	-	-	-	IO	-	-	IO(I)	On
419	SSI	Reserved	SCIFB2	RCAN0	Reserved	SSI	-	-	-	-	-	-		I(GPIO)
T28	SSI_SDATA8	-	SCIFB2_TXD	CAN0_TX_C	-	SSI_SDATA8_B	-	-	-	-	-	-	GP4_23	3.3V/8mA
	IO	-	O	O	-	IO	-	-	-	-	-	-	IO(I)	On
420	SSI	Reserved	SCIFB2	SSI	SSI	Reserved	-	-	-	-	-			I(GPIO)
R25	SSI_SDATA9	-	SCIFB2_CTS#	SSI_WS1	SSI_SDATA5_C	-	-	-	-	-	-		GP4_24	3.3V/8mA
	IO	-	I	IO	IO	-	-	-	-	-	-		IO(I)	On
421	ADG	SCIFB2	Reserved	-	-	-	-	-	-	-	-			I(GPIO)
V31	AUDIO_CLKA	SCIFB2_RTS#	-	-	-	-	-	-	-	-	-		GP4_25	3.3V/8mA
	I	O	-	-	-	-	-	-	-	-	-		IO(I)	On
422	ADG	SCIF	RCAN0	SCU	RCAN0	Reserved	Reserved	-	-	-	-			I(GPIO)
W31	AUDIO_CLKB	SCIF_CLK	CAN0_RX_D	DVC_MUTE	CAN0_RX_C	-	-	-	-	-	-		GP4_26	3.3V/8mA
	I	I	I	I	I	-	-	-	-	-	-		IO(I)	On

SCIFA, HSCIF, SCIF, MSIOF, DU, IIC, I2C, PWM and GPIO (No.423 to 434): Up to 10-Function Multiplexed and Mode Pin Assigned (No.425, 427, 429 and 431)

These pins are set for GPIO after power-on reset. For details, refer to GPSR4 and GPSR5 registers in section 5, Pin Function Controller (PFC).

Function	1	2	3	4	5	6	7	8	9	GPIO	
No.	Module										During POR
Pin No.	Pin Name										V|IOH|
Mode Pin	I/O										Pull-up
423	SCIFA0	HSCIF1	SCIF0	MSIOF3	DU	Reserved	IIC1	I2C1	-		I(GPIO)
AA30	SCIFA0_SCK	HSCK1	SCK0	MSIOF3_SS2	DU_DG2	-	IIC1_SDA_C	I2C1_SDA_C	-	GP4_27	3.3V/8mA
	O	IO	IO	O	O	-	IO	IO	-	IO(I)	On
424	SCIFA0	HSCIF1	SCIF0	DU	Reserved	-	-	-	-		I(GPIO)
AA29	SCIFA0_RXD	HRX1	RX0	DU_DR0	-	-	-	-	-	GP4_28	3.3V/8mA
	I	I	I	O	-	-	-	-	-	IO(I)	On
425	SCIFA0	HSCIF1	SCIF0	DU	Reserved	-	-	-	-		I(Mode Pin)
Y30	SCIFA0_TXD	HTX1	TX0	DU_DR1	-	-	-	-	-	GP4_29	3.3V/8mA
MD5	O	O	O	O	-	-	-	-	-	IO(I)	Off
426	SCIFA0	HSCIF1	SCIF0	MSIOF3	DU	Reserved	PWM0	IIC1	I2C1		I(GPIO)
W25	SCIFA0_CTS#	HCTS1#	CTS0#	MSIOF3_SYNC	DU_DG3	-	PWM0_B	IIC1_SCL_C	I2C1_SCL_C	GP4_30	3.3V/8mA
	I	IO	IO	IO	O	-	O	IO	IO	IO(I)	On
427	SCIFA0	HSCIF1	SCIF0	MSIOF3	DU	Reserved	PWM1	-	-		I(Mode Pin)
Y29	SCIFA0_RTS#	HRTS1#	RTS0#	MSIOF3_SS1	DU_DG0	-	PWM1_B	-	-	GP4_31	3.3V/8mA
MD4	O	IO	IO	O	O	-	O	-	-	IO(I)	Off
428	SCIFA1	Reserved	SCIF1	DU	Reserved	-	-	-	-		I(GPIO)
Y28	SCIFA1_RXD	-	RX1	DU_EXODDF/DU_ODDF/DISP/CDE	-	-	-	-	-	GP5_0	3.3V/8mA
	I	-	I	IO	-	-	-	-	-	IO(I)	On
429	SCIFA1	Reserved	SCIF1	DU	Reserved	-	-	-	-		I(Mode Pin)
Y27	SCIFA1_TXD	-	TX1	DU_DG1	-	-	-	-	-	GP5_1	3.3V/8mA
MD3	O	-	O	O	-	-	-	-	-	IO(I)	Off
430	SCIFA1	Reserved	SCIF1	MSIOF3	DU	Reserved	-	-	-		I(GPIO)
Y25	SCIFA1_CTS#	-	CTS1#	MSIOF3_RXD	DU_DOTCLKOUT0	-	-	-	-	GP5_2	3.3V/8mA
	I	-	IO	I	O	-	-	-	-	IO(I)	On
431	SCIFA1	Reserved	SCIF1	MSIOF3	DU	Reserved	HSCIF0	-	-		I(Mode Pin)
Y26	SCIFA1_RTS#	-	RTS1#	MSIOF3_TXD	DU_DOTCLKOUT1	-	HRTS0#_C	-	-	GP5_3	3.3V/8mA
MD2	O	-	IO	O	O	-	IO	-	-	IO(I)	Off
432	SCIFA2	Reserved	SCIF2	MSIOF3	DU	Reserved	SCIF	-	-		I(GPIO)
AB28	SCIFA2_SCK	-	SCK2	MSIOF3_SCK	DU_DG7	-	SCIF_CLK_B	-	-	GP5_4	3.3V/8mA
	O	-	IO	IO	O	-	I	-	-	IO(I)	On
433	SCIFA2	Reserved	SCIF2	DU	Reserved	IIC2	I2C2	-	-		I(GPIO)
AC27	SCIFA2_RXD	-	TX2	DU_DB0	-	IIC2_SCL	I2C2_SCL	-	-	GP5_5	3.3V/8mA
	I	-	O	O	-	IO	IO	-	-	IO(I)	On
434	SCIFA2	Reserved	SCIF2	DU	Reserved	IIC2	I2C2	-	-		I(GPIO)
AB27	SCIFA2_TXD	-	RX2	DU_DB1	-	IIC2_SDA	I2C2_SDA	-	-	GP5_6	3.3V/8mA
	O	-	I	O	-	IO	IO	-	-	IO(I)	On

HSCIF,, DU, SSI, MSIOF, ADG, SCIFA, IIC, I2C and GPIO (No.435 to 449): Up to 8-Function Multiplexed and Mode Pin Assigned (No.437 and No.442 to 444)

These pins are set for GPIO after power-on reset except for No.446 to 449. For details, refer to GPSR5 register in section 5, Pin Function Controller (PFC).

Function	1	2	3	4	5	6	7	GPIO	
No.	Module								During POR
Pin No.	Pin Name								V/|IOH|
Mode Pin	I/O								Pull-up
435	HSCIF0	Reserved	DU	Reserved	HSCIF0	-	-		I(GPIO)
V28	HSCK0	-	DU_DG4	-	HCTS0#_C	-	-	GP5_7	3.3V/8mA
	IO	-	O	-	IO	-	-	IO(I)	On
436	HSCIF0	DU	Reserved	-	-	-	-		I(GPIO)
V26	HRX0	DU_DB2	-	-	-	-	-	GP5_8	3.3V/8mA
	I	O	-	-	-	-	-	IO(I)	On
437	HSCIF0	DU	Reserved	-	-	-	-		I(Mode Pin)
V27	HTX0	DU_DB3	-	-	-	-	-	GP5_9	3.3V/8mA
MD1	O	O	-	-	-	-	-	IO(I)	Off
438	HSCIF0	SSI	DU	Reserved	-	-	-		I(GPIO)
U26	HCTS0#	SSI_SCK9	DU_DB4	-	-	-	-	GP5_10	3.3V/8mA
	IO	IO	O	-	-	-	-	IO(I)	On
439	HSCIF0	SSI	DU	Reserved	-	-	-		I(GPIO)
U25	HRTS0#	SSI_WS9	DU_DB5	-	-	-	-	GP5_11	3.3V/8mA
	IO	IO	O	-	-	-	-	IO(I)	On
440	MSIOF0	Reserved	Reserved	DU	Reserved	-	-		I(GPIO)
Y31	MSIOF0_SCK	-	-	DU_DB6	-	-	-	GP5_12	3.3V/8mA
	IO	-	-	O	-	-	-	IO(I)	On
441	MSIOF0	Reserved	SSI	Reserved	DU	Reserved	HSCIF0		I(GPIO)
V25	MSIOF0_SYNC	-	SSI_SCK2	-	DU_DB7	-	HRX0_C	GP5_13	3.3V/8mA
	IO	-	IO	-	O	-	I	IO(I)	On
442	MSIOF0	Reserved	DU	Reserved	-	-	-		I(Mode Pin)
W28	MSIOF0_SS1	-	DU_DG5	-	-	-	-	GP5_14	3.3V/8mA
MD0	O	-	O	-	-	-	-	IO(I)	Off
443	MSIOF0	Reserved	DU	Reserved	-	-	-		I(Mode Pin)
W29	MSIOF0_TXD	-	DU_DG6	-	-	-	-	GP5_15	3.3V/8mA
MDT1	O	-	O	-	-	-	-	IO(I)	Off
444	MSIOF0	ADG	Reserved	DU	Reserved	HSCIF0	SCIFA2		I(Mode Pin)
W26	MSIOF0_SS2	AUDIO_CLKOUT	-	DU_DISP	-	HTX0_C	SCIFA2_TXD_B	GP5_16	3.3V/8mA
MDT0	O	O	-	O	-	O	O	IO(I)	Off
445	MSIOF0	Reserved	SSI	Reserved	DU	Reserved	SCIFA2		I(GPIO)
W27	MSIOF0_RXD	-	SSI_WS2	-	DU_CDE	-	SCIFA2_RXD_B	GP5_17	3.3V/8mA
	I	-	IO	-	O	-	I	IO(I)	On
446	IIC0	I2C0	-	-	-	-	-	-	Z
AG15	IIC0_SCL	I2C0_SCL	-	-	-	-	-	-	1.8V/-
	IO(OD, Z)	IO(OD)	-	-	-	-	-	-	-
447	IIC0	I2C0	-	-	-	-	-	-	Z
AF15	IIC0_SDA	I2C0_SDA	-	-	-	-	-	-	1.8V/-
	IO(OD, Z)	IO(OD)	-	-	-	-	-	-	-
448	IIC3(DVFS)	I2C3	-	-	-	-	-	-	Z
AJ15	IIC3_SCL	I2C3_SCL	-	-	-	-	-	-	1.8V/-
	IO(OD, Z)	IO(OD)	-	-	-	-	-	-	-
449	IIC3(DVFS)	I2C3	-	-	-	-	-	-	Z
AH15	IIC3_SDA	I2C3_SDA	-	-	-	-	-	-	1.8V/-
	IO(OD, Z)	IO(OD)	-	-	-	-	-	-	-

USB, ADG, TMU and GPIO (No.450 to 487): Up to 3-Function Multiplexed

These pins are set for USB after power-on reset. For details, refer to GPSR5 register in section 5, Pin Function Controller (PFC).

	Function 1	GPIO	
No.	Module		During POR
Pin No.	Pin Name		V/|IOH|
	I/O		Pull-up
450	USB	-	I
AL14	USB_EXTAL	-	1.8V/-
	I(I)	-	-
451	USB	-	O
AL15	USB_XTAL	-	1.8V/-
	O(O)	-	-
452	USB	-	P
AC24	AVSS	-	-
	P	-	-
453	USB	-	P
AD25	AVSS	-	-
	P	-	-
454	USB	-	P
AE26	AVSS	-	-
	P	-	-
455	USB 2.0 channel 0	-	I
AF31	USB0_DP	-	3.3V/-
	IO(I)	-	-
456	USB 2.0 channel 0	-	I
AE31	USB0_DM	-	3.3V/-
	IO(I)	-	-
457	USB 2.0 channel 0	-	P
AF29	USB0_RREF	-	-
	P	-	-
458	USB 2.0 channel 0	-	P
AE28	VD331	-	-
	P	-	-
459	USB 2.0 channel 0	-	P
AB25	VD181	-	-
	P	-	-
460	USB 2.0 channel 0	-	P
AB24	AVDD	-	-
	P	-	-
461	USB 2.0 channel 0	-	P
AC25	AVDD	-	-
	P	-	-
462	USB 2.0 channel 0	-	P
AD31	VSS	-	-
	P	-	-
463	USB 2.0 channel 0	-	P
AF27	AVSS	-	-
	P	-	-
464	USB 2.0 channel 0	-	P
AE30	VSS	-	-
	P	-	-
465	USB 2.0 channel 0		L
AC28	USB0_PWEN	GP5_18	3.3V/4mA
	O(L)	IO	Off
466	USB 2.0 channel 0		I
AD28	USB0_OVC/VBUS	GP5_19	3.3V/4mA
	I(I)	IO	Off

	Function 1	Function 2	GPIO	
No.	Module			During POR
Pin No.	Pin Name			V/|IOH|
	I/O			Pull-up
467	USB 2.0 channel 1	-	-	I
AH31	USB1_DP	-	-	3.3V/-
	IO(I)	-	-	-
468	USB 2.0 channel 1	-	-	I
AG31	USB1_DM	-	-	3.3V/-
	IO(I)	-	-	-
469	USB 2.0 channel 1	-	-	P
AG29	USB1_RREF	-	-	-
	P	-	-	-
470	USB 2.0 channel 1	-	-	P
AE29	VD331	-	-	-
	P	-	-	-
471	USB 2.0 channel 1	-	-	P
AC26	VD181	-	-	-
	P	-	-	-
472	USB 2.0 channel 1	-	-	P
AD26	AVDD	-	-	-
	P	-	-	-
473	USB 2.0 channel 1	-	-	P
AF30	VSS	-	-	-
	P	-	-	-
474	USB 2.0 channel 1	-	-	P
AF28	AVSS	-	-	-
	P	-	-	-
475	USB 2.0 channel 1	-	-	P
AG30	VSS	-	-	-
	P	-	-	-
476	USB 2.0 channel 1	ADG		L
AC29	USB1_PWEN	AUDIO_CLKOUT_D	GP5_20	3.3V/4mA
	O(L)	O	IO	Off
477	USB 2.0 channel 1	TMU		I
AD29	USB1_OVC	TCLK1_B	GP5_21	3.3V/4mA
	I(I)	I	IO	Off
478	USB 2.0 channel 2	-	-	I
AK31	USB2_DP	-	-	3.3V/-
	IO(I)	-	-	-
479	USB 2.0 channel 2	-	-	I
AJ31	USB2_DM	-	-	3.3V/-
	IO(I)	-	-	-
480	USB 2.0 channel 2	-	-	P
AH29	USB2_RREF	-	-	-
	P	-	-	-
481	USB 2.0 channel 2	-	-	P
AD27	VD181	-	-	-
	P	-	-	-
482	USB 2.0 channel 2	-	-	P
AE27	AVDD	-	-	-
	P	-	-	-
483	USB 2.0 channel 2	-	-	P
AH30	VSS	-	-	-
	P	-	-	-
484	USB 2.0 channel 2	-	-	P
AG28	AVSS	-	-	-
	P	-	-	-
485	USB 2.0 channel 2	-	-	P
AJ30	VSS	-	-	-
	P	-	-	-
486	USB 2.0 channel 2	-		L
AD30	USB2_PWEN	-	GP5_22	3.3V/4mA
	O(L)	-	IO	Off
487	USB 2.0 channel 2	-		I
AC30	USB2_OVC	-	GP5_23	3.3V/4mA
	I(I)	-	IO	Off

SATA, PCIEC and USB3.0 (No.488 to 529): 2-Function Multiplexed

These pins function depends on the MD[24:23] pins setting, and cannot be changed after power-on reset by software.

	Function 1	Function 2	
	MD24 = 0	MD24 = 1	
No.	Module		During POR
Pin No.	Pin Name		V/|IOH|
	I/O		Pull-up
488	SATA1	PCIEC	I
AL23	RIDP1_SATA	RIDP1_PCIe	1.0V/-
	I	I	-
489	SATA1	PCIEC	I
AL24	RIDN1_SATA	RIDN1_PCIe	1.0V/-
	I	I	-
490	SATA1	PCIEC	O
AL25	TODP1_SATA	TODP1_PCIe	1.0V/-
	O	O	-
491	SATA1	PCIEC	O
AL26	TODN1_SATA	TODN1_PCIe	1.0V/-
	O	O	-
492	SATA1	PCIEC	I
AJ26	CICREFP1_SATA	CICREFP1_PCIe	1.0V/-
	I	I	-
493	SATA1	PCIEC	I
AJ25	CICREFN1_SATA	CICREFN1_PCIe	1.0V/-
	I	I	-
494	SATA1	PCIEC	P
AE23	VSS_SATA1	VSS_PCIe	-
	P	P	-
495	SATA1	PCIEC	P
AF23	VDDD_SATA1	VDDD_PCIe	-
	P	P	-
496	SATA1	PCIEC	P
AD23	VSS_SATA1	VSS_PCIe	-
	P	P	-
497	SATA1	PCIEC	P
AF24	VDDA_SATA1	VDDA_PCIe	-
	P	P	-
498	SATA1	PCIEC	P
AG24	VDDA_SATA1	VDDA_PCIe	-
	P	P	-
499	SATA1	PCIEC	P
AG23	VDDD_SATA1	VDDD_PCIe	-
	P	P	-
500	SATA1	PCIEC	P
AH24	VDDD_SATA1	VDDD_PCIe	-
	P	P	-
501	SATA1	PCIEC	P
AE24	VSS_SATA1	VSS_PCIe	-
	P	P	-
502	SATA1	PCIEC	P
AJ24	VSS_SATA1	VSS_PCIe	-
	P	P	-
503	SATA1	PCIEC	P
AK23	VSS_SATA1	VSS_PCIe	-
	P	P	-
504	SATA1	PCIEC	P
AK24	VSS_SATA1	VSS_PCIe	-
	P	P	-
505	SATA1	PCIEC	P
AK25	VSS_SATA1	VSS_PCIe	-
	P	P	-
506	SATA1	PCIEC	P
AK26	VSS_SATA1	VSS_PCIe	-
	P	P	-

	Function 1	Function 2	
	MD23 = 0	MD23 = 1	
No.	Module		During POR
Pin No.	Pin Name		V/|IOH|
	I/O		Pull-up
507	SATA0	USB 3.0	I
AL27	RIDP0_SATA	RIDP0_USB3	1.0V/-
	I	I	-
508	SATA0	USB 3.0	I
AL28	RIDN0_SATA	RIDN0_USB3	1.0V/-
	I	I	-
509	SATA0	USB 3.0	O
AL29	TODP0_SATA	TODP0_USB3	1.0V/-
	O	O	-
510	SATA0	USB 3.0	O
AL30	TODN0_SATA	TODN0_USB3	1.0V/-
	O	O	-
511	SATA0	USB 3.0	I
AJ28	CICREFP0_SATA	CICREFP0_USB3	1.0V/-
	I	I	-
512	SATA0	USB 3.0	I
AJ27	CICREFN0_SATA	CICREFN0_USB3	1.0V/-
	I	I	-
513	SATA0	USB 3.0	P
AF25	VSS_SATA0	VSS_USB3	-
	P	P	-
514	SATA0	USB 3.0	P
AG25	VDDD_SATA0	VDDD_USB3	-
	P	P	-
515	SATA0	USB 3.0	P
AD24	VSS_SATA0	VSS_USB3	-
	P	P	-
516	SATA0	USB 3.0	P
AG26	VDDA_SATA0	VDDA_USB3	-
	P	P	-
517	SATA0	USB 3.0	P
AH27	VDDA_SATA0	VDDA_USB3	-
	P	P	-
518	SATA0	USB 3.0	P
AH25	VDDD_SATA0	VDDD_USB3	-
	P	P	-
519	SATA0	USB 3.0	P
AH26	VDDD_SATA0	VDDD_USB3	-
	P	P	-
520	SATA0	USB 3.0	P
AE25	VSS_SATA0	VSS_USB3	-
	P	P	-
521	SATA0	USB 3.0	P
AF26	VSS_SATA0	VSS_USB3	-
	P	P	-
522	SATA0	USB 3.0	P
AG27	VSS_SATA0	VSS_USB3	-
	P	P	-
523	SATA0	USB 3.0	P
AH28	VSS_SATA0	VSS_USB3	-
	P	P	-
524	SATA0	USB 3.0	P
AJ29	VSS_SATA0	VSS_USB3	-
	P	P	-
525	SATA0	USB 3.0	P
AK27	VSS_SATA0	VSS_USB3	-
	P	P	-
526	SATA0	USB 3.0	P
AK28	VSS_SATA0	VSS_USB3	-
	P	P	-
527	SATA0	USB 3.0	P
AK29	VSS_SATA0	VSS_USB3	-
	P	P	-
528	SATA0	USB 3.0	P
AK30	VSS_SATA0	VSS_USB3	-
	P	P	-
529	SATA0	USB 3.0	P
AL31	VSS_SATA0	VSS_USB3	-
	P	P	-

Thermal Sensor (No.530 and No.531): Single Function

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V/|IOH|
	I/O	Pull-up
530	Thermal Sensor	O
Y7	VTHSENSE0	1.8V/-
	O(analog)	-

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V/|IOH|
	I/O	Pull-up
531	Thermal Sensor	O
AA7	VTHREF0	1.8V/-
	O(analog)	-

- End of Table 4.1 -

4.2 Pin States

Table 4.2 is pin state of the RZ/G1H.

[Legend]

No.: Serial number, Pin No.: BGA package ball grid number, Pin Name: Pin name of function 1 in pin in Table 4.1, I/O: Input or output direction considered about all multiplexed pin functions of the pin.

During POR: Pin state during power-on reset (PRESET# pin input is low-level).

Default Pin Function: Pin function after power-on reset

Default State: Pin state of default pin function

Default pull-up: Internal pull-up control function is available or not from a power-on reset and its pull-up state.

"On": Pull-up control function is available and default state is pulled-up.

(No.292, ACK pin is available internal pull-down function.)

"Off": Pull-up control function is available and default state is not pulled-up.

"-": Pulled-up control function is not available.

For details of pull-up control function, refer to PUPR0 through PUPR6 registers in section 5, Pin Function Controller (PFC).

I: Input, IO: Input and output, O: Output, H: High level output, L: Low level output, X: Undefined value output, Z: High impedance, P: Power supply pin.

Notes: 1. All power supply pins and ground pins include VCCQ, VCCQ18, VDD, VDD_DVFS, VDDQ_M0, VDDQ_M1, VDDQ_M1A, and VSS pins which does not describe in Table 4.2 must be used.

2. All mode pins must be used during power-on reset. For details of mode pin settings, refer to section 3.3, Mode Pin Settings.

3. Boot module related pins (LBSC area 0 or QSPI) should be used during boot operation. For details of QSPI boot, refer to section 18, Booting.

4. For multiplexed pins and modules of each pin, refer to Table 4.1.

Table 4.2 Pin States

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
1	F20	M0CKE0	O	X	M0CKE0	L	-
2	C19	M0CKE1	O	X	M0CKE1	L	-
3	G16	M0VREFCA(VSS)	-	P	M0VREFCA(must be connected to VSS)	P	-
4	H18	M0BKPRST#	I	I	M0BKPRST#	I	-
5	E19	M0RESET#	O	H	M0RESET#	H to L	-
6	G20	M0CK0	O	X	M0CK0	O	-
7	G19	M0CK0#	O	X	M0CK0#	O	-
8	G17	M0CK1	O	X	M0CK1	O	-
9	G18	M0CK1#	O	X	M0CK1#	O	-
10	B20	M0CS0#	O	H	M0CS0#	H	-
11	A19	M0CS1#	O	H	M0CS1#	H	-
12	D20	M0ODT0	O	L	M0ODT0	L	-
13	E18	M0ODT1	O	L	M0ODT1	L	-
14	H16	M0ZQ	IO	IO	M0ZQ	IO	-
15	E21	M0WE#	O	H	M0WE#	H	-
16	D22	M0RAS#	O	H	M0RAS#	H	-
17	C22	M0CAS#	O	H	M0CAS#	H	-
18	E17	M0A0	O	L	M0A0	L	-
19	B22	M0A1	O	L	M0A1	L	-
20	A22	M0A2	O	L	M0A2	L	-
21	D17	M0A3	O	L	M0A3	L	-
22	A21	M0A4	O	L	M0A4	L	-
23	D16	M0A5	O	L	M0A5	L	-
24	B17	M0A6	O	L	M0A6	L	-
25	B21	M0A7	O	L	M0A7	L	-
26	A16	M0A8	O	L	M0A8	L	-
27	B18	M0A9	O	L	M0A9	L	-
28	C18	M0A10	O	L	M0A10	L	-
29	A18	M0A11	O	L	M0A11	L	-
30	E16	M0A12	O	L	M0A12	L	-
31	A17	M0A13	O	L	M0A13	L	-
32	B16	M0A14	O	L	M0A14	L	-
33	D18	M0A15	O	L	M0A15	L	-
34	C21	M0BA0	O	L	M0BA0	L	-
35	C16	M0BA1	O	L	M0BA1	L	-
36	D21	M0BA2	O	L	M0BA2	L	-
37	G21	VDDQ_M0APLL	-	P	VDDQ_M0APLL	P	-
38	H21	VSSQ_M0APLL	-	P	VSSQ_M0APLL	P	-
39	A27	M0DQ0	IO	Z	M0DQ0	Z	-
40	C28	M0DQ1	IO	Z	M0DQ1	Z	-
41	D27	M0DQ2	IO	Z	M0DQ2	Z	-
42	A29	M0DQ3	IO	Z	M0DQ3	Z	-
43	B27	M0DQ4	IO	Z	M0DQ4	Z	-
44	B29	M0DQ5	IO	Z	M0DQ5	Z	-
45	C27	M0DQ6	IO	Z	M0DQ6	Z	-
46	A30	M0DQ7	IO	Z	M0DQ7	Z	-
47	E26	M0DQS0	IO	Z**	M0DQS0	Z**	-
48	E25	M0DQS0#	IO	Z**	M0DQS0#	Z**	-

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
49	A28	M0DM0	O	Z	M0DM0	Z	-
50	G22	VDDQ_M0DPLL0	-	P	VDDQ_M0DPLL0	P	-
51	G23	VSSQ_M0DPLL0	-	P	VSSQ_M0DPLL0	P	-
52	G24	M0VREFDQ0	-	P	M0VREFDQ0	P	-
53	B23	M0DQ8	IO	Z	M0DQ8	Z	-
54	A24	M0DQ9	IO	Z	M0DQ9	Z	-
55	C24	M0DQ10	IO	Z	M0DQ10	Z	-
56	D24	M0DQ11	IO	Z	M0DQ11	Z	-
57	B26	M0DQ12	IO	Z	M0DQ12	Z	-
58	D26	M0DQ13	IO	Z	M0DQ13	Z	-
59	B24	M0DQ14	IO	Z	M0DQ14	Z	-
60	A25	M0DQ15	IO	Z	M0DQ15	Z	-
61	E23	M0DQS1	IO	Z**	M0DQS1	Z**	-
62	E24	M0DQS1#	IO	Z**	M0DQS1#	Z**	-
63	C25	M0DM1	O	Z	M0DM1	Z	-
64	F22	VDDQ_M0DPLL1	-	P	VDDQ_M0DPLL1	P	-
65	F23	VSSQ_M0DPLL1	-	P	VSSQ_M0DPLL1	P	-
66	E31	M0DQ16	IO	Z	M0DQ16	Z	-
67	C30	M0DQ17	IO	Z	M0DQ17	Z	-
68	E29	M0DQ18	IO	Z	M0DQ18	Z	-
69	B31	M0DQ19	IO	Z	M0DQ19	Z	-
70	E30	M0DQ20	IO	Z	M0DQ20	Z	-
71	C31	M0DQ21	IO	Z	M0DQ21	Z	-
72	E28	M0DQ22	IO	Z	M0DQ22	Z	-
73	D29	M0DQ23	IO	Z	M0DQ23	Z	-
74	F27	M0DQS2	IO	Z**	M0DQS2	Z**	-
75	G27	M0DQS2#	IO	Z**	M0DQS2#	Z**	-
76	D31	M0DM2	O	Z	M0DM2	Z	-
77	K25	VDDQ_M0DPLL2	-	P	VDDQ_M0DPLL2	P	-
78	J25	VSSQ_M0DPLL2	-	P	VSSQ_M0DPLL2	P	-
79	H25	M0VREFDQ1	-	P	M0VREFDQ1	P	-
80	F28	M0DQ24	IO	Z	M0DQ24	Z	-
81	G31	M0DQ25	IO	Z	M0DQ25	Z	-
82	F30	M0DQ26	IO	Z	M0DQ26	Z	-
83	H30	M0DQ27	IO	Z	M0DQ27	Z	-
84	H28	M0DQ28	IO	Z	M0DQ28	Z	-
85	J30	M0DQ29	IO	Z	M0DQ29	Z	-
86	H29	M0DQ30	IO	Z	M0DQ30	Z	-
87	H31	M0DQ31	IO	Z	M0DQ31	Z	-
88	J27	M0DQS3	IO	Z**	M0DQS3	Z**	-
89	H27	M0DQS3#	IO	Z**	M0DQS3#	Z**	-
90	G29	M0DM3	O	Z	M0DM3	Z	-
91	K26	VDDQ_M0DPLL3	-	P	VDDQ_M0DPLL3	P	-
92	J26	VSSQ_M0DPLL3	-	P	VSSQ_M0DPLL3	P	-
93	H19	VDDQ_M0BKUP	-	P	VDDQ_M0BKUP	P	-
94	F5	M1CKE0	O	X	M1CKE0/GP_DDR1*[1]	L/O	-
95	G3	M1CKE1	O	X	M1CKE1/GP_DDR2*[1]	L/O	-
96	H7	M1VREFCA	-	P	M1VREFCA	P	-
97	J7	M1BKPRST#	I	I	M1BKPRST#	I	-
98	G5	M1RESET#	O	H/X	M1RESET#/GP_DDR3*[1]	H to L/O	-

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
99	J5	M1CK0	O	X	M1CK0/Reserved*1	O/O	-
100	H5	M1CK0#	O	X	M1CK0#/Reserved*1	O/O	-
101	L5	M1CK1	O	X	M1CK1/Reserved*1	O/O	-
102	K5	M1CK1#	O	X	M1CK1#/Reserved*1	O/O	-
103	F2	M1CS0#	IO	H/I	M1CS0#/GP_DDR5*1	H/I	-
104	G1	M1CS1#	IO	H/I	M1CS1#/GP_DDR8*1	H/I	-
105	F4	M1ODT0	IO	L/I	M1ODT0/GP_DDR6*1	L/I	-
106	H4	M1ODT1	IO	L/I	M1ODT1/GP_DDR10*1	L/I	-
107	L8	M1ZQ	IO	IO	M1ZQ	IO	-
108	E3	M1WE#	O	H/Z	M1WE#/GP_DDR9*1	H/Z	-
109	D3	M1RAS#	O	H/Z	M1RAS#/GP_DDR12*1	H/Z	-
110	E4	M1CAS#	IO	H/I	M1CAS#/GP_DDR4*1	H/I	-
111	B1	M1A0	O	L/Z	M1A0/GP_DDR7*1	L/Z	-
112	H2	M1A1	IO	L/I	M1A1/GP_DDR13*1	L/I	-
113	E2	M1A2	O	L/Z	M1A2/GP_DDR15*1	L/Z	-
114	M3	M1A3	IO	L/I	M1A3/GP_DDR23*1	L/I	-
115	E1	M1A4	O	L/Z	M1A4/GP_DDR17*1	L/Z	-
116	D1	M1A5	O	L/Z	M1A5/GP_DDR11*1	L/Z	-
117	K2	M1A6	O	L/Z	M1A6/GP_DDR24*1	L/Z	-
118	H1	M1A7	IO	L/I	M1A7/GP_DDR14*1	L/I	-
119	M1	M1A8	IO	L/I	M1A8/GP_DDR25*1	L/I	-
120	J2	M1A9	O	L/Z	M1A9/GP_DDR26*1	L/Z	-
121	L3	M1A10	IO	L/I	M1A10/GP_DDR22*1	L/I	-
122	K1	M1A11	O	L/Z	M1A11/GP_DDR21*1	L/Z	-
123	C2	M1A12	O	L/Z	M1A12/GP_DDR16*1	L/Z	-
124	L1	M1A13	IO	L/I	M1A13/GP_DDR27*1	L/I	-
125	M2	M1A14	IO	L/I	M1A14/GP_DDR28*1	L/I	-
126	K3	M1A15	O	L/Z	M1A15/GP_DDR29*1	L/Z	-
127	J3	M1BA0	O	L/Z	M1BA0/GP_DDR20*1	L/Z	-
128	C1	M1BA1	O	L/Z	M1BA1/GP_DDR19*1	L/Z	-
129	H3	M1BA2	IO	L/I	M1BA2/GP_DDR18*1	L/I	-
130	L7	VDDQ_M1APLL	-	P	VDDQ_M1APLL	P	-
131	K7	VSSQ_M1APLL	-	P	VSSQ_M1APLL	P	-
132	L6	VDDQ_M1MPLL	-	P	VDDQ_M1MPLL	P	-
133	K6	VSSQ_M1MPLL	-	P	VSSQ_M1MPLL	P	-
134	B12	M1DQ0	IO	Z	M1DQ0/M0DQ32/Reserved*2	Z/Z/Z	-
135	B11	M1DQ1	IO	Z	M1DQ1/M0DQ33/Reserved*2	Z/Z/Z	-
136	D12	M1DQ2	IO	Z	M1DQ2/M0DQ34/Reserved*2	Z/Z/Z	-
137	A10	M1DQ3	IO	Z	M1DQ3/M0DQ35/Reserved*2	Z/Z/Z	-
138	C11	M1DQ4	IO	Z	M1DQ4/M0DQ36/Reserved*2	Z/Z/Z	-
139	D10	M1DQ5	IO	Z	M1DQ5/M0DQ37/Reserved*2	Z/Z/Z	-
140	C10	M1DQ6	IO	Z	M1DQ6/M0DQ38/Reserved*2	Z/Z/Z	-
141	D11	M1DQ7	IO	Z	M1DQ7/M0DQ39/Reserved*2	Z/Z/Z	-
142	E12	M1DQS0	IO	Z**	M1DQS0/M0DQS4/Reserved*2	Z/Z/Z**	-
143	E11	M1DQS0#	IO	Z**	M1DQS0#/M0DQS4#/Reserved*2	Z/Z/Z**	-
144	A11	M1DM0	O	Z	M1DM0/M0DM4/Reserved*2	Z/Z/Z	-
145	G13	VDDQ_M1DPLL0	-	P	VDDQ_M1DPLL0/VDDQ_M0DPLL4/VDDQ_M0DPLL4*2	P	-
146	G12	VSSQ_M1DPLL0	-	P	VSSQ_M1DPLL0/VSSQ_M0DPLL4/VSSQ_M0DPLL4*2	P	-
147	G14	M1VREFDQ0	-	P	M1VREFDQ0/M0VREFDQ2/M0VREFDQ2*2	P	-
148	A13	M1DQ8	IO	Z	M1DQ8/M0DQ40/Reserved*2	Z/Z/Z	-

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
149	A14	M1DQ9	IO	Z	M1DQ9/M0DQ41/Reserved*2	Z/Z/Z	-
150	D14	M1DQ10	IO	Z	M1DQ10/M0DQ42/Reserved*2	Z/Z/Z	-
151	B14	M1DQ11	IO	Z	M1DQ11/M0DQ43/Reserved*2	Z/Z/Z	-
152	C14	M1DQ12	IO	Z	M1DQ12/M0DQ44/Reserved*2	Z/Z/Z	-
153	B15	M1DQ13	IO	Z	M1DQ13/M0DQ45/Reserved*2	Z/Z/Z	-
154	D15	M1DQ14	IO	Z	M1DQ14/M0DQ46/Reserved*2	Z/Z/Z	-
155	A15	M1DQ15	IO	Z	M1DQ15/M0DQ47/Reserved*2	Z/Z/Z	-
156	E14	M1DQS1	IO	Z**	M1DQS1/M0DQS5/Reserved*2	Z/Z/Z**	-
157	E13	M1DQS1#	IO	Z**	M1DQS1#/M0DQS5#/Reserved*2	Z/Z/Z**	-
158	C13	M1DM1	O	Z	M1DM1/M0DM5/Reserved*2	Z/Z/Z	-
159	F13	VDDQ_M1DPLL1	-	P	VDDQ_M1DPLL1/VDDQ_M0DPLL5/VDDQ_M0DPLL5*2	P	-
160	F12	VSSQ_M1DPLL1	-	P	VSSQ_M1DPLL1/VSSQ_M0DPLL5/VSSQ_M0DPLL5*2	P	-
161	B6	M1DQ16	IO	Z	M1DQ16/M1DQ48/Reserved*2	Z/Z/Z	-
162	A7	M1DQ17	IO	Z	M1DQ17/M0DQ49/Reserved*2	Z/Z/Z	-
163	C8	M1DQ18	IO	Z	M1DQ18/M0DQ50/Reserved*2	Z/Z/Z	-
164	B8	M1DQ19	IO	Z	M1DQ19/M0DQ51/Reserved*2	Z/Z/Z	-
165	D8	M1DQ20	IO	Z	M1DQ20/M0DQ52/Reserved*2	Z/Z/Z	-
166	A8	M1DQ21	IO	Z	M1DQ21/M0DQ53/Reserved*2	Z/Z/Z	-
167	D6	M1DQ22	IO	Z	M1DQ22/M0DQ54/Reserved*2	Z/Z/Z	-
168	B9	M1DQ23	IO	Z	M1DQ23/M0DQ55/Reserved*2	Z/Z/Z	-
169	E8	M1DQS2	IO	Z**	M1DQS2/M0DQS6/Reserved*2	Z/Z/Z**	-
170	E9	M1DQS2#	IO	Z**	M1DQS2#/M0DQS6#/Reserved*2	Z/Z/Z**	-
171	C7	M1DM2	O	Z	M1DM2/M0DM6/Reserved*2	Z/Z/Z	-
172	F10	VDDQ_M1DPLL2	-	P	VDDQ_M1DPLL2/VDDQ_M0DPLL6/VDDQ_M0DPLL6*2	P	-
173	F9	VSSQ_M1DPLL2	-	P	VSSQ_M1DPLL2/VSSQ_M0DPLL6/VSSQ_M0DPLL6*2	P	-
174	G8	M1VREFDQ1	-	P	M1VREFDQ1/M0VREFDQ3/M0VREFDQ3*2	P	-
175	B3	M1DQ24	IO	Z	M1DQ24/M0DQ56/Reserved*2	Z/Z/Z	-
176	D5	M1DQ25	IO	Z	M1DQ25/M0DQ57/Reserved*2	Z/Z/Z	-
177	C4	M1DQ26	IO	Z	M1DQ26/M0DQ58/Reserved*2	Z/Z/Z	-
178	C5	M1DQ27	IO	Z	M1DQ27/M0DQ59/Reserved*2	Z/Z/Z	-
179	A5	M1DQ28	IO	Z	M1DQ28/M0DQ60/Reserved*2	Z/Z/Z	-
180	A3	M1DQ29	IO	Z	M1DQ29/M0DQ61/Reserved*2	Z/Z/Z	-
181	B5	M1DQ30	IO	Z	M1DQ30/M0DQ62/Reserved*2	Z/Z/Z	-
182	A2	M1DQ31	IO	Z	M1DQ31/M0DQ63/Reserved*2	Z/Z/Z	-
183	E7	M1DQS3	IO	Z**	M1DQS3/M0DQS7/Reserved*2	Z/Z/Z**	-
184	E6	M1DQS3#	IO	Z**	M1DQS3#/M0DQS7#/Reserved*2	Z/Z/Z**	-
185	A4	M1DM3	O	Z	M1DM3/M0DM7/Reserved*2	Z/Z/Z	-
186	G10	VDDQ_M1DPLL3	-	P	VDDQ_M1DPLL3/VDDQ_M0DPLL7/VDDQ_M0DPLL7*2	P	-
187	G9	VSSQ_M1DPLL3	-	P	VSSQ_M1DPLL3/VSSQ_M0DPLL7/VSSQ_M0DPLL7*2	P	-
188	G6	VDDQ_M1BKUP	-	P	VDDQ_M1BKUP	P	-
189	AL12	EXTAL	I	I	EXTAL	I	-
190	AL13	XTAL	O	O	XTAL	O	-
191	AF12	EXREFIN	I	I	EXREFIN*3	I	-
192	F16	VDD_CPGPLL1	-	P	VDD_CPGPLL1	P	-
193	F15	VSS_CPGPLL1	-	P	VSS_CPGPLL1	P	-
194	H15	VDD_CPGPLL2	-	P	VDD_CPGPLL2	P	-
195	G15	VSS_CPGPLL2	-	P	VSS_CPGPLL2	P	-
196	N4	VDD_CPGPLL0	-	P	VDD_CPGPLL0	P	-
197	N5	VSS_CPGPLL0	-	P	VSS_CPGPLL0	P	-
198	N7	VDD_CPGPLL3	-	P	VDD_CPGPLL3	P	-

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
199	N6	VSS_CPGPLL3	-	P	VSS_CPGPLL3	P	-
200	AF16	PRESET#	I	I(L)	PRESET#	I	-
201	AJ1	PRESETOUT#	O	L	PRESETOUT#	L to H	-
202	AE15	MPMD0	I	I	MPMD0	I	-
203	AJ14	MPMD1	I	I	MPMD1	I	-
204	AE13	BSMODE	I	I	BSMODE	I	-
205	AA25	AVS1	O	L	AVS1	H or L*4	Off
206	AB26	AVS2	O	L	AVS2	H or L*4	Off
207	AE16	VCCQ_ISO	-	P	VCCQ_ISO	P	-
208	AF9	D0	IO	I	D0/GP0_0*5	I	On
209	AG9	D1	IO	I	D1/GP0_1*5	I	On
210	AH9	D2	IO	I	D2/GP0_2*5	I	On
211	AJ9	D3	IO	I	D3/GP0_3*5	I	On
212	AK9	D4	IO	I	D4/GP0_4*5	I	On
213	AL9	D5	IO	I	D5/GP0_5*5	I	On
214	AF8	D6	IO	I	D6/GP0_6*5	I	On
215	AG8	D7	IO	I	D7/GP0_7*5	I	On
216	AH8	D8	IO	I	D8/GP0_8*5	I	On
217	AJ8	D9	IO	I	D9/GP0_9*5	I	On
218	AK8	D10	IO	I	D10/GP0_10*5	I	On
219	AL8	D11	IO	I	D11/GP0_11*5	I	On
220	AF7	D12	IO	I	D12/GP0_12*5	I	On
221	AG7	D13	IO	I	D13/GP0_13*5	I	On
222	AJ7	D14	IO	I	D14/GP0_14*5	I	On
223	AK7	D15	IO	I	D15/GP0_15*5	I	On
224	AL7	A0	IO	I(MD28)	A0/GP0_16*5	L/I	Off
225	AG6	A1	IO	I(MD27)	A1/GP0_17*5	L/I	Off
226	AH6	A2	IO	I(MD26)	A2/GP0_18*5	L/I	Off
227	AJ6	A3	IO	I(MD25)	A3/GP0_19*5	L/I	Off
228	AL6	A4	IO	I(MD24)	A4/GP0_20*5	L/I	Off
229	AH5	A5	IO	I(MD23)	A5/GP0_21*5	L/I	Off
230	AJ5	A6	IO	I(MD22)	A6/GP0_22*5	L/I	Off
231	AK5	A7	IO	I(MD21)	A7/GP0_23*5	L/I	Off
232	AL5	A8	IO	I	A8/GP0_24*5	L/I	On
233	AJ4	A9	IO	I	A9/GP0_25*5	L/I	On
234	AK4	A10	IO	I	A10/GP0_26*5	L/I	On
235	AL4	A11	IO	I	A11/GP0_27*5	L/I	On
236	AK3	A12	IO	I	A12/GP0_28*5	L/I	On
237	AL3	A13	IO	I	A13/GP0_29*5	L/I	On
238	AL2	A14	IO	I(MD20)	A14/GP0_30*5	L/I	Off
239	AH3	A15	IO	I(MD19)	A15GP0_31*5	L/I	Off
240	AG1	A16	IO	I(MD18)	A16/GP1_0*5	L/I	Off
241	AG2	A17	IO	I(MD17)	A17/GP1_1*5	L/I	Off
242	AG3	A18	IO	I(MD15)	A18/GP1_2*5	L/I	Off
243	AG4	A19	IO	I(MD14)	A19/GP1_3*5	L/I	Off
244	AF1	A20	IO	I	A20/GP1_4*5	L/I	On
245	AF2	A21	IO	I	A21/GP1_5*5	L/I	On
246	AF3	A22	IO	I	A22/GP1_6*5	L/I	On
247	AF4	A23	IO	I	A23/GP1_7*5	L/I	On
248	AF5	A24	IO	I	A24/GP1_8*5	L/I	On

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
249	AE6	A25	IO	I	A25/GP1_9*5	L/I	On
250	AE1	CLKOUT	O	O	CLKOUT	O	-
251	AD1	CS0#	IO	I	CS0#/GP1_10*5	H/I	On
252	AJ2	CS1#/A26	IO	I	[CS1#/A26]/GP1_11*5	[H or L]*6/I	On
253	AC1	EX_CS0#	IO	I	GP1_12	I	On
254	AC2	EX_CS1#	IO	I	GP1_13	I	On
255	AC3	EX_CS2#	IO	I	GP1_14	I	On
256	AC4	EX_CS3#	IO	I	GP1_15	I	On
257	AE3	EX_CS4#	IO	I	GP1_16	I	On
258	AE4	EX_CS5#	IO	I	GP1_17	I	On
259	AE5	BS#	IO	I(MD13)	BS#/GP1_18*5	H/I	Off
260	AD3	RD#	IO	I(MD16)	RD#/GP1_19*5	H/I	Off
261	AD2	RD/WR#	IO	I	GP1_20	I	On
262	AH1	WE0#	IO	I	WE0#/GP1_21*5	H/I	On
263	AH2	WE1#	IO	I	WE1#/GP1_22*5	H/I	On
264	AK1	EX_WAIT0	IO	I	EX_WAIT0/GP1_23*5	I/I	On
265	AC5	DREQ0	IO	I	GP1_24	I	On
266	AC6	DACK0	IO	I	GP1_25	I	On
267	AD5	DREQ1	IO	I	GP1_26	I	On
268	AD4	DACK1	IO	I	GP1_27	I	On
269	AD7	DREQ2	IO	I	GP1_28	I	On
270	AD6	DACK2	IO	I	GP1_29	I	On
271	AH11	ETH_CRS_DV	IO	I	GP2_18	I	On
272	AG11	ETH_RX_ER	IO	I	GP2_19	I	On
273	AF11	ETH_RXD0	IO	I	GP2_20	I	On
274	AE11	ETH_RXD1	IO	I	GP2_21	I	On
275	AK10	ETH_LINK	IO	I	GP2_22	I	On
276	AL10	ETH_REF_CLK	IO	I	GP2_23	I	On
277	AJ10	ETH_MDIO	IO	I	GP2_24	I	On
278	AH10	ETH_TXD1	IO	I(MD12)	GP2_25	I	Off
279	AG10	ETH_TX_EN	IO	I(MD11)	GP2_26	I	Off
280	AF10	ETH_MAGIC	IO	I(MD10)	GP2_27	I	Off
281	AE10	ETH_TXD0	IO	I(MD9)	GP2_28	I	Off
282	AE9	ETH_MDC	IO	I(MD8)	GP2_29	I	Off
283	AE12	PWM0	IO	I(MD7)	GP5_29	I	Off
284	AK11	PWM1	IO	I(MD6)	GP5_30	I	Off
285	AJ11	PWM2	IO	I	GP5_31	I	On
286	AG12	NMI	I	I	NMI	I	-
287	AG16	TRST#	I	I	TRST#	I	On
288	AE14	TCK	I	I	TCK	I	On
289	AF14	TMS	I	I	TMS	I	On
290	AH14	TDI	I	I	TDI	I	On
291	AH12	TDO	O	Z	TDO	Z	-
292	AF13	ACK	IO	I	ACK	I	On (pull-down)
293	AG17	DU_LVDS0_CLK_P	O	Z	DU_LVDS0_CLK_P	Z	-
294	AG18	DU_LVDS0_CLK_N	O	Z	DU_LVDS0_CLK_N	Z	-
295	AJ18	DU_LVDS0_CH0_P	O	Z	DU_LVDS0_CH0_P	Z	-
296	AJ19	DU_LVDS0_CH0_N	O	Z	DU_LVDS0_CH0_N	Z	-

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
297	AG19	DU_LVDS0_CH1_P	O	Z	DU_LVDS0_CH1_P	Z	-
298	AG20	DU_LVDS0_CH1_N	O	Z	DU_LVDS0_CH1_N	Z	-
299	AL18	DU_LVDS0_CH2_P	O	Z	DU_LVDS0_CH2_P	Z	-
300	AL17	DU_LVDS0_CH2_N	O	Z	DU_LVDS0_CH2_N	Z	-
301	AJ17	DU_LVDS0_CH3_P	O	Z	DU_LVDS0_CH3_P	Z	-
302	AJ16	DU_LVDS0_CH3_N	O	Z	DU_LVDS0_CH3_N	Z	-
303	AJ13	DU_DOTCLKIN0	IO	I	GP5_26	I	On
304	AD18	VDDQ_LVDS	-	P	VDDQ_LVDS	P	-
305	AE18	VDDQ_LVDS	-	P	VDDQ_LVDS	P	-
306	AF18	VDDQ_LVDS	-	P	VDDQ_LVDS	P	-
307	AE20	DU_LVDS0_PLL1_VCC	-	P	DU_LVDS0_PLL1_VCC	P	-
308	AD19	DU_LVDS0_PLL1_VSS	-	P	DU_LVDS0_PLL1_VSS	P	-
309	AL19	DU_LVDS1_CLK_P	O	Z	DU_LVDS1_CLK_P	Z	-
310	AL20	DU_LVDS1_CLK_N	O	Z	DU_LVDS1_CLK_N	Z	-
311	AJ23	DU_LVDS1_CH0_P	O	Z	DU_LVDS1_CH0_P	Z	-
312	AJ22	DU_LVDS1_CH0_N	O	Z	DU_LVDS1_CH0_N	Z	-
313	AL21	DU_LVDS1_CH1_P	O	Z	DU_LVDS1_CH1_P	Z	-
314	AL22	DU_LVDS1_CH1_N	O	Z	DU_LVDS1_CH1_N	Z	-
315	AJ20	DU_LVDS1_CH2_P	O	Z	DU_LVDS1_CH2_P	Z	-
316	AJ21	DU_LVDS1_CH2_N	O	Z	DU_LVDS1_CH2_N	Z	-
317	AG22	DU_LVDS1_CH3_P	O	Z	DU_LVDS1_CH3_P	Z	-
318	AG21	DU_LVDS1_CH3_N	O	Z	DU_LVDS1_CH3_N	Z	-
319	AH13	DU_DOTCLKIN1	IO	I	GP5_27	I	On
320	AD22	VDDQ_LVDS	-	P	VDDQ_LVDS	P	-
321	AE22	VDDQ_LVDS	-	P	VDDQ_LVDS	P	-
322	AF22	VDDQ_LVDS	-	P	VDDQ_LVDS	P	-
323	AD20	DU_LVDS1_PLL1_VCC	-	P	DU_LVDS1_PLL1_VCC	P	-
324	AD21	DU_LVDS1_PLL1_VSS	-	P	DU_LVDS1_PLL1_VSS	P	-
325	AJ12	DU_DOTCLKIN2	IO	I	DU_DOTCLKIN2	I	On
326	Y1	VI0_CLK	IO	I	GP2_0	I	On
327	Y6	VI0_DATA0/VI0_B0	IO	I	GP2_1	I	On
328	Y5	VI0_DATA1/VI0_B1	IO	I	GP2_2	I	On
329	Y4	VI0_DATA2/VI0_B2	IO	I	GP2_3	I	On
330	Y3	VI0_DATA3/VI0_B3	IO	I	GP2_4	I	On
331	W7	VI0_DATA4/VI0_B4	IO	I	GP2_5	I	On
332	W6	VI0_DATA5/VI0_B5	IO	I	GP2_6	I	On
333	AA6	VI0_DATA6/VI0_B6	IO	I	GP2_7	I	On
334	AA5	VI0_DATA7/VI0_B7	IO	I	GP2_8	I	On
335	AB1	VI1_CLK	IO	I	GP2_9	I	On
336	AA4	VI1_DATA0/VI1_B0	IO	I	GP2_10	I	On
337	AA3	VI1_DATA1/VI1_B1	IO	I	GP2_11	I	On
338	AB7	VI1_DATA2/VI1_B2	IO	I	GP2_12	I	On
339	AB6	VI1_DATA3/VI1_B3	IO	I	GP2_13	I	On
340	AB4	VI1_DATA4/VI1_B4	IO	I	GP2_14	I	On
341	AB3	VI1_DATA5/VI1_B5	IO	I	GP2_15	I	On
342	AA2	VI1_DATA6/VI1_B6	IO	I	GP2_16	I	On
343	AA1	VI1_DATA7/VI1_B7	IO	I	GP2_17	I	On
344	V1	SD0_CLK	IO	I/Z*7	GP3_0/TDO2*8	I/Z*7	Off/-*9
345	V4	SD0_CMD	IO	I	GP3_1/TRST2#*8	I/I	Off/-*9
346	W2	SD0_DAT0	IO	I	GP3_2/TCK2*8	I/I	Off/-*9

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
347	V7	SD0_DAT1	IO	I	GP3_3/TMS2*8	I/I	Off/-*9
348	V6	SD0_DAT2	IO	I	GP3_4/TDI2*8	I/I	Off/-*9
349	V5	SD0_DAT3	IO	I	GP3_5*8	I/I	Off/-*9
350	W3	SD0_CD	IO	I	GP3_6	I	Off
351	W4	SD0_WP	IO	I	GP3_7	I	Off
352	W8	VCCQ_SD0	-	P	VCCQ_SD0	P	-
353	U1	SD1_CLK	IO	I/Z*7	GP3_8/TDO3*8	I/Z*7	Off/-*9
354	T6	SD1_CMD	IO	I	GP3_9/TRST3#*8	I/I	Off/-*9
355	U6	SD1_DAT0	IO	I	GP3_10//TCK3*8	I/I	Off/-*9
356	U4	SD1_DAT1	IO	I	GP3_11/TMS3*8	I/I	Off/-*9
357	U3	SD1_DAT2	IO	I	GP3_12/TDI3*8	I/I	Off/-*9
358	T7	SD1_DAT3	IO	I	GP3_13*8	I/I	Off/-*9
359	U7	SD1_CD	IO	I	GP3_14	I	Off
360	V3	SD1_WP	IO	I	GP3_15	I	Off
361	U8	VCCQ_SD1	-	P	VCCQ_SD1	P	-
362	R1	SD2_CLK	IO	I	GP3_16	I	Off
363	T4	SD2_CMD	IO	I	GP3_17	I	Off
364	R5	SD2_DAT0	IO	I	GP3_18	I	Off
365	R4	SD2_DAT1	IO	I	GP3_19	I	Off
366	R3	SD2_DAT2	IO	I	GP3_20	I	Off
367	T5	SD2_DAT3	IO	I	GP3_21	I	Off
368	T2	SD2_CD	IO	I	GP3_22	I	Off
369	T3	SD2_WP	IO	I	GP3_23	I	Off
370	T8	VCCQ_SD2	-	P	VCCQ_SD2	P	-
371	P1	SD3_CLK	IO	I	GP3_24	I	Off
372	P5	SD3_CMD	IO	I	GP3_25	I	Off
373	R7	SD3_DAT0	IO	I	GP3_26	I	Off
374	R6	SD3_DAT1	IO	I	GP3_27	I	Off
375	P4	SD3_DAT2	IO	I	GP3_28	I	Off
376	P3	SD3_DAT3	IO	I	GP3_29	I	Off
377	P6	SD3_CD	IO	I	GP3_30	I	Off
378	P7	SD3_WP	IO	I	GP3_31	I	Off
379	P8	VCCQ_SD3	-	P	VCCQ_SD3	P	-
380	L31	NC	-	Z	Reserved	Z	-
381	K31	NC	-	Z	Reserved	Z	-
382	N31	NC	-	Z	Reserved	Z	-
383	M31	NC	-	Z	Reserved	Z	-
384	L29	NC	-	Z	Reserved	Z	-
385	L28	NC	-	Z	Reserved	Z	-
386	M29	NC	-	Z	Reserved	Z	-
387	M28	NC	-	Z	Reserved	Z	-
388	N28	VCCQ18_MLBP	-	P	VCCQ18_MLBP	P	-
389	L25	VDD_MLBPPLL0	-	P	VDD_MLBPPLL0	P	-
390	M25	VSS_MLBPPLL0	-	P	VSS_MLBPPLL0	P	-
391	L26	VDD_MLBPPLL1	-	P	VDD_MLBPPLL1	P	-
392	M26	VSS_MLBPPLL1	-	P	VSS_MLBPPLL1	P	-
393	AB31	NC	-	I	GP4_0	I	-
394	AC31	NC	-	I	GP4_1	I	-
395	AA31	NC	-	I	GP4_2	I	-
396	AB29	NC	-	IO	Reserved	IO	-

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
397	AA27	VDD_MLBPLL	-	P	VDD_MLBPLL	P	-
398	AA26	VSS_MLBPLL	-	P	VSS_MLBPLL	P	-
399	P31	SSI_SCK0129	IO	I	GP4_3	I	On
400	P30	SSI_WS0129	IO	I	GP4_4	I	On
401	P29	SSI_SDATA0	IO	I	GP4_5	I	On
402	P27	SSI_SDATA1	IO	I	GP4_6	I	On
403	R26	SSI_SDATA2	IO	I	GP4_7	I	On
404	R31	SSI_SCK34	IO	I	GP4_8	I	On
405	R28	SSI_WS34	IO	I	GP4_9	I	On
406	R27	SSI_SDATA3	IO	I	GP4_10	I	On
407	T31	SSI_SCK4	IO	I	GP4_11	I	On
408	T29	SSI_WS4	IO	I	GP4_12	I	On
409	R29	SSI_SDATA4	IO	I	GP4_13	I	On
410	U31	SSI_SCK5	IO	I	GP4_14	I	On
411	U30	SSI_WS5	IO	I	GP4_15	I	On
412	P26	SSI_SDATA5	IO	I	GP4_16	I	On
413	U29	SSI_SCK6	IO	I	GP4_17	I	On
414	U27	SSI_WS6	IO	I	GP4_18	I	On
415	T25	SSI_SDATA6	IO	I	GP4_19	I	On
416	V29	SSI_SCK78	IO	I	GP4_20	I	On
417	U28	SSI_WS78	IO	I	GP4_21	I	On
418	T26	SSI_SDATA7	IO	I	GP4_22	I	On
419	T28	SSI_SDATA8	IO	I	GP4_23	I	On
420	R25	SSI_SDATA9	IO	I	GP4_24	I	On
421	V31	AUDIO_CLKA	IO	I	GP4_25	I	On
422	W31	AUDIO_CLKB	IO	I	GP4_26	I	On
423	AA30	SCIFA0_SCK	IO	I	GP4_27	I	On
424	AA29	SCIFA0_RXD	IO	I	GP4_28	I	On
425	Y30	SCIFA0_TXD	IO	I (MD5)	GP4_29	I	Off
426	W25	SCIFA0_CTS#	IO	I	GP4_30	I	On
427	Y29	SCIFA0_RTS#	IO	I (MD4)	GP4_31	I	Off
428	Y28	SCIFA1_RXD	IO	I	GP5_0	I	On
429	Y27	SCIFA1_TXD	IO	I (MD3)	GP5_1	I	Off
430	Y25	SCIFA1_CTS#	IO	I	GP5_2	I	On
431	Y26	SCIFA1_RTS#	IO	I (MD2)	GP5_3	I	Off
432	AB28	SCIFA2_SCK	IO	I	GP5_4	I	On
433	AC27	SCIFA2_RXD	IO	I	GP5_5	I	On
434	AB27	SCIFA2_TXD	IO	I	GP5_6	I	On
435	V28	HSCK0	IO	I	GP5_7	I	On
436	V26	HRX0	IO	I	GP5_8	I	On
437	V27	HTX0	IO	I (MD1)	GP5_9	I	Off
438	U26	HCTS0#	IO	I	GP5_10	I	On
439	U25	HRTS0#	IO	I	GP5_11	I	On
440	Y31	MSIOF0_SCK	IO	I	GP5_12	I	On
441	V25	MSIOF0_SYNC	IO	I	GP5_13	I	On
442	W28	MSIOF0_SS1	IO	I (MD0)	GP5_14	I	Off
443	W29	MSIOF0_TXD	IO	I (MDT1)	GP5_15	I	Off
444	W26	MSIOF0_SS2	IO	I (MDT0)	GP5_16	I	Off
445	W27	MSIOF0_RXD	IO	I	GP5_17	I	On
446	AG15	IIC0_SCL	IO	Z	IIC0_SCL	Z	-

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
447	AF15	IIC0_SDA	IO	Z	IIC0_SDA	Z	-
448	AJ15	IIC3_SCL	IO	Z	IIC3_SCL	Z	-
449	AH15	IIC3_SDA	IO	Z	IIC3_SDA	Z	-
450	AL14	USB_EXTAL	I	I	USB_EXTAL	I	-
451	AL15	USB_XTAL	O	O	USB_XTAL	O	-
452	AC24	AVSS	-	P	AVSS	P	-
453	AD25	AVSS	-	P	AVSS	P	-
454	AE26	AVSS	-	P	AVSS	P	-
455	AF31	USB0_DP	IO	I	USB0_DP	I	-
456	AE31	USB0_DM	IO	I	USB0_DM	I	-
457	AF29	USB0_RREF	-	P	USB0_RREF	P	-
458	AE28	VD331	-	P	VD331	P	-
459	AB25	VD181	-	P	VD181	P	-
460	AB24	AVDD	-	P	AVDD	P	-
461	AC25	AVDD	-	P	AVDD	P	-
462	AD31	VSS	-	P	VSS	P	-
463	AF27	AVSS	-	P	AVSS	P	-
464	AE30	VSS	-	P	VSS	P	-
465	AC28	USB0_PWEN	O	L	USB0_PWEN	L	Off
466	AD28	USB0_OVC/VBUS	I	I	USB0_OVC/VBUS	I	Off
467	AH31	USB1_DP	IO	I	USB1_DP	I	-
468	AG31	USB1_DM	IO	I	USB1_DM	I	-
469	AG29	USB1_RREF	-	P	USB1_RREF	I	-
470	AE29	VD331	-	P	VD331	I	-
471	AC26	VD181	-	P	VD181	I	-
472	AD26	AVDD	-	P	AVDD	I	-
473	AF30	VSS	-	P	VSS	I	-
474	AF28	AVSS	-	P	AVSS	I	-
475	AG30	VSS	-	P	VSS	I	-
476	AC29	USB1_PWEN	O	L	USB1_PWEN	L	Off
477	AD29	USB1_OVC	I	I	USB1_OVC	I	Off
478	AK31	USB2_DP	IO	I	USB2_DP	I	-
479	AJ31	USB2_DM	IO	I	USB2_DM	I	-
480	AH29	USB2_RREF	-	P	USB2_RREF	I	-
481	AD27	VD181	-	P	VD181	I	-
482	AE27	AVDD	-	P	AVDD	I	-
483	AH30	VSS	-	P	VSS	I	-
484	AG28	AVSS	-	P	AVSS	I	-
485	AJ30	VSS	-	P	VSS	I	-
486	AD30	USB2_PWEN	O	L	USB2_PWEN	L	Off
487	AC30	USB2_OVC	I	I	USB2_OVC	I	Off
488	AL23	RIDP1_SATA	I	I	RIDP1_SATA/RIDP1_PCIe*10	I	-
489	AL24	RIDN1_SATA	I	I	RIDN1_SATA/RIDN1_PCIe*10	I	-
490	AL25	TODP1_SATA	O	O	TODP1_SATA/TODP1_PCIe*10	O	-
491	AL26	TODN1_SATA	O	O	TODN1_SATA/TODN1_PCIe*10	O	-
492	AJ26	CICREFP1_SATA	I	I	CICREFP1_SATA/CICREFP1_PCIe*10	I	-
493	AJ25	CICREFN1_SATA	I	I	CICREFN1_SATA/CICREFN1_PCIe*10	I	-
494	AE23	VSS_SATA1	-	P	VSS_SATA1/VSS_PCIe*10	P	-
495	AF23	VDDD_SATA1	-	P	VDDD_SATA1/VDDD_PCIe*10	P	-
496	AD23	VSS_SATA1	-	P	VSS_SATA1/VSS_PCIe*10	P	-

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
497	AF24	VDDA_SATA1	-	P	VDDA_SATA1/VDDA_PCIe*10	P	-
498	AG24	VDDA_SATA1	-	P	VDDA_SATA1/VDDA_PCIe*10	P	-
499	AG23	VDDD_SATA1	-	P	VDDD_SATA1/VDDD_PCIe*10	P	-
500	AH24	VDDD_SATA1	-	P	VDDD_SATA1/VDDD_PCIe*10	P	-
501	AE24	VSS_SATA1	-	P	VSS_SATA1/VSS_PCIe*10	P	-
502	AJ24	VSS_SATA1	-	P	VSS_SATA1/VSS_PCIe*10	P	-
503	AK23	VSS_SATA1	-	P	VSS_SATA1/VSS_PCIe*10	P	-
504	AK24	VSS_SATA1	-	P	VSS_SATA1/VSS_PCIe*10	P	-
505	AK25	VSS_SATA1	-	P	VSS_SATA1/VSS_PCIe*10	P	-
506	AK26	VSS_SATA1	-	P	VSS_SATA1/VSS_PCIe*10	P	-
507	AL27	RIDP0_SATA	I	I	RIDP0_SATA/RIDP0_USB3*10	I/I	-
508	AL28	RIDN0_SATA	I	I	RIDN0_SATA/RIDN0_USB3*10	I/I	-
509	AL29	TODP0_SATA	O	O	TODP0_SATA/TODP0_USB3*10	O/O	-
510	AL30	TODN0_SATA	O	O	TODN0_SATA/TODN0_USB3*10	O/O	-
511	AJ28	CICREFP0_SATA	I	I	CICREFP0_SATA/CICREFP0_USB3*10	I/I	-
512	AJ27	CICREFN0_SATA	I	I	CICREFN0_SATA/CICREFN0_USB3*10	I/I	-
513	AF25	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3*10	P	-
514	AG25	VDDD_SATA0	-	P	VDDD_SATA0/VDDD_USB3*10	P	-
515	AD24	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3*10	P	-
516	AG26	VDDA_SATA0	-	P	VDDA_SATA0/VDDA_USB3*10	P	-
517	AH27	VDDA_SATA0	-	P	VDDA_SATA0/VDDA_USB3*10	P	-
518	AH25	VDDD_SATA0	-	P	VDDD_SATA0/VDDD_USB3*10	P	-
519	AH26	VDDD_SATA0	-	P	VDDD_SATA0/VDDD_USB3*10	P	-
520	AE25	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3*10	P	-
521	AF26	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3*10	P	-
522	AG27	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3*10	P	-
523	AH28	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3*10	P	-
524	AJ29	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3*10	P	-
525	AK27	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3*10	P	-
526	AK28	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3*10	P	-
527	AK29	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3*10	P	-
528	AK30	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3*10	P	-
529	AL31	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3*10	P	-
530	Y7	VTHSENSE0	O	O	VTHSENSE0	O	-
531	AA7	VTHREF0	O	O	VTHREF0	O	-

Notes: 1. No.94, 95, 98 to 106 and 108 to 129: Default pin function
MD[28:27], [22] = 111: DBSC3 channel 1 32-bit operation
MD[28:27], [22] = 011 or 110: GP_DDRn (n = 1 to 29) operation

2. No.134 to 187: Default pin function
MD[28:27], [22] = 111: DBSC3 channel 1 32-bit operation
MD[28:27], [22] = 011: DBSC channel 0 64-bit (M0DQ[63:32] enable) operation
MD[28:27], [22] = 110: Reserved except for power supply pins.

3. No.191: EXREFIN
Must be fixed to VSS (; not user application).

4. No.205 and 206: AVS default state
The output is high or low, depending on product.

5. No.208 to 249, 251, 252, 259, 260, and 262 to 264: Default pin function
MD[3:1] = 000: LBSC (D[15:0], A[25:0], CS0#, CS1#/A26, BS#, RD#, WE[1:0]#, and EX_WAIT0)
MD[3:1] ≠ 000: GPIO (GP0_[31:0], GP1_[11:0], [19:18], and [23:21])

6. No.252 CS1#/A26: Default state
   MD4 = 0: (64-Mbyte mode): high output
   MD4 = 1: (128-Mbyte mode): low output
7. No.344 and 353: Default state
   "I" is in function mode (SDHI), "Z" is in debug mode.
8. No.344 to 349 and 353 to 358: Default pin function
   Depends on MD[21:20], MD[12:10], and MDT[1:0] settings.
9. No.344 to 349 and 353 to 358: Default pull-up
   "-" is in debugging operation only; "Off" is in other than debugging operation.
10. No.488 to 529: Default pin function
    MD[24:23] = 00: SATA1 and SATA0
    MD[24:23] = 01: SATA1 and USB3.0
    MD[24:23] = 10: PCIe and SATA0
    MD[24:23] = 11: PCIe and USB3.0

Note for DBSC3 DQS/DQS# states. ** (No.47/48, 61/62, 74/75, 88/89, 142/143, 156/157, 169/170, 183/184):

The drivers output states are both high-impedance (Z), and the internal circuit controls pin levels as low-level for the MnDQSx pins and high-level for the MnDQSx# pins respectively.

4.3 Handling of Unused Pins

Table 4.3 shows a handling of unused pins of the RZ/G1H.

"Unused pin" means all pin functions of the pin are unused and all modules that have the pin are unused in this section. For handling of some unused pin which belongs to the enable module should be handled following the notification of the module manual. Unless otherwise specified in the module manual, follow the Table 4.3 for handling of unused pins.

[Legend]

No.: Serial number, Pin No.: BGA package ball grid number, Pin Name: Pin name of function 1 in pin multiplex table, Default State: Pin state of default pin function (function 1 or GPIO etc.).

Mode Pin: All mode pins must be used during power-on reset.

Boot: These pins must be used in boot operation (LBSC area 0 or QSPI).

Default pull-up: Internal pull-up control function is available or not from a power-on reset and its pull-up state.

"On": Pull-up control function is available and default state is pulled-up.

(No.292, ACK pin is available internal pull-down function.)

"Off": Pull-up control function is available and default state is not pulled-up.

"-": Pulled-up control function is not available.

For details of pull-up control function, refer to PUPR0 through PUPR6 registers in section 5, Pin Function Controller (PFC).

Notes: 1. All power supply pins and ground pins include VCCQ, VCCQ18, VDD, VDD_DVFS, VDDQ_M0, VDDQ_M1, VDDQ_M1A, and VSS pins must be used.

2. All mode pins (MD[28:0] and MDT[1:0]) must be used during power-on reset. For details of mode pin setting, refer to section 3.3, Mode Pin Settings.

3. Boot module related pins (LBSC or QSPI) should be used during boot operation. For details of QSPI boot, refer to section 18, Booting.

Table 4.3 Handling of Unused Pins

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
1	F20	M0CKE0	L	-	-	-	Open
2	C19	M0CKE1	L	-	-	-	Open
3	G16	M0VREFCA(VSS)	P	-	-	-	Must be used
4	H18	M0BKPRST#	I	-	-	-	Pulled-up to VDDQ_M0BKUP or pulled-down to VSS
5	E19	M0RESET#	H to L	-	-	-	Open
6	G20	M0CK0	O	-	-	-	Open
7	G19	M0CK0#	O	-	-	-	Open
8	G17	M0CK1	O	-	-	-	Open
9	G18	M0CK1#	O	-	-	-	Open
10	B20	M0CS0#	H	-	-	-	Open
11	A19	M0CS1#	H	-	-	-	Open
12	D20	M0ODT0	L	-	-	-	Open
13	E18	M0ODT1	L	-	-	-	Open
14	H16	M0ZQ	IO	-	-	-	Must be used
15	E21	M0WE#	H	-	-	-	Open
16	D22	M0RAS#	H	-	-	-	Open
17	C22	M0CAS#	H	-	-	-	Open
18	E17	M0A0	L	-	-	-	Open
19	B22	M0A1	L	-	-	-	Open
20	A22	M0A2	L	-	-	-	Open
21	D17	M0A3	L	-	-	-	Open
22	A21	M0A4	L	-	-	-	Open
23	D16	M0A5	L	-	-	-	Open
24	B17	M0A6	L	-	-	-	Open
25	B21	M0A7	L	-	-	-	Open
26	A16	M0A8	L	-	-	-	Open
27	B18	M0A9	L	-	-	-	Open
28	C18	M0A10	L	-	-	-	Open
29	A18	M0A11	L	-	-	-	Open
30	E16	M0A12	L	-	-	-	Open
31	A17	M0A13	L	-	-	-	Open
32	B16	M0A14	L	-	-	-	Open
33	D18	M0A15	L	-	-	-	Open
34	C21	M0BA0	L	-	-	-	Open
35	C16	M0BA1	L	-	-	-	Open
36	D21	M0BA2	L	-	-	-	Open
37	G21	VDDQ_M0APLL	P	-	-	-	Must be used
38	H21	VSSQ_M0APLL	P	-	-	-	Must be used
39	A27	M0DQ0	Z	-	-	-	Open
40	C28	M0DQ1	Z	-	-	-	Open
41	D27	M0DQ2	Z	-	-	-	Open
42	A29	M0DQ3	Z	-	-	-	Open
43	B27	M0DQ4	Z	-	-	-	Open
44	B29	M0DQ5	Z	-	-	-	Open
45	C27	M0DQ6	Z	-	-	-	Open
46	A30	M0DQ7	Z	-	-	-	Open
47	E26	M0DQS0	Z**	-	-	-	Open
48	E25	M0DQS0#	Z**	-	-	-	Open

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
49	A28	M0DM0	Z	-	-	-	Open
50	G22	VDDQ_M0DPLL0	P	-	-	-	Must be used
51	G23	VSSQ_M0DPLL0	P	-	-	-	Must be used
52	G24	M0VREFDQ0	P	-	-	-	Must be used
53	B23	M0DQ8	Z	-	-	-	Open
54	A24	M0DQ9	Z	-	-	-	Open
55	C24	M0DQ10	Z	-	-	-	Open
56	D24	M0DQ11	Z	-	-	-	Open
57	B26	M0DQ12	Z	-	-	-	Open
58	D26	M0DQ13	Z	-	-	-	Open
59	B24	M0DQ14	Z	-	-	-	Open
60	A25	M0DQ15	Z	-	-	-	Open
61	E23	M0DQS1	Z**	-	-	-	Open
62	E24	M0DQS1#	Z**	-	-	-	Open
63	C25	M0DM1	Z	-	-	-	Open
64	F22	VDDQ_M0DPLL1	P	-	-	-	Must be used
65	F23	VSSQ_M0DPLL1	P	-	-	-	Must be used
66	E31	M0DQ16	Z	-	-	-	Open
67	C30	M0DQ17	Z	-	-	-	Open
68	E29	M0DQ18	Z	-	-	-	Open
69	B31	M0DQ19	Z	-	-	-	Open
70	E30	M0DQ20	Z	-	-	-	Open
71	C31	M0DQ21	Z	-	-	-	Open
72	E28	M0DQ22	Z	-	-	-	Open
73	D29	M0DQ23	Z	-	-	-	Open
74	F27	M0DQS2	Z**	-	-	-	Open
75	G27	M0DQS2#	Z**	-	-	-	Open
76	D31	M0DM2	Z	-	-	-	Open
77	K25	VDDQ_M0DPLL2	P	-	-	-	Must be used
78	J25	VSSQ_M0DPLL2	P	-	-	-	Must be used
79	H25	M0VREFDQ1	P	-	-	-	Must be used
80	F28	M0DQ24	Z	-	-	-	Open
81	G31	M0DQ25	Z	-	-	-	Open
82	F30	M0DQ26	Z	-	-	-	Open
83	H30	M0DQ27	Z	-	-	-	Open
84	H28	M0DQ28	Z	-	-	-	Open
85	J30	M0DQ29	Z	-	-	-	Open
86	H29	M0DQ30	Z	-	-	-	Open
87	H31	M0DQ31	Z	-	-	-	Open
88	J27	M0DQS3	Z**	-	-	-	Open
89	H27	M0DQS3#	Z**	-	-	-	Open
90	G29	M0DM3	Z	-	-	-	Open
91	K26	VDDQ_M0DPLL3	P	-	-	-	Must be used
92	J26	VSSQ_M0DPLL3	P	-	-	-	Must be used
93	H19	VDDQ_M0BKUP	P	-	-	-	Must be used
94	F5	M1CKE0	O	-	-	-	Open
95	G3	M1CKE1	O	-	-	-	Open
96	H7	M1VREFCA	P	-	-	-	Must be used
97	J7	M1BKPRST#	I	-	-	-	Pulled-up to VDDQ_M1BKUP or pulled-down to VSS
98	G5	M1RESET#	O	-	-	-	Open

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
99	J5	M1CK0	O	-	-	-	Open
100	H5	M1CK0#	O	-	-	-	Open
101	L5	M1CK1	O	-	-	-	Open
102	K5	M1CK1#	O	-	-	-	Open
103	F2	M1CS0#	H/I	-	-	-	Open
104	G1	M1CS1#	H/I	-	-	-	Open
105	F4	M1ODT0	L/I	-	-	-	Open
106	H4	M1ODT1	L/I	-	-	-	Open
107	L8	M1ZQ	IO	-	-	-	Must be used
108	E3	M1WE#	H/Z	-	-	-	Open
109	D3	M1RAS#	H/Z	-	-	-	Open
110	E4	M1CAS#	H/I	-	-	-	Open
111	B1	M1A0	L/Z	-	-	-	Open
112	H2	M1A1	L/I	-	-	-	Open
113	E2	M1A2	L/Z	-	-	-	Open
114	M3	M1A3	L/I	-	-	-	Open
115	E1	M1A4	L/Z	-	-	-	Open
116	D1	M1A5	L/Z	-	-	-	Open
117	K2	M1A6	L/Z	-	-	-	Open
118	H1	M1A7	L/I	-	-	-	Open
119	M1	M1A8	L/I	-	-	-	Open
120	J2	M1A9	L/Z	-	-	-	Open
121	L3	M1A10	L/I	-	-	-	Open
122	K1	M1A11	L/Z	-	-	-	Open
123	C2	M1A12	L/Z	-	-	-	Open
124	L1	M1A13	L/I	-	-	-	Open
125	M2	M1A14	L/I	-	-	-	Open
126	K3	M1A15	L/Z	-	-	-	Open
127	J3	M1BA0	L/Z	-	-	-	Open
128	C1	M1BA1	L/Z	-	-	-	Open
129	H3	M1BA2	L/I	-	-	-	Open
130	L7	VDDQ_M1APLL	P	-	-	-	Must be used
131	K7	VSSQ_M1APLL	P	-	-	-	Must be used
132	L6	VDDQ_M1MPLL	P	-	-	-	Must be used
133	K6	VSSQ_M1MPLL	P	-	-	-	Must be used
134	B12	M1DQ0	Z	-	-	-	Open
135	B11	M1DQ1	Z	-	-	-	Open
136	D12	M1DQ2	Z	-	-	-	Open
137	A10	M1DQ3	Z	-	-	-	Open
138	C11	M1DQ4	Z	-	-	-	Open
139	D10	M1DQ5	Z	-	-	-	Open
140	C10	M1DQ6	Z	-	-	-	Open
141	D11	M1DQ7	Z	-	-	-	Open
142	E12	M1DQS0	Z**	-	-	-	Open
143	E11	M1DQS0#	Z**	-	-	-	Open
144	A11	M1DM0	Z	-	-	-	Open
145	G13	VDDQ_M1DPLL0	P	-	-	-	Must be used
146	G12	VSSQ_M1DPLL0	P	-	-	-	Must be used
147	G14	M1VREFDQ0	P	-	-	-	Must be used
148	A13	M1DQ8	Z	-	-	-	Open

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
149	A14	M1DQ9	Z	-	-	-	Open
150	D14	M1DQ10	Z	-	-	-	Open
151	B14	M1DQ11	Z	-	-	-	Open
152	C14	M1DQ12	Z	-	-	-	Open
153	B15	M1DQ13	Z	-	-	-	Open
154	D15	M1DQ14	Z	-	-	-	Open
155	A15	M1DQ15	Z	-	-	-	Open
156	E14	M1DQS1	Z**	-	-	-	Open
157	E13	M1DQS1#	Z**	-	-	-	Open
158	C13	M1DM1	Z	-	-	-	Open
159	F13	VDDQ_M1DPLL1	P	-	-	-	Must be used
160	F12	VSSQ_M1DPLL1	P	-	-	-	Must be used
161	B6	M1DQ16	Z	-	-	-	Open
162	A7	M1DQ17	Z	-	-	-	Open
163	C8	M1DQ18	Z	-	-	-	Open
164	B8	M1DQ19	Z	-	-	-	Open
165	D8	M1DQ20	Z	-	-	-	Open
166	A8	M1DQ21	Z	-	-	-	Open
167	D6	M1DQ22	Z	-	-	-	Open
168	B9	M1DQ23	Z	-	-	-	Open
169	E8	M1DQS2	Z**	-	-	-	Open
170	E9	M1DQS2#	Z**	-	-	-	Open
171	C7	M1DM2	Z	-	-	-	Open
172	F10	VDDQ_M1DPLL2	P	-	-	-	Must be used
173	F9	VSSQ_M1DPLL2	P	-	-	-	Must be used
174	G8	M1VREFDQ1	P	-	-	-	Must be used
175	B3	M1DQ24	Z	-	-	-	Open
176	D5	M1DQ25	Z	-	-	-	Open
177	C4	M1DQ26	Z	-	-	-	Open
178	C5	M1DQ27	Z	-	-	-	Open
179	A5	M1DQ28	Z	-	-	-	Open
180	A3	M1DQ29	Z	-	-	-	Open
181	B5	M1DQ30	Z	-	-	-	Open
182	A2	M1DQ31	Z	-	-	-	Open
183	E7	M1DQS3	Z**	-	-	-	Open
184	E6	M1DQS3#	Z**	-	-	-	Open
185	A4	M1DM3	Z	-	-	-	Open
186	G10	VDDQ_M1DPLL3	P	-	-	-	Must be used
187	G9	VSSQ_M1DPLL3	P	-	-	-	Must be used
188	G6	VDDQ_M1BKUP	P	-	-	-	Must be used
189	AL12	EXTAL	I	-	-	-	Must be used
190	AL13	XTAL	O	-	-	-	Open
191	AF12	EXREFIN	I	-	-	-	Must be used and must be fixed to VSS
192	F16	VDD_CPGPLL1	P	-	-	-	Must be used
193	F15	VSS_CPGPLL1	P	-	-	-	Must be used
194	H15	VDD_CPGPLL2	P	-	-	-	Must be used
195	G15	VSS_CPGPLL2	P	-	-	-	Must be used
196	N4	VDD_CPGPLL0	P	-	-	-	Must be used
197	N5	VSS_CPGPLL0	P	-	-	-	Must be used
198	N7	VDD_CPGPLL3	P	-	-	-	Must be used

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
199	N6	VSS_CPGPLL3	P	-	-	-	Must be used
200	AF16	PRESET#	I	-	-	-	Must be used
201	AJ1	PRESETOUT#	L to H	-	-	-	Open
202	AE15	MPMD0	I	-	-	-	Must be used (pulled-down to VSS)
203	AJ14	MPMD1	I	-	-	-	Must be used (pulled-down to VSS)
204	AE13	BSMODE	I	-	-	-	Must be used
205	AA25	AVS1	O	-	-	Off	Open
206	AB26	AVS2	O	-	-	Off	Open
207	AE16	VCCQ_ISO	P	-	-	-	Must be used
208	AF9	D0	I	-	Area 0*1	On	Open
209	AG9	D1	I	-	Area 0*1	On	Open
210	AH9	D2	I	-	Area 0*1	On	Open
211	AJ9	D3	I	-	Area 0*1	On	Open
212	AK9	D4	I	-	Area 0*1	On	Open
213	AL9	D5	I	-	Area 0*1	On	Open
214	AF8	D6	I	-	Area 0*1	On	Open
215	AG8	D7	I	-	Area 0*1	On	Open
216	AH8	D8	I	-	Area 0*1	On	Open
217	AJ8	D9	I	-	Area 0*1	On	Open
218	AK8	D10	I	-	Area 0*1	On	Open
219	AL8	D11	I	-	Area 0*1	On	Open
220	AF7	D12	I	-	Area 0*1	On	Open
221	AG7	D13	I	-	Area 0*1	On	Open
222	AJ7	D14	I	-	Area 0*1	On	Open
223	AK7	D15	I	-	Area 0*1	On	Open
224	AL7	A0	L/I	MD28	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
225	AG6	A1	L/I	MD27	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
226	AH6	A2	L/I	MD26	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
227	AJ6	A3	L/I	MD25	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
228	AL6	A4	L/I	MD24	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
229	AH5	A5	L/I	MD23	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
230	AJ5	A6	L/I	MD22	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
231	AK5	A7	L/I	MD21	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
232	AL5	A8	L/I	-	Area 0*1	On	Open
233	AJ4	A9	L/I	-	Area 0*1	On	Open
234	AK4	A10	L/I	-	Area 0*1	On	Open
235	AL4	A11	L/I	-	Area 0*1	On	Open
236	AK3	A12	L/I	-	Area 0*1	On	Open
237	AL3	A13	L/I	-	Area 0*1	On	Open
238	AL2	A14	L/I	MD20	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
239	AH3	A15	L/I	MD19	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
240	AG1	A16	L/I	MD18	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
241	AG2	A17	L/I	MD17	-	Off	Pulled-up to VCCQ or pulled-down to VSS
242	AG3	A18	L/I	MD15	-	Off	Pulled-up to VCCQ or pulled-down to VSS
243	AG4	A19	L/I	MD14	-	Off	Pulled-up to VCCQ or pulled-down to VSS
244	AF1	A20	L/I	-	QSPI*2	On	Open
245	AF2	A21	L/I	-	QSPI*2	On	Open
246	AF3	A22	L/I	-	QSPI*2	On	Open
247	AF4	A23	L/I	-	QSPI*2	On	Open
248	AF5	A24	L/I	-	QSPI*2	On	Open

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
249	AE6	A25	L/I	-	QSPI*2	On	Open
250	AE1	CLKOUT	O	-	Area 0*1	Off	Open
251	AD1	CS0#	H/I	-	Area 0*1	On	Open
252	AJ2	[CS1#/A26]	[O]/I	-	Area 0*1	On	Open
253	AC1	EX_CS0#	I	-	-	On	Open
254	AC2	EX_CS1#	I	-	-	On	Open
255	AC3	EX_CS2#	I	-	-	On	Open
256	AC4	EX_CS3#	I	-	-	On	Open
257	AE3	EX_CS4#	I	-	-	On	Open
258	AE4	EX_CS5#	I	-	-	On	Open
259	AE5	BS#	H/I	MD13	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
260	AD3	RD#	H/I	MD16	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
261	AD2	RD/WR#	I	-	-	On	Open
262	AH1	WE0#	H/I	-	Area 0*1	On	Open
263	AH2	WE1#	H/I	-	Area 0*1	On	Open
264	AK1	EX_WAIT0	I	-	Area 0*1	On	Open
265	AC5	DREQ0	I	-	-	On	Open
266	AC6	DACK0	I	-	-	On	Open
267	AD5	DREQ1	I	-	-	On	Open
268	AD4	DACK1	I	-	-	On	Open
269	AD7	DREQ2	I	-	-	On	Open
270	AD6	DACK2	I	-	-	On	Open
271	AH11	ETH_CRS_DV	I	-	-	On	Open
272	AG11	ETH_RX_ER	I	-	-	On	Open
273	AF11	ETH_RXD0	I	-	-	On	Open
274	AE11	ETH_RXD1	I	-	-	On	Open
275	AK10	ETH_LINK	I	-	-	On	Open
276	AL10	ETH_REF_CLK	I	-	-	On	Open
277	AJ10	ETH_MDIO	I	-	-	On	Open
278	AH10	ETH_TXD1	I	MD12	-	Off	Pulled-up to VCCQ or pulled-down to VSS
279	AG10	ETH_TX_EN	I	MD11	-	Off	Pulled-up to VCCQ or pulled-down to VSS
280	AF10	ETH_MAGIC	I	MD10	-	Off	Pulled-up to VCCQ or pulled-down to VSS
281	AE10	ETH_TXD0	I	MD9	-	Off	Pulled-up to VCCQ or pulled-down to VSS
282	AE9	ETH_MDC	I	MD8	-	Off	Pulled-up to VCCQ or pulled-down to VSS
283	AE12	PWM0	I	MD7	-	Off	Pulled-up to VCCQ or pulled-down to VSS
284	AK11	PWM1	I	MD6	-	Off	Pulled-up to VCCQ or pulled-down to VSS
285	AJ11	PWM2	I	-	-	On	Open
286	AG12	NMI	I	-	-	-	Must be used
287	AG16	TRST#	I	-	-	On	Pulled-down to VSS
288	AE14	TCK	I	-	-	On	Open
289	AF14	TMS	I	-	-	On	Open
290	AH14	TDI	I	-	-	On	Open
291	AH12	TDO	Z	-	-	-	Open
292	AF13	ACK	I	-	-	On (pull-down)	Open
293	AG17	DU_LVDS0_CLK_P	Z	-	-	-	Open
294	AG18	DU_LVDS0_CLK_N	Z	-	-	-	Open
295	AJ18	DU_LVDS0_CH0_P	Z	-	-	-	Open
296	AJ19	DU_LVDS0_CH0_N	Z	-	-	-	Open
297	AG19	DU_LVDS0_CH1_P	Z	-	-	-	Open

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
298	AG20	DU_LVDS0_CH1_N	Z	-	-	-	Open
299	AL18	DU_LVDS0_CH2_P	Z	-	-	-	Open
300	AL17	DU_LVDS0_CH2_N	Z	-	-	-	Open
301	AJ17	DU_LVDS0_CH3_P	Z	-	-	-	Open
302	AJ16	DU_LVDS0_CH3_N	Z	-	-	-	Open
303	AJ13	DU_DOTCLKIN0	I	-	-	On	Open
304	AD18	VDDQ_LVDS	P	-	-	-	Must be used
305	AE18	VDDQ_LVDS	P	-	-	-	Must be used
306	AF18	VDDQ_LVDS	P	-	-	-	Must be used
307	AE20	DU_LVDS0_PLL1_VCC	P	-	-	-	Must be used
308	AD19	DU_LVDS0_PLL1_VSS	P	-	-	-	Must be used
309	AL19	DU_LVDS1_CLK_P	Z	-	-	-	Open
310	AL20	DU_LVDS1_CLK_N	Z	-	-	-	Open
311	AJ23	DU_LVDS1_CH0_P	Z	-	-	-	Open
312	AJ22	DU_LVDS1_CH0_N	Z	-	-	-	Open
313	AL21	DU_LVDS1_CH1_P	Z	-	-	-	Open
314	AL22	DU_LVDS1_CH1_N	Z	-	-	-	Open
315	AJ20	DU_LVDS1_CH2_P	Z	-	-	-	Open
316	AJ21	DU_LVDS1_CH2_N	Z	-	-	-	Open
317	AG22	DU_LVDS1_CH3_P	Z	-	-	-	Open
318	AG21	DU_LVDS1_CH3_N	Z	-	-	-	Open
319	AH13	DU_DOTCLKIN1	I	-	-	On	Open
320	AD22	VDDQ_LVDS	P	-	-	-	Must be used
321	AE22	VDDQ_LVDS	P	-	-	-	Must be used
322	AF22	VDDQ_LVDS	P	-	-	-	Must be used
323	AD20	DU_LVDS1_PLL1_VCC	P	-	-	-	Must be used
324	AD21	DU_LVDS1_PLL1_VSS	P	-	-	-	Must be used
325	AJ12	DU_DOTCLKIN2	I	-	-	On	Open
326	Y1	VI0_CLK	I	-	-	On	Open
327	Y6	VI0_DATA0/VI0_B0	I	-	-	On	Open
328	Y5	VI0_DATA1/VI0_B1	I	-	-	On	Open
329	Y4	VI0_DATA2/VI0_B2	I	-	-	On	Open
330	Y3	VI0_DATA3/VI0_B3	I	-	-	On	Open
331	W7	VI0_DATA4/VI0_B4	I	-	-	On	Open
332	W6	VI0_DATA5/VI0_B5	I	-	-	On	Open
333	AA6	VI0_DATA6/VI0_B6	I	-	-	On	Open
334	AA5	VI0_DATA7/VI0_B7	I	-	-	On	Open
335	AB1	VI1_CLK	I	-	-	On	Open
336	AA4	VI1_DATA0/VI1_B0	I	-	-	On	Open
337	AA3	VI1_DATA1/VI1_B1	I	-	-	On	Open
338	AB7	VI1_DATA2/VI1_B2	I	-	-	On	Open
339	AB6	VI1_DATA3/VI1_B3	I	-	-	On	Open
340	AB4	VI1_DATA4/VI1_B4	I	-	-	On	Open
341	AB3	VI1_DATA5/VI1_B5	I	-	-	On	Open
342	AA2	VI1_DATA6/VI1_B6	I	-	-	On	Open
343	AA1	VI1_DATA7/VI1_B7	I	-	-	On	Open
344	V1	SD0_CLK	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
345	V4	SD0_CMD	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
346	W2	SD0_DAT0	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
347	V7	SD0_DAT1	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
348	V6	SD0_DAT2	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
349	V5	SD0_DAT3	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
350	W3	SD0_CD	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
351	W4	SD0_WP	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
352	W8	VCCQ_SD0	P	-	-	-	Must be used
353	U1	SD1_CLK	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
354	T6	SD1_CMD	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
355	U6	SD1_DAT0	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
356	U4	SD1_DAT1	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
357	U3	SD1_DAT2	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
358	T7	SD1_DAT3	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
359	U7	SD1_CD	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
360	V3	SD1_WP	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
361	U8	VCCQ_SD1	P	-	-	-	Must be used
362	R1	SD2_CLK	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
363	T4	SD2_CMD	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
364	R5	SD2_DAT0	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
365	R4	SD2_DAT1	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
366	R3	SD2_DAT2	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
367	T5	SD2_DAT3	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
368	T2	SD2_CD	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
369	T3	SD2_WP	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
370	T8	VCCQ_SD2	P	-	-	-	Must be used
371	P1	SD3_CLK	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
372	P5	SD3_CMD	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
373	R7	SD3_DAT0	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
374	R6	SD3_DAT1	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
375	P4	SD3_DAT2	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
376	P3	SD3_DAT3	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
377	P6	SD3_CD	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
378	P7	SD3_WP	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
379	P8	VCCQ_SD3	P	-	-	-	Must be used
380	L31	NC	-	-	-	-	Open
381	K31	NC	-	-	-	-	Open
382	N31	NC	-	-	-	-	Open
383	M31	NC	-	-	-	-	Open
384	L29	NC	-	-	-	-	Open
385	L28	NC	-	-	-	-	Open
386	M29	NC	-	-	-	-	Open
387	M28	NC	-	-	-	-	Open
388	N28	VCCQ18_MLBP	P	-	-	-	Must be used
389	L25	VDD_MLBPPLL0	P	-	-	-	Must be used
390	M25	VSS_MLBPPLL0	P	-	-	-	Must be used
391	L26	VDD_MLBPPLL1	P	-	-	-	Must be used
392	M26	VSS_MLBPPLL1	P	-	-	-	Must be used
393	AB31	NC	-	-	-	-	Pulled-up to VCCQ or pulled-down to VSS
394	AC31	NC	-	-	-	-	Pulled-up to VCCQ or pulled-down to VSS
395	AA31	NC	-	-	-	-	Pulled-up to VCCQ or pulled-down to VSS
396	AB29	NC	-	-	-	-	Open
397	AA27	VDD_MLBPLL	P	-	-	-	Must be used

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
398	AA26	VSS_MLBPLL	P	-	-	-	Must be used
399	P31	SSI_SCK0129	I	-	-	On	Open
400	P30	SSI_WS0129	I	-	-	On	Open
401	P29	SSI_SDATA0	I	-	-	On	Open
402	P27	SSI_SDATA1	I	-	-	On	Open
403	R26	SSI_SDATA2	I	-	-	On	Open
404	R31	SSI_SCK34	I	-	-	On	Open
405	R28	SSI_WS34	I	-	-	On	Open
406	R27	SSI_SDATA3	I	-	-	On	Open
407	T31	SSI_SCK4	I	-	-	On	Open
408	T29	SSI_WS4	I	-	-	On	Open
409	R29	SSI_SDATA4	I	-	-	On	Open
410	U31	SSI_SCK5	I	-	-	On	Open
411	U30	SSI_WS5	I	-	-	On	Open
412	P26	SSI_SDATA5	I	-	-	On	Open
413	U29	SSI_SCK6	I	-	-	On	Open
414	U27	SSI_WS6	I	-	-	On	Open
415	T25	SSI_SDATA6	I	-	-	On	Open
416	V29	SSI_SCK78	I	-	-	On	Open
417	U28	SSI_WS78	I	-	-	On	Open
418	T26	SSI_SDATA7	I	-	-	On	Open
419	T28	SSI_SDATA8	I	-	-	On	Open
420	R25	SSI_SDATA9	I	-	-	On	Open
421	V31	AUDIO_CLKA	I	-	-	On	Open
422	W31	AUDIO_CLKB	I	-	-	On	Open
423	AA30	SCIFA0_SCK	I	-	-	On	Open
424	AA29	SCIFA0_RXD	I	-	-	On	Open
425	Y30	SCIFA0_TXD	I	MD5	-	Off	Pulled-up to VCCQ or pulled-down to VSS
426	W25	SCIFA0_CTS#	I	-	-	On	Open
427	Y29	SCIFA0_RTS#	I	MD4	-	Off	Pulled-up to VCCQ or pulled-down to VSS
428	Y28	SCIFA1_RXD	I	-	-	On	Open
429	Y27	SCIFA1_TXD	I	MD3	-	Off	Pulled-up to VCCQ or pulled-down to VSS
430	Y25	SCIFA1_CTS#	I	-	-	On	Open
431	Y26	SCIFA1_RTS#	I	MD2	-	Off	Pulled-up to VCCQ or pulled-down to VSS
432	AB28	SCIFA2_SCK	I	-	-	On	Open
433	AC27	SCIFA2_RXD	I	-	-	On	Open
434	AB27	SCIFA2_TXD	I	-	-	On	Open
435	V28	HSCK0	I	-	-	On	Open
436	V26	HRX0	I	-	-	On	Open
437	V27	HTX0	I	MD1	-	Off	Pulled-up to VCCQ or pulled-down to VSS
438	U26	HCTS0#	I	-	-	On	Open
439	U25	HRTS0#	I	-	-	On	Open
440	Y31	MSIOF0_SCK	I	-	-	On	Open
441	V25	MSIOF0_SYNC	I	-	-	On	Open
442	W28	MSIOF0_SS1	I	MD0	-	Off	Pulled-up to VCCQ or pulled-down to VSS
443	W29	MSIOF0_TXD	I	MDT1	-	Off	Pulled-up to VCCQ or pulled-down to VSS
444	W26	MSIOF0_SS2	I	MDT0	-	Off	Pulled-up to VCCQ or pulled-down to VSS
445	W27	MSIOF0_RXD	I	-	-	On	Open
446	AG15	IIC0_SCL	Z	-	-	-	Pulled-up to VCCQ18
447	AF15	IIC0_SDA	Z	-	-	-	Pulled-up to VCCQ18

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
448	AJ15	IIC3_SCL	Z	-	-	-	Pulled-up to VCCQ18
449	AH15	IIC3_SDA	Z	-	-	-	Pulled-up to VCCQ18
450	AL14	USB_EXTAL	I	-	-	-	Pulled-down to VSS
451	AL15	USB_XTAL	O	-	-	-	Open
452	AC24	AVSS	P	-	-	-	Must be used
453	AD25	AVSS	P	-	-	-	Must be used
454	AE26	AVSS	P	-	-	-	Must be used
455	AF31	USB0_DP	I	-	-	-	Open
456	AE31	USB0_DM	I	-	-	-	Open
457	AF29	USB0_RREF	P	-	-	-	Must be used
458	AE28	VD331	P	-	-	-	Must be used
459	AB25	VD181	P	-	-	-	Must be used
460	AB24	AVDD	P	-	-	-	Must be used
461	AC25	AVDD	P	-	-	-	Must be used
462	AD31	VSS	P	-	-	-	Must be used
463	AF27	AVSS	P	-	-	-	Must be used
464	AE30	VSS	P	-	-	-	Must be used
465	AC28	USB0_PWEN	L	-	-	Off	Open
466	AD28	USB0_OVC/VBUS	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
467	AH31	USB1_DP	I	-	-	-	Open
468	AG31	USB1_DM	I	-	-	-	Open
469	AG29	USB1_RREF	I	-	-	-	Must be used
470	AE29	VD331	I	-	-	-	Must be used
471	AC26	VD181	I	-	-	-	Must be used
472	AD26	AVDD	I	-	-	-	Must be used
473	AF30	VSS	I	-	-	-	Must be used
474	AF28	AVSS	I	-	-	-	Must be used
475	AG30	VSS	I	-	-	-	Must be used
476	AC29	USB1_PWEN	L	-	-	Off	Open
477	AD29	USB1_OVC	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
478	AK31	USB2_DP	I	-	-	-	Open
479	AJ31	USB2_DM	I	-	-	-	Open
480	AH29	USB2_RREF	I	-	-	-	Must be used
481	AD27	VD181	I	-	-	-	Must be used
482	AE27	AVDD	I	-	-	-	Must be used
483	AH30	VSS	I	-	-	-	Must be used
484	AG28	AVSS	I	-	-	-	Must be used
485	AJ30	VSS	I	-	-	-	Must be used
486	AD30	USB2_PWEN	L	-	-	Off	Open
487	AC30	USB2_OVC	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
488	AL23	RIDP1_SATA	I	-	-	-	Open
489	AL24	RIDN1_SATA	I	-	-	-	Open
490	AL25	TODP1_SATA	O	-	-	-	Open
491	AL26	TODN1_SATA	O	-	-	-	Open
492	AJ26	CICREFP1_SATA	I	-	-	-	Fixed to VSS_SATA1
493	AJ25	CICREFN1_SATA	I	-	-	-	Fixed to VSS_SATA1
494	AE23	VSS_SATA1	P	-	-	-	Must be used
495	AF23	VDDD_SATA1	P	-	-	-	Must be used
496	AD23	VSS_SATA1	P	-	-	-	Must be used
497	AF24	VDDA_SATA1	P	-	-	-	Must be used

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
498	AG24	VDDA_SATA1	P	-	-	-	Must be used
499	AG23	VDDD_SATA1	P	-	-	-	Must be used
500	AH24	VDDD_SATA1	P	-	-	-	Must be used
501	AE24	VSS_SATA1	P	-	-	-	Must be used
502	AJ24	VSS_SATA1	P	-	-	-	Must be used
503	AK23	VSS_SATA1	P	-	-	-	Must be used
504	AK24	VSS_SATA1	P	-	-	-	Must be used
505	AK25	VSS_SATA1	P	-	-	-	Must be used
506	AK26	VSS_SATA1	P	-	-	-	Must be used
507	AL27	RIDP0_SATA	I	-	-	-	Open
508	AL28	RIDN0_SATA	I	-	-	-	Open
509	AL29	TODP0_SATA	O	-	-	-	Open
510	AL30	TODN0_SATA	O	-	-	-	Open
511	AJ28	CICREFP0_SATA	I	-	-	-	Fixed to VSS_SATA0
512	AJ27	CICREFN0_SATA	I	-	-	-	Fixed to VSS_SATA0
513	AF25	VSS_SATA0	P	-	-	-	Must be used
514	AG25	VDDD_SATA0	P	-	-	-	Must be used
515	AD24	VSS_SATA0	P	-	-	-	Must be used
516	AG26	VDDA_SATA0	P	-	-	-	Must be used
517	AH27	VDDA_SATA0	P	-	-	-	Must be used
518	AH25	VDDD_SATA0	P	-	-	-	Must be used
519	AH26	VDDD_SATA0	P	-	-	-	Must be used
520	AE25	VSS_SATA0	P	-	-	-	Must be used
521	AF26	VSS_SATA0	P	-	-	-	Must be used
522	AG27	VSS_SATA0	P	-	-	-	Must be used
523	AH28	VSS_SATA0	P	-	-	-	Must be used
524	AJ29	VSS_SATA0	P	-	-	-	Must be used
525	AK27	VSS_SATA0	P	-	-	-	Must be used
526	AK28	VSS_SATA0	P	-	-	-	Must be used
527	AK29	VSS_SATA0	P	-	-	-	Must be used
528	AK30	VSS_SATA0	P	-	-	-	Must be used
529	AL31	VSS_SATA0	P	-	-	-	Must be used
530	Y7	VTHSENSE0	O	-	-	-	Open or fixed to VSS*3
531	AA7	VTHREF0	O	-	-	-	Open or fixed to VSS*3

Notes: 1. No.208 to 240, 250 to 252, 259, 260 and 262 to 264: Boot
Minimum number of pins that is necessary for area 0 boot operation must be used.

2. No.244 to 249: Boot
These pins must be used for QSPI boot.

3. No.530 and 531: Pin handling when not in use
Thermal sensor should be idle state (THSCR.THIDLE[1:0] = B'11) when fixed to VSS. For details, refer to section 60, Thermal Sensor (THS/TSC).

Note for DBSC3 DQS/DQS# states. ** (No.47/48, 61/62, 74/75, 88/89, 142/143, 156/157, 169/170, 183/184):

The drivers output states are both high-impedance (Z), and the internal circuit controls pin levels as low-level for the MnDQSx pins and high-level for the MnDQSx# pins respectively.

5. Pin Function Controller (PFC)

5.1 Overview

The pin function controller (PFC) is a module that consists of registers for selecting the function of the multiplexed pins and controlling the pull-up resistor on each LSI pin.

Notes: 1. Some functions are optional or internal.
2. Pin function name that has two or more functions is indicated by using "_" instead of "/".
3. Mirror pin function name that has two or more functions is indicated one mirror suffix as XXX_XXX_B instead of XXX_B_XXX_B.
For example, VI0_DATA0_B/VI0_B0_B is indicated as VI0_DATA0_VI0_B0_B in this section.

5.1.1 Features

- Register access through the APB bus interface
- Setting multiplexed pin functions for LSI pins
Function of the RZ/G1H pin selectable by setting the registers in the PFC module
(The function of the LSI pin can be selected by the GPIO/peripheral function select registers 0 to 5 (GPSR0 to GPSR5) and peripheral function select registers 0 to 16 (IPSR0 to IPSR16) in the PFC module. For details, see sections 5.3.2, GPIO/Peripheral Function Select Register 0 (GPSR0) through 5.3.24, Peripheral Function Select Register 16 (IPSR16).)
- Module selection
Enable and disable the functions of RZ/G1H LSI pins to which pin functions from multiple pin groups are assigned by setting the registers in the PFC module.
(Selection is handled by the module select register (MOD_SEL), module select register 2 (MOD_SEL2), and module select register 3 (MOD_SEL3). For details, see sections 5.3.25, Module Select Register (MOD_SEL), 5.3.26, Module Select Register 2 (MOD_SEL2), and 5.3.27, Module Select Register 3 (MOD_SEL3).)
- Pull-up control for each LSI pin.
On/off of the pull-up resistors on each LSI pin can be controlled by setting the registers in the PFC module.
(The pull-up resistors on each LSI pin can be turned on or off individually by setting the LSI pin pull-up control registers 0 to 6 (PUPR0 to PUPR6) in the PFC module. For details, see sections 5.3.28, LSI Pin Pull-Up Control Register 0 (PUPR0) through 5.3.34, LSI Pin Pull-Up Control Register 6 (PUPR6).)
Note: The ACK pin is available only for pull-down function.
- Control of IO functions, including SDHI, VIN, LBSC, SSI, and SCIFA.
SDIO functions, including the driving ability, POC of pins, can be controlled by setting registers of the PFC module. For details, see sections 5.3.36, SD Control Register 0 (IOCTRL0) through 5.3.40, POC Control Register (IOCTRL6).
The DDR3 GPIO function can also be selected by setting registers of the PFC. For details, see sections 5.3.41, DDR3 General Port IO Enable Register (DDR3GPEN) through 5.3.44, DDR3 General Port Input Data Register (DDR3GPID).

5.2 Register Configuration

All the registers in the PFC are mapped into the APB bus space. Table 5.1 shows the configuration of the registers provided in the PFC. For details on the registers of the PFC, see section 5.3, Register Description.

Table 5.1 Configuration of Registers in PFC

Name	Abbr.	R/W	Initial Value	Address	Access Size	Condition
LSI multiplexed pin setting mask register	PMMR	R/W	H'0000 0000	H'E606 0000	32	—
GPIO/peripheral function select register 0	GPSR0	R/W	H'FFFF FFFF (when md[3:1] = 000), H'0000 0000 (when md[3:1] ≠ 000)	H'E606 0004	32	The values of bits 31 to 16 in the power-on reset state are retained for 50 µs after release from the power-on reset state. When bits 31 to 16 are to be used for the output of addresses, external handling of the pins is required because these bits are hi-z in the power-on reset state.
GPIO/peripheral function select register 1	GPSR1	R/W	H'00EC 0FFF (when md[3:1] = 000), H'0000 0000 (when md[3:1] ≠ 000)	H'E606 0008	32	The values of bits 18 in the power-on reset state are retained for 50 µs after release from the power-on reset state.
GPIO/peripheral function select register 2	GPSR2	R/W	H'0000 0000	H'E606 000C	32	—
GPIO/peripheral function select register 3	GPSR3	R/W	H'0000 0000	H'E606 0010	32	—
GPIO/peripheral function select register 4	GPSR4	R/W	H'0000 0000	H'E606 0014	32	—
GPIO/peripheral function select register 5	GPSR5	R/W	H'13FC 0000	H'E606 0018	32	—
Peripheral function select register 0	IPSR0	R/W	H'0000 0000	H'E606 0020	32	—
Peripheral function select register 1	IPSR1	R/W	H'0000 0000	H'E606 0024	32	—
Peripheral function select register 2	IPSR2	R/W	H'0000 0000	H'E606 0028	32	—
Peripheral function select register 3	IPSR3	R/W	H'0000 0000	H'E606 002C	32	—
Peripheral function select register 4	IPSR4	R/W	H'0000 0000	H'E606 0030	32	—
Peripheral function select register 5	IPSR5	R/W	H'0000 0000	H'E606 0034	32	—

Name	Abbr.	R/W	Initial Value	Address	Access Size	Condition
Peripheral function select register 6	IPSR6	R/W	H'0000 0000	H'E606 0038	32	—
Peripheral function select register 7	IPSR7	R/W	H'0000 0000	H'E606 003C	32	—
Peripheral function select register 8	IPSR8	R/W	H'0000 0000	H'E606 0040	32	—
Peripheral function select register 9	IPSR9	R/W	H'0000 0000	H'E606 0044	32	—
Peripheral function select register 10	IPSR10	R/W	H'0000 0000	H'E606 0048	32	—
Peripheral function select register 11	IPSR11	R/W	H'0000 0000	H'E606 004C	32	—
Peripheral function select register 12	IPSR12	R/W	H'0000 0000	H'E606 0050	32	—
Peripheral function select register 13	IPSR13	R/W	H'0000 0000	H'E606 0054	32	—
Peripheral function select register 14	IPSR14	R/W	H'0000 0000	H'E606 0058	32	—
Peripheral function select register 15	IPSR15	R/W	H'0000 0000	H'E606 005C	32	—
Peripheral function select register 16	IPSR16	R/W	H'0000 0000	H'E606 0160	32	—
Module select register	MOD_SEL	R/W	H'0000 0000	H'E606 0090	32	—
Module select register 2	MOD_SEL2	R/W	H'0000 0000	H'E606 0094	32	—
Module select register 3	MOD_SEL3	R/W	H'0000 0000	H'E606 0098	32	—
LSI pin pull-up control register 0	PUPR0	R/W	H'FFF0 3F00	H'E606 0100	32	—
LSI pin pull-up control register 1	PUPR1	R/W	H'FFFF BF3C	H'E606 0104	32	—
LSI pin pull-up control register 2	PUPR2	R/W	H'80FF FFE1	H'E606 0108	32	—
LSI pin pull-up control register 3	PUPR3	R/W	H'0000 0000	H'E606 010C	32	—
LSI pin pull-up control register 4	PUPR4	R/W	H'FFFF FFFF	H'E606 0110	32	—
LSI pin pull-up control register 5	PUPR5	R/W	H'E047 BEAB	H'E606 0114	32	—
LSI pin pull-up control register 6	PUPR6	R/W	H'0000 0203	H'E606 0118	32	—
IIC3 (DVFS)/MMC IO cell control register	IOCTRL	R/W	H'0000 0000	H'E606 0070	32	—
SD control register 0	IOCTRL0	R/W	H'FFFF FFFF	H'E606 0060	32	—
SD control register 1	IOCTRL1	R/W	H'FFFF FFFF	H'E606 0064	32	—
VI1 Driving ability control register	IOCTRL4	R/W	H'0000 0200	H'E606 0084	32	—
TDSEL control register	IOCTRL5	R/W	H'0000 0000	H'E606 0088	32	—
POC control register	IOCTRL6	R/W	H'FFFF FFFF	H'E606 008C	32	—
DDR3 general port IO enable register	DDR3GPEN	R/W	H'0000 0000	H'E606 0240	32	—

Name	Abbr.	R/W	Initial Value	Address	Access Size	Condition
DDR3 general port output enable register	DDR3GPOE	R/W	H'0000 0000	H'E606 0244	32	—
DDR3 general port output data register	DDR3GPOD	R/W	H'0000 0000	H'E606 0248	32	—
DDR3 general port input data register	DDR3GPID	R	H'0000 0000	H'E606 024C	32	—

5.3 Register Description

[Legend]

Initial value:	Register value after a reset
:	Undefined value
R/W:	Readable/writable. The written value can be read.
R:	Read-only. The write value should always be 0.
R/WC0:	Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.
R/WC1:	Readable/writable. Writing 1 initializes the bit. Writing 0 is ignored.
W:	Write-only. Reading this bit is prohibited. When the bit is reserved, the write value should always be 0.
—/W:	Write-only. The read value is undefined.

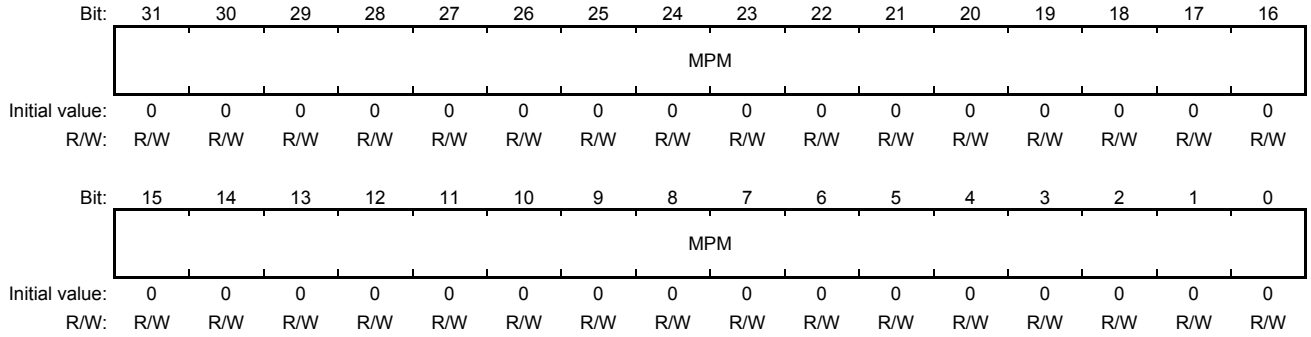
All the bits are active high unless otherwise specified, and deactivated on reset.

All access to registers is made in longword (4-byte) units.

The write value to a reserved bit should always be 0.

5.3.1 LSI Multiplexed Pin Setting Mask Register (PMMR)

Function: PMMR enables/disables writing to the multiplexed pin setting registers.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MPM[31:0]	H'0000 0000	R/W	Multiplexed Pin Setting Mask Writing a value to any register from among the GPIO/peripheral function select registers GPSR0 to GPSR5, peripheral function select registers IPSR0 to IPSR16, module select registers MOD_SEL, MOD_SEL2, and MOD_SEL3, IO cell control registers IOCTRL, IOCTRL0, IOCTRL1 and IOCTRL4 to IOCTRL6 is enabled by writing the inverse of the value to this register.

Note: This register must be set before setting each of the GPIO/peripheral function select registers GPSR0 to GPSR5, peripheral function select registers IPSR0 to IPSR16, module select registers MOD_SEL, MOD_SEL2, and MOD_SEL3, IO cell control registers IOCTRL, IOCTRL0, IOCTRL1 and IOCTRL4 to IOCTRL6.

5.3.2 GPIO/Peripheral Function Select Register 0 (GPSR0)

Function: GPSR0 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP0 [31]	GP0 [30]	GP0 [29]	GP0 [28]	GP0 [27]	GP0 [26]	GP0 [25]	GP0 [24]	GP0 [23]	GP0 [22]	GP0 [21]	GP0 [20]	GP0 [19]	GP0 [18]	GP0 [17]	GP0 [16]
Initial value:	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP0 [15]	GP0 [14]	GP0 [13]	GP0 [12]	GP0 [11]	GP0 [10]	GP0 [9]	GP0 [8]	GP0 [7]	GP0 [6]	GP0 [5]	GP0 [4]	GP0 [3]	GP0 [2]	GP0 [1]	GP0 [0]
Initial value:	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP0[31:0]	H'FFFF FFFF (when md[3:1] = 000), H'0000 0000 (when md[3:1] ≠ 000)	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP0[0]	GP-0-0	Peripheral function selected by IP0[2:0]
GP0[1]	GP-0-1	Peripheral function selected by IP0[5:3]
GP0[2]	GP-0-2	Peripheral function selected by IP0[8:6]
GP0[3]	GP-0-3	Peripheral function selected by IP0[11:9]
GP0[4]	GP-0-4	Peripheral function selected by IP0[15:12]
GP0[5]	GP-0-5	Peripheral function selected by IP0[19:16]
GP0[6]	GP-0-6	Peripheral function selected by IP0[22:20]
GP0[7]	GP-0-7	Peripheral function selected by IP0[26:23]
GP0[8]	GP-0-8	Peripheral function selected by IP0[30:27]
GP0[9]	GP-0-9	Peripheral function selected by IP1[3:0]
GP0[10]	GP-0-10	Peripheral function selected by IP1[7:4]
GP0[11]	GP-0-11	Peripheral function selected by IP1[11:8]
GP0[12]	GP-0-12	Peripheral function selected by IP1[14:12]
GP0[13]	GP-0-13	Peripheral function selected by IP1[17:15]
GP0[14]	GP-0-14	Peripheral function selected by IP1[21:18]
GP0[15]	GP-0-15	Peripheral function selected by IP1[25:22]
GP0[16]	GP-0-16	Peripheral function selected by IP1[27:26]
GP0[17]	GP-0-17	Peripheral function selected by IP1[29:28]
GP0[18]	GP-0-18	Peripheral function selected by IP2[2:0]
GP0[19]	GP-0-19	Peripheral function selected by IP2[5:3]
GP0[20]	GP-0-20	Peripheral function selected by IP2[8:6]
GP0[21]	GP-0-21	Peripheral function selected by IP2[11:9]
GP0[22]	GP-0-22	Peripheral function selected by IP2[14:12]
GP0[23]	GP-0-23	Peripheral function selected by IP2[17:15]

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP0[24]	GP-0-24	Peripheral function selected by IP2[21:18]
GP0[25]	GP-0-25	Peripheral function selected by IP2[25:22]
GP0[26]	GP-0-26	Peripheral function selected by IP2[28:26]
GP0[27]	GP-0-27	Peripheral function selected by IP3[3:0]
GP0[28]	GP-0-28	Peripheral function selected by IP3[7:4]
GP0[29]	GP-0-29	Peripheral function selected by IP3[11:8]
GP0[30]	GP-0-30	Peripheral function selected by IP3[14:12]
GP0[31]	GP-0-31	Peripheral function selected by IP3[17:15]

5.3.3 GPIO/Peripheral Function Select Register 1 (GPSR1)

Function: GPSR1 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP1 [31]	GP1 [30]	GP1 [29]	GP1 [28]	GP1 [27]	GP1 [26]	GP1 [25]	GP1 [24]	GP1 [23]	GP1 [22]	GP1 [21]	GP1 [20]	GP1 [19]	GP1 [18]	GP1 [17]	GP1 [16]
Initial value:	0	0	0	0	0	0	0	0	1/0	1/0	1/0	0	1/0	1/0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP1 [15]	GP1 [14]	GP1 [13]	GP1 [12]	GP1 [11]	GP1 [10]	GP1 [9]	GP1 [8]	GP1 [7]	GP1 [6]	GP1 [5]	GP1 [4]	GP1 [3]	GP1 [2]	GP1 [1]	GP1 [0]
Initial value:	0	0	0	0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP1[31:0]	H'00EC 0FFF (when md[3:1] = 000), H'0000 0000 (when md[3:1] ≠ 000)	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP1[0]	GP-1-0	Peripheral function selected by IP3[19:18]
GP1[1]	GP-1-1	Peripheral function selected by IP3[22:20]
GP1[2]	GP-1-2	Peripheral function selected by IP3[25:23]
GP1[3]	GP-1-3	Peripheral function selected by IP3[28:26]
GP1[4]	GP-1-4	Peripheral function selected by IP3[31:29]
GP1[5]	GP-1-5	Peripheral function selected by IP4[2:0]
GP1[6]	GP-1-6	Peripheral function selected by IP4[5:3]
GP1[7]	GP-1-7	Peripheral function selected by IP4[8:6]
GP1[8]	GP-1-8	Peripheral function selected by IP4[11:9]
GP1[9]	GP-1-9	Peripheral function selected by IP4[14:12]
GP1[10]	GP-1-10	Peripheral function selected by IP4[17:15]
GP1[11]	GP-1-11	Peripheral function selected by IP4[20:18]
GP1[12]	GP-1-12	Peripheral function selected by IP4[23:21]
GP1[13]	GP-1-13	Peripheral function selected by IP4[26:24]
GP1[14]	GP-1-14	Peripheral function selected by IP4[29:27]
GP1[15]	GP-1-15	Peripheral function selected by IP5[2:0]
GP1[16]	GP-1-16	Peripheral function selected by IP5[5:3]
GP1[17]	GP-1-17	Peripheral function selected by IP5[9:6]
GP1[18]	GP-1-18	Peripheral function selected by IP5[12:10]
GP1[19]	GP-1-19	Peripheral function selected by IP5[14:13]
GP1[20]	GP-1-20	Peripheral function selected by IP5[17:15]
GP1[21]	GP-1-21	Peripheral function selected by IP5[20:18]
GP1[22]	GP-1-22	Peripheral function selected by IP5[23:21]
GP1[23]	GP-1-23	Peripheral function selected by IP5[26:24]

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP1[24]	GP-1-24	Peripheral function selected by IP5[29:27]
GP1[25]	GP-1-25	Peripheral function selected by IP6[2:0]
GP1[26]	GP-1-26	Peripheral function selected by IP6[5:3]
GP1[27]	GP-1-27	Peripheral function selected by IP6[8:6]
GP1[28]	GP-1-28	Peripheral function selected by IP6[10:9]
GP1[29]	GP-1-29	Peripheral function selected by IP6[13:11]
GP1[30]	—	—
GP1[31]	—	—

5.3.4 GPIO/Peripheral Function Select Register 2 (GPSR2)

Function: GPSR2 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP2 [31]	GP2 [30]	GP2 [29]	GP2 [28]	GP2 [27]	GP2 [26]	GP2 [25]	GP2 [24]	GP2 [23]	GP2 [22]	GP2 [21]	GP2 [20]	GP2 [19]	GP2 [18]	GP2 [17]	GP2 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP2 [15]	GP2 [14]	GP2 [13]	GP2 [12]	GP2 [11]	GP2 [10]	GP2 [9]	GP2 [8]	GP2 [7]	GP2 [6]	GP2 [5]	GP2 [4]	GP2 [3]	GP2 [2]	GP2 [1]	GP2 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP2[31:0]	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP2[0]	GP-2-0	Peripheral function selected by IP7[28:27]
GP2[1]	GP-2-1	Peripheral function selected by IP7[30:29]
GP2[2]	GP-2-2	Peripheral function selected by IP8[1:0]
GP2[3]	GP-2-3	Peripheral function selected by IP8[3:2]
GP2[4]	GP-2-4	Peripheral function selected by IP8[5:4]
GP2[5]	GP-2-5	Peripheral function selected by IP8[7:6]
GP2[6]	GP-2-6	Peripheral function selected by IP8[9:8]
GP2[7]	GP-2-7	Peripheral function selected by IP8[11:10]
GP2[8]	GP-2-8	Peripheral function selected by IP8[13:12]
GP2[9]	GP-2-9	Peripheral function selected by IP8[15:14]
GP2[10]	GP-2-10	Peripheral function selected by IP8[17:16]
GP2[11]	GP-2-11	Peripheral function selected by IP8[19:18]
GP2[12]	GP-2-12	Peripheral function selected by IP8[21:20]
GP2[13]	GP-2-13	Peripheral function selected by IP8[23:22]
GP2[14]	GP-2-14	Peripheral function selected by IP8[25:24]
GP2[15]	GP-2-15	Peripheral function selected by IP8[26]
GP2[16]	GP-2-16	Peripheral function selected by IP8[27]
GP2[17]	GP-2-17	VI1_DATA7_VI1_B7
GP2[18]	GP-2-18	Peripheral function selected by IP6[16:14]
GP2[19]	GP-2-19	Peripheral function selected by IP6[19:17]
GP2[20]	GP-2-20	Peripheral function selected by IP6[22:20]
GP2[21]	GP-2-21	Peripheral function selected by IP6[25:23]
GP2[22]	GP-2-22	Peripheral function selected by IP6[28:26]
GP2[23]	GP-2-23	Peripheral function selected by IP6[31:29]
GP2[24]	GP-2-24	Peripheral function selected by IP7[2:0]

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP2[25]	GP-2-25	Peripheral function selected by IP7[5:3]
GP2[26]	GP-2-26	Peripheral function selected by IP7[7:6]
GP2[27]	GP-2-27	Peripheral function selected by IP7[9:8]
GP2[28]	GP-2-28	Peripheral function selected by IP7[12:10]
GP2[29]	GP-2-29	Peripheral function selected by IP7[15:13]
GP2[30]	—	—
GP2[31]	—	—

5.3.5 GPIO/Peripheral Function Select Register 3 (GPSR3)

Function: GPSR3 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP3 [31]	GP3 [30]	GP3 [29]	GP3 [28]	GP3 [27]	GP3 [26]	GP3 [25]	GP3 [24]	GP3 [23]	GP3 [22]	GP3 [21]	GP3 [20]	GP3 [19]	GP3 [18]	GP3 [17]	GP3 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP3 [15]	GP3 [14]	GP3 [13]	GP3 [12]	GP3 [11]	GP3 [10]	GP3 [9]	GP3 [8]	GP3 [7]	GP3 [6]	GP3 [5]	GP3 [4]	GP3 [3]	GP3 [2]	GP3 [1]	GP3 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP3[31:0]	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP3[0]	GP-3-0	Peripheral function selected by IP8[28]
GP3[1]	GP-3-1	Peripheral function selected by IP8[30:29]
GP3[2]	GP-3-2	Peripheral function selected by IP9[1:0]
GP3[3]	GP-3-3	Peripheral function selected by IP9[3:2]
GP3[4]	GP-3-4	Peripheral function selected by IP9[5:4]
GP3[5]	GP-3-5	Peripheral function selected by IP9[7:6]
GP3[6]	GP-3-6	Peripheral function selected by IP9[11:8]
GP3[7]	GP-3-7	Peripheral function selected by IP9[15:12]
GP3[8]	GP-3-8	Peripheral function selected by IP9[17:16]
GP3[9]	GP-3-9	Peripheral function selected by IP9[19:18]
GP3[10]	GP-3-10	Peripheral function selected by IP9[21:20]
GP3[11]	GP-3-11	Peripheral function selected by IP9[23:22]
GP3[12]	GP-3-12	Peripheral function selected by IP9[25:24]
GP3[13]	GP-3-13	Peripheral function selected by IP9[27:26]
GP3[14]	GP-3-14	Peripheral function selected by IP9[31:28]
GP3[15]	GP-3-15	Peripheral function selected by IP10[3:0]
GP3[16]	GP-3-16	Peripheral function selected by IP10[6:4]
GP3[17]	GP-3-17	Peripheral function selected by IP10[10:7]
GP3[18]	GP-3-18	Peripheral function selected by IP10[14:11]
GP3[19]	GP-3-19	Peripheral function selected by IP10[18:15]
GP3[20]	GP-3-20	Peripheral function selected by IP10[22:19]
GP3[21]	GP-3-21	Peripheral function selected by IP10[25:23]
GP3[22]	GP-3-22	Peripheral function selected by IP10[29:26]
GP3[23]	GP-3-23	Peripheral function selected by IP11[3:0]
GP3[24]	GP-3-24	Peripheral function selected by IP11[4]

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP3[25]	GP-3-25	Peripheral function selected by IP11[6:5]
GP3[26]	GP-3-26	Peripheral function selected by IP11[8:7]
GP3[27]	GP-3-27	Peripheral function selected by IP11[10:9]
GP3[28]	GP-3-28	Peripheral function selected by IP11[12:11]
GP3[29]	GP-3-29	Peripheral function selected by IP11[14:13]
GP3[30]	GP-3-30	Peripheral function selected by IP11[17:15]
GP3[31]	GP-3-31	Peripheral function selected by IP11[21:18]

5.3.6 GPIO/Peripheral Function Select Register 4 (GPSR4)

Function: GPSR4 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP4 [31]	GP4 [30]	GP4 [29]	GP4 [28]	GP4 [27]	GP4 [26]	GP4 [25]	GP4 [24]	GP4 [23]	GP4 [22]	GP4 [21]	GP4 [20]	GP4 [19]	GP4 [18]	GP4 [17]	GP4 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP4 [15]	GP4 [14]	GP4 [13]	GP4 [12]	GP4 [11]	GP4 [10]	GP4 [9]	GP4 [8]	GP4 [7]	GP4 [6]	GP4 [5]	GP4 [4]	GP4 [3]	GP4 [2]	GP4 [1]	GP4 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP4[31:0]	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP4[0]	GP-4-0	Peripheral function selected by IP11[23:22]
GP4[1]	GP-4-1	Peripheral function selected by IP11[26:24]
GP4[2]	GP-4-2	Peripheral function selected by IP11[29:27]
GP4[3]	GP-4-3	Peripheral function selected by IP11[31:30]
GP4[4]	GP-4-4	Peripheral function selected by IP12[1:0]
GP4[5]	GP-4-5	Peripheral function selected by IP12[3:2]
GP4[6]	GP-4-6	Peripheral function selected by IP12[5:4]
GP4[7]	GP-4-7	Peripheral function selected by IP12[7:6]
GP4[8]	GP-4-8	Peripheral function selected by IP12[10:8]
GP4[9]	GP-4-9	Peripheral function selected by IP12[13:11]
GP4[10]	GP-4-10	Peripheral function selected by IP12[16:14]
GP4[11]	GP-4-11	Peripheral function selected by IP12[19:17]
GP4[12]	GP-4-12	Peripheral function selected by IP12[22:20]
GP4[13]	GP-4-13	Peripheral function selected by IP12[24:23]
GP4[14]	GP-4-14	Peripheral function selected by IP12[27:25]
GP4[15]	GP-4-15	Peripheral function selected by IP12[30:28]
GP4[16]	GP-4-16	Peripheral function selected by IP13[2:0]
GP4[17]	GP-4-17	Peripheral function selected by IP13[6:3]
GP4[18]	GP-4-18	Peripheral function selected by IP13[9:7]
GP4[19]	GP-4-19	Peripheral function selected by IP13[12:10]
GP4[20]	GP-4-20	Peripheral function selected by IP13[15:13]
GP4[21]	GP-4-21	Peripheral function selected by IP13[18:16]
GP4[22]	GP-4-22	Peripheral function selected by IP13[22:19]
GP4[23]	GP-4-23	Peripheral function selected by IP13[25:23]
GP4[24]	GP-4-24	Peripheral function selected by IP13[28:26]

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP4[25]	GP-4-25	Peripheral function selected by IP13[30:29]
GP4[26]	GP-4-26	Peripheral function selected by IP14[2:0]
GP4[27]	GP-4-27	Peripheral function selected by IP14[5:3]
GP4[28]	GP-4-28	Peripheral function selected by IP14[8:6]
GP4[29]	GP-4-29	Peripheral function selected by IP14[11:9]
GP4[30]	GP-4-30	Peripheral function selected by IP14[15:12]
GP4[31]	GP-4-31	Peripheral function selected by IP14[18:16]

5.3.7 GPIO/Peripheral Function Select Register 5 (GPSR5)

Function: GPSR5 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP5 [31]	GP5 [30]	GP5 [29]	GP5 [28]	GP5 [27]	GP5 [26]	GP5 [25]	GP5 [24]	GP5 [23]	GP5 [22]	GP5 [21]	GP5 [20]	GP5 [19]	GP5 [18]	GP5 [17]	GP5 [16]
Initial value:	0	0	0	1	0	0	1	1	1	1	1	1	1	1	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP5 [15]	GP5 [14]	GP5 [13]	GP5 [12]	GP5 [11]	GP5 [10]	GP5 [9]	GP5 [8]	GP5 [7]	GP5 [6]	GP5 [5]	GP5 [4]	GP5 [3]	GP5 [2]	GP5 [1]	GP5 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP5[31:0]	H'13FC 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP5[0]	GP-5-0	Peripheral function selected by IP14[21:19]
GP5[1]	GP-5-1	Peripheral function selected by IP14[24:22]
GP5[2]	GP-5-2	Peripheral function selected by IP14[27:25]
GP5[3]	GP-5-3	Peripheral function selected by IP14[30:28]
GP5[4]	GP-5-4	Peripheral function selected by IP15[2:0]
GP5[5]	GP-5-5	Peripheral function selected by IP15[5:3]
GP5[6]	GP-5-6	Peripheral function selected by IP15[8:6]
GP5[7]	GP-5-7	Peripheral function selected by IP15[11:9]
GP5[8]	GP-5-8	Peripheral function selected by IP15[13:12]
GP5[9]	GP-5-9	Peripheral function selected by IP15[15:14]
GP5[10]	GP-5-10	Peripheral function selected by IP15[17:16]
GP5[11]	GP-5-11	Peripheral function selected by IP15[19:18]
GP5[12]	GP-5-12	Peripheral function selected by IP15[22:20]
GP5[13]	GP-5-13	Peripheral function selected by IP15[25:23]
GP5[14]	GP-5-14	Peripheral function selected by IP15[27:26]
GP5[15]	GP-5-15	Peripheral function selected by IP15[29:28]
GP5[16]	GP-5-16	Peripheral function selected by IP16[2:0]
GP5[17]	GP-5-17	Peripheral function selected by IP16[5:3]
GP5[18]	GP-5-18	USB0_PWEN
GP5[19]	GP-5-19	USB0_OVC_VBUS
GP5[20]	GP-5-20	Peripheral function selected by IP16[6]
GP5[21]	GP-5-21	Peripheral function selected by IP16[7]
GP5[22]	GP-5-22	USB2_PWEN
GP5[23]	GP-5-23	USB2_OVC
GP5[24]	GP-5-24	AVS1

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP5[25]	GP-5-25	AVS2
GP5[26]	GP-5-26	DU_DOTCLKIN0
GP5[27]	GP-5-27	Peripheral function selected by IP7[26:25]
GP5[28]	GP-5-28	DU_DOTCLKIN2
GP5[29]	GP-5-29	Peripheral function selected by IP7[18:16]
GP5[30]	GP-5-30	Peripheral function selected by IP7[21:19]
GP5[31]	GP-5-31	Peripheral function selected by IP7[24:22]

5.3.8 Peripheral Function Select Register 0 (IPSR0)

Function: IPSR0 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	IP0 [30]	IP0 [29]	IP0 [28]	IP0 [27]	IP0 [26]	IP0 [25]	IP0 [24]	IP0 [23]	IP0 [22]	IP0 [21]	IP0 [20]	IP0 [19]	IP0 [18]	IP0 [17]	IP0 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP0 [15]	IP0 [14]	IP0 [13]	IP0 [12]	IP0 [11]	IP0 [10]	IP0 [9]	IP0 [8]	IP0 [7]	IP0 [6]	IP0 [5]	IP0 [4]	IP0 [3]	IP0 [2]	IP0 [1]	IP0 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Function 9 (Set Value = H'8)	Function 10 (Set Value = H'9)	Others (Set Value = H'A to H'F)
IP0[2:0]	D0	MSIOF3_SCK_B	VI3_DATA0	VI0_G4	VI0_G4_B	—	—	—	—	—	—
IP0[5:3]	D1	MSIOF3_SYNC_B	VI3_DATA1	VI0_G5	VI0_G5_B	—	—	—	—	—	—
IP0[8:6]	D2	MSIOF3_RXD_B	VI3_DATA2	VI0_G6	VI0_G6_B	—	—	—	—	—	—
IP0 [11:9]	D3	MSIOF3_TXD_B	VI3_DATA3	VI0_G7	VI0_G7_B	—	—	—	—	—	—
IP0 [15:12]	D4	SCIFB1_RXD_F	SCIFB0_RXD_C	VI3_DATA4	VI0_R0	VI0_R0_B	RX0_B	—	—	—	—
IP0 [19:16]	D5	SCIFB1_TXD_F	SCIFB0_TXD_C	VI3_DATA5	VI0_R1	VI0_R1_B	TX0_B	—	—	—	—
IP0 [22:20]	D6	IIC2_SCL_C	VI3_DATA6	VI0_R2	VI0_R2_B	I2C2_SCL_C	—	—	—	—	—
IP0 [26:23]	D7	—	IIC2_SDA_C	VI3_DATA7	VI0_R3	VI0_R3_B	I2C2_SDA_C	TCLK1	—	—	—
IP0 [30:27]	D8	SCIFA1_SCK_C	AVB_TXD0	—	VI0_G0	VI0_G0_B	VI2_DATA0_VI2_B0	—	—	—	—

Legend: — Setting prohibited

5.3.9 Peripheral Function Select Register 1 (IPSR1)

Function: IPSR1 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	IP1 [29]	IP1 [28]	IP1 [27]	IP1 [26]	IP1 [25]	IP1 [24]	IP1 [23]	IP1 [22]	IP1 [21]	IP1 [20]	IP1 [19]	IP1 [18]	IP1 [17]	IP1 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP1 [15]	IP1 [14]	IP1 [13]	IP1 [12]	IP1 [11]	IP1 [10]	IP1 [9]	IP1 [8]	IP1 [7]	IP1 [6]	IP1 [5]	IP1 [4]	IP1 [3]	IP1 [2]	IP1 [1]	IP1 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Function 9 (Set Value = H'8)	Others (Set Value = H'9 to H'F)
IP1[3:0]	D9	SCIFA1_RXD_C	AVB_TXD1	—	VI0_G1	VI0_G1_B	VI2_DATA1_VI2_B1	—	—	—
IP1[7:4]	D10	SCIFA1_TXD_C	AVB_TXD2	—	VI0_G2	VI0_G2_B	VI2_DATA2_VI2_B2	—	—	—
IP1[11:8]	D11	SCIFA1_CTS#_C	AVB_TXD3	—	VI0_G3	VI0_G3_B	VI2_DATA3_VI2_B3	—	—	—
IP1[14:12]	D12	SCIFA1_RTS#_C	AVB_TXD4	VI0_HSYNC#	VI0_HSYNC#_B	VI2_DATA4_VI2_B4	—	—	—	—
IP1[17:15]	D13	AVB_TXD5	VI0_VSYNC#	VI0_VSYNC#_B	VI2_DATA5_VI2_B5	—	—	—	—	—
IP1[21:18]	D14	SCIFB1_RXD_C	AVB_TXD6	RX1_B	VI0_CLKENB	VI0_CLKENB_B	VI2_DATA6_VI2_B6	—	—	—
IP1[25:22]	D15	SCIFB1_TXD_C	AVB_TXD7	TX1_B	VI0_FIELD	VI0_FIELD_B	VI2_DATA7_VI2_B7	—	—	—
IP1[27:26]	A0	PWM3	—	—	—	—	—	—	—	—
IP1[29:28]	A1	PWM4	—	—	—	—	—	—	—	—

Legend: — Setting prohibited

5.3.10 Peripheral Function Select Register 2 (IPSR2)

Function: IPSR2 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	IP2 [28]	IP2 [27]	IP2 [26]	IP2 [25]	IP2 [24]	IP2 [23]	IP2 [22]	IP2 [21]	IP2 [20]	IP2 [19]	IP2 [18]	IP2 [17]	IP2 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP2 [15]	IP2 [14]	IP2 [13]	IP2 [12]	IP2 [11]	IP2 [10]	IP2 [9]	IP2 [8]	IP2 [7]	IP2 [6]	IP2 [5]	IP2 [4]	IP2 [3]	IP2 [2]	IP2 [1]	IP2 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Function 9 (Set Value = H'8)	Function 10 (Set Value = H'9)	Others (Set Value = H'A to H'F)
IP2[2:0]	A2	PWM5	MSIOF1_SS1_B	—	—	—	—	—	—	—	—
IP2[5:3]	A3	PWM6	MSIOF1_SS2_B	—	—	—	—	—	—	—	—
IP2[8:6]	A4	MSIOF1_TXD_B	TPU0TO0	—	—	—	—	—	—	—	—
IP2[11:9]	A5	SCIFA1_TXD_B	TPU0TO1	—	—	—	—	—	—	—	—
IP2[14:12]	A6	SCIFA1_RTS#_B	TPU0TO2	—	—	—	—	—	—	—	—
IP2[17:15]	A7	SCIFA1_SCK_B	AUDIO_CLKOUT_B	TPU0TO3	—	—	—	—	—	—	—
IP2[21:18]	A8	SCIFA1_RXD_B	SSI_SCK5_B	VI0_R4	VI0_R4_B	SCIFB2_RXD_C	RX2_B	VI2_DATA0_VI2_B0_B	—	—	—
IP2[25:22]	A9	SCIFA1_CTS#_B	SSI_WS5_B	VI0_R5	VI0_R5_B	SCIFB2_TXD_C	TX2_B	VI2_DATA1_VI2_B1_B	—	—	—
IP2[28:26]	A10	SSI_SDATA5_B	MSIOF2_SYNC	VI0_R6	VI0_R6_B	VI2_DATA2_VI2_B2_B	—	—	—	—	—

Legend: — Setting prohibited

5.3.11 Peripheral Function Select Register 3 (IPSR3)

Function: IPSR3 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP3 [31]	IP3 [30]	IP3 [29]	IP3 [28]	IP3 [27]	IP3 [26]	IP3 [25]	IP3 [24]	IP3 [23]	IP3 [22]	IP3 [21]	IP3 [20]	IP3 [19]	IP3 [18]	IP3 [17]	IP3 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP3 [15]	IP3 [14]	IP3 [13]	IP3 [12]	IP3 [11]	IP3 [10]	IP3 [9]	IP3 [8]	IP3 [7]	IP3 [6]	IP3 [5]	IP3 [4]	IP3 [3]	IP3 [2]	IP3 [1]	IP3 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Function 9 (Set Value = H'8)	Function 10 (Set Value = H'9)	Others (Set Value = H'A to H'F)
IP3[3:0]	A11	SCIFB2_CTS#_B	MSIOF2_SCK	VI1_R0	VI1_R0_B	VI2_G0	VI2_DATA3_VI2_B3_B	—	—	—	—
IP3[7:4]	A12	SCIFB2_RXD_B	MSIOF2_TXD	VI1_R1	VI1_R1_B	VI2_G1	VI2_DATA4_VI2_B4_B	—	—	—	—
IP3 [11:8]	A13	SCIFB2_RTS#_B	EX_WAIT2	MSIOF2_RXD	VI1_R2	VI1_R2_B	VI2_G2	VI2_DATA5_VI2_B5_B	—	—	—
IP3 [14:12]	A14	SCIFB2_TXD_B	ATACS11#	MSIOF2_SS1	—	—	—	—	—	—	—
IP3 [17:15]	A15	SCIFB2_SCK_B	ATARD1#	MSIOF2_SS2	—	—	—	—	—	—	—
IP3 [19:18]	A16	ATAWR1#	—	—	—	—	—	—	—	—	—
IP3 [22:20]	A17	—	ATADIR1#	—	—	—	—	—	—	—	—
IP3 [25:23]	A18	—	ATAG1#	—	—	—	—	—	—	—	—
IP3 [28:26]	A19	—	ATACS01#	EX_WAIT0_B	—	—	—	—	—	—	—
IP3 [31:29]	A20	SPCLK	VI1_R3	VI1_R3_B	VI2_G4	—	—	—	—	—	—

Legend: — Setting prohibited

5.3.12 Peripheral Function Select Register 4 (IPSR4)

Function: IPSR4 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	IP4 [29]	IP4 [28]	IP4 [27]	IP4 [26]	IP4 [25]	IP4 [24]	IP4 [23]	IP4 [22]	IP4 [21]	IP4 [20]	IP4 [19]	IP4 [18]	IP4 [17]	IP4 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP4 [15]	IP4 [14]	IP4 [13]	IP4 [12]	IP4 [11]	IP4 [10]	IP4 [9]	IP4 [8]	IP4 [7]	IP4 [6]	IP4 [5]	IP4 [4]	IP4 [3]	IP4 [2]	IP4 [1]	IP4 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Others (Set Value = H'8 to H'F)
IP4[2:0]	A21	MOSI_IO0	VI1_R4	VI1_R4_B	VI2_G5	—	—	—	—
IP4[5:3]	A22	MISO_IO1	VI1_R5	VI1_R5_B	VI2_G6	—	—	—	—
IP4[8:6]	A23	IO2	VI1_G7	VI1_G7_B	VI2_G7	—	—	—	—
IP4[11:9]	A24	IO3	VI1_R7	VI1_R7_B	VI2_CLKENB	VI2_CLKENB_B	—	—	—
IP4[14:12]	A25	SSL	VI1_G6	VI1_G6_B	VI2_FIELD	VI2_FIELD_B	—	—	—
IP4[17:15]	CS0#	VI1_R6	VI1_R6_B	VI2_G3	MSIOF0_SS2_B	—	—	—	—
IP4[20:18]	CS1#_A26	—	VI0_R7	VI0_R7_B	VI2_CLK	VI2_CLK_B	—	—	—
IP4[23:21]	EX_CS0#	HRX1_B	VI1_G5	VI1_G5_B	VI2_R0	HTX0_B	MSIOF0_SS1_B	—	—
IP4[26:24]	EX_CS1#	—	HCTS1#_B	VI1_FIELD	VI1_FIELD_B	VI2_R1	—	—	—
IP4[29:27]	EX_CS2#	—	HRTS1#_B	VI3_CLKENB	VI1_G0	VI1_G0_B	VI2_R2	—	—

Legend: — Setting prohibited

5.3.13 Peripheral Function Select Register 5 (IPSR5)

Function: IPSR5 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	IP5 [29]	IP5 [28]	IP5 [27]	IP5 [26]	IP5 [25]	IP5 [24]	IP5 [23]	IP5 [22]	IP5 [21]	IP5 [20]	IP5 [19]	IP5 [18]	IP5 [17]	IP5 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP5 [15]	IP5 [14]	IP5 [13]	IP5 [12]	IP5 [11]	IP5 [10]	IP5 [9]	IP5 [8]	IP5 [7]	IP5 [6]	IP5 [5]	IP5 [4]	IP5 [3]	IP5 [2]	IP5 [1]	IP5 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Function 9 (Set Value = H'8)	Function 10 (Set Value = H'9)	Others (Set Value = H'A to H'F)
IP5[2:0]	EX_CS3#	—	VI3_FIELD	VI1_G1	VI1_G1_B	VI2_R3	—	—	—	—	—
IP5[5:3]	EX_CS4#	MSIOF1_SCK_B	VI3_HSYNC#	VI2_HSYNC#	IIC1_SCL	VI2_HSYNC#_B	—	I2C1_SCL	—	—	—
IP5[9:6]	EX_CS5#	CAN0_RX	MSIOF1_RXD_B	VI3_VSYNC#	VI1_G2	VI1_G2_B	VI2_R4	IIC1_SDA	—	I2C1_SDA	—
IP5 [12:10]	BS#	—	HTX1_B	CAN1_TX	DRACK0	—	—	—	—	—	—
IP5 [14:13]	RD#	CAN0_TX	SCIFA0_SCK_B	—	—	—	—	—	—	—	—
IP5 [17:15]	RD_WR#	VI1_G3	VI1_G3_B	VI2_R5	SCIFA0_RXD_B	—	—	—	—	—	—
IP5 [20:18]	WE0#	—	CAN_CLK	VI2_VSYNC#	SCIFA0_TXD_B	VI2_VSYNC#_B	—	—	—	—	—
IP5 [23:21]	WE1#	—	CAN1_RX	VI1_G4	VI1_G4_B	VI2_R6	SCIFA0_CTS#_B	—	—	—	—
IP5 [26:24]	EX_WAIT0	IRQ3	—	VI3_CLK	SCIFA0_RTS#_B	HRX0_B	MSIOF0_SCK_B	—	—	—	—
IP5 [29:27]	DREQ0	VI1_HSYNC#	VI1_HSYNC#_B	VI2_R7	SSI_SCK78_C	SSI_WS78_B	—	—	—	—	—

Legend: — Setting prohibited

5.3.14 Peripheral Function Select Register 6 (IPSR6)

Function: IPSR6 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP6 [31]	IP6 [30]	IP6 [29]	IP6 [28]	IP6 [27]	IP6 [26]	IP6 [25]	IP6 [24]	IP6 [23]	IP6 [22]	IP6 [21]	IP6 [20]	IP6 [19]	IP6 [18]	IP6 [17]	IP6 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP6 [15]	IP6 [14]	IP6 [13]	IP6 [12]	IP6 [11]	IP6 [10]	IP6 [9]	IP6 [8]	IP6 [7]	IP6 [6]	IP6 [5]	IP6 [4]	IP6 [3]	IP6 [2]	IP6 [1]	IP6 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Others (Set Value = H'8 to H'F)
IP6[2:0]	DACK0	IRQ0	—	SSI_SCK6_B	VI1_VSYNC#	VI1_VSYNC#_B	SSI_WS78_C	—	—
IP6[5:3]	DREQ1	VI1_CLKENB	VI1_CLKENB_B	SSI_SDATA7_C	SSI_SCK78_B	—	—	—	—
IP6[8:6]	DACK1	IRQ1	—	SSI_WS6_B	SSI_SDATA8_C	—	—	—	—
IP6[10:9]	DREQ2	HSCK1_B	HCTS0#_B	MSIOF0_TXD_B	—	—	—	—	—
IP6[13:11]	DACK2	IRQ2	—	SSI_SDATA6_B	HRTS0#_B	MSIOF0_RXD_B	—	—	—
IP6[16:14]	ETH_CRS_DV	—	—	—	—	IIC2_SCL_E	I2C2_SCL_E	—	—
IP6[19:17]	ETH_RX_ER	—	—	—	—	IIC2_SDA_E	I2C2_SDA_E	—	—
IP6[22:20]	ETH_RXD0	—	—	—	—	SCIFB1_SCK_G	SCK1_E	—	—
IP6[25:23]	ETH_RXD1	—	HRX0_E	—	—	—	SCIFB1_RXD_G	RX1_E	—
IP6[28:26]	ETH_LINK	—	HTX0_E	—	SCIFB1_TXD_G	TX1_E	—	—	—
IP6[31:29]	ETH_REF_CLK	—	HCTS0#_E	—	HRX0_F	—	—	—	—

Legend: — Setting prohibited

5.3.15 Peripheral Function Select Register 7 (IPSR7)

Function: IPSR7 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	IP7 [30]	IP7 [29]	IP7 [28]	IP7 [27]	IP7 [26]	IP7 [25]	IP7 [24]	IP7 [23]	IP7 [22]	IP7 [21]	IP7 [20]	IP7 [19]	IP7 [18]	IP7 [17]	IP7 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP7 [15]	IP7 [14]	IP7 [13]	IP7 [12]	IP7 [11]	IP7 [10]	IP7 [9]	IP7 [8]	IP7 [7]	IP7 [6]	IP7 [5]	IP7 [4]	IP7 [3]	IP7 [2]	IP7 [1]	IP7 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Others (Set Value = H'6 to H'F)
IP7[2:0]	ETH_MDIO	—	HRTS0#_E	—	HCTS0#_F	—	—
IP7[5:3]	ETH_TXD1	—	HTX0_F	—	—	—	—
IP7[7:6]	ETH_TX_EN	—	—	HRTS0#_F	—	—	—
IP7[9:8]	ETH_MAGIC	—	—	—	—	—	—
IP7[12:10]	ETH_TXD0	—	—	—	—	—	—
IP7[15:13]	ETH_MDC	—	—	—	—	—	—
IP7[18:16]	PWM0	SCIFA2_SCK_C	—	—	—	—	—
IP7[21:19]	PWM1	SCIFA2_TXD_C	—	—	—	—	—
IP7[24:22]	PWM2	—	SCIFA2_RXD_C	—	——	—	—
IP7[26:25]	DU_DOTCLKIN1	AUDIO_CLKC	AUDIO_CLKOUT_C	—	—	—	—
IP7[28:27]	VI0_CLK	ATACS00#	AVB_RXD1	—	—	—	—
IP7[30:29]	VI0_DATA0_VI0_B0	ATACS10#	AVB_RXD2	—	—	—	—

Legend: — Setting prohibited

5.3.16 Peripheral Function Select Register 8 (IPSR8)

Function: IPSR8 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	IP8 [30]	IP8 [29]	IP8 [28]	IP8 [27]	IP8 [26]	IP8 [25]	IP8 [24]	IP8 [23]	IP8 [22]	IP8 [21]	IP8 [20]	IP8 [19]	IP8 [18]	IP8 [17]	IP8 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP8 [15]	IP8 [14]	IP8 [13]	IP8 [12]	IP8 [11]	IP8 [10]	IP8 [9]	IP8 [8]	IP8 [7]	IP8 [6]	IP8 [5]	IP8 [4]	IP8 [3]	IP8 [2]	IP8 [1]	IP8 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Function 9 (Set Value = H'8)	Others (Set Value = H'9 to H'F)
IP8[1:0]	VI0_DATA1_VI0_B1	ATARD0#	AVB_RXD3	—	—	—	—	—	—	—
IP8[3:2]	VI0_DATA2_VI0_B2	ATAWR0#	AVB_RXD4	—	—	—	—	—	—	—
IP8[5:4]	VI0_DATA3_VI0_B3	ATADIR0#	AVB_RXD5	—	—	—	—	—	—	—
IP8[7:6]	VI0_DATA4_VI0_B4	ATAG0#	AVB_RXD6	—	—	—	—	—	—	—
IP8[9:8]	VI0_DATA5_VI0_B5	EX_WAIT1	AVB_RXD7	—	—	—	—	—	—	—
IP8[11:10]	VI0_DATA6_VI0_B6	AVB_RX_ER	—	—	—	—	—	—	—	—
IP8[13:12]	VI0_DATA7_VI0_B7	AVB_RX_CLK	—	—	—	—	—	—	—	—
IP8[15:14]	VI1_CLK	AVB_RX_DV	—	—	—	—	—	—	—	—
IP8[17:16]	VI1_DATA0_VI1_B0	SCIFA1_SCK_D	AVB_CRS	—	—	—	—	—	—	—
IP8[19:18]	VI1_DATA1_VI1_B1	SCIFA1_RXD_D	AVB_MDC	—	—	—	—	—	—	—
IP8[21:20]	VI1_DATA2_VI1_B2	SCIFA1_TXD_D	AVB_MDIO	—	—	—	—	—	—	—
IP8[23:22]	VI1_DATA3_VI1_B3	SCIFA1_CTS#_D	AVB_GTX_CLK	—	—	—	—	—	—	—
IP8[25:24]	VI1_DATA4_VI1_B4	SCIFA1_RTS#_D	AVB_MAGIC	—	—	—	—	—	—	—
IP8[26]	VI1_DATA5_VI1_B5	AVB_PHY_INT	—	—	—	—	—	—	—	—
IP8[27]	VI1_DATA6_VI1_B6	AVB_GTXREFCLK	—	—	—	—	—	—	—	—
IP8[28]	SD0_CLK	VI1_DATA0_VI1_B0_B	—	—	—	—	—	—	—	—
IP8[30:29]	SD0_CMD	SCIFB1_SCK_B	VI1_DATA1_VI1_B1_B	—	—	—	—	—	—	—

Legend: — Setting prohibited

5.3.17 Peripheral Function Select Register 9 (IPSR9)

Function: IPSR9 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP9 [31]	IP9 [30]	IP9 [29]	IP9 [28]	IP9 [27]	IP9 [26]	IP9 [25]	IP9 [24]	IP9 [23]	IP9 [22]	IP9 [21]	IP9 [20]	IP9 [19]	IP9 [18]	IP9 [17]	IP9 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP9 [15]	IP9 [14]	IP9 [13]	IP9 [12]	IP9 [11]	IP9 [10]	IP9 [9]	IP9 [8]	IP9 [7]	IP9 [6]	IP9 [5]	IP9 [4]	IP9 [3]	IP9 [2]	IP9 [1]	IP9 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Function 9 (Set Value = H'8)	Function 10 (Set Value = H'9)	Others (Set Value = H'A to H'F)
IP9[1:0]	SD0_DAT0	SCIFB1_RXD_B	VI1_DATA2_VI1_B2_B	—	—	—	—	—	—	—	—
IP9[3:2]	SD0_DAT1	SCIFB1_TXD_B	VI1_DATA3_VI1_B3_B	—	—	—	—	—	—	—	—
IP9[5:4]	SD0_DAT2	SCIFB1_CTS#_B	VI1_DATA4_VI1_B4_B	—	—	—	—	—	—	—	—
IP9[7:6]	SD0_DAT3	SCIFB1_RTS#_B	VI1_DATA5_VI1_B5_B	—	—	—	—	—	—	—	—
IP9 [11:8]	SD0_CD	MMC0_D6	—	—	—	VI1_DATA6_VI1_B6_B	IIC1_SCL_B	I2C1_SCL_B	VI2_DATA6_VI2_B6_B	—	—
IP9 [15:12]	SD0_WP	MMC0_D7	—	—	—	VI1_DATA7_VI1_B7_B	IIC1_SDA_B	I2C1_SDA_B	VI2_DATA7_VI2_B7_B	—	—
IP9 [17:16]	SD1_CLK	AVB_TX_EN	—	—	—	—	—	—	—	—	—
IP9 [19:18]	SD1_CMD	AVB_TX_ER	—	SCIFB0_SCK_B	—	—	—	—	—	—	—
IP9 [21:20]	SD1_DAT0	AVB_TX_CLK	—	SCIFB0_RXD_B	—	—	—	—	—	—	—
IP9 [23:22]	SD1_DAT1	AVB_LINK	—	SCIFB0_TXD_B	—	—	—	—	—	—	—
IP9 [25:24]	SD1_DAT2	AVB_COL	—	SCIFB0_CTS#_B	—	—	—	—	—	—	—
IP9 [27:26]	SD1_DAT3	AVB_RXD0	—	SCIFB0_RTS#_B	—	—	—	—	—	—	—
IP9 [31:28]	SD1_CD	MMC1_D6	—	—	—	VI0_CLK_B	IIC2_SCL_D	I2C2_SCL_D	—	VI3_CLK_B	—

Legend: — Setting prohibited

5.3.18 Peripheral Function Select Register 10 (IPSR10)

Function: IPSR10 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	IP10 [29]	IP10 [28]	IP10 [27]	IP10 [26]	IP10 [25]	IP10 [24]	IP10 [23]	IP10 [22]	IP10 [21]	IP10 [20]	IP10 [19]	IP10 [18]	IP10 [17]	IP10 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP10 [15]	IP10 [14]	IP10 [13]	IP10 [12]	IP10 [11]	IP10 [10]	IP10 [9]	IP10 [8]	IP10 [7]	IP10 [6]	IP10 [5]	IP10 [4]	IP10 [3]	IP10 [2]	IP10 [1]	IP10 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Function 9 (Set Value = H'8)	Function 10 (Set Value = H'9)	Others (Set Value = H'A to H'F)
IP10 [3:0]	SD1_WP	MMC1_D7	—	—	—	VI1_CLK_B	IIC2_SDA_D	I2C2_SDA_D	—	—	—
IP10 [6:4]	SD2_CLK	MMC0_CLK	—	VI0_DATA0_VI0_B0_B	—	—	VI3_DATA0_B	—	—	—	—
IP10 [10:7]	SD2_CMD	MMC0_CMD	—	VI0_DATA1_VI0_B1_B	SCIFB1_SCK_E	SCK1_D	—	—	VI3_DATA1_B	—	—
IP10 [14:11]	SD2_DAT0	MMC0_D0	—	VI0_DATA2_VI0_B2_B	SCIFB1_RXD_E	RX1_D	—	—	VI3_DATA2_B	—	—
IP10 [18:15]	SD2_DAT1	MMC0_D1	—	—	VI0_DATA3_VI0_B3_B	SCIFB1_TXD_E	TX1_D	—	—	VI3_DATA3_B	—
IP10 [22:19]	SD2_DAT2	MMC0_D2	—	—	VI0_DATA4_VI0_B4_B	HRX0_D	—	—	VI3_DATA4_B	—	—
IP10 [25:23]	SD2_DAT3	MMC0_D3	—	VI0_DATA5_VI0_B5_B	HTX0_D	—	—	VI3_DATA5_B	—	—	—
IP10 [29:26]	SD2_CD	MMC0_D4	—	—	—	VI0_DATA6_VI0_B6_B	HCTS0#_D	—	—	VI3_DATA6_B	—

Legend: — Setting prohibited

5.3.19 Peripheral Function Select Register 11 (IPSR11)

Function: IPSR11 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP11 [31]	IP11 [30]	IP11 [29]	IP11 [28]	IP11 [27]	IP11 [26]	IP11 [25]	IP11 [24]	IP11 [23]	IP11 [22]	IP11 [21]	IP11 [20]	IP11 [19]	IP11 [18]	IP11 [17]	IP11 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP11 [15]	IP11 [14]	IP11 [13]	IP11 [12]	IP11 [11]	IP11 [10]	IP11 [9]	IP11 [8]	IP11 [7]	IP11 [6]	IP11 [5]	IP11 [4]	IP11 [3]	IP11 [2]	IP11 [1]	IP11 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Function 9 (Set Value = H'8)	Function 10 (Set Value = H'9)	Others (Set Value = H'A to H'F)
IP11 [3:0]	SD2_WP	MMC0_D5	—	—	—	VI0_DATA7_VI0_B7_B	HRTS0#_D	—	—	VI3_DATA7_B	—
IP11[4]	SD3_CLK	MMC1_CLK	—	—	—	—	—	—	—	—	—
IP11 [6:5]	SD3_CMD	MMC1_CMD	—	—	—	—	—	—	—	—	—
IP11 [8:7]	SD3_DAT0	MMC1_D0	—	—	—	—	—	—	—	—	—
IP11 [10:9]	SD3_DAT1	MMC1_D1	—	—	—	—	—	—	—	—	—
IP11 [12:11]	SD3_DAT2	MMC1_D2	—	—	—	—	—	—	—	—	—
IP11 [14:13]	SD3_DAT3	MMC1_D3	—	—	—	—	—	—	—	—	—
IP11 [17:15]	SD3_CD	MMC1_D4	—	—	—	—	—	—	—	—	—
IP11 [21:18]	SD3_WP	MMC1_D5	—	—	—	—	—	—	—	—	—
IP11 [23:22]	—	IIC2_SCL_B	I2C2_SCL_B	—	—	—	—	—	—	—	—
IP11 [26:24]	—	SCIFB1_RXD_D	RX1_C	IIC2_SDA_B	I2C2_SDA_B	—	—	—	—	—	—
IP11 [29:27]	—	—	SCIFB1_TXD_D	TX1_C	—	—	—	—	—	—	—
IP11 [31:30]	SSI_SCK0129	CAN_CLK_B	—	—	—	—	—	—	—	—	—

Legend: — Setting prohibited

5.3.20 Peripheral Function Select Register 12 (IPSR12)

Function: IPSR12 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	IP12 [30]	IP12 [29]	IP12 [28]	IP12 [27]	IP12 [26]	IP12 [25]	IP12 [24]	IP12 [23]	IP12 [22]	IP12 [21]	IP12 [20]	IP12 [19]	IP12 [18]	IP12 [17]	IP12 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP12 [15]	IP12 [14]	IP12 [13]	IP12 [12]	IP12 [11]	IP12 [10]	IP12 [9]	IP12 [8]	IP12 [7]	IP12 [6]	IP12 [5]	IP12 [4]	IP12 [3]	IP12 [2]	IP12 [1]	IP12 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Others (Set Value = H'7 to H'F)
IP12[1:0]	SSI_WS0129	CAN0_TX_B	—	—	—	—	—	—
IP12[3:2]	SSI_SDATA0	CAN0_RX_B	—	—	—	—	—	—
IP12[5:4]	SSI_SDATA1	CAN1_TX_B	—	—	—	—	—	—
IP12[7:6]	SSI_SDATA2	CAN1_RX_B	SSI_SCK1	—	—	—	—	—
IP12[10:8]	SSI_SCK34	—	SCIFB0_SCK	MSIOF1_SCK	—	—	—	—
IP12[13:11]	SSI_WS34	—	SCIFB0_RXD	MSIOF1_SYNC	—	—	—	—
IP12[16:14]	SSI_SDATA3	—	SCIFB0_TXD	MSIOF1_SS1	—	—	—	—
IP12[19:17]	SSI_SCK4	—	SCIFB0_CTS#	MSIOF1_SS2	SSI_SCK5_C	—	—	—
IP12[22:20]	SSI_WS4	—	SCIFB0_RTS#	MSIOF1_TXD	SSI_WS5_C	—	—	—
IP12[24:23]	SSI_SDATA4	—	MSIOF1_RXD	—	—	—	—	—
IP12[27:25]	SSI_SCK5	SCIFB1_SCK	—	DU_EXHSYNC_DU_HSYNC	—	—	—	—
IP12[30:28]	SSI_WS5	SCIFB1_RXD	—	DU_EXVSYNC_DU_VSYNC	—		—	—

Legend: — Setting prohibited

5.3.21 Peripheral Function Select Register 13 (IPSR13)

Function: IPSR13 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	IP13 [30]	IP13 [29]	IP13 [28]	IP13 [27]	IP13 [26]	IP13 [25]	IP13 [24]	IP13 [23]	IP13 [22]	IP13 [21]	IP13 [20]	IP13 [19]	IP13 [18]	IP13 [17]	IP13 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP13 [15]	IP13 [14]	IP13 [13]	IP13 [12]	IP13 [11]	IP13 [10]	IP13 [9]	IP13 [8]	IP13 [7]	IP13 [6]	IP13 [5]	IP13 [4]	IP13 [3]	IP13 [2]	IP13 [1]	IP13 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Function 9 (Set Value = H'8)	Function 10 (Set Value = H'9)	Function 11 (Set Value = H'A)	Function 12 (Set Value = H'B)	Others (Set Value = H'C to H'F)
IP13 [2:0]	SSI_SDATA 5	SCIFB1_TX D	—	DU_DR2	—	—	—	—	—	—	—	—	—
IP13 [6:3]	SSI_SCK6	SCIFB1_CT S#	—	—	DU_DR3	—	—	—	—	—	—	—	—
IP13 [9:7]	SSI_WS6	SCIFB1_RT S#	CAN0_TX_ D	DU_DR4	—	—	—	—	—	—	—	—	—
IP13 [12:10]	SSI_SDATA 6	—	—	DU_DR5	—	—	—	—	—	—	—	—	—
IP13 [15:13]	SSI_SCK78	—	SCK1	SCIFA1_SC K	DU_DR6	—	—	—	—	—	—	—	—
IP13 [18:16]	SSI_WS78	—	SCIFB2_SC K	SCIFA2_CT S#	DU_DR7	—	—	—	—	—	—	—	—
IP13 [22:19]	SSI_SDATA 7	—	SCIFB2_RX D	SCIFA2_RT S#	TCLK2	—	—	—	—	SSI_SDATA 7_B	—	—	—
IP13 [25:23]	SSI_SDATA 8	—	SCIFB2_TX D	CAN0_TX_ C	—	SSI_SDATA 8_B	—	—	—	—	—	—	—
IP13 [28:26]	SSI_SDATA 9	—	SCIFB2_CT S#	SSI_WS1	SSI_SDATA 5_C	—	—	—	—	—	—	—	—
IP13 [30:29]	AUDIO_CL KA	SCIFB2_RT S#	—	—	—	—	—	—	—	—	—	—	—

Legend: — Setting prohibited

5.3.22 Peripheral Function Select Register 14 (IPSR14)

Function: IPSR14 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	IP14 [30]	IP14 [29]	IP14 [28]	IP14 [27]	IP14 [26]	IP14 [25]	IP14 [24]	IP14 [23]	IP14 [22]	IP14 [21]	IP14 [20]	IP14 [19]	IP14 [18]	IP14 [17]	IP14 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP14 [15]	IP14 [14]	IP14 [13]	IP14 [12]	IP14 [11]	IP14 [10]	IP14 [9]	IP14 [8]	IP14 [7]	IP14 [6]	IP14 [5]	IP14 [4]	IP14 [3]	IP14 [2]	IP14 [1]	IP14 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Function 9 (Set Value = H'8)	Others (Set Value = H'9 to H'F)
IP14[2:0]	AUDIO_CLKB	SCIF_CLK	CAN0_RX_D	DVC_MUTE	CAN0_RX_C	—	—	—	—	—
IP14[5:3]	SCIFA0_SCK	HSCK1	SCK0	MSIOF3_SS2	DU_DG2	—	IIC1_SDA_C	I2C1_SDA_C	—	—
IP14[8:6]	SCIFA0_RXD	HRX1	RX0	DU_DR0	—	—	—	—	—	—
IP14[11:9]	SCIFA0_TXD	HTX1	TX0	DU_DR1	—	—	—	—	—	—
IP14[15:12]	SCIFA0_CTS#	HCTS1#	CTS0#	MSIOF3_SYNC	DU_DG3	—	PWM0_B	IIC1_SCL_C	I2C1_SCL_C	—
IP14[18:16]	SCIFA0_RTS#	HRTS1#	RTS0#	MSIOF3_SS1	DU_DG0	—	PWM1_B	—	—	—
IP14[21:19]	SCIFA1_RXD	—	RX1	DU_EXODDF_ DU_ODDF_DIS P_CDE	—	—	—	—	—	—
IP14[24:22]	SCIFA1_TXD	—	TX1	DU_DG1	—	—	—	—	—	—
IP14[27:25]	SCIFA1_CTS#	—	CTS1#	MSIOF3_RXD	DU_DOTCLKO UT0	—	—	—	—	—
IP14[30:28]	SCIFA1_RTS#	—	RTS1#	MSIOF3_TXD	DU_DOTCLKO UT1	—	HRTS0#_C	—	—	—

Legend: — Setting prohibited

5.3.23 Peripheral Function Select Register 15 (IPSR15)

Function: IPSR15 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	IP15 [29]	IP15 [28]	IP15 [27]	IP15 [26]	IP15 [25]	IP15 [24]	IP15 [23]	IP15 [22]	IP15 [21]	IP15 [20]	IP15 [19]	IP15 [18]	IP15 [17]	IP15 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP15 [15]	IP15 [14]	IP15 [13]	IP15 [12]	IP15 [11]	IP15 [10]	IP15 [9]	IP15 [8]	IP15 [7]	IP15 [6]	IP15 [5]	IP15 [4]	IP15 [3]	IP15 [2]	IP15 [1]	IP15 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Function 9 (Set Value = H'8)	Others (Set Value = H'9 to H'F)
IP15[2:0]	SCIFA2_SCK	—	SCK2	MSIOF3_SCK	DU_DG7	—	SCIF_CLK_B	—	—	—
IP15[5:3]	SCIFA2_RXD	—	TX2	DU_DB0	—	IIC2_SCL	I2C2_SCL	—	—	—
IP15[8:6]	SCIFA2_TXD	—	RX2	DU_DB1	—	IIC2_SDA	I2C2_SDA	—	—	—
IP15[11:9]	HSCK0	—	DU_DG4	—	HCTS0#_C	—	—	—	—	—
IP15[13:12]	HRX0	DU_DB2	—	—	—	—	—	—	—	—
IP15[15:14]	HTX0	DU_DB3	—	—	—	—	—	—	—	—
IP15[17:16]	HCTS0#	SSI_SCK9	DU_DB4	—	—	—	—	—	—	—
IP15[19:18]	HRTS0#	SSI_WS9	DU_DB5	—	—	—	—	—	—	—
IP15[22:20]	MSIOF0_SCK	—	—	DU_DB6	—	—	—	—	—	—
IP15[25:23]	MSIOF0_SYNC	—	SSI_SCK2	—	DU_DB7	—	HRX0_C	—	—	—
IP15[27:26]	MSIOF0_SS1	—	DU_DG5	—	—	—	—	—	—	—
IP15[29:28]	MSIOF0_TXD	—	DU_DG6	—	—	—	—	—	—	—

Legend: — Setting prohibited

5.3.24 Peripheral Function Select Register 16 (IPSR16)

Function: IPSR16 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	IP16 [7]	IP16 [6]	IP16 [5]	IP16 [4]	IP16 [3]	IP16 [2]	IP16 [1]	IP16 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Function 9 (Set Value = H'8)	Others (Set Value = H'9 to H'F)
IP16[2:0]	MSIOF0_SS2	AUDIO_CLKOUT	—	DU_DISP	—	HTX0_C	SCIFA2_TXD_B	—	—	—
IP16[5:3]	MSIOF0_RXD	—	SSI_WS2	—	DU_CDE	—	SCIFA2_RXD_B	—	—	—
IP16[6]	USB1_PWEN	AUDIO_CLKOUT_D	—	—	—	—	—	—	—	—
IP16[7]	USB1_OVC	TCLK1_B	—	—	—	—	—	—	—	—

Legend: — Setting prohibited

Table 5.2 shows the correspondence between the function signals and the bit settings in the GPIO/peripheral function select registers and peripheral function select registers.

Table 5.2 Correspondence between Function Signals and Register Bit Settings

GPIO (GP Set Value = 0)	Peripheral Module (GP Set Value = 1) Function Selected by IP Bits: Function 1 (IP Set Value = H'0)	Function 2 (IP Set Value = H'1)	Function 3 (IP Set Value = H'2)	Function 4 (IP Set Value = H'3)	Function 5 (IP Set Value = H'4)	Function 6 (IP Set Value = H'5)	Function 7 (IP Set Value = H'6)	Function 8 (IP Set Value = H'7)	Function 9 (IP Set Value = H'8)	Function 10 (IP Set Value = H'9)	Function 11 (IP Set Value = H'A)	Function 12 (IP Set Value = H'B)	GPIO/ Peripheral Function Selecting Bit	Peripheral Function Selecting Bit
GP-0-0	D0	MSIOF3_SCK_B	VI3_DATA0	VI0_G4	VI0_G4_B	—	—	—	—	—	—	—	GP0[0]	IP0[2:0]
GP-0-1	D1	MSIOF3_SYNC_B	VI3_DATA1	VI0_G5	VI0_G5_B	—	—	—	—	—	—	—	GP0[1]	IP0[5:3]
GP-0-2	D2	MSIOF3_RXD_B	VI3_DATA2	VI0_G6	VI0_G6_B	—	—	—	—	—	—	—	GP0[2]	IP0[8:6]
GP-0-3	D3	MSIOF3_TXD_B	VI3_DATA3	VI0_G7	VI0_G7_B	—	—	—	—	—	—	—	GP0[3]	IP0[11:9]
GP-0-4	D4	SCIFB1_RXD_F	SCIFB0_RXD_C	VI3_DATA4	VI0_R0	VI0_R0_B	RX0_B	—	—	—	—	—	GP0[4]	IP0[15:12]
GP-0-5	D5	SCIFB1_TXD_F	SCIFB0_TXD_C	VI3_DATA5	VI0_R1	VI0_R1_B	TX0_B	—	—	—	—	—	GP0[5]	IP0[19:16]
GP-0-6	D6	IIC2_SCL_C	VI3_DATA6	VI0_R2	VI0_R2_B	I2C2_SCL_C	—	—	—	—	—	—	GP0[6]	IP0[22:20]
GP-0-7	D7	—	IIC2_SDA_C	VI3_DATA7	VI0_R3	VI0_R3_B	I2C2_SDA_C	TCLK1	—	—	—	—	GP0[7]	IP0[26:23]
GP-0-8	D8	SCIFA1_SCK_C	AVB_TXD0	—	VI0_G0	VI0_G0_B	VI2_DATA0_VI2_B0	—	—	—	—	—	GP0[8]	IP0[30:27]
GP-0-9	D9	SCIFA1_RXD_C	AVB_TXD1	—	VI0_G1	VI0_G1_B	VI2_DATA1_VI2_B1	—	—	—	—	—	GP0[9]	IP1[3:0]
GP-0-10	D10	SCIFA1_TXD_C	AVB_TXD2	—	VI0_G2	VI0_G2_B	VI2_DATA2_VI2_B2	—	—	—	—	—	GP0[10]	IP1[7:4]
GP-0-11	D11	SCIFA1_CTS#_C	AVB_TXD3	—	VI0_G3	VI0_G3_B	VI2_DATA3_VI2_B3	—	—	—	—	—	GP0[11]	IP1[11:8]
GP-0-12	D12	SCIFA1_RTS#_C	AVB_TXD4	VI0_HSYNC#	VI0_HSYNC#_B	VI2_DATA4_VI2_B4	—	—	—	—	—	—	GP0[12]	IP1[14:12]
GP-0-13	D13	AVB_TXD5	VI0_VSYNC#	VI0_VSYNC#_B	VI2_DATA5_VI2_B5	—	—	—	—	—	—	—	GP0[13]	IP1[17:15]
GP-0-14	D14	SCIFB1_RXD_C	AVB_TXD6	RX1_B	VI0_CLKENB	VI0_CLKENB_B	VI2_DATA6_VI2_B6	—	—	—	—	—	GP0[14]	IP1[21:18]
GP-0-15	D15	SCIFB1_TXD_C	AVB_TXD7	TX1_B	VI0_FIELD	VI0_FIELD_B	VI2_DATA7_VI2_B7	—	—	—	—	—	GP0[15]	IP1[25:22]
GP-0-16	A0	PWM3	—	—	—	—	—	—	—	—	—	—	GP0[16]	IP1[27:26]
GP-0-17	A1	PWM4	—	—	—	—	—	—	—	—	—	—	GP0[17]	IP1[29:28]
GP-0-18	A2	PWM5	MSIOF1_SS1_B	—	—	—	—	—	—	—	—	—	GP0[18]	IP2[2:0]
GP-0-19	A3	PWM6	MSIOF1_SS2_B	—	—	—	—	—	—	—	—	—	GP0[19]	IP2[5:3]
GP-0-20	A4	MSIOF1_TXD_B	TPU0TO0	—	—	—	—	—	—	—	—	—	GP0[20]	IP2[8:6]
GP-0-21	A5	SCIFA1_TXD_B	TPU0TO1	—	—	—	—	—	—	—	—	—	GP0[21]	IP2[11:9]
GP-0-22	A6	SCIFA1_RTS#_B	TPU0TO2	—	—	—	—	—	—	—	—	—	GP0[22]	IP2[14:12]
GP-0-23	A7	SCIFA1_SCK_B	AUDIO_CLKOUT_B	TPU0TO3	—	—	—	—	—	—	—	—	GP0[23]	IP2[17:15]
GP-0-24	A8	SCIFA1_RXD_B	SSI_SCK5_B	VI0_R4	VI0_R4_B	SCIFB2_RXD_C	RX2_B	VI2_DATA0_VI2_B0_B	—	—	—	—	GP0[24]	IP2[21:18]
GP-0-25	A9	SCIFA1_CTS#_B	SSI_WS5_B	VI0_R5	VI0_R5_B	SCIFB2_TXD_C	TX2_B	VI2_DATA1_VI2_B1_B	—	—	—	—	GP0[25]	IP2[25:22]
GP-0-26	A10	SSI_SDATA5_B	MSIOF2_SYNC	VI0_R6	VI0_R6_B	VI2_DATA2_VI2_B2_B	—	—	—	—	—	—	GP0[26]	IP2[28:26]
GP-0-27	A11	SCIFB2_CTS#_B	MSIOF2_SCK	VI1_R0	VI1_R0_B	VI2_G0	VI2_DATA3_VI2_B3_B	—	—	—	—	—	GP0[27]	IP3[3:0]
GP-0-28	A12	SCIFB2_RXD_B	MSIOF2_TXD	VI1_R1	VI1_R1_B	VI2_G1	VI2_DATA4_VI2_B4_B	—	—	—	—	—	GP0[28]	IP3[7:4]
GP-0-29	A13	SCIFB2_RTS#_B	EX_WAIT2	MSIOF2_RXD	VI1_R2	VI1_R2_B	VI2_G2	VI2_DATA5_VI2_B5_B	—	—	—	—	GP0[29]	IP3[11:8]
GP-0-30	A14	SCIFB2_TXD_B	ATACS11#	MSIOF2_SS1	—	—	—	—	—	—	—	—	GP0[30]	IP3[14:12]
GP-0-31	A15	SCIFB2_SCK_B	ATARD1#	MSIOF2_SS2	—	—	—	—	—	—	—	—	GP0[31]	IP3[17:15]

GPIO (GP Set Value = 0)	Peripheral Module (GP Set Value = 1) Function Selected by IP Bits Function 1 (IP Set Value = H'0)	Function 2 (IP Set Value = H'1)	Function 3 (IP Set Value = H'2)	Function 4 (IP Set Value = H'3)	Function 5 (IP Set Value = H'4)	Function 6 (IP Set Value = H'5)	Function 7 (IP Set Value = H'6)	Function 8 (IP Set Value = H'7)	Function 9 (IP Set Value = H'8)	Function 10 (IP Set Value = H'9)	Function 11 (IP Set Value = H'A)	Function 12 (IP Set Value = H'B)	GPIO/ Peripheral Function Selecting Bit	Peripheral Function Selecting Bit
GP-1-0	A16	ATAWR1#	—	—	—	—	—	—	—	—	—	—	GP1[0]	IP3[19:18]
GP-1-1	A17	—	ATADIR1#	—	—	—	—	—	—	—	—	—	GP1[1]	IP3[22:20]
GP-1-2	A18	—	ATAG1#	—	—	—	—	—	—	—	—	—	GP1[2]	IP3[25:23]
GP-1-3	A19	—	ATACS01#	EX_WAIT0_B	—	—	—	—	—	—	—	—	GP1[3]	IP3[28:26]
GP-1-4	A20	SPCLK	VI1_R3	VI1_R3_B	VI2_G4	—	—	—	—	—	—	—	GP1[4]	IP3[31:29]
GP-1-5	A21	MOSI_IO0	VI1_R4	VI1_R4_B	VI2_G5	—	—	—	—	—	—	—	GP1[5]	IP4[2:0]
GP-1-6	A22	MISO_IO1	VI1_R5	VI1_R5_B	VI2_G6	—	—	—	—	—	—	—	GP1[6]	IP4[5:3]
GP-1-7	A23	IO2	VI1_G7	VI1_G7_B	VI2_G7	—	—	—	—	—	—	—	GP1[7]	IP4[8:6]
GP-1-8	A24	IO3	VI1_R7	VI1_R7_B	VI2_CLKENB	VI2_CLKENB_B	—	—	—	—	—	—	GP1[8]	IP4[11:9]
GP-1-9	A25	SSL	VI1_G6	VI1_G6_B	VI2_FIELD	VI2_FIELD_B	—	—	—	—	—	—	GP1[9]	IP4[14:12]
GP-1-10	CS0#	VI1_R6	VI1_R6_B	VI2_G3	MSIOF0_SS2_B	—	—	—	—	—	—	—	GP1[10]	IP4[17:15]
GP-1-11	CS1#_A26	—	VI0_R7	VI0_R7_B	VI2_CLK	VI2_CLK_B	—	—	—	—	—	—	GP1[11]	IP4[20:18]
GP-1-12	EX_CS0#	HRX1_B	VI1_G5	VI1_G5_B	VI2_R0	HTX0_B	MSIOF0_SS1_B	—	—	—	—	—	GP1[12]	IP4[23:21]
GP-1-13	EX_CS1#	—	HCTS1#_B	VI1_FIELD	VI1_FIELD_B	VI2_R1	—	—	—	—	—	—	GP1[13]	IP4[26:24]
GP-1-14	EX_CS2#	—	HRTS1#_B	VI3_CLKENB	VI1_G0	VI1_G0_B	VI2_R2	—	—	—	—	—	GP1[14]	IP4[29:27]
GP-1-15	EX_CS3#	—	VI3_FIELD	VI1_G1	VI1_G1_B	VI2_R3	—	—	—	—	—	—	GP1[15]	IP5[2:0]
GP-1-16	EX_CS4#	MSIOF1_SCK_B	VI3_HSYNC#	VI2_HSYNC#	IIC1_SCL	VI2_HSYNC#_B	—	I2C1_SCL	—	—	—	—	GP1[16]	IP5[5:3]
GP-1-17	EX_CS5#	CAN0_RX	MSIOF1_RXD_B	VI3_VSYNC#	VI1_G2	VI1_G2_B	VI2_R4	IIC1_SDA	—	I2C1_SDA	—	—	GP1[17]	IP5[9:6]
GP-1-18	BS#	—	HTX1_B	CAN1_TX	DRACK0	—	—	—	—	—	—	—	GP1[18]	IP5[12:10]
GP-1-19	RD#	CAN0_TX	SCIFA0_SCK_B	—	—	—	—	—	—	—	—	—	GP1[19]	IP5[14:13]
GP-1-20	RD_WR#	VI1_G3	VI1_G3_B	VI2_R5	SCIFA0_RXD_B	—	—	—	—	—	—	—	GP1[20]	IP5[17:15]
GP-1-21	WE0#	—	CAN_CLK	VI2_VSYNC#	SCIFA0_TXD_B	VI2_VSYNC#_B	—	—	—	—	—	—	GP1[21]	IP5[20:18]
GP-1-22	WE1#	—	CAN1_RX	VI1_G4	VI1_G4_B	VI2_R6	SCIFA0_CTS#_B	—	—	—	—	—	GP1[22]	IP5[23:21]
GP-1-23	EX_WAIT0	IRQ3	—	VI3_CLK	SCIFA0_RTS#_B	HRX0_B	MSIOF0_SCK_B	—	—	—	—	—	GP1[23]	IP5[26:24]
GP-1-24	DREQ0	VI1_HSYNC#	VI1_HSYNC#_B	VI2_R7	SSI_SCK78_C	SSI_WS78_B	—	—	—	—	—	—	GP1[24]	IP5[29:27]
GP-1-25	DACK0	IRQ0	—	SSI_SCK6_B	VI1_VSYNC#	VI1_VSYNC#_B	SSI_WS78_C	—	—	—	—	—	GP1[25]	IP6[2:0]
GP-1-26	DREQ1	VI1_CLKENB	VI1_CLKENB_B	SSI_SDATA7_C	SSI_SCK78_B	—	—	—	—	—	—	—	GP1[26]	IP6[5:3]
GP-1-27	DACK1	IRQ1	—	SSI_WS6_B	SSI_SDATA8_C	—	—	—	—	—	—	—	GP1[27]	IP6[8:6]
GP-1-28	DREQ2	HSCK1_B	HCTS0#_B	MSIOF0_TXD_B	—	—	—	—	—	—	—	—	GP1[28]	IP6[10:9]
GP-1-29	DACK2	IRQ2	—	SSI_SDATA6_B	HRTS0#_B	MSIOF0_RXD_B	—	—	—	—	—	—	GP1[29]	IP6[13:11]
GP-1-30	—	—	—	—	—	—	—	—	—	—	—	—	GP1[30]	—
GP-1-31	—	—	—	—	—	—	—	—	—	—	—	—	GP1[31]	—
GP-2-0	VI0_CLK	ATACS00#	AVB_RXD1	—	—	—	—	—	—	—	—	—	GP2[0]	IP7[28:27]
GP-2-1	VI0_DATA0_VI0_B0	ATACS10#	AVB_RXD2	—	—	—	—	—	—	—	—	—	GP2[1]	IP7[30:29]
GP-2-2	VI0_DATA1_VI0_B1	ATARD0#	AVB_RXD3	—	—	—	—	—	—	—	—	—	GP2[2]	IP8[1:0]
GP-2-3	VI0_DATA2_VI0_B2	ATAWR0#	AVB_RXD4	—	—	—	—	—	—	—	—	—	GP2[3]	IP8[3:2]
GP-2-4	VI0_DATA3_VI0_B3	ATADIR0#	AVB_RXD5	—	—	—	—	—	—	—	—	—	GP2[4]	IP8[5:4]
GP-2-5	VI0_DATA4_VI0_B4	ATAG0#	AVB_RXD6	—	—	—	—	—	—	—	—	—	GP2[5]	IP8[7:6]
GP-2-6	VI0_DATA5_VI0_B5	EX_WAIT1	AVB_RXD7	—	—	—	—	—	—	—	—	—	GP2[6]	IP8[9:8]

GPIO (GP Set Value = 0)	Peripheral Module (GP Set Value = 1) Function Selected by IP Bits Function 1 (IP Set Value = H'0)	Function 2 (IP Set Value = H'1)	Function 3 (IP Set Value = H'2)	Function 4 (IP Set Value = H'3)	Function 5 (IP Set Value = H'4)	Function 6 (IP Set Value = H'5)	Function 7 (IP Set Value = H'6)	Function 8 (IP Set Value = H'7)	Function 9 (IP Set Value = H'8)	Function 10 (IP Set Value = H'9)	Function 11 (IP Set Value = H'A)	Function 12 (IP Set Value = H'B)	GPIO/ Peripheral Function Selecting Bit	Peripheral Function Selecting Bit
GP-2-7	VI0_DATA6_VI0_B6	AVB_RX_ER	—	—	—	—	—	—	—	—	—	—	GP2[7]	IP8[11:10]
GP-2-8	VI0_DATA7_VI0_B7	AVB_RX_CLK	—	—	—	—	—	—	—	—	—	—	GP2[8]	IP8[13:12]
GP-2-9	VI1_CLK	AVB_RX_DV	—	—	—	—	—	—	—	—	—	—	GP2[9]	IP8[15:14]
GP-2-10	VI1_DATA0_VI1_B0	SCIFA1_SCK_D	AVB_CRS	—	—	—	—	—	—	—	—	—	GP2[10]	IP8[17:16]
GP-2-11	VI1_DATA1_VI1_B1	SCIFA1_RXD_D	AVB_MDC	—	—	—	—	—	—	—	—	—	GP2[11]	IP8[19:18]
GP-2-12	VI1_DATA2_VI1_B2	SCIFA1_TXD_D	AVB_MDIO	—	—	—	—	—	—	—	—	—	GP2[12]	IP8[21:20]
GP-2-13	VI1_DATA3_VI1_B3	SCIFA1_CTS#_D	AVB_GTX_CLK	—	—	—	—	—	—	—	—	—	GP2[13]	IP8[23:22]
GP-2-14	VI1_DATA4_VI1_B4	SCIFA1_RTS#_D	AVB_MAGIC	—	—	—	—	—	—	—	—	—	GP2[14]	IP8[25:24]
GP-2-15	VI1_DATA5_VI1_B5	AVB_PHY_INT	—	—	—	—	—	—	—	—	—	—	GP2[15]	IP8[26]
GP-2-16	VI1_DATA6_VI1_B6	AVB_GTXREFCLK	—	—	—	—	—	—	—	—	—	—	GP2[16]	IP8[27]
GP-2-17	VI1_DATA7_VI1_B7	—	—	—	—	—	—	—	—	—	—	—	GP2[17]	—
GP-2-18	ETH_CRS_DV	—	—	—	—	IIC2_SCL_E	I2C2_SCL_E	—	—	—	—	—	GP2[18]	IP6[16:14]
GP-2-19	ETH_RX_ER	—	—	—	—	IIC2_SDA_E	I2C2_SDA_E	—	—	—	—	—	GP2[19]	IP6[19:17]
GP-2-20	ETH_RXD0	—	—	—	—	SCIFB1_SCK_G	SCK1_E	—	—	—	—	—	GP2[20]	IP6[22:20]
GP-2-21	ETH_RXD1	—	HRX0_E	—	—	—	SCIFB1_RXD_G	RX1_E	—	—	—	—	GP2[21]	IP6[25:23]
GP-2-22	ETH_LINK	—	HTX0_E	—	SCIFB1_TXD_G	TX1_E	—	—	—	—	—	—	GP2[22]	IP6[28:26]
GP-2-23	ETH_REF_CLK	—	HCTS0#_E	—	HRX0_F	—	—	—	—	—	—	—	GP2[23]	IP6[31:29]
GP-2-24	ETH_MDIO	—	HRTS0#_E	—	HCTS0#_F	—	—	—	—	—	—	—	GP2[24]	IP7[2:0]
GP-2-25	ETH_TXD1	—	HTX0_F	—	—	—	—	—	—	—	—	—	GP2[25]	IP7[5:3]
GP-2-26	ETH_TX_EN	—	—	HRTS0#_F	—	—	—	—	—	—	—	—	GP2[26]	IP7[7:6]
GP-2-27	ETH_MAGIC	—	—	—	—	—	—	—	—	—	—	—	GP2[27]	IP7[9:8]
GP-2-28	ETH_TXD0	—	—	—	—	—	—	—	—	—	—	—	GP2[28]	IP7[12:10]
GP-2-29	ETH_MDC	—	—	—	—	—	—	—	—	—	—	—	GP2[29]	IP7[15:13]
GP-2-30	—	—	—	—	—	—	—	—	—	—	—	—	GP2[30]	—
GP-2-31	—	—	—	—	—	—	—	—	—	—	—	—	GP2[31]	—
GP-3-0	SD0_CLK	VI1_DATA0_VI1_B0_B	—	—	—	—	—	—	—	—	—	—	GP3[0]	IP8[28]
GP-3-1	SD0_CMD	SCIFB1_SCK_B	VI1_DATA1_VI1_B1_B	—	—	—	—	—	—	—	—	—	GP3[1]	IP8[30:29]
GP-3-2	SD0_DAT0	SCIFB1_RXD_B	VI1_DATA2_VI1_B2_B	—	—	—	—	—	—	—	—	—	GP3[2]	IP9[1:0]
GP-3-3	SD0_DAT1	SCIFB1_TXD_B	VI1_DATA3_VI1_B3_B	—	—	—	—	—	—	—	—	—	GP3[3]	IP9[3:2]
GP-3-4	SD0_DAT2	SCIFB1_CTS#_B	VI1_DATA4_VI1_B4_B	—	—	—	—	—	—	—	—	—	GP3[4]	IP9[5:4]
GP-3-5	SD0_DAT3	SCIFB1_RTS#_B	VI1_DATA5_VI1_B5_B	—	—	—	—	—	—	—	—	—	GP3[5]	IP9[7:6]
GP-3-6	SD0_CD	MMC0_D6	—	—	—	VI1_DATA6_VI1_B6_B	IIC1_SCL_B	I2C1_SCL_B	VI2_DATA6_VI2_B6_B	—	—	—	GP3[6]	IP9[11:8]
GP-3-7	SD0_WP	MMC0_D7	—	—	—	VI1_DATA7_VI1_B7_B	IIC1_SDA_B	I2C1_SDA_B	VI2_DATA7_VI2_B7_B	—	—	—	GP3[7]	IP9[15:12]
GP-3-8	SD1_CLK	AVB_TX_EN	—	—	—	—	—	—	—	—	—	—	GP3[8]	IP9[17:16]
GP-3-9	SD1_CMD	AVB_TX_ER	—	SCIFB0_SCK_B	—	—	—	—	—	—	—	—	GP3[9]	IP9[19:18]
GP-3-10	SD1_DAT0	AVB_TX_CLK	—	SCIFB0_RXD_B	—	—	—	—	—	—	—	—	GP3[10]	IP9[21:20]
GP-3-11	SD1_DAT1	AVB_LINK	—	SCIFB0_TXD_B	—	—	—	—	—	—	—	—	GP3[11]	IP9[23:22]
GP-3-12	SD1_DAT2	AVB_COL	—	SCIFB0_CTS#_B	—	—	—	—	—	—	—	—	GP3[12]	IP9[25:24]

GPIO (GP Set Value = 0)	Peripheral Module (GP Set Value = 1) Function Selected by IP Bits Function 1 (IP Set Value = H'0)	Function 2 (IP Set Value = H'1)	Function 3 (IP Set Value = H'2)	Function 4 (IP Set Value = H'3)	Function 5 (IP Set Value = H'4)	Function 6 (IP Set Value = H'5)	Function 7 (IP Set Value = H'6)	Function 8 (IP Set Value = H'7)	Function 9 (IP Set Value = H'8)	Function 10 (IP Set Value = H'9)	Function 11 (IP Set Value = H'A)	Function 12 (IP Set Value = H'B)	GPIO/ Peripheral Function Selecting Bit	Peripheral Function Selecting Bit
GP-3-13	SD1_DAT3	AVB_RXD0	—	SCIFB0_RTS#_B	—	—	—	—	—	—	—	—	GP3[13]	IP9[27:26]
GP-3-14	SD1_CD	MMC1_D6	—	—	—	VI0_CLK_B	IIC2_SCL_D	I2C2_SCL_D	—	VI3_CLK_B	—	—	GP3[14]	IP9[31:28]
GP-3-15	SD1_WP	MMC1_D7	—	—	—	VI1_CLK_B	IIC2_SDA_D	I2C2_SDA_D	—	—-	—	—	GP3[15]	IP10[3:0]
GP-3-16	SD2_CLK	MMC0_CLK	—	VI0_DATA0_VI0_B0_B	—	—	VI3_DATA0_B	—	—	—	—	—	GP3[16]	IP10[6:4]
GP-3-17	SD2_CMD	MMC0_CMD	—	VI0_DATA1_VI0_B1_B	SCIFB1_SCK_E	SCK1_D	—	—	VI3_DATA1_B	—	—	—	GP3[17]	IP10[10:7]
GP-3-18	SD2_DAT0	MMC0_D0	—	VI0_DATA2_VI0_B2_B	SCIFB1_RXD_E	RX1_D	—	—	VI3_DATA2_B	—	—	—	GP3[18]	IP10[14:11]
GP-3-19	SD2_DAT1	MMC0_D1	—	—	VI0_DATA3_VI0_B3_B	SCIFB1_TXD_E	TX1_D	—	—	VI3_DATA3_B	—	—	GP3[19]	IP10[18:15]
GP-3-20	SD2_DAT2	MMC0_D2	—	—	VI0_DATA4_VI0_B4_B	HRX0_D	—	—	VI3_DATA4_B	—	—	—	GP3[20]	IP10[22:19]
GP-3-21	SD2_DAT3	MMC0_D3	—	VI0_DATA5_VI0_B5_B	HTX0_D	—	—	VI3_DATA5_B	—	—	—	—	GP3[21]	IP10[25:23]
GP-3-22	SD2_CD	MMC0_D4	—	—	—	VI0_DATA6_VI0_B6_B	HCTS0#_D	—	—	VI3_DATA6_B	—	—	GP3[22]	IP10[29:26]
GP-3-23	SD2_WP	MMC0_D5	—	—	—	VI0_DATA7_VI0_B7_B	HRTS0#_D	—	—	VI3_DATA7_B	—	—	GP3[23]	IP11[3:0]
GP-3-24	SD3_CLK	MMC1_CLK	—	—	—	—	—	—	—	—	—	—	GP3[24]	IP11[4]
GP-3-25	SD3_CMD	MMC1_CMD	—	—	—	—	—	—	—	—	—	—	GP3[25]	IP11[6:5]
GP-3-26	SD3_DAT0	MMC1_D0	—	—	—	—	—	—	—	—	—	—	GP3[26]	IP11[8:7]
GP-3-27	SD3_DAT1	MMC1_D1	—	—	—	—	—	—	—	—	—	—	GP3[27]	IP11[10:9]
GP-3-28	SD3_DAT2	MMC1_D2	—	—	—	—	—	—	—	—	—	—	GP3[28]	IP11[12:11]
GP-3-29	SD3_DAT3	MMC1_D3	—	—	—	—	—	—	—	—	—	—	GP3[29]	IP11[14:13]
GP-3-30	SD3_CD	MMC1_D4	—	—	—	—	—	—	—	—	—	—	GP3[30]	IP11[17:15]
GP-3-31	SD3_WP	MMC1_D5	—	—	—	—	—	—	—	—	—	—	GP3[31]	IP11[21:18]
GP-4-0	—	IIC2_SCL_B	I2C2_SCL_B	—	—	—	—	—	—	—	—	—	GP4[0]	IP11[23:22]
GP-4-1	—	SCIFB1_RXD_D	RX1_C	IIC2_SDA_B	I2C2_SDA_B	—	—	—	—	—	—	—	GP4[1]	IP11[26:24]
GP-4-2	—	—	SCIFB1_TXD_D	TX1_C	—	—	—	—	—	—	—	—	GP4[2]	IP11[29:27]
GP-4-3	SSI_SCK0129	CAN_CLK_B	—	—	—	—	—	—	—	—	—	—	GP4[3]	IP11[31:30]
GP-4-4	SSI_WS0129	CAN0_TX_B	—	—	—	—	—	—	—	—	—	—	GP4[4]	IP12[1:0]
GP-4-5	SSI_SDATA0	CAN0_RX_B	—	—	—	—	—	—	—	—	—	—	GP4[5]	IP12[3:2]
GP-4-6	SSI_SDATA1	CAN1_TX_B	—	—	—	—	—	—	—	—	—	—	GP4[6]	IP12[5:4]
GP-4-7	SSI_SDATA2	CAN1_RX_B	SSI_SCK1	—	—	—	—	—	—	—	—	—	GP4[7]	IP12[7:6]
GP-4-8	SSI_SCK34	—	SCIFB0_SCK	MSIOF1_SCK	—	—	—	—	—	—	—	—	GP4[8]	IP12[10:8]
GP-4-9	SSI_WS34	—	SCIFB0_RXD	MSIOF1_SYNC	—	—	—	—	—	—	—	—	GP4[9]	IP12[13:11]
GP-4-10	SSI_SDATA3	—	SCIFB0_TXD	MSIOF1_SS1	—	—	—	—	—	—	—	—	GP4[10]	IP12[16:14]
GP-4-11	SSI_SCK4	—	SCIFB0_CTS#	MSIOF1_SS2	SSI_SCK5_C	—	—	—	—	—	—	—	GP4[11]	IP12[19:17]
GP-4-12	SSI_WS4	—	SCIFB0_RTS#	MSIOF1_TXD	SSI_WS5_C	—	—	—	—	—	—	—	GP4[12]	IP12[22:20]
GP-4-13	SSI_SDATA4	—	MSIOF1_RXD	—	—	—	—	—	—	—	—	—	GP4[13]	IP12[24:23]
GP-4-14	SSI_SCK5	SCIFB1_SCK	—	DU_EXHSYNC_DU_HSYNC	—	—	—	—	—	—	—	—	GP4[14]	IP12[27:25]
GP-4-15	SSI_WS5	SCIFB1_RXD	—	DU_EXVSYNC_DU_VSYNC	—	—	—	—	—	—	—	—	GP4[15]	IP12[30:28]
GP-4-16	SSI_SDATA5	SCIFB1_TXD	—	DU_DR2	—	—	—	—	—	—	—	—	GP4[16]	IP13[2:0]
GP-4-17	SSI_SCK6	SCIFB1_CTS#	—	—	DU_DR3	—	—	—	—	—	—	—	GP4[17]	IP13[6:3]
GP-4-18	SSI_WS6	SCIFB1_RTS#	CAN0_TX_D	DU_DR4	—	—	—	—	—	—	—	—	GP4[18]	IP13[9:7]
GP-4-19	SSI_SDATA6	—	—	DU_DR5	—	—	—	—	—	—	—	—	GP4[19]	IP13[12:10]
GP-4-20	SSI_SCK78	—	SCK1	SCIFA1_SCK	DU_DR6	—	—	—	—	—	—	—	GP4[20]	IP13[15:13]
GP-4-21	SSI_WS78	—	SCIFB2_SCK	SCIFA2_CTS#	DU_DR7	—	—	—	—	—	—	—	GP4[21]	IP13[18:16]
GP-4-22	SSI_SDATA7	—	SCIFB2_RXD	SCIFA2_RTS#	TCLK2	—	—	—	—	SSI_SDATA7_B	—	—	GP4[22]	IP13[22:19]
GP-4-23	SSI_SDATA8	—	SCIFB2_TXD	CAN0_TX_C	—	SSI_SDATA8_B	—	—	—	—	—	—	GP4[23]	IP13[25:23]

GPIO (GP Set Value = 0)	Peripheral Module (GP Set Value = 1) Function Selected by IP Bits												GPIO/ Peripheral Function Selecting Bit	Peripheral Function Selecting Bit
	Function 1 (IP Set Value = H'0)	Function 2 (IP Set Value = H'1)	Function 3 (IP Set Value = H'2)	Function 4 (IP Set Value = H'3)	Function 5 (IP Set Value = H'4)	Function 6 (IP Set Value = H'5)	Function 7 (IP Set Value = H'6)	Function 8 (IP Set Value = H'7)	Function 9 (IP Set Value = H'8)	Function 10 (IP Set Value = H'9)	Function 11 (IP Set Value = H'A)	Function 12 (IP Set Value = H'B)		
GP-4-24	SSI_SDATA9	—	SCIFB2_CTS#	SSI_WS1	SSI_SDATA5_C	—	—	—	—	—	—	—	GP4[24]	IP13[28:26]
GP-4-25	AUDIO_CLKA	SCIFB2_RTS#	—	—	—	—	—	—	—	—	—	—	GP4[25]	IP13[30:29]
GP-4-26	AUDIO_CLKB	SCIF_CLK	CAN0_RX_D	DVC_MUTE	CAN0_RX_C	—	—	—	—	—	—	—	GP4[26]	IP14[2:0]
GP-4-27	SCIFA0_SCK	HSCK1	SCK0	MSIOF3_SS2	DU_DG2	—	IIC1_SDA_C	I2C1_SDA_C	—	—	—	—	GP4[27]	IP14[5:3]
GP-4-28	SCIFA0_RXD	HRX1	RX0	DU_DR0	—	—	—	—	—	—	—	—	GP4[28]	IP14[8:6]
GP-4-29	SCIFA0_TXD	HTX1	TX0	DU_DR1	—	—	—	—	—	—	—	—	GP4[29]	IP14[11:9]
GP-4-30	SCIFA0_CTS#	HCTS1#	CTS0#	MSIOF3_SYNC	DU_DG3	—	PWM0_B	IIC1_SCL_C	I2C1_SCL_C	—	—	—	GP4[30]	IP14[15:12]
GP-4-31	SCIFA0_RTS#	HRTS1#	RTS0#	MSIOF3_SS1	DU_DG0	—	PWM1_B	—	—	—	—	—	GP4[31]	IP14[18:16]
GP-5-0	SCIFA1_RXD	—	RX1	DU_EXODDF_DU_ODDF_DISP_CDE	—	—	—	—	—	—	—	—	GP5[0]	IP14[21:19]
GP-5-1	SCIFA1_TXD	—	TX1	DU_DG1	—	—	—	—	—	—	—	—	GP5[1]	IP14[24:22]
GP-5-2	SCIFA1_CTS#	—	CTS1#	MSIOF3_RXD	DU_DOTCLKOUT0	—	—	—	—	—	—	—	GP5[2]	IP14[27:25]
GP-5-3	SCIFA1_RTS#	—	RTS1#	MSIOF3_TXD	DU_DOTCLKOUT1	—	HRTS0#_C	—	—	—	—	—	GP5[3]	IP14[30:28]
GP-5-4	SCIFA2_SCK	—	SCK2	MSIOF3_SCK	DU_DG7	—	SCIF_CLK_B	—	—	—	—	—	GP5[4]	IP15[2:0]
GP-5-5	SCIFA2_RXD	—	TX2	DU_DB0	—	IIC2_SCL	I2C2_SCL	—	—	—	—	—	GP5[5]	IP15[5:3]
GP-5-6	SCIFA2_TXD	—	RX2	DU_DB1	—	IIC2_SDA	I2C2_SDA	—	—	—	—	—	GP5[6]	IP15[8:6]
GP-5-7	HSCK0	—	DU_DG4	—	HCTS0#_C	—	—	—	—	—	—	—	GP5[7]	IP15[11:9]
GP-5-8	HRX0	DU_DB2	—	—	—	—	—	—	—	—	—	—	GP5[8]	IP15[13:12]
GP-5-9	HTX0	DU_DB3	—	—	—	—	—	—	—	—	—	—	GP5[9]	IP15[15:14]
GP-5-10	HCTS0#	SSI_SCK9	DU_DB4	—	—	—	—	—	—	—	—	—	GP5[10]	IP15[17:16]
GP-5-11	HRTS0#	SSI_WS9	DU_DB5	—	—	—	—	—	—	—	—	—	GP5[11]	IP15[19:18]
GP-5-12	MSIOF0_SCK	—	—	DU_DB6	—	—	—	—	—	—	—	—	GP5[12]	IP15[22:20]
GP-5-13	MSIOF0_SYNC	—	SSI_SCK2	—	DU_DB7	—	HRX0_C	—	—	—	—	—	GP5[13]	IP15[25:23]
GP-5-14	MSIOF0_SS1	—	DU_DG5	—	—	—	—	—	—	—	—	—	GP5[14]	IP15[27:26]
GP-5-15	MSIOF0_TXD	—	DU_DG6	—	—	—	—	—	—	—	—	—	GP5[15]	IP15[29:28]
GP-5-16	MSIOF0_SS2	AUDIO_CLKOUT	—	DU_DISP	—	HTX0_C	SCIFA2_TXD_B	—	—	—	—	—	GP5[16]	IP16[2:0]
GP-5-17	MSIOF0_RXD	—	SSI_WS2	—	DU_CDE	—	SCIFA2_RXD_B	—	—	—	—	—	GP5[17]	IP16[5:3]
GP-5-18	USB0_PWEN	—	—	—	—	—	—	—	—	—	—	—	GP5[18]	—
GP-5-19	USB0_OVC	—	—	—	—	—	—	—	—	—	—	—	GP5[19]	—
GP-5-20	USB1_PWEN	AUDIO_CLKOUT_D	—	—	—	—	—	—	—	—	—	—	GP5[20]	IP16[6]
GP-5-21	USB1_OVC	TCLK1_B	—	—	—	—	—	—	—	—	—	—	GP5[21]	IP16[7]
GP-5-22	USB2_PWEN	—	—	—	—	—	—	—	—	—	—	—	GP5[22]	—
GP-5-23	USB2_OVC	—	—	—	—	—	—	—	—	—	—	—	GP5[23]	—
GP-5-24	AVS1	—	—	—	—	—	—	—	—	—	—	—	GP5[24]	—
GP-5-25	AVS2	—	—	—	—	—	—	—	—	—	—	—	GP5[25]	—
GP-5-26	DU_DOTCLKIN0	—	—	—	—	—	—	—	—	—	—	—	GP5[26]	—
GP-5-27	DU_DOTCLKIN1	AUDIO_CLKC	AUDIO_CLKOUT_C	—	—	—	—	—	—	—	—	—	GP5[27]	IP7[26:25]
GP-5-28	DU_DOTCLKIN2	—	—	—	—	—	—	—	—	—	—	—	GP5[28]	—
GP-5-29	PWM0	SCIFA2_SCK_C	—	—	—	—	—	—	—	—	—	—	GP5[29]	IP7[18:16]
GP-5-30	PWM1	SCIFA2_TXD_C	—	—	—	—	—	—	—	—	—	—	GP5[30]	IP7[21:19]
GP-5-31	PWM2	—	SCIFA2_RXD_C	—	—	—	—	—	—	—	—	—	GP5[31]	IP7[24:22]

Legend: — Setting prohibited

5.3.25 Module Select Register (MOD_SEL)

Function: MOD_SEL selects the group for multiple LSI pins with multiplexed pin functions.

Each input or input/output signal of the MSIOF, LBSC, VIN, SRU, and SCIF is assigned to two or more groups of pins. Select one of these groups when using these signals. Do not use the module pins in the unselected group; if a module pin in the unselected group is used, correct operation is not guaranteed.

For some modules, however, although the output signals are assigned to two or more groups of pins, there is no bit for selecting the group. Select one of these pins for each output signal through the corresponding peripheral function select register. Also note that each pin can only be used in combination with the other input or input/output pins of the same group. Correct operation is not guaranteed when a pin is used in combination with pins from other groups. When ssi7 and ssi8 (in MOD_SEL2 register) are to be used simultaneously, the values of sel_ssi7[1:0] and sel_ssi8[1:0] must be the same so that the selected pins belong to the same group. If this is not the case, correct operation is not guaranteed.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	sel_scif1 [2]	sel_scif1 [1]	sel_scif1 [0]	sel_scifb [1]	sel_scifb [0]	sel_scifb2 [1]	sel_scifb2 [0]	sel_scifb1 [2]	sel_scifb1 [1]	sel_scifb1 [0]	sel_scifa1 [1]	sel_scifa1 [0]	sel_scif0	sel_scfa	sel_sof1	sel_ssi7 [1]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	sel_ssi7 [0]	sel_ssi6	sel_ssi5 [1]	sel_ssi5 [0]	sel_vi3	sel_vi2	sel_vi1	sel_vi0	—	—	—	sel_lbs	—	—	sel_sof3	sel_sof0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	These bits select multiplexed pin functions as indicated in the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
sel_scif1 [2:0]	SCK1 of the SSI_SCK78 pin TX1 of the SCIFA1_TXD pin RX1 of the SCIFA1_RXD pin	TX1_B of the D15 pin RX1_B of the D14 pin	TX1_C of the MLB_DAT pin RX1_C of the MLB_SIG pin	SCK1_D of the SD2_CMD pin TX1_D of the SD2_DAT1 pin RX1_D of the SD2_DAT0 pin	SCK1_E of the ETH_RXD0 pin TX1_E of the ETH_LINK pin RX1_E of the ETH_RXD1 pin	—	—
sel_scifb [1:0]	SCIFB0_SCK of the SSI_SCK34 pin SCIFB0_RXD of the SSI_WS34 pin SCIFB0_TXD of the SSI_SDATA3 pin SCIFB0_CTS# of the SSI_SCK4 pin SCIFB0_RTS# of the SSI_WS4 pin	SCIFB0_SCK_B of the SD1_CMD pin SCIFB0_RXD_B of the SD1_DAT0 pin SCIFB0_TXD_B of the SD1_DAT1 pin SCIFB0_CTS#_B of the SD1_DAT2 pin SCIFB0_RTS#_B of the SD1_DAT3 pin	SCIFB0_RXD_C of the D4 pin SCIFB0_TXD_C of the D5 pin	—	—	—	—
sel_scifb2 [1:0]	SCIFB2_SCK of the SSI_WS78 pin SCIFB2_RXD of the SSI_SDATA7 pin SCIFB2_TXD of the SSI_SDATA8 pin SCIFB2_CTS# of the SSI_SDATA9 pin SCIFB2_RTS# of the AUDIO_CLKA pin	SCIFB2_RXD_B of the A12 pin SCIFB2_TXD_B of the A14 pin SCIFB2_CTS#_B of the A11 pin SCIFB2_RTS#_B of the A13 pin SCIFB2_SCK_B of the A15 pin	SCIFB2_RXD_C of the A8 pin SCIFB2_TXD_C of the A9 pin	—	—	—	—
sel_scifb1 [2:0]	SCIFB1_SCK of the SSI_SCK5 pin SCIFB1_RXD of the SSI_WS5 pin SCIFB1_TXD of the SSI_SDATA5 pin SCIFB1_CTS# of the SSI_SCK6 pin SCIFB1_RTS# of the SSI_WS6 pin	SCIFB1_SCK_B of the SD0_CMD pin SCIFB1_RXD_B of the SD0_DAT0 pin SCIFB1_TXD_B of the SD0_DAT1 pin SCIFB1_CTS#_B of the SD0_DAT2 pin SCIFB1_RTS#_B of the SD0_DAT3 pin	SCIFB1_RXD_C of the D14 pin SCIFB1_TXD_C of the D15 pin	SCIFB1_RXD_D of the MLB_SIG pin SCIFB1_TXD_D of the MLB_DAT pin	SCIFB1_SCK_E of the SD2_CMD pin SCIFB1_RXD_E of the SD2_DAT0 pin SCIFB1_TXD_E of the SD2_DAT1 pin	SCIFB1_RXD_F of the D4 pin SCIFB1_TXD_F of the D5 pin	SCIFB1_SCK_G of the ETH_RXD0 pin SCIFB1_RXD_G of the ETH_RXD1 pin SCIFB1_TXD_G of the ETH_LINK pin

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
sel_scifa1 [1:0]	SCIFA1_SCK of the SSI_SCK78 pin SCIFA1_RXD of the SCIFA1_RXD pin SCIFA1_TXD of the SCIFA1_TXD pin SCIFA1_CTS# of the SCIFA1_CTS# pin SCIFA1_RTS# of the SCIFA1_RTS# pin	SCIFA1_SCK_B of the A7 pin SCIFA1_RXD_B of the A8 pin SCIFA1_TXD_B of the A5 pin SCIFA1_CTS#_B of the A9 pin SCIFA1_RTS#_B of the A6 pin	SCIFA1_SCK_C of the D8 pin SCIFA1_RXD_C of the D9 pin SCIFA1_TXD_C of the D10 pin SCIFA1_CTS#_C of the D11 pin SCIFA1_RTS#_C of the D12 pin	SCIFA1_SCK_D of the VI1_DATA0_VI1_B0 pin SCIFA1_RXD_D of the VI1_DATA1_VI1_B1 pin SCIFA1_TXD_D of the VI1_DATA2_VI1_B2 pin SCIFA1_CTS#_D of the VI1_DATA3_VI1_B3 pin SCIFA1_RTS#_D of the VI1_DATA4_VI1_B4 pin	—	—	—
sel_scif0	TX0 of the SCIFA0_TXD pin RX0 of the SCIFA0_RXD pin	TX0_B of the D5 pin RX0_B of the D4 pin	—	—	—	—	—
sel_scfa	SCIFA0_SCK of the SCIFA0_SCK pin SCIFA0_RXD of the SCIFA0_RXD pin SCIFA0_TXD of the SCIFA0_TXD pin SCIFA0_CTS# of the SCIFA0_CTS# pin SCIFA0_RTS# of the SCIFA0_RTS# pin	SCIFA0_SCK_B of the RD# pin SCIFA0_RXD_B of the RD_WR# pin SCIFA0_TXD_B of the WE0# pin SCIFA0_CTS#_B of the WE1# pin SCIFA0_RTS#_B of the EX_WAIT0 pin	—	—	—	—	—
sel_sof1	MSIOF1_SCK of the SSI_SCK34 pin MSIOF1_SS1 of the SSI_SDATA3 pin MSIOF1_SS2 of the SSI_SCK4 pin MSIOF1_TXD of the SSI_WS4 pin MSIOF1_RXD of the SSI_SDATA4 pin	MSIOF1_SCK_B of the EX_CS4# pin MSIOF1_SS1_B of the A2 pin MSIOF1_SS2_B of the A3 pin MSIOF1_TXD_B of the A4 pin MSIOF1_RXD_B of the EX_CS5# pin	—	—	—	—	—
sel_ssi7 [1:0]	SSI_SCK78 of the SSI_SCK78 pin SSI_WS78 of the SSI_WS78 pin SSI_SDATA7 of the SSI_SDATA7 pin	SSI_SCK78_B of the DREQ1 pin SSI_WS78_B of the DREQ0 pin SSI_SDATA7_B of the SSI_SDATA7 pin	SSI_SCK78_C of the DREQ0 pin SSI_WS78_C of the DACK0 pin SSI_SDATA7_C of the DREQ1 pin	—	—	—	—
sel_ssi6	SSI_SCK6 of the SSI_SCK6 pin SSI_WS6 of the SSI_WS6 pin SSI_SDATA6 of the SSI_SDATA6 pin	SSI_SCK6_B of the DACK0 pin SSI_WS6_B of the DACK1 pin SSI_SDATA6_B of the DACK2 pin	—	—	—	—	—
sel_ssi5 [1:0]	SSI_SCK5 of the SSI_SCK5 pin SSI_WS5 of the SSI_WS5 pin SSI_SDATA5 of the SSI_SDATA5 pin	SSI_SCK5_B of the A8 pin SSI_WS5_B of the A9 pin SSI_SDATA5_B of the A10 pin	SSI_SCK5_C of the SSI_SCK4 pin SSI_WS5_C of the SSI_WS4 pin SSI_SDATA5_C of the SSI_SDATA9 pin	—	—	—	—
sel_vi3	VI3_CLK of the EX_WAIT0 pin VI3_DATA0 of the D0 pin VI3_DATA1 of the D1 pin VI3_DATA2 of the D2 pin VI3_DATA3 of the D3 pin VI3_DATA4 of the D4 pin VI3_DATA5 of the D5 pin VI3_DATA6 of the D6 pin VI3_DATA7 of the D7 pin	VI3_CLK_B of the SD1_CD pin VI3_DATA0_B of the SD2_CLK pin VI3_DATA1_B of the SD2_CMD pin VI3_DATA2_B of the SD2_DAT0 pin VI3_DATA3_B of the SD2_DAT1 pin VI3_DATA4_B of the SD2_DAT2 pin VI3_DATA5_B of the SD2_DAT3 pin VI3_DATA6_B of the SD2_CD pin VI3_DATA7_B of the SD2_WP pin	—	—	—	—	—
sel_vi2	VI2_DATA0_VI2_B0 of the D8 pin VI2_DATA1_VI2_B1 of the D9 pin VI2_DATA2_VI2_B2 of the D10 pin VI2_DATA3_VI2_B3 of the D11 pin VI2_DATA4_VI2_B4 of the D12 pin VI2_DATA5_VI2_B5 of the D13 pin VI2_DATA6_VI2_B6 of the D14 pin VI2_DATA7_VI2_B7 of the D15 pin VI2_CLKENB of the A24 pin VI2_FIELD of the A25 pin VI2_HSYNC# of the EX_CS4# pin VI2_VSYNC# of the WE0# pin VI2_CLK of the CS1#_A26 pin	VI2_DATA0_VI2_B0_B of the A8 pin VI2_DATA1_VI2_B1_B of the A9 pin VI2_DATA2_VI2_B2_B of the A10 pin VI2_DATA3_VI2_B3_B of the A11 pin VI2_DATA4_VI2_B4_B of the A12 pin VI2_DATA5_VI2_B5_B of the A13 pin VI2_DATA6_VI2_B6_B of the SD0_CD pin VI2_DATA7_VI2_B7_B of the SD0_WP pin VI2_CLKENB_B of the A24 pin VI2_FIELD_B of the A25 pin VI2_HSYNC#_B of the EX_CS4# pin VI2_VSYNC#_B of the WE0# pin VI2_CLK_B of the CS1#_A26 pin	—	—	—	—	—

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
sel_vi1	VI1_CLKENB of the DREQ1 pin	VI1_CLKENB_B of the DREQ1 pin	—	—	—	—	—
	VI1_FIELD of the EX_CS1# pin	VI1_FIELD_B of the EX_CS1# pin					
	VI1_CLK of the VI1_CLK pin	VI1_CLK_B of the SD1_WP pin					
	VI1_HSYNC# of the DREQ0 pin	VI1_HSYNC#_B of the DREQ0 pin					
	VI1_VSYNC# of the DACK0 pin	VI1_VSYNC#_B of the DACK0 pin					
	VI1_DATA0_VI1_B0 of the	VI1_DATA0_VI1_B0_B of the SD0_CLK					
	VI1_DATA0_VI1_B0 pin	pin					
	VI1_DATA1_VI1_B1 of the	VI1_DATA1_VI1_B1_B of the					
	VI1_DATA1_VI1_B1 pin	SD0_CMD pin					
	VI1_DATA2_VI1_B2 of the	VI1_DATA2_VI1_B2_B of the					
	VI1_DATA2_VI1_B2 pin	SD0_DAT0 pin					
	VI1_DATA3_VI1_B3 of the	VI1_DATA3_VI1_B3_B of the					
	VI1_DATA3_VI1_B3 pin	SD0_DAT1 pin					
	VI1_DATA4_VI1_B4 of the	VI1_DATA4_VI1_B4_B of the					
	VI1_DATA4_VI1_B4 pin	SD0_DAT2 pin					
	VI1_DATA5_VI1_B5 of the	VI1_DATA5_VI1_B5_B of the					
	VI1_DATA5_VI1_B5 pin	SD0_DAT3 pin					
	VI1_DATA6_VI1_B6 of the	VI1_DATA6_VI1_B6_B of the SD0_CD					
	VI1_DATA6_VI1_B6 pin	pin					
	VI1_DATA7_VI1_B7 of the	VI1_DATA7_VI1_B7_B of the SD0_WP					
	VI1_DATA7_VI1_B7 pin	pin VI1_G0_B of the EX_CS2# pin					
	VI1_G0 of the EX_CS2# pin	VI1_G1_B of the EX_CS3# pin					
	VI1_G1 of the EX_CS3# pin	VI1_G2_B of the EX_CS5# pin					
	VI1_G2 of the EX_CS5# pin	VI1_G3_B of the RD_WR# pin					
	VI1_G3 of the RD_WR# pin	VI1_G4_B of the WE1# pin					
	VI1_G4 of the WE1# pin	VI1_G5_B of the EX_CS0# pin					
	VI1_G5 of the EX_CS0# pin	VI1_G6_B of the A25 pin					
	VI1_G6 of the A25 pin	VI1_G7_B of the A23 pin					
	VI1_G7 of the A23 pin	VI1_R0_B of the A11 pin					
	VI1_R0 of the A11 pin	VI1_R1_B of the A12 pin					
	VI1_R1 of the A12 pin	VI1_R2_B of the A13 pin					
	VI1_R2 of the A13 pin	VI1_R3_B of the A20 pin					
	VI1_R3 of the A20 pin	VI1_R4_B of the A21 pin					
	VI1_R4 of the A21 pin	VI1_R5_B of the A22 pin					
	VI1_R5 of the A22 pin	VI1_R6_B of the CS0# pin					
	VI1_R6 of the CS0# pin	VI1_R7_B of the A24 pin					
	VI1_R7 of the A24 pin						
sel_vi0	VI0_CLKENB of the D14 pin	VI0_CLKENB_B of the D14 pin	—	—	—	—	—
	VI0_CLK of the VI0_CLK pin	VI0_CLK_B of the SD1_CD pin					
	VI0_FIELD of the D15 pin	VI0_FIELD_B of the D15 pin					
	VI0_HSYNC# of the D12 pin	VI0_HSYNC#_B of the D12 pin					
	VI0_VSYNC# of the D13 pin	VI0_VSYNC#_B of the D13 pin					
	VI0_DATA0_VI0_B0 of the	VI0_DATA0_VI0_B0_B of the SD2_CLK					
	VI0_DATA0_VI0_B0 pin	pin					
	VI0_DATA1_VI0_B1 of the	VI0_DATA1_VI0_B1_B of the					
	VI0_DATA1_VI0_B1 pin	SD2_CMD pin					
	VI0_DATA2_VI0_B2 of the	VI0_DATA2_VI0_B2_B of the					
	VI0_DATA2_VI0_B2 pin	SD2_DAT0 pin					
	VI0_DATA3_VI0_B3 of the	VI0_DATA3_VI0_B3_B of the					
	VI0_DATA3_VI0_B3 pin	SD2_DAT1 pin					
	VI0_DATA4_VI0_B4 of the	VI0_DATA4_VI0_B4_B of the					
	VI0_DATA4_VI0_B4 pin	SD2_DAT2 pin					
	VI0_DATA5_VI0_B5 of the	VI0_DATA5_VI0_B5_B of the					
	VI0_DATA5_VI0_B5 pin	SD2_DAT3 pin					
	VI0_DATA6_VI0_B6 of the	VI0_DATA6_VI0_B6_B of the SD2_CD					
	VI0_DATA6_VI0_B6 pin	pin					
	VI0_DATA7_VI0_B7 of the	VI0_DATA7_VI0_B7_B of the SD2_WP					
	VI0_DATA7_VI0_B7 pin	pin					
	VI0_G0 of the D8 pin	VI0_G0_B of the D8 pin					
	VI0_G1 of the D9 pin	VI0_G1_B of the D9 pin					
	VI0_G2 of the D10 pin	VI0_G2_B of the D10 pin					
	VI0_G3 of the D11 pin	VI0_G3_B of the D11 pin					
	VI0_G4 of the D0 pin	VI0_G4_B of the D0 pin					
	VI0_G5 of the D1 pin	VI0_G5_B of the D1 pin					
	VI0_G6 of the D2 pin	VI0_G6_B of the D2 pin					
	VI0_G7 of the D3 pin	VI0_G7_B of the D3 pin					
	VI0_R0 of the D4 pin	VI0_R0_B of the D4 pin					
	VI0_R1 of the D5 pin	VI0_R1_B of the D5 pin					
	VI0_R2 of the D6 pin	VI0_R2_B of the D6 pin					
	VI0_R3 of the D7 pin	VI0_R3_B of the D7 pin					
	VI0_R4 of the A8 pin	VI0_R4_B of the A8 pin					
	VI0_R5 of the A9 pin	VI0_R5_B of the A9 pin					
	VI0_R6 of the A10 pin	VI0_R6_B of the A10 pin					
	VI0_R7 of the CS1#_A26 pin	VI0_R7_B of the CS1#_A26 pin					

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
sel_lbs	EX_WAIT0 of the EX_WAIT0 pin	EX_WAIT0_B of the A19 pin	—	—	—	—	—
sel_sof3	MSIOF3_SCK of the SCIFA2_SCK pin MSIOF3_SYNC of the SCIFA0_CTS# pin MSIOF3_TXD of the SCIFA1_RTS# pin MSIOF3_RXD of the SCIFA1_CTS# pin	MSIOF3_SCK_B of the D0 pin MSIOF3_SYNC_B of the D1 pin MSIOF3_TXD_B of the D3 pin MSIOF3_RXD_B of the D2 pin	—	—	—	—	—
sel_sof0	MSIOF0_SCK of the MSIOF0_SCK pin MSIOF0_SS1 of the MSIOF0_SS1 pin MSIOF0_SS2 of the MSIOF0_SS2 pin MSIOF0_TXD of the MSIOF0_TXD pin MSIOF0_RXD of the MSIOF0_RXD pin	MSIOF0_SCK_B of the EX_WAIT0 pin MSIOF0_SS1_B of the EX_CS0# pin MSIOF0_SS2_B of the CS0# pin MSIOF0_TXD_B of the DREQ2 pin MSIOF0_RXD_B of the DACK2 pin	—	—	—	—	—

Legend: – Setting prohibited

5.3.26 Module Select Register 2 (MOD_SEL2)

Function: MOD_SEL2 selects the group for multiple LSI pins with multiplexed pin functions.

Each input or input/output signal of the SRU, HSCIF, ADCIF, RCAN, SCIF, and TMU is assigned to two or more groups of pins. Select one of these groups when using these signals. Do not use the module pins in the unselected group; if a module pin in the unselected group is used, correct operation is not guaranteed.

For some modules, however, although the output signals are assigned to two or more groups of pins, there is no bit for selecting the group. Select one of these pins for each output signal through the corresponding peripheral function select register. Also note that each pin can only be used in combination with the other input or input/output pins of the same group. When ssi8 and ssi7 (in MOD_SEL register) are to be used simultaneously, the values of sel_ssi8[1:0] and sel_ssi7[1:0] must be the same so that the selected pins belong to the same group. Correct operation is not guaranteed when a pin is used in combination with pins from other groups.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	sel_tmu1	sel_hscif1	sel_scifclk	sel_can0[1]	sel_can0[0]	sel_canclk	sel_scifa2[1]	sel_scifa2[0]	sel_can1	—	—	sel_scif2	sel_adi
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	sel_hscif0[2]	sel_hscif0[1]	sel_hscif0[0]	—	—	—	—	—	—	—	sel_ssi8[1]	sel_ssi8[0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	These bits select multiplexed pin functions as indicated in the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
sel_tmu1	TCLK1 of the D7 pin	TCLK1_B of the USB1_OVC pin	—	—	—	—	—
sel_hscif1	HSCK1 of the SCIFA0_SCK pin HCTS1# of the SCIFA0_CTS# pin HRTS1# of the SCIFA0_RTS# pin HTX1 of the SCIFA0_TXD pin HRX1 of the SCIFA0_RXD pin	HSCK1_B of the DREQ2 pin HCTS1#_B of the EX_CS1# pin HRTS1#_B of the EX_CS2# pin HTX1_B of the BS# pin HRX1_B of the EX_CS0# pin	—	—	—	—	—
sel_scifclk	SCIF_CLK of the AUDIO_CLKB pin	SCIF_CLK_B of the SCIFA2_SCK pin	—	—	—	—	—
sel_can0 [1:0]	CAN0_TX of the RD# pin CAN0_RX of the EX_CS5# pin	CAN0_TX_B of the SSI_WS0129 pin CAN0_RX_B of the SSI_SDATA0 pin	CAN0_TX_C of the SSI_SDATA8 pin CAN0_RX_C of the AUDIO_CLKB pin	CAN0_TX_D of the SSI_WS6 pin CAN0_RX_D of the AUDIO_CLKB pin	—	—	—
sel_canclk	CAN_CLK of the WE0# pin	CAN_CLK_B of the SSI_SCK0129 pin	—	—	—	—	—
sel_scifa2 [1:0]	SCIFA2_SCK of the SCIFA2_SCK pin SCIFA2_RXD of the SCIFA2_RXD pin SCIFA2_TXD of the SCIFA2_TXD pin	HRX0_C of the MSIOF0_SYNC pin SCIFA2_TXD_B of the MSIOF0_SS2 pin	SCIFA2_SCK_C of the PWM0 pin SCIFA2_RXD_C of the PWM2 pin SCIFA2_TXD_C of the PWM1 pin	—	—	—	—

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
sel_can1	CAN1_TX of the BS# pin CAN1_RX of the WE1# pin	CAN1_TX_B of the SSI_SDATA1 pin CAN1_RX_B of the SSI_SDATA2 pin	—	—	—	—	—
sel_scif2	TX2 of the SCIFA2_RXD pin RX2 of the SCIFA2_TXD pin	TX2_B of the A9 pinRX2_B of the A8 pin	—	—	—	—	—
sel_hscif0 [2:0]	HRX0 of the HRX0 pin HTX0 of the HTX0 pin HCTS0# of the HCTS0# pin HRTS0# of the HRTS0# pin	HRX0_B of the EX_WAIT0 pin HTX0_B of the EX_CS0# pin HCTS0#_B of the DREQ2 pin HRTS0#_B of the DACK2 pin	SCIFA2_RXD_B of the MSIOF0_RXD pin HTX0_C of the MSIOF0_SS2 pin HCTS0#_C of the HSCK0 pin HRTS0#_C of the SCIFA1_RTS# pin	HRX0_D of the SD2_DAT2 pin HTX0_D of the SD2_DAT3 pin HCTS0#_D of the SD2_CD pin HRTS0#_D of the SD2_WP pin	HRX0_E of the ETH_RXD1 pin HTX0_E of the ETH_LINK pin HCTS0#_E of the ETH_REF_CLK pin HRTS0#_E of the ETH_MDIO pin	HRX0_F of the ETH_REF_CLK pin HTX0_F of the ETH_TXD1 pin HCTS0#_F of the ETH_MDIO pin HRTS0#_F of the ETH_TX_EN pin	—
sel_ssi8 [1:0]	SSI_SDATA8 of the SSI_SDATA8 pin	SSI_SDATA8_B of the SSI_SDATA8 pin	SSI_SDATA8_C of the DACK1 pin	—	—	—	—

Legend: – Setting prohibited

5.3.27 Module Select Register 3 (MOD_SEL3)

Function: MOD_SEL3 selects the group for multiple LSI pins with multiplexed pin functions.

Each input or input/output signal of the IIC3 (DVFS), and TMU is assigned to two or more groups of pins. Select one of these groups when using these signals. Do not use the module pins in the unselected group; if a module pin in the unselected group is used, correct operation is not guaranteed.

For some modules, however, although the output signals are assigned to two or more groups of pins, there is no bit for selecting the group. Select one of these pins for each output signal through the corresponding peripheral function select register. Also note that each pin can only be used in combination with the other input or input/output pins of the same group.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	sel_iic3	sel_iic0	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	sel_iic2_[2]	sel_iic2_[1]	sel_iic2_[0]	sel_iic1_[1]	sel_iic1_[0]	sel_i2c2_[2]	sel_i2c2_[1]	sel_i2c2_[0]	sel_i2c1_[1]	sel_i2c1_[0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	These bits select multiplexed pin functions as indicated in the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
sel_iic3 (dvfs)	IIC3_SCL of IIC3 (DVFS) of the IIC3_SCL pin IIC3_SDA of IIC3 (DVFS) of the IIC3_SDA pin	I2C3_SCL of I2C3 of the IIC3_SCL pin I2C3_SDA of I2C3 of the IIC3_SDA pin	—	—	—	—	—
sel_iic0	IIC0_SCLof the IIC0_SCLpin IIC0_SDAof the IIC0_SDApin	I2C0_SCLof the IIC0_SCLpin I2C0_SDAof the IIC0_SDApin	—	—	—	—	—
sel_iic2[2:0]	IIC2_SCL of the SCIFA2_RXD pin IIC2_SDA of the SCIFA2_TXD pin	IIC2_SCL_B of the MLB_CLK pin IIC2_SDA_B of the MLB_SIG pin	IIC2_SCL_C of the D6 pin IIC2_SDA_C of the D7 pin	IIC2_SCL_D of the SD1_CD pin IIC2_SDA_D of the SD1_WP pin	IIC2_SCL_E of the ETH_CRS_DV pin IIC2_SDA_E of the ETH_RX_ER pin	—	—
sel_iic1[1:0]	IIC1_SCL of the EX_CS4# pin IIC1_SDA of the EX_CS5# pin	IIC1_SCL_B of the SD0_CD pin IIC1_SDA_B of the SD0_WP pin	IIC1_SCL_C of the SCIFA0_CTS# pin IIC1_SDA_C of the SCIFA0_SCK pin	—	—	—	—
sel_i2c2[2:0]	I2C2_SCL of the SCIFA2_RXD pin I2C2_SDA of the SCIFA2_TXD pin	I2C2_SCL_B of the MLB_CLK pin I2C2_SDA_B of the MLB_SIG pin	I2C2_SCL_C of the D6 pin I2C2_SDA_C of the D7 pin	I2C2_SCL_D of the SD1_CD pin I2C2_SDA_D of the SD1_WP pin	I2C2_SCL_E of the ETH_CRS_DV pin I2C2_SDA_E of the ETH_RX_ER pin	—	—
sel_i2c1[1:0]	I2C1_SCL of the EX_CS4# pin I2C1_SDA of the EX_CS5# pin	I2C1_SCL_B of the SD0_CD pin I2C1_SDA_B of the SD0_WP pin	I2C1_SCL_C of the SCIFA0_CTS# pin I2C1_SDA_C of the SCIFA0_SCK pin	—	—	—	—

Legend: – Setting prohibited

5.3.28 LSI Pin Pull-Up Control Register 0 (PUPR0)

Function: PUPR0 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EX_CS5#	EX_CS4#	EX_CS3#	EX_CS2#	EX_CS1#	EX_CS0#	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	H'FFF0 3F00	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

5.3.29 LSI Pin Pull-Up Control Register 1 (PUPR1)

Function: PUPR1 performs on/off control of the pull-up/down resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	ACK	—	TDI	TMS	TCK	TRST#	CS1#_A26	CS0#	AVS2	AVS1	EX_WAIT0	WE1#	WE0#	RD_WR#	RD#	BS#
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0	0	1	1	1	1	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0 (except for 15)	—	H'FFFF BF3C	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.
15	ACK			Performs on/off control of the pull-down resistor provided in the ACK pin of the LSI. 0: Pull-down function is disabled. 1: Pull-down function is enabled (default).

5.3.30 LSI Pin Pull-Up Control Register 2 (PUPR2)

Function: PUPR2 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DU_DOTCLKIN0	—	MLB_DAT	MLB_SIG	MLB_CLK	—	—	—	DU_DOTCLKIN1	VI1_DATA7_VI1_B7	VI1_DATA6_VI1_B6	VI1_DATA5_VI1_B5	VI1_DATA4_VI1_B4	VI1_DATA3_VI1_B3	VI1_DATA2_VI1_B2	VI1_DATA1_VI1_B1	VI1_DATA0_VI1_B0	VI1_CLK	VI0_DATA7_VI0_B7	VI0_DATA6_VI0_B6	VI0_DATA5_VI0_B5	VI0_DATA4_VI0_B4	VI0_DATA3_VI0_B3	VI0_DATA2_VI0_B2	VI0_DATA1_VI0_B1	VI0_DATA0_VI0_B0	VI0_CLK	—	—	—	—	DU_DOTCLKIN2
Initial value:	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	H'80FF FFE1	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

5.3.31 LSI Pin Pull-Up Control Register 3 (PUPR3)

Function: PUPR3 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SD3_WP	SD3_CD	SD3_DAT3	SD3_DAT2	SD3_DAT1	SD3_DAT0	SD3_CMD	SD3_CLK	SD2_WP	SD2_CD	SD2_DAT3	SD2_DAT2	SD2_DAT1	SD2_DAT0	SD2_CMD	SD2_CLK	SD1_WP	SD1_CD	SD1_DAT3	SD1_DAT2	SD1_DAT1	SD1_DAT0	SD1_CMD	SD1_CLK	SD0_WP	SD0_CD	SD0_DAT3	SD0_DAT2	SD0_DAT1	SD0_DAT0	SD0_CMD	SD0_CLK
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	H'0000 0000	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

5.3.32 LSI Pin Pull-Up Control Register 4 (PUPR4)

Function: PUPR4 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ETH_RX_ER	ETH_CRS_DV	DACK2	DREQ2	DACK1	DREQ1	DACK0	DREQ0	AUDIO_CLKB	AUDIO_CLKA	SSI_SDATA9	SSI_SDATA8	SSI_SDATA7	SSI_WS78	SSI_SCK78	SSI_SDATA6	SSI_WS6	SSI_SCK6	SSI_SDATA5	SSI_WS5	SSI_SCK5	SSI_SDATA4	SSI_WS4	SSI_SCK4	SSI_SDATA3	SSI_WS34	SSI_SCK34	SSI_SDATA2	SSI_SDATA1	SSI_SDATA0	SSI_WS0129	SSI_SCK0129
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	H'FFFF FFFF	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

5.3.33 LSI Pin Pull-Up Control Register 5 (PUPR5)

Function: PUPR5 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ETH_LINK	ETH_RXD1	ETH_RXD0	USB2_OVC	USB2_PWEN	USB1_OVC	USB1_PWEN	USB0_OVC_VBUS	USB0_PWEN	MSIOF0_RXD	MSIOF0_SS2	MSIOF0_TXD	MSIOF0_SS1	MSIOF0_SYNC	MSIOF0_SCK	HRTS0#	HCTS0#	HTX0	HRX0	HSCK0	SCIFA2_TXD	SCIFA2_RXD	SCIFA2_SCK	SCIFA1_RTS#	SCIFA1_CTS#	SCIFA1_TXD	SCIFA1_RXD	SCIFA0_RTS#	SCIFA0_CTS#	SCIFA0_TXD	SCIFA0_RXD	SCIFA0_SCK
Initial value:	1	1	1	0	0	0	0	0	0	1	0	0	0	1	1	1	1	0	1	1	1	1	1	0	1	0	1	0	1	0	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	H'E047 BEAB	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

5.3.34 LSI Pin Pull-Up Control Register 6 (PUPR6)

Function: PUPR6 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM2	PWM1	PWM0	ETH_MDC	ETH_TXD0	ETH_MAGIC	ETH_TX_EN	ETH_TXD1	ET_MDIO	ETH_REF_CLK
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	H'0000 0203	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

5.3.35 IIC3 (DVFS)/MMC IO Cell Control Register (IOCTRL)

Function: IOCTRL controls the driving abilities of pins in use for the IIC3 (DVFS) and MMC interfaces.

This register is internal use and reserved; the value of this register should not be changed.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	gpreg_msel03_p	gpreg_msel07_p	gpreg_msel07_p	gpreg_msel07_p	gpreg_msel07_p	conta_iic3 (dvfs)	contb_iic3 (dvfs)	—	—	conta_iic0	contb_iic0	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R/W	—
12	gpreg_msel03_p	0	R/W	Debug monitor function Setting 0: Use MSIOF, HSCIF and SCIFA pins for debug monitor function. 1: Use SDHI pins for debug monitor function.
11	gpreg_msel07_p	0	R/W	Reserved
10	gpreg_msel07_p	0	R/W	Reserved
9	gpreg_msel07_p	0	R/W	Reserved
8	gpreg_msel07_p	0	R/W	Reserved
7	conta_iic3 (dvfs)	0	R/W	Control TOF*1 value of IIC3 (DVFS) IO cell 0: 0.3VPU 1: 0.7VPU
6	contb_iic3 (dvfs)	0	R/W	Control VIH/VIL*2 value of IIC3 (DVFS) IO cell 0: VIL 1: VIH
5	—	0	R/W	—
4	—	0	R/W	—
3	conta_iic0	0	R/W	Control TOF*1 value of IIC0 IO cell 0: 0.3VPU 1: 0.7VPU
2	contb_iic0	0	R/W	Control VIH/VIL*2 value of IIC0 IO cell 0: VIL 1: VIH
1	—	0	R/W	—
0	—	0	R/W	—

Notes: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

*1 Output fall time from VIH min to VIL max or from 0.7VPU to 0.3VPU

*2 VIH and VIL respectively indicate high-level input voltage and low-level input voltage.

5.3.36 SD Control Register 0 (IOCTRL0)

Function: IOCTRL0 controls the driving abilities of pins in use for the SD0 and SD3 interfaces.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	drv2_sd3wp	drv1_sd3wp	drv2_sd3cd	drv1_sd3cd	drv2_sd3clk	drv1_sd3clk	drv2_sd3cmd	drv1_sd3cmd	drv2_sd3d3	drv1_sd3d3	drv2_sd3d2	drv1_sd3d2	drv2_sd3d1	drv1_sd3d1	drv2_sd3d0	drv1_sd3d0	drv2_sd0wp	drv1_sd0wp	drv2_sd0cd	drv1_sd0cd	drv2_sd0clk	drv1_sd0clk	drv2_sd0cmd	drv1_sd0cmd	drv2_sd0d3	drv1_sd0d3	drv2_sd0d2	drv1_sd0d2	drv2_sd0d1	drv1_sd0d1	drv2_sd0d0	drv1_sd0d0
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	drv2_sd3wp	1	R/W	SD3_WP Setting:
30	drv1_sd3wp	1	R/W	The value of these bits must be 11.
29	drv2_sd3cd	1	R/W	SD3_CD Setting:
28	drv1_sd3cd	1	R/W	The value of these bits must be 11.
27	drv2_sd3clk	1	R/W	SD3_CLK Setting 1:
26	drv1_sd3clk	1	R/W	The value of these bits must be 11.
25	drv2_sd3cmd	1	R/W	SD3_CMD Setting:
24	drv1_sd3cmd	1	R/W	The value of these bits must be 11.
23	drv2_sd3d3	1	R/W	SD3_DAT3 Setting:
22	drv1_sd3d3	1	R/W	The value of these bits must be 11.
21	drv2_sd3d2	1	R/W	SD3_DAT2 Setting:
20	drv1_sd3d2	1	R/W	The value of these bits must be 11.
19	drv2_sd3d1	1	R/W	SD3_DAT1 Setting:
18	drv1_sd3d1	1	R/W	The value of these bits must be 11.
17	drv2_sd3d0	1	R/W	SD3_DAT0 Setting:
16	drv1_sd3d0	1	R/W	The value of these bits must be 11.
15	drv2_sd0wp	1	R/W	SD0_WP Setting:
14	drv1_sd0wp	1	R/W	The value of these bits must be 11.
13	drv2_sd0cd	1	R/W	SD0_CD Setting:
12	drv1_sd0cd	1	R/W	The value of these bits must be 11.
11	drv2_sd0clk	1	R/W	SD0_CLK Setting 1:
10	drv1_sd0clk	1	R/W	The value of these bits must be 11.
9	drv2_sd0cmd	1	R/W	SD0_CMD Setting:
8	drv1_sd0cmd	1	R/W	The value of these bits must be 11.
7	drv2_sd0d3	1	R/W	SD0_DAT3 Setting:
6	drv1_sd0d3	1	R/W	The value of these bits must be 11.
5	drv2_sd0d2	1	R/W	SD0_DAT2 Setting:
4	drv1_sd0d2	1	R/W	The value of these bits must be 11.
3	drv2_sd0d1	1	R/W	SD0_DAT1 Setting:
2	drv1_sd0d1	1	R/W	The value of these bits must be 11.

Bit	Bit Name	Initial Value	R/W	Description
1	drv2_sd0d0	1	R/W	SD0_DAT0 Setting:
0	drv1_sd0d0	1	R/W	The value of these bits must be 11.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

For two-bit fields, "specify a value of 10" and similar expressions mean setting the higher-order bit (drv2_xx) to 1 and the lower-order bit (drv1_xx) to 0, respectively.

5.3.37 SD Control Register 1 (IOCTRL1)

Function: IOCTRL1 controls the driving abilities of pins in use for the SD1 and SD2 interfaces.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	drv2_sd2wp	drv1_sd2wp	drv2_sd2cd	drv1_sd2cd	drv2_sd2clk	drv1_sd2clk	drv2_sd2cmd	drv1_sd2cmd	drv2_sd2d3	drv1_sd2d3	drv2_sd2d2	drv1_sd2d2	drv2_sd2d1	drv1_sd2d1	drv2_sd2d0	drv1_sd2d0	drv2_sd1wp	drv1_sd1wp	drv2_sd1cd	drv1_sd1cd	drv2_sd1clk	drv1_sd1clk	drv2_sd1cmd	drv1_sd1cmd	drv2_sd1d3	drv1_sd1d3	drv2_sd1d2	drv1_sd1d2	drv2_sd1d1	drv1_sd1d1	drv2_sd1d0	drv1_sd1d0
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	drv2_sd2wp	1	R/W	SD2_WP Setting.
30	drv1_sd2wp	1	R/W	The value of these bits must be 11.
29	drv2_sd2cd	1	R/W	SD2_CD Setting.
28	drv1_sd2cd	1	R/W	The value of these bits must be 11.
27	drv2_sd2clk	1	R/W	SD2_CLK Setting.
26	drv1_sd2clk	1	R/W	The value of these bits must be 11.
25	drv2_sd2cmd	1	R/W	SD2_CMD Setting.
24	drv1_sd2cmd	1	R/W	The value of these bits must be 11.
23	drv2_sd2d3	1	R/W	SD2_DAT3 Setting.
22	drv1_sd2d3	1	R/W	The value of these bits must be 11.
21	drv2_sd2d2	1	R/W	SD2_DAT2 Setting.
20	drv1_sd2d2	1	R/W	The value of these bits must be 11.
19	drv2_sd2d1	1	R/W	SD2_DAT1 Setting.
18	drv1_sd2d1	1	R/W	The value of these bits must be 11.
17	drv2_sd2d0	1	R/W	SD2_DAT0 Setting.
16	drv1_sd2d0	1	R/W	The value of these bits must be 11.
15	drv2_sd1wp	1	R/W	SD1_WP Setting.
14	drv1_sd1wp	1	R/W	The value of these bits must be 11.
13	drv2_sd1cd	1	R/W	SD1_CD Setting.
12	drv1_sd1cd	1	R/W	The value of these bits must be 11.
11	drv2_sd1clk	1	R/W	SD1_CLK Setting.
10	drv1_sd1clk	1	R/W	The value of these bits must be 11.
9	drv2_sd1cmd	1	R/W	SD1_CMD Setting.
8	drv1_sd1cmd	1	R/W	The value of these bits must be 11.
7	drv2_sd1d3	1	R/W	SD1_DAT3 Setting.
6	drv1_sd1d3	1	R/W	The value of these bits must be 11.
5	drv2_sd1d2	1	R/W	SD1_DAT2 Setting.
4	drv1_sd1d2	1	R/W	The value of these bits must be 11.
3	drv2_sd1d1	1	R/W	SD1_DAT1 Setting.
2	drv1_sd1d1	1	R/W	The value of these bits must be 11.

Bit	Bit Name	Initial Value	R/W	Description
1	drv2_sd1d0	1	R/W	SD1_DAT0 Setting.
0	drv1_sd1d0	1	R/W	The value of these bits must be 11.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.
For two-bit fields, "specify a value of 10" and similar expressions mean setting the higher-order bit (drv2_xx) to 1 and the lower-order bit (drv1_xx) to 0, respectively.

5.3.38 VI1 Driving Ability Control Register (IOCTRL4)

Function: IOCTRL4 controls the driving abilities of pin in use for the VIN1 interface.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																							drv2_vi1datb3	drv1_vi1datb3								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R/W	—
9	drv2_vi1datb3	1	R/W	VI1_DATA3_VI1_B3 Setting:
8	drv1_vi1datb3	0	R/W	The value of these bits must be 10.
7 to 0	—	All 0	R/W	—

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.
For two-bit fields, "specify a value of 10" and similar expressions mean setting the higher-order bit (drv2_xx) to 1 and the lower-order bit (drv1_xx) to 0, respectively.

5.3.39 TDSEL Control Register (IOCTRL5)

Function: IOCTRL5 controls the internal-chip clock delay to be used for data reception. This register is internal use and reserved; the value of this register should not be changed.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	sd0tdsel1	sd0tdsel0	sd1tdsel1	sd1tdsel0	sd2tdsel1	sd2tdsel0	sd3tdsel1	sd3tdsel0	d0_tdsel1	d0_tdsel0	a11_tdsel1	a11_tdsel0	excs4_tdsel1	excs4_tdsel0	exwait0_tdsel1	exwait0_tdsel0	ssi_tdsel1	ssi_tdsel0	scifa2_tdsel1	scifa2_tdsel0	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R/W	—
21	sd0tdsel1	0	R/W	SD0_CLK Setting 2: The setting value of these bits must be 00.
20	sd0tdsel0	0	R/W	
19	sd1tdsel1	0	R/W	SD1_CLK Setting 2: The setting value of these bits must be 00.
18	sd1tdsel0	0	R/W	
17	sd2tdsel1	0	R/W	SD2_CLK Setting 2: The setting value of these bits must be 00.
16	sd2tdsel0	0	R/W	
15	sd3tdsel1	0	R/W	SD1_CLK Setting 2: The setting value of these bits must be 00.
14	sd3tdsel0	0	R/W	
13	d0_tdsel1	0	R/W	D0 Setting: The setting value of these bits must be 00.
12	d0_tdsel0	0	R/W	
11	a11_tdsel1	0	R/W	A11 Setting: The setting value of these bits must be 00.
10	a11_tdsel0	0	R/W	
9	excs4_tdsel1	0	R/W	EX_CS4# Setting: The setting value of these bits must be 00.
8	excs4_tdsel0	0	R/W	
7	exwait0_tdsel1	0	R/W	EX_WAIT0 Setting: The setting value of these bits must be 00.
6	exwait0_tdsel0	0	R/W	
5	ssi_tdsel1	0	R/W	SSI_SCK34 Setting: The setting value of these bits must be 00.
4	ssi_tdsel0	0	R/W	
3	scifa2_tdsel1	0	R/W	SCIFA2_SCK Setting: The setting value of these bits must be 00.
2	scifa2_tdsel0	0	R/W	
1, 0	—	All 0	R/W	—

Note: For two-bit fields, "specify a value of 10" and similar expressions mean setting the higher-order bit (xx_tdsel1) to 1 and the lower-order bit (xx_tdsel0) to 0, respectively.

5.3.40 POC Control Register (IOCTRL6)

Function: IOCTRL6 controls the IO voltage of pins in use for the SD interfaces.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	poc_sd0clk	poc_sd0cmd	poc_sd0dat0	poc_sd0dat1	poc_sd0dat2	poc_sd0dat3	poc_sd0cd	poc_sd0wp	poc_sd1clk	poc_sd1cmd	poc_sd1dat0	poc_sd1dat1	poc_sd1dat2	poc_sd1dat3	poc_sd1cd	poc_sd1wp	poc_sd2clk	poc_sd2cmd	poc_sd2dat0	poc_sd2dat1	poc_sd2dat2	poc_sd2dat3	poc_sd2cd	poc_sd2wp	poc_sd3clk	poc_sd3cmd	poc_sd3dat0	poc_sd3dat1	poc_sd3dat2	poc_sd3dat3	poc_sd3cd	poc_sd3wp
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	poc_sd0clk	H'FF	R/W	Selecting IO voltage for the SD0 H'00: 1.8 V (VCCQ_SD0 = 1.8 V) H'FF: 3.3 V (VCCQ_SD0 = 3.3 V) Other than above: Setting prohibited Note: H'00 can only be set for the SDHI SDR50/SDR104 mode and the GPIO multiplexed with the SDHI that can be used either 3.3 V or 1.8 V.
30	poc_sd0cmd			
29	poc_sd0dat0			
28	poc_sd0dat1			
27	poc_sd0dat2			
26	poc_sd0dat3			
25	poc_sd0cd			
24	poc_sd0wp			
23	poc_sd1clk	H'FF	R/W	Selecting IO voltage for the SD1 H'00: 1.8 V (VCCQ_SD1 = 1.8 V) H'FF: 3.3 V (VCCQ_SD1 = 3.3 V) Other than above: Setting prohibited Note: H'00 can only be set for the SDHI SDR50/SDR104 mode and the GPIO multiplexed with the SDHI that can be used either 3.3 V or 1.8 V.
22	poc_sd1cmd			
21	poc_sd1dat0			
20	poc_sd1dat1			
19	poc_sd1dat2			
18	poc_sd1dat3			
17	poc_sd1cd			
16	poc_sd1wp			
15	poc_sd2clk	H'FF	R/W	Selecting IO voltage for the SD2 H'00: 1.8 V (VCCQ_SD2 = 1.8 V) H'FF: 3.3 V (VCCQ_SD2 = 3.3 V) Other than above: Setting prohibited Note: H'00 can only be set for the SDHI SDR50/SDR104 mode and the GPIO multiplexed with the SDHI that can be used either 3.3 V or 1.8 V.
14	poc_sd2cmd			
13	poc_sd2dat0			
12	poc_sd2dat1			
11	poc_sd2dat2			
10	poc_sd2dat3			
9	poc_sd2cd			
8	poc_sd2wp			
7	poc_sd3clk	H'FF	R/W	Selecting IO voltage for the SD3 H'00: 1.8 V (VCCQ_SD3 = 1.8 V) H'FF: 3.3 V (VCCQ_SD3 = 3.3 V) Other than above: Setting prohibited Note: H'00 can only be set for the SDHI SDR50/SDR104 mode and the GPIO multiplexed with the SDHI that can be used either 3.3 V or 1.8 V.
6	poc_sd3cmd			
5	poc_sd3dat0			
4	poc_sd3dat1			
3	poc_sd3dat2			
2	poc_sd3dat3			
1	poc_sd3cd			
0	poc_sd3wp			

Notes: 1. Any pin belongs to the same SD channel must be set to the same IO voltage as VCCQ_SDn. Even though setting different voltage for each pin of the same SD channel, it is impossible to change each pin voltage from the power supply voltage of the VCCQ_SDn.

2. When the VCCQ_SDn power supply voltage is 1.8-V to use the SDHI interface as SDR50/SDR104 mode or the GPIO (multiplexed with SDHI channel n pin) as 1.8-V IO, specify 1.8-V for IOCTRL6, then IO voltage of the SDHI channel n pins and multiplexed other function pins is all 1.8-V. In this condition, never input 3.3-V signal to these pins; if input 3.3-V signal, the LSI may be permanently damaged even though specifying the pin voltage to 3.3-V individually, furthermore, pull-up voltage of the unused pin which belongs to the same SD channel must be 1.8-V.

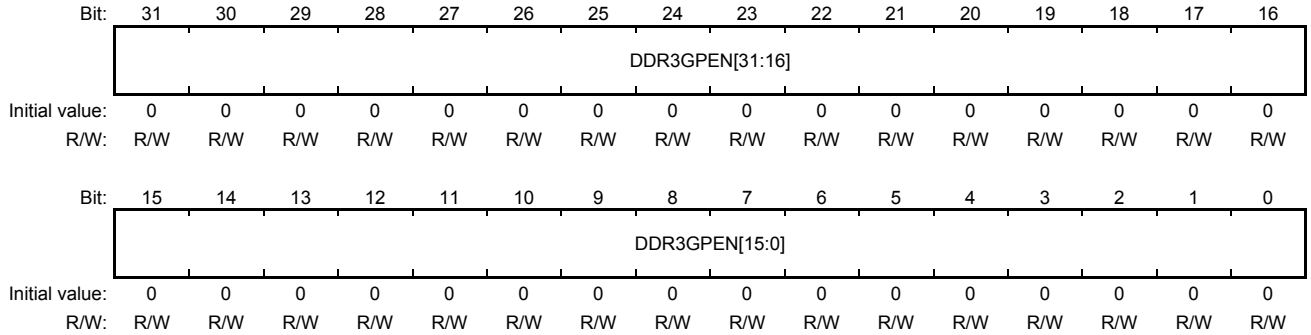
3. When the VCCQ_SDn power supply voltage is 3.3-V, to use the SDHI inter face as default mode, high-speed mode or other module function, specify 3.3-V for IOCTRL6, then IO voltage of the SDHI channel n and multiplexed other function pins is all 3.3-V. In this condition, output level of the pin is 3.3-V and if the external device can only operate with1.8-V, the external device may be permanently damaged even though specifying the pin voltage to 1.8-V individually.

4. For details of SDn related pin function settings, refer to following section.
Section 5.3.5 GPSR 3, 5.3.16 IPSR 8 through 5.3.19 IPSR11, 5.3.25 MOD_SEL, 5.3.26, MOD_SEL2, 5.3.27 MOD_SEL3.

5. Some of the following module pins are multiplexed with the SDn pins. They cannot be used with 1.8-V power supply (VCCQ_SDn) except for the multiplexed GPIO. Use them with 3.3-V power supply and specify supply voltage as 3.3-V by IOCTRL6.
MMC1, MMC0, EtherAVB, SCIFB1(B, E), SCIFB0(B), VIN3(B), VIN2(B), VIN1(B), VIN0(B), I2C1(B), I2C2(D), IIC1(B), IIC2(D), HSCIF0(D), SCIF1(D).
For details of multiplexed pins of SDn, refer to Table 4.1, List of Multiplexed Pin Functions in section 4, Pin Multiplexing.

5.3.41 DDR3 General Port IO Enable Register (DDR3GPEN)

Function: DDR3GPEN is used to write values to enable DDR3 general port function.

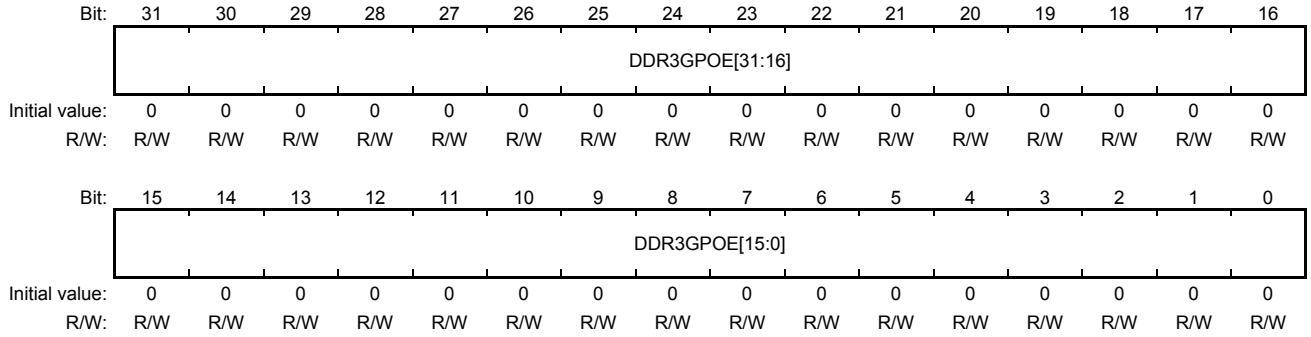


Bit	Bit Name	Initial Value	R/W	Description
31, 30	DDR3GPEN[31:30]	00	R/W	—
29 to 1	DDR3GPEN[29:1]	All 0	R/W	For enabling DDR3 general port function bit 29 to 1: 0: Disabled. 1: Enabled.
0	DDR3GPEN[0]	0	R/W	—

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.42 DDR3 General Port Output Enable Register (DDR3GPOE)

Function: DDR3GPOE is use to enable output of DDR3 general port function.



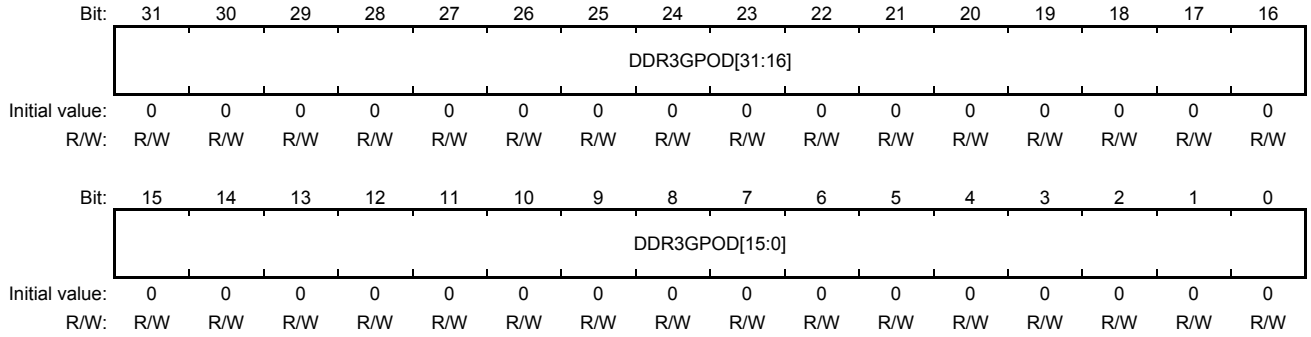
Bit	Bit Name	Initial Value	R/W	Description
31	DDR3GPOE[31]	0	R/W	—
30	DDR3GPOE[30]	0	R/W	—
29	DDR3GPOE[29]	0	R/W	Enabling output of DDR3 general port function bit 29 0: Disabled. 1: Enabled.
28	DDR3GPOE[28]	0	R/W	—
27	DDR3GPOE[27]	0	R/W	—
26	DDR3GPOE[26]	0	R/W	Enabling output of DDR3 general port function bit 26 0: Disabled. 1: Enabled.
25	DDR3GPOE[25]	0	R/W	—
24	DDR3GPOE[24]	0	R/W	Enabling output of DDR3 general port function bit 24 0: Disabled. 1: Enabled.
23	DDR3GPOE[23]	0	R/W	—
22	DDR3GPOE[22]	0	R/W	—
21	DDR3GPOE[21]	0	R/W	Enabling output of DDR3 general port function bit 21 0: Disabled. 1: Enabled.
20	DDR3GPOE[20]	0	R/W	Enabling output of DDR3 general port function bit 20 0: Disabled. 1: Enabled.
19	DDR3GPOE[19]	0	R/W	Enabling output of DDR3 general port function bit 19 0: Disabled. 1: Enabled.
18	DDR3GPOE[18]	0	R/W	—
17	DDR3GPOE[17]	0	R/W	Enabling output of DDR3 general port function bit 17 0: Disabled. 1: Enabled.

Bit	Bit Name	Initial Value	R/W	Description
16	DDR3GPOE[16]	0	R/W	Enabling output of DDR3 general port function bit 16 0: Disabled. 1: Enabled.
15	DDR3GPOE[15]	0	R/W	Enabling output of DDR3 general port function bit 15 0: Disabled. 1: Enabled.
14	DDR3GPOE[14]	0	R/W	—
13	DDR3GPOE[13]	0	R/W	—
12	DDR3GPOE[12]	0	R/W	Enabling output of DDR3 general port function bit 12 0: Disabled. 1: Enabled.
11	DDR3GPOE[11]	0	R/W	Enabling output of DDR3 general port function bit 11 0: Disabled. 1: Enabled.
10	DDR3GPOE[10]	0	R/W	—
9	DDR3GPOE[9]	0	R/W	Enabling output of DDR3 general port function bit 9 0: Disabled. 1: Enabled.
8	DDR3GPOE[8]	0	R/W	—
7	DDR3GPOE[7]	0	R/W	Enabling output of DDR3 general port function bit 7 0: Disabled. 1: Enabled.
6	DDR3GPOE[6]	0	R/W	—
5	DDR3GPOE[5]	0	R/W	—
4	DDR3GPOE[4]	0	R/W	—
3	DDR3GPOE[3]	0	R/W	Enabling output of DDR3 general port function bit 3 0: Disabled. 1: Enabled.
2	DDR3GPOE[2]	0	R/W	Enabling output of DDR3 general port function bit 2 0: Disabled. 1: Enabled.
1	DDR3GPOE[1]	0	R/W	Enabling output of DDR3 general port function bit 1 0: Disabled. 1: Enabled.
0	DDR3GPOE[0]	0	R/W	—

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.43 DDR3 General Port Output Data Register (DDR3GPOD)

Function: DDR3GPOD is use to write data to DDR3 general port.



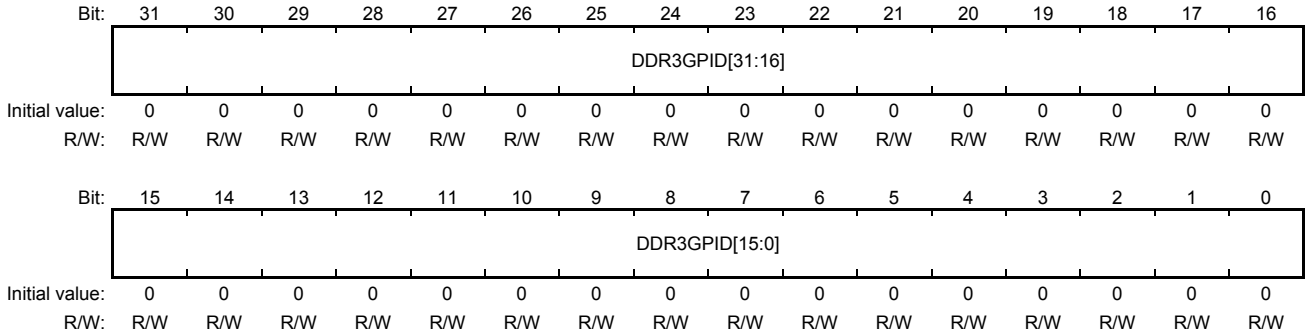
Bit	Bit Name	Initial Value	R/W	Description
31	DDR3GPOD[31]	0	R/W	—
30	DDR3GPOD[30]	0	R/W	—
29	DDR3GPOD[29]	0	R/W	For writing values to DDR3 general port bit 29
28	DDR3GPOD[28]	0	R/W	—
27	DDR3GPOD[27]	0	R/W	—
26	DDR3GPOD[26]	0	R/W	For writing values to DDR3 general port bit 26
25	DDR3GPOD[25]	0	R/W	—
24	DDR3GPOD[24]	0	R/W	For writing values to DDR3 general port bit 24
23	DDR3GPOD[23]	0	R/W	—
22	DDR3GPOD[22]	0	R/W	—
21	DDR3GPOD[21]	0	R/W	For writing values to DDR3 general port bit 21
20	DDR3GPOD[20]	0	R/W	For writing values to DDR3 general port bit 20
19	DDR3GPOD[19]	0	R/W	For writing values to DDR3 general port bit 19
18	DDR3GPOD[18]	0	R/W	—
17	DDR3GPOD[17]	0	R/W	For writing values to DDR3 general port bit 17
16	DDR3GPOD[16]	0	R/W	For writing values to DDR3 general port bit 16
15	DDR3GPOD[15]	0	R/W	For writing values to DDR3 general port bit 15
14	DDR3GPOD[14]	0	R/W	—
13	DDR3GPOD[13]	0	R/W	—
12	DDR3GPOD[12]	0	R/W	For writing values to DDR3 general port bit 12
11	DDR3GPOD[11]	0	R/W	For writing values to DDR3 general port bit 11
10	DDR3GPOD[10]	0	R/W	—
9	DDR3GPOD[9]	0	R/W	For writing values to DDR3 general port bit 9
8	DDR3GPOD[8]	0	R/W	—
7	DDR3GPOD[7]	0	R/W	For writing values to DDR3 general port bit 7
6	DDR3GPOD[6]	0	R/W	—
5	DDR3GPOD[5]	0	R/W	—
4	DDR3GPOD[4]	0	R/W	—
3	DDR3GPOD[3]	0	R/W	For writing values to DDR3 general port bit 3
2	DDR3GPOD[2]	0	R/W	For writing values to DDR3 general port bit 2

Bit	Bit Name	Initial Value	R/W	Description
1	DDR3GPOD[1]	0	R/W	For writing values to DDR3 general port bit 1
0	DDR3GPOD[0]	0	R/W	—

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.44 DDR3 General Port Input Data Register (DDR3GPID)

Function: DDR3GPID is use to read input data from DDR3 general port.



Bit	Bit Name	Initial Value	R/W	Description
31	DDR3GPID[31]	0	R	—
30	DDR3GPID[30]	0	R	—
29	DDR3GPID[29]	0	R	—
28	DDR3GPID[28]	0	R	Indicating values from DDR3 general port bit 28
27	DDR3GPID[27]	0	R	Indicating values from DDR3 general port bit 27
26	DDR3GPID[26]	0	R	—
25	DDR3GPID[25]	0	R	Indicating values from DDR3 general port bit 25
24	DDR3GPID[24]	0	R	—
23	DDR3GPID[23]	0	R	Indicating values from DDR3 general port bit 23
22	DDR3GPID[22]	0	R	Indicating values from DDR3 general port bit 22
21	DDR3GPID[21]	0	R	—
20	DDR3GPID[20]	0	R	—
19	DDR3GPID[19]	0	R	—
18	DDR3GPID[18]	0	R	Indicating values from DDR3 general port bit 18
17	DDR3GPID[17]	0	R	—
16	DDR3GPID[16]	0	R	—
15	DDR3GPID[15]	0	R	—
14	DDR3GPID[14]	0	R	Indicating values from DDR3 general port bit 14
13	DDR3GPID[13]	0	R	Indicating values from DDR3 general port bit 13
12	DDR3GPID[12]	0	R	—
11	DDR3GPID[11]	0	R	—
10	DDR3GPID[10]	0	R	Indicating values from DDR3 general port bit 10
9	DDR3GPID[9]	0	R	—
8	DDR3GPID[8]	0	R	Indicating values from DDR3 general port bit 8
7	DDR3GPID[7]	0	R	—
6	DDR3GPID[6]	0	R	Indicating values from DDR3 general port bit 6
5	DDR3GPID[5]	0	R	Indicating values from DDR3 general port bit 5
4	DDR3GPID[4]	0	R	Indicating values from DDR3 general port bit 4
3	DDR3GPID[3]	0	R	—
2	DDR3GPID[2]	0	R	—
1	DDR3GPID[1]	0	R	—

Bit	Bit Name	Initial Value	R/W	Description
0	DDR3GPID[0]	0	R	—

5.4 Operation

5.4.1 Function Setting for Multiplexed Pins

Setting the LSI multiplexed pin setting mask register (PMMR) is necessary before setting each of the GPIO/peripheral function select registers 0 to 5 (GPSR0 to GPSR5) and peripheral function select registers 0 to 16 (IPSR0 to IPSR16). Specifically, the inverse of the value to be set in the select register must be written to the LSI multiplexed pin setting mask register. Otherwise, the GPIO/peripheral function select registers 0 to 5 (GPSR0 to GPSR5) and peripheral function select registers 0 to 16 (IPSR0 to IPSR16) cannot be set. IPSR0 to IPSR16, MOD_SEL, MOD_SEL2 and MOD_SEL3 registers shall be set before setting GPSR0 to GPSR5 registers in case that they need to be configured. MOD_SEL, MOD_SEL2, and MOD_SEL3 registers can be set either earlier or later than setting IPSR0 to IPSR16 registers.

(1) Procedure for changing pin function from GPIO to peripheral function

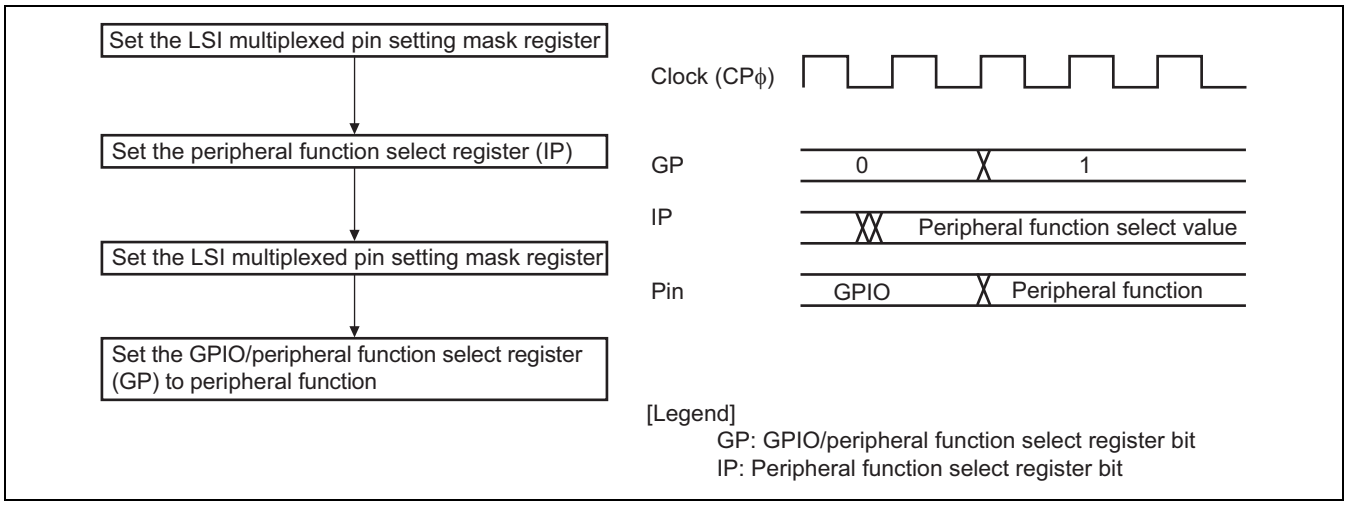


Figure 5.1 Procedure for Changing Pin Function from GPIO to Peripheral Function

(2) Procedure for changing pin function from peripheral function to GPIO

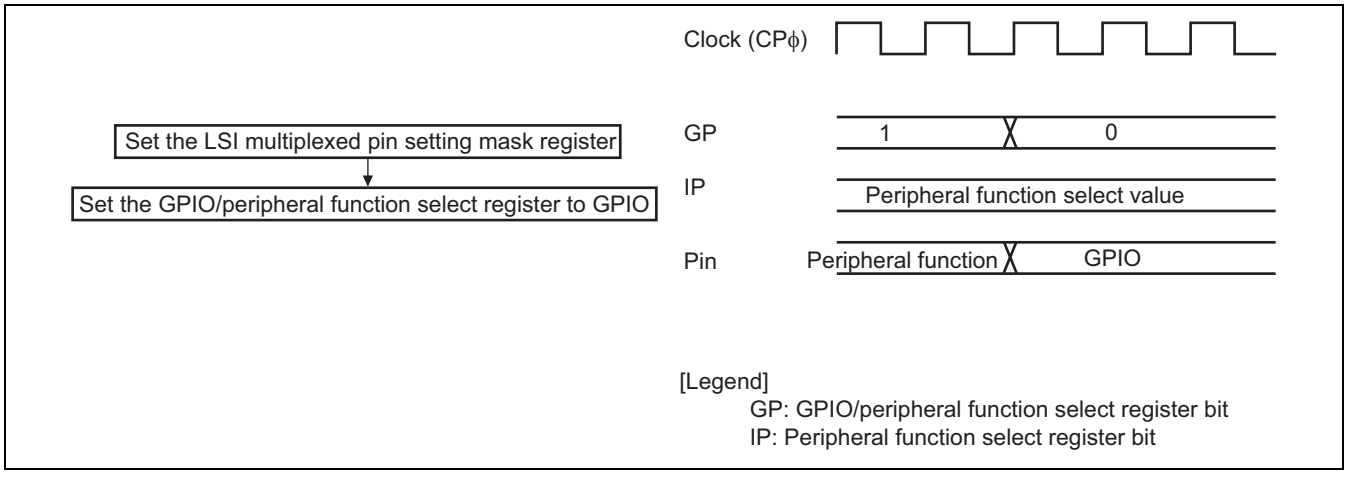


Figure 5.2 Procedure for Changing Pin Function from Peripheral function to GPIO

(3) Procedure 1 for changing pin function from one peripheral function to another peripheral function

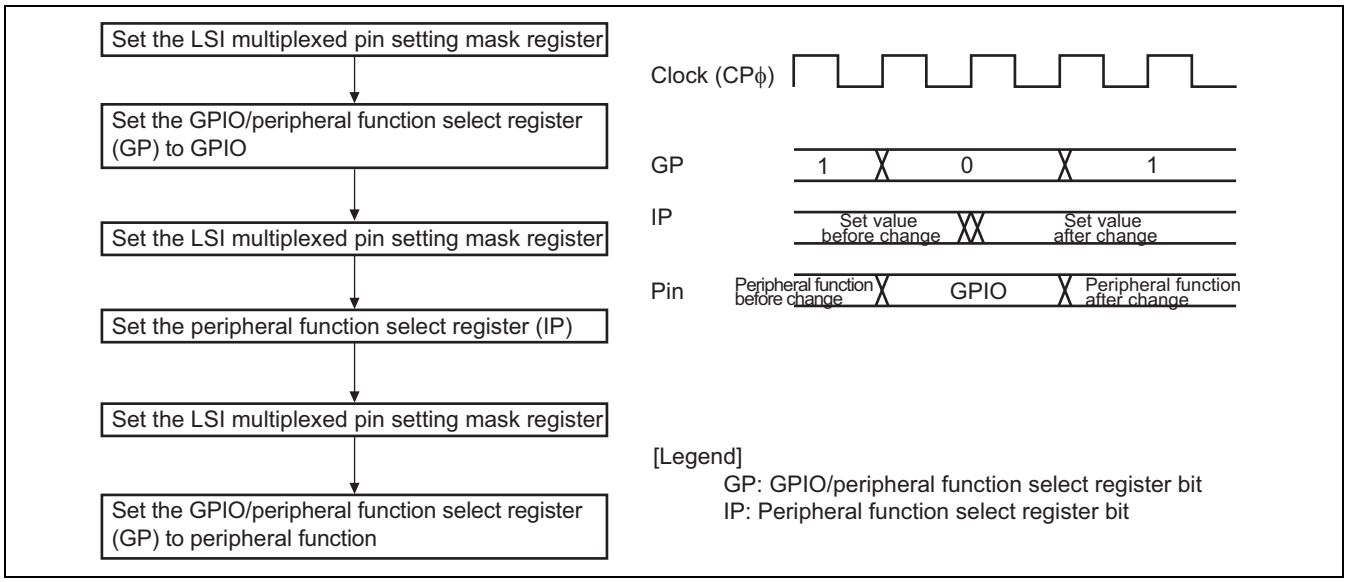


Figure 5.3 Procedure for Changing Pin Function from One Peripheral Function to Another Peripheral Function (with GPIO Setting)

5.4.2 Setting Pull-Up Resistors

The LSI pin pull-up control registers 0 to 6 (PUPR0 to PUPR6) are used to switch the pull-up resistors on and off.

Main Revisions and Additions in this Edition

Minor revisions such as corrections of errors in spelling and modifications of wording are not included in the revision history.

Rev.	Description		
	Page	Contents	Summary
1.00	—	First edition issued	

RZ/G1H User’s Manual: Hardware

Publication Date: Rev.1.00 Sep 30, 2016

Published by: Renesas Electronics Corporation

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 4.0

RZ/G1H

Renesas Electronics Corporation

R01UH0627EJ0100