

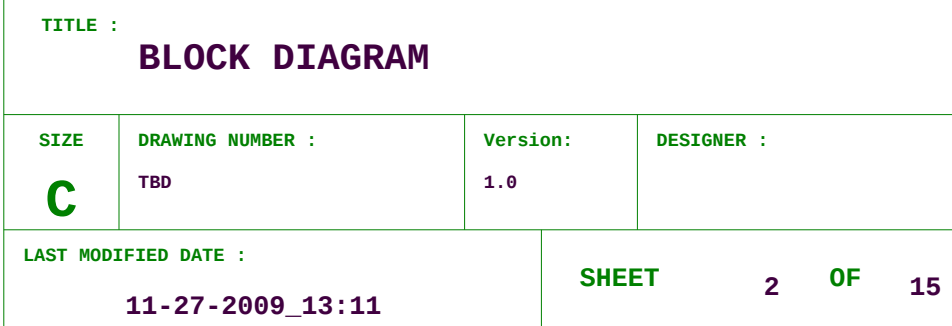
1	2	3	4	5	6	7	
F	Tsi383 (QFP) Evaluation Board Schematics						F
E	TABLE OF CONTENTS						E
D	PAGE 01 - Table of Contents						D
	PAGE 02 - Block Diagram						
	PAGE 03 - Tsi383 PCIe/Misc						
	PAGE 04 - PCIe Connectors						
	PAGE 05 - Tsi383 PCI Interface						
	PAGE 06 - PCI Slot 0 (R/A Top)						
	PAGE 07 - PCI Slot 1 (Vertical)						
	PAGE 08 - PCI Slot 3 (Vertical)						
	PAGE 09 - PCI Slot 2 (Vertical)						
	PAGE 10 - Clock Distribution						
C	PAGE 11 - Power Sources						C
	PAGE 12 - Tsi383 Power/Regulators						
	PAGE 13 - PCI Regulators						
	PAGE 14 - Test Devices						
	PAGE 15 - Test Devices Cont'd						
B							B
A							A
1	2	3	4	5	6	7	

TABLE OF CONTENTS

- PAGE 01 - Table of Contents
- PAGE 02 - Block Diagram
- PAGE 03 - Tsi383 PCIe/Misc
- PAGE 04 - PCIe Connectors
- PAGE 05 - Tsi383 PCI Interface
- PAGE 06 - PCI Slot 0 (R/A Top)
- PAGE 07 - PCI Slot 1 (Vertical)
- PAGE 08 - PCI Slot 3 (Vertical)
- PAGE 09 - PCI Slot 2 (Vertical)
- PAGE 10 - Clock Distribution
- PAGE 11 - Power Sources
- PAGE 12 - Tsi383 Power/Regulators
- PAGE 13 - PCI Regulators
- PAGE 14 - Test Devices
- PAGE 15 - Test Devices Cont'd

TITLE :			
TABLE OF CONTENTS			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	TBD	1.0	
LAST MODIFIED DATE :		SHEET 1 OF 15	
11-27-2009_13:11			

TITLE : BLOCK DIAGRAM			
SIZE C	DRAWING NUMBER : TBD	Version: 1.0	DESIGNER :
LAST MODIFIED DATE : 11-27-2009_13:11		SHEET 2 OF 15	



TSI383 PCIE/MISC INTERFACE

TSI383 STRAPS

RESET CONTROLLER

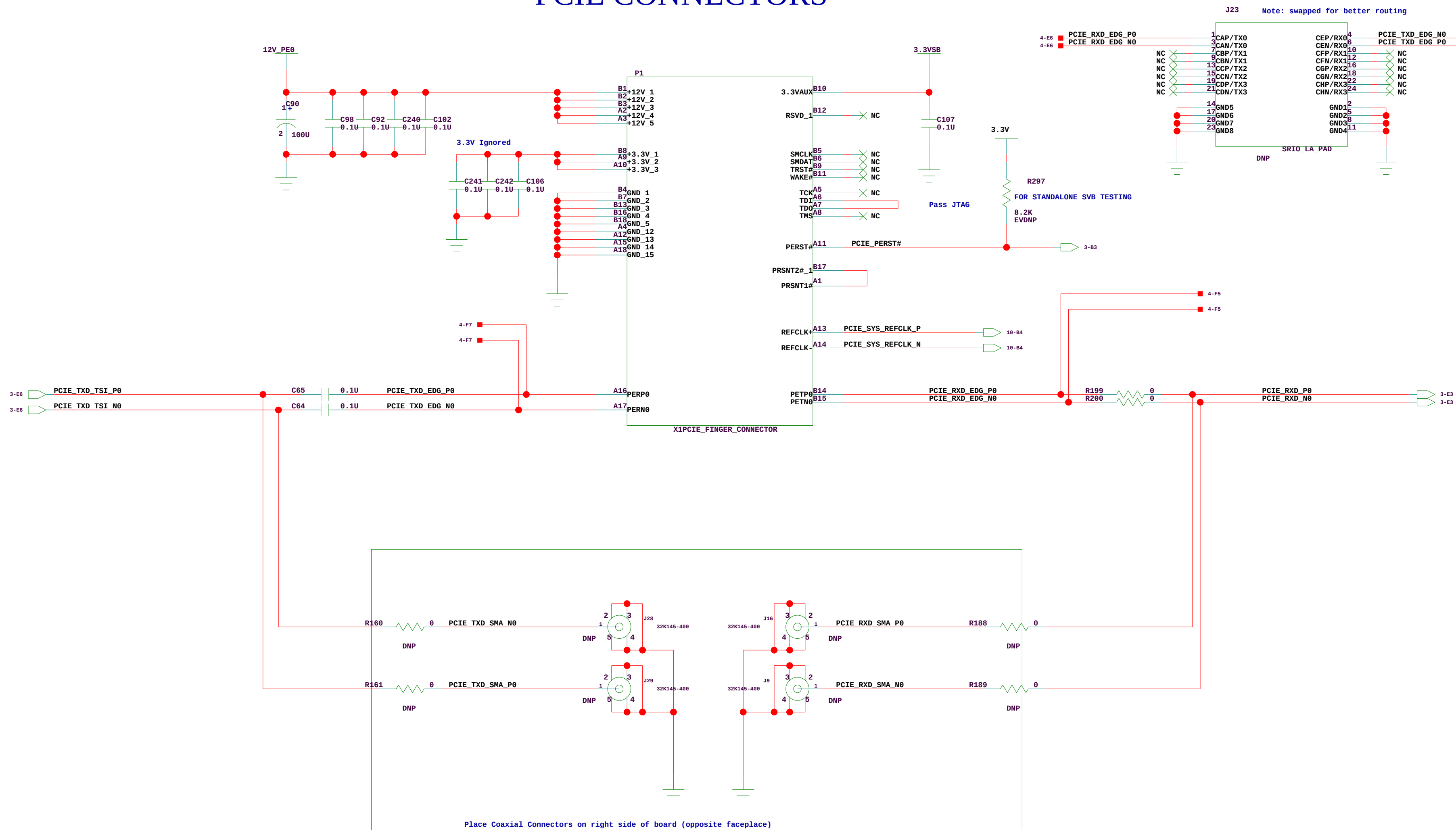
TSI383JTAG

TITLE :
TSI383 PCIE/MISC

SIZE C	DRAWING NUMBER : TBD	Version: 1.0	DESIGNER :
-----------	-------------------------	-----------------	------------

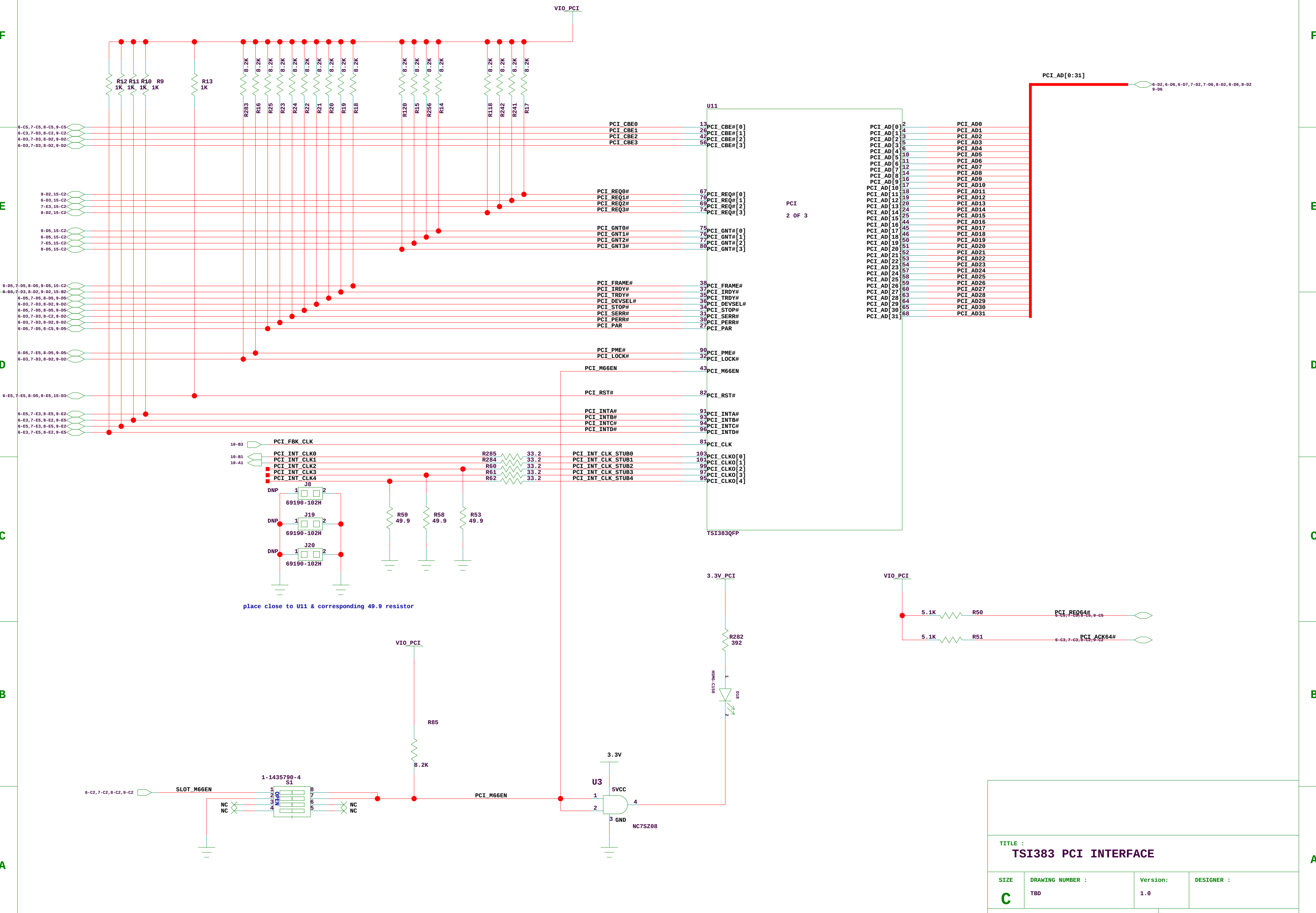
LAST MODIFIED DATE : 11-27-2009_13:11	SHEET 3 OF 15
--	------------------

3 4



TITLE :			
PCIE CONNECTORS			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	TBD	1.0	
LAST MODIFIED DATE :		SHEET 4 OF 15	
11-27-2009_13:11			

TSI383 PCI INTERFACE



TITLE : TSI383 PCI INTERFACE			
SIZE C	DRAWING NUMBER : TBD	Version: 1.0	DESIGNER :
LAST MODIFIED DATE : 11-27-2009_13:11		SHEET 5 OF 15	

PCI SLOT 0 (R/A)

IDSEL AD16

- Required Interrupt Routing

SLOT : BRIDGE

INTA -> INTA

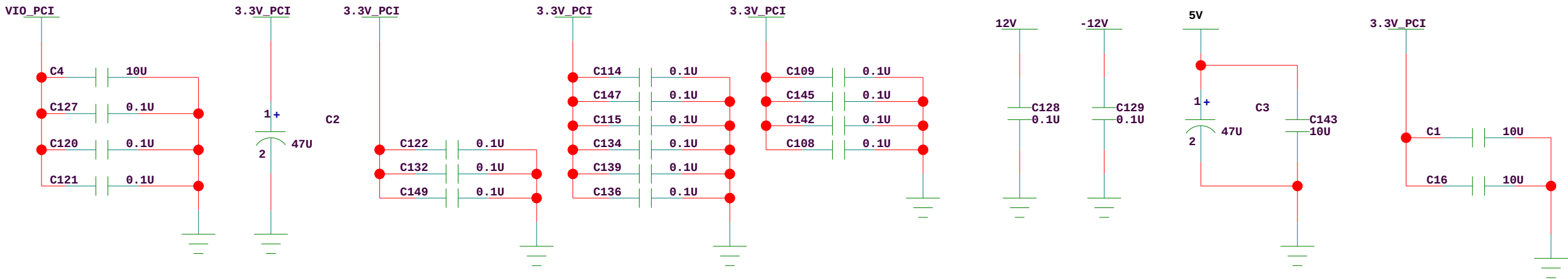
INTB -> INTB

INTC -> INTC

INTD -> INTD

- PCI Clock PCI_CLK0

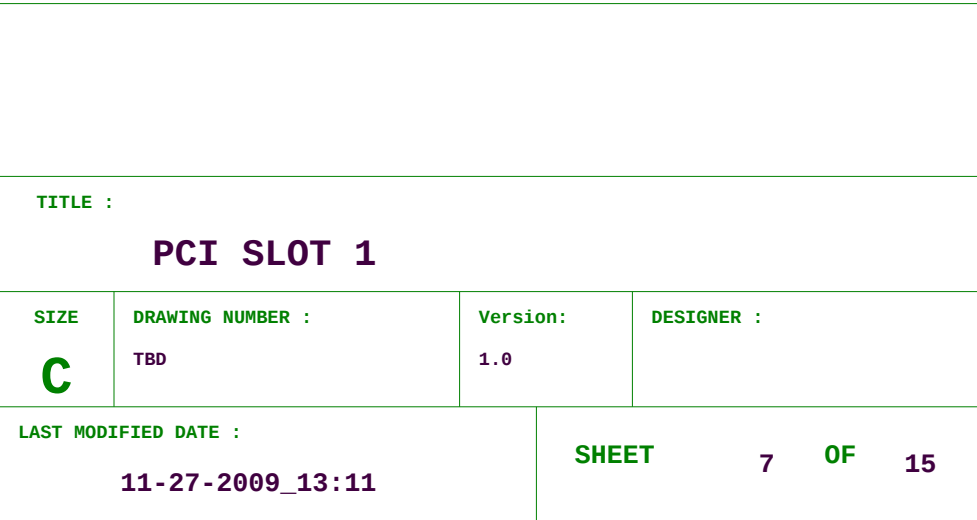
- PCI Arbitration PCI_GNT#1/PCI_REQ#1



TITLE :			
PCI SLOT 0			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	TBD	1.0	
LAST MODIFIED DATE :		SHEET 6 OF 15	
11-27-2009_13:11			

```
IDSEL AD17
```

- Required Interrupt Routing
 - SLOT : BRIDGE
 - INTA -> INTB
 - INTB -> INTC
 - INTC -> INTD
 - INTD -> INTA
- PCI Clock PCI_CLK1
- PCI Arbitration PCI_GNT#2/PCI_REQ#2



PCI SLOT 3 (Vertical)

IDSEL AD18

- Required Interrupt Routing

SLOT : BRIDGE

INTA -> INTC

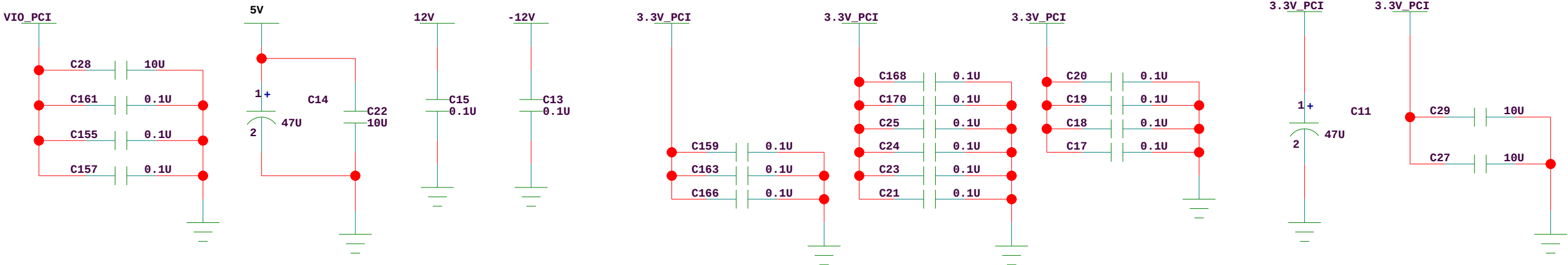
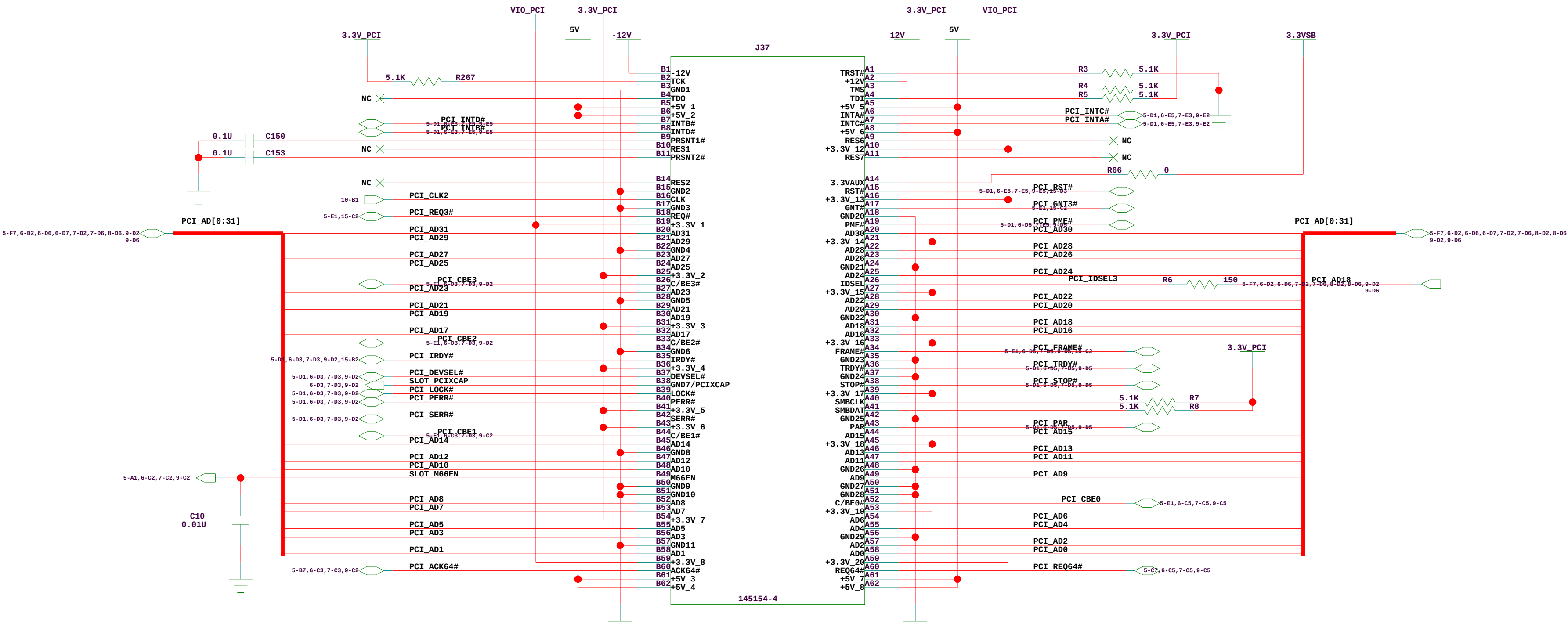
INTB -> INTD

INTC -> INTA

INTD -> INTB

- PCI Clock PCI_CLK2

- PCI Arbitration PCI_GNT#3/PCI_REQ#3



TITLE : PCI SLOT 3			
SIZE C	DRAWING NUMBER : TBD	Version: 1.0	DESIGNER :
LAST MODIFIED DATE : 11-27-2009_13:11		SHEET 8 OF 15	

PCI SLOT 2 (Vertical)

IDSEL AD19

- Required Interrupt Routing

SLOT : BRIDGE

INTA -> INTD

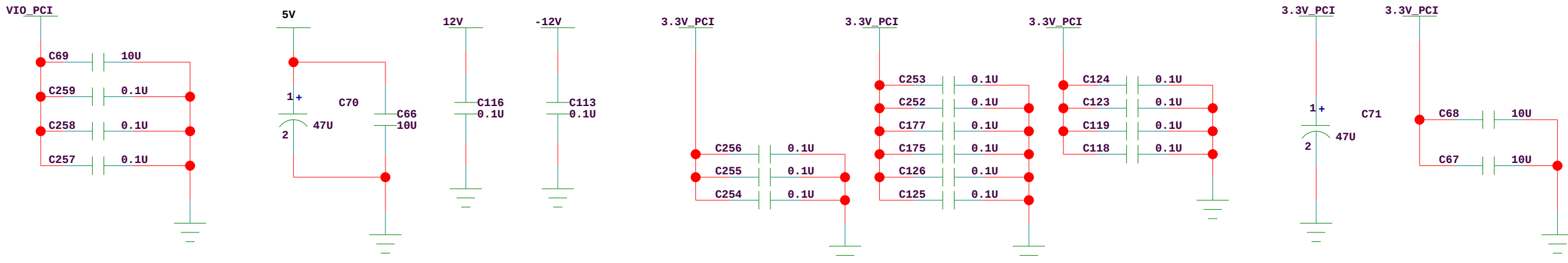
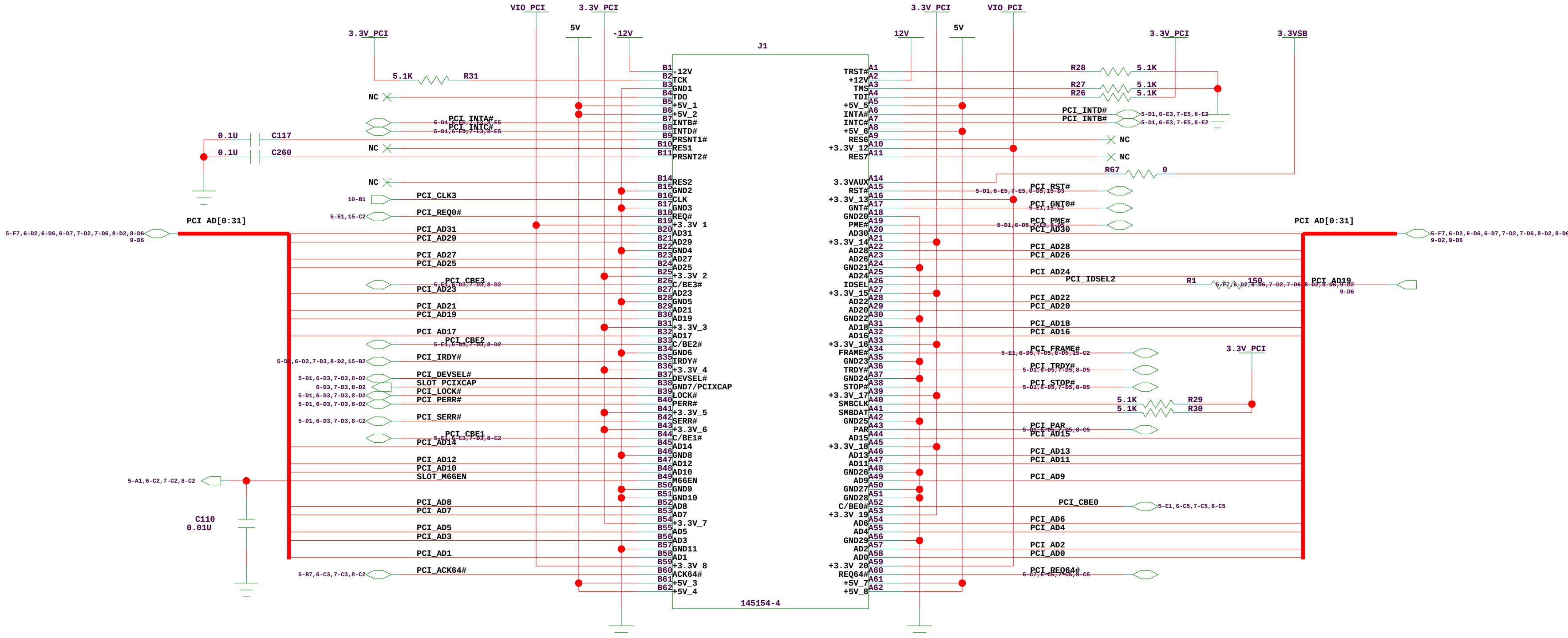
INTB -> INTA

INTC -> INTB

INTD -> INTC

- PCI Clock PCI_CLK3

- PCI Arbitration PCI_GNT#0/PCI_REQ#0



TITLE :			
PCI SLOT 2			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	TBD	1.0	
LAST MODIFIED DATE :		SHEET 9 OF 15	
11-27-2009_13:11			

CLOCK DISTRIBUTION

PCI EXTERNAL CLOCK

PCIe LOCAL CLOCKGEN

SYS/LOCAL PCIE CLOCK MULTIPLEXER

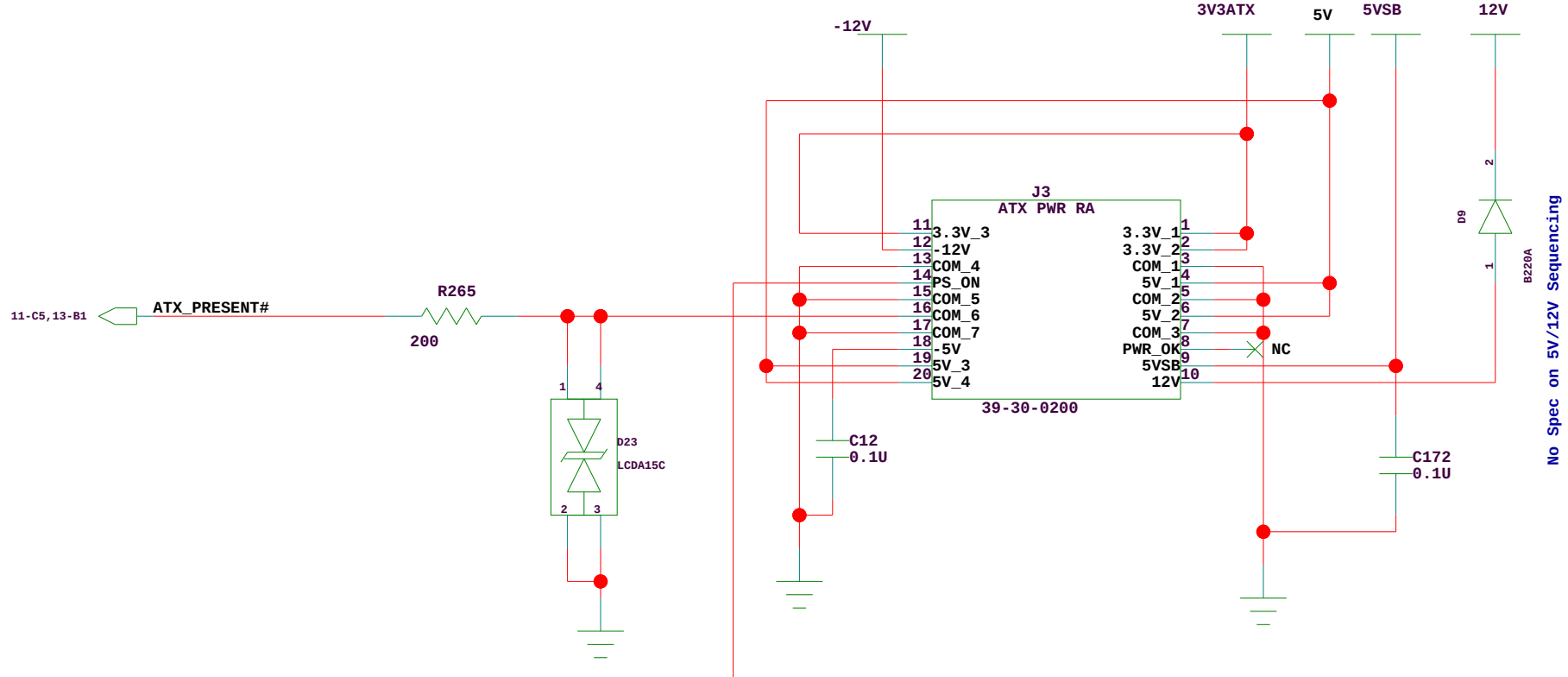
Frequency Select (ICS87604I)		
FBDIV_SEL[0:1]	DIV_SEL[0:1]	OUTPUT
0:0	0:0	100Mhz
0:0	1:0	50Mhz
0:0	1:1	25Mhz
0:1	0:0	133Mhz
0:1	1:0	66Mhz
0:1	1:1	33Mhz

Place resistors near CY2305

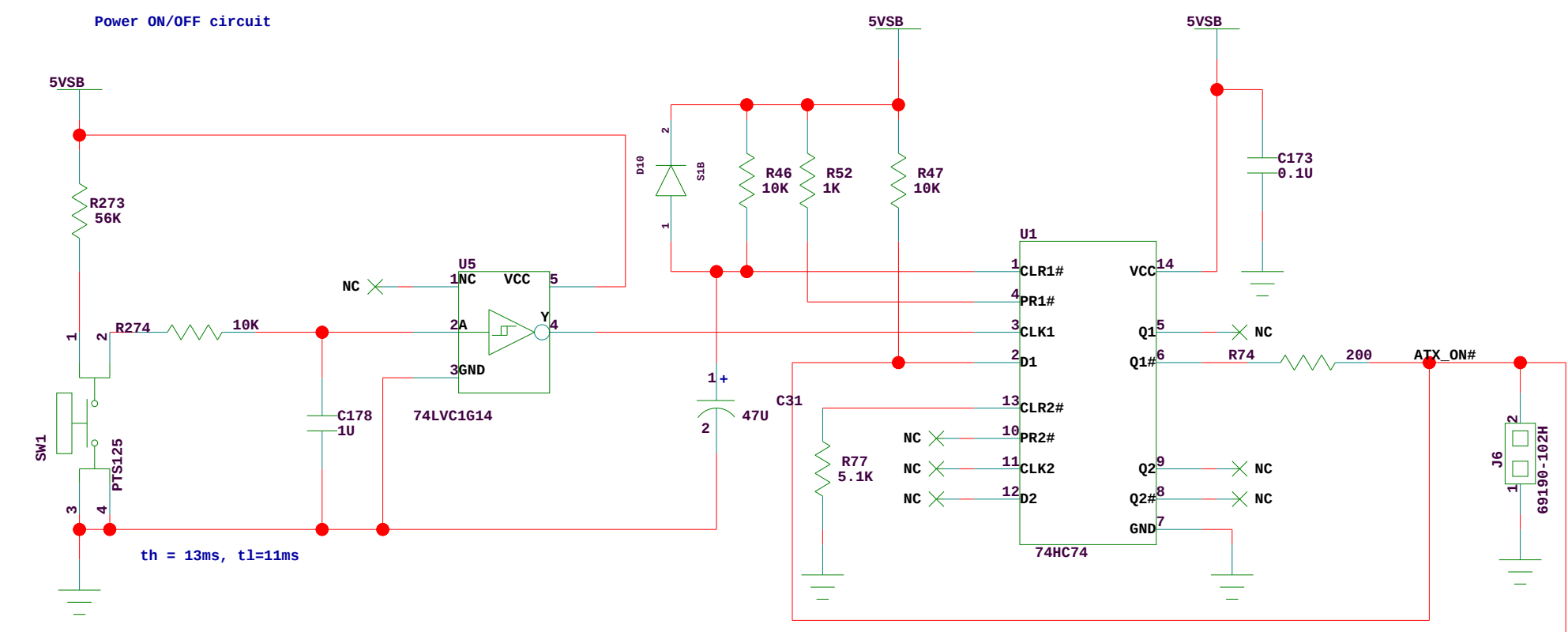
TITLE :			
CLOCK DISTRIBUTION			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C		1.0	
LAST MODIFIED DATE :		SHEET 10 OF 15	
11-27-2009_13:11			

POWER SOURCES

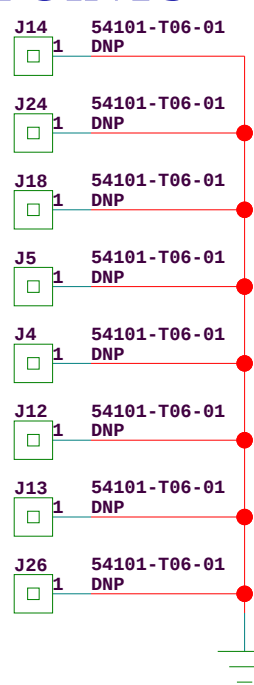
ATX



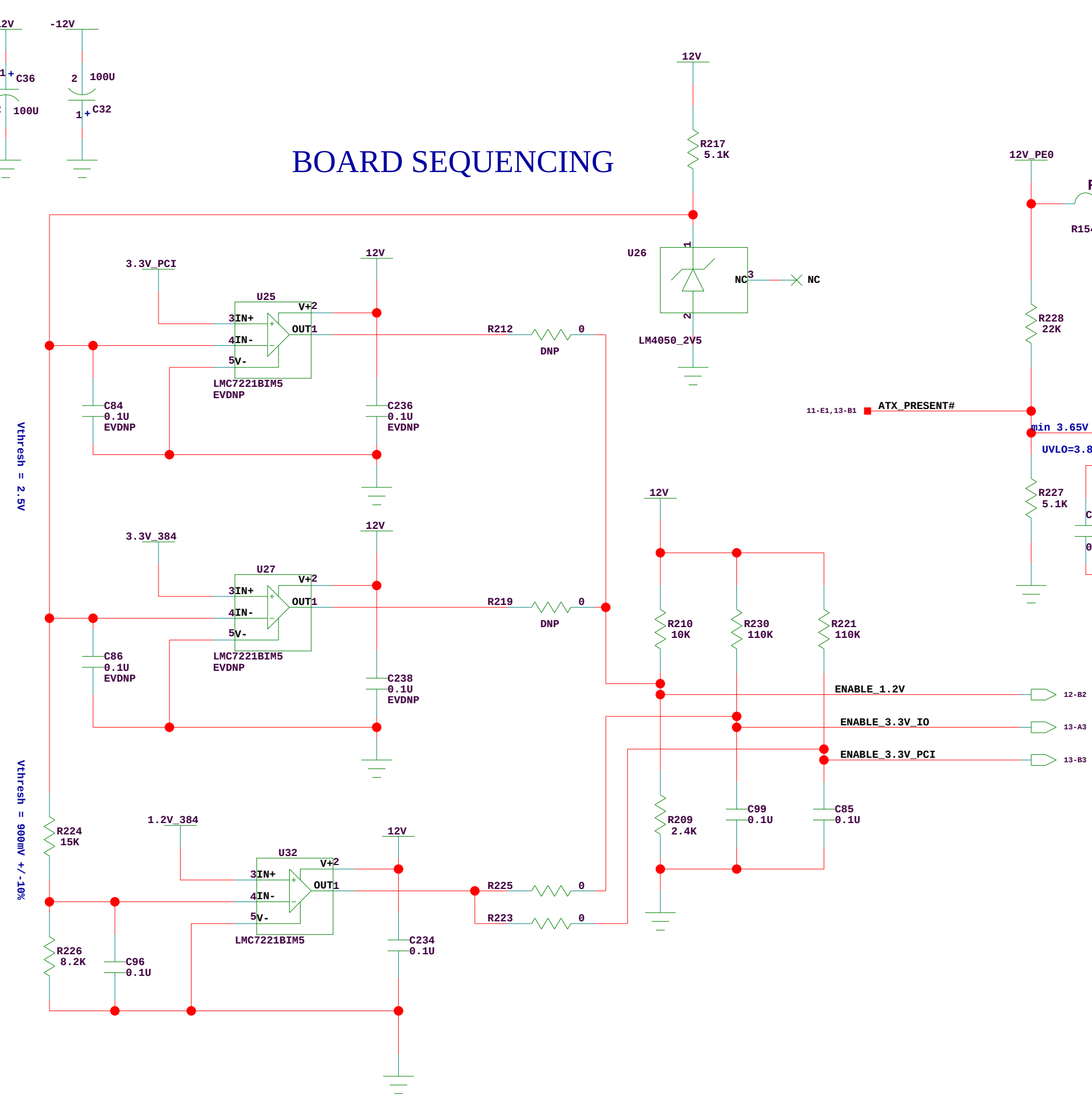
ATX SUPPLY TOGGLE



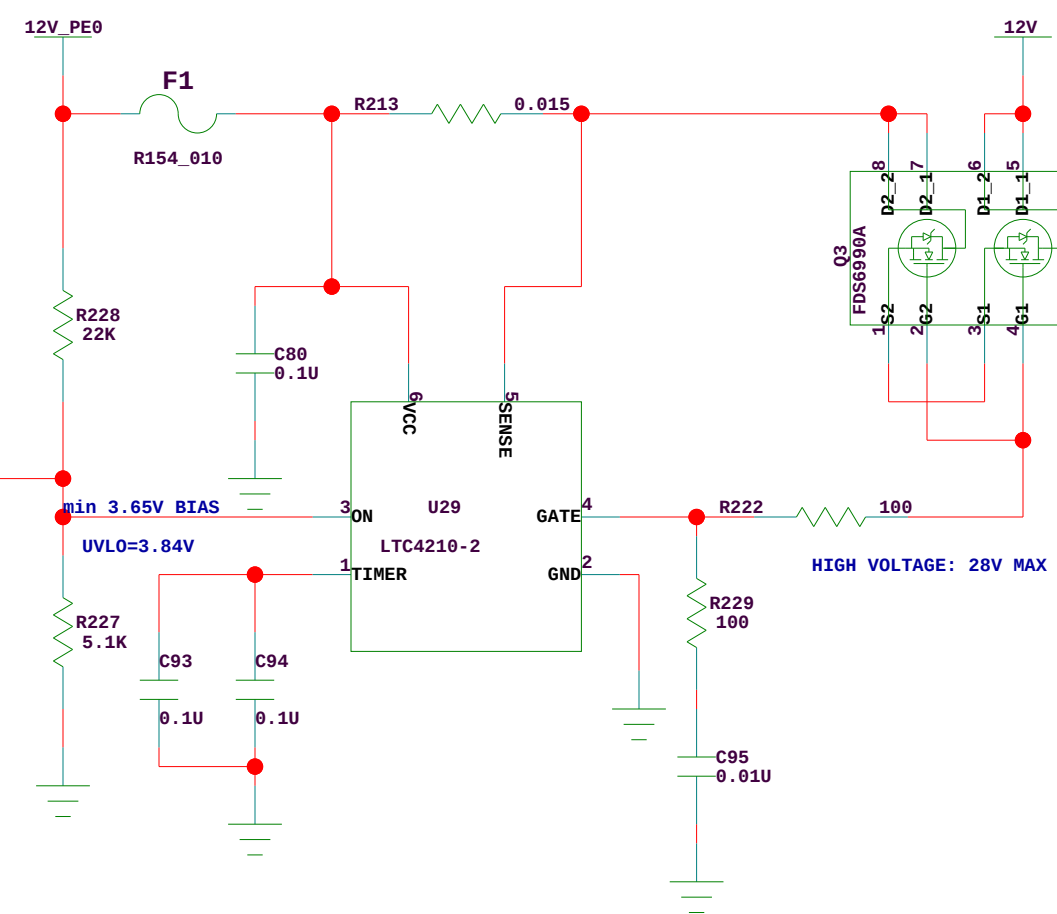
GND TESTPOINTS



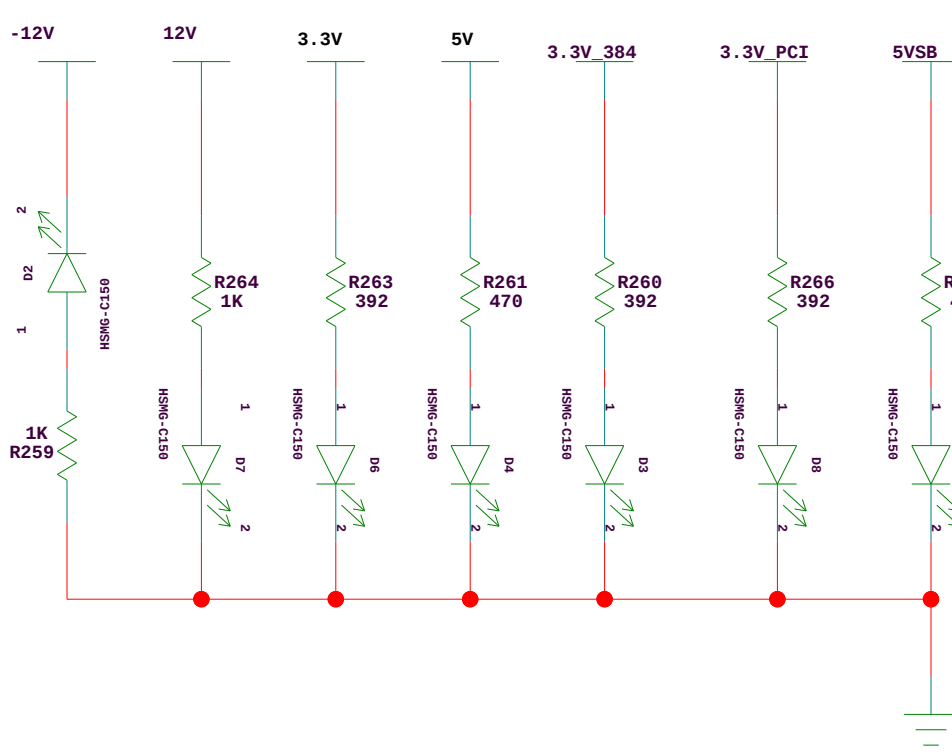
BOARD SEQUENCING



SYS SUPPLY SWITCH

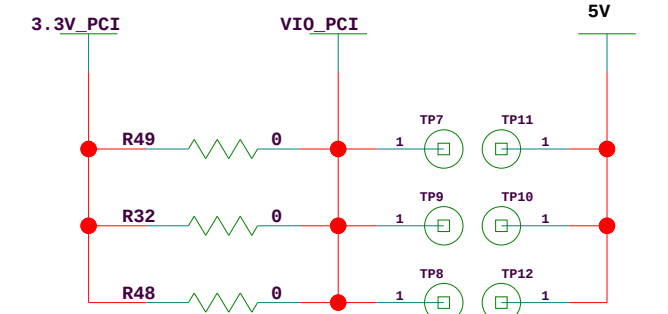


POWER STATUS



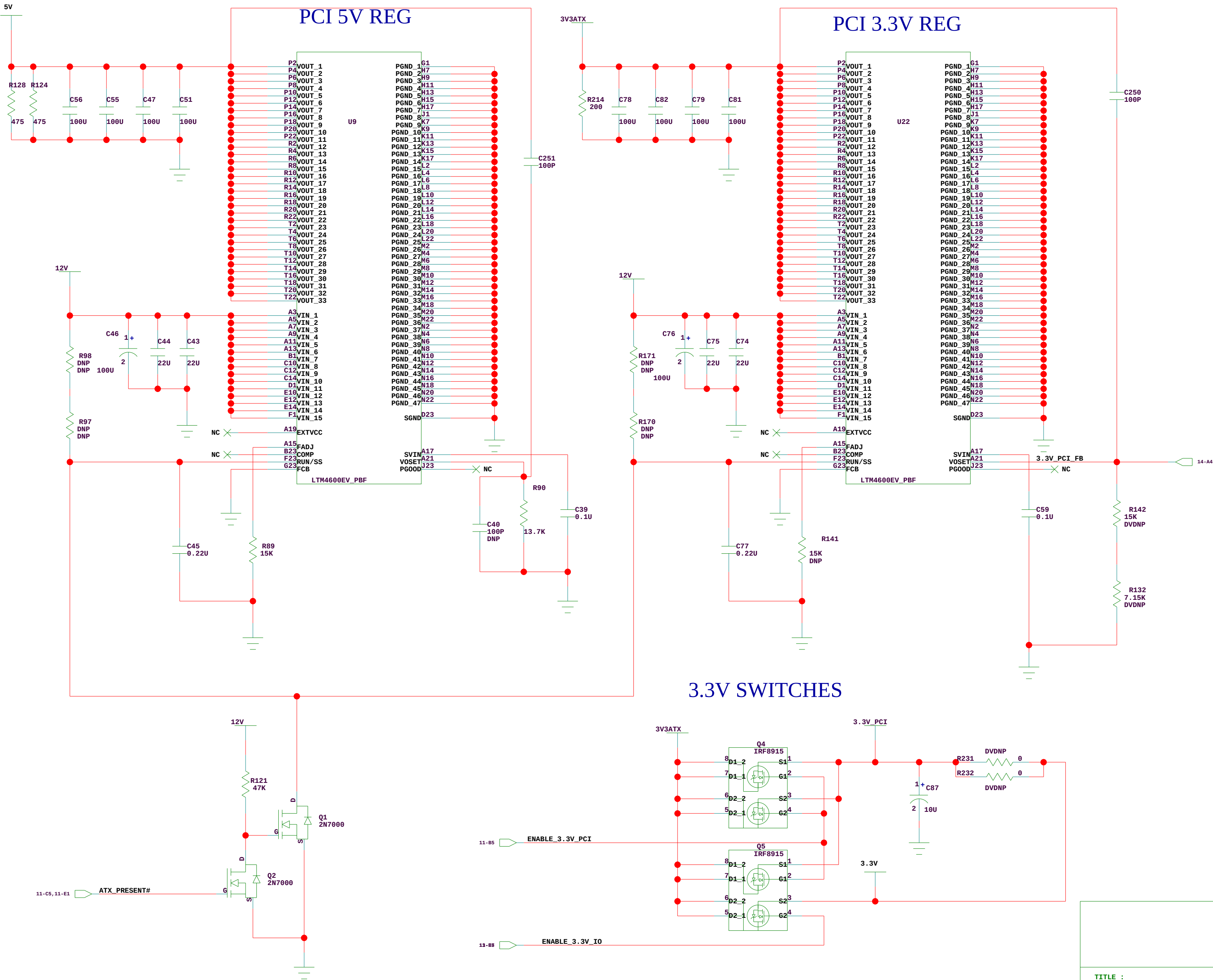
TITLE : POWER SOURCES			
SIZE C	DRAWING NUMBER : TBD	Version: 1.0	DESIGNER :
LAST MODIFIED DATE : 11-27-2009_13:11		SHEET 11 OF 15	

TSI383 VIO CURRENT SENSE



TITLE :			
TSI383 POWER/REGULATORS			
SIZE C	DRAWING NUMBER : TBD	Version: 1.0	DESIGNER :
LAST MODIFIED DATE : 11-27-2009_13:11		SHEET 12 OF 15	

PCI POWER REGULATORS



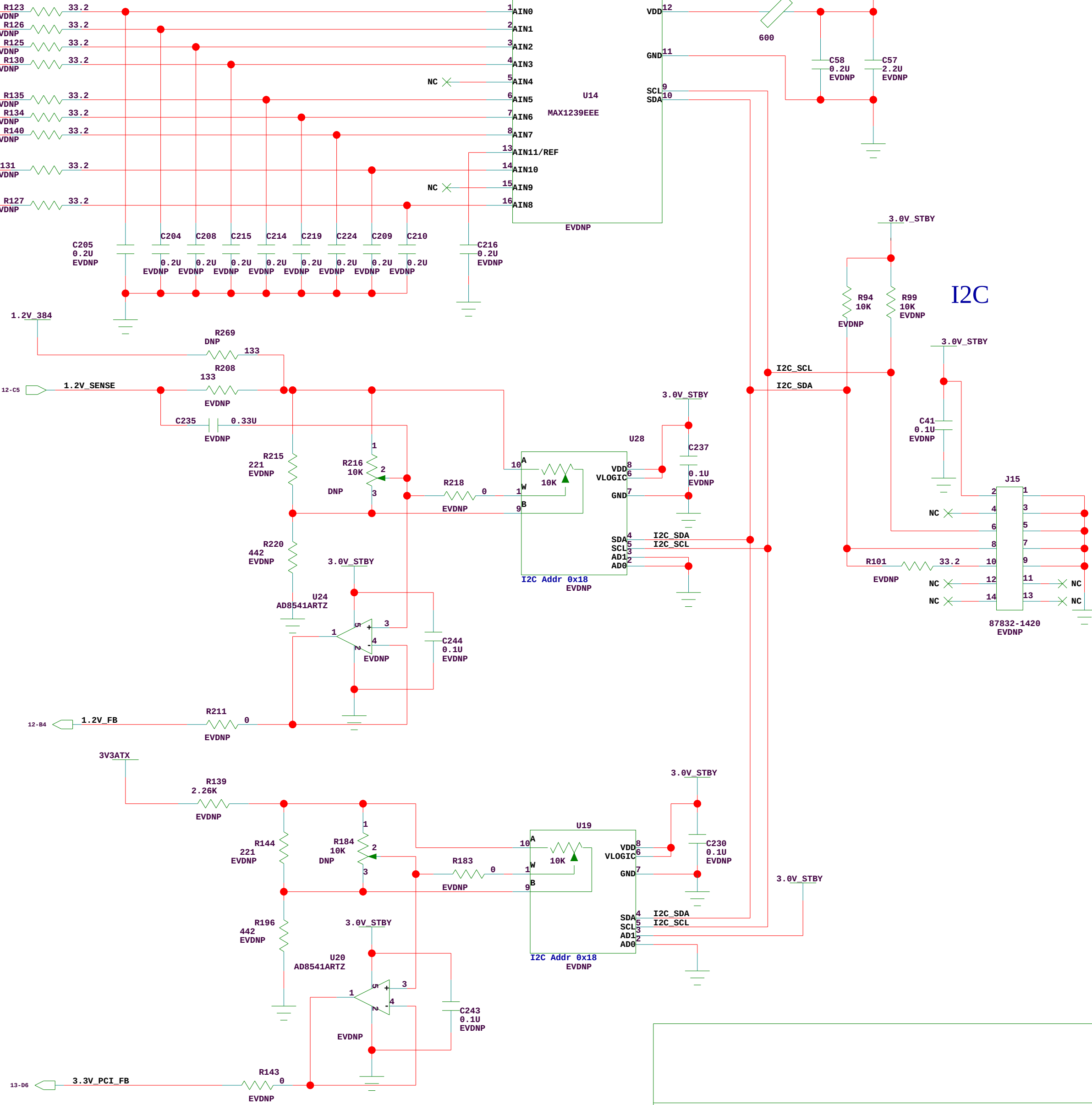
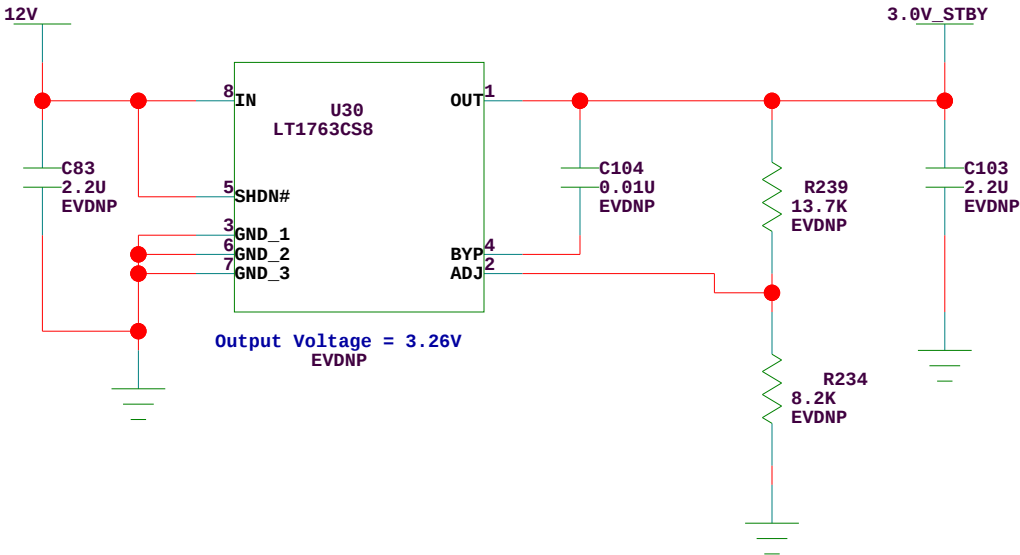
TITLE :			
PCI POWER REGULATORS			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	TBD	1.0	
LAST MODIFIED DATE :		SHEET 13 OF 15	
11-27-2009_13:11			

TEST DEVICES

TSI383 V/I ADC

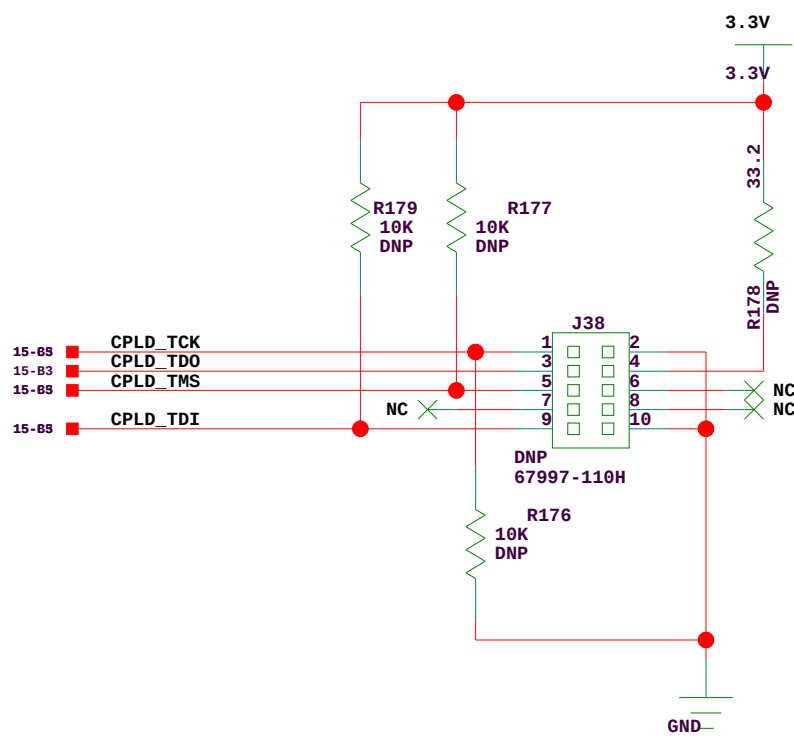
ANALOG SUPPLY

I2C

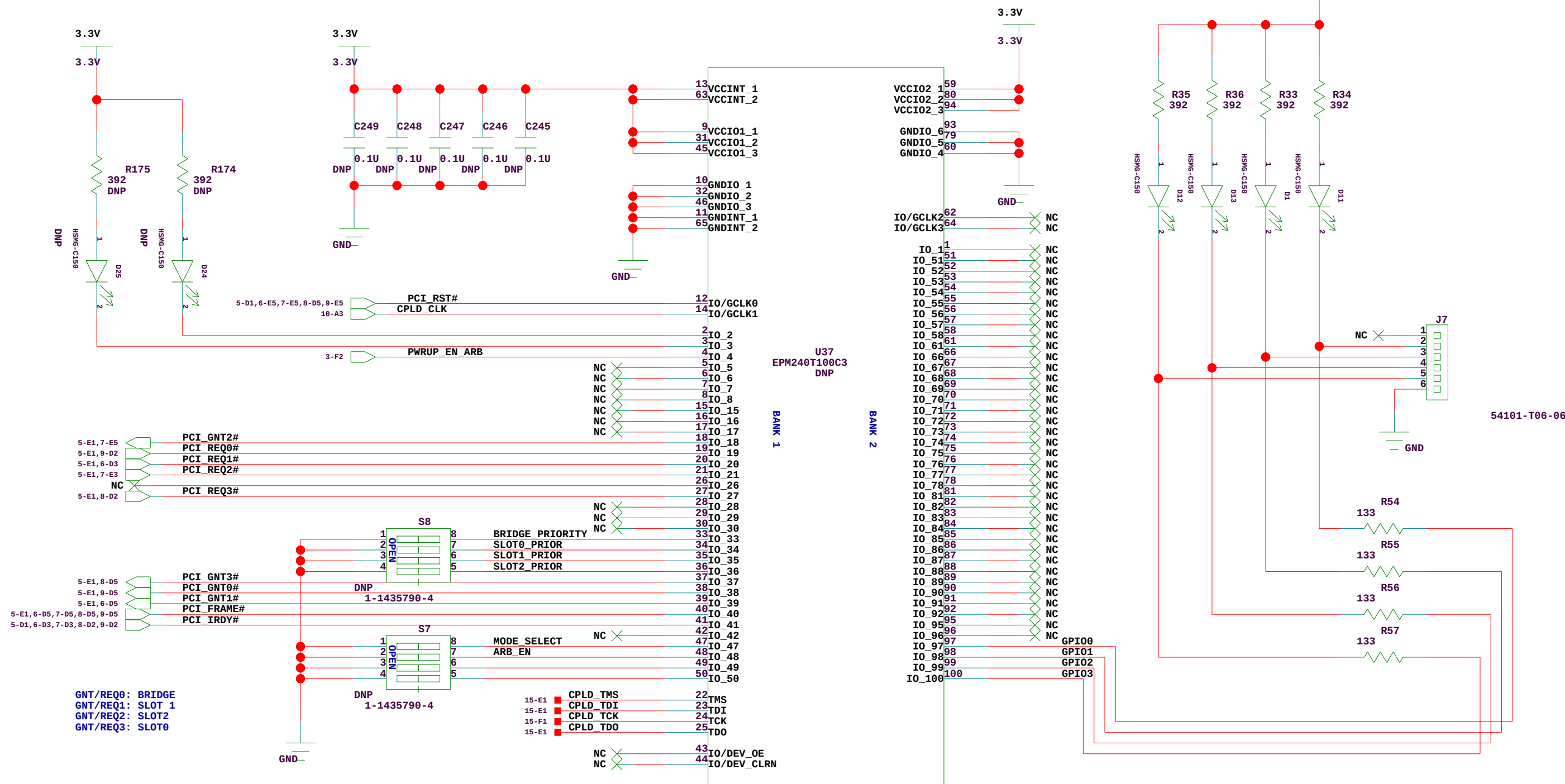


TITLE : TEST DEVICES			
SIZE C	DRAWING NUMBER : TBD	Version: 1.0	DESIGNER :
LAST MODIFIED DATE : 11-27-2009_13:11		SHEET 14 OF 15	

TEST DEVICES CONT'D



PCIARBITER/GPIO CONTROL



TITLE :

TEST DEVICES CONT'D

SIZE

DRAWING NUMBER :

TBD

Version:

1.0

DESIGNER :

LAST MODIFIED DATE :

11-27-2009_13:11

SHEET

15

OF

15