User's Manual

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M16C/5M Group, M16C/57 Group

User's Manual: Hardware

RENESAS MCU

M16C Family / M16C/50 Series

Renesas Electronics
www.renesas.com

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

About This Manual

1. Purpose and Target User

This manual is designed to be read primarily by application developers who have an understanding of this microcomputer (MCU) including its hardware functions and electrical characteristics. The user should have a basic understanding of electric circuits, logic circuits and, MCUs.
This manual consists of six main categories: Overview, CPU, System Control, Peripherals, Electrical Characteristics, and Usage Notes.

Carefully read all notes in this document prior to use. Notes are found throughout each chapter, at the end of each chapter, and in the dedicated Usage Notes chapter.

The Revision History at the end of this manual summarizes primary modifications and additions to the previous versions. For details, please refer to the relative chapters or sections of this manual.

The M16C/5M Group, M16C/57 Group includes the documents listed below. Verify this manual is the latest version by visiting the Renesas Electronics website.

Type of Document	Contents	Document Name	Document Number
Datasheet	Overview of Hardware and Electrical Characteristics	M16C/5M Group, M16C/57 Group Datasheet	R01DS0019EJ0110
User's Manual: Hardware	Specifications and detailed descriptions of: -pin layout -memory map -peripherals -electrical characteristics -timing characteristics Refer to the Application Manual for peripheral usage.	M16C/5M Group, M16C/57 Group User's Manual: Hardware	This publication
User's Manual: Software/Software Manual	Descriptions of instruction set	M16C/60, M16C/20, M16C/Tiny Series Software Manual	REJ09B0137
Application Note	-Usages -Applications -Sample programs -Programming technics using Assembly language or C programming language	Available on the Renesas Electronics website.	
Renesas Technical Update	Bulletins on product specifications, documents, etc.		

2. Numbers and Symbols

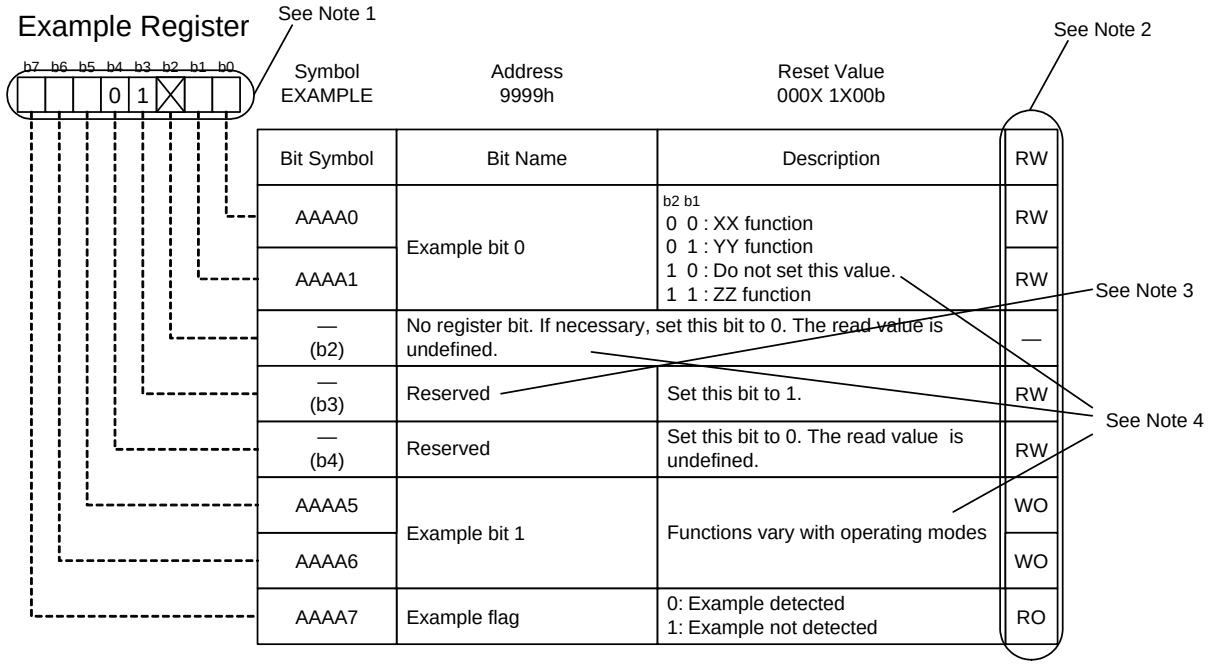
The following explains the denotations used in this manual for registers, bits, pins and various numbers.

(1) Registers, bits, and pins
Registers, bits, and pins are indicated by symbols. Each symbol has a register/bit/pin identifier after the symbol.
Example: PM03 bit in the PM0 register
P3_5 pin, VCC pin

(2) Numbers
A binary number has the suffix “b” except for a 1-bit value.
A hexadecimal number has the suffix “h”.
A decimal number has no suffix.
Example: Binary notation: 11b
Hexadecimal notation: EFA0h
Decimal notation: 1234

3. Registers

The following illustration describes registers used throughout this manual.



Notes:

1. Blank box: Set this bit to 0 or 1 according to the function.
   0: Set this bit to 0.
   1: Set this bit to 1.
   X: Nothing is assigned to this bit.

2. RW: Read and write
   RO: Read only
   WO: Write only (the read value is undefined)
   —: Not applicable

3. Reserved bit: This bit field is reserved. Set this bit to a specified value. For RW bits, the written value is read unless otherwise noted.

4.
- No register bit(s): No register bit(s) is/are assigned to this field. If necessary, set to 0 for possible future implementation.
- Do not use this combination: Proper operation is not guaranteed when this value is set.
- Functions vary with operating modes: Functions vary with peripheral operating modes. Refer to register illustrations of the respective mode.

4. Abbreviations and Acronyms

The following acronyms and terms are used throughout this manual.

Abbreviation/Acronym	Meaning
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connection
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

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0009h			
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D345h	CAN1 Mailbox 20: Data Length		
D346h	CAN1 Mailbox 20: Data Field		
D347h			
D348h			
D349h			
D34Ah			
D34Bh			
D34Ch			
D34Dh			
D34Eh	CAN1 Mailbox 20: Time Stamp		
D34Fh			
D350h	CAN1 Mailbox 21: Message Identifier	C1MB21	673
D351h			
D352h			
D353h			
D354h			
D355h	CAN1 Mailbox 21: Data Length		
D356h	CAN1 Mailbox 21: Data Field		
D357h			
D358h			
D359h			
D35Ah			
D35Bh			
D35Ch			
D35Dh			
D35Eh	CAN1 Mailbox 21: Time Stamp		
D35Fh			
D360h	CAN1 Mailbox 22: Message Identifier	C1MB22	673
D361h			
D362h			
D363h			
D364h			
D365h	CAN1 Mailbox 22: Data Length		
D366h	CAN1 Mailbox 22: Data Field		
D367h			
D368h			
D369h			
D36Ah			
D36Bh			
D36Ch			
D36Dh			
D36Eh	CAN1 Mailbox 22: Time Stamp		
D36Fh			

The blank areas are reserved. No access is allowed.

Address	Register	Symbol	Page
D370h	CAN1 Mailbox 23: Message Identifier	C1MB23	673
D371h			
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D373h			
D374h			
D375h	CAN1 Mailbox 23: Data Length		
D376h	CAN1 Mailbox 23: Data Field		
D377h			
D378h			
D379h			
D37Ah			
D37Bh			
D37Ch			
D37Dh			
D37Eh	CAN1 Mailbox 23: Time Stamp		
D37Fh			
D380h	CAN1 Mailbox 24: Message Identifier	C1MB24	673
D381h			
D382h			
D383h			
D384h			
D385h	CAN1 Mailbox 24: Data Length		
D386h	CAN1 Mailbox 24: Data Field		
D387h			
D388h			
D389h			
D38Ah			
D38Bh			
D38Ch			
D38Dh			
D38Eh	CAN1 Mailbox 24: Time Stamp		
D38Fh			
D390h	CAN1 Mailbox 25: Message Identifier	C1MB25	673
D391h			
D392h			
D393h			
D394h			
D395h	CAN1 Mailbox 25: Data Length		
D396h	CAN1 Mailbox 25: Data Field		
D397h			
D398h			
D399h			
D39Ah			
D39Bh			
D39Ch			
D39Dh			
D39Eh	CAN1 Mailbox 25: Time Stamp		
D39Fh			
D3A0h	CAN1 Mailbox 26: Message Identifier	C1MB26	673
D3A1h			
D3A2h			
D3A3h			
D3A4h			
D3A5h	CAN1 Mailbox 26: Data Length		
D3A6h	CAN1 Mailbox 26: Data Field		
D3A7h			
D3A8h			
D3A9h			
D3AAh			
D3ABh			
D3ACh			
D3ADh			
D3AEh	CAN1 Mailbox 26: Time Stamp		
D3AFh			

Address	Register	Symbol	Page
D3B0h	CAN1 Mailbox 27: Message Identifier	C1MB27	673
D3B1h			
D3B2h			
D3B3h			
D3B4h			
D3B5h	CAN1 Mailbox 27: Data Length		
D3B6h	CAN1 Mailbox 27: Data Field		
D3B7h			
D3B8h			
D3B9h			
D3BAh			
D3BBh			
D3BCh			
D3BDh			
D3BEh	CAN1 Mailbox 27: Time Stamp		
D3BFh			
D3C0h	CAN1 Mailbox 28: Message Identifier	C1MB28	673
D3C1h			
D3C2h			
D3C3h			
D3C4h			
D3C5h	CAN1 Mailbox 28: Data Length		
D3C6h	CAN1 Mailbox 28: Data Field		
D3C7h			
D3C8h			
D3C9h			
D3CAh			
D3CBh			
D3CCh			
D3CDh			
D3CEh	CAN1 Mailbox 28: Time Stamp		
D3CFh			
D3D0h	CAN1 Mailbox 29: Message Identifier	C1MB29	673
D3D1h			
D3D2h			
D3D3h			
D3D4h			
D3D5h	CAN1 Mailbox 29: Data Length		
D3D6h	CAN1 Mailbox 29: Data Field		
D3D7h			
D3D8h			
D3D9h			
D3DAh			
D3DBh			
D3DCh			
D3DDh			
D3DEh	CAN1 Mailbox 29: Time Stamp		
D3DFh			
D3E0h	CAN1 Mailbox 30: Message Identifier	C1MB30	673
D3E1h			
D3E2h			
D3E3h			
D3E4h			
D3E5h	CAN1 Mailbox 30: Data Length		
D3E6h	CAN1 Mailbox 30: Data Field		
D3E7h			
D3E8h			
D3E9h			
D3EAh			
D3EBh			
D3ECh			
D3EDh			
D3EEh	CAN1 Mailbox 30: Time Stamp		
D3EFh			

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Address	Register	Symbol	Page
D3F0h	CAN1 Mailbox 31: Message Identifier	C1MB31	673
D3F1h			
D3F2h			
D3F3h			
D3F4h			
D3F5h	CAN1 Mailbox 31: Data Length		
D3F6h	CAN1 Mailbox 31: Data Field		
D3F7h			
D3F8h			
D3F9h			
D3FAh			
D3FBh			
D3FCh			
D3FDh			
D3FEh	CAN1 Mailbox 31: Time Stamp		
D3FFh			
D400h	CAN1 Mask Register 0	C1MKR0	669
D401h			
D402h			
D403h			
D404h	CAN1 Mask Register 1	C1MKR1	669
D405h			
D406h			
D407h			
D408h	CAN1 Mask Register 2	C1MKR2	669
D409h			
D40Ah			
D40Bh			
D40Ch	CAN1 Mask Register 3	C1MKR3	669
D40Dh			
D40Eh			
D40Fh			
D410h	CAN1 Mask Register 4	C1MKR4	669
D411h			
D412h			
D413h			
D414h	CAN1 Mask Register 5	C1MKR5	669
D415h			
D416h			
D417h			
D418h	CAN1 Mask Register 6	C1MKR6	669
D419h			
D41Ah			
D41Bh			
D41Ch	CAN1 Mask Register 7	C1MKR7	669
D41Dh			
D41Eh			
D41Fh			
D420h	CAN1FIFO Receive ID Compare Register 0	C1FIDCR0	670
D421h			
D422h			
D423h			
D424h	CAN1FIFO Receive ID Compare Register 1	C1FIDCR1	670
D425h			
D426h			
D427h			
D428h	CAN1 Mask Invalid Register	C1MKIVLR	672
D429h			
D42Ah			
D42Bh			
D42Ch	CAN1 Mailbox Interrupt Enable Register	C1MIER	677
D42Dh			
D42Eh			
D42Fh			
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D4A0h	CAN1 Message Control Register 0	C1MCTL0	678
D4A1h	CAN1 Message Control Register 1	C1MCTL1	678
D4A2h	CAN1 Message Control Register 2	C1MCTL2	678
D4A3h	CAN1 Message Control Register 3	C1MCTL3	678
D4A4h	CAN1 Message Control Register 4	C1MCTL4	678
D4A5h	CAN1 Message Control Register 5	C1MCTL5	678
D4A6h	CAN1 Message Control Register 6	C1MCTL6	678
D4A7h	CAN1 Message Control Register 7	C1MCTL7	678
D4A8h	CAN1 Message Control Register 8	C1MCTL8	678
D4A9h	CAN1 Message Control Register 9	C1MCTL9	678
D4AAh	CAN1 Message Control Register 10	C1MCTL10	678
D4ABh	CAN1 Message Control Register 11	C1MCTL11	678
D4ACh	CAN1 Message Control Register 12	C1MCTL12	678
D4ADh	CAN1 Message Control Register 13	C1MCTL13	678
D4AEh	CAN1 Message Control Register 14	C1MCTL14	678
D4AFh	CAN1 Message Control Register 15	C1MCTL15	678
D4B0h	CAN1 Message Control Register 16	C1MCTL16	678
D4B1h	CAN1 Message Control Register 17	C1MCTL17	678
D4B2h	CAN1 Message Control Register 18	C1MCTL18	678
D4B3h	CAN1 Message Control Register 19	C1MCTL19	678
D4B4h	CAN1 Message Control Register 20	C1MCTL20	678
D4B5h	CAN1 Message Control Register 21	C1MCTL21	678
D4B6h	CAN1 Message Control Register 22	C1MCTL22	678
D4B7h	CAN1 Message Control Register 23	C1MCTL23	678
D4B8h	CAN1 Message Control Register 24	C1MCTL24	678
D4B9h	CAN1 Message Control Register 25	C1MCTL25	678
D4BAh	CAN1 Message Control Register 26	C1MCTL26	678
D4BBh	CAN1 Message Control Register 27	C1MCTL27	678
D4BCh	CAN1 Message Control Register 28	C1MCTL28	678
D4BDh	CAN1 Message Control Register 29	C1MCTL29	678
D4BEh	CAN1 Message Control Register 30	C1MCTL30	678
D4BFh	CAN1 Message Control Register 31	C1MCTL31	678
D4C0h	CAN1 Control Register	C1CTLR	662
D4C1h			
D4C2h	CAN1 Status Register	C1STR	689
D4C3h			
D4C4h	CAN1 Bit Configuration Register	C1BCR	667
D4C5h			
D4C6h			
D4C7h	CAN1 Clock Select Register	C1CLKR	666
D4C8h	CAN1 Receive FIFO Control Register	C1RFCR	682
D4C9h	CAN1 Receive FIFO Pointer Control Register	C1RFPCR	685
D4CAh	CAN1 Transmit FIFO Control Register	C1TFCR	686
D4CBh	CAN1 Transmit FIFO Pointer Control Register	C1TFPCR	688
D4CCh	CAN1 Error Interrupt Enable Register	C1EIER	697
D4CDh	CAN1 Error Interrupt Source Judge Register	C1EIFR	699
D4CEh	CAN1 Receive Error Count Register	C1RECR	702
D4CFh	CAN1 Transmit Error Count Register	C1TECR	703
D4D0h	CAN1 Error Code Store Register	C1ECSR	704
D4D1h	CAN1 Channel Search Support Register	C1CSSR	695
D4D2h	CAN1 Mailbox Search Status Register	C1MSSR	693
D4D3h	CAN1 Mailbox Search Mode Register	C1MSMR	692
D4D4h	CAN1 Time Stamp Register	C1TSR	706
D4D5h			
D4D6h	CAN1 Acceptance Filter Support Register	C1AFSR	696
D4D7h			
D4D8h	CAN1 Test Control Register	C1TCR	707
D4D9h			
D4DAh			
D4DBh			
D4DCh			
D4DDh			
D4DEh			
D4DFh			
D4E0h to D4FFh			

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Address	Register	Symbol	Page
D500h	CAN0 Mailbox 0: Message Identifier	C0MB0	674
D501h			
D502h			
D503h			
D504h			
D505h	CAN0 Mailbox 0: Data Length		
D506h	CAN0 Mailbox 0: Data Field		
D507h			
D508h			
D509h			
D50Ah			
D50Bh			
D50Ch			
D50Dh			
D50Eh	CAN0 Mailbox 0: Time Stamp		
D50Fh			
D510h	CAN0 Mailbox 1: Message Identifier	C0MB1	674
D511h			
D512h			
D513h			
D514h			
D515h	CAN0 Mailbox 1: Data Length		
D516h	CAN0 Mailbox 1: Data Field		
D517h			
D518h			
D519h			
D51Ah			
D51Bh			
D51Ch			
D51Dh			
D51Eh	CAN0 Mailbox 1: Time Stamp		
D51Fh			
D520h	CAN0 Mailbox 2: Message Identifier	C0MB2	674
D521h			
D522h			
D523h			
D524h			
D525h	CAN0 Mailbox 2: Data Length		
D526h	CAN0 Mailbox 2: Data Field		
D527h			
D528h			
D529h			
D52Ah			
D52Bh			
D52Ch			
D52Dh			
D52Eh	CAN0 Mailbox 2: Time Stamp		
D52Fh			
D530h	CAN0 Mailbox 3: Message Identifier	C0MB3	674
D531h			
D532h			
D533h			
D534h			
D535h	CAN0 Mailbox 3: Data Length		
D536h	CAN0 Mailbox 3: Data Field		
D537h			
D538h			
D539h			
D53Ah			
D53Bh			
D53Ch			
D53Dh			
D53Eh	CAN0 Mailbox 3: Time Stamp		
D53Fh			

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D540h	CAN0 Mailbox 4: Message Identifier	C0MB4	674
D541h			
D542h			
D543h			
D544h			
D545h	CAN0 Mailbox 4: Data Length		
D546h	CAN0 Mailbox 4: Data Field		
D547h			
D548h			
D549h			
D54Ah			
D54Bh			
D54Ch			
D54Dh			
D54Eh	CAN0 Mailbox 4: Time Stamp		
D54Fh			
D550h	CAN0 Mailbox 5: Message Identifier	C0MB5	674
D551h			
D552h			
D553h			
D554h			
D555h	CAN0 Mailbox 5: Data Length		
D556h	CAN0 Mailbox 5: Data Field		
D557h			
D558h			
D559h			
D55Ah			
D55Bh			
D55Ch			
D55Dh			
D55Eh	CAN0 Mailbox 5: Time Stamp		
D55Fh			
D560h	CAN0 Mailbox 6: Message Identifier	C0MB6	674
D561h			
D562h			
D563h			
D564h			
D565h	CAN0 Mailbox 6: Data Length		
D566h	CAN0 Mailbox 6: Data Field		
D567h			
D568h			
D569h			
D56Ah			
D56Bh			
D56Ch			
D56Dh			
D56Eh	CAN0 Mailbox 6: Time Stamp		
D56Fh			
D570h	CAN0 Mailbox 7: Message Identifier	C0MB7	674
D571h			
D572h			
D573h			
D574h			
D575h	CAN0 Mailbox 7: Data Length		
D576h	CAN0 Mailbox 7: Data Field		
D577h			
D578h			
D579h			
D57Ah			
D57Bh			
D57Ch			
D57Dh			
D57Eh	CAN0 Mailbox 7: Time Stamp		
D57Fh			

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D580h	CAN0 Mailbox 8: Message Identifier	C0MB8	674
D581h			
D582h			
D583h			
D584h			
D585h	CAN0 Mailbox 8: Data Length		
D586h	CAN0 Mailbox 8: Data Field		
D587h			
D588h			
D589h			
D58Ah			
D58Bh			
D58Ch			
D58Dh			
D58Eh	CAN0 Mailbox 8: Time Stamp		
D58Fh			
D590h	CAN0 Mailbox 9: Message Identifier	C0MB9	674
D591h			
D592h			
D593h			
D594h			
D595h	CAN0 Mailbox 9: Data Length		
D596h	CAN0 Mailbox 9: Data Field		
D597h			
D598h			
D599h			
D59Ah			
D59Bh			
D59Ch			
D59Dh			
D59Eh	CAN0 Mailbox 9: Time Stamp		
D59Fh			
D5A0h	CAN0 Mailbox 10: Message Identifier	C0MB10	674
D5A1h			
D5A2h			
D5A3h			
D5A4h			
D5A5h	CAN0 Mailbox 10: Data Length		
D5A6h	CAN0 Mailbox 10: Data Field		
D5A7h			
D5A8h			
D5A9h			
D5AAh			
D5ABh			
D5ACh			
D5ADh			
D5AEh	CAN0 Mailbox 10: Time Stamp		
D5AFh			
D5B0h	CAN0 Mailbox 11: Message Identifier	C0MB11	674
D5B1h			
D5B2h			
D5B3h			
D5B4h			
D5B5h	CAN0 Mailbox 11: Data Length		
D5B6h	CAN0 Mailbox 11: Data Field		
D5B7h			
D5B8h			
D5B9h			
D5BAh			
D5BBh			
D5BCh			
D5BDh			
D5BEh	CAN0 Mailbox 11: Time Stamp		
D5BFh			

Address	Register	Symbol	Page
D5C0h	CAN0 Mailbox 12: Message Identifier	C0MB12	674
D5C1h			
D5C2h			
D5C3h			
D5C4h			
D5C5h	CAN0 Mailbox 12: Data Length		
D5C6h	CAN0 Mailbox 12: Data Field		
D5C7h			
D5C8h			
D5C9h			
D5CAh			
D5CBh			
D5CCh			
D5CDh			
D5CEh	CAN0 Mailbox 12: Time Stamp		
D5CFh			
D5D0h	CAN0 Mailbox 13: Message Identifier	C0MB13	674
D5D1h			
D5D2h			
D5D3h			
D5D4h			
D5D5h	CAN0 Mailbox 13: Data Length		
D5D6h	CAN0 Mailbox 13: Data Field		
D5D7h			
D5D8h			
D5D9h			
D5DAh			
D5DBh			
D5DCh			
D5DDh			
D5DEh	CAN0 Mailbox 13: Time Stamp		
D5DFh			
D5E0h	CAN0 Mailbox 14: Message Identifier	C0MB14	674
D5E1h			
D5E2h			
D5E3h			
D5E4h			
D5E5h	CAN0 Mailbox 14: Data Length		
D5E6h	CAN0 Mailbox 14: Data Field		
D5E7h			
D5E8h			
D5E9h			
D5EAh			
D5EBh			
D5ECh			
D5EDh			
D5EEh	CAN0 Mailbox 14: Time Stamp		
D5EFh			
D5F0h	CAN0 Mailbox 15: Message Identifier	C0MB15	674
D5F1h			
D5F2h			
D5F3h			
D5F4h			
D5F5h	CAN0 Mailbox 15: Data Length		
D5F6h	CAN0 Mailbox 15: Data Field		
D5F7h			
D5F8h			
D5F9h			
D5FAh			
D5FBh			
D5FCh			
D5FDh			
D5FEh	CAN0 Mailbox 15: Time Stamp		
D5FFh			

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Address	Register	Symbol	Page
D600h	CAN0 Mailbox 16: Message Identifier	C0MB16	674
D601h			
D602h			
D603h			
D604h			
D605h	CAN0 Mailbox 16: Data Length		
D606h	CAN0 Mailbox 16: Data Field		
D607h			
D608h			
D609h			
D60Ah			
D60Bh			
D60Ch			
D60Dh			
D60Eh	CAN0 Mailbox 16: Time Stamp		
D60Fh			
D610h	CAN0 Mailbox 17: Message Identifier	C0MB17	674
D611h			
D612h			
D613h			
D614h			
D615h	CAN0 Mailbox 17: Data Length		
D616h	CAN0 Mailbox 17: Data Field		
D617h			
D618h			
D619h			
D61Ah			
D61Bh			
D61Ch			
D61Dh			
D61Eh	CAN0 Mailbox 17: Time Stamp		
D61Fh			
D620h	CAN0 Mailbox 18: Message Identifier	C0MB18	674
D621h			
D622h			
D623h			
D624h			
D625h	CAN0 Mailbox 18: Data Length		
D626h	CAN0 Mailbox 18: Data Field		
D627h			
D628h			
D629h			
D62Ah			
D62Bh			
D62Ch			
D62Dh			
D62Eh	CAN0 Mailbox 18: Time Stamp		
D62Fh			
D630h	CAN0 Mailbox 19: Message Identifier	C0MB19	674
D631h			
D632h			
D633h			
D634h			
D635h	CAN0 Mailbox 19: Data Length		
D636h	CAN0 Mailbox 19: Data Field		
D637h			
D638h			
D639h			
D63Ah			
D63Bh			
D63Ch			
D63Dh			
D63Eh	CAN0 Mailbox 19: Time Stamp		
D63Fh			

Address	Register	Symbol	Page
D640h	CAN0 Mailbox 20: Message Identifier	C0MB20	674
D641h			
D642h			
D643h			
D644h			
D645h	CAN0 Mailbox 20: Data Length		
D646h	CAN0 Mailbox 20: Data Field		
D647h			
D648h			
D649h			
D64Ah			
D64Bh			
D64Ch			
D64Dh			
D64Eh	CAN0 Mailbox 20: Time Stamp		
D64Fh			
D650h	CAN0 Mailbox 21: Message Identifier	C0MB21	674
D651h			
D652h			
D653h			
D654h			
D655h	CAN0 Mailbox 21: Data Length		
D656h	CAN0 Mailbox 21: Data Field		
D657h			
D658h			
D659h			
D65Ah			
D65Bh			
D65Ch			
D65Dh			
D65Eh	CAN0 Mailbox 21: Time Stamp		
D65Fh			
D660h	CAN0 Mailbox 22: Message Identifier	C0MB22	674
D661h			
D662h			
D663h			
D664h			
D665h	CAN0 Mailbox 22: Data Length		
D666h	CAN0 Mailbox 22: Data Field		
D667h			
D668h			
D669h			
D66Ah			
D66Bh			
D66Ch			
D66Dh			
D66Eh	CAN0 Mailbox 22: Time Stamp		
D66Fh			
D670h	CAN0 Mailbox 23: Message Identifier	C0MB23	674
D671h			
D672h			
D673h			
D674h			
D675h	CAN0 Mailbox 23: Data Length		
D676h	CAN0 Mailbox 23: Data Field		
D677h			
D678h			
D679h			
D67Ah			
D67Bh			
D67Ch			
D67Dh			
D67Eh	CAN0 Mailbox 23: Time Stamp		
D67Fh			

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Address	Register	Symbol	Page
D680h	CAN0 Mailbox 24: Message Identifier	C0MB24	674
D681h			
D682h			
D683h			
D684h			
D685h	CAN0 Mailbox 24: Data Length		
D686h	CAN0 Mailbox 24: Data Field		
D687h			
D688h			
D689h			
D68Ah			
D68Bh			
D68Ch			
D68Dh			
D68Eh	CAN0 Mailbox 24: Time Stamp		
D68Fh			
D690h	CAN0 Mailbox 25: Message Identifier	C0MB25	674
D691h			
D692h			
D693h			
D694h			
D695h	CAN0 Mailbox 25: Data Length		
D696h	CAN0 Mailbox 25: Data Field		
D697h			
D698h			
D699h			
D69Ah			
D69Bh			
D69Ch			
D69Dh			
D69Eh	CAN0 Mailbox 25: Time Stamp		
D69Fh			
D6A0h	CAN0 Mailbox 26: Message Identifier	C0MB26	674
D6A1h			
D6A2h			
D6A3h			
D6A4h			
D6A5h	CAN0 Mailbox 26: Data Length		
D6A6h	CAN0 Mailbox 26: Data Field		
D6A7h			
D6A8h			
D6A9h			
D6AAh			
D6ABh			
D6ACh			
D6ADh			
D6AEh	CAN0 Mailbox 26: Time Stamp		
D6AFh			
D6B0h	CAN0 Mailbox 27: Message Identifier	C0MB27	674
D6B1h			
D6B2h			
D6B3h			
D6B4h			
D6B5h	CAN0 Mailbox 27: Data Length		
D6B6h	CAN0 Mailbox 27: Data Field		
D6B7h			
D6B8h			
D6B9h			
D6BAh			
D6BBh			
D6BCh			
D6BDh			
D6BEh	CAN0 Mailbox 27: Time Stamp		
D6BFh			

Address	Register	Symbol	Page
D6C0h	CAN0 Mailbox 28: Message Identifier	C0MB28	674
D6C1h			
D6C2h			
D6C3h			
D6C4h			
D6C5h	CAN0 Mailbox 28: Data Length		
D6C6h	CAN0 Mailbox 28: Data Field		
D6C7h			
D6C8h			
D6C9h			
D6CAh			
D6CBh			
D6CCh			
D6CDh			
D6CEh	CAN0 Mailbox 28: Time Stamp		
D6CFh			
D6D0h	CAN0 Mailbox 29: Message Identifier	C0MB29	674
D6D1h			
D6D2h			
D6D3h			
D6D4h			
D6D5h	CAN0 Mailbox 29: Data Length		
D6D6h	CAN0 Mailbox 29: Data Field		
D6D7h			
D6D8h			
D6D9h			
D6DAh			
D6DBh			
D6DCh			
D6DDh			
D6DEh	CAN0 Mailbox 29: Time Stamp		
D6DFh			
D6E0h	CAN0 Mailbox 30: Message Identifier	C0MB30	674
D6E1h			
D6E2h			
D6E3h			
D6E4h			
D6E5h	CAN0 Mailbox 30: Data Length		
D6E6h	CAN0 Mailbox 30: Data Field		
D6E7h			
D6E8h			
D6E9h			
D6EAh			
D6EBh			
D6ECh			
D6EDh			
D6EEh	CAN0 Mailbox 30: Time Stamp		
D6EFh			
D6F0h	CAN0 Mailbox 31: Message Identifier	C0MB31	674
D6F1h			
D6F2h			
D6F3h			
D6F4h			
D6F5h	CAN0 Mailbox 31: Data Length		
D6F6h	CAN0 Mailbox 31: Data Field		
D6F7h			
D6F8h			
D6F9h			
D6FAh			
D6FBh			
D6FCh			
D6FDh			
D6FEh	CAN0 Mailbox 31: Time Stamp		
D6FFh			

The blank areas are reserved. No access is allowed.

Address	Register	Symbol	Page
D700h	CAN0 Mask Register 0	C0MKR0	669
D701h			
D702h			
D703h			
D704h	CAN0 Mask Register 1	C0MKR1	669
D705h			
D706h			
D707h			
D708h	CAN0 Mask Register 2	C0MKR2	669
D709h			
D70Ah			
D70Bh			
D70Ch	CAN0 Mask Register 3	C0MKR3	669
D70Dh			
D70Eh			
D70Fh			
D710h	CAN0 Mask Register 4	C0MKR4	669
D711h			
D712h			
D713h			
D714h	CAN0 Mask Register 5	C0MKR5	669
D715h			
D716h			
D717h			
D718h	CAN0 Mask Register 6	C0MKR6	669
D719h			
D71Ah			
D71Bh			
D71Ch	CAN0 Mask Register 7	C0MKR7	669
D71Dh			
D71Eh			
D71Fh			
D720h	CAN0 FIFO Receive ID Compare Register 0	C0FIDCR0	670
D721h			
D722h			
D723h			
D724h	CAN0 FIFO Receive ID Compare Register 1	C0FIDCR1	670
D725h			
D726h			
D727h			
D728h	CAN0 Mask Invalid Register	C0MKIVLR	672
D729h			
D72Ah			
D72Bh			
D72Ch	CAN0 Mailbox Interrupt Enable Register	C0MIER	677
D72Dh			
D72Eh			
D72Fh			
D730h to D79Fh			
D7A0h	CAN0 Message Control Register 0	C0MCTL0	678
D7A1h	CAN0 Message Control Register 1	C0MCTL1	678
D7A2h	CAN0 Message Control Register 2	C0MCTL2	678
D7A3h	CAN0 Message Control Register 3	C0MCTL3	678
D7A4h	CAN0 Message Control Register 4	C0MCTL4	678
D7A5h	CAN0 Message Control Register 5	C0MCTL5	678
D7A6h	CAN0 Message Control Register 6	C0MCTL6	678
D7A7h	CAN0 Message Control Register 7	C0MCTL7	678
D7A8h	CAN0 Message Control Register 8	C0MCTL8	678
D7A9h	CAN0 Message Control Register 9	C0MCTL9	678
D7AAh	CAN0 Message Control Register 10	C0MCTL10	678
D7ABh	CAN0 Message Control Register 11	C0MCTL11	678
D7ACh	CAN0 Message Control Register 12	C0MCTL12	678
D7ADh	CAN0 Message Control Register 13	C0MCTL13	678
D7AEh	CAN0 Message Control Register 14	C0MCTL14	678
D7AFh	CAN0 Message Control Register 15	C0MCTL15	678

Address	Register	Symbol	Page
D7B0h	CAN0 Message Control Register 16	C0MCTL16	678
D7B1h	CAN0 Message Control Register 17	C0MCTL17	678
D7B2h	CAN0 Message Control Register 18	C0MCTL18	678
D7B3h	CAN0 Message Control Register 19	C0MCTL19	678
D7B4h	CAN0 Message Control Register 20	C0MCTL20	678
D7B5h	CAN0 Message Control Register 21	C0MCTL21	678
D7B6B	CAN0 Message Control Register 22	C0MCTL22	678
D7B7h	CAN0 Message Control Register 23	C0MCTL23	678
D7B8h	CAN0 Message Control Register 24	C0MCTL24	678
D7B9h	CAN0 Message Control Register 25	C0MCTL25	678
D7BAh	CAN0 Message Control Register 26	C0MCTL26	678
D7BBh	CAN0 Message Control Register 27	C0MCTL27	678
D7BCh	CAN0 Message Control Register 28	C0MCTL28	678
D7BDh	CAN0 Message Control Register 29	C0MCTL29	678
D7BEh	CAN0 Message Control Register 30	C0MCTL30	678
D7BFh	CAN0 Message Control Register 31	C0MCTL31	678
D7C0h	CAN0 Control Register	C0CTLR	662
D7C1h			
D7C2h	CAN0 Status Register	C0STR	689
D7C3h			
D7C4h	CAN0 Bit Configuration Register	C0BCR	667
D7C5h			
D7C6h			
D7C7h	CAN0 Clock Select Register	C0CLKR	666
D7C8h	CAN0 Receive FIFO Control Register	C0RFCR	682
D7C9h	CAN0 Receive FIFO Pointer Control Register	C0RFPCR	685
D7CAh	CAN0 Transmit FIFO Control Register	C0TFCR	686
D7CBh	CAN0 Transmit FIFO pointer Control Register	C0TFPCR	688
D7CCh	CAN0 Error Interrupt Enable Register	C0EIER	697
D7CDh	CAN0 Error Interrupt Source Judge Register	C0EIFR	699
D7CEh	CAN0 Receive Error Count Register	C0RECR	702
D7CFh	CAN0 Transmit Error Count Register	C0TECR	703
D7D0h	CAN0 Error Code Store Register	C0ECSR	704
D7D1h	CAN0 Channel Search Support Register	C0CSSR	695
D7D2h	CAN0 Mailbox Search Status Register	C0MSSR	693
D7D3h	CAN0 Mailbox Search Mode Register	C0MSMR	692
D7D4h	CAN0 Time Stamp Register	C0TSR	706
D7D5h			
D7D6h	CAN0 Acceptance Filter Support Register	C0AFSR	696
D7D7h			
D7D8h	CAN0 Test Control Register	C0TCR	707
D7D9h			
D7DAh			
D7DBh			
D7DCh			
D7DDh			
D7DEh			
D7DFh			

The blank areas are reserved. No access is allowed.

FFFDBh	Optional Function Select Address 2	OFS2	233
FFFFFh	Optional Function Select Address 1	OFS1	232

The OFS1 and OFS2 addresses are not SFRs.

1. Overview

1.1 Features

The M16C/5M and M16C/57 Group's microcomputers (MCUs) are single-chip control units that utilize high-performance silicon gate CMOS technology with the M16C/60 Series CPU core. The M16C/5M Group and M16C/57 Group are available in 64-pin, 80-pin, and 100-pin plastic molded LQFP packages. The MCUs employ sophisticated instructions for a high level of efficiency and they are capable of executing instructions at high speed.

The MCUs have the CAN module (M16C/5M Group) and LIN module, which makes them suitable for automotive control and factory automation LAN systems. In addition, the CPU core boasts a multiplier and DMAC for high-speed operation processing which makes it adequate for controlling office equipment, home appliances, and industrial equipment.

The M16C/5M and M16C/57 Group's MCUs are a high-end microcontroller series in the M16C/5L and M16C/56 Group, featuring a single architecture as well as compatible pin assignments and peripheral functions. They have an on-chip E^2PROM emulation data flash (E^2dataFlash) which is a data flash with serial E^2PROM.

1.1.1 Applications

Automotive, car audio, factory automation LAN system, etc.

1.2 Specifications

Table 1.1 to Table 1.6 list specifications of the M16C/5M Group, M16C/57 Group.

Table 1.1 Specifications (100-pin Package) (1/2)

Item	Function	Specification
CPU	Central processing unit	M16C/60 Series CPU Core (Multiplier: 16 × 16 → 32 bits, Multiply-accumulate unit: 16 × 16 + 32 → 32 bits)) • Basic instructions: 91 • Minimum instruction execution time: • Operating mode: Single-chip mode
Memory	ROM, RAM, data flash, E^2dataFlash	See Table 1.7 to Table 1.10.
Voltage Detection	Voltage detector	• 2 voltage detect points
Clock	Clock generator	• 5 circuits (Main clock, sub clock, PLL frequency synthesizer, 125 kHz on-chip oscillator, 40 MHz on-chip oscillator) • Oscillation stop detector: Main clock oscillator stop/restart detection • Frequency divide circuit: Divide-by-1, 2, 4, 8, or 16 selectable • Low-power consumption modes: Wait mode, stop mode • Real-time clock
I/O Ports	Programmable I/O ports	• 70 CMOS inputs/outputs, a pull-up resistor selectable • N-channel open drain ports: 1
Interrupts		• Interrupt vectors: 70 • External interrupt inputs: 13 ($\overline{NMI}$, $\overline{INT}$ × 8, key input × 4) • Interrupt priority levels: 7
Watchdog Timer		• 15 bits × 1 (with prescaler) • Automatic reset start function selectable • Dedicated 125 kHz on-chip oscillator for the watchdog timer contained
DMA	DMAC	• 4 channels, Cycle-steal transfer mode • Trigger sources: 50 • Transfer modes: 2 (single transfer, repeat transfer)
Timers	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse-width modulation (PWM) mode Two-phase pulse signal processing in event counter mode (two-phase encoder input) × 3 Programmable output mode × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse frequency measurement mode, pulse-width measurement mode
	Timer function for three-phase motor control	Three-phase motor control timer × 1 (timers A1, A2, A4, and B2 used) On-chip dead time timer
	Timer S (Input capture/ output compare)	• 16-bit timer × 1 (base timer) • I/O: 8 channels
	Task monitoring timer	16-bit timer × 1 channel
	Real-time clock	Count: seconds, minutes, hours, weeks
Serial Interface	UART0 to UART4	4 channels (UART, clock synchronous serial interface) 1 channels (UART, clock synchronous serial interface, I^2C-bus, IEBus)
Multi-master I^2C-bus Interface		1 channel
A/D Converter		10-bit resolution × 26 channels
D/A Converter		8-bit resolution × 1 channel

Table 1.2 Specifications (100-pin Package) (2/2)

Item	Function	Specification
CRC Calculator		• 1 circuit • CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant • MSB/LSB selectable
Serial Bus Interface		1 channel • Clock synchronous serial communication mode • 4-wire bus communication mode • Programmable character length: 8 to 16 bits
LIN Module		1 channel
CAN Module		32-slot message buffer × 2 channels or 1 channel (M16C/5M Group) (1)
Flash Memory		• Programming and erasure supply voltage: 3.0 to 5.5 V • Programming and erasure endurance: 1,000 times (program ROM 1, program ROM 2)/10,000 times (data flash) • Program security: ROM code protect, ID code check
E^2dataFlash		Programming and erasure endurance: 100,000 (1)
Debug Functions		On-board flash rewrite function, address match × 4
Operating Frequency/Power Supply Voltage		32 MHz / 3.0 to 5.5 V
Current Consumption		Described in 31. “Electrical Characteristics”
Operating Temperature		-40°C to 85°C -40°C to 125°C (1)
Package		100-pin plastic mold LQFP: PLQP0100KB-A (Previous package code: 100P6Q-A)

Note:

1. Refer to Table 1.7 “M16C/5M Group Product List (J-Version)” to Table 1.10 “M16C/57 Group Product List (K-Version) for Operating Temperature, CAN Module, and E^2dataFlash.

Table 1.3 Specifications (80-pin Package) (1/2)

Item	Function	Specification
CPU	Central processing unit	M16C/60 Series CPU Core (Multiplier: 16 × 16 → 32 bits, Multiply-accumulate unit: 16 × 16 + 32 → 32 bits)) • Basic instructions: 91 • Minimum instruction execution time: • Operating mode: Single-chip mode
Memory	ROM, RAM, data flash, E2dataFlash	See Table 1.7 to Table 1.10.
Voltage Detection	Voltage detector	• 2 voltage detect points
Clock	Clock generator	• 5 circuits (Main clock, sub clock, PLL frequency synthesizer, 125 kHz on-chip oscillator, 40 MHz on-chip oscillator) • Oscillation stop detector: Main clock oscillator stop/restart detection • Frequency divide circuit: Divide-by-1, 2, 4, 8, or 16 selectable • Low-power consumption modes: Wait mode, stop mode • Real-time clock
I/O Ports	Programmable I/O ports	• 70 CMOS inputs/outputs, a pull-up resistor selectable • N-channel open drain ports: 1
Interrupts		• Interrupt vectors: 70 • External interrupt inputs: 11 ($\overline{NMI}$, $\overline{INT}$ × 6, key input × 4) • Interrupt priority levels: 7
Watchdog Timer		• 15 bits × 1 (with prescaler) • Automatic reset start function selectable • Dedicated 125 kHz on-chip oscillator for the watchdog timer contained
DMA	DMAC	• 4 channels, Cycle-steal transfer mode • Trigger sources: 43 • Transfer modes: 2 (single transfer, repeat transfer)
Timers	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse-width modulation (PWM) mode Two-phase pulse signal processing in event counter mode (two-phase encoder input) × 3 Programmable output mode × 3
	Timer B	16-bit timer × 3 Timer mode, event counter mode, pulse frequency measurement mode, pulse-width measurement mode
	Timer function for three-phase motor control	Three-phase motor control timer × 1 (timers A1, A2, A4, and B2 used) On-chip dead time timer
	Timer S (Input capture/ output compare)	• 16-bit timer × 1 (base timer) • I/O: 8 channels
	Task monitoring timer	16-bit timer × 1 channel
	Real-time clock	Count: seconds, minutes, hours, weeks
Serial Interface	UART0 to UART4	4 channels (UART, clock synchronous serial interface) 1 channels (UART, clock synchronous serial interface, I2C-bus, IEBus)
Multi-master I2C-bus Interface		1 channel
A/D Converter		10-bit resolution × 27 channels
D/A Converter		8-bit resolution × 1 channel

Table 1.4 Specifications (80-pin Package) (2/2)

Item	Function	Specification
CRC Calculator		• 1 circuit • CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant • MSB/LSB selectable
Serial Bus Interface		1 channel • Clock synchronous serial communication mode • 4-wire bus communication mode • Programmable character length: 8 to 16 bits
LIN Module		1 channel
CAN Module		32-slot message buffer × 2 channels or 1 channel (M16C/5M Group) (1)
Flash Memory		• Programming and erasure supply voltage: 3.0 to 5.5 V • Programming and erasure endurance: 1,000 times (program ROM 1, program ROM 2)/10,000 times (data flash) • Program security: ROM code protect, ID code check
E^2dataFlash		Programming and erasure endurance: 100,000 (1)
Debug Functions		On-board flash rewrite function, address match × 4
Operating Frequency/Power Supply Voltage		32 MHz / 3.0 to 5.5 V
Current Consumption		Described in 31. “Electrical Characteristics”
Operating Temperature		-40°C to 85°C -40°C to 125°C (1)
Package		80-pin plastic mold LQFP: PLQP0080KB-A (Previous package code: 80P6Q-A)

Note:
1. Refer to Table 1.7 “M16C/5M Group Product List (J-Version)” to Table 1.10 “M16C/57 Group Product List (K-Version) for Operating Temperature, CAN Module, and E^2dataFlash.

Table 1.5 Specifications (64-pin Package) (1/2)

Item	Function	Specification
CPU	Central processing unit	M16C/60 Series CPU Core (Multiplier: 16 × 16 → 32 bits, Multiply-accumulate unit: 16 × 16 + 32 → 32 bits)) • Basic instructions: 91 • Minimum instruction execution time: • Operating mode: Single-chip mode
Memory	ROM, RAM, data flash, E2dataFlash	See Table 1.7 to Table 1.10.
Voltage Detection	Voltage detector	• 2 voltage detect points
Clock	Clock generator	• 5 circuits (Main clock, sub clock, PLL frequency synthesizer, 125 kHz on-chip oscillator, 40 MHz on-chip oscillator) • Oscillation stop detector: Main clock oscillator stop/restart detection • Frequency divide circuit: Divide-by-1, 2, 4, 8, or 16 selectable • Low-power consumption modes: Wait mode, stop mode • Real-time clock
I/O Ports	Programmable I/O ports	• 54 CMOS inputs/outputs, a pull-up resistor selectable • N-channel open drain ports: 1
Interrupts		• Interrupt vectors: 70 • External interrupt inputs: 11 ($\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 6, key input × 4) • Interrupt priority levels: 7
Watchdog Timer		• 15 bits × 1 (with prescaler) • Automatic reset start function selectable • Dedicated 125 kHz on-chip oscillator for the watchdog timer contained
DMA	DMAC	• 4 channels, Cycle-steal transfer mode • Trigger sources: 41 • Transfer modes: 2 (single transfer, repeat transfer)
Timers	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse-width modulation (PWM) mode Two-phase pulse signal processing in event counter mode (two-phase encoder input) × 3 Programmable output mode × 3
	Timer B	16-bit timer × 3 Timer mode, event counter mode, pulse frequency measurement mode, pulse-width measurement mode
	Timer function for three-phase motor control	Three-phase motor control timer × 1 (timers A1, A2, A4, and B2 used) On-chip dead time timer
	Timer S (Input capture/ output compare)	• 16-bit timer × 1 (base timer) • I/O: 8 channels
	Task monitoring timer	16-bit timer × 1 channel
	Real-time clock	Count: seconds, minutes, hours, weeks
Serial Interface	UART0 to UART3	3 channels (UART, clock synchronous serial interface) 1 channels (UART, clock synchronous serial interface, I2C-bus, IEBus)
Multi-master I2C-bus Interface		1 channel
A/D Converter		10-bit resolution × 16 channels
D/A Converter		8-bit resolution × 1 channel

Table 1.6 Specifications (64-pin Package) (2/2)

Item	Function	Specification
CRC Calculator		• 1 circuit • CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant • MSB/LSB selectable
Serial Bus Interface		1 channel • Clock synchronous serial communication mode • 4-wire bus communication mode • Programmable character length: 8 to 16 bits
LIN Module		1 channel
CAN Module		32-slot message buffer × 2 channels or 1 channel (M16C/5M Group) (1)
Flash Memory		• Programming and erasure supply voltage: 3.0 to 5.5 V • Programming and erasure endurance: 1,000 times (program ROM 1, program ROM 2)/10,000 times (data flash) • Program security: ROM code protect, ID code check
E^2dataFlash		Programming and erasure endurance: 100,000 (1)
Debug Functions		On-board flash rewrite function, address match × 4
Operating Frequency/Power Supply Voltage		32 MHz / 3.0 to 5.5 V
Current Consumption		Described in 31. “Electrical Characteristics”
Operating Temperature		-40°C to 85°C -40°C to 125°C (1)
Package		64-pin plastic mold LQFP: PLQP0064KB-A (Previous package code: 64P6Q-A)

Note:

1. Refer to Table 1.7 “M16C/5M Group Product List (J-Version)” to Table 1.10 “M16C/57 Group Product List (K-Version) for Operating Temperature, CAN Module, and E^2dataFlash.

1.3 Product List

Table 1.7 to Table 1.10 list product informations. Figure 1.1 shows part numbers, memory sizes, and packages. Figure 1.2 shows marking drawing (top view).

Table 1.7 M16C/5M Group Product List (J-Version) As of September 2011

Part Number	ROM Capacity				RAM Capacity	CAN	Package Name	Remarks
	Program ROM 1	Program ROM 2	Data flash	E^2dataFlash				
R5F35M23JFE	96 KB	16 KB	4 KB × 2 blocks	4 KB	8 KB	1 channel	PLQP0080KB-A	Operating Temperature -40°C to 85°C
R5F35M33JFF							PLQP0064KB-A	
R5F35M73JFE				—			PLQP0080KB-A	
R5F35M83JFF							PLQP0064KB-A	
R5F35M16JFB	128 KB	16 KB	4 KB × 2 blocks	4 KB	12 KB		PLQP0100KB-A	
R5F35M26JFE							PLQP0080KB-A	
R5F35M36JFF							PLQP0064KB-A	
R5F35M66JFB				—			PLQP0100KB-A	
R5F35M76JFE							PLQP0080KB-A	
R5F35M86JFF							PLQP0064KB-A	
R5F35M1EJFB	256 KB	16 KB	4 KB × 2 blocks	4 KB	20 KB		PLQP0100KB-A	
R5F35M2EJFE							PLQP0080KB-A	
R5F35M3EJFF							PLQP0064KB-A	
R5F35M6EJFB				—			PLQP0100KB-A	
R5F35M7EJFE							PLQP0080KB-A	
R5F35M8EJFF							PLQP0064KB-A	
R5F35MB3JFE	96 KB	16 KB	4 KB × 2 blocks	4 KB	8 KB	2 channels	PLQP0080KB-A	
R5F35MC3JFF							PLQP0064KB-A	
R5F35ME3JFE				—			PLQP0080KB-A	
R5F35MF3JFF							PLQP0064KB-A	
R5F35MA6JFB	128 KB	16 KB	4 KB × 2 blocks	4 KB	12 KB		PLQP0100KB-A	
R5F35MB6JFE							PLQP0080KB-A	
R5F35MC6JFF							PLQP0064KB-A	
R5F35MD6JFB				—			PLQP0100KB-A	
R5F35ME6JFE							PLQP0080KB-A	
R5F35MF6JFF							PLQP0064KB-A	
R5F35MAEJFB	256 KB	16 KB	4 KB × 2 blocks	4 KB	20 KB		PLQP0100KB-A	
R5F35MBEJFE							PLQP0080KB-A	
R5F35MCEJFF							PLQP0064KB-A	
R5F35MDEJFB				—			PLQP0100KB-A	
R5F35MEEJFE							PLQP0080KB-A	
R5F35MFEJFF							PLQP0064KB-A	

(D): Under development
(P): Under planning

The old package names are as follows:
PLQP00100KB-A: 100P6Q-A
PLQP0080KB-A: 80P6Q-A
PLQP0064KB-A: 64P6Q-A

Table 1.8 M16C/5M Group Product List (K-Version) As of September 2011

Part Number	ROM Capacity				RAM Capacity	CAN	Package Name	Remarks
	Program ROM 1	Program ROM 2	Data flash	E^2dataFlash				
R5F35M23KFE	96 KB	16 KB	4 KB × 2 blocks	4 KB	8 KB	1 channel	PLQP0080KB-A	Operating Temperature -40°C to 125°C
R5F35M33KFF							PLQP0064KB-A	
R5F35M73KFE				—			PLQP0080KB-A	
R5F35M83KFF							PLQP0064KB-A	
R5F35M16KFB	128 KB	16 KB	4 KB × 2 blocks	4 KB	12 KB		PLQP0100KB-A	
R5F35M26KFE							PLQP0080KB-A	
R5F35M36KFF							PLQP0064KB-A	
R5F35M66KFB				—			PLQP0100KB-A	
R5F35M76KFE							PLQP0080KB-A	
R5F35M86KFF							PLQP0064KB-A	
R5F35M1EKFB	256 KB	16 KB	4 KB × 2 blocks	4 KB	20 KB		PLQP0100KB-A	
R5F35M2EKFE							PLQP0080KB-A	
R5F35M3EKFF							PLQP0064KB-A	
R5F35M6EKFB				—			PLQP0100KB-A	
R5F35M7EKFE							PLQP0080KB-A	
R5F35M8EKFF							PLQP0064KB-A	
R5F35MB3KFE	96 KB	16 KB	4 KB × 2 blocks	4 KB	8 KB	2 channels	PLQP0080KB-A	
R5F35MC3KFF							PLQP0064KB-A	
R5F35ME3KFE				—			PLQP0080KB-A	
R5F35MF3KFF							PLQP0064KB-A	
R5F35MA6KFB	128 KB	16 KB	4 KB × 2 blocks	4 KB	12 KB		PLQP0100KB-A	
R5F35MB6KFE							PLQP0080KB-A	
R5F35MC6KFF							PLQP0064KB-A	
R5F35MD6KFB				—			PLQP0100KB-A	
R5F35ME6KFE							PLQP0080KB-A	
R5F35MF6KFF							PLQP0064KB-A	
R5F35MAEKFB	256 KB	16 KB	4 KB × 2 blocks	4 KB	20 KB		PLQP0100KB-A	
R5F35MBEKFE							PLQP0080KB-A	
R5F35MCEKFF							PLQP0064KB-A	
R5F35MDEKFB				—			PLQP0100KB-A	
R5F35MEEKFE							PLQP0080KB-A	
R5F35MFEKFF							PLQP0064KB-A	

(D): Under development
(P): Under planning

The old package names are as follows:
PLQP00100KB-A: 100P6Q-A
PLQP0080KB-A: 80P6Q-A
PLQP0064KB-A: 64P6Q-A

Table 1.9 M16C/57 Group Product List (J-Version) As of September 2011

Part Number	ROM Capacity				RAM Capacity	CAN	Package Name	Remarks
	Program ROM 1	Program ROM 2	Data flash	E^2dataFlash				
R5F35723JFE	96 KB	16 KB	4 KB × 2 blocks	4 KB	8 KB	N/A	PLQP0080KB-A	Operating Temperature -40°C to 85°C
R5F35733JFF							PLQP0064KB-A	
R5F35773JFE				—			PLQP0080KB-A	
R5F35783JFF							PLQP0064KB-A	
R5F35716JFB	128 KB	16 KB	4 KB × 2 blocks	4 KB	12 KB		PLQP0100KB-A	
R5F35726JFE							PLQP0080KB-A	
R5F35736JFF							PLQP0064KB-A	
R5F35766JFB				—			PLQP0100KB-A	
R5F35776JFE							PLQP0080KB-A	
R5F35786JFF							PLQP0064KB-A	
R5F3571EJFB	256 KB	16 KB	4 KB × 2 blocks	4 KB	20 KB		PLQP0100KB-A	
R5F3572EJFE							PLQP0080KB-A	
R5F3573EJFF							PLQP0064KB-A	
R5F3576EJFB				—			PLQP0100KB-A	
R5F3577EJFE							PLQP0080KB-A	
R5F3578EJFF							PLQP0064KB-A	

(D): Under development
(P): Under planning

The old package names are as follows:
PLQP00100KB-A: 100P6Q-A
PLQP0080KB-A: 80P6Q-A
PLQP0064KB-A: 64P6Q-A

Table 1.10 M16C/57 Group Product List (K-Version) As of September 2011

Part Number	ROM Capacity				RAM Capacity	CAN	Package Name	Remarks
	Program ROM 1	Program ROM 2	Data flash	E^2dataFlash				
R5F35723KFE	96 KB	16 KB	4 KB × 2 blocks	4 KB	8 KB	N/A	PLQP0080KB-A	Operating Temperature -40°C to 125°C
R5F35733KFF							PLQP0064KB-A	
R5F35773KFE				—			PLQP0080KB-A	
R5F35783KFF							PLQP0064KB-A	
R5F35716KFB	128 KB	16 KB	4 KB × 2 blocks	4 KB	12 KB		PLQP0100KB-A	
R5F35726KFE							PLQP0080KB-A	
R5F35736KFF							PLQP0064KB-A	
R5F35766KFB				—			PLQP0100KB-A	
R5F35776KFE							PLQP0080KB-A	
R5F35786KFF							PLQP0064KB-A	
R5F3571EKFB	256 KB	16 KB	4 KB × 2 blocks	4 KB	20 KB		PLQP0100KB-A	
R5F3572EKFE							PLQP0080KB-A	
R5F3573EKFF							PLQP0064KB-A	
R5F3576EKFB				—			PLQP0100KB-A	
R5F3577EKFE							PLQP0080KB-A	
R5F3578EKFF							PLQP0064KB-A	

(D): Under development
(P): Under planning

The old package names are as follows:
PLQP00100KB-A: 100P6Q-A
PLQP0080KB-A: 80P6Q-A
PLQP0064KB-A: 64P6Q-A

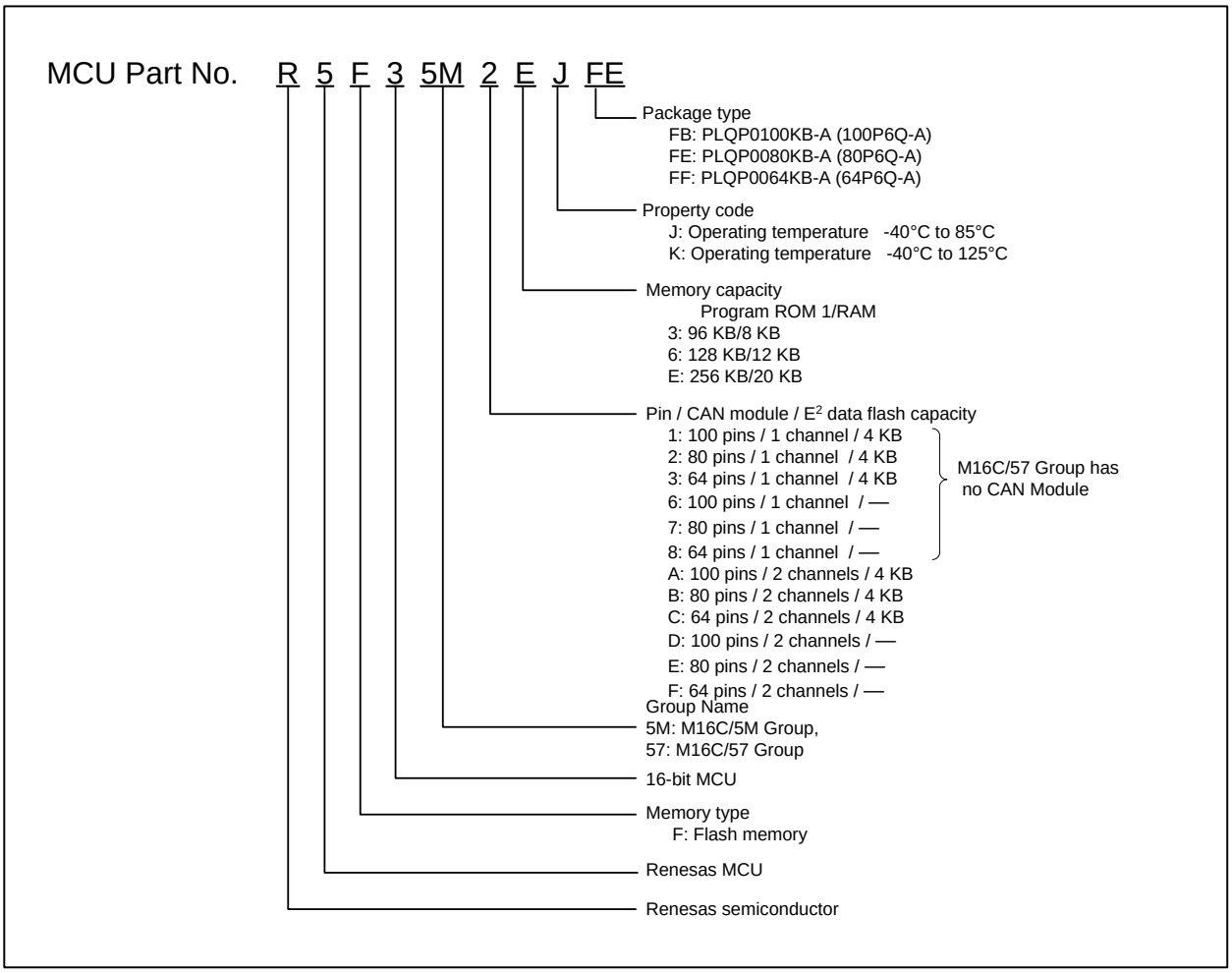


Figure 1.1 Part Number, Memory Size, and Package

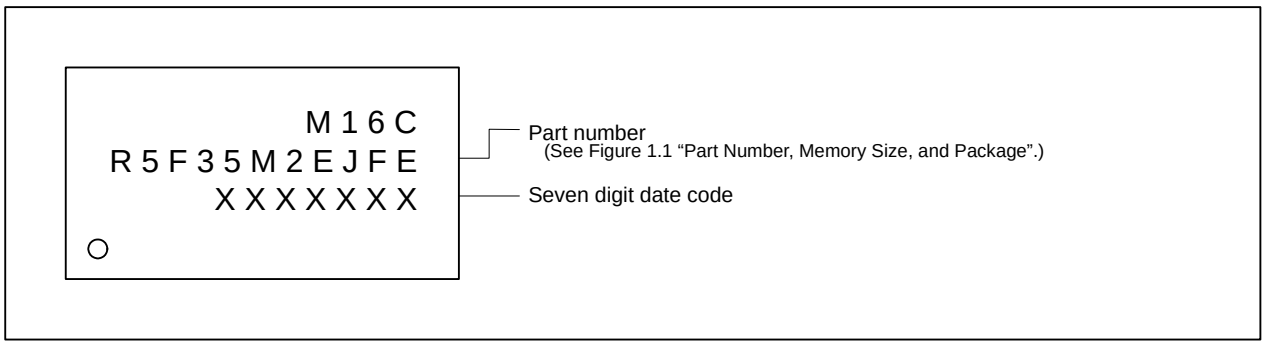
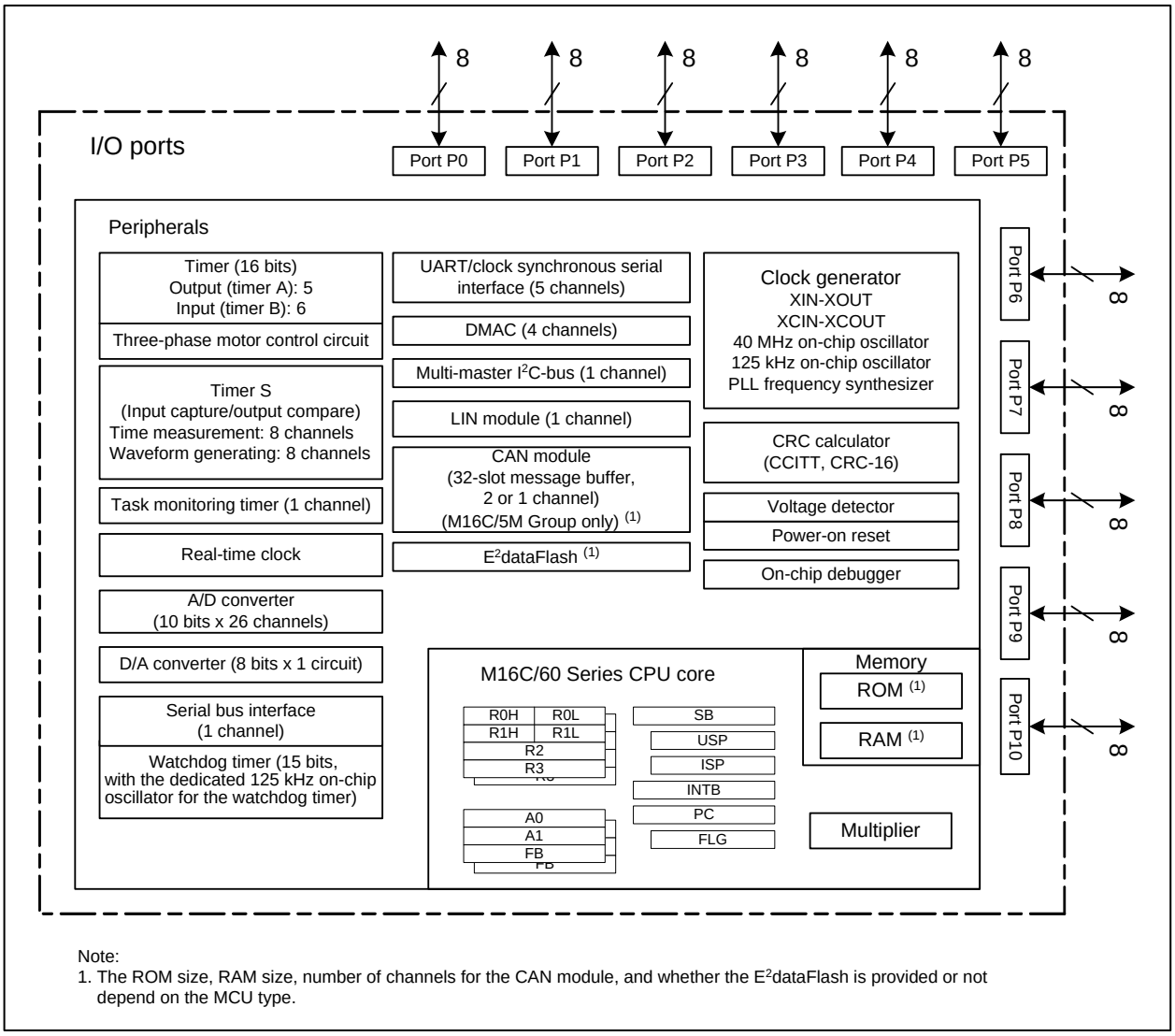


Figure 1.2 Marking Diagram of Flash Memory Version (Top View)

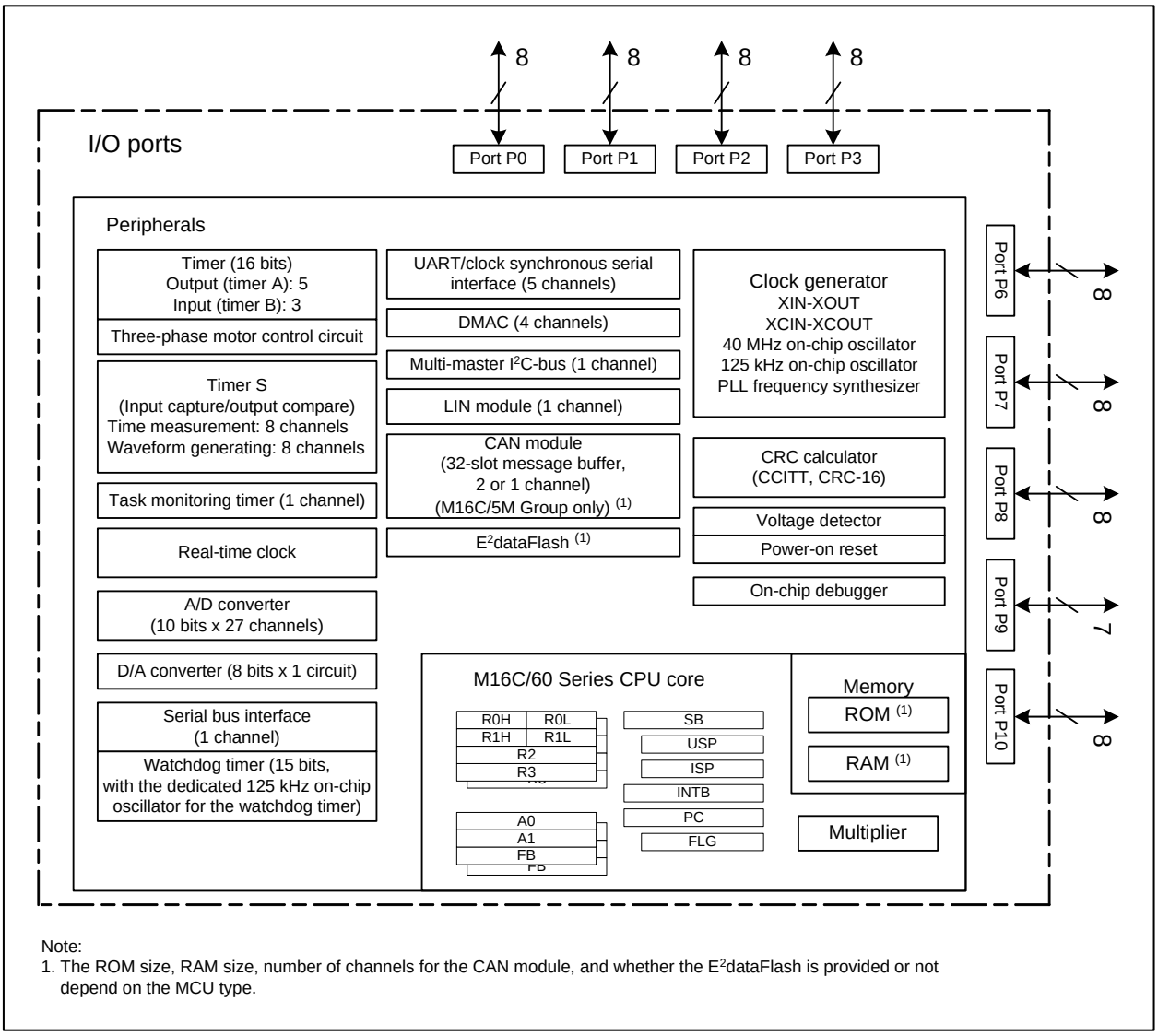
1.4 Block Diagrams

Figure 1.3 to Figure 1.5 show a block diagram of M16C/5M Group and M16C/57 Group.



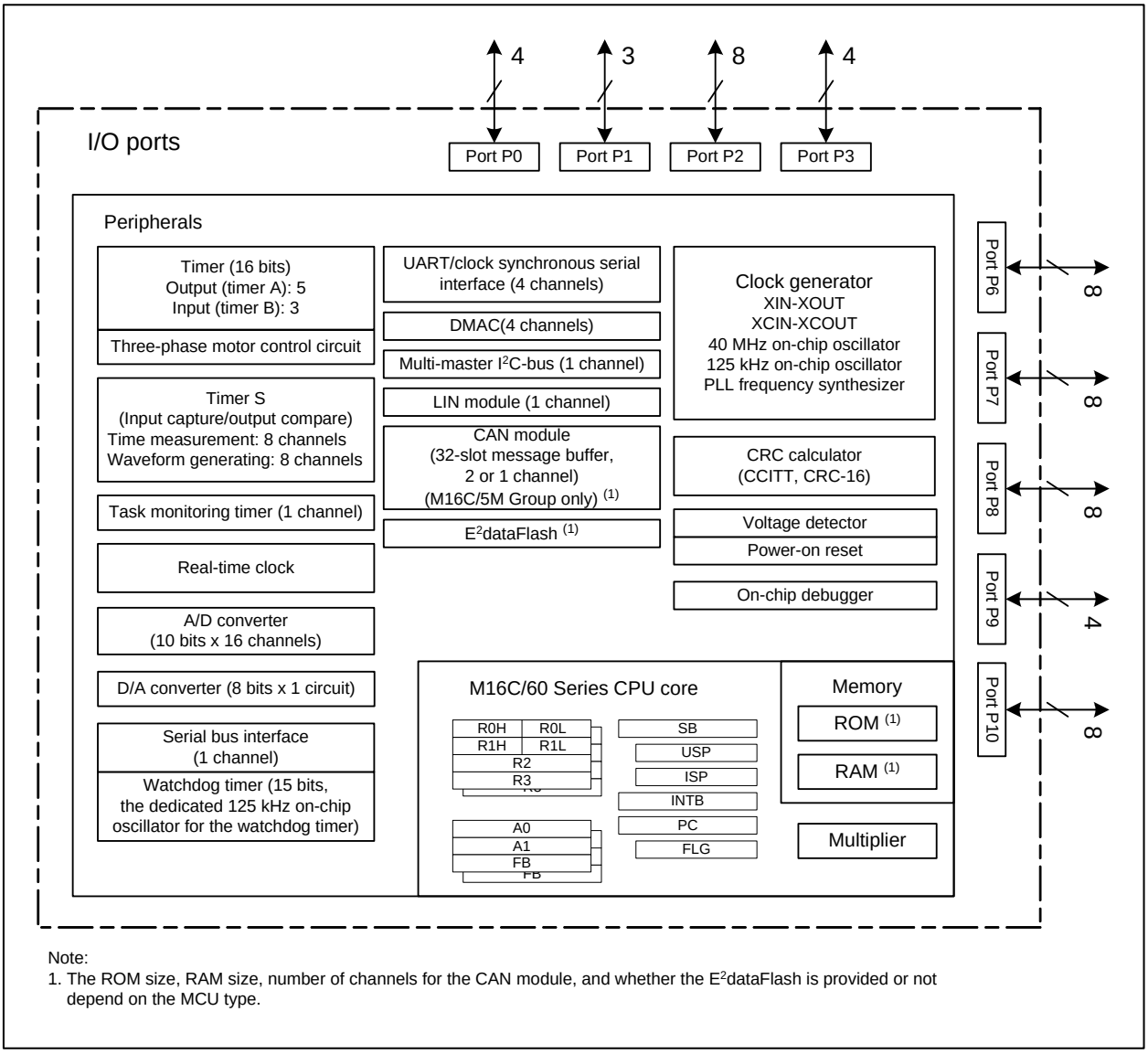
Note:
1. The ROM size, RAM size, number of channels for the CAN module, and whether the E2dataFlash is provided or not depend on the MCU type.

Figure 1.3 100-Pin Block Diagram



Note:
1. The ROM size, RAM size, number of channels for the CAN module, and whether the E2dataFlash is provided or not depend on the MCU type.

Figure 1.4 80-Pin Block Diagram

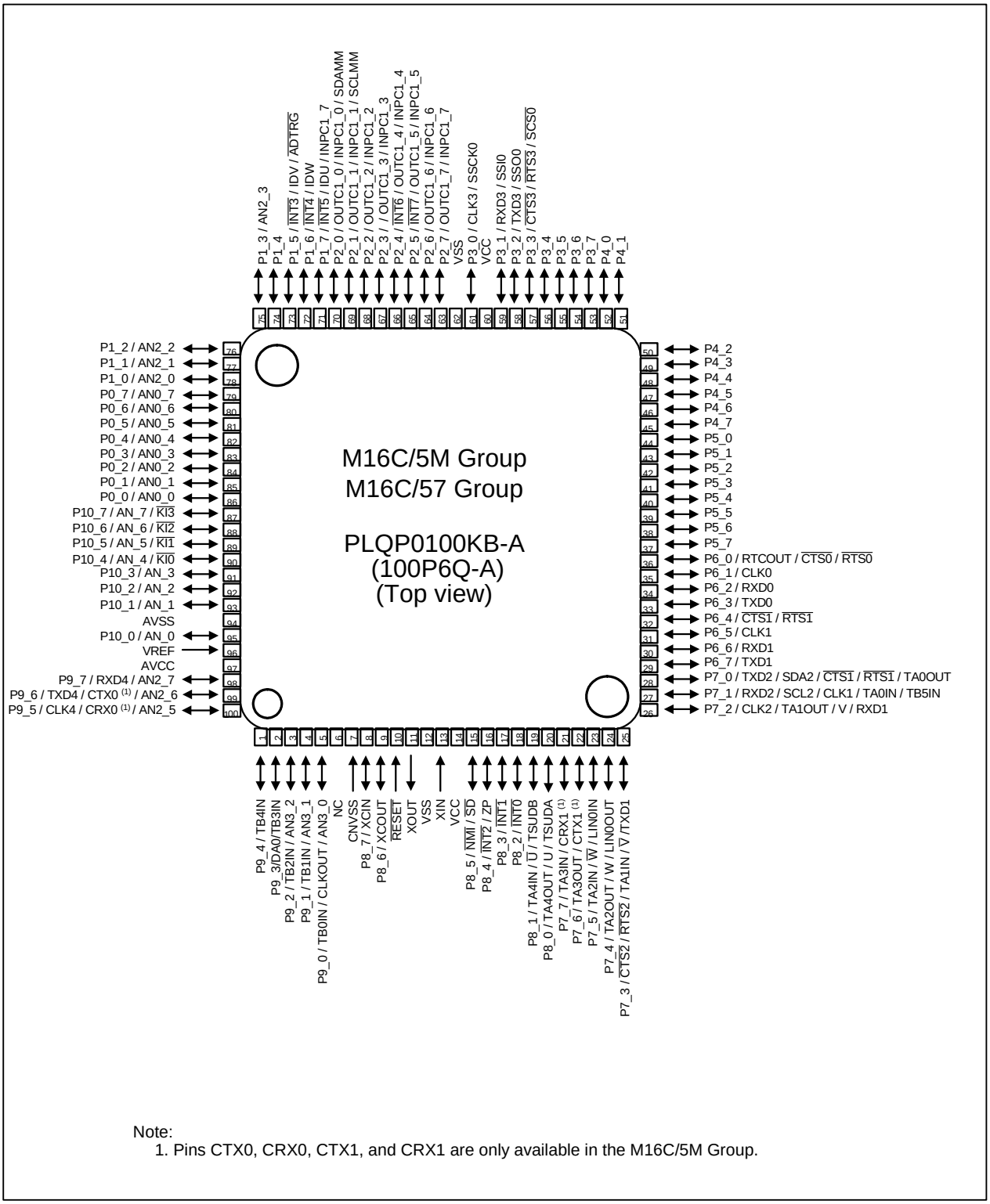


Note:
1. The ROM size, RAM size, number of channels for the CAN module, and whether the E2dataFlash is provided or not depend on the MCU type.

Figure 1.5 64-Pin Block Diagram

1.5 Pin Assignments

Figure 1.6 shows the pin assignments for the 100-pin package, Figure 1.7 shows the pin assignments for the 80-pin package, and Figure 1.8 shows the pin assignments for the 64-pin package.



Note:
1. Pins CTX0, CRX0, CTX1, and CRX1 are only available in the M16C/5M Group.

Figure 1.6 Pin Assignments for 100-Pin Package (Top View)

Set bits PACR2 to PACR0 in the PACR register to 100b before signals are input or output to individual pins after reset. When the PACR register is not set, signals are not input or output for some of the pins.

Table 1.11 Pin Names, 100-Pin Package(1/2)

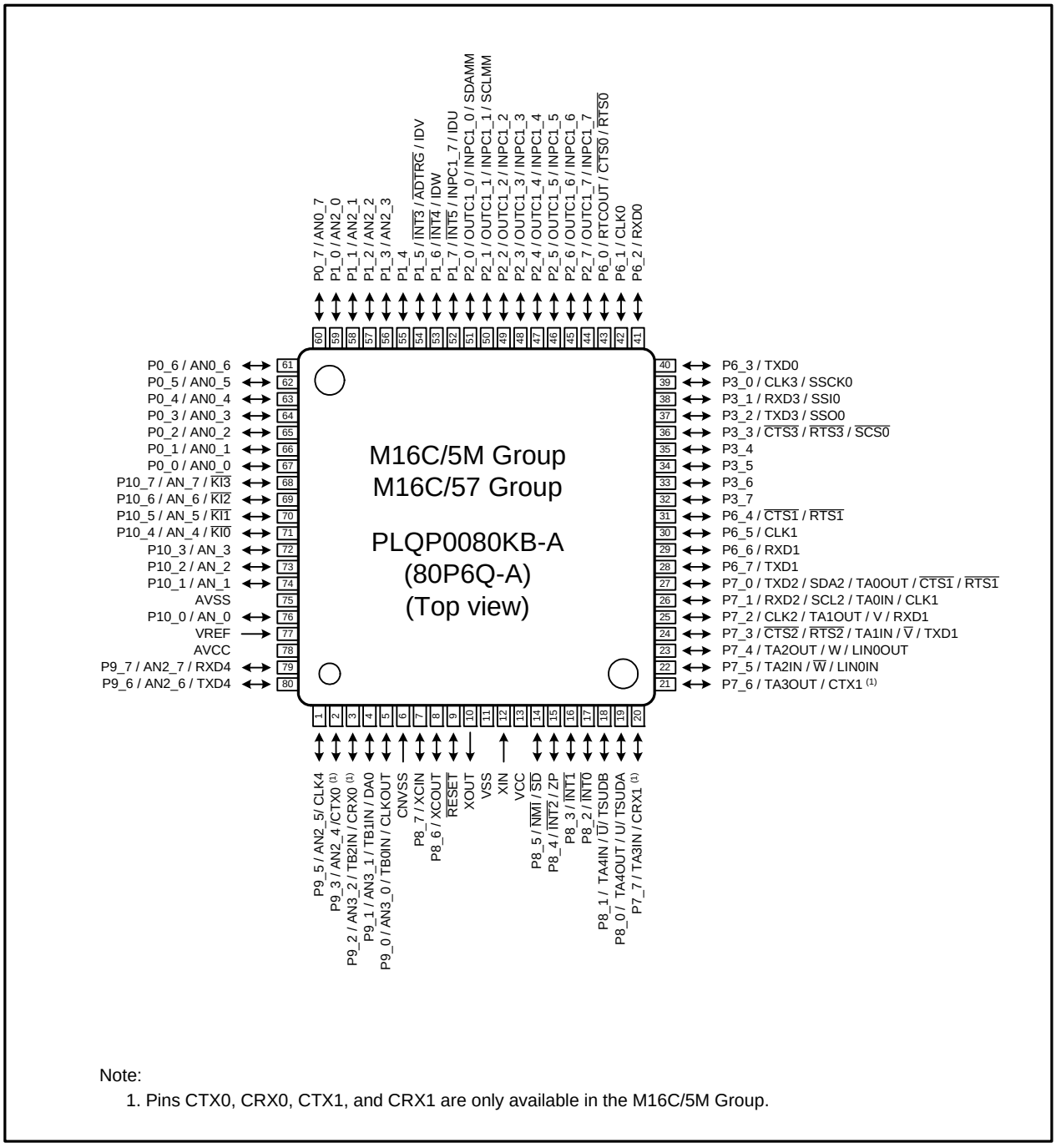
Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART/CAN/LIN/Serial Bus Interface Pin	Multi-master I²C-bus Pin	Analog Pin
1		P9_4		TB4IN				
2		P9_3		TB3IN				DA0
3		P9_2		TB2IN				AN3_2
4		P9_1		TB1IN				AN3_1
5	CLKOUT	P9_0		TB0IN				AN3_0
6	NC							
7	CNVSS							
8	XCIN	P8_7						
9	XCOUT	P8_6						
10	$\overline{\text{RESET}}$							
11	XOUT							
12	VSS							
13	XIN							
14	VCC							
15		P8_5	$\overline{\text{NMI}}$	$\overline{\text{SD}}$				
16		P8_4	$\overline{\text{INT2}}$	ZP				
17		P8_3	$\overline{\text{INT1}}$					
18		P8_2	$\overline{\text{INT0}}$					
19		P8_1		TA4IN/$\overline{\text{U}}$	TSUDB			
20		P8_0		TA4OUT/U	TSUDA			
21		P7_7		TA3IN		CRX1(1)		
22		P7_6		TA3OUT		CTX1 (1)		
23		P7_5		TA2IN/$\overline{\text{W}}$		LIN0IN		
24		P7_4		TA2OUT/W		LIN0OUT		
25		P7_3		TA1IN/$\overline{\text{V}}$		$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/TXD1		
26		P7_2		TA1OUT/V		CLK2/RXD1		
27		P7_1		TA0IN/TB5IN		RXD2/SCL2/CLK1		
28		P7_0		TA0OUT		TXD2/SDA2/$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$		
29		P6_7				TXD1		
30		P6_6				RXD1		
31		P6_5				CLK1		
32		P6_4				$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$		
33		P6_3				TXD0		
34		P6_2				RXD0		
35		P6_1				CLK0		
36		P6_0	RTCOUT			$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$		
37		P5_7						
38		P5_6						
39		P5_5						
40		P5_4						
41		P5_3						
42		P5_2						
43		P5_1						
44		P5_0						
45		P4_7						
46		P4_6						
47		P4_5						
48		P4_4						
49		P4_3						
50		P4_2						

Note:
1. There are pins CTX1 and CRX1 only in the M16C/5M Group.

Table 1.12 Pin Names, 100-Pin Package(2/2)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART/CAN/LIN/Serial Bus Interface Pin	Multi-master I²C-bus Pin	Analog Pin
51		P4_1						
52		P4_0						
53		P3_7						
54		P3_6						
55		P3_5						
56		P3_4						
57		P3_3				$\overline{CTS3}/\overline{RTS3}/\overline{SCS0}$		
58		P3_2				TXD3/SSO0		
59		P3_1				RXD3/SSI0		
60	VCC							
61		P3_0				CLK3/SSCK0		
62	VSS							
63		P2_7			OUTC1_7/INPC1_7			
64		P2_6			OUTC1_6/INPC1_6			
65		P2_5	$\overline{INT7}$		OUTC1_5/INPC1_5			
66		P2_4	$\overline{INT6}$		OUTC1_4/INPC1_4			
67		P2_3			OUTC1_3/INPC1_3			
68		P2_2			OUTC1_2/INPC1_2			
69		P2_1			OUTC1_1/INPC1_1		SCLMM	
70		P2_0			OUTC1_0/INPC1_0		SDAMM	
71		P1_7	$\overline{INT5}$	IDU	INPC1_7			
72		P1_6	$\overline{INT4}$	IDW				
73		P1_5	$\overline{INT3}$	IDV				$\overline{ADTRG}$
74		P1_4						
75		P1_3						AN2_3
76		P1_2						AN2_2
77		P1_1						AN2_1
78		P1_0						AN2_0
79		P0_7						AN0_7
80		P0_6						AN0_6
81		P0_5						AN0_5
82		P0_4						AN0_4
83		P0_3						AN0_3
84		P0_2						AN0_2
85		P0_1						AN0_1
86		P0_0						AN0_0
87		P10_7	$\overline{KI3}$					AN_7
88		P10_6	$\overline{KI2}$					AN_6
89		P10_5	$\overline{KI1}$					AN_5
90		P10_4	$\overline{KI0}$					AN_4
91		P10_3						AN_3
92		P10_2						AN_2
93		P10_1						AN_1
94	AVSS							
95		P10_0						AN_0
96	VREF							
97	AVCC							
98		P9_7				RXD4		AN2_7
99		P9_6				TXD4/CTX0 (1)		AN2_6
100		P9_5				CLK4/CRX0 (1)		AN2_5

Note:
1. Pins CTX0 and CRX0 are only available in the M16C/5M Group.



Note:
1. Pins CTX0, CRX0, CTX1, and CRX1 are only available in the M16C/5M Group.

Figure 1.7 Pin Assignment for 80-Pin Package (Top View)

Set bits PACR2 to PACR0 in the PACR register to 011b before signals are input or output to individual pins after reset. When the PACR register is not set, signals are not input or output for some of the pins.

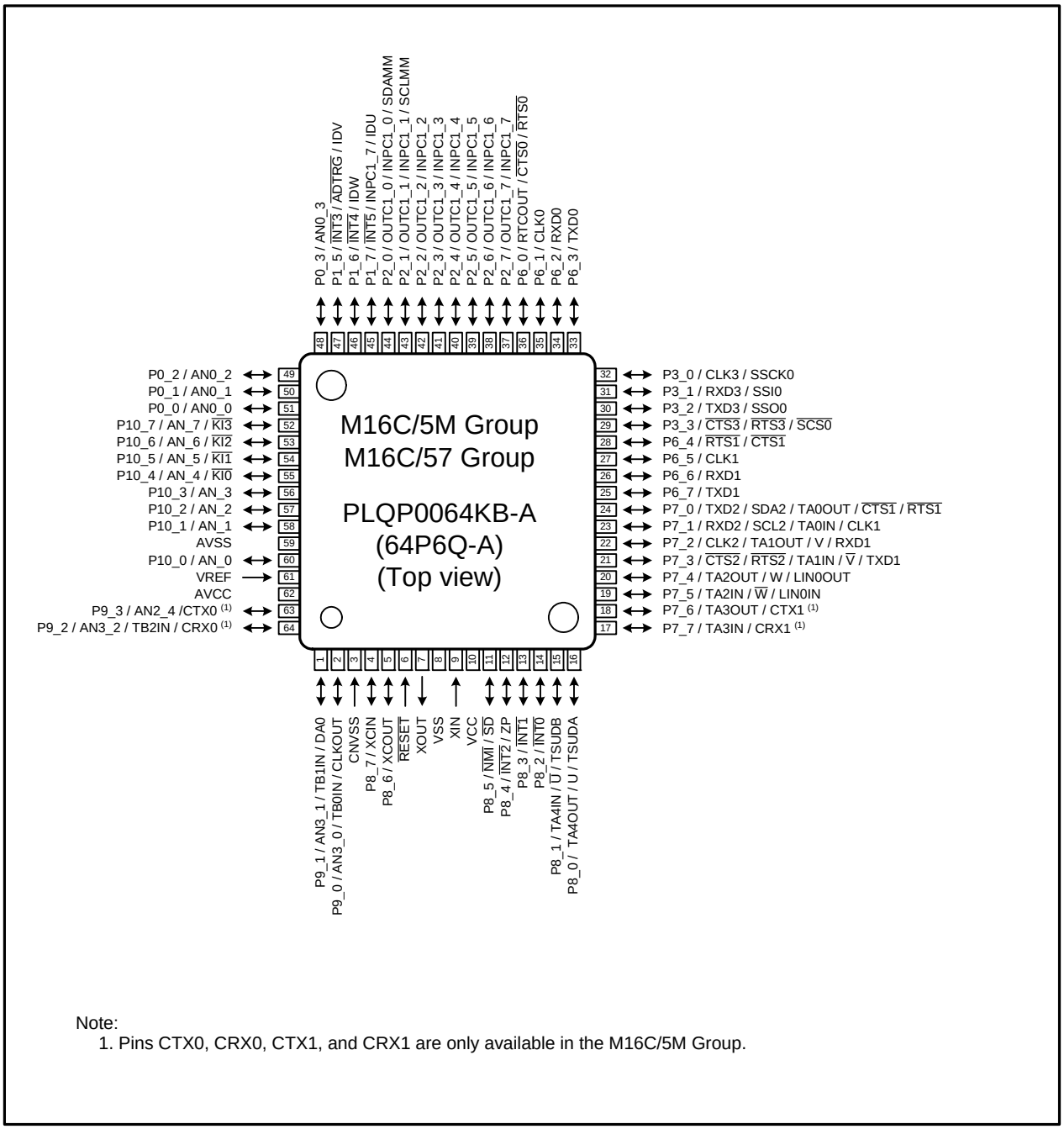
Table 1.13 Pin Names, 80-Pin Package (1/2)

Pin No.	Control pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART/CAN/LIN/Serial Bus Interface Pin	Multi-master I²C-bus pin	Analog Pin
1		P9_5				CLK4		AN2_5
2		P9_3				CTX0 (1)		AN2_4
3		P9_2		TB2IN		CRX0 (1)		AN3_2
4		P9_1		TB1IN				AN3_1/ DA0
5	CLKOUT	P9_0		TB0IN				AN3_0
6	CNVSS							
7	XCIN	P8_7						
8	XCOUT	P8_6						
9	$\overline{\text{RESET}}$							
10	XOUT							
11	VSS							
12	XIN							
13	VCC							
14		P8_5	$\overline{\text{NMI}}$	$\overline{\text{SD}}$				
15		P8_4	$\overline{\text{INT2}}$	ZP				
16		P8_3	$\overline{\text{INT1}}$					
17		P8_2	$\overline{\text{INT0}}$					
18		P8_1		TA4IN/$\overline{\text{U}}$	TSUDB			
19		P8_0		TA4OUT/U	TSUDA			
20		P7_7		TA3IN		CRX1 (1)		
21		P7_6		TA3OUT		CTX1 (1)		
22		P7_5		TA2IN/$\overline{\text{W}}$		LIN0IN		
23		P7_4		TA2OUT/W		LIN0OUT		
24		P7_3		TA1IN/$\overline{\text{V}}$		$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/TXD1		
25		P7_2		TA1OUT/V		CLK2/RXD1		
26		P7_1		TA0IN		RXD2/SCL2/CLK1		
27		P7_0		TA0OUT		TXD2/SDA2/$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$		
28		P6_7				TXD1		
29		P6_6				RXD1		
30		P6_5				CLK1		
31		P6_4				$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$		
32		P3_7						
33		P3_6						
34		P3_5						
35		P3_4						
36		P3_3				$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$/$\overline{\text{SCS0}}$		
37		P3_2				TXD3/SSO0		
38		P3_1				RXD3/SSI0		
39		P3_0				CLK3/SSCK0		
40		P6_3				TXD0		

Note:
1. Pins CTX0, CRX0, CTX1 and CRX1 are only available in the M16C/5M Group.

Table 1.14 Pin Names, 80-Pin Package (2/2)

Pin No.	Control pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART/CAN/LIN/Serial Bus Interface Pin	Multi-master I^2C-bus pin	Analog Pin
41		P6_2				RXD0		
42		P6_1				CLK0		
43		P6_0		RTCOUT		$\overline{CTS0}/\overline{RTS0}$		
44		P2_7			OUTC1_7/INPC1_7			
45		P2_6			OUTC1_6/INPC1_6			
46		P2_5			OUTC1_5/INPC1_5			
47		P2_4			OUTC1_4/INPC1_4			
48		P2_3			OUTC1_3/INPC1_3			
49		P2_2			OUTC1_2/INPC1_2			
50		P2_1			OUTC1_1/INPC1_1		SCLMM	
51		P2_0			OUTC1_0/INPC1_0		SDAMM	
52		P1_7	$\overline{INT5}$	IDU	INPC1_7			
53		P1_6	$\overline{INT4}$	IDW				
54		P1_5	$\overline{INT3}$	IDV				$\overline{ADTRG}$
55		P1_4						
56		P1_3						AN2_3
57		P1_2						AN2_2
58		P1_1						AN2_1
59		P1_0						AN2_0
60		P0_7						AN0_7
61		P0_6						AN0_6
62		P0_5						AN0_5
63		P0_4						AN0_4
64		P0_3						AN0_3
65		P0_2						AN0_2
66		P0_1						AN0_1
67		P0_0						AN0_0
68		P10_7	$\overline{KI3}$					AN_7
69		P10_6	$\overline{KI2}$					AN_6
70		P10_5	$\overline{KI1}$					AN_5
71		P10_4	$\overline{KI0}$					AN_4
72		P10_3						AN_3
73		P10_2						AN_2
74		P10_1						AN_1
75	AVSS							
76		P10_0						AN_0
77	VREF							
78	AVCC							
79		P9_7				RXD4		AN2_7
80		P9_6				TXD4		AN2_6



Note:
1. Pins CTX0, CRX0, CTX1, and CRX1 are only available in the M16C/5M Group.

Figure 1.8 Pin Assignments for 64-Pin Package (Top View)

Set bits PACR2 to PACR0 in the PACR register to 010b before signals are input or output to individual pins after reset. When the PACR register is not set, signals are not input or output for some of the pins.

Table 1.15 Pin Names, 64-Pin Package (1/2)

Pin No.	Control pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART/CAN/LIN/Serial Bus Interface Pin	Multi-master I^2C-bus Pin	Analog Pin
1		P9_1		TB1IN				AN3_1/ DA0
2	CLKOUT	P9_0		TB0IN				AN3_0
3	CNVSS							
4	XCIN	P8_7						
5	XCOUT	P8_6						
6	$\overline{\text{RESET}}$							
7	XOUT							
8	VSS							
9	XIN							
10	VCC							
11		P8_5	$\overline{\text{NMI}}$	$\overline{\text{SD}}$				
12		P8_4	$\overline{\text{INT2}}$	ZP				
13		P8_3	$\overline{\text{INT1}}$					
14		P8_2	$\overline{\text{INT0}}$					
15		P8_1		TA4IN/$\overline{\text{U}}$	TSUDB			
16		P8_0		TA4OUT/U	TSUDA			
17		P7_7		TA3IN		CRX1 (1)		
18		P7_6		TA3OUT		CTX1 (1)		
19		P7_5		TA2IN/$\overline{\text{W}}$		LIN0IN		
20		P7_4		TA2OUT/W		LIN0OUT		
21		P7_3		TA1IN/$\overline{\text{V}}$		$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/TXD1		
22		P7_2		TA1OUT/V		CLK2/RXD1		
23		P7_1		TA0IN		RXD2/SCL2/CLK1		
24		P7_0		TA0OUT		TXD2/SDA2/$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$		
25		P6_7				TXD1		
26		P6_6				RXD1		
27		P6_5				CLK1		
28		P6_4				$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$		
29		P3_3				$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$ / $\overline{\text{SCS0}}$		
30		P3_2				TXD3 / SSO0		

Note:
1. Pins CTX1 and CRX1 are only available in the M16C/5M Group.

Table 1.16 Pin Names, 64-Pin Package (2/2)

Pin No.	Control pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART/CAN/LIN/Serial Bus Interface Pin	Multi-master I^2C-bus pin	Analog Pin
31		P3_1				RXD3 / SSI0		
32		P3_0				CLK3 / SSCK0		
33		P6_3				TXD0		
34		P6_2				RXD0		
35		P6_1				CLK0		
36		P6_0		RTCOUT		$\overline{CTS0}/\overline{RTS0}$		
37		P2_7			OUTC1_7/INPC1_7			
38		P2_6			OUTC1_6/INPC1_6			
39		P2_5			OUTC1_5/INPC1_5			
40		P2_4			OUTC1_4/INPC1_4			
41		P2_3			OUTC1_3/INPC1_3			
42		P2_2			OUTC1_2/INPC1_2			
43		P2_1			OUTC1_1/INPC1_1		SCLMM	
44		P2_0			OUTC1_0/INPC1_0		SDAMM	
45		P1_7	$\overline{INT5}$	IDU	INPC1_7			
46		P1_6	$\overline{INT4}$	IDW				
47		P1_5	$\overline{INT3}$	IDV				$\overline{ADTRG}$
48		P0_3						AN0_3
49		P0_2						AN0_2
50		P0_1						AN0_1
51		P0_0						AN0_0
52		P10_7	$\overline{KI3}$					AN_7
53		P10_6	$\overline{KI2}$					AN_6
54		P10_5	$\overline{KI1}$					AN_5
55		P10_4	$\overline{KI0}$					AN_4
56		P10_3						AN_3
57		P10_2						AN_2
58		P10_1						AN_1
59	AVSS							
60		P10_0						AN_0
61	VREF							
62	AVCC							
63		P9_3				CTX0 (1)		AN2_4
64		P9_2		TB2IN		CRX0 (1)		AN3_2

Note:
1. Pins CTX0 and CRX0 are only available in the M16C/5M Group.

1.6 Pin Functions

Table 1.17 Pin Functions (64-Pin, 80-Pin, and 100-Pin Packages)

Signal Name	Pin Name	I/O	Description
Power supply	VCC, VSS	I	Apply 3.0 to 5.5 V to the VCC pin and 0 V to the VSS pin.
Analog power supply	AVCC, AVSS	I	Power supply for the A/D converter and D/A converter. Pins AVCC and AVSS should be connected to VCC and VSS, respectively.
Reset input	$\overline{\text{RESET}}$	I	Driving this pin low resets the MCU.
CNVSS	CNVSS	I	Connect to VSS via a resistor.
Main clock input	XIN	I	Input/output for the main clock oscillator. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. (1) To apply an external clock, connect it to XIN and leave XOUT open. When XIN is not used, connect XIN to VCC pin and leave XOUT open.
Main clock output	XOUT	O	
Sub clock input	XCIN	I	Input/output for the sub clock oscillator. Connect a crystal oscillator between XCIN and XCOUT. (1)
Sub clock output	XCOUT	O	
Clock output	CLKOUT	O	This pin outputs the clock having the same frequency as f1, f8, f32, or fC.
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT5}}$	I	Input for $\overline{\text{INT}}$ interrupt
$\overline{\text{NMI}}$ input	$\overline{\text{NMI}}$	I	Input for $\overline{\text{NMI}}$
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Input for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	Timers A0 to A4 input/output
	TA0IN to TA4IN	I	Timers A0 to A4 input
	ZP	I	Input for Z-phase
Timer B	TB0IN to TB2IN	I	Timers B0 to B2 input
Three-phase motor control timer	U,$\overline{\text{U}}$,V,$\overline{\text{V}}$,W,$\overline{\text{W}}$	O	Output for three-phase motor control timer
	IDU, IDW, IDV, $\overline{\text{SD}}$	I	Input for three-phase motor control timer
Real-time clock	RTCOUT	O	Output for real-time clock
Serial interface UART0 to UART3	$\overline{\text{CTS0}}$ to $\overline{\text{CTS3}}$	I	Input to control data transmission
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS3}}$	O	Output to control data reception
	CLK0 to CLK3	I/O	Transfer clock input/output
	RXD0 to RXD3	I	Serial data input
	TXD0 to TXD3	O	Serial data output
UART2 I^2C mode	SDA2	I/O	Serial data input/output
	SCL2	I/O	Transfer clock input/output
Multi-master I^2C-bus	SDAMM	I/O	Serial data input/output
	SCLMM		Transfer clock input/output

Note:
1. Please contact the manufacturer of crystal/ceramic resonator for oscillation characteristic.

Table 1.18 Pin Functions (64-Pin, 80-Pin, and 100-Pin Packages)

Signal Name	Pin Name	I/O	Description
Reference voltage input	VREF	I	Reference voltage input for the A/D converter and D/A converter.
A/D converter	AN_0 to AN_7 AN0_0 to AN0_3 AN3_0 to AN3_2	I	Analog input
	$\overline{\text{ADTRG}}$	I	Input for an external trigger
Timer S	INPC1_0 to INPC1_7	I	Input for time measurement function
	OUTC1_0 to OUTC1_7	O	Output for waveform generating function
	TSUDA, TSUDB	I	Two-phase pulse input
CAN Module (1)	CRX0, CRX1	I	Receive data input for CAN communication
	CTX0, CTX1	O	Transmit data output for CAN communication
D/A converter	DA0	O	Output for the D/A converter
LIN module	LIN0OUT	O	Transmit data output for LIN communication
	LIN0IN	I	Receive data input for LIN communication
Serial bus interface	SSO0	O	Serial data output
	SSI0	I	Serial data input
	SSCK0	I/O	Input/output for transmit/receive clock
	$\overline{\text{SCS0}}$	I	Input to control the serial interface
I/O port	P0_0 to P0_3 P1_5 to P1_7 P2_0 to P2_7 P3_0 to P3_3 P6_0 to P6_7 P7_0 to P7_7 P8_0 to P8_7 P9_0 to P9_3 P10_0 to P10_7	I/O	CMOS I/O ports. Each port has a corresponding direction register with which each pin can be set to input or output. For input ports, pull-up resistor is selectable for every unit of 4 bits. However, P8_5 output is N-channel open drain output and does not have a pull-up resistor. Port P8_5 shares the pin with $\overline{\text{NMI}}$, so that the $\overline{\text{NMI}}$ input level can be read from the P8 register P8_5 bit.

Note:
1. The CAN module is only in the M16C/5M Group.

Table 1.19 Pin Functions (100-Pin Package Only)

Signal Name	Pin Name	I/O	Description
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT6}}$ and $\overline{\text{INT7}}$	I	Input for $\overline{\text{INT}}$ interrupt
Timer B	TB3IN to TB5IN	I	Timers B3 to B5 input
I/O port	P4_0 to P4_7 P5_0 to P5_7 P9_4	I/O	CMOS I/O ports. Each port has a corresponding direction register with which each pin can be set to input or output. For input ports, pull-up resistor is selectable for every unit of 4 bits.

Table 1.20 Pin Functions (80-Pin and 64-Pin Package Only)

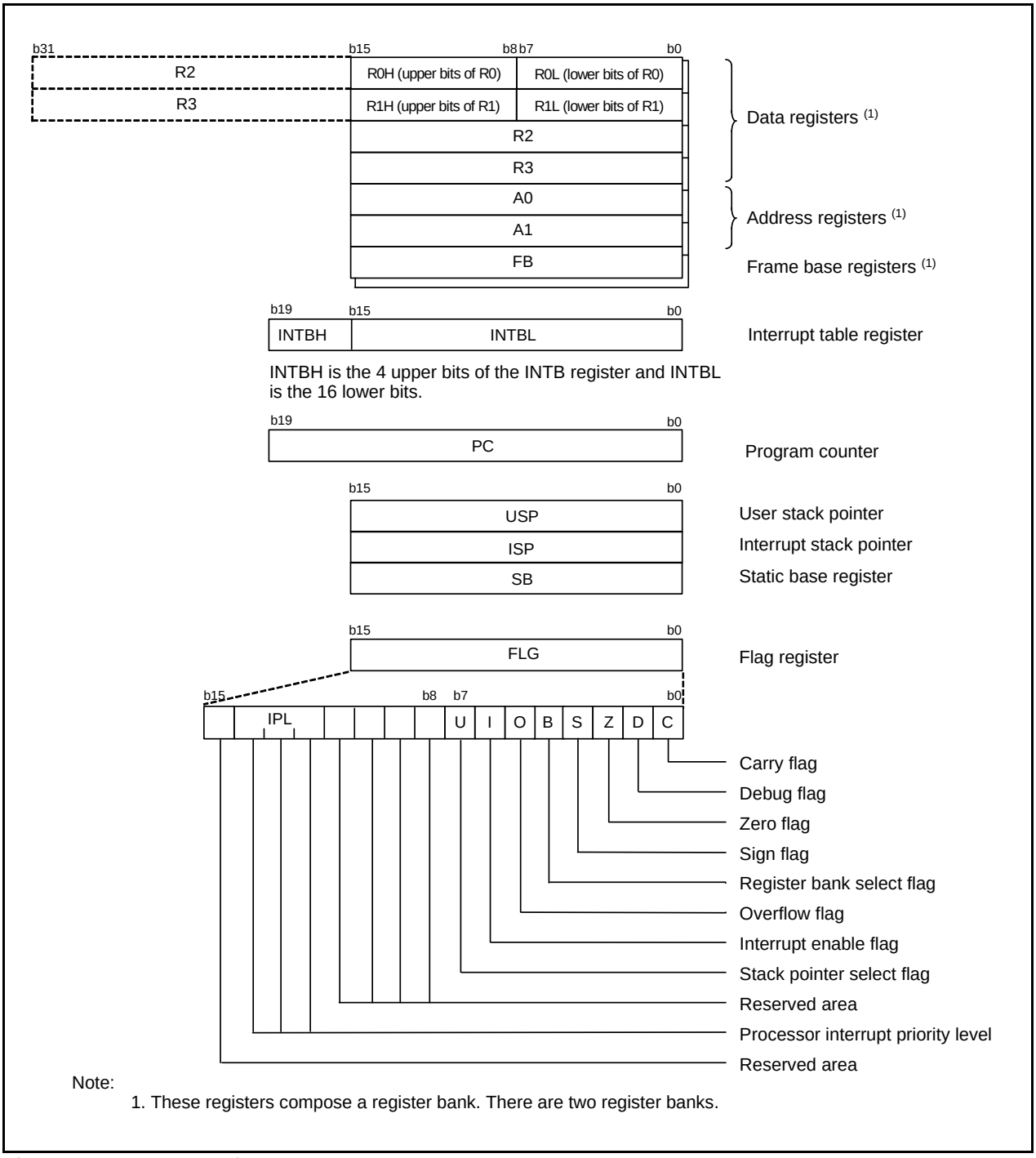
Signal Name	Pin Name	I/O	Description
A/D converter	AN2_4	I	Analog input

Table 1.21 Pin Functions (100-Pin and 80-Pin Package Only)

Signal Name	Pin Name	I/O	Description
Serial Interface UART4	CLK4	I/O	Transfer clock input/output
	RXD4	I	Serial data input
	TXD4	O	Serial data output
A/D converter	AN0_4 to AN0_7 AN2_0 to AN2_3 AN2_5 to AN2_7	I	Analog input
I/O port	P0_4 to P0_7 P1_0 to P1_4 P3_4 to P3_7 P9_5 to P9_7	I/O	CMOS I/O ports. Each port has a corresponding direction register with which each pin can be set to input or output. For input ports, Pull-up resistor is selectable for every unit of 4 bits.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. Seven registers (R0, R1, R2, R3, A0, A1, and FB) out of 13 compose a register bank, and there are two register banks.



Note:
1. These registers compose a register bank. There are two register banks.

Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0, R1, R2, and R3 are 16-bit registers used for transfer, arithmetic, and logic operations. R0 and R1 can be split into upper (R0H/R1H) and lower (R0L/R1L) bits to be used separately as 8-bit data registers. R0 can be combined with R2, and R3 can be combined with R1 and be used as 32-bit data registers R2R0 and R3R1, respectively.

2.2 Address Registers (A0 and A1)

A0 and A1 are 16-bit registers used for indirect addressing, relative addressing, transfer, arithmetic, and logic operations. A0 can be combined with A1 and used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register that is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of a relocatable interrupt vector table.

2.5 Program Counter (PC)

The PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The USP and ISP stack pointers (SP) are each comprised of 16 bits. The U flag is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register used for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register that indicates the CPU state.

2.8.1 Carry Flag (C Flag)

The C flag retains a carry, borrow, or shift-out bit generated by the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z Flag)

The Z flag becomes 1 when an arithmetic operation results in 0. Otherwise, it becomes 0.

2.8.4 Sign Flag (S Flag)

The S flag becomes 1 when an arithmetic operation results in a negative value. Otherwise, it becomes 0.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O Flag)

The O flag becomes 1 when an arithmetic operation results in an overflow. Otherwise, it becomes 0.

2.8.7 Interrupt Enable Flag (I Flag)

The I flag enables maskable interrupts.
Maskable interrupts are disabled when the I flag is 0, and enabled when it is 1. The I flag becomes 0 when an interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is 0. USP is selected when the U flag is 1.
The U flag becomes 0 when a hardware interrupt request is accepted, or the INT instruction of software interrupt number 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from 0 to 7.
If a requested interrupt has higher priority than IPL, the interrupt request is enabled.

2.8.10 Reserved Areas

Only set these bits to 0. The read value is undefined.

3. Memory

Special function registers (SFRs) are allocated from address 00000h to 003FFh and from 0D000h to 0D7FFh. Peripheral function control registers are located here. All blank spaces within SFRs are reserved, so do not access any blank spaces.

The internal RAM is allocated from address 00400h to superior direction. For example, a 8 KB internal RAM is addressed from 00400h to 023FFh. The internal RAM is used not only for data storage but also for stack area when subroutines are called or when interrupt request are acknowledged.

The internal ROM is flash memory. Four internal ROM areas are available: E^2dataFlash, data flash, program ROM 1, and program ROM 2.

The data flash is addressed from 0E000h to 0FFFFh. This data flash space is used not only for data storage but also for program storage.

Program ROM 2 is assigned addresses 10000h to 13FFFh. Program ROM 1 is assigned addresses FFFFFh to inferior direction. For example, the 64 KB program ROM 1 space has addresses F0000h to FFFFFh.

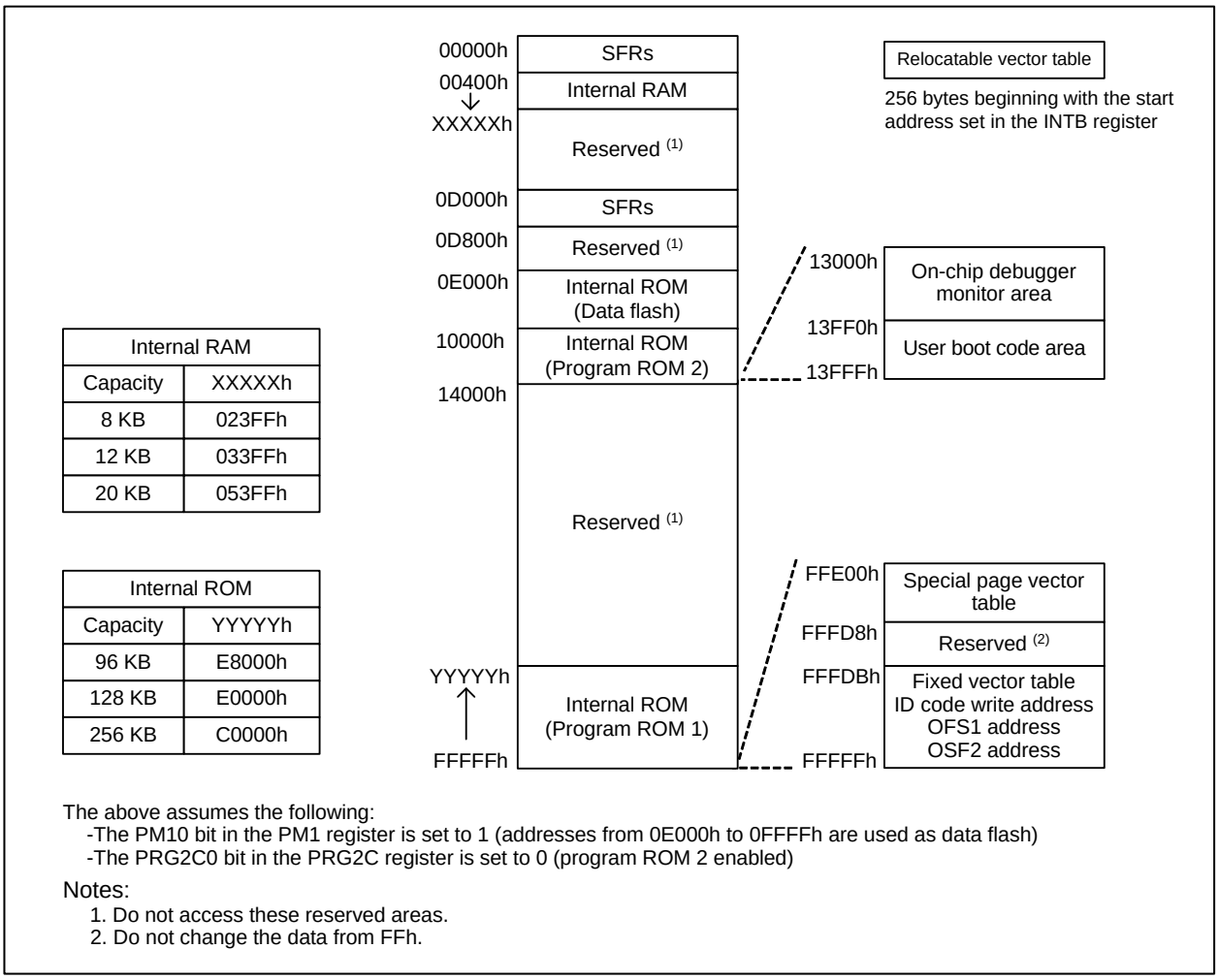
The E^2dataFlash is not shown in the memory map because the E2FA register value is used as an address.

The E^2dataFlash cannot be used for program storage. Whether the E^2dataFlash is provided or not depends on the product.

The special page vectors are assigned addresses FFE00h to FFFD7h. They are used for the JMPS instruction and JSRS instruction. Refer to the M16C/60, M16C/20, M16C/Tiny Series Software Manual for details.

The fixed vector table for interrupts, ID code write address, OFS1 address and OSF2 address are assigned addresses FFFDBh to FFFFFh.

The 256 bytes beginning with the start address set in the INTB register compose the relocatable vector table for interrupts.



Internal RAM	
Capacity	XXXXXh
8 KB	023FFh
12 KB	033FFh
20 KB	053FFh

Internal ROM	
Capacity	YYYYYh
96 KB	E8000h
128 KB	E0000h
256 KB	C0000h

The above assumes the following:
-The PM10 bit in the PM1 register is set to 1 (addresses from 0E000h to 0FFFFh are used as data flash)
-The PRG2C0 bit in the PRG2C register is set to 0 (program ROM 2 enabled)

Notes:
1. Do not access these reserved areas.
2. Do not change the data from FFh.

Figure 3.1 Memory Map

4. Special Function Registers (SFRs)

4.1 SFRs

An SFR is a control register for a peripheral function.

Table 4.1 SFR Information (1) (1)

Address	Register	Symbol	Reset Value
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	0000 1000b
0006h	System Clock Control Register 0	CM0	0100 1000b
0007h	System Clock Control Register 1	CM1	0010 0000b
0008h			
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	CM2	0X00 0010b (3)
000Dh			
000Eh			
000Fh			
0010h	Program 2 Area Control Register	PRG2C	XXXX XX00b
0011h			
0012h	Peripheral Clock Select Register	PCLKR	0000 0011b
0013h			
0014h			
0015h	Clock Prescaler Reset Flag	CPSRF	0XXX XXXXb
0016h			
0017h			
0018h	Reset Source Determine Register	RSTFR	XX0X 001Xb (hardware reset) (4)
0019h	Voltage Detector 2 Flag Register	VCR1	0000 1000b (2)
001Ah	Voltage Detector Operation Enable Register	VCR2	000X 0000b (2, 5) 001X 0000b (2, 6)
001Bh			
001Ch	PLL Control Register 0	PLC0	0X01 X010b
001Dh			
001Eh	Processor Mode Register 2	PM2	XX00 0X01b
001Fh			

X: Undefined

Notes:
1. The blank areas are reserved. No access is allowed.
2. Software reset, watchdog timer reset, oscillator stop detect reset, and voltage monitor 2 reset do not affect the following registers: registers VCR1 and VCR2.
3. Oscillator stop detect reset does not affect bits CM20, CM21, and CM27.
4. The state of bits in the RSTFR register depends on the reset type.
5. This is the reset value when the LVDAS bit of the OFS1 address is 1 during hardware reset.
6. This is the reset value after voltage monitor 0 reset, power-on reset, or when the LVDAS bit of the OFS1 address is 0 during hardware reset.

Table 4.2 SFR Information (2) (1)

Address	Register	Symbol	Reset Value
0020h			
0021h			
0022h	40 MHz On-Chip Oscillator Control Register 0	FRA0	XXXX XX00b
0023h			
0024h	40 MHz On-Chip Oscillator Control Register 2	FRA2	0XX0 X000b
0025h			
0026h	Voltage Monitor Function Select Register	VWCE	00h
0027h			
0028h	Voltage Detector 2 Level Select Register	VD2LS	0000 0100b(2)
0029h			
002Ah	Voltage Monitor 0 Control Register	VW0C	1100 1X10b(3, 4) 1100 1X11b(3, 5)
002Bh			
002Ch	Voltage Monitor 2 Control Register	VW2C	1000 0X10b(3, 6)
002Dh			
002Eh			
002Fh			
0030h			
0031h			
0032h			
0033h			
0034h			
0035h			
0036h			
0037h			
0038h			
0039h			
003Ah			
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			

X: Undefined

Notes:
1. The blank areas are reserved. No access is allowed.
2. Hardware reset, power-on reset, voltage monitor 0 reset, or voltage monitor 2 reset.
3. Software reset, watchdog timer reset, oscillator stop detect reset, voltage monitor 0 reset, and voltage monitor 2 reset do not affect the following registers or bit: the VW0C register, and bits VW2C2 and VW2C3 in the VW2C register.
4. This is the reset value when the LVDAS bit of the OFS1 address is 1 during hardware reset
5. This is the reset value after voltage monitor 0 reset, power-on reset, or when the LVDAS bit of the OFS1 address is 0 during hardware reset.
6. This is the reset value after hardware reset, power-on reset, or voltage monitor 0 reset

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	Reset Value
0040h			
0041h	E²dataFlash Interrupt Control Register	E2FIC	XXXX X000b
0042h	INT7 Interrupt Control Register Serial Bus Interface 0 Interrupt Control Register	INT7IC SS0IC	XX00 X000b
0043h	INT6 Interrupt Control Register LIN0 Interrupt Control Register	INT6IC LIN0IC	XX00 X000b
0044h	INT3 Interrupt Control Register	INT3IC	XX00 X000b
0045h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
0046h	Timer B4 Interrupt Control Register	TB4IC	XXXX X000b
0047h	Timer B3 Interrupt Control Register	TB3IC	XXXX X000b
0048h	INT5 Interrupt Control Register	INT5IC	XX00 X000b
0049h	INT4 Interrupt Control Register	INT4IC	XX00 X000b
004Ah	UART2 Bus Collision Detection Interrupt Control Register Task Monitoring Timer Interrupt Control Register	BCNIC TMOSIC	XXXX X000b
004Bh	DMA0 Interrupt Control Register	DM0IC	XXXX X000b
004Ch	DMA1 Interrupt Control Register	DM1IC	XXXX X000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXX X000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXX X000b
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXX X000b
0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXX X000b
0051h	UART0 Transmit Interrupt Control Register LIN0 Low Detection Interrupt Control Register	S0TIC L0WIC	XXXX X000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXX X000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXX X000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXX X000b
0055h	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
0058h	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
0059h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
005Ah	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
005Bh	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00 X000b
005Eh	INT1 Interrupt Control Register	INT1IC	XX00 X000b
005Fh	INT2 Interrupt Control Register	INT2IC	XX00 X000b

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	Reset Value
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h	DMA2 Interrupt Control Register	DM2IC	XXXX X000b
006Ah	DMA3 Interrupt Control Register	DM3IC	XXXX X000b
006Bh	CAN 1 Reception Complete Interrupt Control Register	C1RIC	XXXX X000b
006Ch	CAN 1 Transmission Complete Interrupt Control Register	C1TIC	XXXX X000b
006Dh	CAN 1 Receive FIFO Interrupt Control Register	C1FRIC	XXXX X000b
006Eh	CAN 1 Transmit FIFO Interrupt Control Register	C1FTIC	XXXX X000b
006Fh	UART4 Transmit Interrupt Control Register Real-Time Clock Compare Interrupt Control Register	S4TIC RTCCIC	XXXX X000b
0070h	UART4 Receive Interrupt Control Register	S4RIC	XXXX X000b
0071h	CAN0 Wake-up Interrupt Control Register	C0WIC	XXXX X000b
0072h	UART3 Transmit Interrupt Control Register CAN0 Error Interrupt Control Register	S3TIC C0EIC	XXXX X000b
0073h	UART3 Receive Interrupt Control Register CAN 1 Wake-up Interrupt Control Register	S3RIC C1WIC	XXXX X000b
0074h	Real-Time Clock Cycle Interrupt Control Register CAN 1 Error Interrupt Control Register	RTCTIC C1EIC	XXXX X000b
0075h	CAN0 Reception Complete Interrupt Control Register	C0RIC	XXXX X000b
0076h	CAN0 Transmission Complete Interrupt Control Register	C0TIC	XXXX X000b
0077h	CAN0 Receive FIFO Interrupt Control Register	C0FRIC	XXXX X000b
0078h	CAN0 Transmit FIFO Interrupt Control Register	C0FTIC	XXXX X000b
0079h	IC/OC Interrupt 0 Control Register	ICOC0IC	XXXX X000b
007Ah	IC/OC Channel 0 Interrupt Control Register	ICOCH0IC	XXXX X000b
007Bh	IC/OC Interrupt 1 Control Register I2C-bus Interface Interrupt Control Register	ICOC1IC IICIC	XXXX X000b
007Ch	IC/OC Channel 1 Interrupt Control Register SCL/SDA Interrupt Control Register	ICOCH1IC SCLDAIC	XXXX X000b
007Dh	IC/OC Channel 2 Interrupt Control Register	ICOCH2IC	XXXX X000b
007Eh	IC/OC Channel 3 Interrupt Control Register	ICOCH3IC	XXXX X000b
007Fh	IC/OC Base Timer Interrupt Control Register	BTIC	XXXX X000b

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.5 SFR Information (5) (1)

Address	Register	Symbol	Reset Value
0080h	E²dataFlash Address Register	E2FA	00h
0081h			00h
0082h			XXh
0083h			XXh
0084h			
0085h			
0086h			
0087h			
0088h	E²dataFlash Command Register	E2FI	00h
0089h			XXh
008Ah			
008Bh			
008Ch	E²dataFlash Data Register	E2FD	XXh
008Dh			XXh
008Eh			
008Fh			
0090h	E²dataFlash Mode Register	E2FM	00h
0091h			
0092h	E²dataFlash Control Register	E2FC	XXXX XXX0b
0093h			
0094h	E²dataFlash Status Register 1	E2FS1	XXXX XXX0b
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h			
00A1h	E²dataFlash Status Register 0	E2FS0	0X00 XXXXb
00A2h			
00A3h			
00A4h			
00A5h			
00A6h			
00A7h			
00A8h			
00A9h			
00AAh			
00ABh			
00ACh			
00ADh			
00AEh			
00AFh			
00B0h to 015Fh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	Reset Value
0160h			
0161h	LIN Wake-up Baud Rate Select Register	LWBR	00h
0162h	LIN Baud Rate Prescaler 0 Register	LBRP0	00h
0163h	LIN Baud Rate Prescaler 1 Register	LBRP1	00h
0164h	LIN Self-test Control Register	LSTC	00h
0165h	LIN Port Clock Control Register	LPC	00h
0166h			
0167h			
0168h	LIN0 Mode Register	L0MD	00h
0169h	LIN0 Break Field Setting Register	L0BRK	00h
016Ah	LIN0 Space Width Setting Register	L0SPC	00h
016Bh	LIN0 Wake-up Setting Register	L0WUP	00h
016Ch	LIN0 Interrupt Enable Register	L0IE	00h
016Dh	LIN0 Error Detection Enable Register	L0EDE	00h
016Eh	LIN0 Control Register	L0C	00h
016Fh			
0170h	LIN0 Transmit Control Register	L0TC	00h
0171h	LIN0 Mode Status Register	L0MST	00h
0172h	LIN0 Status Register	L0ST	00h
0173h	LIN0 Error Status Register	L0EST	00h
0174h	LIN0 Response Field Setting Register	L0RFC	00h
0175h	LIN0 ID Buffer Register	L0IDB	XXh
0176h	LIN0 Checksum Buffer Register	L0CB	XXh
0177h			
0178h	LIN0 Data 1 Buffer Register	L0DB1	XXh
0179h	LIN0 Data 2 Buffer Register	L0DB2	XXh
017Ah	LIN0 Data 3 Buffer Register	L0DB3	XXh
017Bh	LIN0 Data 4 Buffer Register	L0DB4	XXh
017Ch	LIN0 Data 5 Buffer Register	L0DB5	XXh
017Dh	LIN0 Data 6 Buffer Register	L0DB6	XXh
017Eh	LIN0 Data 7 Buffer Register	L0DB7	XXh
017Fh	LIN0 Data 8 Buffer Register	L0DB8	XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.7 SFR Information (7) (1)

Address	Register	Symbol	Reset Value
0180h	DMA0 Source Pointer	SAR0	XXh
0181h			XXh
0182h			0Xh
0183h			
0184h	DMA0 Destination Pointer	DAR0	XXh
0185h			XXh
0186h			0Xh
0187h			
0188h	DMA0 Transfer Counter	TCR0	XXh
0189h			XXh
018Ah			
018Bh			
018Ch	DMA0 Control Register	DM0CON	0000 0X00b
018Dh			
018Eh			
018Fh			
0190h	DMA1 Source Pointer	SAR1	XXh
0191h			XXh
0192h			0Xh
0193h			
0194h	DMA1 Destination Pointer	DAR1	XXh
0195h			XXh
0196h			0Xh
0197h			
0198h	DMA1 Transfer Counter	TCR1	XXh
0199h			XXh
019Ah			
019Bh			
019Ch	DMA1 Control Register	DM1CON	0000 0X00b
019Dh			
019Eh			
019Fh			
01A0h	DMA2 Source Pointer	SAR2	XXh
01A1h			XXh
01A2h			0Xh
01A3h			
01A4h	DMA2 Destination Pointer	DAR2	XXh
01A5h			XXh
01A6h			0Xh
01A7h			
01A8h	DMA2 Transfer Counter	TCR2	XXh
01A9h			XXh
01AAh			
01ABh			
01ACh	DMA2 Control Register	DM2CON	0000 0X00b
01ADh			
01AEh			
01AFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.8 SFR Information (8) (1)

Address	Register	Symbol	Reset Value
01B0h	DMA3 Source Pointer	SAR3	XXh
01B1h			XXh
01B2h			0Xh
01B3h			
01B4h	DMA3 Destination Pointer	DAR3	XXh
01B5h			XXh
01B6h			0Xh
01B7h			
01B8h	DMA3 Transfer Counter	TCR3	XXh
01B9h			XXh
01BAh			
01BBh			
01BCh	DMA3 Control Register	DM3CON	0000 0X00b
01BDh			
01BEh			
01BFh			
01C0h	Timer B0-1 Register	TB01	XXh
01C1h			XXh
01C2h	Timer B1-1 Register	TB11	XXh
01C3h			XXh
01C4h	Timer B2-1 Register	TB21	XXh
01C5h			XXh
01C6h	Pulse Period/Pulse Width Measurement Mode Function Select Register 1	PPWFS1	XXXX X000b
01C7h			
01C8h	Timer B Count Source Select Register 0	TBCS0	00h
01C9h	Timer B Count Source Select Register 1	TBCS1	X0h
01CAh			
01CBh	Timer AB Division Control Register 0	TCKDIVC0	0000 X000b
01CCh			
01CDh			
01CEh			
01CFh			
01D0h	Timer A Count Source Select Register 0	TACS0	00h
01D1h	Timer A Count Source Select Register 1	TACS1	00h
01D2h	Timer A Count Source Select Register 2	TACS2	X0h
01D3h			
01D4h	16-bit Pulse Width Modulation Mode Function Select Register	PWMFS	0XX0 X00Xb
01D5h	Timer A Waveform Output Function Select Register	TAPOFS	XXX0 0000b
01D6h			
01D7h			
01D8h	Timer A Output Waveform Change Enable Register	TAOW	XXX0 X00Xb
01D9h			
01DAh	Three-Phase Protect Control Register	TPRC	00h
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.9 SFR Information (9) (1)

Address	Register	Symbol	Reset Value
01E0h	Timer B3-1 Register	TB31	XXh
01E1h			XXh
01E2h	Timer B4-1 Register	TB41	XXh
01E3h			XXh
01E4h	Timer B5-1 Register	TB51	XXh
01E5h			XXh
01E6h	Pulse Period/Pulse Width Measurement Mode Function Select Register 2	PPWFS2	XXXX X000b
01E7h			
01E8h	Timer B Count Source Select Register 2	TBCS2	00h
01E9h	Timer B Count Source Select Register 3	TBCS3	X0h
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Task Monitor Timer Register	TMOS	XXh
01F1h			XXh
01F2h	Task Monitor Timer Count Start Flag	TMOSSR	XXXX XXX0b
01F3h	Task Monitor Timer Count Source Select Register	TMOSCS	XXXX 0000b
01F4h	Task Monitor Timer Protect Register	TMOSPR	00h
01F5h			
01F6h			
01F7h			
01F8h			
01F9h			
01FAh			
01FBh			
01FCh			
01FDh			
01FEh			
01FFh			
0200h			
0201h			
0202h			
0203h			
0204h	Interrupt Source Select Register 4	IFSR4A	00h
0205h	Interrupt Source Select Register 3	IFSR3A	00h
0206h	Interrupt Source Select Register 2	IFSR2A	00h
0207h	Interrupt Source Select Register	IFSR	00h
0208h			
0209h			
020Ah			
020Bh			
020Ch			
020Dh			
020Eh	Address Match Interrupt Enable Register	AIER	XXXX XX00b
020Fh	Address Match Interrupt Enable Register 2	AIER2	XXXX XX00b

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.10 SFR Information (10) (1)

Address	Register	Symbol	Reset Value
0210h	Address Match Interrupt Register 0	RMAD0	00h
0211h			00h
0212h			X0h
0213h			
0214h	Address Match Interrupt Register 1	RMAD1	00h
0215h			00h
0216h			X0h
0217h			
0218h	Address Match Interrupt Register 2	RMAD2	00h
0219h			00h
021Ah			X0h
021Bh			
021Ch	Address Match Interrupt Register 3	RMAD3	00h
021Dh			00h
021Eh			X0h
021Fh			
0220h	Flash Memory Control Register 0	FMR0	0000 0001b (Other than user boot mode) 0010 0001b (User boot mode)
0221h	Flash Memory Control Register 1	FMR1	00X0 XX0Xb
0222h	Flash Memory Control Register 2	FMR2	XXXX 0000b
0223h	Flash Memory Control Register 3	FMR3	XXXX 0000b
0224h			
0225h			
0226h			
0227h			
0228h			
0229h			
022Ah			
022Bh			
022Ch			
022Dh			
022Eh			
022Fh			
0230h	Flash Memory Control Register 6	FMR6	XX0X XX00b
0231h			
0232h			
0233h			
0234h			
0235h			
0236h			
0237h			
0238h			
0239h			
023Ah			
023Bh			
023Ch			
023Dh			
023Eh			
023Fh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.11 SFR Information (11) (1)

Address	Register	Symbol	Reset Value
0240h			
0241h			
0242h			
0243h			
0244h			
0245h			
0246h			
0247h			
0248h	UART0 Transmit/Receive Mode Register	U0MR	00h
0249h	UART0 Bit Rate Register	U0BRG	XXh
024Ah	UART0 Transmit Buffer Register	U0TB	XXh
024Bh			XXh
024Ch	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000b
024Dh	UART0 Transmit/Receive Control Register 1	U0C1	0000 0010b
024Eh	UART0 Receive Buffer Register	U0RB	XXh
024Fh			XXh
0250h			
0251h			
0252h	UART Clock Select Register	UCLKSEL0	X0h
0253h			
0254h			
0255h			
0256h			
0257h			
0258h	UART1 Transmit/Receive Mode Register	U1MR	00h
0259h	UART1 Bit Rate Register	U1BRG	XXh
025Ah	UART1 Transmit Buffer Register	U1TB	XXh
025Bh			XXh
025Ch	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000b
025Dh	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010b
025Eh	UART1 Receive Buffer Register	U1RB	XXh
025Fh			XXh
0260h			
0261h			
0262h			
0263h			
0264h	UART2 Special Mode Register 4	U2SMR4	00h
0265h	UART2 Special Mode Register 3	U2SMR3	000X 0X0Xb
0266h	UART2 Special Mode Register 2	U2SMR2	X000 0000b
0267h	UART2 Special Mode Register	U2SMR	X000 0000b
0268h	UART2 Transmit/Receive Mode Register	U2MR	00h
0269h	UART2 Bit Rate Register	U2BRG	XXh
026Ah	UART2 Transmit Buffer Register	U2TB	XXh
026Bh			XXh
026Ch	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000b
026Dh	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010b
026Eh	UART2 Receive Buffer Register	U2RB	XXh
026Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.12 SFR Information (12) (1)

Address	Register	Symbol	Reset Value
0270h			
0271h			
0272h			
0273h			
0274h			
0275h			
0276h			
0277h			
0278h			
0279h			
027Ah			
027Bh			
027Ch			
027Dh			
027Eh			
027Fh			
0280h			
0281h			
0282h			
0283h			
0284h			
0285h			
0286h			
0287h			
0288h			
0289h			
028Ah			
028Bh			
028Ch			
028Dh			
028Eh			
028Fh			
0290h			
0291h			
0292h			
0293h			
0294h			
0295h			
0296h			
0297h			
0298h	UART4 Transmit/Receive Mode Register	U4MR	00h
0299h	UART4 Bit Rate Register	U4BRG	XXh
029Ah	UART4 Transmit Buffer Register	U4TB	XXh
029Bh			XXh
029Ch	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000b
029Dh	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010b
029Eh	UART4 Receive Buffer Register	U4RB	XXh
029Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.13 SFR Information (13) (1)

Address	Register	Symbol	Reset Value
02A0h			
02A1h			
02A2h			
02A3h			
02A4h			
02A5h			
02A6h			
02A7h			
02A8h	UART3 Transmit/Receive Mode Register	U3MR	00h
02A9h	UART3 Bit Rate Register	U3BRG	XXh
02AAh	UART3 Transmit Buffer Register	U3TB	XXh
02ABh			XXh
02ACh	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000b
02ADh	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010b
02AEh	UART3 Receive Buffer Register	U3RB	XXh
02AFh			XXh
02B0h	I2C0 Data Shift Register	S00	XXh
02B1h			
02B2h	I2C0 Address Register 0	S0D0	0000 000Xb
02B3h	I2C0 Control Register 0	S1D0	00h
02B4h	I2C0 Clock Control Register	S20	00h
02B5h	I2C0 Start/Stop Condition Control Register	S2D0	0001 1010b
02B6h	I2C0 Control Register 1	S3D0	0011 0000b
02B7h	I2C0 Control Register 2	S4D0	00h
02B8h	I2C0 Status Register 0	S10	0001 000Xb
02B9h	I2C0 Status Register 1	S11	XXXX X000b
02BAh	I2C0 Address Register 1	S0D1	0000 000Xb
02BBh	I2C0 Address Register 2	S0D2	0000 000Xb
02BCh			
02BDh			
02BEh			
02BFh			
02C0h	Time Measurement Register 0	G1TM0	XXh
02C1h	Waveform Generation Register 0	G1PO0	XXh
02C2h	Time Measurement Register 1	G1TM1	XXh
02C3h	Waveform Generation Register 1	G1PO1	XXh
02C4h	Time Measurement Register 2	G1TM2	XXh
02C5h	Waveform Generation Register 2	G1PO2	XXh
02C6h	Time Measurement Register 3	G1TM3	XXh
02C7h	Waveform Generation Register 3	G1PO3	XXh
02C8h	Time Measurement Register 4	G1TM4	XXh
02C9h	Waveform Generation Register 4	G1PO4	XXh
02CAh	Time Measurement Register 5	G1TM5	XXh
02CBh	Waveform Generation Register 5	G1PO5	XXh
02CCh	Time Measurement Register 6	G1TM6	XXh
02CDh	Waveform Generation Register 6	G1PO6	XXh
02CEh	Time Measurement Register 7	G1TM7	XXh
02CFh	Waveform Generation Register 7	G1PO7	XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.14 SFR Information (14) (1)

Address	Register	Symbol	Reset Value
02D0h	Waveform Generation Control Register 0	G1POCR0	0X00 XX00b
02D1h	Waveform Generation Control Register 1	G1POCR1	0X00 XX00b
02D2h	Waveform Generation Control Register 2	G1POCR2	0X00 XX00b
02D3h	Waveform Generation Control Register 3	G1POCR3	0X00 XX00b
02D4h	Waveform Generation Control Register 4	G1POCR4	0X00 XX00b
02D5h	Waveform Generation Control Register 5	G1POCR5	0X00 XX00b
02D6h	Waveform Generation Control Register 6	G1POCR6	0X00 XX00b
02D7h	Waveform Generation Control Register 7	G1POCR7	0X00 XX00b
02D8h	Time Measurement Control Register 0	G1TMCR0	00h
02D9h	Time Measurement Control Register 1	G1TMCR1	00h
02DAh	Time Measurement Control Register 2	G1TMCR2	00h
02DBh	Time Measurement Control Register 3	G1TMCR3	00h
02DCh	Time Measurement Control Register 4	G1TMCR4	00h
02DDh	Time Measurement Control Register 5	G1TMCR5	00h
02DEh	Time Measurement Control Register 6	G1TMCR6	00h
02DFh	Time Measurement Control Register 7	G1TMCR7	00h
02E0h	Base Timer Register	G1BT	XXh
02E1h			XXh
02E2h	Base Timer Control Register 0	G1BCR0	00h
02E3h	Base Timer Control Register 1	G1BCR1	00h
02E4h	Time Measurement Prescaler Register 6	G1TPR6	00h
02E5h	Time Measurement Prescaler Register 7	G1TPR7	00h
02E6h	Function Enable Register	G1FE	00h
02E7h	Function Select Register	G1FS	00h
02E8h	Base Timer Reset Register	G1BTRR	XXh
02E9h			XXh
02EAh	Count Source Divide Register	G1DV	00h
02EBh			
02ECh	Waveform Output Master Enable Register	G1OER	00h
02EDh			
02EEh	Timer S I/O Control Register 0	G1IOR0	00h
02EFh	Timer S I/O Control Register 1	G1IOR1	00h
02F0h	Interrupt Request Register	G1IR	XXh
02F1h	Interrupt Enable Register 0	G1IE0	00h
02F2h	Interrupt Enable Register 1	G1IE1	00h
02F3h			
02F4h			
02F5h			
02F6h			
02F7h			
02F8h			
02F9h			
02FAh			
02FBh			
02FCh			
02FDh			
02FEh	$\overline{\text{NMI}}$ Digital Debounce Register	NDDR	FFh
02FFh	P1_7 Digital Debounce Register	P17DDR	FFh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.15 SFR Information (15) (1)

Address	Register	Symbol	Reset Value
0300h	Timer B3/B4/B5 Count Start Flag	TBSR	000X XXXXb
0301h			
0302h	Timer A1-1 Register	TA11	XXh
0303h			XXh
0304h	Timer A2-1 Register	TA21	XXh
0305h			XXh
0306h	Timer A4-1 Register	TA41	XXh
0307h			XXh
0308h	Three-Phase PWM Control Register 0	INVC0	00h
0309h	Three-Phase PWM Control Register 1	INVC1	00h
030Ah	Three-Phase Output Buffer Register 0	IDB0	XX11 1111b
030Bh	Three-Phase Output Buffer Register 1	IDB1	XX11 1111b
030Ch	Dead Time Timer	DTT	XXh
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XXh
030Eh	Position-Data-Retain Function Control Register	PDRF	XXXX 0000b
030Fh			
0310h	Timer B3 Register	TB3	XXh
0311h			XXh
0312h	Timer B4 Register	TB4	XXh
0313h			XXh
0314h	Timer B5 Register	TB5	XXh
0315h			XXh
0316h			
0317h			
0318h	Port Function Control Register	PFCR	0011 1111b
0319h			
031Ah			
031Bh	Timer B3 Mode Register	TB3MR	00XX 0000b
031Ch	Timer B4 Mode Register	TB4MR	00XX 0000b
031Dh	Timer B5 Mode Register	TB5MR	00XX 0000b
031Eh			
031Fh			
0320h	Count Start Flag	TABSR	00h
0321h			
0322h	One-Shot Start Flag	ONSF	00h
0323h	Trigger Select Register	TRGSR	00h
0324h	Increment/Decrement Flag	UDF	00h
0325h			
0326h	Timer A0 Register	TA0	XXh
0327h			XXh
0328h	Timer A1 Register	TA1	XXh
0329h			XXh
032Ah	Timer A2 Register	TA2	XXh
032Bh			XXh
032Ch	Timer A3 Register	TA3	XXh
032Dh			XXh
032Eh	Timer A4 Register	TA4	XXh
032Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.16 SFR Information (16) (1)

Address	Register	Symbol	Reset Value
0330h	Timer B0 Register	TB0	XXh
0331h			XXh
0332h	Timer B1 Register	TB1	XXh
0333h			XXh
0334h	Timer B2 Register	TB2	XXh
0335h			XXh
0336h	Timer A0 Mode Register	TA0MR	00h
0337h	Timer A1 Mode Register	TA1MR	00h
0338h	Timer A2 Mode Register	TA2MR	00h
0339h	Timer A3 Mode Register	TA3MR	00h
033Ah	Timer A4 Mode Register	TA4MR	00h
033Bh	Timer B0 Mode Register	TB0MR	00XX 0000b
033Ch	Timer B1 Mode Register	TB1MR	00XX 0000b
033Dh	Timer B2 Mode Register	TB2MR	00XX 0000b
033Eh	Timer B2 Special Mode Register	TB2SC	X000 0000b
033Fh			
0340h	Real-Time Clock Second Data Register	RTCSEC	00h
0341h	Real-Time Clock Minute Data Register	RTCMIN	X000 0000b
0342h	Real-Time Clock Hour Data Register	RTCHR	XX00 0000b
0343h	Real-Time Clock Day Data Register	RTCWK	XXXX X000b
0344h	Real-Time Clock Control Register 1	RTCCR1	0000 X00Xb
0345h	Real-Time Clock Control Register 2	RTCCR2	X000 0000b
0346h	Real-Time Clock Count Source Select Register	RTCCSR	XXX0 0000b
0347h			
0348h	Real-Time Clock Second Compare Data Register	RTCCSEC	X000 0000b
0349h	Real-Time Clock Minute Compare Data Register	RTCCMIN	X000 0000b
034Ah	Real-Time Clock Hour Compare Data Register	RTCCHR	X000 0000b
034Bh			
034Ch			
034Dh			
034Eh			
034Fh			
0350h			
0351h			
0352h			
0353h	SS0 Bit Counter Register	SS0BR	1111 1000b
0354h	SS0 Transmit Data Register	SS0TDR	FFh
0355h			FFh
0356h	SS0 Receive Data Register	SS0RDR	FFh
0357h			FFh
0358h	SS0 Control Register H	SS0CRH	00h
0359h	SS0 Control Register L	SS0CRL	0111 1101b
035Ah	SS0 Mode Register	SS0MR	0001 0000b
035Bh	SS0 Enable Register	SS0ER	00h
035Ch	SS0 Status Register	SS0SR	00h
035Dh	SS0 Mode Register 2	SS0MR2	00h
035Eh			
035Fh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.17 SFR Information (17) (1)

Address	Register	Symbol	Reset Value
0360h	Pull-Up Control Register 0	PUR0	00h
0361h	Pull-Up Control Register 1	PUR1	00h
0362h	Pull-Up Control Register 2	PUR2	00h
0363h			
0364h			
0365h			
0366h	Port Control Register	PCR	0XX0 0XX0b
0367h			
0368h			
0369h			
036Ah			
036Bh			
036Ch	Input Threshold Select Register 0	VLT0	00h
036Dh	Input Threshold Select Register 1	VLT1	00h
036Eh	Input Threshold Select Register 2	VLT2	XX00 0000b
036Fh			
0370h	Pin Assignment Control Register	PACR	0XXX X000b
0371h			
0372h			
0373h			
0374h			
0375h			
0376h			
0377h			
0378h			
0379h			
037Ah			
037Bh			
037Ch	Count Source Protection Mode Register	CSPR	00h (2)
037Dh	Watchdog Timer Refresh Register	WDTR	XXh
037Eh	Watchdog Timer Start Register	WDTS	XXh
037Fh	Watchdog Timer Control Register	WDC	00XX XXXXb
0380h			
0381h			
0382h			
0383h			
0384h			
0385h			
0386h			
0387h			
0388h			
0389h			
038Ah			
038Bh			
038Ch			
038Dh			
038Eh			
038Fh			

X: Undefined

Notes:
1. The blank areas are reserved. No access is allowed.
2. When the CSPROINI bit in the OFS1 address is 0, the reset value is 1000 0000b.

Table 4.18 SFR Information (18) (1)

Address	Register	Symbol	Reset Value
0390h	DMA2 Source Select Register	DM2SL	00h
0391h			
0392h	DMA3 Source Select Register	DM3SL	00h
0393h			
0394h			
0395h			
0396h			
0397h			
0398h	DMA0 Source Select Register	DM0SL	00h
0399h			
039Ah	DMA1 Source Select Register	DM1SL	00h
039Bh			
039Ch			
039Dh			
039Eh			
039Fh			
03A0h			
03A1h			
03A2h	Open-Circuit Detection Assist Function Register	AINRST	XX00 XXXXb
03A3h			
03A4h			
03A5h			
03A6h			
03A7h			
03A8h			
03A9h			
03AAh			
03ABh			
03ACh			
03ADh			
03AEh			
03AFh			
03B0h			
03B1h			
03B2h			
03B3h			
03B4h	SFR Snoop Address Register	CRCSAR	XXXX XXXXb
03B5h			00XX XXXXb
03B6h	CRC Mode Register	CRCMR	0XXX XXX0b
03B7h			
03B8h			
03B9h			
03BAh			
03BBh			
03BCh	CRC Data Register	CRCD	XXh
03BDh			XXh
03BEh	CRC Input Register	CRCIN	XXh
03BFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.19 SFR Information (19) (1)

Address	Register	Symbol	Reset Value
03C0h	A/D Register 0	AD0	XXXX XXXXb
03C1h			0000 00XXb
03C2h	A/D Register 1	AD1	XXXX XXXXb
03C3h			0000 00XXb
03C4h	A/D Register 2	AD2	XXXX XXXXb
03C5h			0000 00XXb
03C6h	A/D Register 3	AD3	XXXX XXXXb
03C7h			0000 00XXb
03C8h	A/D Register 4	AD4	XXXX XXXXb
03C9h			0000 00XXb
03CAh	A/D Register 5	AD5	XXXX XXXXb
03CBh			0000 00XXb
03CCh	A/D Register 6	AD6	XXXX XXXXb
03CDh			0000 00XXb
03CEh	A/D Register 7	AD7	XXXX XXXXb
03CFh			0000 00XXb
03D0h			
03D1h			
03D2h			
03D3h			
03D4h	A/D Control Register 2	ADCON2	0000 X00Xb
03D5h			
03D6h	A/D Control Register 0	ADCON0	0000 0XXXb
03D7h	A/D Control Register 1	ADCON1	0000 X000b
03D8h	D/A0 Register	DA0	00h
03D9h			
03DAh			
03DBh			
03DCh	D/A Control Register	DACON	00h
03DDh			
03DEh			
03DFh			
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h	Port P4 Register	P4	XXh
03E9h	Port P5 Register	P5	XXh
03EAh	Port P4 Direction Register	PD4	00h
03EBh	Port P5 Direction Register	PD5	00h
03ECh	Port P6 Register	P6	XXh
03EDh	Port P7 Register	P7	XXh
03EEh	Port P6 Direction Register	PD6	00h
03EFh	Port P7 Direction Register	PD7	00h

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.20 SFR Information (20) (1)

Address	Register	Symbol	Reset Value
03F0h	Port P8 Register	P8	XXh
03F1h	Port P9 Register	P9	XXh
03F2h	Port P8 Direction Register	PD8	00h
03F3h	Port P9 Direction Register	PD9	00h
03F4h	Port P10 Register	P10	XXh
03F5h			
03F6h	Port P10 Direction Register	PD10	00h
03F7h			
03F8h			
03F9h			
03FAh			
03FBh			
03FCh			
03FDh			
03FEh			
03FFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.21 SFR Information (21) (1)

Address	Register	Symbol	Reset Value
D1F0h			
D1F1h			
D1F2h			
D1F3h			
D1F4h			
D1F5h			
D1F6h			
D1F7h			
D1F8h			
D1F9h			
D1FAh			
D1FBh			
D1FCh			
D1FDh			
D1FEh			
D1FFh			
D200h	CAN1 Mailbox 0: Message Identifier	C1MB0	XXh
D201h			XXh
D202h			XXh
D203h			XXh
D204h			
D205h	CAN1 Mailbox 0: Data Length		XXh
D206h	CAN1 Mailbox 0: Data Field		XXh
D207h			XXh
D208h			XXh
D209h			XXh
D20Ah			XXh
D20Bh			XXh
D20Ch			XXh
D20Dh			XXh
D20Eh	CAN1 Mailbox 0: Time Stamp		XXh
D20Fh			XXh
D210h	CAN1 Message Identifier	C1MB1	XXh
D211h			XXh
D212h			XXh
D213h			XXh
D214h			
D215h	CAN1 Mailbox 1: Data Length		XXh
D216h	CAN1 Mailbox 1: Data Field		XXh
D217h			XXh
D218h			XXh
D219h			XXh
D21Ah			XXh
D21Bh			XXh
D21Ch			XXh
D21Dh			XXh
D21Eh	CAN1 Mailbox 1: Time Stamp		XXh
D21Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.22 SFR Information (22) (1)

Address	Register	Symbol	Reset Value
D220h	CAN1 Mailbox 2: Message Identifier	C1MB2	XXh
D221h			XXh
D222h			XXh
D223h			XXh
D224h			
D225h	CAN1 Mailbox 2: Data Length		XXh
D226h	CAN1 Mailbox 2: Data Field		XXh
D227h			XXh
D228h			XXh
D229h			XXh
D22Ah			XXh
D22Bh			XXh
D22Ch			XXh
D22Dh			XXh
D22Eh	CAN1 Mailbox 2: Time Stamp		XXh
D22Fh			XXh
D230h	CAN1 Mailbox 3: Message Identifier	C1MB3	XXh
D231h			XXh
D232h			XXh
D233h			XXh
D234h			
D235h	CAN1 Mailbox 3: Data Length		XXh
D236h	CAN1 Mailbox 3: Data Field		XXh
D237h			XXh
D238h			XXh
D239h			XXh
D23Ah			XXh
D23Bh			XXh
D23Ch			XXh
D23Dh			XXh
D23Eh	CAN1 Mailbox 3: Time Stamp		XXh
D23Fh			XXh
D240h	CAN1 Mailbox 4: Message Identifier	C1MB4	XXh
D241h			XXh
D242h			XXh
D243h			XXh
D244h			
D245h	CAN1 Mailbox 4: Data Length		XXh
D246h	CAN1 Mailbox 4: Data Field		XXh
D247h			XXh
D248h			XXh
D249h			XXh
D24Ah			XXh
D24Bh			XXh
D24Ch			XXh
D24Dh			XXh
D24Eh	CAN1 Mailbox 4: Time Stamp		XXh
D24Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.23 SFR Information (23) (1)

Address	Register	Symbol	Reset Value
D250h	CAN1 Mailbox 5: Message Identifier	C1MB5	XXh
D251h			XXh
D252h			XXh
D253h			XXh
D254h			
D255h	CAN1 Mailbox 5: Data Length		XXh
D256h	CAN1 Mailbox 5: Data Field		XXh
D257h			XXh
D258h			XXh
D259h			XXh
D25Ah			XXh
D25Bh			XXh
D25Ch			XXh
D25Dh			XXh
D25Eh	CAN1 Mailbox 5: Time Stamp		XXh
D25Fh			XXh
D260h	CAN1 Mailbox 6: Message Identifier	C1MB6	XXh
D261h			XXh
D262h			XXh
D263h			XXh
D264h			
D265h	CAN1 Mailbox 6: Data Length		XXh
D266h	CAN1 Mailbox 6: Data Field		XXh
D267h			XXh
D268h			XXh
D269h			XXh
D26Ah			XXh
D26Bh			XXh
D26Ch			XXh
D26Dh			XXh
D26Eh	CAN1 Mailbox 6: Time Stamp		XXh
D26Fh			XXh
D270h	CAN1 Mailbox 7: Message Identifier	C1MB7	XXh
D271h			XXh
D272h			XXh
D273h			XXh
D274h			
D275h	CAN1 Mailbox 7: Data Length		XXh
D276h	CAN1 Mailbox 7: Data Field		XXh
D277h			XXh
D278h			XXh
D279h			XXh
D27Ah			XXh
D27Bh			XXh
D27Ch			XXh
D27Dh			XXh
D27Eh	CAN1 Mailbox 7: Time Stamp		XXh
D27Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.24 SFR Information (24) (1)

Address	Register	Symbol	Reset Value
D280h	CAN1 Mailbox 8: Message Identifier	C1MB8	XXh
D281h			XXh
D282h			XXh
D283h			XXh
D284h			
D285h	CAN1 Mailbox 8: Data Length		XXh
D286h	CAN1 Mailbox 8: Data Field		XXh
D287h			XXh
D288h			XXh
D289h			XXh
D28Ah			XXh
D28Bh			XXh
D28Ch			XXh
D28Dh			XXh
D28Eh	CAN1 Mailbox 8: Time Stamp		XXh
D28Fh			XXh
D290h	CAN1 Mailbox 9: Message Identifier	C1MB9	XXh
D291h			XXh
D292h			XXh
D293h			XXh
D294h			
D295h	CAN1 Mailbox 9: Data Length		XXh
D296h	CAN1 Mailbox 9: Data Field		XXh
D297h			XXh
D298h			XXh
D299h			XXh
D29Ah			XXh
D29Bh			XXh
D29Ch			XXh
D29Dh			XXh
D29Eh	CAN1 Mailbox 9: Time Stamp		XXh
D29Fh			XXh
D2A0h	CAN1 Mailbox 10: Message Identifier	C1MB10	XXh
D2A1h			XXh
D2A2h			XXh
D2A3h			XXh
D2A4h			
D2A5h	CAN1 Mailbox 10: Data Length		XXh
D2A6h	CAN1 Mailbox 10: Data Field		XXh
D2A7h			XXh
D2A8h			XXh
D2A9h			XXh
D2AAh			XXh
D2ABh			XXh
D2ACh			XXh
D2ADh			XXh
D2AEh	CAN1 Mailbox 10: Time Stamp		XXh
D2AFh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.25 SFR Information (25) (1)

Address	Register	Symbol	Reset Value
D2B0h	CAN1 Mailbox 11: Message Identifier	C1MB11	XXh
D2B1h			XXh
D2B2h			XXh
D2B3h			XXh
D2B4h			
D2B5h	CAN1 Mailbox 11: Data Length		XXh
D2B6h	CAN1 Mailbox 11: Data Field		XXh
D2B7h			XXh
D2B8h			XXh
D2B9h			XXh
D2BAh			XXh
D2BBh			XXh
D2BCh			XXh
D2BDh			XXh
D2BEh	CAN1 Mailbox 11: Time Stamp		XXh
D2BFh			XXh
D2C0h	CAN1 Mailbox 12: Message Identifier	C1MB12	XXh
D2C1h			XXh
D2C2h			XXh
D2C3h			XXh
D2C4h			
D2C5h	CAN1 Mailbox 12: Data Length		XXh
D2C6h	CAN1 Mailbox 12: Data Field		XXh
D2C7h			XXh
D2C8h			XXh
D2C9h			XXh
D2CAh			XXh
D2CBh			XXh
D2CCh			XXh
D2CDh			XXh
D2CEh	CAN1 Mailbox 12: Time Stamp		XXh
D2CFh			XXh
D2D0h	CAN1 Mailbox 13: Message Identifier	C1MB13	XXh
D2D1h			XXh
D2D2h			XXh
D2D3h			XXh
D2D4h			
D2D5h	CAN1 Mailbox 13: Data Length		XXh
D2D6h	CAN1 Mailbox 13: Data Field		XXh
D2D7h			XXh
D2D8h			XXh
D2D9h			XXh
D2DAh			XXh
D2DBh			XXh
D2DCh			XXh
D2DDh			XXh
D2DEh	CAN1 Mailbox 13: Time Stamp		XXh
D2DFh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.26 SFR Information (26) (1)

Address	Register	Symbol	Reset Value
D2E0h	CAN1 Mailbox 14: Message Identifier	C1MB14	XXh
D2E1h			XXh
D2E2h			XXh
D2E3h			XXh
D2E4h			
D2E5h	CAN1 Mailbox 14: Data Length		XXh
D2E6h	CAN1 Mailbox 14: Data Field		XXh
D2E7h			XXh
D2E8h			XXh
D2E9h			XXh
D2EAh			XXh
D2EBh			XXh
D2ECh			XXh
D2EDh			XXh
D2EEh	CAN1 Mailbox 14: Time Stamp		XXh
D2EFh			XXh
D2F0h	CAN1 Mailbox 15: Message Identifier	C1MB15	XXh
D2F1h			XXh
D2F2h			XXh
D2F3h			XXh
D2F4h			
D2F5h	CAN1 Mailbox 15: Data Length		XXh
D2F6h	CAN1 Mailbox 15: Data Field		XXh
D2F7h			XXh
D2F8h			XXh
D2F9h			XXh
D2FAh			XXh
D2FBh			XXh
D2FCh			XXh
D2FDh			XXh
D2FEh	CAN1 Mailbox 15: Time Stamp		XXh
D2FFh			XXh
D300h	CAN1 Mailbox16: Message Identifier	C1MB16	XXh
D301h			XXh
D302h			XXh
D303h			XXh
D304h			
D305h	CAN1 Mailbox 16: Data Length		XXh
D306h	CAN1 Mailbox 16: Data Field		XXh
D307h			XXh
D308h			XXh
D309h			XXh
D30Ah			XXh
D30Bh			XXh
D30Ch			XXh
D30Dh			XXh
D30Eh	CAN1 Mailbox 16: Time Stamp		XXh
D30Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.27 SFR Information (27) (1)

Address	Register	Symbol	Reset Value
D310h	CAN1 Mailbox 17: Message Identifier	C1MB17	XXh
D311h			XXh
D312h			XXh
D313h			XXh
D314h			
D315h	CAN1 Mailbox 17: Data Length		XXh
D316h	CAN1 Mailbox 17: Data Field		XXh
D317h			XXh
D318h			XXh
D319h			XXh
D31Ah			XXh
D31Bh			XXh
D31Ch			XXh
D31Dh			XXh
D31Eh	CAN1 Mailbox 17: Time Stamp		XXh
D31Fh			XXh
D320h	CAN1 Mailbox 18: Message Identifier	C1MB18	XXh
D321h			XXh
D322h			XXh
D323h			XXh
D324h			
D325h	CAN1 Mailbox 18: Data Length		XXh
D326h	CAN1 Mailbox 18: Data Field		XXh
D327h			XXh
D328h			XXh
D329h			XXh
D32Ah			XXh
D32Bh			XXh
D32Ch			XXh
D32Dh			XXh
D32Eh	CAN1 Mailbox 18: Time Stamp		XXh
D32Fh			XXh
D330h	CAN1 Mailbox 19: Message Identifier	C1MB19	XXh
D331h			XXh
D332h			XXh
D333h			XXh
D334h			
D335h	CAN1 Mailbox 19: Data Length		XXh
D336h	CAN1 Mailbox 19: Data Field		XXh
D337h			XXh
D338h			XXh
D339h			XXh
D33Ah			XXh
D33Bh			XXh
D33Ch			XXh
D33Dh			XXh
D33Eh	CAN1 Mailbox 19: Time Stamp		XXh
D33Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.28 SFR Information (28) (1)

Address	Register	Symbol	Reset Value
D340h	CAN1 Mailbox 20: Message Identifier	C1MB20	XXh
D341h			XXh
D342h			XXh
D343h			XXh
D344h			
D345h	CAN1 Mailbox 20: Data Length		XXh
D346h	CAN1 Mailbox 20: Data Field		XXh
D347h			XXh
D348h			XXh
D349h			XXh
D34Ah			XXh
D34Bh			XXh
D34Ch			XXh
D34Dh			XXh
D34Eh	CAN1 Mailbox 20: Time Stamp		XXh
D34Fh			XXh
D350h	CAN1 Mailbox 21: Message Identifier	C1MB21	XXh
D351h			XXh
D352h			XXh
D353h			XXh
D354h			
D355h	CAN1 Mailbox 21: Data Length		XXh
D356h	CAN1 Mailbox 21: Data Field		XXh
D357h			XXh
D358h			XXh
D359h			XXh
D35Ah			XXh
D35Bh			XXh
D35Ch			XXh
D35Dh			XXh
D35Eh	CAN1 Mailbox 21: Time Stamp		XXh
D35Fh			XXh
D360h	CAN1 Mailbox 22: Message Identifier	C1MB22	XXh
D361h			XXh
D362h			XXh
D363h			XXh
D364h			
D365h	CAN1 Mailbox 22: Data Length		XXh
D366h	CAN1 Mailbox 22: Data Field		XXh
D367h			XXh
D368h			XXh
D369h			XXh
D36Ah			XXh
D36Bh			XXh
D36Ch			XXh
D36Dh			XXh
D36Eh	CAN1 Mailbox 22: Time Stamp		XXh
D36Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.29 SFR Information (29) (1)

Address	Register	Symbol	Reset Value
D370h	CAN1 Mailbox 23: Message Identifier	C1MB23	XXh
D371h			XXh
D372h			XXh
D373h			XXh
D374h			
D375h	CAN1 Mailbox 23: Data Length		XXh
D376h	CAN1 Mailbox 23: Data Field		XXh
D377h			XXh
D378h			XXh
D379h			XXh
D37Ah			XXh
D37Bh			XXh
D37Ch			XXh
D37Dh			XXh
D37Eh	CAN1 Mailbox 23: Time Stamp		XXh
D37Fh			XXh
D380h	CAN1 Mailbox 24: Message Identifier	C1MB24	XXh
D381h			XXh
D382h			XXh
D383h			XXh
D384h			
D385h	CAN1 Mailbox 24: Data Length		XXh
D386h	CAN1 Mailbox 24: Data Field		XXh
D387h			XXh
D388h			XXh
D389h			XXh
D38Ah			XXh
D38Bh			XXh
D38Ch			XXh
D38Dh			XXh
D38Eh	CAN1 Mailbox 24: Time Stamp		XXh
D38Fh			XXh
D390h	CAN1 Mailbox 25: Message Identifier	C1MB25	XXh
D391h			XXh
D392h			XXh
D393h			XXh
D394h			
D395h	CAN1 Mailbox 25: Data Length		XXh
D396h	CAN1 Mailbox 25: Data Field		XXh
D397h			XXh
D398h			XXh
D399h			XXh
D39Ah			XXh
D39Bh			XXh
D39Ch			XXh
D39Dh			XXh
D39Eh	CAN1 Mailbox 25: Time Stamp		XXh
D39Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.30 SFR Information (30) (1)

Address	Register	Symbol	Reset Value
D3A0h	CAN1 Mailbox 26: Message Identifier	C1MB26	XXh
D3A1h			XXh
D3A2h			XXh
D3A3h			XXh
D3A4h			
D3A5h	CAN1 Mailbox 26: Data Length		XXh
D3A6h	CAN1 Mailbox 26: Data Field		XXh
D3A7h			XXh
D3A8h			XXh
D3A9h			XXh
D3AAh			XXh
D3ABh			XXh
D3ACh			XXh
D3ADh			XXh
D3AEh	CAN1 Mailbox 26: Time Stamp		XXh
D3AFh			XXh
D3B0h	CAN1 Mailbox 27: Message Identifier	C1MB27	XXh
D3B1h			XXh
D3B2h			XXh
D3B3h			XXh
D3B4h			
D3B5h	CAN1 Mailbox 27: Data Length		XXh
D3B6h	CAN1 Mailbox 27: Data Field		XXh
D3B7h			XXh
D3B8h			XXh
D3B9h			XXh
D3BAh			XXh
D3BBh			XXh
D3BCh			XXh
D3BDh			XXh
D3BEh	CAN1 Mailbox 27: Time Stamp		XXh
D3BFh			XXh
D3C0h	CAN1 Mailbox 28: Message Identifier	C1MB28	XXh
D3C1h			XXh
D3C2h			XXh
D3C3h			XXh
D3C4h			
D3C5h	CAN1 Mailbox 28: Data Length		XXh
D3C6h	CAN1 Mailbox 28: Data Field		XXh
D3C7h			XXh
D3C8h			XXh
D3C9h			XXh
D3CAh			XXh
D3CBh			XXh
D3CCh			XXh
D3CDh			XXh
D3CEh	CAN1 Mailbox 28: Time Stamp		XXh
D3CFh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.31 SFR Information (31) (1)

Address	Register	Symbol	Reset Value
D3D0h	CAN1 Mailbox 29: Message Identifier	C1MB29	XXh
D3D1h			XXh
D3D2h			XXh
D3D3h			XXh
D3D4h			
D3D5h	CAN1 Mailbox 29: Data Length		XXh
D3D6h	CAN1 Mailbox 29: Data Field		XXh
D3D7h			XXh
D3D8h			XXh
D3D9h			XXh
D3DAh			XXh
D3DBh			XXh
D3DCh			XXh
D3DDh			XXh
D3DEh	CAN1 Mailbox 29: Time Stamp		XXh
D3DFh			XXh
D3E0h	CAN1 Mailbox 30: Message Identifier	C1MB30	XXh
D3E1h			XXh
D3E2h			XXh
D3E3h			XXh
D3E4h			
D3E5h	CAN1 Mailbox 30: Data Length		XXh
D3E6h	CAN1 Mailbox 30: Data Field		XXh
D3E7h			XXh
D3E8h			XXh
D3E9h			XXh
D3EAh			XXh
D3EBh			XXh
D3ECh			XXh
D3EDh			XXh
D3EEh	CAN1 Mailbox 30: Time Stamp		XXh
D3EFh			XXh
D3F0h	CAN1 Mailbox 31: Message Identifier	C1MB31	XXh
D3F1h			XXh
D3F2h			XXh
D3F3h			XXh
D3F4h			
D3F5h	CAN1 Mailbox 31: Data Length		XXh
D3F6h	CAN1 Mailbox 31: Data Field		XXh
D3F7h			XXh
D3F8h			XXh
D3F9h			XXh
D3FAh			XXh
D3FBh			XXh
D3FCh			XXh
D3FDh			XXh
D3FEh	CAN1 Mailbox 31: Time Stamp		XXh
D3FFh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.32 SFR Information (32) (1)

Address	Register	Symbol	Reset Value
D400h	CAN1 Mask Register 0	C1MKR0	XXh
D401h			XXh
D402h			XXh
D403h			XXh
D404h	CAN1 Mask Register 1	C1MKR1	XXh
D405h			XXh
D406h			XXh
D407h			XXh
D408h	CAN1 Mask Register 2	C1MKR2	XXh
D409h			XXh
D40Ah			XXh
D40Bh			XXh
D40Ch	CAN1 Mask Register 3	C1MKR3	XXh
D40Dh			XXh
D40Eh			XXh
D40Fh			XXh
D410h	CAN1 Mask Register 4	C1MKR4	XXh
D411h			XXh
D412h			XXh
D413h			XXh
D414h	CAN1 Mask Register 5	C1MKR5	XXh
D415h			XXh
D416h			XXh
D417h			XXh
D418h	CAN1 Mask Register 6	C1MKR6	XXh
D419h			XXh
D41Ah			XXh
D41Bh			XXh
D41Ch	CAN1 Mask Register 7	C1MKR7	XXh
D41Dh			XXh
D41Eh			XXh
D41Fh			XXh
D420h	CAN1FIFO Receive ID Compare Register 0	C1FIDCR0	XXh
D421h			XXh
D422h			XXh
D423h			XXh
D424h	CAN1FIFO Receive ID Compare Register 1	C1FIDCR1	XXh
D425h			XXh
D426h			XXh
D427h			XXh
D428h	CAN1 Mask Invalid Register	C1MKIVLR	XXh
D429h			XXh
D42Ah			XXh
D42Bh			XXh
D42Ch	CAN1 Mailbox Interrupt Enable Register	C1MIER	XXh
D42Dh			XXh
D42Eh			XXh
D42Fh			XXh
D430h to D49Fh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.33 SFR Information (33) (1)

Address	Register	Symbol	Reset Value
D4A0h	CAN1 Message Control Register 0	C1MCTL0	00h
D4A1h	CAN1 Message Control Register 1	C1MCTL1	00h
D4A2h	CAN1 Message Control Register 2	C1MCTL2	00h
D4A3h	CAN1 Message Control Register 3	C1MCTL3	00h
D4A4h	CAN1 Message Control Register 4	C1MCTL4	00h
D4A5h	CAN1 Message Control Register 5	C1MCTL5	00h
D4A6h	CAN1 Message Control Register 6	C1MCTL6	00h
D4A7h	CAN1 Message Control Register 7	C1MCTL7	00h
D4A8h	CAN1 Message Control Register 8	C1MCTL8	00h
D4A9h	CAN1 Message Control Register 9	C1MCTL9	00h
D4AAh	CAN1 Message Control Register 10	C1MCTL10	00h
D4ABh	CAN1 Message Control Register 11	C1MCTL11	00h
D4ACh	CAN1 Message Control Register 12	C1MCTL12	00h
D4ADh	CAN1 Message Control Register 13	C1MCTL13	00h
D4AEh	CAN1 Message Control Register 14	C1MCTL14	00h
D4AFh	CAN1 Message Control Register 15	C1MCTL15	00h
D4B0h	CAN1 Message Control Register 16	C1MCTL16	00h
D4B1h	CAN1 Message Control Register 17	C1MCTL17	00h
D4B2h	CAN1 Message Control Register 18	C1MCTL18	00h
D4B3h	CAN1 Message Control Register 19	C1MCTL19	00h
D4B4h	CAN1 Message Control Register 20	C1MCTL20	00h
D4B5h	CAN1 Message Control Register 21	C1MCTL21	00h
D4B6h	CAN1 Message Control Register 22	C1MCTL22	00h
D4B7h	CAN1 Message Control Register 23	C1MCTL23	00h
D4B8h	CAN1 Message Control Register 24	C1MCTL24	00h
D4B9h	CAN1 Message Control Register 25	C1MCTL25	00h
D4BAh	CAN1 Message Control Register 26	C1MCTL26	00h
D4BBh	CAN1 Message Control Register 27	C1MCTL27	00h
D4BCh	CAN1 Message Control Register 28	C1MCTL28	00h
D4BDh	CAN1 Message Control Register 29	C1MCTL29	00h
D4BEh	CAN1 Message Control Register 30	C1MCTL30	00h
D4BFh	CAN1 Message Control Register 31	C1MCTL31	00h

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.34 SFR Information (34) (1)

Address	Register	Symbol	Reset Value
D4C0h	CAN1 Control Register	C1CTLR	0000 0101b
D4C1h			00h
D4C2h	CAN1 Status Register	C1STR	0000 0101b
D4C3h			00h
D4C4h	CAN1 Bit Configuration Register	C1BCR	00h
D4C5h			00h
D4C6h			00h
D4C7h	CAN1 Clock Select Register	C1CLKR	00h
D4C8h	CAN1 Receive FIFO Control Register	C1RFCR	10000000b
D4C9h	CAN1 Receive FIFO Pointer Control Register	C1RFPCR	XXh
D4CAh	CAN1 Transmit FIFO Control Register	C1TFCR	1000 0000b
D4CBh	CAN1 Transmit FIFO Pointer Control Register	C1TFPCR	XXh
D4CCh	CAN1 Error Interrupt Enable Register	C1EIER	00h
D4CDh	CAN1 Error Interrupt Source Judge Register	C1EIFR	00h
D4CEh	CAN1 Receive Error Count Register	C1RECR	00h
D4CFh	CAN1 Transmit Error Count Register	C1TECR	00h
D4D0h	CAN1 Error Code Store Register	C1ECSR	00h
D4D1h	CAN1 Channel Search Support Register	C1CSSR	XXh
D4D2h	CAN1 Mailbox Search Status Register	C1MSSR	1000 0000b
D4D3h	CAN1 Mailbox Search Mode Register	C1MSMR	0000 0000b
D4D4h	CAN1 Time Stamp Register	C1TSR	00h
D4D5h			00h
D4D6h	CAN1 Acceptance Filter Support Register	C1AFSR	XXh
D4D7h			XXh
D4D8h	CAN1 Test Control Register	C1TCR	00h
D4D9h			
D4DAh			
D4DBh			
D4DCh			
D4DDh			
D4DEh			
D4DFh			
D4E0h to D4FFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.35 SFR Information (35) (1)

Address	Register	Symbol	Reset Value
D500h	CAN0 Mailbox 0: Message Identifier	C0MB0	XXh
D501h			XXh
D502h			XXh
D503h			XXh
D504h			
D505h	CAN0 Mailbox 0: Data Length		XXh
D506h	CAN0 Mailbox 0: Data Field		XXh
D507h			XXh
D508h			XXh
D509h			XXh
D50Ah			XXh
D50Bh			XXh
D50Ch			XXh
D50Dh			XXh
D50Eh	CAN0 Mailbox 0: Time Stamp		XXh
D50Fh			XXh
D510h	CAN0 Mailbox 1: Message Identifier	C0MB1	XXh
D511h			XXh
D512h			XXh
D513h			XXh
D514h			
D515h	CAN0 Mailbox 1: Data Length		XXh
D516h	CAN0 Mailbox 1: Data Field		XXh
D517h			XXh
D518h			XXh
D519h			XXh
D51Ah			XXh
D51Bh			XXh
D51Ch			XXh
D51Dh			XXh
D51Eh	CAN0 Mailbox 1: Time Stamp		XXh
D51Fh			XXh
D520h	CAN0 Mailbox 2: Message Identifier	C0MB2	XXh
D521h			XXh
D522h			XXh
D523h			XXh
D524h			
D525h	CAN0 Mailbox 2: Data Length		XXh
D526h	CAN0 Mailbox 2: Data Field		XXh
D527h			XXh
D528h			XXh
D529h			XXh
D52Ah			XXh
D52Bh			XXh
D52Ch			XXh
D52Dh			XXh
D52Eh	CAN0 Mailbox 2: Time Stamp		XXh
D52Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.36 SFR Information (36) (1)

Address	Register	Symbol	Reset Value
D530h	CAN0 Mailbox 3: Message Identifier	C0MB3	XXh
D531h			XXh
D532h			XXh
D533h			XXh
D534h			
D535h	CAN0 Mailbox 3: Data Length		XXh
D536h	CAN0 Mailbox 3: Data Field		XXh
D537h			XXh
D538h			XXh
D539h			XXh
D53Ah			XXh
D53Bh			XXh
D53Ch			XXh
D53Dh			XXh
D53Eh	CAN0 Mailbox 3: Time Stamp		XXh
D53Fh			XXh
D540h	CAN0 Mailbox 4: Message Identifier	C0MB4	XXh
D541h			XXh
D542h			XXh
D543h			XXh
D544h			
D545h	CAN0 Mailbox 4: Data Length		XXh
D546h	CAN0 Mailbox 4: Data Field		XXh
D547h			XXh
D548h			XXh
D549h			XXh
D54Ah			XXh
D54Bh			XXh
D54Ch			XXh
D54Dh			XXh
D54Eh	CAN0 Mailbox 4: Time Stamp		XXh
D54Fh			XXh
D550h	CAN0 Mailbox 5: Message Identifier	C0MB5	XXh
D551h			XXh
D552h			XXh
D553h			XXh
D554h			
D555h	CAN0 Mailbox 5: Data Length		XXh
D556h	CAN0 Mailbox 5: Data Field		XXh
D557h			XXh
D558h			XXh
D559h			XXh
D55Ah			XXh
D55Bh			XXh
D55Ch			XXh
D55Dh			XXh
D55Eh	CAN0 Mailbox 5: Time Stamp		XXh
D55Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.37 SFR Information (37) (1)

Address	Register	Symbol	Reset Value
D560h	CAN0 Mailbox 6: Message Identifier	C0MB6	XXh
D561h			XXh
D562h			XXh
D563h			XXh
D564h			
D565h	CAN0 Mailbox 6: Data Length		XXh
D566h	CAN0 Mailbox 6: Data Field		XXh
D567h			XXh
D568h			XXh
D569h			XXh
D56Ah			XXh
D56Bh			XXh
D56Ch			XXh
D56Dh			XXh
D56Eh	CAN0 Mailbox 6: Time Stamp		XXh
D56Fh			XXh
D570h	CAN0 Mailbox 7: Message Identifier	C0MB7	XXh
D571h			XXh
D572h			XXh
D573h			XXh
D574h			
D575h	CAN0 Mailbox 7: Data Length		XXh
D576h	CAN0 Mailbox 7: Data Field		XXh
D577h			XXh
D578h			XXh
D579h			XXh
D57Ah			XXh
D57Bh			XXh
D57Ch			XXh
D57Dh			XXh
D57Eh	CAN0 Mailbox 7: Time Stamp		XXh
D57Fh			XXh
D580h	CAN0 Mailbox 8: Message Identifier	C0MB8	XXh
D581h			XXh
D582h			XXh
D583h			XXh
D584h			
D585h	CAN0 Mailbox 8: Data Length		XXh
D586h	CAN0 Mailbox 8: Data Field		XXh
D587h			XXh
D588h			XXh
D589h			XXh
D58Ah			XXh
D58Bh			XXh
D58Ch			XXh
D58Dh			XXh
D58Eh	CAN0 Mailbox 8: Time Stamp		XXh
D58Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.38 SFR Information (38) (1)

Address	Register	Symbol	Reset Value
D590h	CAN0 Mailbox 9: Message Identifier	C0MB9	XXh
D591h			XXh
D592h			XXh
D593h			XXh
D594h			
D595h	CAN0 Mailbox 9: Data Length		XXh
D596h	CAN0 Mailbox 9: Data Field		XXh
D597h			XXh
D598h			XXh
D599h			XXh
D59Ah			XXh
D59Bh			XXh
D59Ch			XXh
D59Dh			XXh
D59Eh	CAN0 Mailbox 9: Time Stamp		XXh
D59Fh			XXh
D5A0h	CAN0 Mailbox 10: Message Identifier	C0MB10	XXh
D5A1h			XXh
D5A2h			XXh
D5A3h			XXh
D5A4h			
D5A5h	CAN0 Mailbox 10: Data Length		XXh
D5A6h	CAN0 Mailbox 10: Data Field		XXh
D5A7h			XXh
D5A8h			XXh
D5A9h			XXh
D5AAh			XXh
D5ABh			XXh
D5ACh			XXh
D5ADh			XXh
D5AEh	CAN0 Mailbox 10: Time Stamp		XXh
D5AFh			XXh
D5B0h	CAN0 Mailbox 11: Message Identifier	C0MB11	XXh
D5B1h			XXh
D5B2h			XXh
D5B3h			XXh
D5B4h			
D5B5h	CAN0 Mailbox 11: Data Length		XXh
D5B6h	CAN0 Mailbox 11: Data Field		XXh
D5B7h			XXh
D5B8h			XXh
D5B9h			XXh
D5BAh			XXh
D5BBh			XXh
D5BCh			XXh
D5BDh			XXh
D5BEh	CAN0 Mailbox 11: Time Stamp		XXh
D5BFh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.39 SFR Information (39) (1)

Address	Register	Symbol	Reset Value
D5C0h	CAN0 Mailbox 12: Message Identifier	C0MB12	XXh
D5C1h			XXh
D5C2h			XXh
D5C3h			XXh
D5C4h			
D5C5h	CAN0 Mailbox 12: Data Length		XXh
D5C6h	CAN0 Mailbox 12: Data Field		XXh
D5C7h			XXh
D5C8h			XXh
D5C9h			XXh
D5CAh			XXh
D5CBh			XXh
D5CCh			XXh
D5CDh			XXh
D5CEh	CAN0 Mailbox 12: Time Stamp		XXh
D5CFh			XXh
D5D0h	CAN0 Mailbox 13: Message Identifier	C0MB13	XXh
D5D1h			XXh
D5D2h			XXh
D5D3h			XXh
D5D4h			
D5D5h	CAN0 Mailbox 13: Data Length		XXh
D5D6h	CAN0 Mailbox 13: Data Field		XXh
D5D7h			XXh
D5D8h			XXh
D5D9h			XXh
D5DAh			XXh
D5DBh			XXh
D5DCh			XXh
D5DDh			XXh
D5DEh	CAN0 Mailbox 13: Time Stamp		XXh
D5DFh			XXh
D5E0h	CAN0 Mailbox 14: Message Identifier	C0MB14	XXh
D5E1h			XXh
D5E2h			XXh
D5E3h			XXh
D5E4h			
D5E5h	CAN0 Mailbox 14: Data Length		XXh
D5E6h	CAN0 Mailbox 14: Data Field		XXh
D5E7h			XXh
D5E8h			XXh
D5E9h			XXh
D5EAh			XXh
D5EBh			XXh
D5ECh			XXh
D5EDh			XXh
D5EEh	CAN0 Mailbox 14: Time Stamp		XXh
D5EFh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.40 SFR Information (40) (1)

Address	Register	Symbol	Reset Value
D5F0h	CAN0 Mailbox 15: Message Identifier	C0MB15	XXh
D5F1h			XXh
D5F2h			XXh
D5F3h			XXh
D5F4h			
D5F5h	CAN0 Mailbox 15: Data Length		XXh
D5F6h	CAN0 Mailbox 15: Data Field		XXh
D5F7h			XXh
D5F8h			XXh
D5F9h			XXh
D5FAh			XXh
D5FBh			XXh
D5FCh			XXh
D5FDh			XXh
D5FEh	CAN0 Mailbox 15: Time Stamp		XXh
D5FFh			XXh
D600h	CAN0 Mailbox 16: Message Identifier	C0MB16	XXh
D601h			XXh
D602h			XXh
D603h			XXh
D604h			
D605h	CAN0 Mailbox 16: Data Length		XXh
D606h	CAN0 Mailbox 16: Data Field		XXh
D607h			XXh
D608h			XXh
D609h			XXh
D60Ah			XXh
D60Bh			XXh
D60Ch			XXh
D60Dh			XXh
D60Eh	CAN0 Mailbox 16: Time Stamp		XXh
D60Fh			XXh
D610h	CAN0 Mailbox 17: Message Identifier	C0MB17	XXh
D611h			XXh
D612h			XXh
D613h			XXh
D614h			
D615h	CAN0 Mailbox 17: Data Length		XXh
D616h	CAN0 Mailbox 17: Data Field		XXh
D617h			XXh
D618h			XXh
D619h			XXh
D61Ah			XXh
D61Bh			XXh
D61Ch			XXh
D61Dh			XXh
D61Eh	CAN0 Mailbox 17: Time Stamp		XXh
D61Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.41 SFR Information (41) (1)

Address	Register	Symbol	Reset Value
D620h	CAN0 Mailbox 18: Message Identifier	C0MB18	XXh
D621h			XXh
D622h			XXh
D623h			XXh
D624h			
D625h	CAN0 Mailbox 18: Data Length		XXh
D626h	CAN0 Mailbox 18: Data Field		XXh
D627h			XXh
D628h			XXh
D629h			XXh
D62Ah			XXh
D62Bh			XXh
D62Ch			XXh
D62Dh			XXh
D62Eh	CAN0 Mailbox 18: Time Stamp		XXh
D62Fh			XXh
D630h	CAN0 Mailbox 19: Message Identifier	C0MB19	XXh
D631h			XXh
D632h			XXh
D633h			XXh
D634h			
D635h	CAN0 Mailbox 19: Data Length		XXh
D636h	CAN0 Mailbox 19: Data Field		XXh
D637h			XXh
D638h			XXh
D639h			XXh
D63Ah			XXh
D63Bh			XXh
D63Ch			XXh
D63Dh			XXh
D63Eh	CAN0 Mailbox 19: Time Stamp		XXh
D63Fh			XXh
D640h	CAN0 Mailbox 20: Message Identifier	C0MB20	XXh
D641h			XXh
D642h			XXh
D643h			XXh
D644h			
D645h	CAN0 Mailbox 20: Data Length		XXh
D646h	CAN0 Mailbox 20: Data Field		XXh
D647h			XXh
D648h			XXh
D649h			XXh
D64Ah			XXh
D64Bh			XXh
D64Ch			XXh
D64Dh			XXh
D64Eh	CAN0 Mailbox 20: Time Stamp		XXh
D64Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.42 SFR Information (42) (1)

Address	Register	Symbol	Reset Value
D650h	CAN0 Mailbox 21: Message Identifier	C0MB21	XXh
D651h			XXh
D652h			XXh
D653h			XXh
D654h			
D655h	CAN0 Mailbox 21: Data Length		XXh
D656h	CAN0 Mailbox 21: Data Field		XXh
D657h			XXh
D658h			XXh
D659h			XXh
D65Ah			XXh
D65Bh			XXh
D65Ch			XXh
D65Dh			XXh
D65Eh	CAN0 Mailbox 21: Time Stamp		XXh
D65Fh			XXh
D660h	CAN0 Mailbox 22: Message Identifier	C0MB22	XXh
D661h			XXh
D662h			XXh
D663h			XXh
D664h			
D665h	CAN0 Mailbox 22: Data Length		XXh
D666h	CAN0 Mailbox 22: Data Field		XXh
D667h			XXh
D668h			XXh
D669h			XXh
D66Ah			XXh
D66Bh			XXh
D66Ch			XXh
D66Dh			XXh
D66Eh	CAN0 Mailbox 22: Time Stamp		XXh
D66Fh			XXh
D670h	CAN0 Mailbox 23: Message Identifier	C0MB23	XXh
D671h			XXh
D672h			XXh
D673h			XXh
D674h			
D675h	CAN0 Mailbox 23: Data Length		XXh
D676h	CAN0 Mailbox 23: Data Field		XXh
D677h			XXh
D678h			XXh
D679h			XXh
D67Ah			XXh
D67Bh			XXh
D67Ch			XXh
D67Dh			XXh
D67Eh	CAN0 Mailbox 23: Time Stamp		XXh
D67Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.43 SFR Information (43) (1)

Address	Register	Symbol	Reset Value
D680h	CAN0 Mailbox 24: Message Identifier	C0MB24	XXh
D681h			XXh
D682h			XXh
D683h			XXh
D684h			
D685h	CAN0 Mailbox 24: Data Length		XXh
D686h	CAN0 Mailbox 24: Data Field		XXh
D687h			XXh
D688h			XXh
D689h			XXh
D68Ah			XXh
D68Bh			XXh
D68Ch			XXh
D68Dh			XXh
D68Eh	CAN0 Mailbox 24: Time Stamp		XXh
D68Fh			XXh
D690h	CAN0 Mailbox 25: Message Identifier	C0MB25	XXh
D691h			XXh
D692h			XXh
D693h			XXh
D694h			
D695h	CAN0 Mailbox 25: Data Length		XXh
D696h	CAN0 Mailbox 25: Data Field		XXh
D697h			XXh
D698h			XXh
D699h			XXh
D69Ah			XXh
D69Bh			XXh
D69Ch			XXh
D69Dh			XXh
D69Eh	CAN0 Mailbox 25: Time Stamp		XXh
D69Fh			XXh
D6A0h	CAN0 Mailbox 26: Message Identifier	C0MB26	XXh
D6A1h			XXh
D6A2h			XXh
D6A3h			XXh
D6A4h			
D6A5h	CAN0 Mailbox 26: Data Length		XXh
D6A6h	CAN0 Mailbox 26: Data Field		XXh
D6A7h			XXh
D6A8h			XXh
D6A9h			XXh
D6AAh			XXh
D6ABh			XXh
D6ACh			XXh
D6ADh			XXh
D6AEh	CAN0 Mailbox 26: Time Stamp		XXh
D6AFh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.44 SFR Information (44) (1)

Address	Register	Symbol	Reset Value
D6B0h	CAN0 Mailbox 27: Message Identifier	C0MB27	XXh
D6B1h			XXh
D6B2h			XXh
D6B3h			XXh
D6B4h			
D6B5h	CAN0 Mailbox 27: Data Length		XXh
D6B6h	CAN0 Mailbox 27: Data Field		XXh
D6B7h			XXh
D6B8h			XXh
D6B9h			XXh
D6BAh			XXh
D6BBh			XXh
D6BCh			XXh
D6BDh			XXh
D6BEh	CAN0 Mailbox 27: Time Stamp		XXh
D6BFh			XXh
D6C0h	CAN0 Mailbox 28: Message Identifier	C0MB28	XXh
D6C1h			XXh
D6C2h			XXh
D6C3h			XXh
D6C4h			
D6C5h	CAN0 Mailbox 28: Data Length		XXh
D6C6h	CAN0 Mailbox 28: Data Field		XXh
D6C7h			XXh
D6C8h			XXh
D6C9h			XXh
D6CAh			XXh
D6CBh			XXh
D6CCh			XXh
D6CDh			XXh
D6CEh	CAN0 Mailbox 28: Time Stamp		XXh
D6CFh			XXh
D6D0h	CAN0 Mailbox 29: Message Identifier	C0MB29	XXh
D6D1h			XXh
D6D2h			XXh
D6D3h			XXh
D6D4h			
D6D5h	CAN0 Mailbox 29: Data Length		XXh
D6D6h	CAN0 Mailbox 29: Data Field		XXh
D6D7h			XXh
D6D8h			XXh
D6D9h			XXh
D6DAh			XXh
D6DBh			XXh
D6DCh			XXh
D6DDh			XXh
D6DEh	CAN0 Mailbox 29: Time Stamp		XXh
D6DFh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.45 SFR Information (45) (1)

Address	Register	Symbol	Reset Value
D6E0h	CAN0 Mailbox 30: Message Identifier	C0MB30	XXh
D6E1h			XXh
D6E2h			XXh
D6E3h			XXh
D6E4h			
D6E5h	CAN0 Mailbox 30: Data Length		XXh
D6E6h	CAN0 Mailbox 30: Data Field		XXh
D6E7h			XXh
D6E8h			XXh
D6E9h			XXh
D6EAh			XXh
D6EBh			XXh
D6ECh			XXh
D6EDh			XXh
D6EEh	CAN0 Mailbox 30: Time Stamp		XXh
D6EFh			XXh
D6F0h	CAN0 Mailbox 31: Message Identifier	C0MB31	XXh
D6F1h			XXh
D6F2h			XXh
D6F3h			XXh
D6F4h			
D6F5h	CAN0 Mailbox 31: Data Length		XXh
D6F6h	CAN0 Mailbox 31: Data Field		XXh
D6F7h			XXh
D6F8h			XXh
D6F9h			XXh
D6FAh			XXh
D6FBh			XXh
D6FCh			XXh
D6FDh			XXh
D6FEh	CAN0 Mailbox 31: Time Stamp		XXh
D6FFh			XXh
D700h	CAN0 Mask Register 0	C0MKR0	XXh
D701h			XXh
D702h			XXh
D703h			XXh
D704h	CAN0 Mask Register 1	C0MKR1	XXh
D705h			XXh
D706h			XXh
D707h			XXh
D708h	CAN0 Mask Register 2	C0MKR2	XXh
D709h			XXh
D70Ah			XXh
D70Bh			XXh
D70Ch	CAN0 Mask Register 3	C0MKR3	XXh
D70Dh			XXh
D70Eh			XXh
D70Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.46 SFR Information (46) (1)

Address	Register	Symbol	Reset Value
D710h	CAN0 Mask Register 4	C0MKR4	XXh
D711h			XXh
D712h			XXh
D713h			XXh
D714h	CAN0 Mask Register 5	C0MKR5	XXh
D715h			XXh
D716h			XXh
D717h			XXh
D718h	CAN0 Mask Register 6	C0MKR6	XXh
D719h			XXh
D71Ah			XXh
D71Bh			XXh
D71Ch	CAN0 Mask Register 7	C0MKR7	XXh
D71Dh			XXh
D71Eh			XXh
D71Fh			XXh
D720h	CAN0 FIFO Receive ID Compare Register 0	C0FIDCR0	XXh
D721h			XXh
D722h			XXh
D723h			XXh
D724h	CAN0 FIFO Receive ID Compare Register 1	C0FIDCR1	XXh
D725h			XXh
D726h			XXh
D727h			XXh
D728h	CAN0 Mask Invalid Register	C0MKIVLR	XXh
D729h			XXh
D72Ah			XXh
D72Bh			XXh
D72Ch	CAN0 Mailbox Interrupt Enable Register	C0MIER	XXh
D72Dh			XXh
D72Eh			XXh
D72Fh			XXh
D730h to D79Fh			
D7A0h	CAN0 Message Control Register 0	C0MCTL0	00h
D7A1h	CAN0 Message Control Register 1	C0MCTL1	00h
D7A2h	CAN0 Message Control Register 2	C0MCTL2	00h
D7A3h	CAN0 Message Control Register 3	C0MCTL3	00h
D7A4h	CAN0 Message Control Register 4	C0MCTL4	00h
D7A5h	CAN0 Message Control Register 5	C0MCTL5	00h
D7A6h	CAN0 Message Control Register 6	C0MCTL6	00h
D7A7h	CAN0 Message Control Register 7	C0MCTL7	00h
D7A8h	CAN0 Message Control Register 8	C0MCTL8	00h
D7A9h	CAN0 Message Control Register 9	C0MCTL9	00h
D7AAh	CAN0 Message Control Register 10	C0MCTL10	00h
D7ABh	CAN0 Message Control Register 11	C0MCTL11	00h
D7ACh	CAN0 Message Control Register 12	C0MCTL12	00h
D7ADh	CAN0 Message Control Register 13	C0MCTL13	00h
D7AEh	CAN0 Message Control Register 14	C0MCTL14	00h
D7AFh	CAN0 Message Control Register 15	C0MCTL15	00h

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.47 SFR Information (47) (1)

Address	Register	Symbol	Reset Value
D7B0h	CAN0 Message Control Register 16	C0MCTL16	00h
D7B1h	CAN0 Message Control Register 17	C0MCTL17	00h
D7B2h	CAN0 Message Control Register 18	C0MCTL18	00h
D7B3h	CAN0 Message Control Register 19	C0MCTL19	00h
D7B4h	CAN0 Message Control Register 20	C0MCTL20	00h
D7B5h	CAN0 Message Control Register 21	C0MCTL21	00h
D7B6h	CAN0 Message Control Register 22	C0MCTL22	00h
D7B7h	CAN0 Message Control Register 23	C0MCTL23	00h
D7B8h	CAN0 Message Control Register 24	C0MCTL24	00h
D7B9h	CAN0 Message Control Register 25	C0MCTL25	00h
D7BAh	CAN0 Message Control Register 26	C0MCTL26	00h
D7BBh	CAN0 Message Control Register 27	C0MCTL27	00h
D7BCh	CAN0 Message Control Register 28	C0MCTL28	00h
D7BDh	CAN0 Message Control Register 29	C0MCTL29	00h
D7BEh	CAN0 Message Control Register 30	C0MCTL30	00h
D7BFh	CAN0 Message Control Register 31	C0MCTL31	00h
D7C0h	CAN0 Control Register	C0CTLR	0000 0101b
D7C1h			00h
D7C2h	CAN0 Status Register	C0STR	0000 0101b
D7C3h			00h
D7C4h	CAN0 Bit Configuration Register	C0BCR	00h
D7C5h			00h
D7C6h			00h
D7C7h	CAN0 Clock Select Register	C0CLKR	00h
D7C8h	CAN0 Receive FIFO Control Register	C0RFCR	1000 0000b
D7C9h	CAN0 Receive FIFO Pointer Control Register	C0RFPCR	XXh
D7CAh	CAN0 Transmit FIFO Control Register	C0TFCR	1000 0000b
D7CBh	CAN0 Transmit FIFO pointer Control Register	C0TFPCR	XXh
D7CCh	CAN0 Error Interrupt Enable Register	C0EIER	00h
D7CDh	CAN0 Error Interrupt Source Judge Register	C0EIFR	00h
D7CEh	CAN0 Receive Error Count Register	C0RECR	00h
D7CFh	CAN0 Transmit Error Count Register	C0TECR	00h
D7D0h	CAN0 Error Code Store Register	C0ECSR	00h
D7D1h	CAN0 Channel Search Support Register	C0CSSR	XXh
D7D2h	CAN0 Mailbox Search Status Register	C0MSSR	1000 0000b
D7D3h	CAN0 Mailbox Search Mode Register	C0MSMR	0000 0000b
D7D4h	CAN0 Time Stamp Register	C0TSR	00h
D7D5h			00h
D7D6h	CAN0 Acceptance Filter Support Register	C0AFSR	XXh
D7D7h			XXh
D7D8h	CAN0 Test Control Register	C0TCR	00h
D7D9h			
D7DAh			
D7DBh			
D7DCh			
D7DDh			
D7DEh			
D7DFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

4.2 Notes on SFRs

4.2.1 Register Settings

Table 4.48 lists Registers with Write-Only Bits and registers whose function differs between reading and writing. Set these registers with immediate values. Do not use read-modify-write instructions. When establishing the next value by altering the existing value, write the existing value to the RAM as well as to the register. Transfer the next value to the register after making changes in the RAM.
Read-modify-write instructions can be used when writing to the no register bits.

Table 4.48 Registers with Write-Only Bits

Address	Register	Symbol
0249h	UART0 Bit Rate Register	U0BRG
024Bh to 024Ah	UART0 Transmit Buffer Register	U0TB
0259h	UART1 Bit Rate Register	U1BRG
025Bh to 025Ah	UART1 Transmit Buffer Register	U1TB
0269h	UART2 Bit Rate Register	U2BRG
026Bh to 026Ah	UART2 Transmit Buffer Register	U2TB
0299h	UART4 Bit Rate Register	U4BRG
029Bh to 029Ah	UART4 Transmit Buffer Register	U4TB
02A9h	UART3 Bit Rate Register	U3BRG
02ABh to 02AAh	UART3 Transmit Buffer Register	U3TB
02B6h	I2C0 Control Register 1	S3D0
02B8h	I2C0 Status Register 0	S10
0303h to 0302h	Timer A1-1 Register	TA11
0305h to 0304h	Timer A2-1 Register	TA21
0307h to 0306h	Timer A4-1 Register	TA41
030Ah	Three-Phase Output Buffer Register 0	IDB0
030Bh	Three-Phase Output Buffer Register 1	IDB1
030Ch	Dead Time Timer	DTT
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2
0327h to 0326h	Timer A0 Register	TA0
0329h to 0328h	Timer A1 Register	TA1
032Bh to 032Ah	Timer A2 Register	TA2
032Dh to 032Ch	Timer A3 Register	TA3
032Fh to 032Eh	Timer A4 Register	TA4
037Dh	Watchdog Timer Refresh Register	WDTR
037Eh	Watchdog Timer Start Register	WDTS
D4C9h	CAN1 Receive FIFO Pointer Control Register	C1RFPCR
D4CBh	CAN1 Transmit FIFO Pointer Control Register	C1TFPCR
D7C9h	CAN0 Receive FIFO Pointer Control Register	C0RFPCR
D7CBh	CAN0 Transmit FIFO pointer Control Register	C0TFPCR

Table 4.49 Read-Modify-Write Instructions

Function	Mnemonic
Transfer	MOV*Dir*
Bit processing	BCLR, BM*Cnd*, BNOT, BSET, BTSTC, and BTSTS
Shifting	ROLC, RORC, ROT, SHA, and SHL
Arithmetic operation	ABS, ADC, ADCF, ADD, DEC, DIV, DIVU, DIVX, EXTS, INC, MUL, MULU, NEG, SBB, and SUB
Decimal operation	DADC, DADD, DSBB, and DSUB
Logical operation	AND, NOT, OR, and XOR
Jump	ADJNZ, SBJNZ

5. Protection

5.1 Introduction

In the event that a program runs out of control, this function protects the important registers so that they will not be rewritten easily.

5.2 Register

Table 5.1 Registers

Address	Register	Symbol	Reset Value
000Ah	Protect Register	PRCR	00h

5.2.1 Protect Register (PRCR)

Protect Register

b7	b6	b5	b4	b3	b2	b1	b0
		0	0				

Symbol	Address	Reset value
PRCR	000Ah	00h

Bit Symbol	Bit Name	Function	RW
PRC0	Protect bit 0	Enable write access to registers CM0, CM1, CM2, PLC0, PCLKR, FRA0, and FRA2 0: Write disabled 1: Write enabled	RW
PRC1	Protect bit 1	Enable write access to registers PM0, PM1, PM2, TB2SC, INVC0, and INVC1 0: Write disabled 1: Write enabled	RW
PRC2	Protect bit 2	Enable write access to registers PD9, U4MR, NDDR, and PACR 0: Write disabled 1: Write enabled	RW
PRC3	Protect bit 3	Enable write access to registers VCR2, VWCE, VD2LS, VW0C, and VW2C 0: Write disabled 1: Write enabled	RW
— (b5-b4)	Reserved bits	Set to 0.	RW
PRC6	Protect bit 6	Enable write to the PRG2C register 0: Write disabled 1: Write enabled	RW
PRC7	Protect bit 7	Enable write to the E2FM register 0: Write disabled 1: Write enabled	RW

PRC7, PRC6, PRC3, PRC1, PRC0 (Protect bits 7, 6, 3, 1, 0) (b7, b6, b3, b1, b0)

When setting bits PRC7, PRC6, PRC3, PRC1, and PRC0 to 1 (write enabled), these bits remain 1 (write enabled). To change registers protected by these bits, follow these steps:

(1) Set the PRCi bit to 1. (i = 0, 1, 3, 6, 7)
(2) Write to the register protected by the PRCi bit.
(3) Set the PRCi bit to 0 (write protected).

PRC2 (Protect bit 2) (b2)

After setting the PRC2 bit to 1 (write enabled), by writing to a given SFR, the PRC2 bit becomes 0. Change the registers protected by the PRC2 bit in the next instruction after setting the PRC2 bit to 1. The steps are shown below. Make sure there are no interrupts or DMA transfers between steps (1) and (2).

(1) Set the PRC2 bit to 1.
(2) Write to the register protected by the PRC2 bit.

5.3 Notes on Protection

After setting the PRC2 bit to 1 (write enabled), by writing to a given SFR, the PRC2 bit becomes 0 (write disabled). Change the registers protected by the PRC2 bit in the next instruction after setting the PRC2 bit to 1. Make sure there are no interrupts or DMA transfers between the instruction that sets the PRC2 bit to 1 and the next instruction.

6. Resets

6.1 Introduction

The following resets can be used to reset the MCU: hardware reset, power-on reset, voltage monitor 0 reset, voltage monitor 2 reset, oscillator stop detect reset, watchdog timer reset, and software reset.
Table 6.1 lists the Types of Resets and Figure 6.1 shows the Reset Circuit Block Diagram. Symbols (A) to (D) in the table and figure is explained in Table 6.2. Table 6.3 lists the I/O Pins.

Table 6.1 Types of Resets

Reset Name	Trigger	Registers and Bits Not to Reset
Hardware reset	A low-level signal is applied to the $\overline{\text{RESET}}$ pin.	(A)
Power-on reset	A rise in voltage on VCC	N/A
Voltage monitor 0 reset	A drop in voltage on VCC (reference voltage: Vdet0)	N/A
Voltage monitor 2 reset	A drop in voltage on VCC (reference voltage: Vdet2)	(B)
Oscillator stop detect reset	A stop in the main clock oscillator is detected.	(B) (C) (D)
Watchdog timer reset	The watchdog timer underflows.	(B) (C)
Software reset	Setting the PM03 bit in the PM0 register to 1.	(B) (C)

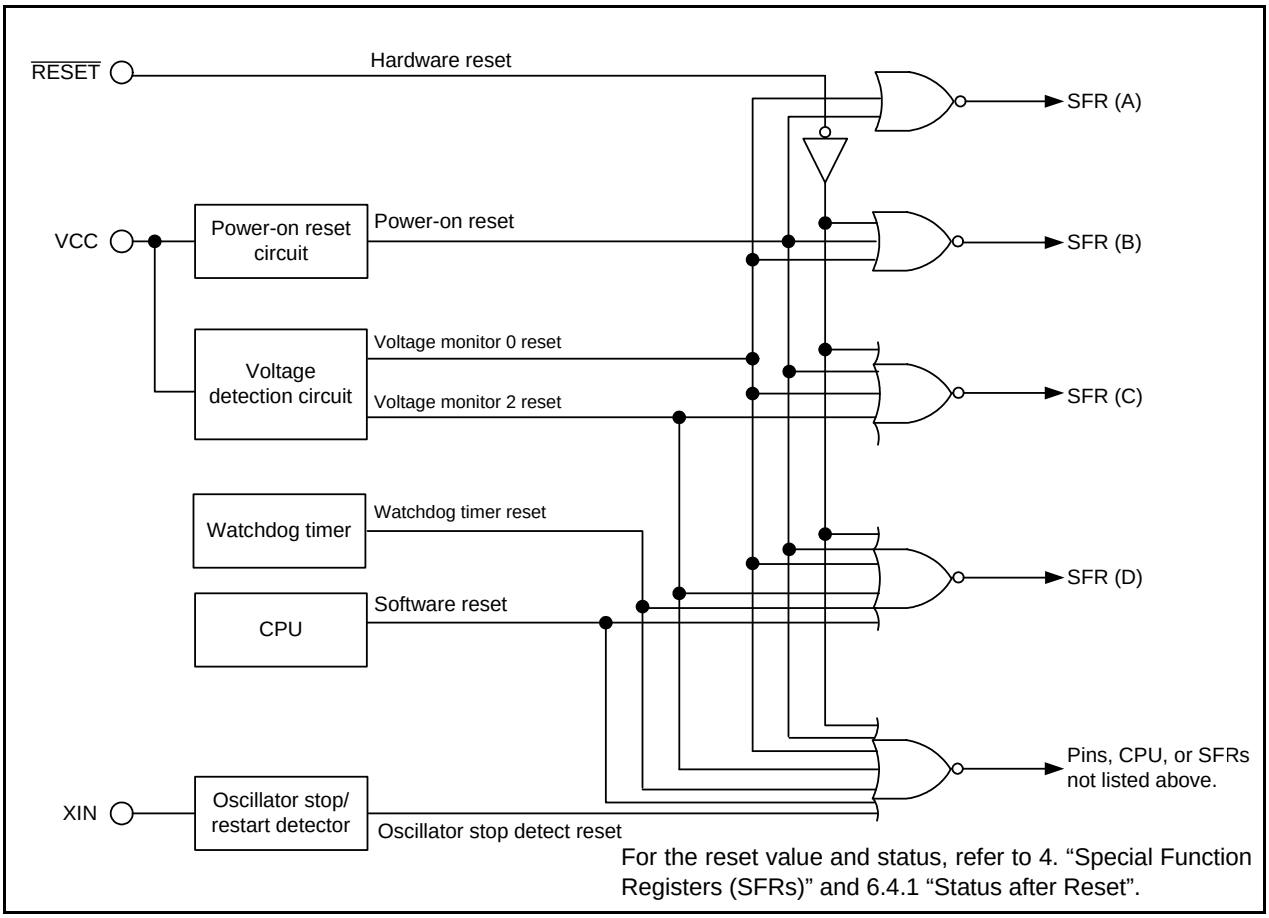


Figure 6.1 Reset Circuit Block Diagram

Table 6.2 Classification of SFRs Which are Reset

SFR	Register and Bit
SFR (A)	OSDR bit in the RSTFR register
SFR (B)	Registers VCR1, VCR2, and VW0C Bits VW2C2 and VW2C3 in the VW2C register
SFR (C)	VD2LS register
SFR (D)	Bits CM20, CM21, and CM27 in the CM2 register

Table 6.3 I/O Pins

Pin	I/O	Function
$\overline{\text{RESET}}$	Input	Hardware reset input
VCC	Input	Power input. The power-on reset, voltage monitor 0 reset, and voltage monitor 2 reset are generated by monitoring VCC.
XIN	Input	Main clock input. The oscillator stop detect reset is generated by monitoring the main clock.

6.2 Registers

Refer to 7. “Voltage Detector” for registers used with the voltage monitor 0 reset, and voltage monitor 2 reset. Refer to 13. “Watchdog Timer” for registers used with the watchdog timer reset. Refer to 8.7 “Oscillator Stop/Restart Detect Function” for registers used with the oscillator stop detect reset.

Table 6.4 Registers

Address	Register	Symbol	Reset Value
0004h	Processor Mode Register 0	PM0	00h
0018h	Reset Source Determine Register	RSTFR	_ (1)

Note:
1. Refer to 6.2.2 “Reset Source Determine Register (RSTFR)”

6.2.1 Processor Mode Register 0 (PM0)

Processor Mode Register 0

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0		0	0	0

Symbol	Address	Reset Value
PM0	0004h	00h

Bit Symbol	Bit Name	Function	RW
(b2-b0)	Reserved bits	Set to 0.	RW
PM03	Software reset bit	Setting this bit to 1 resets the MCU. The read value is 0.	RW
(b7-b4)	Reserved bits	Set to 0.	RW

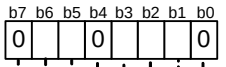
Write to this register after setting the PRC1 bit in the PRCR register to 1 (write enabled).

PM03 (Software reset bit) (b3)

A software reset is generated by setting the PM03 bit to 1.

6.2.2 Reset Source Determine Register (RSTFR)

Reset Source Determine Register



Symbol: RSTFR | Address: 0018h | Reset Value: See Table 6.5.

Bit Symbol	Bit Name	Function	RW
— (b0)	Reserved bit	If necessary, set to 0. The read value is undefined.	RW
HWR	Hardware reset detection flag	0: Not detected 1: Detected	RO
SWR	Software reset detection flag	0: Not detected 1: Detected	RO
WDR	Watchdog timer reset detection flag	0: Not detected 1: Detected	RO
— (b4)	Reserved bit	If necessary, set to 0. The read value is undefined.	RW
LVD2R	Voltage monitor 2 reset detection flag	0: Not detected 1: Detected	RO
OSDR	Oscillator stop detect reset detect flag	0: Not detected 1: Detected	RW
— (b7)	Reserved bit	If necessary, set to 0. The read value is undefined.	RW

Table 6.5 RSTFR Register Reset Value

Reset	Bits in the RSTFR Register				
	OSDR	LVD2R	WDR	SWR	HWR
Hardware reset	No change	0	0	0	1
Power-on reset	0	0	0	0	0
Voltage monitor 0 reset	0	0	0	0	0
Voltage monitor 2 reset	0	1	0	0	0
Oscillator stop detect reset	1	0	0	0	0
Watchdog timer reset	0	0	1	0	0
Software reset	0	0	0	1	0

HWR (Hardware Reset Detect Flag) (b1)

When setting the LVDAS bit in the OFS1 address to 0 (voltage detector 0 reset is enabled after resetting the hardware), or the voltage monitor 0 reset is enabled by a program after reset, the HWR bit after the hardware reset is undefined.

OSDR (Oscillator stop detect reset detect flag) (b6)

The OSDR bit also changes when following condition is met:
Conditions to become 0:

- Power-on
- Setting this bit to 0

This bit will not become 1 even when written to 1.

6.3 Optional Function Select Area

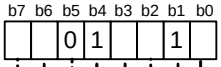
In the optional function select area, the MCU state after reset and the function to prevent rewrite in parallel I/O mode are selected.

The optional function select area is not an SFR, and therefore cannot be rewritten by a program. Set an appropriate value when writing a program to flash memory. The entire optional function select area becomes FFh when the block including the optional function select area is erased.

In blank products, the OFS1 address value is FFh when shipped. After a value is written by the user, this address takes on the written value. In programmed products, the OFS1 address is the value set in the user program prior to shipping.

6.3.1 Optional Function Select Address 1 (OFS1)

Optional Function Select Address 1



Symbol: OFS1

Address: FFFFFFh

Bit Symbol	Bit Name	Function
WDTON	Watchdog timer start select bit	0 : Watchdog timer starts automatically after reset. 1 : Watchdog timer is in a stopped state after reset.
— (b1)	Reserved bit	Set to 1.
ROMCR	ROM code protect cancel bit	0 : ROM code protection cancelled. 1 : ROMCP1 bit enabled.
ROMCP1	ROM code protect bit	0 : ROM code protection enabled. 1 : ROM code protection cancelled.
— (b4)	Reserved bit	Set to 1.
— (b5)	Reserved bit	Set to 0.
LVDAS	Voltage detector 0 start bit	0 : Voltage monitor 0 reset enabled after hardware reset. 1 : Voltage monitor 0 reset disabled after hardware reset.
CSPROINI	After-reset count source protection mode select bit	0 : Count source protection mode enabled after reset. 1 : Count source protection mode disabled after reset.

WDTON (Watchdog timer start select bit) (b0)

CSPROINI (After-reset count source protection mode select bit) (b7)

These bits select the state of the watchdog timer after reset.

Set the WDTON bit to 0 (watchdog timer starts automatically after reset) when setting the CSPROINI bit to 0 (count source protection mode enabled after reset).

Refer to 13. “Watchdog Timer” for details on the watchdog timer and count source protection mode.

ROMCR (ROM code protect cancel bit) (b2)
ROMCP1 (ROM code protect bit) (b3)

These bits prevent the flash memory from being read or changed in parallel I/O mode.

Table 6.6 ROM Code Protection

Bit Setting		ROM Code Protection
ROMCR bit	ROMCP1 bit	
0	0	Cancelled
0	1	
1	0	Enabled
1	1	Cancelled

Reserved bit (b5)

Set to 0.

LVDAS (Voltage detector 0 start bit) (b6)

Set this bit to 0 (voltage monitor 0 reset enabled after hardware reset) when using the power-on reset. This bit is enabled in single-chip mode, while disabled in boot mode.

6.4 Operations

6.4.1 Status after Reset

The status of SFRs after reset depends on the reset type. See the Reset Value column in 4. “Special Function Registers (SFRs)”. Table 6.7 lists Pin Status When $\overline{\text{RESET}}$ Pin Level is Low, Figure 6.2 shows CPU Register Status after Reset, and Figure 6.3 shows Reset Sequence.

Table 6.7 Pin Status When $\overline{\text{RESET}}$ Pin Level is Low

Pin Name	Status (1)
P0 to P10	Input port (high-impedance)

Note:
1. The pin status shown here is when the internal power supply voltage has stabilized after power-on. The pin status is undefined until td(P-R) has elapsed after power-on.

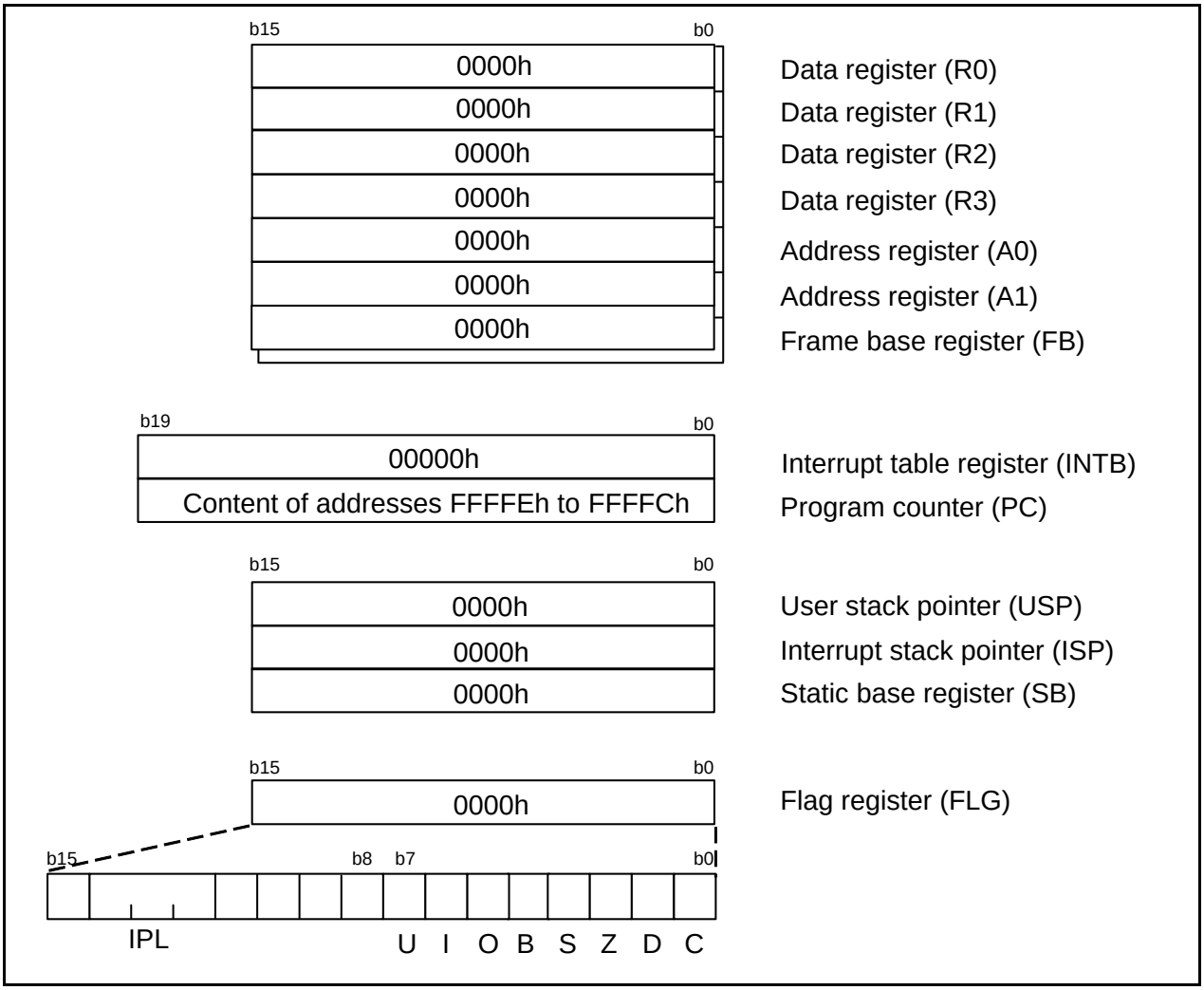


Figure 6.2 CPU Register Status after Reset

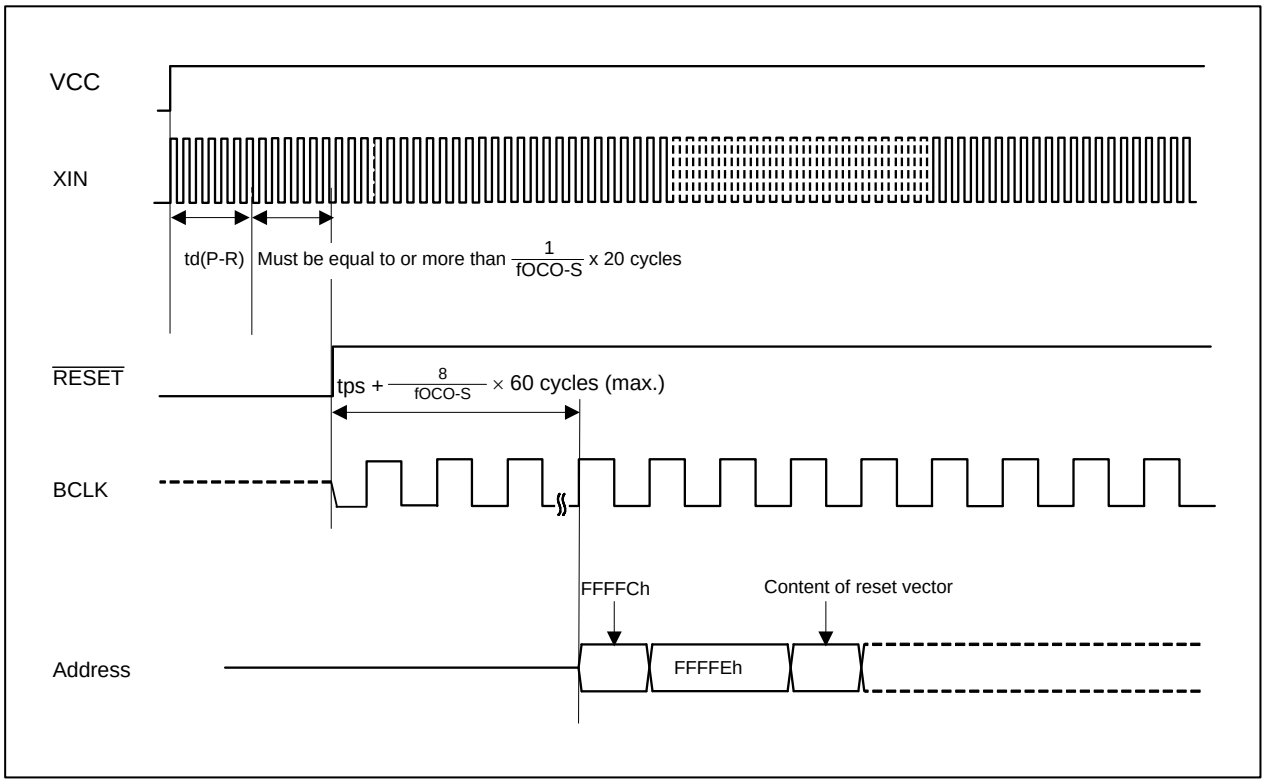


Figure 6.3 Reset Sequence

6.4.2 Hardware Reset

This reset is triggered by the $\overline{\text{RESET}}$ pin. When the power supply voltage meets the recommended operating conditions, the MCU resets the pins, CPU, and SFRs when a low-level signal is applied to the $\overline{\text{RESET}}$ pin.

When changing the signal applied to the $\overline{\text{RESET}}$ pin from low to high, the MCU executes the program at the address indicated by the reset vector. fOCO-S divided by 8 is automatically selected as the CPU clock after reset.

The HWR bit in the RSTFR register becomes 1 (hardware reset detected) after hardware reset. However, if the LVDAS bit in the OFS1 address is 0 (voltage detector 0 reset is enabled after resetting the hardware), the HWR bit is undefined. Refer to 4. “Special Function Registers (SFRs)” for the remaining SFR states after reset.

The internal RAM is not reset. When a low-level signal is applied to the $\overline{\text{RESET}}$ pin while writing data to the internal RAM, the internal RAM becomes undefined.

The procedures for generating a hardware reset are as follows:

When the power supply is stable

(1) Apply a low-level signal to the $\overline{\text{RESET}}$ pin.
(2) Wait for tw(RSTL).
(3) Apply a high-level signal to the $\overline{\text{RESET}}$ pin.

When the power is turned on

(1) Apply a low-level signal to the $\overline{\text{RESET}}$ pin.
(2) Raise the power supply voltage to the recommended operating level.
(3) Wait for td(P-R) until the internal voltage stabilizes.
(4) Wait for $\frac{1}{fOCO-S} \times 20$ cycles.
(5) Apply a high-level signal to the $\overline{\text{RESET}}$ pin.

Figure 6.4 shows an Reset Circuit Example.

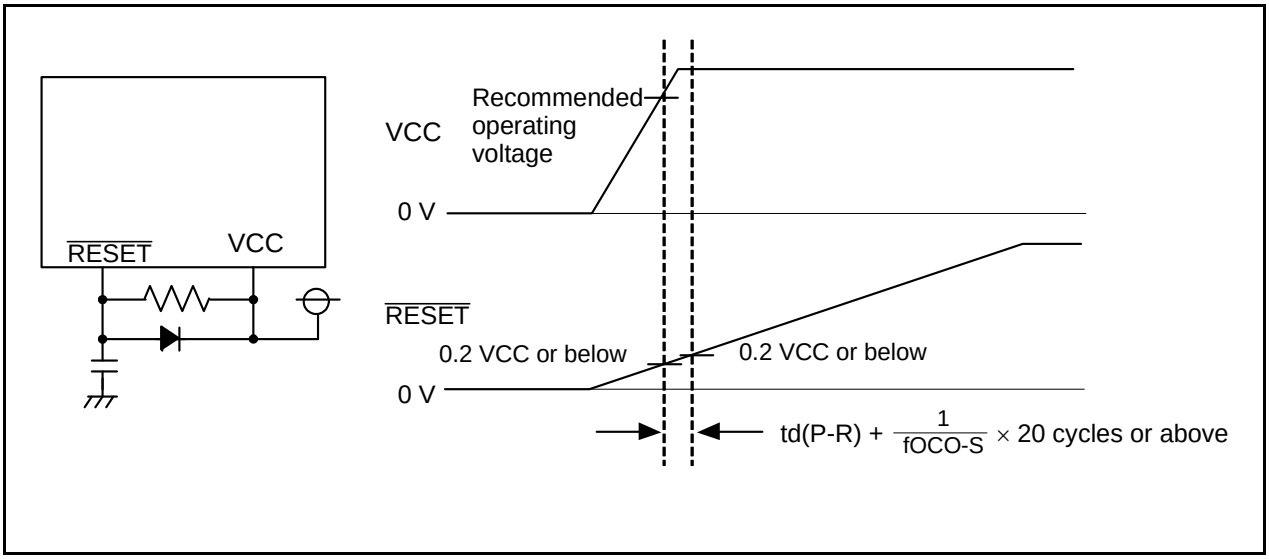


Figure 6.4 Reset Circuit Example

6.4.3 Power-On Reset Function

When the $\overline{\text{RESET}}$ pin is connected to VCC via a pull-up resistor, and the VCC voltage level rises while the rise gradient is trth or more, the power-on reset function is enabled and the MCU resets the pins, CPU, and SFRs. Also, when a capacitor is connected to the $\overline{\text{RESET}}$ pin, always keep the voltage to the $\overline{\text{RESET}}$ pin in the range of VIH.

When the input voltage to the VCC pin reaches Vdet0 or above, the fOCO-S count starts. When the fOCO-S count reaches 128, the internal reset signal becomes high and the MCU executes the program at the address indicated by the reset vector. fOCO-S divided by 8 is automatically selected as the CPU clock after reset.

The internal RAM is not reset.

Use the voltage monitor 0 reset together with the power-on reset. Set the LVDAS bit in the OFS1 address to 0 (voltage monitor 0 reset enabled after hardware reset) to use the power-on reset. In this case, the voltage monitor 0 reset is enabled (the VW0C0 bit and bit 6 in the VW0C register are 1 and the VC25 bit in the VCR2 register is 1). Do not set these bits to 0 by a program.

Refer to 7. “Voltage Detector” for details of the voltage monitor 0 reset.

Figure 6.5 shows Example of Power-On Reset Operation.

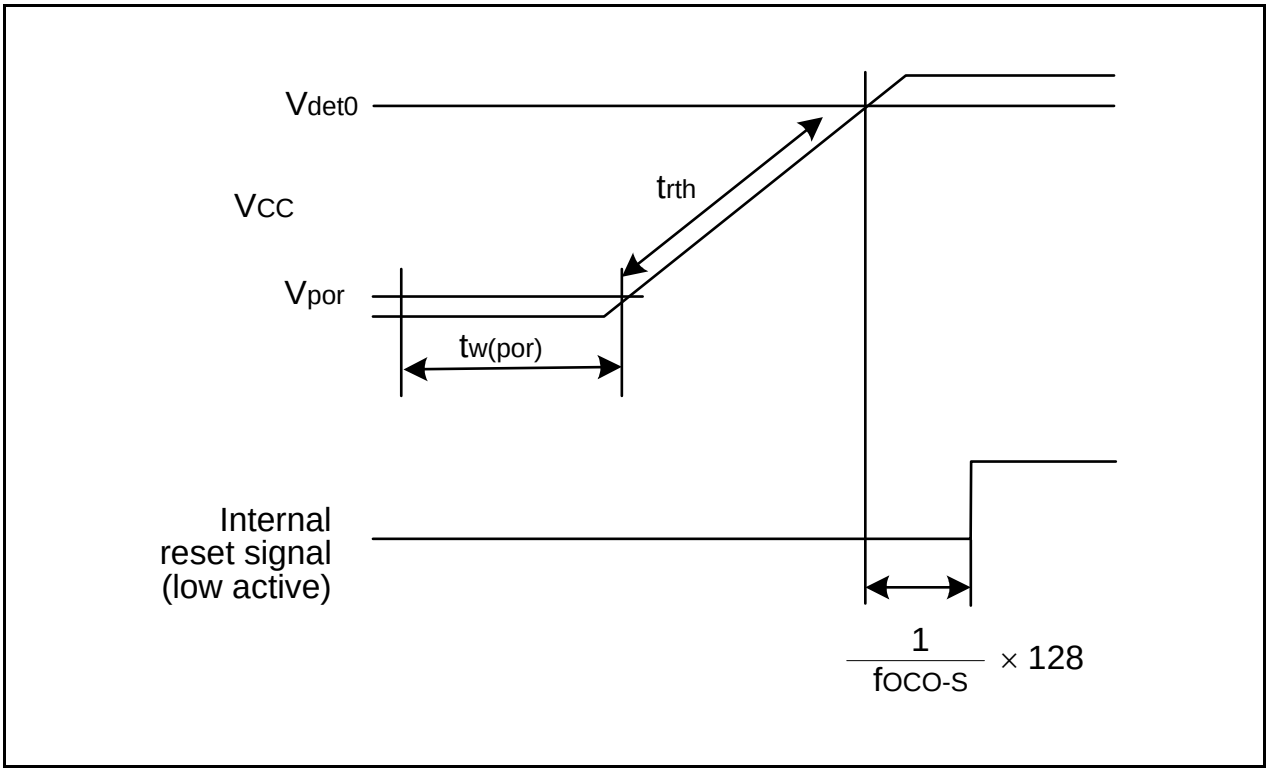


Figure 6.5 Example of Power-On Reset Operation

6.4.4 Voltage Monitor 0 Reset

This reset is triggered by the MCU's on-chip voltage detector 0. The voltage detector 0 monitors the voltage applied to the VCC pin (Vdet0).

The MCU resets the pins, CPU, and SFRs when the voltage applied to the VCC pin drops to Vdet0 or below.

Then, the fOCO-S count starts when the voltage applied to the VCC pin rises to Vdet0 or above. The internal reset signal becomes high after 128 cycles of fOCO-S, and then the MCU executes the program at the address indicated by the reset vector. fOCO-S divided by 8 is automatically selected as the CPU clock after reset.

The internal RAM is not reset. When the voltage applied to the VCC pin drops to Vdet0 or below while writing data to the internal RAM, the internal RAM becomes undefined.

Refer to 7. “Voltage Detector” for details of the voltage monitor 0 reset.

6.4.5 Voltage Monitor 2 Reset

This reset is triggered by the MCU's on-chip voltage detector 2. Voltage detector 2 monitors the voltage applied to the VCC pin (Vdet2).

When the VW2C6 bit in the VW2C register is 1 (voltage monitor 2 reset when Vdet2 passage is detected), the MCU resets the pins, CPU, and SFRs when the voltage applied to the VCC pin drops to Vdet2 or below. fOCO-S divided by 8 is automatically selected as the CPU clock after reset.Then, after the set amount of time, the MCU executes the program at the address indicated by the reset vector.

The LVD2R bit in the RSTFR register becomes 1 (voltage monitor 2 reset detected) after voltage monitor 2 reset. Some SFRs are not reset at voltage monitor 2 reset. Refer to 4. “Special Function Registers (SFRs)” for details.

The internal RAM is not reset.

Refer to 7. “Voltage Detector” for details of the voltage monitor 2 reset.

6.4.6 Oscillator Stop Detect Reset

The MCU resets and stops the pins, CPU, and SFRs when the CM27 bit in the CM2 register is 0 (reset when oscillator stop detected), if it detects that the main clock oscillator has stopped.

The OSDR bit in the RSTFR register becomes 1 (oscillator stop detect reset detected) after oscillator stop detect reset.

Some SFRs are not reset at oscillator stop detect reset. Refer to 4. “Special Function Registers (SFRs)” for details. The internal RAM is not reset. When the main clock oscillator stop is detected while writing data to the internal RAM, the internal RAM becomes undefined.

Oscillator stop detect reset is canceled by hardware reset or voltage monitor 0 reset.

Refer to 8.7 “Oscillator Stop/Restart Detect Function” for details.

6.4.7 Watchdog Timer Reset

The MCU resets the pins, CPU, and SFRs when the PM12 bit in the PM1 register is 1 (reset when watchdog timer underflows) and the watchdog timer underflows. Then the MCU executes the program at the address determined by the reset vector. fOCO-S divided by 8 is automatically selected as the CPU clock after reset.

The WDR bit in the RSTFR register becomes 1 (watchdog timer reset detected) after watchdog timer reset. Some SFRs are not reset at watchdog timer reset. Refer to 4. “Special Function Registers (SFRs)” for details.

The internal RAM is not reset. When the watchdog timer underflows while writing data to the internal RAM, the internal RAM becomes undefined.

Refer to 13. “Watchdog Timer” for details.

6.4.8 Software Reset

The MCU resets the pins, CPU, and SFRs when the PM03 bit in the PM0 register is 1 (MCU reset). Then the MCU executes the program at the address determined by the reset vector. fOCO-S divided by 8 is automatically selected as the CPU clock after reset.

The SWR bit in the RSTFR register becomes 1 (software reset detected) after software reset. Some SFRs are not reset at software reset. Refer to 4. “Special Function Registers (SFRs)” for details. The internal RAM is not reset.

6.5 Notes on Resets

6.5.1 Power Supply Rising Gradient

When supplying power to the MCU, make sure that the power supply voltage applied to the VCC pin meets the SVCC conditions.

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
SVCC	Power supply rising gradient (VCC) (Voltage range: 0 to 2)	0.05			V/ms

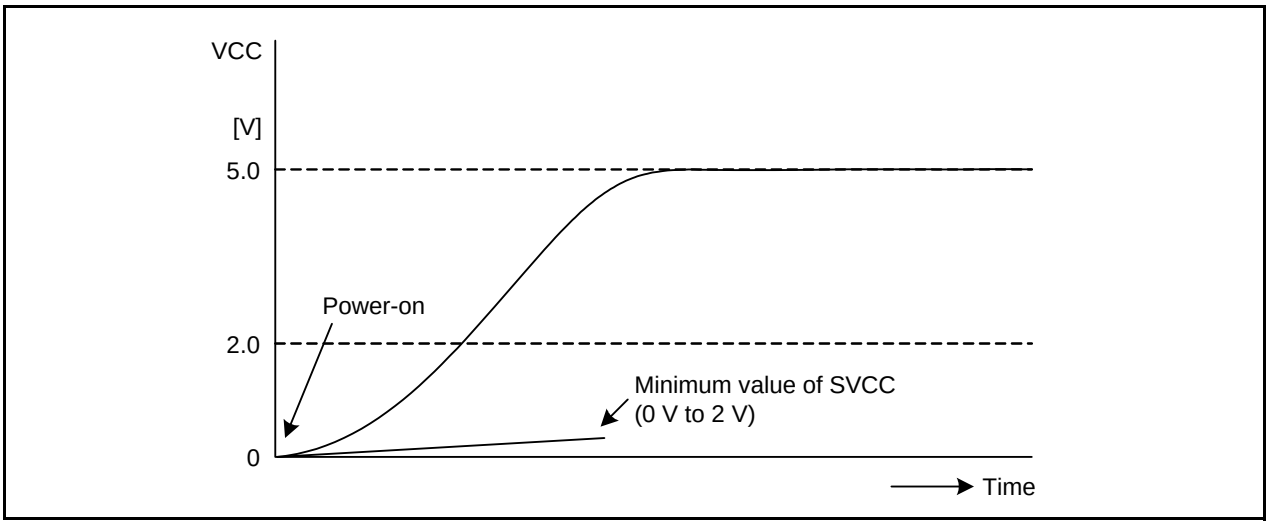


Figure 6.6 SVCC Timing

6.5.2 Power-On Reset

Use the voltage monitor 0 reset together with the power-on reset. To use the power-on reset, set the LVDAS bit in the OFS1 address to 0 (voltage monitor 0 reset enabled after hardware reset). In this case, the voltage monitor 0 reset is enabled (the VW0C0 bit and bit 6 in the VW0C register are 1, and the VC25 bit in the VCR2 register is 1) after power-on reset. Do not disable these bits by a program.

6.5.3 OSDR Bit (Oscillation Stop Detect Reset Detect Flag)

When an oscillator stop detect reset is generated, the MCU is reset and then stopped. This state is canceled by hardware reset or voltage monitor 0 reset.

Note that the OSDR bit in the RSTFR register is not affected by a hardware reset, but becomes 0 (not detected) from a voltage monitor 0 reset.

6.5.4 Hardware Reset When VCC < Vdet0

If a hardware reset is executed when the LVDAS bit in the OFS1 address is 0 (voltage monitor 0 reset enabled after hardware reset) and VCC < Vdet0, the MCU executes the program at the address indicated by the reset vector when changing the signal applied to the $\overline{\text{RESET}}$ pin from low to high. A voltage monitor 0 reset is not generated.

7. Voltage Detector

7.1 Introduction

The voltage detector monitors the voltage applied to the VCC pin. This circuit can be programmed to monitor the VCC input voltage. Voltage monitor 0 reset, voltage monitor 2 interrupt, and voltage monitor 2 reset can also be used.

Table 7.1 lists the Voltage Detector Specifications and Figure 7.1 shows Voltage Detector Block Diagram.

Table 7.1 Voltage Detector Specifications

Item		Voltage Detector 0	Voltage Detector 2
VCC monitor	Voltage to monitor	Vdet0	Vdet2
	Detection target	Whether passing Vdet0 by rising or falling	Whether passing Vdet2 by rising or falling
	Monitor	None	VC13 bit in VCR1 register
			Whether VCC is higher or lower than Vdet2
Process when voltage is detected	Reset	Voltage monitor 0 reset	Voltage monitor 2 reset
		Reset at Vdet0 > VCC; restart CPU operation at VCC > Vdet0	Reset at Vdet2 > VCC; restart CPU operation after a specified time
	Interrupt	None	Voltage monitor 2 interrupt
			Interrupt request at Vdet2 > VCC and VCC > Vdet2 when digital filter is enabled; interrupt request at Vdet2 > VCC or VCC > Vdet2 when digital filter is disabled
Digital filter	Switch enabled/disabled	None	Available
	Sampling time	None	(Divide-by-n of fOCO-S) × 3 n: 1, 2, 4, 8

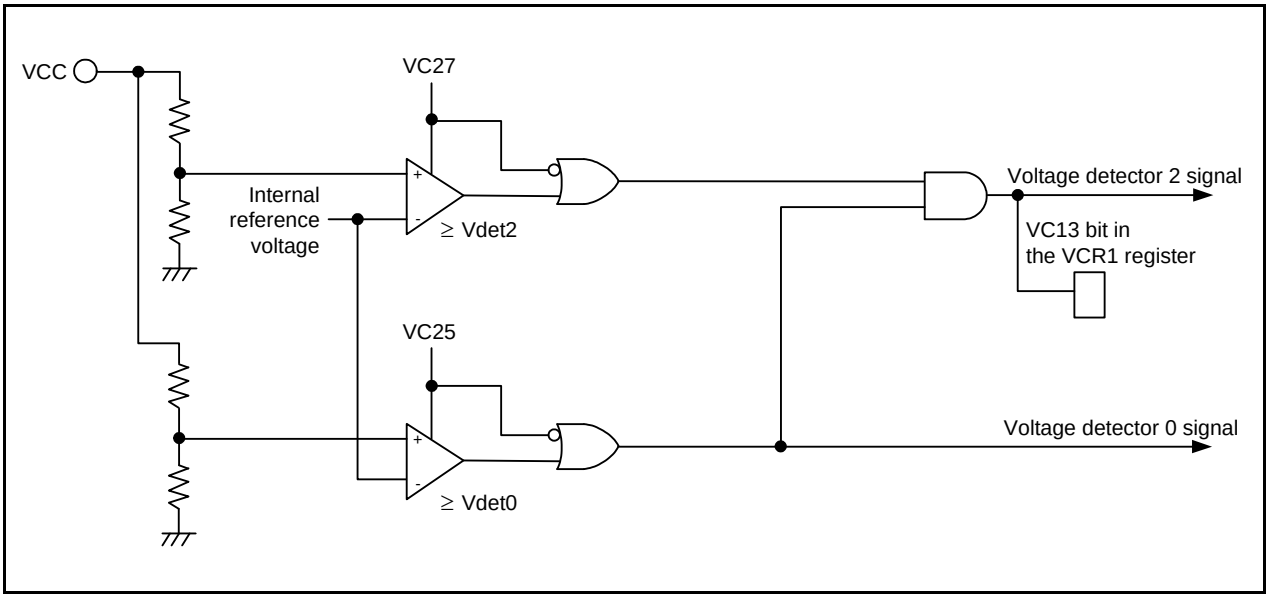


Figure 7.1 Voltage Detector Block Diagram

7.2 Registers

Table 7.2 Registers

Address	Register Name	Register Symbol	Reset Value
0019h	Voltage Detector 2 Flag Register	VCR1	0000 1000b (1, 5)
001Ah	Voltage Detector Operation Enable Register	VCR2	000X 0000b (2, 5) 001X 0000b (3, 5)
0026h	Voltage Monitor Function Select Register	VWCE	00h
0028h	Voltage Detector 2 Level Select Register	VD2LS	0000 0100b (4, 6)
002Ah	Voltage Monitor 0 Control Register	VW0C	1100 1X10b (2, 5) 1100 1X11b (3, 5)
002Ch	Voltage Monitor 2 Control Register	VW2C	1000 0X10b (1, 7)

Notes:
1. Hardware reset, power-on reset, or voltage monitor 0 reset
2. When the LVDAS bit of the OFS1 address is 1 at hardware reset.
3. This value shows the value after any of the following resets.
   - Voltage monitor 0 reset
   - When the LVDAS bit of the OFS1 address is 0 at hardware reset
   - Power-on reset
4. Hardware reset, power-on reset, voltage monitor 0 reset, or voltage monitor 2 reset
5. The value does not change after voltage monitor 2 reset, oscillator stop detect reset, watchdog timer reset, or software reset.
6. The value does not change after oscillator stop detect reset, watchdog timer reset, or software reset.
7. Bits VW2C2 and VW2C3 are not changed after voltage monitor 2 reset, oscillator stop detect reset, watchdog timer reset, or software reset.

7.2.1 Voltage Detector 2 Flag Register (VCR1)

Voltage Detector 2 Flag Register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0		0	0	0

Symbol	Address	Reset Value
VCR1	0019h	0000 1000b (hardware reset, power-on reset, voltage monitor 0 reset)

Bit Symbol	Bit Name	Function	RW
— (b2-b0)	Reserved bits	Set to 0	RW
VC13	Low-voltage monitor flag	0: VCC < Vdet2 1: VCC ≥ Vdet2 or voltage detector 2 disabled	RO
— (b7-b4)	Reserved bits	Set to 0	RW

This register does not change at voltage monitor 2 reset, oscillator stop detect reset, watchdog timer reset, or software reset.

VC13 (Low-voltage monitor flag) (b3)

The VC13 bit is enabled when the VW12E bit in the VWCE register is 1 (voltage monitor 2 enabled) and the VC27 bit in the VCR2 register is 1 (voltage detector 2 enabled).

Condition to become 0:

- VCC < Vdet2 (when the VW12E bit is 1 and the VC27 bit is 1)

Conditions to become 1:

- VCC ≥ Vdet2 (when the VW12E bit is 1 and the VC27 bit is 1)
- The VC27 bit is 0 (voltage detector 2 disabled).

7.2.2 Voltage Detector Operation Enable Register (VCR2)

Voltage Detector Operation Enable Register

b7	b6	b5	b4	b3	b2	b1	b0
	0		X	0	0	0	0

Symbol	Address	Reset Value
VCR2	001Ah	000X 0000b (1) 001X 0000b (2)

Bit Symbol	Bit Name	Function	RW
— (b3-b0)	Reserved bits	Set to 0	RW
— (b4)	No register bit. If necessary, set to 0. The read value is undefined.		—
VC25	Voltage detector 0 enable bit	0 : Disable voltage detector 0 1 : Enable voltage detector 0	RW
— (b6)	Reserved bit	Set to 0	RW
VC27	Voltage detector 2 enable bit	0 : Disable voltage detector 2 1 : Enable voltage detector 2	RW

Notes:
1. When the LVDAS bit of the OFS1 address is 1 at hardware reset
2. This value shows the value after any of the following resets:
   - Voltage monitor 0 reset
   - When the LVDAS bit of the OFS1 address is 0 at hardware reset
   - Power-on reset

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting this register.
This register does not change at voltage monitor 2 reset, oscillator stop detect reset, watchdog timer reset, or software reset.

VC25 (Voltage detector 0 enable bit) (b5)

To use voltage monitor 0 reset, set the VC25 bit to 1 (voltage detector 0 enabled). After changing the VC25 bit to 1, the detector starts operating when the td(E-A) elapses.

VC27 (Voltage detector 2 enable bit) (b7)

Voltage detector 2 is enabled when the VW12E bit in the VWCE register is set to 1 (voltage monitor 2 enabled) and the VC27 bit is 1 (voltage detector 2 enabled). Set bits VW12E and VC27 to 1 under the following conditions:

- When using voltage monitor 2 interrupt/reset
- When using the VC13 bit in the VCR1 register
- When using the VW2C2 bit in the VW2C register

After changing this bit from 0 to 1, the detector will start operating after td(E-A) elapses.

7.2.3 Voltage Monitor Function Select Register (VWCE)

Voltage Monitor Function Select Register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	0	

Symbol	Address	Reset Value
VWCE	0026h	00h

Bit Symbol	Bit Name	Function	RW
VW12E	Voltage monitor 2 enable bit	0: Voltage monitor 2 disabled 1: Voltage monitor 2 enabled	RW
— (b7-b1)	Reserved bits	Set to 0	RW

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting this register.

VW12E (Voltage monitor 2 enable bit) (b0)

Set the VW12E bit to 1 (enabled) when the VC27 bit in the VCR2 register is 1 (enabled).

7.2.4 Voltage Detector 2 Level Select Register (VD2LS)

Voltage Detector 2 Level Select Register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0				

Symbol	Address	Reset Value
VD2LS	0028h	0000 0100b (Hardware reset, power-on reset, voltage monitor 0 reset, voltage monitor 2 reset)

Bit Symbol	Bit Name	Function	RW
VD2LS0	Vdet2 select bit	b3 b2 b1 b0 0 0 0 0 : Vdet2_0 0 0 0 1 : Vdet2_1 0 0 1 0 : Vdet2_2 0 0 1 1 : Vdet2_3 0 1 0 0 : Vdet2_4 0 1 0 1 : Vdet2_5 0 1 1 0 : Vdet2_6 0 1 1 1 : Vdet2_7 Only set the values listed above.	RW
VD2LS1			RW
VD2LS2			RW
VD2LS3			RW
— (b7-b4)	Reserved bits	Set to 0.	RW

Set the PRC3 bit in the PRCR register to 1 (write enabled) before the VD2LS register is rewritten.
This register does not change at watchdog timer reset, oscillation stop detector reset, or software reset.
The value of the VD2LS register is affected by the VW12E bit in the VWCE register. Table 7.3 lists VD2LS Register Value. When setting the VW12E bit to 0 and then 1 after setting a value to the VD2LS register, the setting value to the VD2LS register is returned.

Table 7.3 VD2LS Register Value

VW12E Bit	Value of the VD2LS Register
0	0000 0100b
1	Value set in the VD2LS register (0000 0111b when no value is set in the VD2LS register)

VD2LS3-VD2LS0 (Vdet2 select bit) (b3-b0)

When using voltage detector 2, set the values shown in the VD2LS register diagram.
When not using voltage detector 2, the reset values can remain as is.

7.2.5 Voltage Monitor 0 Control Register (VW0C)

Voltage Monitor 0 Control Register

b7	b6	b5	b4	b3	b2	b1	b0
1	1	0	0		0	1	

Symbol	Address	Reset Value
VW0C	002Ah	1100 1X10b (1) 1100 1X11b (2)

Bit Symbol	Bit Name	Function	RW
VW0C0	Voltage monitor 0 reset enable bit	0 : Disabled 1 : Enabled	RW
— (b1)	Reserved bit	Set to 1	RW
— (b2)	Reserved bit	Set to 0. The read value is undefined.	RW
— (b3)	Reserved bit	The read value is undefined.	RO
— (b4)	Reserved bit	Set to 0	RW
— (b5)	Reserved bit	Set to 0	RW
— (b7-b6)	Reserved bits	Set to 1	RW

Notes:
1. When the LVDAS bit of the OFS1 address is 1 at hardware reset
2. This value shows the value after any of the following resets:
   - Voltage monitor 0 reset
   - When the LVDAS bit of the OFS1 address is 0 at hardware reset
   - Power-on reset

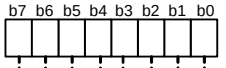
Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting to this register.
This register does not change at voltage monitor 2 reset, oscillator stop detect reset, watchdog timer reset, or software reset.

VW0C0 (Voltage monitor 0 reset enable bit) (b0)

The VW0C0 bit is enabled when the VC25 bit in the VCR2 register is 1 (voltage detector 0 enabled). Set the VW0C0 bit to 0 (disabled) when the VC25 bit is 0 (voltage detector 0 disabled). Set bit 6 in the VW0C register, as well, when setting the VW0C0 bit to 1 (enabled).

7.2.6 Voltage Monitor 2 Control Register (VW2C)

Voltage Monitor 2 Control Register



Symbol	Address	Reset Value
VW2C	002Ch	1000 0X10b (hardware reset, power-on reset, voltage monitor 0 reset)

Bit Symbol	Bit Name	Function	RW
VW2C0	Voltage monitor 2 interrupt/ reset enable bit	0 : Disabled 1 : Enabled	RW
VW2C1	Voltage monitor 2 digital filter disable mode select bit	0 : Digital filter enabled 1 : Digital filter disabled	RW
VW2C2	Voltage change detection flag	0 : Not detected 1 : Vdet2 passage detected	RW
VW2C3	Watchdog timer detection flag	0 : Not detected 1 : Watchdog timer underflow detected	RW
VW2F0	Sampling clock select bit	b5 b4 0 0 : fOCO-S divided by 1 0 1 : fOCO-S divided by 2 1 0 : fOCO-S divided by 4 1 1 : fOCO-S divided by 8	RW
VW2F1			
VW2C6	Voltage monitor 2 mode select bit	0 : Voltage monitor 2 interrupt at Vdet2 passage 1 : Voltage monitor 2 reset at Vdet2 passage	RW
VW2C7	Voltage monitor 2 interrupt/ reset generation condition select bit	0: When VCC reaches or goes above Vdet2 1: When VCC reaches or goes below Vdet2	RW

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW2C register.
Bits VW2C2 and VW2C3 do not change at voltage monitor 2 reset, oscillator stop detect reset, watchdog timer reset, or software reset.
When rewriting the VW2C register (excluding the VW2C3 bit), the VW2C2 bit may become 1. Set the VW2C2 bit to 0 after rewriting the VW2C register.

VW2C0 (Voltage monitor 2 interrupt/reset enable bit) (b0)

The VW2C0 bit is enabled when the VW12E bit in the VWCE register is 1 (voltage monitor 2 enabled) and the VC27 bit in the VCR2 register is 1 (voltage detector 2 enabled). Set the VW2C0 bit to 0 (disabled) when the VC27 bit is 0 (voltage detector 2 disabled).

VW2C1 (Voltage monitor 2 digital filter disable mode select bit) (b1)

After using the voltage monitor 2 interrupt to exit stop mode, to use it again to exit stop mode, set the VW2C1 bit to 0 first and then to 1.

VW2C2 (Voltage change detection flag) (b2)

The VW2C2 bit is enabled when the VC27 bit in the VCR2 register is 1 (voltage detector 2 enabled).
This bit does not change even if set to 1.
Condition to become 0:

- Writing this bit to 0

Condition to become 1:

- Refer to the following table.

Table 7.4 Conditions Under Which the VW2C2 Bit Becomes 1

Bit Setting (1)			Conditions under Which the VW2C2 Bit Becomes 1
VW2C1	VW2C6	VW2C7	
0	0	0 or 1	The VC13 bit changes from 0 to 1 or from 1 to 0.
	1	1	The VC13 bit changes from 1 to 0.
1	0	0	The VC13 bit changes from 0 to 1.
		1	The VC13 bit changes from 1 to 0.
	1	1	The VC13 bit changes from 1 to 0.

VC13 bit: Bit in the VCR1 register
Note:

1. Only set the values listed above.

VW2C6 (Voltage monitor 2 mode select bit) (b6)

The VW2C6 bit is enabled when the VW2C0 bit is 1 (voltage monitor 2 interrupt/reset enabled).

VW2C7 (Voltage monitor 2 interrupt/reset generation condition select bit) (b7)

The voltage monitor 2 interrupt/reset generation condition can be selected by the VW2C7 bit when the VW2C6 bit is 0 (voltage monitor 2 interrupt at Vdet2 passage) and the VW2C1 bit is 1 (digital filter disabled).
When the VW2C6 bit is 1 (voltage monitor 2 reset at Vdet2 passage), set the VW2C7 bit to 1 (when VCC reaches Vdet2 or below). (Do not set the VW2C7 bit to 0.)
When the VW2C1 bit is 0 (digital filter enabled), regardless of the VW2C7 bit setting, the voltage monitor 2 interrupt is generated when VCC reaches Vdet2 or above, and also when VCC reaches Vdet2 or below.

7.3 Optional Function Select Area

In the optional function select area, the MCU state after reset and the function to prevent rewrite in parallel I/O mode are selected.

The optional function select area is not an SFR, and therefore cannot be rewritten by a program. Set an appropriate value when writing a program to flash memory. The entire optional function select area becomes FFh when the block including the optional function select area is erased.

In blank products, the OFS1 address value is FFh when shipped. After a value is written by the user, this address takes on the written value.

In programmed products, the OFS1 address value is the value set in the user program prior to shipping.

7.3.1 Optional Function Select Address 1 (OFS1)

Optional Function Select Address 1

b7	b6	b5	b4	b3	b2	b1	b0
		0	1			1	

Symbol: OFS1

Address: FFFFFh

Bit Symbol	Bit Name	Function
WDTON	Watchdog timer start select bit	0 : Watchdog timer starts automatically after reset. 1 : Watchdog timer is in a stopped state after reset.
— (b1)	Reserved bit	Set to 1.
ROMCR	ROM code protect cancel bit	0 : ROM code protection cancelled. 1 : ROMCP1 bit enabled.
ROMCP1	ROM code protect bit	0 : ROM code protection enabled. 1 : ROM code protection cancelled.
— (b4)	Reserved bit	Set to 1.
— (b5)	Reserved bit	Set to 0.
LVDAS	Voltage detector 0 start bit	0 : Voltage monitor 0 reset enabled after hardware reset. 1 : Voltage monitor 0 reset disabled after hardware reset.
CSPROINI	After-reset count source protection mode select bit	0 : Count source protection mode enabled after reset. 1 : Count source protection mode disabled after reset.

LVDAS (Voltage detector 0 start bit) (b6)

When using power-on reset, set this bit to 0 (voltage monitor 0 reset enabled after hardware reset). This bit is enabled in single-chip mode, while disabled in boot mode.

7.4 Operations

7.4.1 Digital Filter

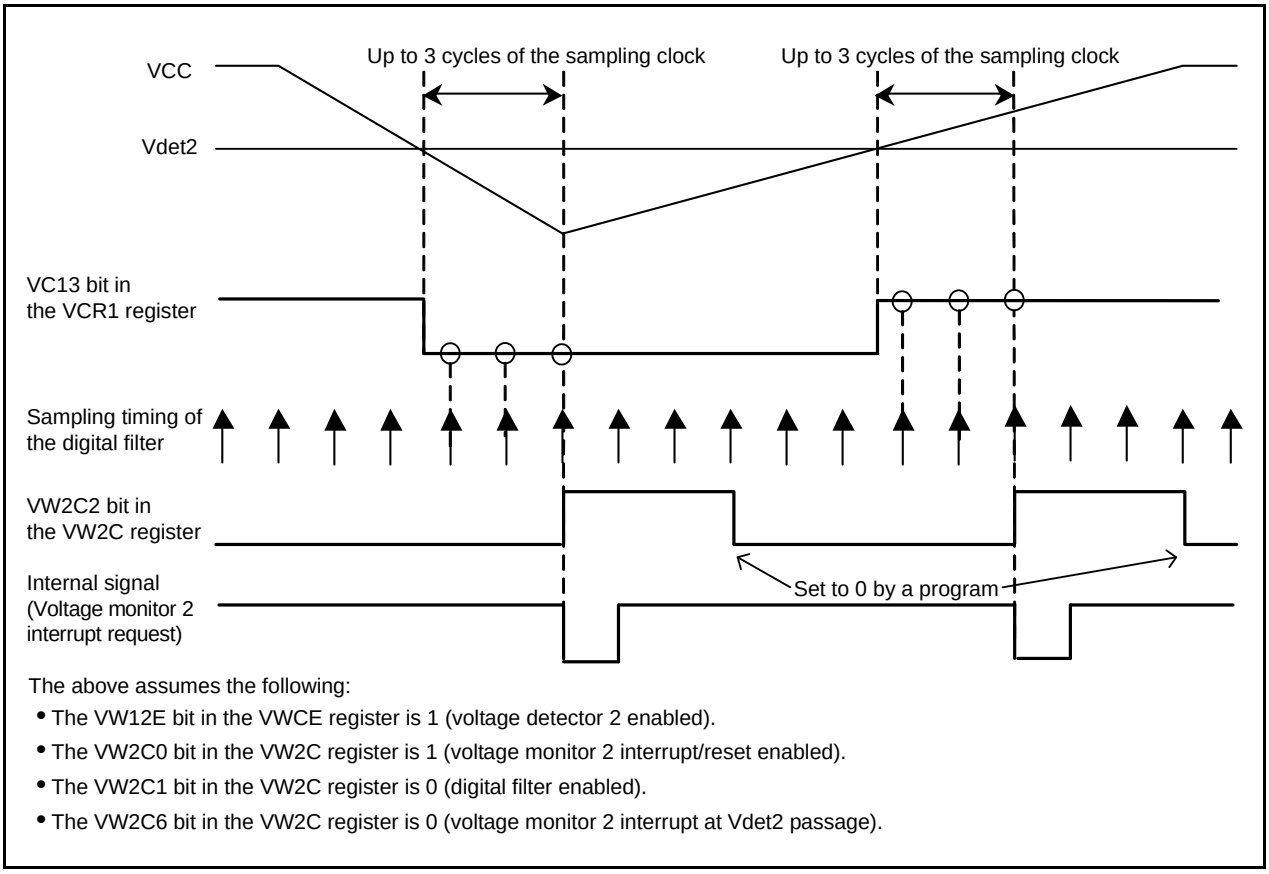
A digital filter can be used to monitor VCC input voltage. For voltage detector 2, the digital filter is enabled when the VW2C1 bit in the VW2C register is set to 0 (digital filter enabled).

fOCO-S divided by 1, 2, 4, or 8 is selected as a sampling clock. When using the digital filter, set the CM14 bit in the CM1 register to 0 (125 kHz on-chip oscillator on).

The VCC input level is sampled by the digital filter for every sampling clock. When the same sampled level is detected three times in a row, at the third sampling timing, the internal reset signal goes low or a voltage monitor 2 interrupt request is generated. Therefore, when the digital filter is used, the time from when the VCC input voltage level passes Vdet2 until when a reset or an interrupt is generated is up to three cycles of the sampling clock.

Since fOCO-S stops in stop mode, the digital filter does not function. When using voltage detector 2 to exit stop mode, set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).

Figure 7.2 shows Digital Filter Operation Example.



The above assumes the following:

- The VW12E bit in the VWCE register is 1 (voltage detector 2 enabled).
- The VW2C0 bit in the VW2C register is 1 (voltage monitor 2 interrupt/reset enabled).
- The VW2C1 bit in the VW2C register is 0 (digital filter enabled).
- The VW2C6 bit in the VW2C register is 0 (voltage monitor 2 interrupt at Vdet2 passage).

Figure 7.2 Digital Filter Operation Example

7.4.2 Voltage Detector 0

When the VC25 bit in the VCR2 register is 1 (voltage detector 0 enabled), voltage detector 0 monitors the voltage applied to the VCC pin and detects whether the voltage rises through or falls through Vdet0.

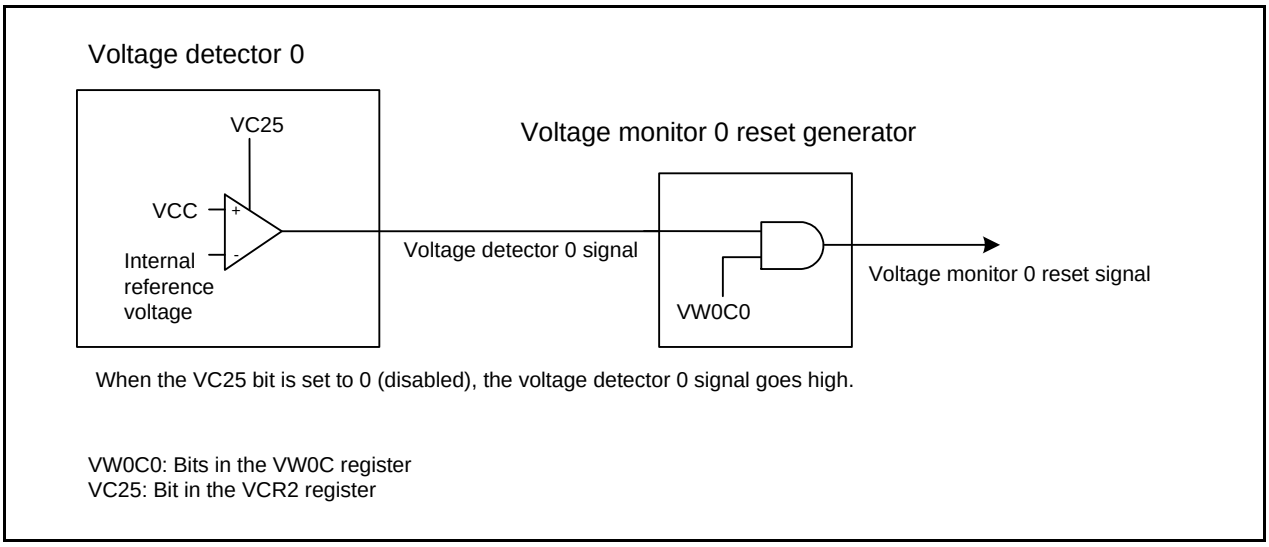


Figure 7.3 Voltage Monitor 0 Reset Generator Block Diagram

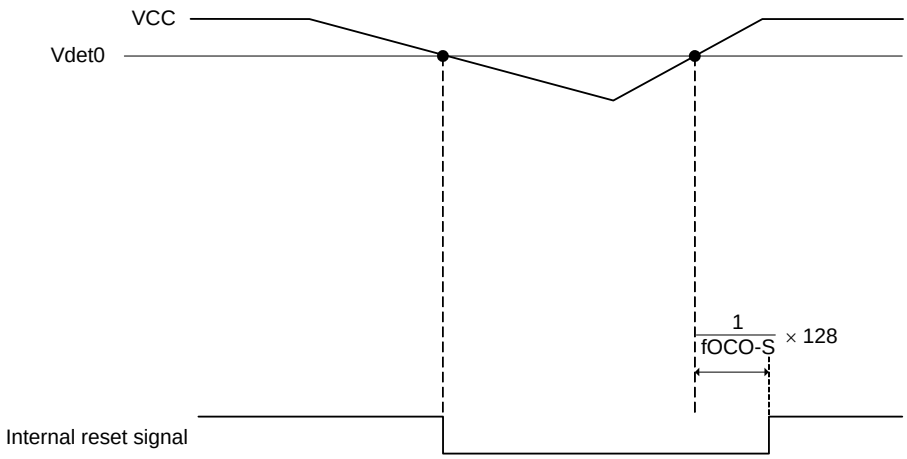
7.4.2.1 Voltage Monitor 0 Reset

Table 7.5 lists Steps to Set Voltage Monitor 0 Reset Related Bits.

Table 7.5 Steps to Set Voltage Monitor 0 Reset Related Bits

Step	
1	Set the VC25 bit in the VCR2 register to 1 (voltage detector 0 enabled).
2	Wait for td(E-A).
3	Set bits 6 and 7 in the VW0C register to 1.
4	Set bit 2 in the VW0C register to 0 (set this bit to 0 once again after step 3).
5	Set the VW0C0 bit in the VW0C register to 1 (voltage monitor 0 reset enabled).

Figure 7.4 shows Voltage Monitor 0 Reset Operation Example.



The above assumes the following:
- The VC25 bit in the VCR2 register is 1 (voltage detector 0 enabled).
- The VW0C0 bit in the VW0C register is 1 (voltage monitor 0 reset enabled).

The pins, CPU, and SFRs are initialized when the internal reset signal goes low.
The MCU executes the program at the address indicated by the reset vector when the internal reset signal changes from low to high.
Refer to 4. “Special Function Registers (SFRs)” for the SFR status after reset.

Figure 7.4 Voltage Monitor 0 Reset Operation Example

7.4.3 Voltage Detector 2

When the VW12E bit in the VWCE register is 1 (voltage monitor 2 enabled) and the VC27 bit in the VCR2 register is 1 (voltage detector 2 enabled), voltage detector 2 monitors the voltage applied to the VCC pin and detects whether the voltage rises through or falls through Vdet2.

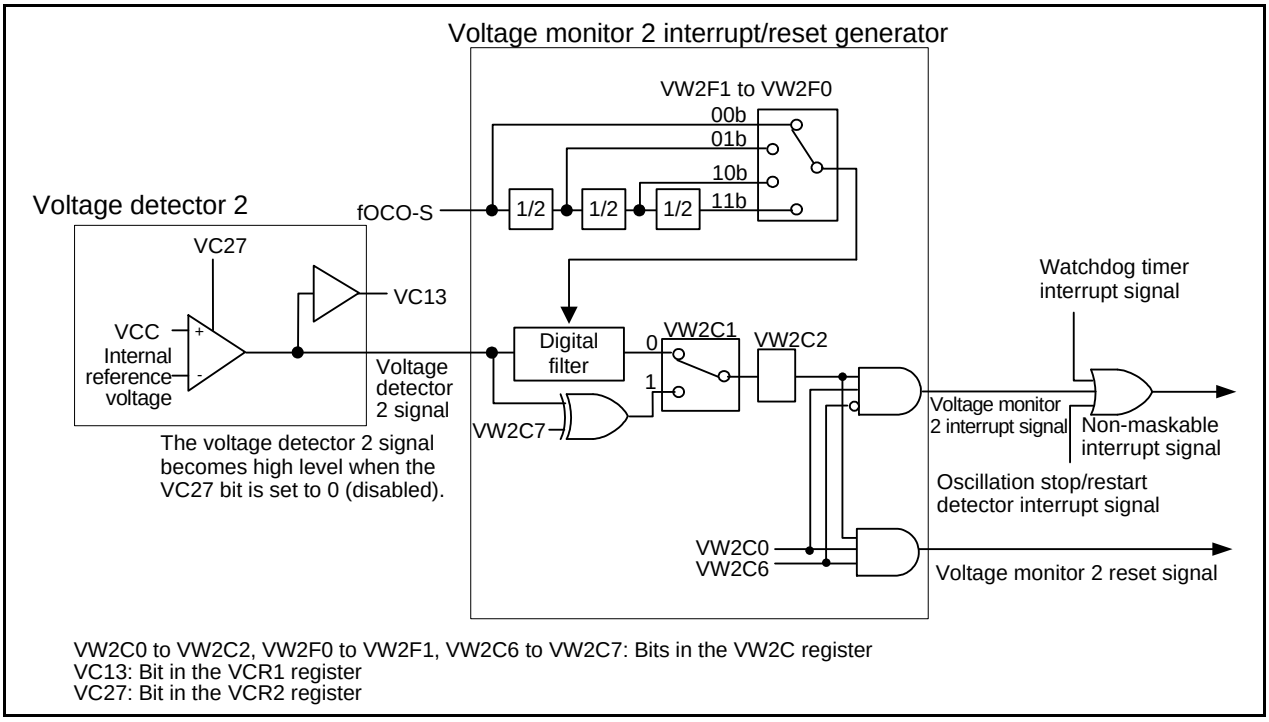


Figure 7.5 Voltage Monitor 2 Interrupt/Reset Generator

7.4.3.1 Monitoring Vdet2

Set the VW12E bit in the VWCE register to 1 (voltage monitor 2 enabled) and the VC27 bit in the VCR2 register to 1 (voltage detector 2 enabled). Vdet2 can be monitored using the VC13 bit in the VCR1 register after td(E-A) elapses.

7.4.3.2 Voltage Monitor 2 Interrupt and Voltage Monitor 2 Reset

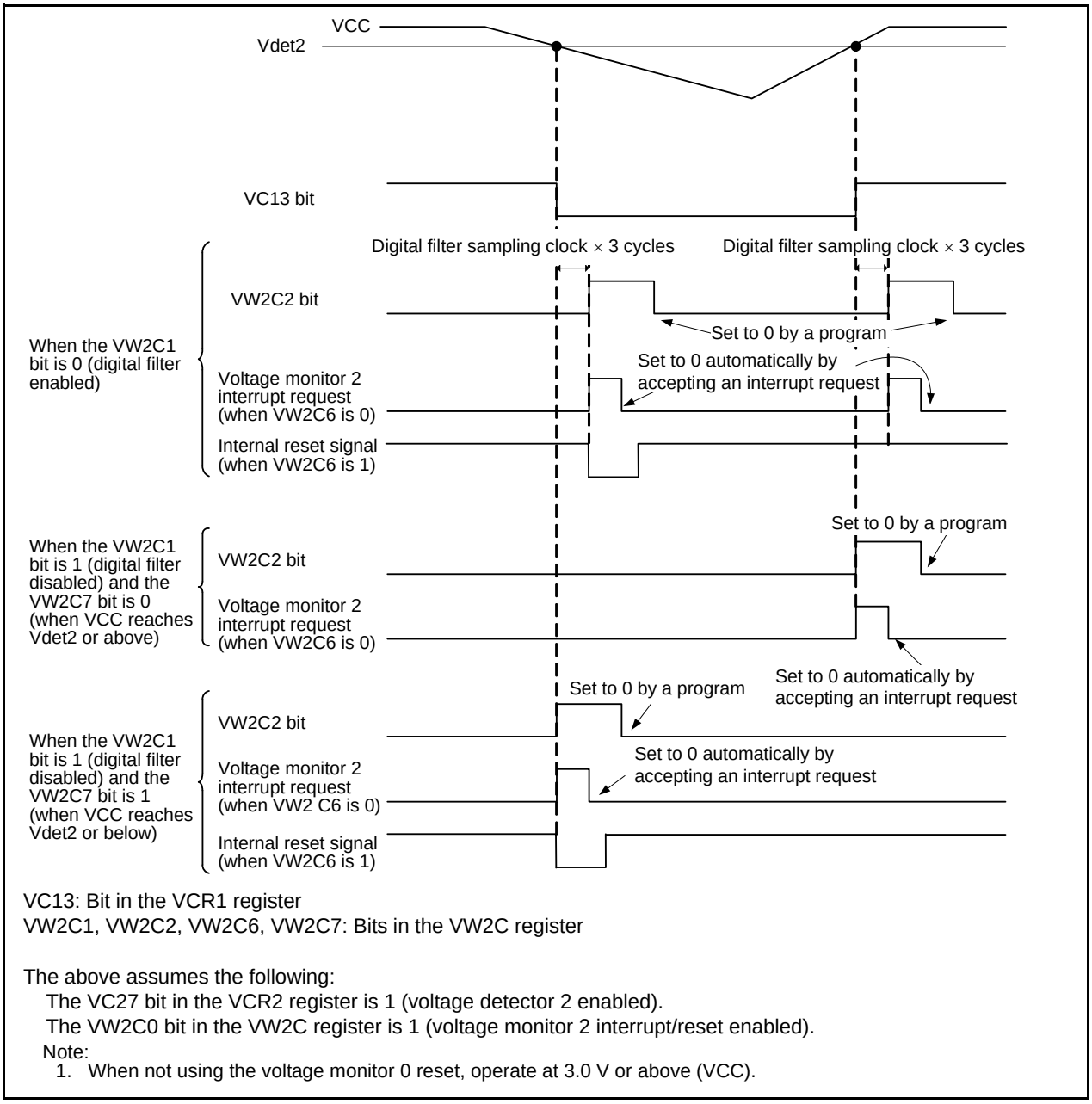
Table 7.6 lists Procedure for Setting Voltage Monitor 2 Interrupt/Reset Related Bits.

Table 7.6 Procedure for Setting Voltage Monitor 2 Interrupt/Reset Related Bits

Step	When Using the Digital Filter		When Not Using the Digital Filter	
	Voltage Monitor 2 Interrupt	Voltage Monitor 2 Reset	Voltage Monitor 2 Interrupt	Voltage Monitor 2 Reset
1	Set the CM14 bit in the CM1 register to 0 (125 kHz on-chip oscillator on)		—	
2	Wait for digital filter sampling clock x 3 cycles.		— (no wait time)	
3	Set the VW12E bit in the VWCE register to 1 (voltage detector enabled).			
4	Use bits VD2LS3 to VD2LS0 in the VD2LS register to select Vdet2.			
5	Set the VC27 bit in the VCR2 register to 1 (voltage detector 2 enabled).			
6	Wait for td(E-A).			
7	Use bits VW2F0 to VW2F1 in the VW2C register to select the digital filter sampling clock.		Use the VW2C7 bit in the VW2C register to select the timing of the interrupt and reset request. (1)	
8 (2)	Set the VW2C1 bit in the VW2C register to 0 (digital filter enabled).		Set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).	
9 (2)	Set the VW2C6 bit in the VW2C register to 0 (voltage monitor 2 interrupt mode).	Set the VW2C6 bit in the VW2C register to 1 (voltage monitor 2 reset mode).	Set the VW2C6 bit in the VW2C register to 0 (voltage monitor 2 interrupt mode).	Set the VW2C6 bit in the VW2C register to 1 (voltage monitor 2 reset mode).
10	Set the VW2C2 bit in the VW2C register to 0 (Vdet2 passage not detected).			
11	Set the VW2C0 bit in the VW2C register to 1 (voltage monitor 2 interrupt/reset enabled).			

Notes:
1. Set the VW2C7 bit to 1 (when VCC reaches Vdet2 or below) for the voltage monitor 2 reset.
2. When the VW2C0 bit is 0, steps 7, 8, and 9 can be executed simultaneously (with one instruction).

When using voltage monitor 2 interrupt or voltage monitor 2 reset to exit stop mode, set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).
When voltage monitor 2 reset is generated, the LVD2R bit in the RSTFR register is automatically becomes 1 (voltage monitor 2 reset detected). Refer to 6.4.5 “Voltage Monitor 2 Reset” for status after reset.
Figure 7.6 shows Voltage Monitor 2 Interrupt/Reset Operation Example.



VC13: Bit in the VCR1 register
VW2C1, VW2C2, VW2C6, VW2C7: Bits in the VW2C register

The above assumes the following:
The VC27 bit in the VCR2 register is 1 (voltage detector 2 enabled).
The VW2C0 bit in the VW2C register is 1 (voltage monitor 2 interrupt/reset enabled).

Note:
1. When not using the voltage monitor 0 reset, operate at 3.0 V or above (VCC).

Figure 7.6 Voltage Monitor 2 Interrupt/Reset Operation Example

7.5 Interrupts

The voltage monitor 2 interrupt is a non-maskable interrupt.

The watchdog timer interrupt, oscillator stop/restart detect interrupt, and voltage monitor 2 interrupt share the same vector. When using some functions together, read the detect flags of the events in an interrupt processing program, and determine the source of the interrupt.

The detect flag for voltage monitor 2 is the VW2C2 bit in the VW2C register. After the interrupt source is determined, set the VW2C2 bit to 0 (not detected).

8. Clock Generator

8.1 Introduction

The clock generator generates operating clocks for the CPU and peripheral functions. The following circuits are incorporated to generate the system clock signals.

- Main clock oscillator
- PLL frequency synthesizer
- 40 MHz on-chip oscillator
- 125 kHz on-chip oscillator
- Sub clock oscillator

Table 8.1 lists the specifications of the clock generator, and Figure 8.1 shows the block diagram of system clock generator.

Table 8.1 Clock Generator Specifications

Item	Main Clock Oscillator	PLL Frequency Synthesizer	On-Chip Oscillator		Sub Clock Oscillator
			40 MHz on-chip oscillator	125 kHz on-chip oscillator	
Application	• CPU clock source • Peripheral function clock source	• CPU clock source • Peripheral function clock source	• CPU clock source • Peripheral function clock source • CPU and peripheral function clock sources when the main clock stops oscillating	• CPU clock source • Peripheral function clock source • CPU and peripheral function clock sources when the main clock stops oscillating • Watchdog timer count source when the CPU clock is stopped	• CPU clock source • Peripheral function clock source
Clock frequency	f(XIN)	f(PLL)	fOCO40M	fOCO-S	f(XCIN)
Connectable oscillators	• Ceramic resonator • Crystal	- (see note 1)	-	-	Crystal
Pins connecting to oscillator	XIN, XOUT	- (see note 1)	-	-	XCIN, XCOUT
Oscillator start/ stop function	Enabled	Enabled	Enabled	Enabled	Enabled
Oscillator status after reset	Oscillating	Stopped	Stopped	Oscillating	Stopped
Other	An externally generated clock can be input.	- (see note 1)	-	-	-

Note:
1. The PLL frequency synthesizer uses the main clock oscillator as a reference clock source. The items above are based on the main clock oscillator.

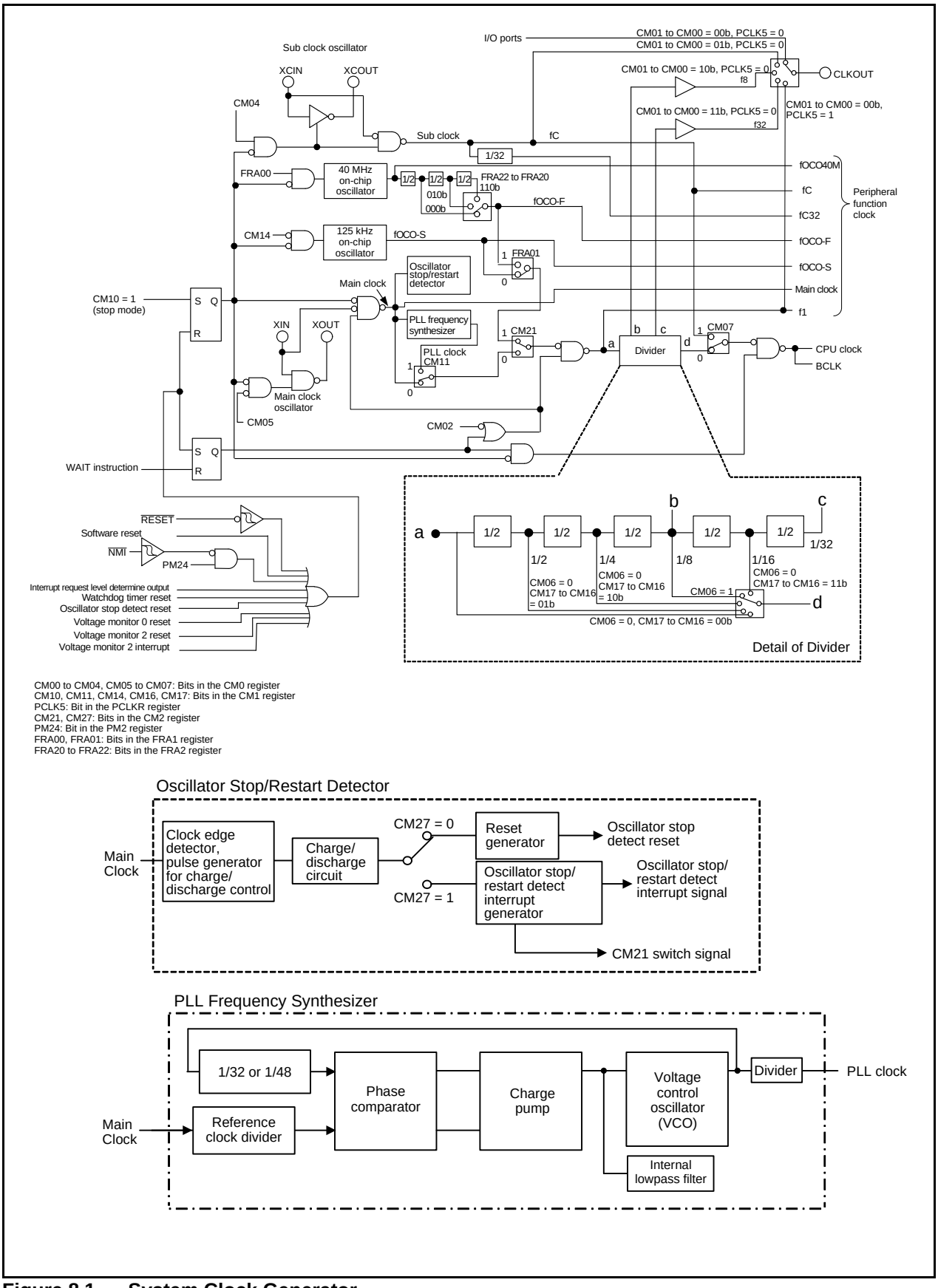


Figure 8.1 System Clock Generator

Table 8.2 I/O Pins

Pin Name	I/O	Function
XIN	Input	I/O pins for the main clock oscillator
XOUT	Output	
XCIN	Input (1)	I/O pins for a sub clock oscillator
XCOUT	Output (1)	
CLKOUT	Output	Clock output

Note:
1. Set the port direction bits which share pins to 0 (input mode).

8.2 Registers

Table 8.3 Registers

Address	Register	Symbol	Reset Value
0006h	System Clock Control Register 0	CM0	0100 1000b
0007h	System Clock Control Register 1	CM1	0010 0000b
000Ch	Oscillation Stop Detection Register	CM2	0X00 0010b (1)
0012h	Peripheral Clock Select Register	PCLKR	0000 0011b
001Ch	PLL Control Register 0	PLC0	0X01 X010b
001Eh	Processor Mode Register 2	PM2	XX00 0X01b
0022h	40 MHz On-Chip Oscillator Control Register 0	FRA0	XXXX XX00b
0024h	40 MHz On-Chip Oscillator Control Register 2	FRA2	0XX0 X000b

Note:
1. Bits CM20, CM21, and CM27 remain unchanged at oscillator stop detect reset.

8.2.1 System Clock Control Register 0 (CM0)

System Clock Control Register 0

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	Reset Value
CM0	0006h	0100 1000b

Bit Symbol	Bit Name	Function	RW
CM00	Clock output function select bit	b1 b0 0 0 : I/O port 0 1 : Output fC 1 0 : Output f8 1 1 : Output f32	RW
CM01			
CM02	Wait mode peripheral function clock stop bit	0 : Peripheral function clock f1 does not stop in wait mode 1 : Peripheral function clock f1 stops in wait mode	RW
CM03	XCIN-XCOUT drive capacity select bit	0 : Low 1 : High	RW
CM04	Port XC select bit	0 : I/O port 1 : XCIN-XCOUT oscillation function	RW
CM05	Main clock stop bit	0 : On 1 : Off	RW
CM06	Main clock division select bit 0	0 : Bits CM16 and CM17 in the CM1 register enabled 1 : Divide-by-8 mode	RW
CM07	System clock select bit	0 : Main clock, PLL clock, or on-chip oscillator clock 1 : Sub clock	RW

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting this register.
See Table 9.3 “Clock-Related Bit Setting and Modes” to select a clock and mode.

CM01 and CM00 (Clock output function select bit) (b1-b0)

The CLKOUT pin outputs can be selected. These bits are enabled when the PCLK5 bit in the PCLKR register is set to 0. When the PCLK5 bit is 1, set bits CM01 and CM00 to 00b. Table 8.4 lists CLKOUT Pin Functions.

Table 8.4 CLKOUT Pin Functions

PCLKR Register	CM0 Register		CLKOUT Pin Output
PCLK5 bit	CM01 bit	CM00 bit	
0	0	0	I/O port
0	0	1	fC is output
0	1	0	f8 is output
0	1	1	f32 is output
1	0	0	f1 is output

Only set the combinations listed above.

CM02 (Wait mode peripheral function clock stop bit) (b2)

This bit is used to stop the f1 peripheral function clock in wait mode. fC, fC32, fOCO-S, fOCO-F, and fOCO40M are not affected by the CM02 bit.
When the PM21 bit in the PM2 register is 1 (clock change disabled), the CM02 bit remains unchanged even when written to.

CM03 (XCIN-XCOUT drive capacity select Bit) (b3)

Setting the driving capacity to low while sub clock oscillation is stable reduces power consumption.
The CM03 bit becomes 1 (high) while the CM04 bit is 0 (P8_6 and P8_7 are I/O ports), or when entering stop mode.

CM04 (Port XC select bit) (b4)

The CM03 bit becomes 1 (high) while the CM04 bit is 0 (P8_6 and P8_7 are I/O ports).

CM05 (Main clock stop bit) (b5)

This bit is used to stop the main clock. The main clock is allowed to stop in the following cases.

- Entering low power mode
- Entering 125 kHz on-chip oscillator low power mode
- Stopping the main clock in 40 MHz on-chip oscillator mode

This bit cannot be used to detect if the main clock is stopped or not. Refer to 8.7 “Oscillator Stop/Restart Detect Function” for details on main clock stop detection.
When the PM21 bit in the PM2 register is 1 (clock change disabled), this bit remains unchanged even when written to.

CM06 (Main clock division select bit) (b6)

The CM06 bit becomes 1 (divide-by-8 mode) under the following conditions:

- When entering stop mode
- When the CM21 bit in the CM2 register is 0 (main clock or PLL clock) and the CM05 bit is 1 (main clock off)

CM07 (System clock select bit) (b7)

The CPU clock source and the peripheral function clock f1 depend on combinations of the bit status of the CM07 bit, the CM11 bit in the CM1 register, and the CM21 bit in the CM2 register. When the CM07 bit is 0 (main clock, PLL clock or on-chip oscillator clock used as CPU clock), the CPU clock source and the peripheral function clock f1 can be selected by combinations of the bit status of the CM11 bit and the CM21 bit. When the CM07 bit is 1 (sub clock used as CPU clock), the CPU clock source is fC, and the peripheral function clock f1 can be selected by combinations of the bit status of bits CM11 and CM21.
When setting the PM21 bit in the PM2 register to 1 (clock change disabled), set the CM07 bit to 0 (main clock) before setting the PM21 bit to 1. When the PM21 bit is set to 1, this bit remains unchanged even when written to.

8.2.2 System Clock Control Register 1 (CM1)

System Clock Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0
					0		

Symbol	Address	Reset Value
CM1	0007h	0010 0000b

Bit Symbol	Bit Name	Function	RW
CM10	All clock stop control bit	0 : Clock on 1 : All clocks off (stop mode)	RW
CM11	System clock select bit 1	0 : Main clock 1 : PLL clock	RW
— (b2)	Reserved bit	Set to 0	RW
CM13	XIN-XOUT feedback resistor select bit	0 : Internal feedback resistor connected 1 : Internal feedback resistor not connected	RW
CM14	125 kHz on-chip oscillator stop bit	0 : 125 kHz on-chip oscillator on 1 : 125 kHz on-chip oscillator off	RW
CM15	XIN-XOUT drive capacity select bit	0 : Low 1 : High	RW
CM16	Main clock division select bit 1	b7 b6 0 0 : No division mode 0 1 : Divide-by-2 mode 1 0 : Divide-by-4 mode 1 1 : Divide-by-16 mode	RW
CM17			

Rewrite the CM1 register after setting the PRC0 bit in the PRCR register to 1 (write enabled).
See Table 9.3 “Clock-Related Bit Setting and Modes” to select a clock and a mode.

CM10 (All clock stop control bit) (b0)

When the CM11 bit is 1 (PLL clock), or the CM20 bit in the CM2 register is 1 (oscillator stop/restart detect function enabled), do not set the CM10 bit to 1.
In the following cases, this bit remains unchanged even when written to (The MCU does not enter stop mode).

- The PM21 bit in the PM2 register is 1 (clock change disabled).
- The CSPRO bit in the CSPR register is 1 (watchdog timer count source protection mode enabled).
- The PLC07 bit in the PLC0 register is 1 (PLL on).
- A low is input to the $\overline{\text{NMI}}$ pin.

CM11 (System clock select bit) (b1)

The CM11 bit is valid when the CM21 bit in the CM2 register is set to 0 (main clock or PLL clock).
The CPU clock source and the peripheral function clock f1 can be selected by the CM11 bit when the CM07 bit is 0 (main clock, PLL clock, or on-chip oscillator clock used as CPU clock). The peripheral function clock f1 can be selected by the CM11 bit when the CM07 bit is 1 (sub clock used as CPU clock).
When the PM21 bit in the PM2 register is 1 (clock change disabled), the CM11 bit remains unchanged even when written to.

CM13 (XIN-XOUT feedback resistor select bit) (b3)

The CM13 bit can be used when the main clock is not used at all, or when the externally generated clock is supplied to the XIN pin. When connecting a ceramic resonator or crystal between pins XIN and XOUT, set the CM13 bit to 0 (internal feedback resistor connected). Do not set this bit to 1.
When the CM10 bit is 1 (stop mode), the feedback resistor is not connected regardless of the CM13 bit value.

CM14 (125 kHz on-chip oscillator stop bit) (b4)

The CM14 bit can be set to 1 (125 kHz on-chip oscillator off) when the CM21 bit is 0 (main clock or PLL clock). When the CM21 bit is set to 1 (on-chip oscillator clock), the CM14 bit is automatically set to 0 (125 kHz on-chip oscillator on) and remains unchanged even when 1 is written to this bit. Note that the 125 kHz on-chip oscillator does not stop.
When the CSPRO bit in the CSPR register is 1 (watchdog timer count source protection mode), the CM14 bit is automatically set to 0 (125 kHz on-chip oscillator on) and remains unchanged even when 1 is written to this bit. Note that the 125 kHz on-chip oscillator does not stop.

CM15 (XIN-XOUT drive capacity select bit) (b5)

In the following cases, the CM15 bit is fixed as 1 (drive capacity high):

- Entering stop mode.
- The CM21 bit in the CM2 register is 0 (main clock or PLL clock) and the CM05 bit in the CM0 register is set to 1 (main clock stopped).

CM17 and CM16 (Main clock division select bit 1) (b7-b6)

Bits CM17 and CM16 are enabled when the CM06 bit is 0 (bits CM17 and CM16 enabled).

8.2.3 Oscillation Stop Detection Register (CM2)

Oscillation Stop Detection Register

b7	b6	b5	b4	b3	b2	b1	b0
	X	0	0				

Symbol	Address	Reset Value
CM2	000Ch	0X00 0010b

Bit Symbol	Bit Name	Function	RW
CM20	Oscillator stop/restart detect enable bit	0: Oscillator stop/restart detect function disabled 1: Oscillator stop/restart detect function enabled	RW
CM21	System clock select bit 2	0: Main clock or PLL clock 1: On-chip oscillator clock	RW
CM22	Oscillator stop/restart detect flag	0: Main clock stop/restart not detected 1: Main clock stop/restart detected	RW
CM23	XIN monitor flag	0: Main clock oscillating 1: Main clock stopped	RO
— (b5-b4)	Reserved bits	Set to 0	RW
— (b6)	No register bit. If necessary, set to 0. The read value is undefined.		—
CM27	Operation select bit (when an oscillator stop/restart is detected)	0: Oscillator stop detect reset 1: Oscillator stop/restart detect interrupt	RW

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting this register.
Bits CM20, CM21, and CM27 do not change at oscillator stop detect reset.
See Table 9.3 “Clock-Related Bit Setting and Modes” to select a clock and a mode.

CM20 (Oscillator stop/restart detect enable bit) (b0)

Set the CM20 bit to 0 (oscillator stop/restart detect function disabled) to enter stop mode. Set the CM20 bit back to 1 (enabled) after exiting stop mode.
When the PM21 bit in the PM2 register is 1 (clock change disabled), the CM20 bit remains unchanged even when being written.

CM21 (System clock select bit 2) (b1)

When the CM07 bit is 0 (main clock, PLL clock, or on-chip oscillator clock used as CPU clock source), the CPU clock source and the peripheral function clock f1 can be selected by the CM21 bit. When the CM07 bit is 1 (sub clock used as CPU clock source), the peripheral function clock f1 can be selected by the CM21 bit.
To set the CM21 bit to 1 (on-chip oscillator clock), set the FRA01 bit in the FRA0 register to select either the 125 kHz on-chip oscillator, or the 40 MHz on-chip oscillator.
When the CM20 bit is 1 (oscillator stop/restart detect function enabled) and the CM23 bit is 1 (main clock stopped), do not set the CM21 bit to 0 (main clock or PLL clock).
When the CM20 bit is 1 (oscillator stop/restart detect function enabled), the CM27 bit is 1 (oscillator stop/restart detect interrupt), and the main clock is used as a CPU clock source, the CM21 bit becomes 1 (on-chip oscillator clock) if the main clock stop is detected. Refer to 8.7 “Oscillator Stop/Restart Detect Function” for details.

CM22 (Oscillator stop/restart detect flag) (b2)

Condition to become 0:

- Set it to 0.

Conditions to become 1:

- Main clock stop is detected.
- Main clock restart is detected.
  (The CM22 bit remains unchanged even if 1 is written.)

When the CM22 bit changes state from 0 to 1, an oscillator stop/restart detect interrupt is generated. Use this bit in an interrupt routine to determine the factors of interrupts between the oscillator stop/restart detect interrupt and other interrupts.

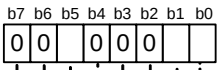
When the CM22 bit is 1 and oscillator stop or restart is detected, an oscillator stop/restart detect interrupt is not generated. The bit does not become 0 even if an oscillator stop/restart detect interrupt request is accepted.

CM23 (XIN monitor flag) (b3)

Determine the main clock status by reading the CM23 bit several times in the oscillator stop/restart detect interrupt routine.

8.2.4 Peripheral Clock Select Register (PCLKR)

Peripheral Clock Select Register



Symbol	Address	Reset Value
PCLKR	0012h	00000011b

Bit Symbol	Bit Name	Function	RW
PCLK0	Timers A, B, S, multi-master I^2C-bus interface clock select bit (clock source for timers A , B, S, dead time timer, and multi-master I^2C-bus interface)	0: f2TIMAB/f2IIC 1: f1TIMAB/f1IIC	RW
PCLK1	SI/O clock select bit (clock source for UART0 to UART4)	0: f2SIO 1: f1SIO	RW
— (b4-b2)	Reserved bits	Set to 0.	RW
PCLK5	Clock output function extension bit	0: Selected by setting bits CM01 and CM00 in the CM0 register 1: Outputs f1	RW
— (b7-b6)	Reserved bits	Set to 0.	RW

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting this register.

PCLK5 (Clock output function extension bit) (b5)

Output from the CLKOUT pin is selectable. When the PCLK5 bit is 1, set bits CM01 and CM00 to 00b. See Table 8.4 “CLKOUT Pin Functions”.

8.2.5 PLL Control Register 0 (PLC0)

PLL Control Register 0

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	Reset Value
PLC0	001Ch	0X01 X010b

Bit Symbol	Bit Name	Function	RW
PLC00	PLL multiplying factor select bit	b2 b1 b0 0 0 0 : Do not set 0 0 1 : Multiply-by-2 0 1 0 : Multiply-by-4 0 1 1 : Multiply-by-6 1 0 0 : Multiply-by-8 1 0 1 : 1 1 0 : Do not set these values 1 1 1 :	RW
PLC01			RW
PLC02			RW
— (b3)	Reserved bit	The read value is undefined	RO
PLC04	Reference frequency counter set bit	b5 b4 0 0 : No division 0 1 : Divide-by-2 1 0 : Divide-by-4 1 1 : Do not set	RW
PLC05			RW
— (b6)	No register bit. If necessary, set to 0. The read value is undefined.		—
PLC07	Operation enable bit	0 : PLL off 1 : PLL on	RW

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting this register.

PLC02 to PLC00 (PLL multiplying factor select bit) (b2-b0)

Write to bits PLC00 to PLC02 when the PLC07 bit is 0 (PLL off).
When the PM21 bit in the PM2 register is 1 (clock change disabled), writing to bits PLC02 to PLC00 has no effect.

PLC05 and PLC04 (Reference frequency counter set bit) (b5-b4)

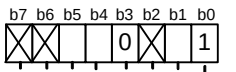
Write to bits PLC05 and PLC04 when the PLC07 bit is 0 (PLL off).
When the PM21 bit in the PM2 register is 1 (clock change disabled), writing to bits PLC05 and PLC04 has no effect.

PLC07 (Operation enable bit) (b7)

When the PM21 bit in the PM2 register is 1 (clock change disabled), writing to the PLC07 bit has no effect.

8.2.6 Processor Mode Register 2 (PM2)

Processor Mode Register 2



Symbol: PM2 | Address: 001Eh | Reset Value: XX00 0X01b

Bit Symbol	Bit Name	Function	RW
— (b0)	Reserved bit	Set to 1.	RW
PM21	System clock protection bit	0 : Clock is protected by PRCR register 1 : Clock change disabled	RW
— (b2)	No register bit. If necessary, set to 0. The read value is undefined.		—
— (b3)	Reserved bit	Set to 0	RW
PM24	$\overline{\text{NMI}}$ interrupt enable bit	0 : $\overline{\text{NMI}}$ interrupt disabled 1 : $\overline{\text{NMI}}$ interrupt enabled	RW
PM25	Peripheral clock fC provide bit	0 : Not provided 1 : Provided	RW
— (b7-b6)	No register bits. If necessary, set to 0. The read value is undefined.		—

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting this register.

PM21 (System clock protection bit) (b1)

The PM21 bit is used to protect the CPU clock. (Refer to 8.6 “System Clock Protection Function”).
When the PM21 bit is set to 1, writing to the following bits has no effect:

- Bits CM02, CM05, and CM07 in the CM0 register
- Bits CM10 and CM11 in the CM1 register
- The CM20 bit in the CM2 register
- All bits in the PLC0 register

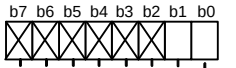
Do not execute the WAIT instruction when the PM21 bit is 1.
Once the PM21 bit is set to 1, it cannot be set to 0 by a program (writing 0 has no effect).

PM25 (Peripheral clock fC provide bit) (b5)

The PM25 bit provides fC to the real-time clock. (See Figure 8.5 “Peripheral Function Clocks”.)

8.2.7 40 MHz On-Chip Oscillator Control Register 0 (FRA0)

40 MHz On-Chip Oscillator Control Register 0



Symbol	Address	Reset Value
FRA0	0022h	XXXX XX00b

Bit Symbol	Bit Name	Function	RW
FRA00	40 MHz on-chip oscillator start bit	0 : 40 MHz on-chip oscillator off 1 : 40 MHz on-chip oscillator on	RW
FRA01	On-chip oscillator select bit	0 : 125 kHz on-chip oscillator 1 : 40 MHz on-chip oscillator	RW
— (b7-b2)	No register bits. If necessary, set to 0. The read value is undefined.		—

Rewrite the FRA0 register after setting the PRC0 bit in the PRCR register to 1 (write enabled).
See Table 9.3 “Clock-Related Bit Setting and Modes”to select a clock and a mode.

FRA00 (40 MHz on-chip oscillator start bit) (b0)

When using an oscillator stop/restart detect interrupt, do not set the FRA00 bit to 0 (40 MHz on-chip oscillator off) while the FRA01 bit to 1 (40 MHz on-chip oscillator), and vice versa.

FRA01 (On-chip oscillator select bit) (b1)

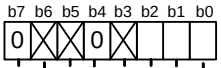
Change the FRA01 bit if the both of the following conditions are met:

- When the FRA00 bit is 1 (40 MHz on-chip oscillator on) and oscillation is stable
- When the CM14 bit in the CM1 register is 0 (125 kHz on-chip oscillator on) and oscillation is stable

When setting the FRA01 bit to 0 (125 kHz on-chip oscillator), do not set the FRA00 bit to 0 (40 MHz on-chip oscillator off) at the same time. Set the FRA00 bit to 0 after setting the FRA01 bit to 0.

8.2.8 40 MHz On-Chip Oscillator Control Register 2 (FRA2)

40 MHz On-Chip Oscillator Control Register 2



Symbol	Address	Reset Value
FRA2	0024h	0XX0 X000b

Bit Symbol	Bit Name	Function	RW
FRA20	40 MHz on-chip oscillator division select bit	b2 b1 b0 0 0 0: Divide-by-2 mode 0 1 0: Divide-by-4 mode 1 1 0: Divide-by-8 mode Other than the above : Do not set	RW
FRA21			RW
FRA22			RW
— (b3)	No register bit. If necessary, set to 0. The read value is undefined.		—
— (b4)	Reserved bit	Set to 0.	RW
— (b6-b5)	No register bits. If necessary, set to 0. The read value is undefined.		—
— (b7)	Reserved bit	Set to 0.	RW

Set the FRA2 register after the PRC0 bit in the PRCR register is set to 1 (write enabled).

8.3 Clocks Generated by Clock Generators

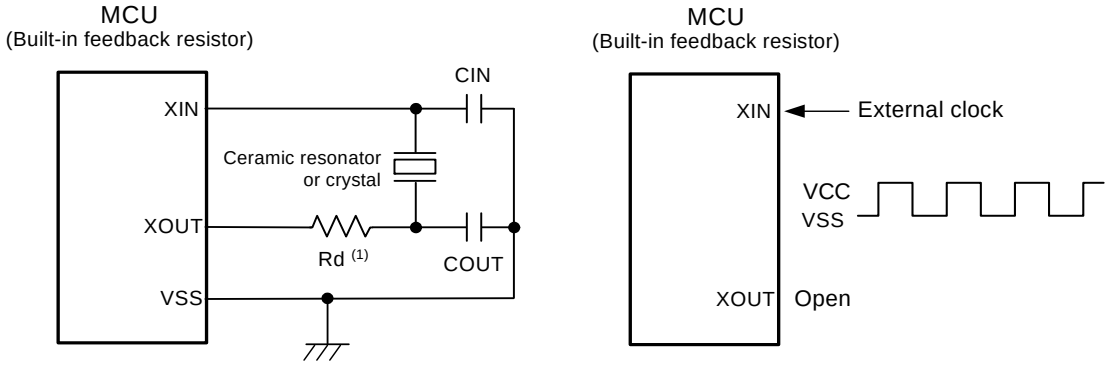
Clocks generated by the clock generators are described below.

8.3.1 Main Clock

This clock is supplied by the main clock oscillator and used as a clock source for the CPU and peripheral function clocks. After reset, the main clock is running, but is not used as a clock source for the CPU.

The main clock oscillator is configured by connecting a ceramic resonator or crystal between pins XIN and XOUT. The main clock oscillator contains a feedback resistor, which is disconnected from the oscillator in stop mode in order to reduce the amount of power consumed by the chip. The main clock oscillator may also be configured by feeding an externally generated clock to the XIN pin.

Figure 8.2 shows Main Clock Connection Example.



Note:
1. Insert a damping resistor if required. The resistance will vary depending on a crystal/ceramic resonator and the oscillation drive capacity setting. Use the value recommended by the manufacturer of crystal/ceramic resonator.
When the oscillation drive capacity is set to low, check if oscillation is stable in a low state. Also, place a feedback resistor between XIN and XOUT if the manufacturer recommends placing the resistor externally.

Figure 8.2 Main Clock Connection Example

The XOUT becomes high by setting the CM05 bit in the CM0 register to 1 (main clock oscillator turned off) after switching the clock source for the CPU clock to the sub clock (fC) or on-chip oscillator clock (fOCO-F, fOCO-S). In this case, the XIN is pulled high to the XOUT via the feedback resistor because the internal feedback resistor remains connected.

When the main clock oscillator is not used, setting the CM13 bit in the CM1 register to 1 enables to select the internal feedback resistor not connected.

Perform the following steps to start or stop the main clock. Refer to 8.2 “Registers” for details on register and bit access.

To start the main clock oscillation:

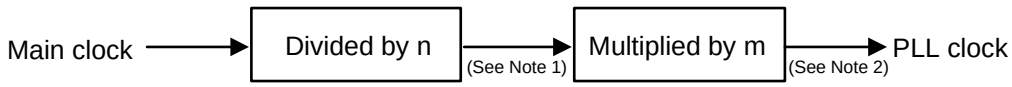
(1) Set the CM15 bit to 1 (drive capacity high) when a ceramic resonator or crystal is connected between pins XIN and XOUT.
(2) Set the CM05 bit to 0 (main clock oscillating).
(3) Wait until main clock oscillation stabilizes. (When using an external clock, input the external clock through the XIN pin.)

To stop the main clock oscillation,

(1) Set the CM20 bit in the CM2 register to 0 (oscillator stop/restart detect function disabled).
(2) Set the CM05 bit to 1 (stop).
(3) Stop the external clock (when inputting the external clock through the XIN pin).

8.3.2 PLL Clock

PLL clock is generated by the PLL frequency synthesizer. This clock is used as the clock source for the CPU and peripheral function clocks.
After reset, the PLL frequency synthesizer is stopped.
PLL clock is a clock which divides the main clock by the selected values of bits PLC05 to PLC04 in the PLC0 register, and then multiplied by the selected values of bits PLC02 to PLC00. Set bits PLC05 and PLC04 to fit divided frequency between 2 MHz and 5 MHz. Figure 8.3 shows Relation between Main Clock and PLL Clock.



n: 1, 2, 4 (selected by setting bits PLC05 and PLC04 in the PLC0 register)
m: 2, 4, 6, 8 (selected by setting bits PLC02 to PLC00 in the PLC0 register)

Notes:
1. Set the frequency divided by n to between 2 MHz and 5 MHz.
2. Set the PLL clock frequency to be within the f(PLL) range.

Figure 8.3 Relation between Main Clock and PLL Clock

Table 8.5 Example Settings for PLL Clock Frequencies

Main Clock	Setting Value		PLL Clock
	Bits PLC05 to PLC04	Bits PLC02 to PLC00	
10 MHz	01b (divide-by-2)	010b (multiply-by-4)	20 MHz
5 MHz	00b (not divided)	010b (multiply-by-4)	
12 MHz	10b (divide-by-4)	100b (multiply-by-8)	24 MHz
6 MHz	01b (divide-by-2)	100b (multiply-by-8)	
16 MHz	10b (divide-by-4)	100b (multiply-by-8)	32 MHz
8 MHz	01b (divide-by-2)	100b (multiply-by-8)	

8.3.3 fOCO40M

fOCO40M is a 40 MHz clock (approx.) supplied by the 40 MHz on-chip oscillator. It is the clock source for ϕAD in the A/D converter.

Follow the steps below to start or stop the 40 MHz on-chip oscillator clock. Refer to 8.2 “Registers” for details on register and bit access.

40 MHz on-chip oscillator start

(1) Set the FRA00 bit in the FRA0 register to 1 (40 MHz on-chip oscillator on).
(2) Wait for tsu(fOCO40M).

40 MHz on-chip oscillator stop

(1) Set the FRA01 bit in the FRA0 register to 0 (125 MHz on-chip oscillator) (when the CM27 bit is 1 (oscillator stop/restart detect interrupt)).
(2) Set the FRA00 bit in the FRA0 register to 0 (40 MHz on-chip oscillator off).

8.3.4 fOCO-F

fOCO-F is a 40 MHz clock (approx.) supplied by the 40 MHz on-chip oscillator, and divided by the selected values of bits FRA22 to FRA20 in the FRA2 register. It is the clock source for the CPU and peripheral function clocks.

After reset, fOCO-F is stopped.

If the main clock stops oscillating and the FRA01 bit is 1 when the CM20 bit in the CM2 register is 1 (oscillator stop/restart detect function enabled), and the CM27 bit is 1 (oscillator stop/restart detect interrupt), fOCO-F is used as the clock source for the CPU.

Refer to 8.3.3 “fOCO40M” to start or stop the 40 MHz on-chip oscillator clock.

8.3.5 125 kHz On-Chip Oscillator Clock (fOCO-S)

This clock is approximately 125 kHz, and is supplied by the 125 kHz on-chip oscillator. It is used as the clock source for the CPU and peripheral function clocks. In addition, when the CSPRO bit in the CSPR register is 1 (count source protection mode enabled), this clock is used as the count source for the watchdog timer (refer to 13.4.3 “Count Source Protection Mode Enabled”).

After reset, fOCO-S divided by 8 becomes the CPU clock.

If the main clock stops oscillating and the FRA01 bit is 0, when the CM20 bit in the CM2 register is 1 (oscillator stop/restart detect function enabled) and the CM27 bit is 1 (oscillator stop/restart detect interrupt), the 125 kHz on-chip oscillator automatically starts operating and supplying the necessary clock for the MCU.

Follow the steps below to start or stop fOCO-S. Refer to 8.2 “Registers” for details on register and bit access.

To start fOCO-S:

(1) Set the CM14 bit in the CM1 register to 0 (125 kHz on-chip oscillator on).
(2) Wait for tsu(fOCO-S).

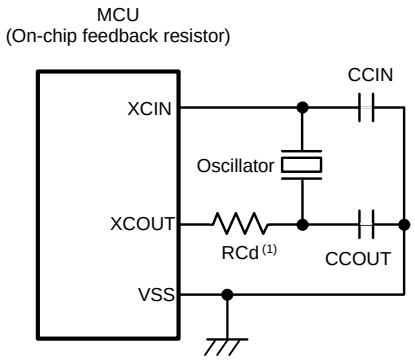
To start fOCO-S:

(1) Set the CM14 bit in the CM1 register to 1 (125 kHz on-chip oscillator off).

When the CM21 bit is 1 (on-chip oscillator used as the clock source for the CPU), the CM14 bit becomes 0 (125 kHz on-chip oscillator on).

8.3.6 Sub Clock (fC)

The sub clock is supplied by the sub clock oscillator. This clock is the clock source for count sources of the CPU clock, timer A, timer B, real-time clock.
The sub clock oscillator is configured by connecting a crystal between pins XCIN and XCOUT. The sub clock oscillator contains a feedback resistor, which is disconnected from the oscillation circuit in stop mode in order to reduce the amount of power consumed by the chip.
Figure 8.4 shows Sub Clock Connection Example.



Note:
1. Insert a damping resistor if required. Resistance values vary depending on a crystal/ceramic resonator and the drive level. Use the resistance values recommended by the manufacturer of crystal/ceramic resonator.
When setting the oscillation drive level to low, check if the oscillation stabilizes. If the manufacturer recommends to place a feedback resistor on the chip externally, insert a feedback resistor between the XCIN and XCOUT pins following the instructions.

Figure 8.4 Sub Clock Connection Example

After reset, the sub clock is stopped. At this time, the feedback resistor is disconnected from the oscillator.
Follow the steps below to start the sub clock. Refer to 8.2 “Registers” for details on register and bit access.

(1) Set the PU21 bit in the PUR2 register to 0 (P8_4, P8_6 and P8_7 not pulled high).
(2) Set bits PD8_6 and PD8_7 in the PD8 register to 0 (P8_6, P8_7 function as input ports).
(3) Set the CM04 bit to 1 (XCIN-XCOUT oscillation function). Set the CM03 bit to 1 (XCIN-XCOUT drive capacity high).
(4) Wait until sub clock oscillation stabilizes.

8.4 CPU Clock and Peripheral Function Clocks

The CPU is run by the CPU clock, and the peripheral functions are run by the peripheral function clocks.

8.4.1 CPU Clock and BCLK

The CPU clock is an operating clock for the CPU and watchdog timer.
The main clock, PLL clock, fOCO-F, fOCO-S, or fC can be selected as the clock source for the CPU clock. (See Table 9.2 “Clocks in Normal Operating Mode”.)
When the main clock, PLL clock, fOCO-F or fOCO-S is selected as the clock source for the CPU clock, the selected clock divided by 1, 2, 4, 8 or 16 becomes the CPU clock. Use the CM06 bit in the CM0 register and bits CM17 to CM16 in the CM1 register to select a frequency-divided value.
When fC is selected as the clock source for the CPU clock, it is not divided and is used directly as the CPU clock.
After reset, fOCO-S divided by 8 becomes the CPU clock. Note that when entering stop mode or when the CM21 bit in the CM2 register is 0 (main clock or PLL clock) and the CM05 bit is 1 (main clock off), the CM06 bit in the CM0 register becomes 1 (divide-by-8 mode).
BCLK is a bus reference clock.

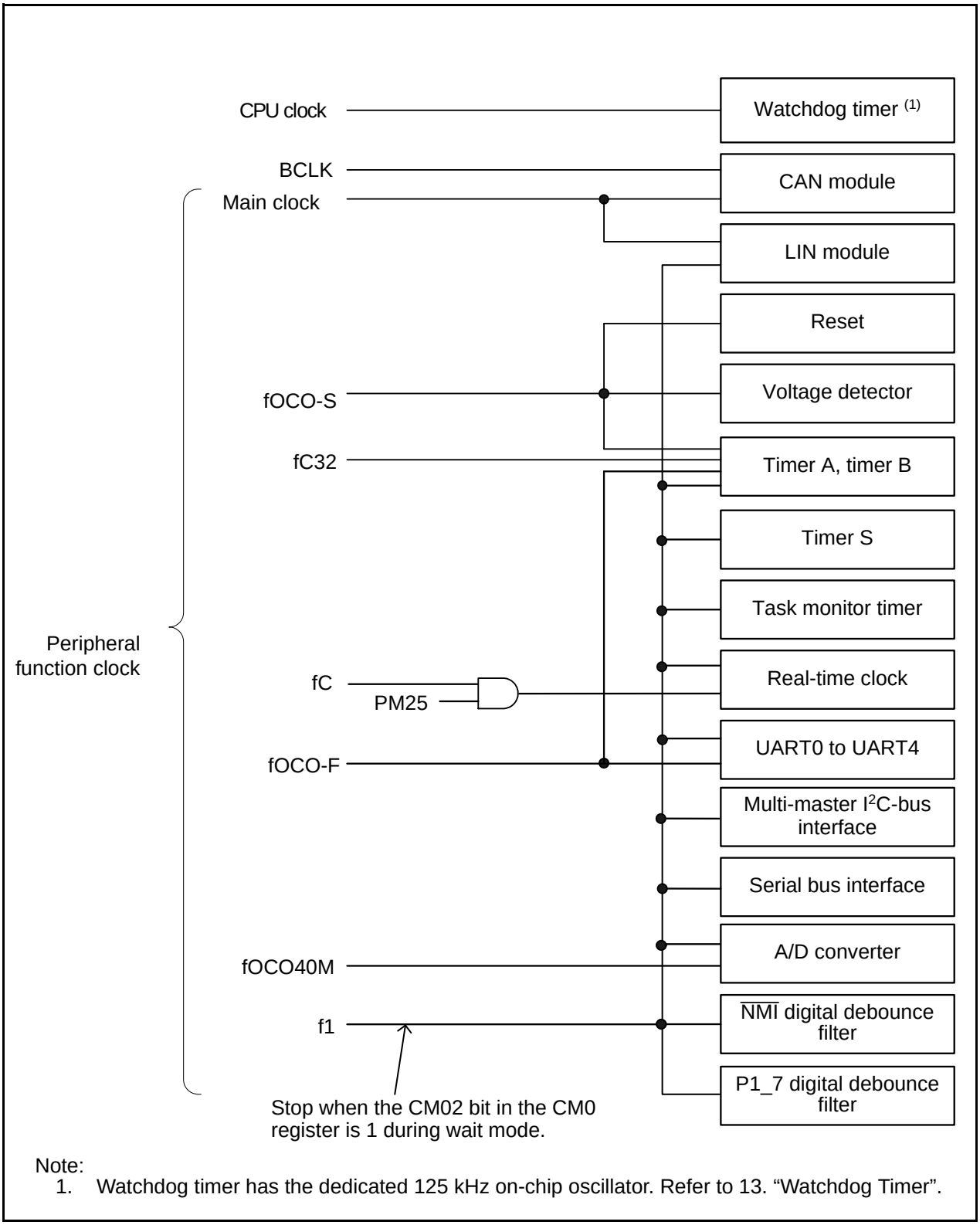
8.4.2 Peripheral Function Clocks (f1, fOCO40M, fOCO-F, fOCO-S, fC32, fC, Main Clock)

f1, fOCO40M, fOCO-F, fOCO-S, and fC32 are operating clocks for the peripheral functions.
f1 is one of the following:

- Main clock divided by 1 (no division)
- PLL clock divided by 1 (no division)
- fOCO-S divided by 1 (no division)
- fOCO-F divided by 1 (no division)

f1 is used for timers A, B, and S, the task monitor timer, real-time clock, UART0 to UART4, multi-master I^2C-bus interface, serial bus interface, the LIN module and the A/D converter. It also can be used as a sampling clock for $\overline{NMI}$, P1_7 digital debounce filter.
When the WAIT instruction is executed after setting the CM02 bit in the CM0 register to 1 (peripheral function clock f1 turned off during wait mode), the f1 clock is stopped.
fOCO40M can be used for the A/D converter. fOCO40M can be used when the FRA00 bit in the FRA0 register is 1 (40 MHz on-chip oscillator on).
fOCO-F can be used for timers A and B, and UART0 to UART4.
fOCO-F can be used when the FRA00 bit in the FRA0 register is 1 (40 MHz on-chip oscillator on).
fOCO-S is used for timers A and B. It is also used for reset, voltage detector. fOCO-S is also used when the CM14 bit in the CM1 register is set to 0 (125 kHz on-chip oscillator on).
fC divided by 32 becomes fC32. fC32 is used for timers A and B, and can be used when the sub clock is on.
fC is used as the count source for the real-time clock when the PM25 bit in the PM2 register is 1 (peripheral clock fC provided). fC can be used when the sub clock is on.
The main clock can be used for the LIN module and CAN module.

Figure 8.5 shows Peripheral Function Clocks.



Note:
1. Watchdog timer has the dedicated 125 kHz on-chip oscillator. Refer to 13. “Watchdog Timer”.

Figure 8.5 Peripheral Function Clocks

8.5 Clock Output Function

The f1, f8, f32 or fC clock can be output from the CLKOUT pin. Use bits CM01 to CM00 in the CM0 register, and the PCLK5 bit in the PCLKR register to select a clock. f8 has the same frequency as f1 divided by 8, and f32 has the same frequency as f1 divided by 32.
Set the frequency of the clock output from the CLKOUT pin to 25 MHz or below.

8.6 System Clock Protection Function

The system clock protection function prohibits the CPU clock from changing clock sources when the main clock is selected as the CPU clock source. This is to prevent the CPU clock from stopping due to an unexpected program operation.
When the PM21 bit in the PM2 register is set to 1 (clock change disabled), the following bits remain unchanged even if they are written to:

- The CM02 bit in the CM0 register (peripheral function clock f1 in wait mode)
- The CM05 bit in the CM0 register (to prevent the main clock from being stopped)
- The CM07 bit in the CM0 register (clock source of the CPU clock)
- The CM10 bit in the CM1 register (MCU does not enter stop mode)
- The CM11 bit in the CM1 register (clock source of the CPU clock)
- The CM20 bit in the CM2 register (oscillator stop/restart detect function set)
- All bits in the PLC0 register (PLL frequency synthesizer set)

To use the system clock protect function, set the CM05 bit in the CM0 register to 0 (main clock oscillation) and CM07 bit to 0 (main clock as CPU clock source), and then follow the steps below.

(1) Set the PRC1 bit in the PRCR register to 1 (write to PM2 register enabled).
(2) Set the PM21 bit in the PM2 register to 1 (clock change disabled).
(3) Set the PRC1 bit in the PRCR register to 0 (write to PM2 register disabled).

When the PM21 bit is 1, do not execute the WAIT instruction.

8.7 Oscillator Stop/Restart Detect Function

This function detects a stop/restart of the main clock oscillator. The oscillator stop/restart detect function can be enabled and disabled with the CM20 bit in the CM2 register.
A reset or oscillator stop/restart detect interrupt is generated when an oscillator stop or restart is detected. Set the CM27 bit in the CM2 register to select the reset or interrupt.
Table 8.6 lists Oscillator Stop/Restart Detect Function Specifications.

Table 8.6 Oscillator Stop/Restart Detect Function Specifications

Item	Specification
Oscillator stop detectable clock and frequency bandwidth	f(XIN) ≥ 2 MHz
Enabling condition for the oscillator stop/restart detect function	Set the CM20 bit to 1 (enabled)
Operation when oscillator stop/restart detected	When CM27 bit is 0: Oscillator stop detect reset generated When CM27 bit is 1: Oscillator stop/restart detect interrupt generated

8.7.1 Operation When CM27 Bit is 0 (Oscillator Stop Detect Reset)

When main clock stop is detected while the CM20 bit is 1 (oscillator stop/restart detect function enabled), the MCU is initialized, and then stops (oscillator stop reset). Refer to 4. “Special Function Registers (SFRs)” and 6. “Resets”.
The status can be cancelled by a hardware reset or a voltage monitor 0 reset. The MCU can also be initialized and stopped when a restart is detected, but do not use the MCU in this manner. During main clock stop, do not set the CM20 bit to 1 and the CM27 bit to 0.

8.7.2 Operation When CM27 Bit is 1 (Oscillator Stop/Restart Detect Interrupt)

When the CM20 bit is 1 (oscillator stop/restart detect function enabled), the system is placed in the state shown in Table 8.7 if the main clock detects oscillator stop or restart.

The CM21 bit becomes 1 in high-speed, medium-speed, or low-speed mode. The FRA01 bit does not change. Thus, high-speed and medium-speed mode become 125 kHz on-chip oscillator mode or 40 MHz on-chip oscillator mode. Because the CM07 bit does not change, low-speed mode remains in low-speed mode, but fOCO-S or fOCO-F becomes the clock source for the peripheral functions.

When the CM21 bit is set to 1, the CM14 bit becomes 0 (125 kHz on-chip oscillator on), but the FRA00 bit does not change (40 MHz on-chip oscillator does not oscillate automatically). Thus, when the FRA01 bit is 1 (40 MHz on-chip oscillator selected), set the FRA00 bit to 1 (40 MHz on-chip oscillator on). Do not set the FRA00 bit to 0 while the FRA01 bit is 1, and vice versa.

Since the CM21 bit does not change in PLL operating mode, change the mode to 125 kHz on-chip oscillator mode or 40 MHz on-chip oscillator mode in the interrupt routine.

Table 8.7 State after Oscillator Stop/Restart Detect When CM27 Bit is 1

Condition		After Detection
Main clock oscillator stop detected	High-speed mode Medium-speed mode	• Oscillator stop/restart detect interrupt is generated • CM14 bit is 0 (125 kHz on-chip oscillator on) • CM21 bit is 1 (fOCO-S or fOCO-F is used as the clock source for the CPU and peripheral function clocks) (1, 2) • CM22 bit is 1 (main clock stop detected) • CM23 bit is 1 (main clock stopped)
	Low-speed mode	
	40 MHz on-chip oscillator mode	
	125 kHz on-chip oscillator mode	
	PLL operating mode	• Oscillator stop/restart detect interrupt is generated • CM14 bit is 0 (125 kHz on-chip oscillator on) • CM21 bit remains unchanged • CM22 bit is 1 (main clock stop detected) • CM23 bit is 1 (main clock stopped)
Main clock oscillator restart detected	-	• Oscillator stop/restart detect interrupt is generated • CM14 bit is 0 (125 kHz on-chip oscillator on) • CM21 bit does not change • CM22 bit is 1 (main clock stop detected) • CM23 bit is 0 (main clock oscillating)

CM14 bit: Bit in the CM1 register

Bits CM21, CM22, CM23: Bits in the CM2 register

Notes:

1. fOCO-S or fOCO-F is selected depending on the FRA01 bit setting.
2. fC is used as the CPU clock in low-speed mode.

8.7.3 Using the Oscillator Stop/Restart Detect Function

After oscillator stop is detected, if the main clock reoscillates, set the main clock back to the clock source for the CPU clock and peripheral functions by a program. Figure 8.6 shows the Switching from On-Chip Oscillator Clock to Main Clock.

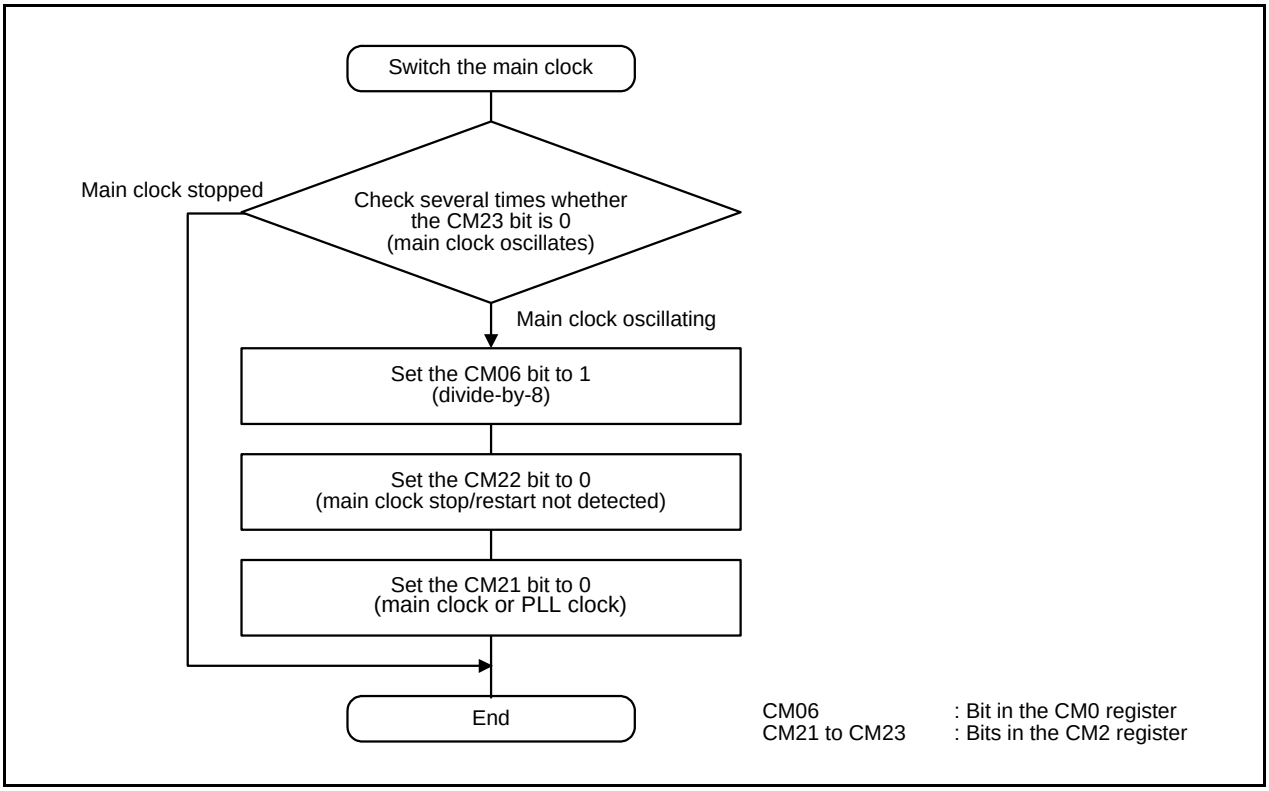


Figure 8.6 Switching from On-Chip Oscillator Clock to Main Clock

The CM22 bit becomes 1 at the same time an oscillator stop/restart detect interrupt is generated. When the CM22 bit is 1, the oscillator stop/restart detect interrupt is disabled. When setting the CM22 bit to 0 by a program, the oscillator stop/restart detect interrupt is enabled.

8.8 Interrupt

The oscillator stop/restart detect interrupt is a non-maskable interrupt.

The watchdog timer interrupt, oscillator stop/restart detect interrupt, and voltage monitor 2 interrupt share the same vector. When using multiple interrupts together, read the detect flags of the events in the interrupt processing program, and determine the source of the interrupt.

The detect flag for oscillator stop/restart detect is the CM22 bit in the CM2 register. After the interrupt source is determined, set the CM22 bit to 0 (not detected).

8.9 Notes on Clock Generator

8.9.1 Oscillator Using a Crystal or a Ceramic Resonator

To connect a crystal/ceramic resonator follow the instructions below:

- The oscillation characteristics are tied closely to the user's board design. Perform a careful evaluation of the board before connecting an oscillator.
- Oscillator structure depends on a crystal/ceramic resonator. The M16C/5M Group, M16C/57 Group MCUs contain a feedback resistor, but an additional external feedback resistor may be required. Contact the manufacturer of crystal/ceramic resonator regarding circuit constants, as they are dependent on the a crystal/ceramic resonator or stray capacitance of the mounted circuit.
- Check output from the CLKOUT pin to confirm that the clock generated by the oscillator is properly transmitted to the MCU.

The procedure for outputting a clock from the CLKOUT pin is listed below. Set the clock output from the CLKOUT pin to 25 MHz or lower.

Outputting the main clock

(1) Set the PRC0 bit in the PRCR register to 1 (write enabled).
(2) Set the CM11 bit in the CM1 register, the CM07 bit in the CM0 register, and the CM21 bit in the CM2 register all to 0 (main clock selected).
(3) Select the clock output from the CLKOUT pin (see the table below).
(4) Set the PRC0 bit in the PRCR register to 0 (write disabled).

Table 8.8 Output from CLKOUT Pin When Selecting Main Clock

Bit Setting		Output from the CLKOUT Pin
PCLKR register	CM0 register	
PCLK5 bit	Bits CM01 to CM00	
1	00b	Clock with the same frequency as the main clock
0	10b	Main clock divided by 8
0	11b	Main clock divided by 32

Outputting the sub clock

(1) Set the PRC0 bit in the PRCR register to 1 (write enabled).
(2) Set the CM07 bit in the CM0 register to 1 (sub clock selected).
(3) Set the PCLK5 bit in the PCLKR register to 0, and bits CM01 to CM00 in the CM0 register to 01b (fC output from CLKOUT pin).
(4) Set the PRC0 bit in the PRCR register to 0 (write disabled).

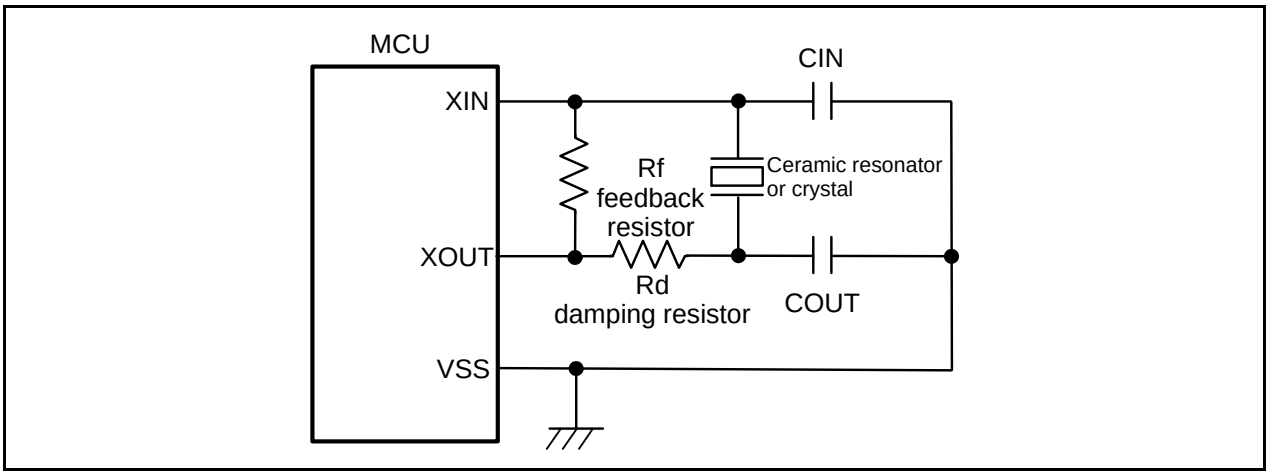


Figure 8.7 Oscillator Example

8.9.2 Noise Countermeasure

8.9.2.1 Clock I/O Pin Wiring

- Connect the shortest possible wiring to the clock I/O pin.
- Connect (a) the capacitor's ground lead connected to the crystal/ceramic resonator, and (b) the MCU's VSS pin, with the shortest possible wiring (maximum 20 mm).

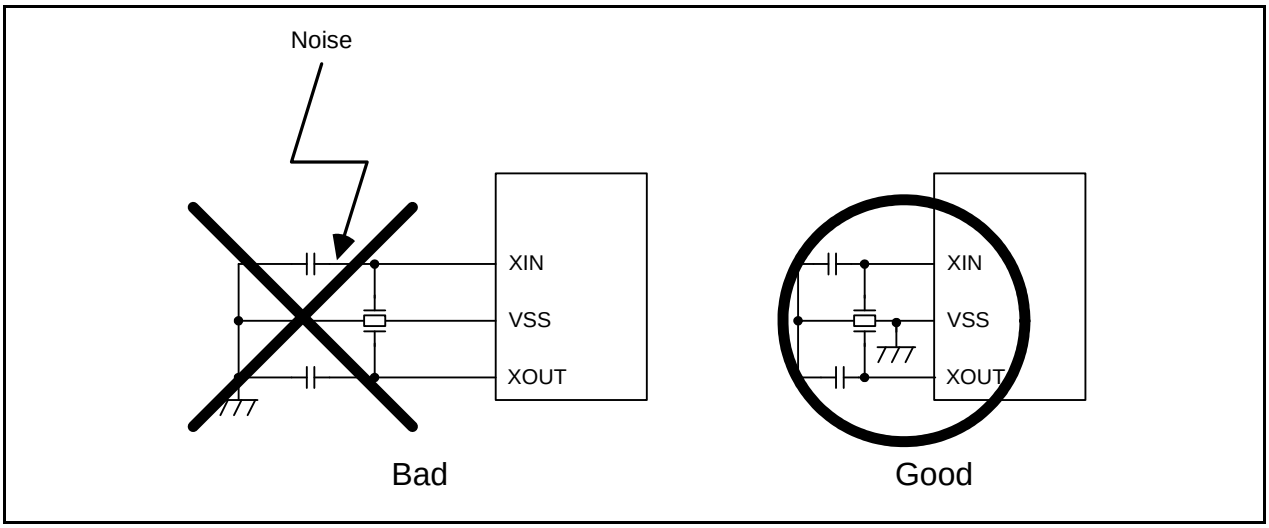


Figure 8.8 Clock I/O Pin Wiring

Reason:
When noise enters the clock I/O pin, the clock waveform becomes unstable, which causes an error in operation or a program runaway. Also, if a potential difference attributed to the noise occurs between the VSS level of the MCU and the VSS level of the crystal/ceramic resonator, an accurate clock is not input to the MCU.

8.9.2.2 Large Current Signal Line

For large currents that exceed the MCU's current range, wire the signal lines as far away from the MCU as possible (especially the crystal/ceramic resonator).

Reason:
In the system using the MCU, there are signal lines for controlling motors, LEDs, and thermal heads. When a large current flows through these signal lines, noise is generated due to mutual inductance.

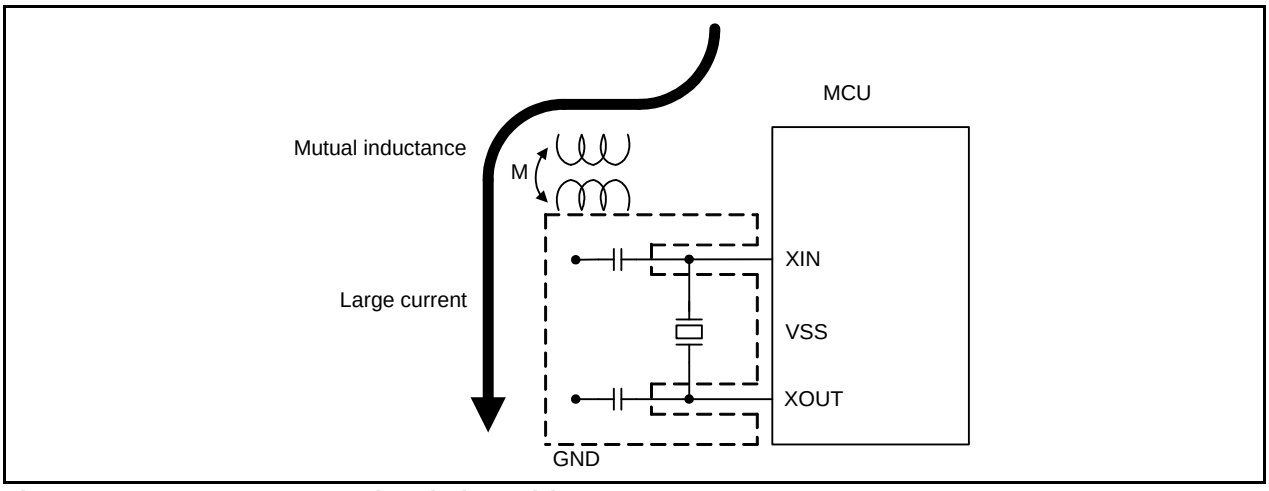


Figure 8.9 Large Current Signal Line Wiring

8.9.2.3 Signal Line Whose Level Changes at a High-Speed

For a signal line whose level changes at a high-speed, wire it as far away from the crystal/ceramic resonator and its wiring pattern as possible. Do not wire it across or extend it parallel to a clock-related signal line or other signal lines which are sensitive to noise.

Reason:
A signal whose level changes at a high-speed (such as the signal from the TAiOUT pin) affects other signal lines due to the level change at rising or falling edges. Specifically, when the signal line crosses the clock-related signal line, the clock waveform becomes unstable, which causes an error in operation or a program runaway.

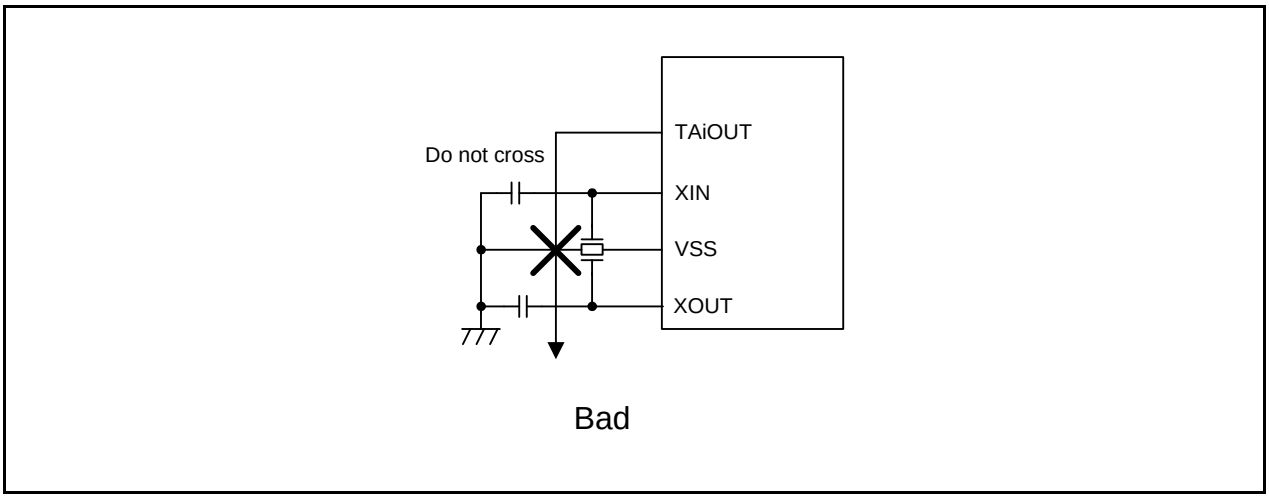


Figure 8.10 Wiring of Signal Line Whose Level Changes at High-Speed

8.9.3 CPU Clock

(Technical update number: TN-M16C-109-0309)
When an external clock is input from the XIN pin and the main clock is used as the CPU clock, do not stop the external clock.

8.9.4 Oscillator Stop/Restart Detect Function

- In the following cases, set the CM20 bit to 0 (oscillator stop/restart detect function disabled), and then change the setting of each bit.
  - When the CM05 bit is set to 1 (main clock stopped)
  - When the CM10 bit is set to 1 (stop mode)
- To enter wait mode while using the oscillator stop/restart detect function, set the CM02 bit to 0 (peripheral function clock f1 not turned off during wait mode).
- This function cannot be used if the main clock frequency is 2 MHz or lower. In that case, set the CM20 bit to 0 (oscillator stop/restart detect function disabled).
- While the CM27 bit is 1 (oscillation stop/restart detect interrupt), when the FRA01 bit is 1 (40 MHz on-chip oscillator selected), set the FRA00 bit to 1 (40 MHz on-chip oscillator on). (Do not set the FRA00 bit to 0 while FRA01 bit is 1, and vice versa.)

8.9.5 PLL Frequency Synthesizer

To use the PLL frequency synthesizer, stabilize the supply voltage within the acceptable range of power supply ripple.

Table 8.9 Acceptable Range of Power Supply Ripple

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$f_{(ripple)}$	Power supply ripple allowable frequency (VCC)				10	kHz
$V_{P-P(ripple)}$	Power supply ripple allowable amplitude voltage	(VCC = 5 V)			0.5	V
		(VCC = 3 V)			0.3	V
$V_{CC(\lvert\Delta V/\Delta T\rvert)}$	Power supply ripple rising/falling gradient	(VCC = 5 V)			0.3	V/ms
		(VCC = 3 V)			0.3	V/ms

f(ripple)
Power supply ripple allowable frequency (VCC)

Vp-p(ripple)
Power supply ripple allowable amplitude voltage

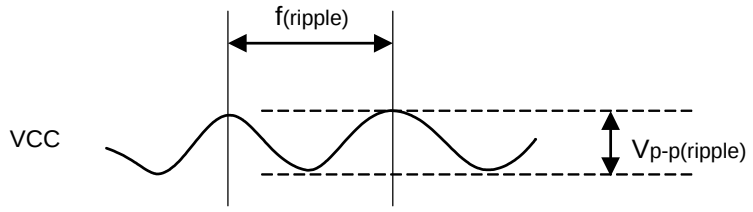


Figure 8.11 Voltage Fluctuation Timing

9. Power Control

9.1 Introduction

This chapter describes how to reduce the amount of current consumption.

9.2 Registers

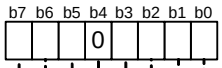
Refer to 8. “Clock Generator” for clock-related registers.

Table 9.1 Registers

Address	Register	Symbol	Reset Value
0220h	Flash Memory Control Register 0	FMR0	0000 0001b (Other than user boot mode) 0010 0001b (User boot mode)
0222h	Flash Memory Control Register 2	FMR2	XXXX 0000b

9.2.1 Flash Memory Control Register 0 (FMR0)

Flash Memory Control Register 0



Symbol: FMR0 | Address: 0220h | Reset Value: 0000 0001b (other than user boot mode), 0010 0001b (user boot mode)

Bit Symbol	Bit Name	Function	RW
FMR00	RY/$\overline{BY}$ status flag	0 : Busy (being written or erased) 1 : Ready	RO
FMR01	CPU rewrite mode select bit	0 : CPU rewrite mode disabled 1 : CPU rewrite mode enabled	RW
FMR02	Lock bit disable select bit	0 : Lock bit enabled 1 : Lock bit disabled	RW
FMSTP	Flash memory stop bit	0 : Flash memory operation enabled 1 : Flash memory operation stopped (low power-mode, flash memory initialized)	RW
— (b4)	Reserved bit	Set to 0	RW
— (b5)	Reserved bit	Set to 0 in other than user boot mode Set to 1 in user boot mode	RW
FMR06	Program status flag	0 : Completed as expected 1 : Completed in error	RO
FMR07	Erase status flag	0 : Completed as expected 1 : Completed in error	RO

FMR01 (CPU rewrite mode select bit) (b1)

Commands can be accepted by setting the FMR01 bit to 1 (CPU rewrite mode enabled).
To set the FMR01 bit to 1, write 0 and then 1 in succession. Do not generate any interrupts or DMA transfers between setting 0 and 1.
Change the FMR01 bit when the PM24 bit in the PM2 register is 0 ($\overline{NMI}$ interrupt disabled) or high is input to the $\overline{NMI}$ pin.
While in EW0 mode, write to this bit from a program in RAM.
Enter read array mode, and then set this bit to 0.

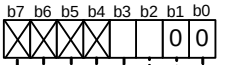
FMSTP (Flash memory stop bit) (b3)

The FMSTP bit resets the flash memory control circuits and minimizes current consumption in the flash memory. Access to the internal flash memory is disabled when the FMSTP bit is set to 1 (flash memory operation stopped). Set the FMSTP bit by a program located in RAM.
Set the FMSTP bit to 1 under the following condition:

- A flash memory access error occurs while erasing or programming in EW0 mode (the FMR00 bit does not revert to 1 (ready)).

9.2.2 Flash Memory Control Register 2 (FMR2)

Flash Memory Control Register 2



Symbol: FMR2 | Address: 0222h | Reset Value: XXXX 0000b

Bit Symbol	Bit Name	Function	RW
— (b1-b0)	Reserved bits	Set to 0	RW
FMR22	Slow read mode enable bit	0 : Disabled 1 : Enabled	RW
FMR23	Low current consumption read mode enable bit	0 : Disabled 1 : Enabled	RW
— (b7-b4)	No register bits. If necessary, set to 0. The read value is undefined.		—

FMR22 (Slow read mode enable bit) (b2)

This bit enables the mode which reduces the amount of current consumption when reading the flash memory. When rewriting the flash memory (CPU rewrite mode), set the FMR22 bit to 0 (slow read mode disabled).

To set the FMR22 bit to 1, write 0 and then 1 in succession. Make sure no interrupts or DMA transfers occur between writing 0 and 1.

Set the FMR23 bit to 1 (low current consumption read mode enabled) after the FMR22 bit is set to 1 (slow read mode enabled). Also, set the FMR22 bit to 0 (slow read mode disabled) after the FMR23 bit is set to 0 (low current consumption read mode disabled). Do not change the FMR22 bit and FMR23 bit at the same time.

FMR23 (Low current consumption read mode enable bit) (b3)

This bit enables the mode which reduces the amount of current consumption when reading the flash memory. When rewriting the flash memory (CPU rewrite mode), set the FMR23 bit to 0 (low current consumption read mode disabled).

Low current consumption read mode can be used when the CM07 bit in the CM0 register is 1 (sub clock used as CPU clock).

To set the FMR23 bit to 1, write 0 and then 1 in succession. Make sure no interrupts or DMA transfers occur between writing 0 and 1.

Set the FMR23 bit to 1 (low current consumption read mode enabled) after the FMR22 bit is set to 1 (slow read mode enabled). Also, set the FMR22 bit to 0 (slow read mode disabled) after the FMR23 bit is set to 0 (low current consumption read mode disabled). Do not change bits FMR22 and FMR23 at the same time.

Do not set the FMR23 bit to 1 (low current consumption read mode enabled) when any of the following occurs:

- When the CM07 bit is 0 (main clock, PLL clock, or on-chip oscillator clock selected as CPU clock source).
- When the FMR22 bit is 0 (slow read mode disabled)
- When the FMSTP bit is 1 (flash memory stopped)
- During the wake up operation when the FMSTP bit is changed from 1 to 0 (tps)

Do not perform the operations below when the FMR23 bit is 1. Set the FMR23 to 0 before performing them.

- Change the CPU clock
- Set to the FMSTP bit to 1 (flash memory stopped)
- Enter the wait mode or stop mode
- Execute the following commands:
  Program, block erase, lock bit program, read lock bit status, and block blank check

9.3 Clock

The amount of current consumption correlates with the number of operating clocks and frequency. When there are fewer operating clocks and a lower frequency, current consumption will be low.
Normal operating mode, wait mode, and stop mode can be used to control power consumption. All mode states, except wait mode and stop mode, are referred to as normal operating mode in this document.

9.3.1 Normal Operating Mode

In normal operating mode, because both the CPU clock and the peripheral function clocks are supplied, the CPU and the peripheral functions are operating. Power control is exercised by controlling the CPU clock frequency. The higher the CPU clock frequency, the higher the processing capability. The lower the CPU clock frequency, the lower the power consumption in the chip. If unnecessary oscillator are stopped, power consumption is further reduced.

9.3.1.1 High-Speed Mode and Medium-Speed Mode

In high-speed mode, the main clock divided by 1 (no division) is used as the CPU clock.
In medium-speed mode, the main clock divided by 2, 4, 8 or 16 is used as the CPU clock.
f1 with the same frequency of the main clock divided by 1 is used as the peripheral function clocks in both high-speed and medium-speed modes. When fC is supplied, fC and fC32 can be used as the peripheral function clocks. When fOCO-S is supplied, it can be used as the peripheral function clocks. When fOCO40M and fOCO-F are supplied, they can be used as the peripheral function clocks.

9.3.1.2 PLL Operating Mode

The PLL clock divided by 1 (no division), 2, 4, 8 or 16 is used as the CPU clock. f1 with the same frequency of the PLL clock divided by 1 (no division) is used as the peripheral function clocks.
When fC is supplied, fC and fC32 can be used as the peripheral function clocks. When fOCO-S is supplied, it can be used as the peripheral function clocks. When fOCO40M and fOCO-F are supplied, they can be used as the peripheral function clocks.
PLL operating mode can be entered and exited from high-speed mode or medium-speed mode. To enter other modes including wait mode and stop mode, enter high-speed mode or medium-speed mode first, and then enter the intended mode. Refer to Figure 9.1 “Clock Mode Transition” for details.

9.3.1.3 40 MHz On-Chip Oscillator Mode

The fOCO-F clock divided by 1 (no division), 2, 4, 8 or 16 is used as the CPU clock. f1 with the same frequency of the fOCO-F clock divided by 1 is used as the peripheral function clocks.
When fC is supplied, fC and fC32 can be used as the peripheral function clocks. When fOCO-S is supplied, it can be used as the peripheral function clocks. fOCO40M and fOCO-F can be used as the peripheral function clocks.

9.3.1.4 125 kHz On-Chip Oscillator Mode

The fOCO-S clock divided by 1 (no division), 2, 4, 8 or 16 is used as the CPU clock. f1 with the same frequency of the fOCO-S clock divided by 1 is used as the peripheral function clocks.
When fC is supplied, fC and fC32 can be used as the peripheral function clocks. fOCO-S can be used as the peripheral function clocks. When fOCO40M and fOCO-F are supplied, they can be used as the peripheral function clocks.

9.3.1.5 125 kHz On-Chip Oscillator Low Power Mode

The main clock and fOCO-F are turned off after the MCU enters 125 kHz on-chip oscillator mode. The fOCO-S clock divided by 1 (no division), 2, 4, 8 or 16 is used as the CPU clock. f1 with the same frequency of the fOCO-S clock divided by 1 is used as the peripheral function clocks.
When fC is supplied, fC and fC32 can be used as the peripheral function clocks. fOCO-S can be used as the peripheral function clocks.

9.3.1.6 Low-Speed Mode

fC is used as the CPU clock.
When the CM21 bit is 0 and the CM11 bit is 0 (main clock), f1 with the same frequency of the main clock divided by 1 is used as the peripheral function clocks. When the CM21 bit is 0 and the CM11 bit is 1 (PLL clock), f1 with the same frequency of the PLL clock divided by 1 is used as the peripheral function clocks.When the CM21 bit is 1 (on-chip oscillator clock) and the FRA01 bit is 0 (125 kHz on-chip oscillator), f1 with the same frequency as the fOCO-S clock divided by 1 is used as the peripheral function clocks. When the CM21 bit is 1 (on-chip oscillator clock) and the FRA01 bit is 1 (40 MHz on-chip oscillator), f1 with the same frequency as the fOCO-F clock divided by 1 is used as the peripheral function clocks.
fC and fC32 can be used as the peripheral function clocks. When fOCO-S is supplied, it can be used as the peripheral function clocks. When fOCO40M and fOCO-F are supplied, they can be used as the peripheral function clocks.

9.3.1.7 Low Power Mode

The main clock and fOCO-F are stopped after the MCU enters low-speed mode. fC is used as the CPU clock. When the CM21 bit is 1 (on-chip oscillator clock) and the FRA01 bit is 0 (125 kHz on-chip oscillator clock), f1 with the same frequency as the fOCO-S clock divided by 1 is used as the peripheral function clocks.
fC and fC32 can be used as the peripheral function clocks. When fOCO-S is supplied, it can be used as the peripheral function clocks.

Table 9.2 Clocks in Normal Operating Mode

Mode	CPU Clock	Peripheral Clocks (2)			
		f1	fC, fC32	fOCO-S	fOCO-F fOCO40M
High-speed mode	Main clock divided by 1 (1)	Main clock divided by 1	Enabled	Enabled	Enabled
Medium-speed mode	Main clock divided by n (1)				
PLL operating mode	PLL clock divided by n (1)	PLL clock divided by 1			
40 MHz on-chip oscillator mode	fOCO-F divided by n (1)	fOCO-F divided by 1	Enabled	Enabled	Enabled
125 kHz on-chip oscillator mode	fOCO-S divided by n (1)	fOCO-S divided by 1	Enabled	Enabled	Enabled
125 kHz on-chip oscillator low power mode	fOCO-S divided by n (1)	fOCO-S divided by 1	Enabled	Enabled	Disabled
Low-speed mode	fC	Any of the following: Main clock divided by 1 (when the CM21 is 0 and the CM11 is 0) PLL clock divided by 1 (when the CM21 is 0 and the CM11 is 1) fOCO-F divided by 1 (when the CM21 is 1 and the FRA01 is 1) fOCO-S divided by 1 (when the CM21 is 1 and the FRA01 is 0)	Enabled	Enabled	Enabled
Low power mode	fC	fOCO-S divided by 1 (when the CM21 is 1 and the FRA01 is 0)	Enabled	Enabled	Disabled

CM11 : Bit in the CM1 register
CM21 : Bit in the CM2 register
FRA01 : Bit in the FRA0 register

Notes:
1. Select by setting the CM06 bit in the CM0 register and bits CM17 to CM16 in the CM1 register.
2. The peripheral clock is enabled when each clock is supplied. Refer to 8. “Clock Generator” for the clock supply method.

Table 9.3 Clock-Related Bit Setting and Modes

Mode	CM2 Register	CM1 Register		CM0 Register			FRA0 Register	
	CM21	CM14	CM11	CM07	CM05	CM04	FRA01	FRA00
High-speed mode, medium-speed mode	0	–	0	0	0	–	–	–
PLL operating mode	0	–	1	0	0	–	–	–
40 MHz on-chip oscillator mode	1	–	0	0	–	–	1	1
125 kHz on-chip oscillator mode	1	0	0	0	0 (1)	–	0	1 (1)
125 kHz on-chip oscillator low power mode	1	0	0	0	1	–	0	0
Low-speed mode	–	–	0	1	0 (1)	1	–	1 (1)
Low power mode	–	–	0	1	1	1	–	0

–: 0 or 1

Note:
1. Both or either the main clock and fOCO-F are oscillated.

Table 9.4 Selecting Clock Division Related Bits (1)

Division	CM1 Register	CM0 Register
	Bits CM17 to CM16	CM06 bit
No division (2)	00b	0
Divide-by-2	01b	0
Divide-by-4	10b	0
Divide-by-8	–	1
Divide-by-16	11b	0

–: Any value from 00b to 11b

Notes:
1. While in high-speed mode, medium-speed mode, PLL operating mode, 125 kHz on-chip oscillator mode, or 125 kHz on-chip oscillator low power mode.
2. Select divide-by-1 (no division) in high-speed mode.

Table 9.5 Example Settings for 40 MHz On-Chip Oscillator Mode Division Related Bits

Division	CPU Clock Frequency	FRA2 Register	CM1 Register	CM0 Register
		Bits FRA22 to FRA20	Bits CM17 to CM16	CM06 bit
Divide-by-2	Approx. 20 MHz	000b (divide-by-2)	00b (no division)	0
Divide-by-4	Approx. 10 MHz	000b (divide-by-2)	01b (divide-by-2)	0
Divide-by-8	Approx. 5 MHz	000b (divide-by-2)	10b (divide-by-4)	0
Divide-by-16	Approx. 2.5 MHz	000b (divide-by-2)	–	1 (divide-by-8)
Divide-by-32	Approx. 1.25 MHz	000b (divide-by-2)	11b (divide-by-16)	0
Divide-by-64	Approx. 625 kHz	010b (divide-by-4)	11b (divide-by-16)	0
Divide-by-128	Approx. 312.5 kHz	110b (divide-by-8)	11b (divide-by-16)	0

–: Any value from 00b to 11b

9.3.2 Clock Mode Transition Procedure

Figure 9.1 shows Clock Mode Transition. Arrows indicate possible mode transitions.

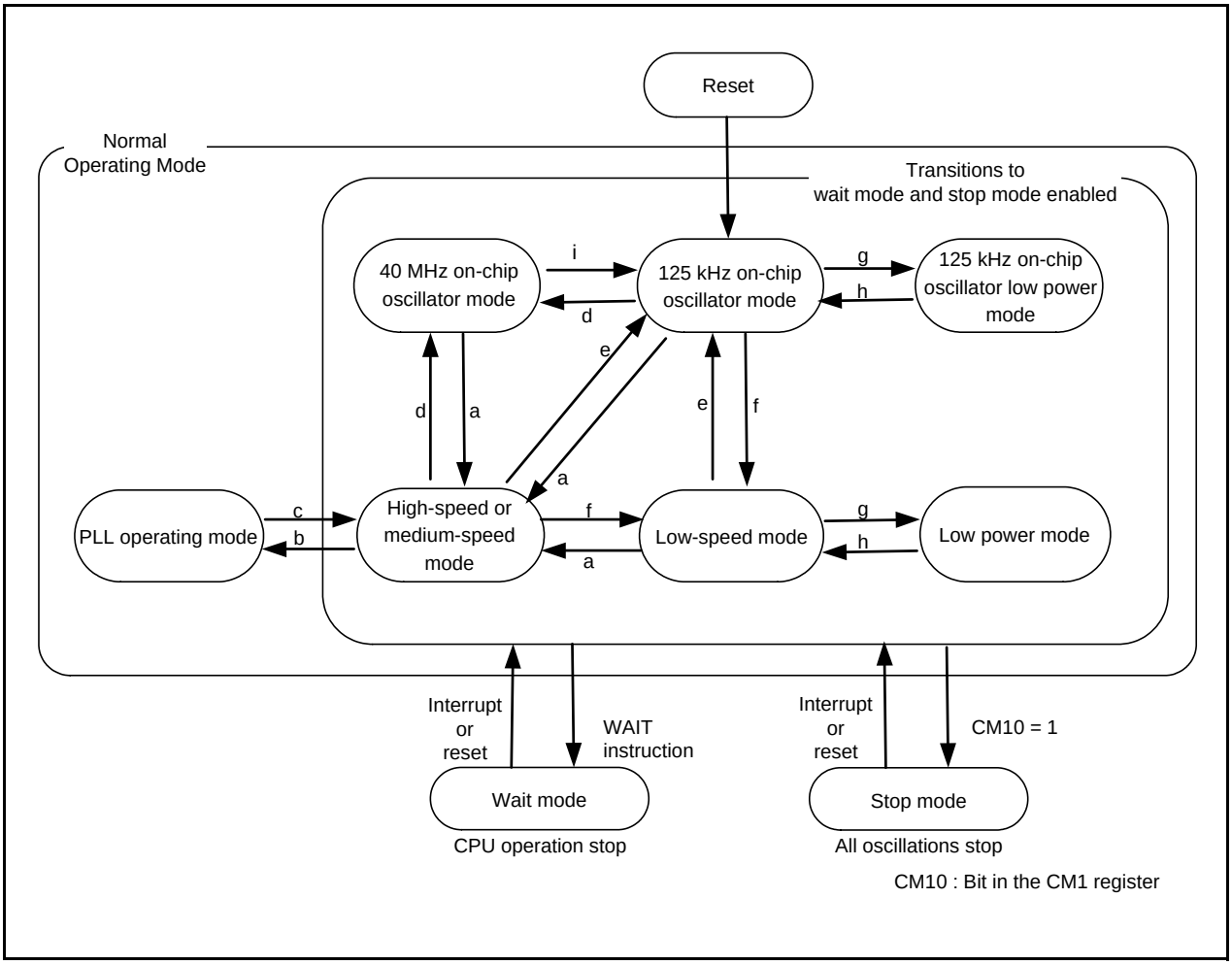


Figure 9.1 Clock Mode Transition

To start or stop clock oscillations, or to change modes in normal operating mode, follow the instructions below.

- Enter a different mode after the clock for that mode stabilizes completely.
- When stopping a clock, do it after mode transition is completed. Do not stop the clock at the same time as mode transition.
- To change the mode, follow procedures listed below. For details on register and bit access, refer to 9.2 “Registers”. Letters a to i correspond to those in Figure 9.1 “Clock Mode Transition”.
- For details on oscillator start and stop, refer to 8.3.1 “Main Clock” to 8.3.6 “Sub Clock (fC)”.

a. Entering high-speed mode or medium-speed mode from 40 MHz on-chip oscillator mode, 125 kHz on-chip oscillator mode or low-speed mode

(1) Start the main clock and wait until the oscillation stabilizes. Refer to 8.3.1 “Main Clock” for details.
(2) Set the CM06 bit to 1 (divide-by-8 mode).
(3) Set the CM11 bit to 0, the CM21 bit to 0 and the CM07 bit to 0 (main clock selected as CPU clock source).

b. Entering PLL operating mode from high-speed mode or medium-speed mode

(1) Select the division of reference frequency counter by setting bits PLC05 and PLC04 in the PLC0 register, and the multiplication rate by setting bits PLC02 to PLC00 in the PLC0 register.
(2) Set the PLC07 bit to 1 (PLL on).
(3) Wait for tsu(PLL) until the PLL clock stabilizes.
(4) Set the CM11 bit to 1, the CM21 bit to 0, and the CM07 bit to 0 (PLL clock selected as CPU clock source).

c. Entering high-speed mode or medium-speed mode from PLL operating mode

(1) Select the main clock divide ratio by the CM06 bit and bits CM17 to CM16.
(2) Set the CM11 bit to 0, the CM21 bit to 0, and the CM07 bit to 0 (main clock selected as CPU clock source).
(3) Set the PLC07 bit to 0 (PLL off).

d. Entering 40 MHz on-chip oscillator mode from high-speed mode, medium-speed mode, or 125 kHz on-chip oscillator mode

(1) Start the 40 MHz on-chip oscillator and wait until the oscillation stabilizes. Refer to 8.3.4 “fOCO-F” for details.
(2) Set the CM06 bit to 1 (divide-by-8 mode)
(3) Set the FRA01 bit to 1 (40 MHz on-chip oscillator).
(4) Set the CM21 bit to 1 (on-chip oscillator clock selected as CPU clock source).

e. Entering 125 kHz on-chip oscillator mode from high-speed mode, or medium-speed mode, or low-speed mode

(1) Start the 125 kHz on-chip oscillator and wait until the oscillation stabilizes. Refer to 8.3.5 “125 kHz On-Chip Oscillator Clock (fOCO-S)” for details.
(2) Set the FRA01 bit to 0 (125 kHz on-chip oscillator).
(3) Set the CM21 bit to 1 (on-chip oscillator clock selected as CPU clock source).
(4) Set the CM07 bit to 0 (main clock, PLL clock, or on-chip oscillator clock selected as CPU clock source).

f. Entering low-speed mode from high-speed mode, medium-speed mode, or 125 kHz on-chip oscillator mode

(1) Start the sub clock and wait until the oscillation stabilizes. Refer to 8.3.6 “Sub Clock (fC)” for details.
(2) Set the CM07 bit to 1 (sub clock selected as CPU clock source).

g. Entering 125 kHz on-chip oscillator low power mode from 125 kHz on-chip oscillator mode
Entering low power mode from low-speed mode

Follow both or either of the procedures below (in no particular order).
(1) Stop the main clock. Refer to 8.3.1 “Main Clock” for details.
(2) Stop the 40 MHz on-chip oscillator. Refer to 8.3.4 “fOCO-F” for details for details.

h. Entering 125 kHz on-chip oscillator mode from 125 kHz on-chip oscillator low power mode
Entering low-speed mode from low power mode

Follow both or either of the procedures below (in no particular order).

(1) Start the main clock and wait until the oscillation stabilizes. Refer to 8.3.1 “Main Clock” for details.
(2) Start the 40 MHz on-chip oscillator and wait until the oscillation stabilizes. Refer to 8.3.4 “fOCO-F” for details.

i. Entering 125 kHz on-chip oscillator mode from 40 MHz on-chip oscillator mode

(1) Start the 125 kHz on-chip oscillator and wait until the oscillation stabilizes. Refer to 8.3.5 “125 kHz On-Chip Oscillator Clock (fOCO-S)” for details.
(2) Set the CM06 bit to 1 (divide-by-8 mode) or the bits FRA22 to FRA20 to 110b (divide-by-8 mode).
(3) Set the FRA01 bit to 0 (125 kHz on-chip oscillator).

9.3.3 Wait Mode

The CPU clock stops in wait mode, therefore, the CPU and the watchdog timer clocked by the CPU clock stops running. However, if the CSPRO bit in the CSPR register is 1 (count source protection mode enabled), the watchdog timer remains active. Because the clock generator does not stop, peripheral functions supplied by a peripheral clock keep operating.

9.3.3.1 Peripheral Function Clock Stop Function

When the CM02 bit is 1 (peripheral function clock f1 stops in wait mode), the f1 clock is turned off while in wait mode, and power consumption is reduced. However, all the peripheral clocks except f1 (i.e. fOCO40M, fOCO-F, fOCO-S, fC, and fC32) do not stop.

9.3.3.2 Entering Wait Mode

The MCU enters wait mode by executing a WAIT instruction.
When the CM11 bit is 1 (PLL clock selected as CPU clock source), set the CM11 bit to 0 (main clock selected as CPU clock source) before entering wait mode. Chip power consumption can be reduced by setting the PLC07 bit to 0 (PLL off).
When using wait mode, set the following:

(1) Set the I flag to 0.
(2) Set the interrupt priority level of bits ILVL2 to ILVL0 in the interrupt control register for the peripheral function interrupt which is used to exit wait mode. Start the peripheral function which is used to exit wait mode if it is stopped.
(3) Set 000b (interrupt disabled) to bits ILVL2 to ILVL0 in the interrupt control registers for the peripheral function interrupts not used to exit wait mode.
(When using any of the following resets or interrupts to exit wait mode, set 000b to bits ILVL2 to ILVL0 in all interrupt control registers for peripheral function interrupts: hardware reset, voltage monitor 0 reset, voltage monitor 2 reset, watchdog timer reset, $\overline{\text{NMI}}$ interrupt, or voltage monitor 2 interrupt).
(4) Set the I flag to 1.
(5) Execute the WAIT instruction.

9.3.3.3 Pin Status in Wait Mode

Table 9.6 lists Pin Status in Wait Mode.

Table 9.6 Pin Status in Wait Mode

Pin		Pin State
I/O ports		Maintains the pin state immediately before entering wait mode
CLKOUT	When fC is selected	Continues to output the clock
	When f1, f8, f32 are selected	• When the CM02 bit is 0 (peripheral clock, f1, does not stop in wait mode): Continues to output the clock • When the CM02 bit is 1 (peripheral clock, f1, stops in wait mode): Maintains the pin state immediately before entering wait mode

9.3.3.4 Exiting Wait Mode

The MCU exits wait mode by a reset or interrupt. Table 9.7 lists Resets and Interrupts to Exit Wait Mode and Conditions for Use.

The peripheral function interrupts are affected by the CM02 bit in the CM0 register. When the CM02 bit is 0 (peripheral function clock f1 does not stop in wait mode), peripheral function interrupts can be used to exit wait mode. When the CM02 bit is 1 (peripheral function clock f1 stops in wait mode), the peripheral functions using the peripheral function clock f1 stop operating, so the peripheral functions activated by external signals and the peripheral function clocks except f1 (fOCO40M, fOCO-F, fOCO-S, fC, fC32) can be used to exit wait mode.

Table 9.7 Resets and Interrupts to Exit Wait Mode and Conditions for Use

Interrupt, Reset			Conditions for Use	
			CM02 = 0	CM02 = 1
Interrupt	Peripheral function interrupt	$\overline{\text{INT}}$	Usable	Usable ($\overline{\text{INT5}}$ is usable when the digital debounce filter is disabled (P17DDR register is FFh))
		Key input	Usable	Usable
		Timer A, timer B	Usable in all modes	Usable when fOCO-F, fOCO-S or fC32 is supplied and is used as count source. Usable when counting external signals in event counter mode.
		Timer S	Usable in all modes except the following: not usable in IC/OC interrupt 0 and 1	Not usable
		Serial interface	Usable in internal clock or external clock	Usable in external clock The internal clock can be used when fOCO-F is supplied and the internal clock is operated by fOCO-F
		Multi-master I^2C-bus interface	Usable	SCL/SDA interrupt is usable
		CAN0 wake-up and CAN1 wake-up	Usable in CAN sleep mode	Usable in CAN sleep mode
		A/D converter	Usable in one-shot mode or single sweep mode.	Usable when fOCO40M is supplied and is used as fAD in one-shot mode or single sweep mode.
		Real-time clock	Usable when fC is supplied and is used as count source	
		LIN0 Low detection	Usable	
		LIN0	Usable	Not usable
	Voltage monitor 2		Usable when the digital filter is disabled (VW2C1 bit in the VW2C register is 1). Usable when the digital filter is enabled (VW2C1 bit in the VW2C register is 0) and fOCO-S is supplied (CM14 bit in the CM1 register is 0).	
	$\overline{\text{NMI}}$		Usable	Usable when the digital debounce filter is disabled (NDDR register is FFh)
Reset	Hardware reset		Usable	
	Voltage monitor 0 reset		Usable	
	Voltage monitor 2 reset		Usable when the digital filter is disabled (VW2C1 bit in the VW2C register is 1). Usable when the digital filter is enabled (VW2C1 bit in the VW2C register is 0) and fOCO-S is supplied (CM14 bit in the CM1 register is 0).	
	Watchdog timer		Usable when count source protection mode is enabled (the CSPRO bit in the CSPR register is 1).	

When the MCU exits wait mode by using an interrupt, an interrupt request is generated, the CPU clock starts running, and interrupt routine is performed.

When the MCU exits wait mode by an interrupt, the CPU clock is the same CPU clock used while executing the WAIT instruction.

9.3.4 Stop Mode

In stop mode, all oscillator are stopped, so the CPU clock and peripheral function clocks are also stopped. Therefore, the CPU and the peripheral functions using these clocks stop operating. The least amount of power is consumed in this mode. If the voltage applied to pin VCC is VRAM or greater, the contents of internal RAM are retained. When applying 3.0 V or less to pin VCC, make sure VCC ≥ VRAM.

However, the peripheral functions activated by external signals keep operating.

9.3.4.1 Entering Stop Mode

The MCU enters stop mode by setting the CM10 bit in the CM1 register to 1 (all clocks turned off). At the same time, the CM06 bit in the CM0 register becomes 1 (divide-by-8 mode), and the CM15 bit in the CM1 register becomes 1 (main clock oscillator drive capability high).

Before entering stop mode, set the CM20 bit to 0 (oscillator stop/restart detect function disabled).

When the CM11 bit is 1 (PLL clock used as the CPU clock source), set the CM11 bit to 0 (main clock used as the CPU clock source), and then the PLC07 bit to 0 (PLL turned off) before entering stop mode.

When using stop mode, set the following:

(1) Set the I flag to 0.

(2) Set the interrupt priority level of bits ILVL2 to ILVL0 in the interrupt control register for the peripheral function interrupt which is used to exit stop mode. Start the peripheral function which is used to stop mode if it is stopped.

(3) Set 000b (interrupt disabled) to bits ILVL2 to ILVL0 in the interrupt control registers for the peripheral function interrupts not used to exit stop mode.
(When using any of the following resets or interrupts to exit stop mode, set 000b to bits ILVL2 to ILVL0 in all interrupt control registers for peripheral function interrupts: hardware reset, voltage monitor 0 reset, $\overline{\text{NMI}}$ interrupt, or voltage monitor 2 interrupt)

(4) Set the I flag to 1.

(5) Set the CM10 bit in the CM1 register to 1.

When using the $\overline{\text{NMI}}$ interrupt to exit stop mode, set the NDDR register to FFh before setting the CM10 bit to 1. When using the $\overline{\text{INT5}}$ interrupt to exit stop mode, set the P17DDR register to FFh before setting the CM10 bit to 1.

9.3.4.2 Pin Status in Stop Mode

Table 9.8 lists Pin Status in Stop Mode.

Table 9.8 Pin Status in Stop Mode

Pin	Pin State
I/O ports	Maintains the pin state immediately before entering stop mode
CLKOUT	High
XOUT	High
XCIN, XCOUT	High-impedance

9.3.4.3 Exiting Stop Mode

Use a reset or an interrupt to exit stop mode. Table 9.9 lists Resets and Interrupts to Exit Stop Mode and Conditions for Use.

Table 9.9 Resets and Interrupts to Exit Stop Mode and Conditions for Use

Interrupt, Reset			Conditions for Use
Interrupt	Peripheral function interrupt	$\overline{\text{INT}}$	Usable($\overline{\text{INT5}}$ is usable when the digital debounce filter is disabled (P17DDR register is FFh))
		Key input	Usable
		Timer A, timer B	Usable when counting external signals in event counter mode
		Serial interface	Usable when an external clock is selected
		Multi-master I^2C-bus interface	SCL/SDA interrupt is usable
		CAN0 wake-up, CAN1 wake-up	Usable in CAN sleep mode
		LIN0 Low detection	Usable
	Voltage monitor 2 interrupt		Usable when the digital filter is disabled (VW2C1 bit in the VW2C register is 1)
	$\overline{\text{NMI}}$		Usable when the digital debounce filter is disabled (NDDR register is FFh)
Reset	Hardware reset		Usable
	Voltage monitor 0 reset		Usable

To exit stop mode by using hardware reset, voltage monitor 0 reset, $\overline{\text{NMI}}$ interrupt, or voltage monitor 2 interrupt, set bits ILVL2 to ILVL0 in the interrupt control registers for the peripheral function interrupt to 000b (interrupt disabled) before setting the CM10 bit to 1.

When the MCU exits stop mode by using an interrupt, an interrupt request is generated, the CPU clock starts running, and interrupt routine is performed.
When exiting stop mode by means of an interrupt, the CPU clock source varies depending on the CPU clock source setting before the MCU had entered stop mode. Table 9.10 lists CPU Clock After Exiting Stop Mode.

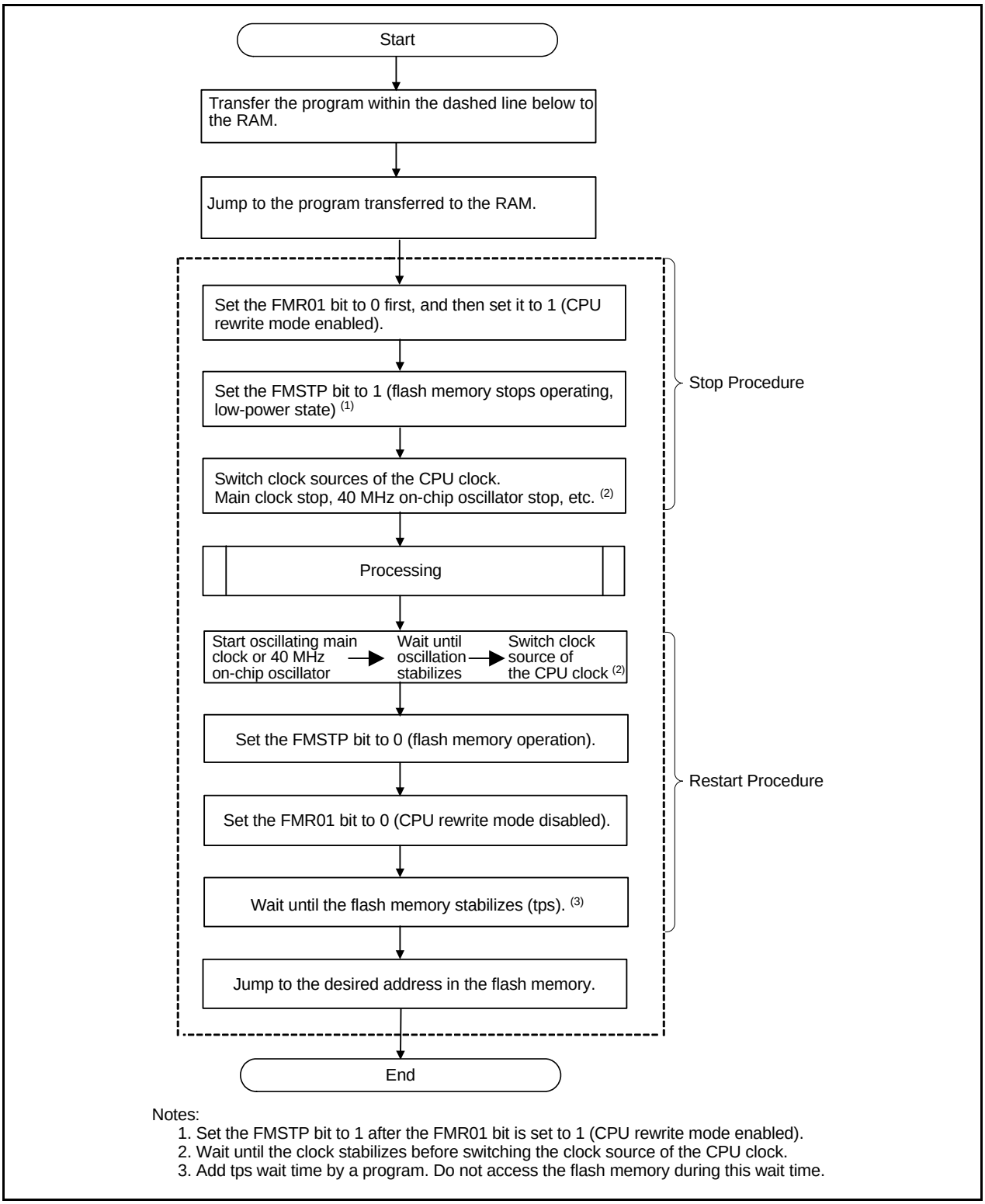
Table 9.10 CPU Clock After Exiting Stop Mode

CPU Clock Before Entering Stop Mode	CPU Clock After Exiting Stop Mode
Main clock divided by 1 (no division), 2, 4, 8 or 16	Main clock divided by 8
fOCO-S divided by 1 (no division), 2, 4, 8 or 16	fOCO-S divided by 8
fOCO-F divided by 1 (no division), 2, 4, 8 or 16	fOCO-F divided by 8
fC	fC

9.4 Power Control in Flash Memory

9.4.1 Stopping Flash Memory

When the flash memory is stopped, current consumption is reduced. Execute a program in the RAM. Figure 9.2 shows the setting procedure to stop and restart the flash memory. Follow the flowchart of Figure 9.2.



Notes:
1. Set the FMSTP bit to 1 after the FMR01 bit is set to 1 (CPU rewrite mode enabled).
2. Wait until the clock stabilizes before switching the clock source of the CPU clock.
3. Add tps wait time by a program. Do not access the flash memory during this wait time.

Figure 9.2 Stop and Restart of the Flash Memory

9.4.2 Reading Flash Memory

Current consumption while reading the flash memory can be reduced by using bits FMR22 and FMR23 in the FMR2 register.

9.4.2.1 Slow Read Mode

Slow read mode can be used when f(BCLK) is less than or equal to f(SLOW_R) and the PM17 bit in the PM1 register is 1 (one wait). Figure 9.3 shows Setting and Canceling Slow Read Mode.
When using 125 kHz on-chip oscillator clock or sub clock as the CPU clock source, a wait is unnecessary (technical update number: TN-16C-A179A/E).

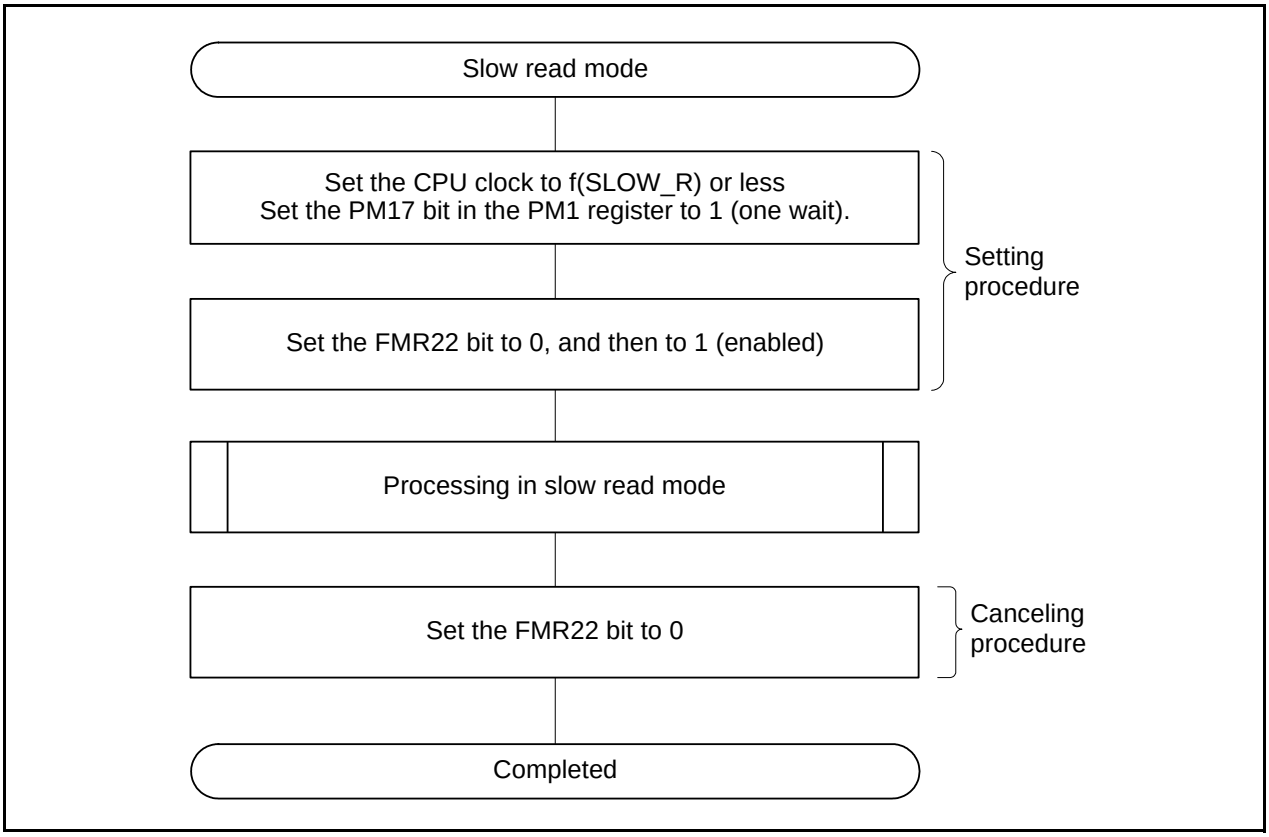
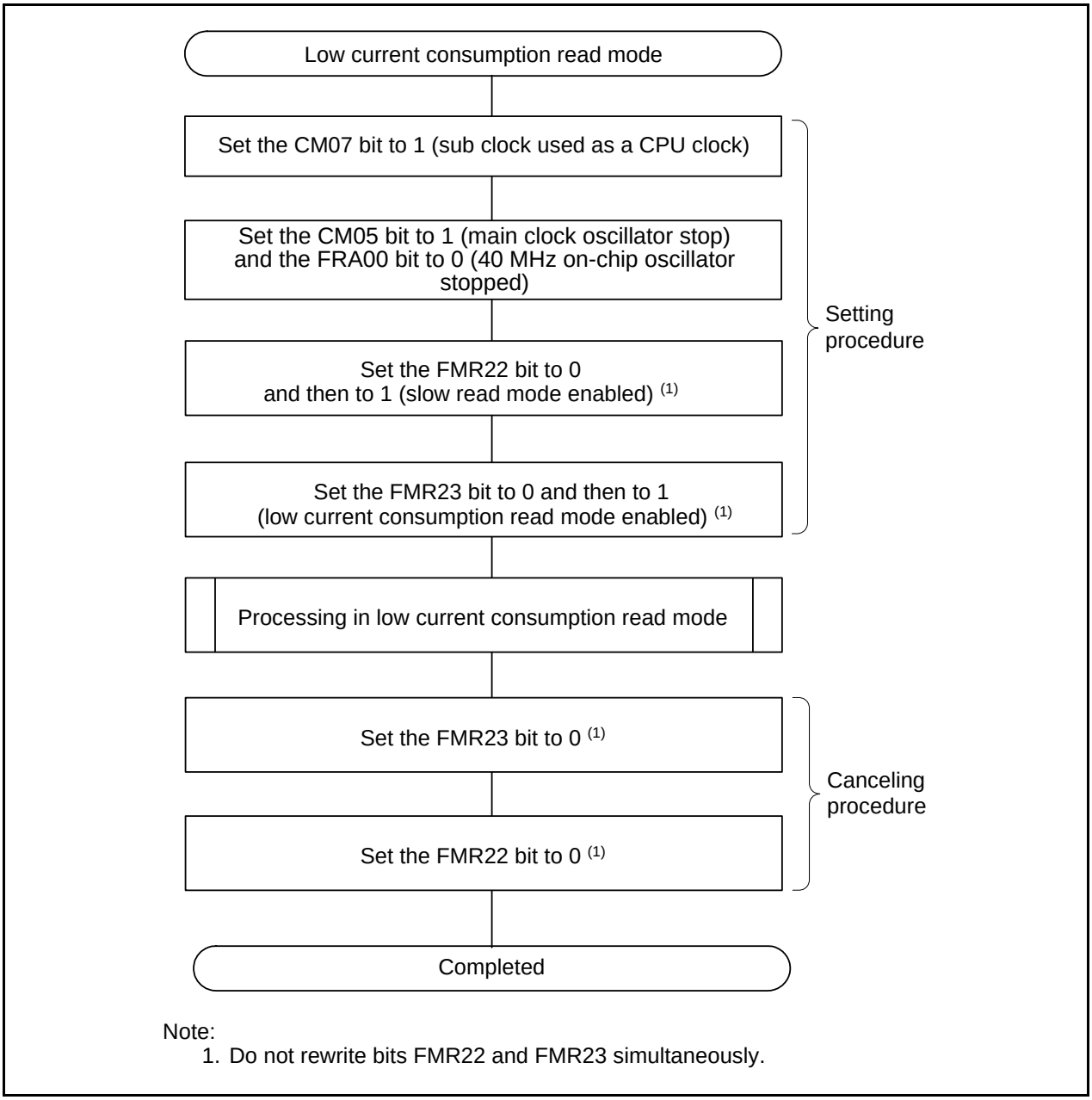


Figure 9.3 Setting and Canceling Slow Read Mode

9.4.2.2 Low Current Consumption Read Mode

Low current consumption read mode can be used when the CM07 bit in the CM0 register is 1 (sub clock used as CPU clock). Figure 9.4 shows Setting and Canceling Low Current Consumption Read Mode.



Note:
1. Do not rewrite bits FMR22 and FMR23 simultaneously.

Figure 9.4 Setting and Canceling Low Current Consumption Read Mode

9.5 Reducing Power Consumption

To reduce power consumption, refer to the following descriptions when designing a system or writing a program.

9.5.1 Ports

The MCU retains the state of each I/O port even when it enters wait mode or stop mode. A current flows in the active output ports. A shoot-through current flows to the input ports in the high-impedance state. Set the unassigned pins to input state, wait until the potential stabilizes, and then enter wait mode or stop mode.

9.5.2 A/D Converter

When not performing A/D conversion, set the ADSTBY bit in the ADCON1 register to 0 (A/D operation stopped).

9.5.3 D/A Converter

When not performing D/A conversion, set the DA0E bit in the DACON register to 0 (Output disabled) and the DA0 register to 00h.

9.5.4 Stopping Peripheral Functions

Use the CM02 bit in the CM0 register to stop the unnecessary peripheral functions while in wait mode.

9.5.5 Switching the Oscillation-Driving Capacity

Set the driving capacity to low when oscillation is stable.

9.6 Notes on Power Control

9.6.1 CPU Clock

When switching the CPU clock source, wait until oscillation of the switched clock source is stable. After exiting stop mode, wait until oscillation stabilizes before changing the division.

9.6.2 Wait Mode

- Insert four or more NOP instructions following the WAIT instruction. When entering wait mode, because the instruction queue prefetches instructions that follow the WAIT instruction, prefetched instructions are sometimes executed prior to the interrupt routine used to exit wait mode. As shown below, when the instruction to set the I flag to 1 is allocated just before the WAIT instruction, interrupt requests are not accepted before the WAIT instruction is executed.

  The following is an example program for entering wait mode:

```
Program Example: FSET    I          ;
                 WAIT               ; Enter wait mode
                 NOP                ; Insert at least four NOP instructions
                 NOP
                 NOP
                 NOP
```

- Do not enter wait mode from PLL operating mode. To enter wait mode from PLL operating mode, first enter medium-speed mode, then set the PLC07 bit to 0 (PLL off).
- Do not enter wait mode from low current consumption read mode. To enter wait mode from low current consumption read mode, set the FMR23 bit in the FMR2 register to 0 (low current consumption read mode disabled).
- Do not enter wait mode from CPU rewrite mode. To enter wait mode from CPU rewrite mode, first set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled), then disable the DMA transfer.
- Set the PLC07 bit in the PLC0 register to 0 (PLL off). When the PLC07 bit is 1 (PLL on), current consumption cannot be reduced even in wait mode.

9.6.3 Stop Mode

- When exiting stop mode by a hardware reset, drive the $\overline{\text{RESET}}$ pin low for 20 fOCO-S cycles or more.
- Set the MR0 bit in the TAiMR register (i = 0 to 4) to 0 (pulse not output) when using timer A to exit stop mode.
- When entering stop mode, insert a JMP.B instruction immediately after executing an instruction that sets the CM10 bit in the CM1 register to 1 (stop mode), and then insert at least four NOP instructions. When entering stop mode, the instruction queue reads ahead the instructions following the instruction which sets the CM10 bit to 1. Thus, some of the instructions may be executed before the MCU enters stop mode or before the interrupt routine for returning from stop mode. As shown below, when the instruction to set the I flag to 1 is allocated just before the instruction to set the CM10 bit to 1, interrupt requests are not accepted before entering stop mode.

The following is an example program for entering stop mode:

```
Program Example:  FSET   I
                  BSET   0, CM1   ; Enter stop mode
                  JMP.B  L2       ; Insert a JMP.B instruction
          L2:
                  NOP             ; At least four NOP instructions
                  NOP
                  NOP
                  NOP
```

- The CLKOUT pin outputs a high-level signal in stop mode. Thus, if stop mode is entered right after output on the CLKOUT pin changes state from high to low, the low-level duration of the output signal to the CLKOUT pin becomes shorter.

- Do not enter stop mode from PLL operating mode. To enter stop mode from PLL operating mode, first enter medium-speed mode, then set the PLC07 bit to 0 (PLL off).
- Do not enter stop mode from low current consumption read mode. To enter stop mode from low current consumption read mode, set the FMR23 bit in the FMR2 register to 0 (low current consumption read mode disabled).
- Do not enter stop mode from CPU rewrite mode. To enter stop mode from CPU rewrite mode, first set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled), then disable the DMA transfer.
- Do not enter stop mode when the oscillator stop/restart detect function is enabled. To enter stop mode, set the CM20 bit in the CM2 register to 0 (oscillator stop/restart detect function disabled).
- Do not enter stop mode when the FMR01 bit is 1 (CPU rewrite mode enabled), and do not enter stop mode when the flash memory is stopped (bits FMR01 and FMSTP are 1).

9.6.4 Low Current Consumption Read Mode

- Enter low current consumption read mode through slow read mode (see Figure 9.4 “Setting and Canceling Low Current Consumption Read Mode” for details).
- When the FMR23 bit in the FMR2 register is 1 (low current consumption read mode enabled), do not set the FMSTP bit to 1 (flash memory stopped). Also, when the FMSTP bit is 1, do not set the FMR23 bit to 1.
- When the FMR01 bit in the FMR0 register to 1 (CPU rewrite mode enabled), do not set the FMR23 bit in the FMR2 register to 1 (low current consumption read mode enable).

9.6.5 Slow Read Mode

- When the FMR01 bit in the FMR0 register to 1 (CPU rewrite mode enabled), do not set the FMR22 bit in the FMR2 register to 1 (slow read mode enabled).

10. Processor Mode

10.1 Introduction

Single-chip mode is supported as a processor mode. Table 10.1 lists the Processor Mode Features.

Table 10.1 Processor Mode Features

Processor Mode	Access Space	Pins Assigned as I/O Ports
Single-chip mode	SFR, internal RAM, internal ROM	All pins are I/O ports or peripheral function I/O pins

10.2 Registers

Table 10.2 Registers

Address	Register	Symbol	Reset Value
0005h	Processor Mode Register 1	PM1	0000 1000b
0010h	Program 2 Area Control Register	PRG2C	XXXX XX00b
0221h	Flash Memory Control Register 1	FMR1	00X0 XX0Xb

10.2.1 Processor Mode Register 1 (PM1)

Processor Mode Register 1

b7	b6	b5	b4	b3	b2	b1	b0
	0	0	0	1		0	

Symbol	Address	Reset Value
PM1	0005h	00001000b

Bit Symbol	Bit Name	Function	RW
PM10	Data flash enable bit	0: Reserved area (0E000h to 0FFFFh) 1: Data flash (0E000h to 0FFFFh)	RW
— (b1)	Reserved bit	Set to 0.	RW
PM12	Watchdog timer function select bit	0: Watchdog timer interrupt 1: Watchdog timer reset	RW
— (b3)	Reserved bit	Set to 1.	RW
— (b6-b4)	Reserved bits	Set to 0.	RW
PM17	Wait bit	0: No wait state 1: One wait	RW

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting this register.
The PM12 bit becomes 1 by a program. Setting it to 0 has no effect.

PM10 (Data flash enable bit) (b0)

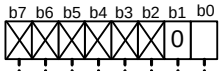
This bit is used to select the function of addresses 0E000h to 0FFFFh.
Data flash includes block A (addresses 0E000h to 0EFFFh) and block B (addresses 0F000h to 0FFFFh). When data flash is selected by the setting of the PM10 bit, both block A and block B can be used.
The PM10 bit automatically becomes 1 while the FMR01 bit in the FMR0 register is 1 (CPU rewrite mode).

PM17 (Wait Bit) (b7)

This is a software wait select bit for internal memory.

10.2.2 Program 2 Area Control Register (PRG2C)

Program 2 Area Control Register



Symbol	Address	Reset Value
PRG2C	0010h	XXXX XX00b

Bit Symbol	Bit Name	Function	RW
PRG2C0	Program ROM 2 disable bit	0 : Enable program ROM 2 1 : Disable program ROM 2(reserved area)	RW
(b1)	Reserved bit	Set to 0.	RW
— (b7-b2)	No register bits. If necessary, set to 0. The read value is undefined.		—

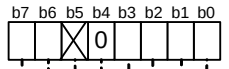
Set the PRC6 bit in the PRCR register to 1 (write enabled) before rewriting this register.

PRG2C0 (Program ROM 2 disable bit) (b0)

This bit is used to select the function of program ROM 2 (addresses 10000h to 13FFFh).
Program ROM 2 includes the on-chip debugger monitor area and user boot code area. Refer to 29.7.1 “User Boot Function” for details.

10.2.3 Flash Memory Control Register 1 (FMR1)

Flash Memory Control Register 1



Symbol	Address	Reset Value
FMR1	0221h	00X0 XX0Xb

Bit Symbol	Bit Name	Function	RW
— (b0)	Reserved bit	The read value is undefined.	RO
FMR11	Write to FMR6 register enable bit	0 : Disabled 1 : Enabled	RW
— (b3-b2)	Reserved bits	The read value is undefined.	RO
— (b4)	Reserved bit	Set to 0	RW
— (b5)	No register bit. If necessary, set to 0. The read value is undefined.		—
FMR16	Lock bit status flag	0 : Lock 1 : Unlock	RO
FMR17	Data flash wait bit	0 : 1 wait 1 : Follow the setting of the PM17 bit in the PM1 register	RW

FMR17 (Data Flash Wait Bit) (b7)

This bit is used to select the number of wait states for data flash.
When setting this bit to 0, one wait is inserted to the read cycle of the data flash. The write cycle is not affected.

10.3 Software Wait

The PM17 bit in the PM1 register, PM20 bit in the PM2 register, and FMR17 bit in the FMR1 register select software wait and the bus cycles will be determined accordingly. Table 10.3 lists the relation between software wait related bits and bus cycle.

Table 10.3 Software Wait Related Bits and Bus Cycles

Area		Software Wait Related Bits and Settings		Software Wait	Bus Cycle
		FMR17 bit in the FMR1 register	PM17 bit in the PM1 register		
SFR		—	—	1 wait	2 BCLK cycles (1)
Internal RAM		—	0	no wait	1 BCLK cycle (1)
			1	1 wait	2 BCLK cycles
Internal ROM	Program ROM 1 Program ROM 2	—	0	no wait	1 BCLK cycles (1)
			1	1 wait	2 BCLK cycles
	Data flash	0	—	1 wait	2 BCLK cycles (1)
		1	0	no wait	1 BCLK cycle
			1	1 wait	2 BCLK cycles

—: 0 or 1 has no effect

Note:
1. Status after reset.

10.4 Bus Hold

The internal bus is in a hold state under the following condition:

- Rewriting the flash memory in EW1 mode while auto-programming or auto-erasing

When the bus is in hold state, the following occur:

- CPU stops.
- DMAC stops.
- The watchdog timer stops when the CSPRO bit in the CSPR register is 0 (count source protection mode disabled).
- The I/O port state is maintained.

Bus use priority is given to bus hold, DMAC, and CPU in descending order. However, if the CPU is accessing an odd address in word units, DMAC cannot gain control of the bus between two separate accesses. Figure 10.1 “Bus Use Priority” shows the bus use priority.

Bus Hold > DMAC > CPU

Figure 10.1 Bus Use Priority

11. Programmable I/O Ports

Note

The 80-pin package has no P4_0 to P4_7, P5_0 to P5_7, P9_4.
The 64-pin package has no P0_4 to P0_7, P1_0 to P1_4, P3_4 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P9_4 to P9_7.

11.1 Introduction

Table 11.1 lists Programmable I/O Port Specifications (hereafter referred to as I/O ports).
Each pin functions as a programmable I/O port or a peripheral function input/output.
To set peripheral functions, refer to the description for the individual function. To use ports as peripheral function input/output pins, refer to 11.4 “Peripheral Function I/O”.
Table 11.2 lists the I/O ports.

Table 11.1 Programmable I/O Ports Specifications

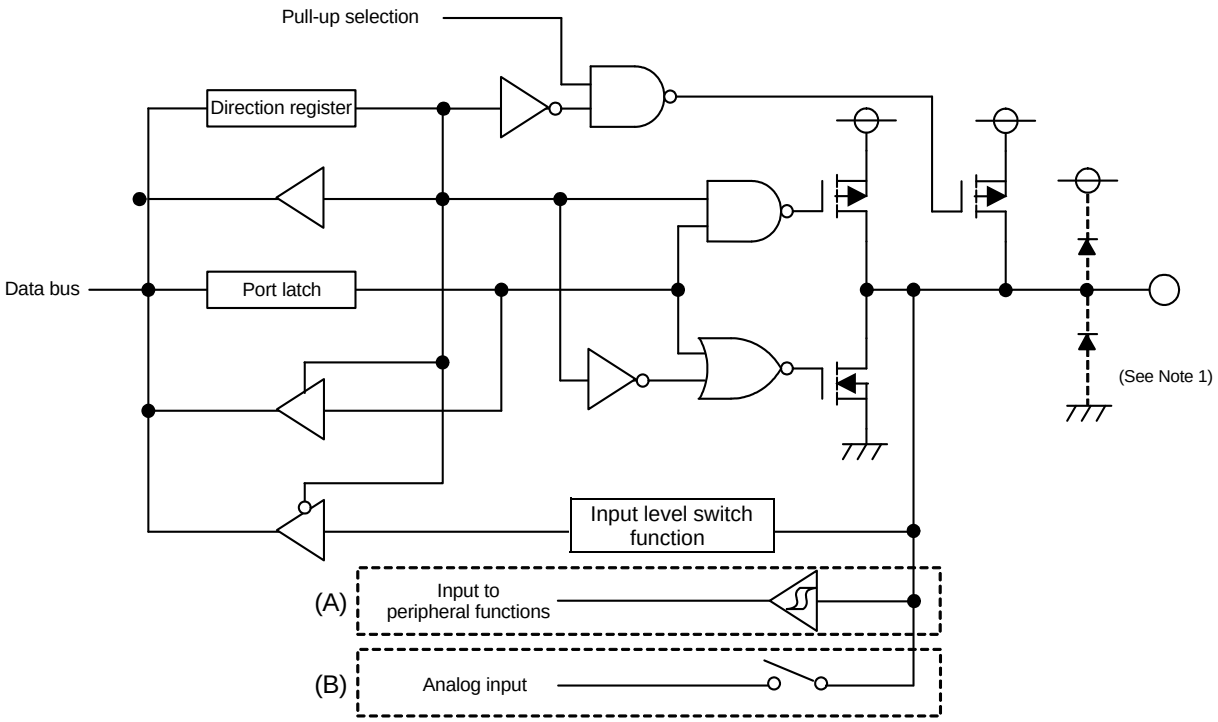
Item	Specification		
	100-pin	80-pin	64-pin
The number of ports	88	71	55
Input/output	Select input/output for each port by a program.		
Selectable function	A pull-up resistor is selectable for every four input ports. (P8_5: No pull-up resistor) Select the input level for every eight input ports.		

Table 11.2 I/O Ports

Pin Name			I/O Type	Function
100-pin	80-pin	64-pin		
P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6 to P8_7, P9_0 to P9_7, P10_0 to P10_7	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	P0_0 to P0_3, P1_5 to P1_7, P2_0 to P2_7, P3_0 to P3_3, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6 to P8_7, P9_0 to P9_3, P10_0 to P10_7	I/O	Input/output port CMOS output, pull-up resistor selectable Input level selectable
P8_5	P8_5	P8_5	I/O	Input/output port N-channel open drain output, no pull-up resistor, pull-up resistor selectable

11.2 I/O Ports and Pins

Figure 11.1 to Figure 11.6, and Table 11.3 and Table 11.8 show the programmable I/O ports, and Figure 11.8 shows the pins.



Note:

1. ----|◄---- symbolizes a parasitic diode.
   Make sure the input voltage to each port does not exceed VCC.

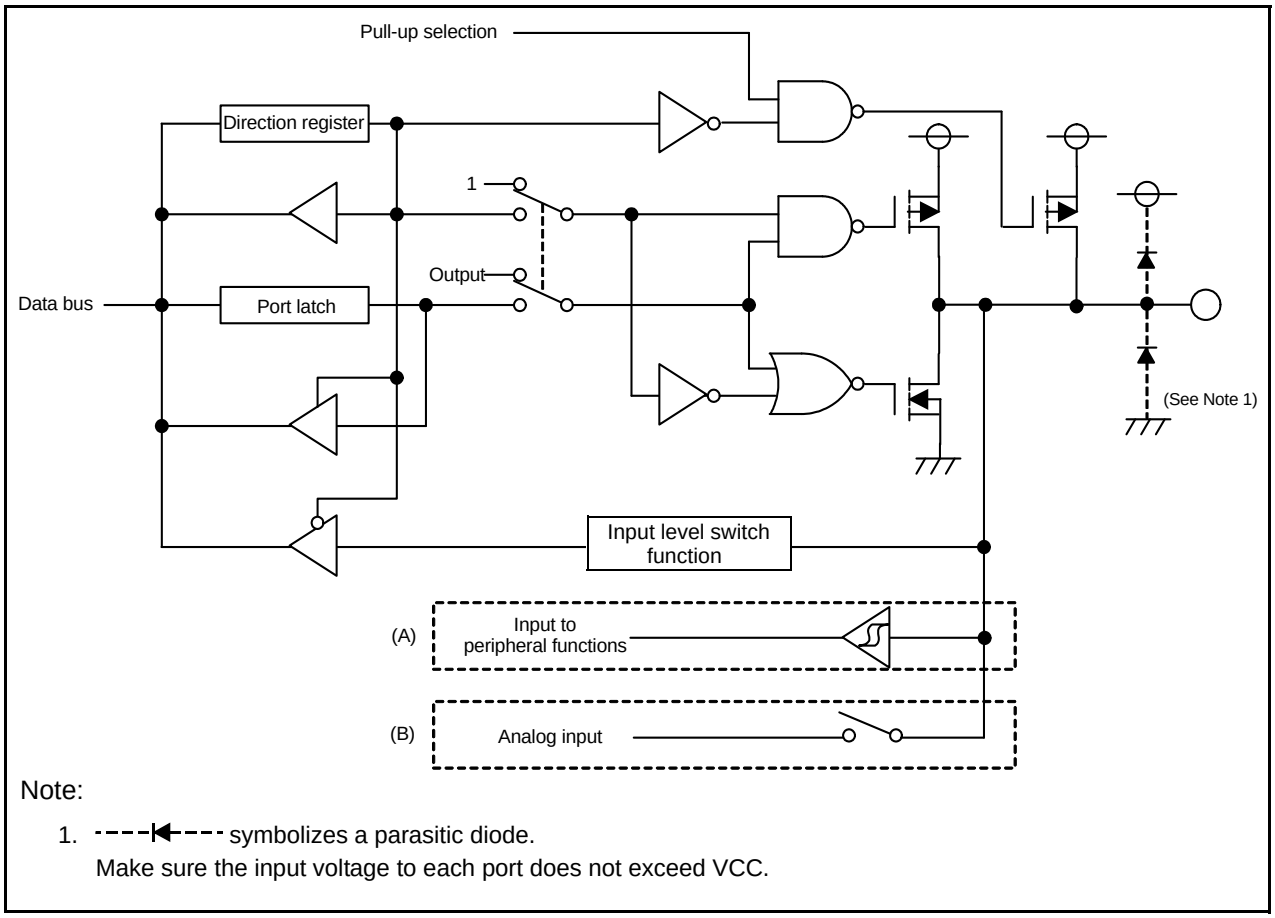
Figure 11.1 I/O Ports (Basic)

Table 11.3 I/O Ports (Basic)

Port	Peripheral Function I/O	
	Peripheral function input (A) in Figure 11.1	Analog input (B) in Figure 11.1
P3_4 to P3_7, P4_0 to P4_7, P5_0 to P5_7	N/A	N/A
P0_0 to P0_7, P10_0 to P10_3, P9_3 (1)	N/A	Available
P3_1, P6_2, P6_6, P7_7, P8_2 to P8_4, P9_4	Available	N/A
P9_1(2), P9_2, P9_7, P10_4 to P10_7	Available	Available

Notes:

1. P9_3 is for the 80-pin package and 64-pin package of the M16C/57 Group
2. P9_1 is for the 100-pin package of the M16C/5M, M16C/57 Group



Note:

1. ----|◄---- symbolizes a parasitic diode.
   Make sure the input voltage to each port does not exceed VCC.

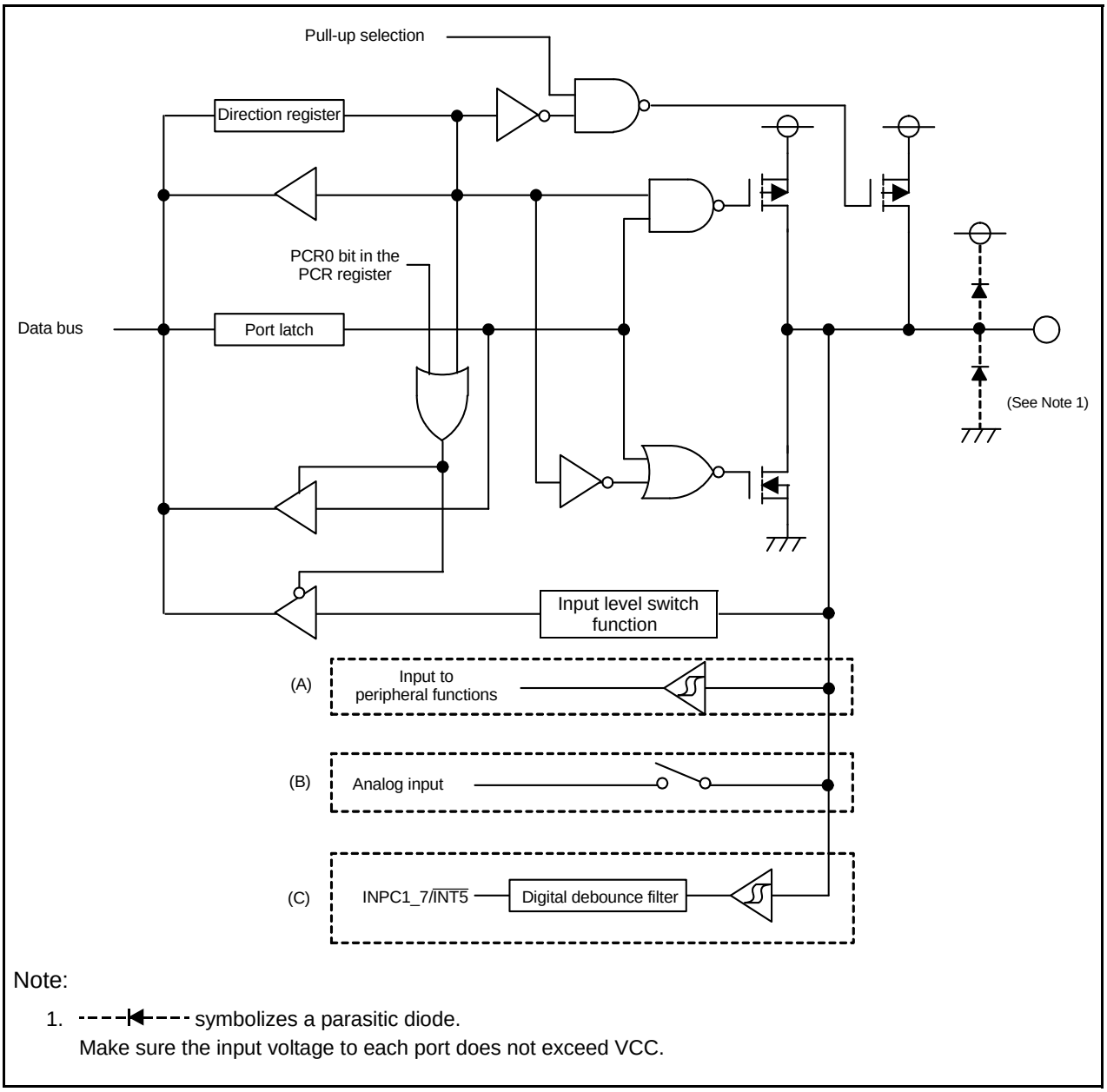
Figure 11.2 I/O Ports (Output)

Table 11.4 I/O Ports (Output)

Port	Peripheral Function I/O	
	Peripheral function input (A) in Figure 11.2	Analog input (B) in Figure 11.2
P9_3 (1)	N/A	Available
P2_2 to P2_7, P3_0, P3_3, P6_0, P6_1, P6_4, P6_5, P7_4 to P7_6, P8_0, P8_1	Available	N/A
P9_0, P9_5	Available	Available

Note:

1. P9_3 is for the 80-pin package and 64-pin package of the M16C/5M Group



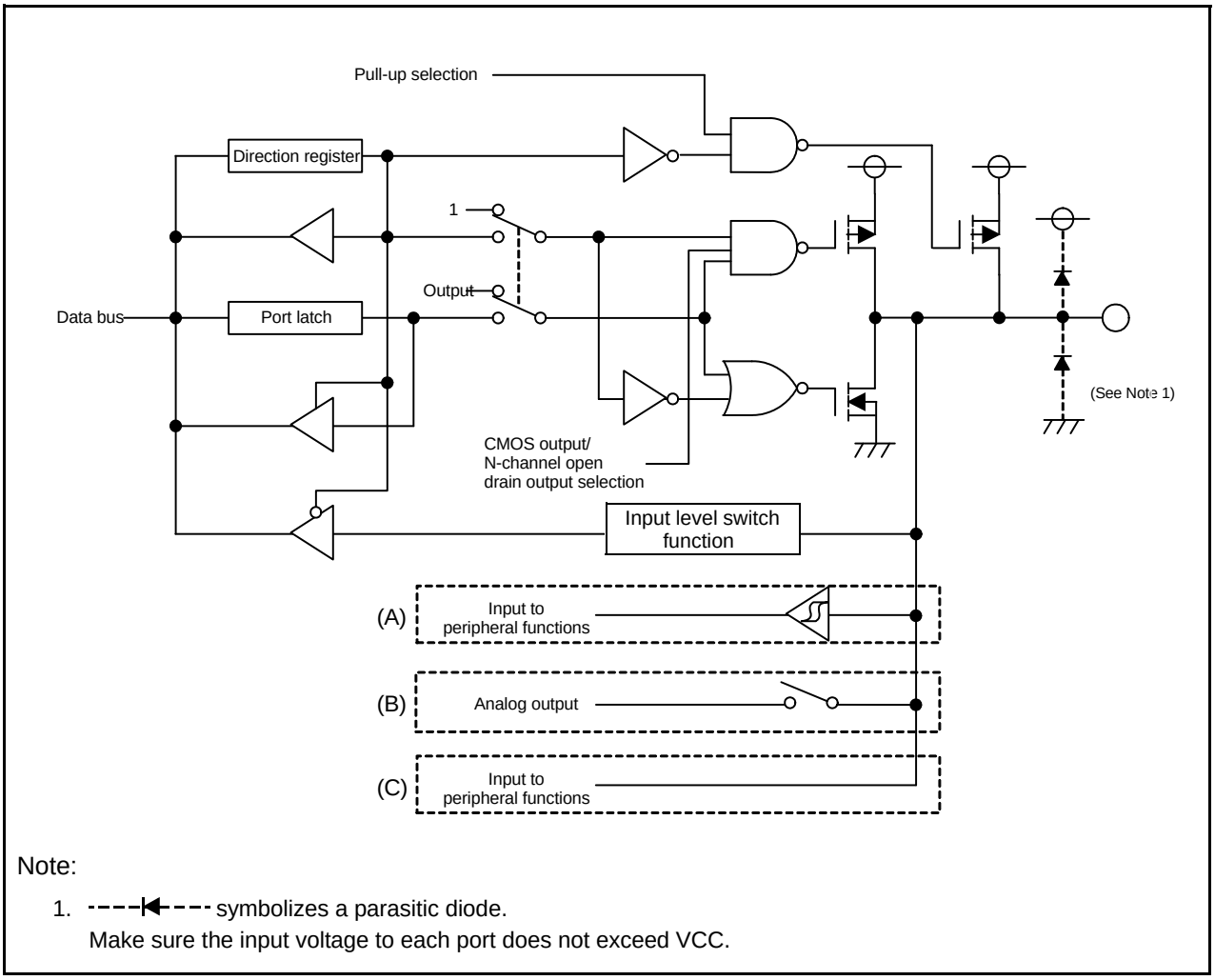
Note:

1. ----|◄|---- symbolizes a parasitic diode.
   Make sure the input voltage to each port does not exceed VCC.

Figure 11.3 I/O Ports (Port P1, P1_7)

Table 11.5 I/O Ports (Port P1, P1_7)

Port	Peripheral Function I/O		
	Peripheral Function Input (A) in Figure 11.3	Analog input (B) in Figure 11.3	Peripheral function input (C) in Figure 11.3
P1_4	N/A	N/A	N/A
P1_0 to P1_3	N/A	Available	N/A
P1_5, P1_6	Available	N/A	N/A
P1_7	Available	N/A	Available



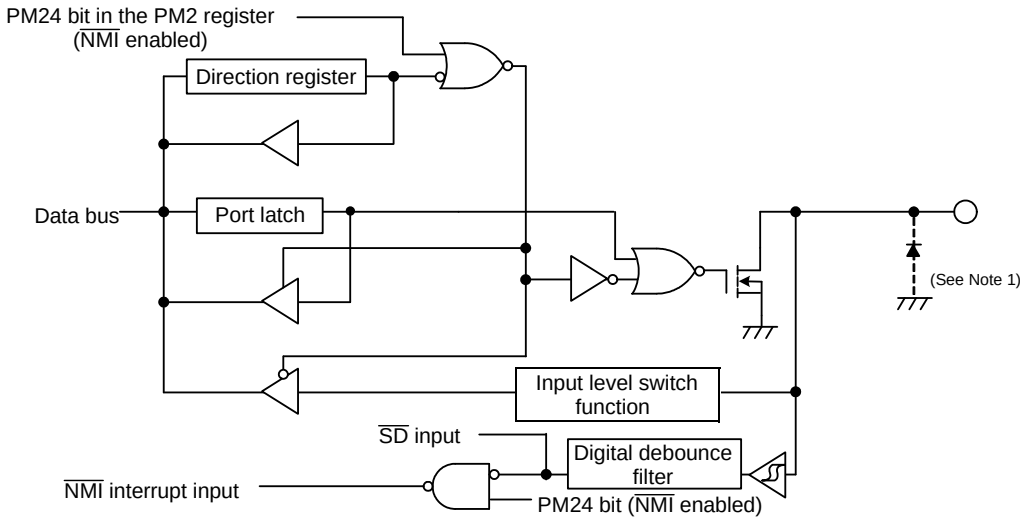
Note:

1. ----|◄---- symbolizes a parasitic diode.
   Make sure the input voltage to each port does not exceed VCC.

Figure 11.4 I/O Ports (CMOS output/N-channel open drain output selection)

Table 11.6 I/O Ports (CMOS output/N-channel open drain output selection)

Port	Peripheral Function I/O		
	Peripheral function input (A) in Figure 11.4	Analog input (B) in Figure 11.4	Peripheral function input (C) in Figure 11.4
P3_2, P6_3, P6_7	N/A	N/A	N/A
P9_6	N/A	Available	N/A
P7_0 to P7_3	Available	N/A	N/A
P2_0, P2_1	Available	N/A	Available



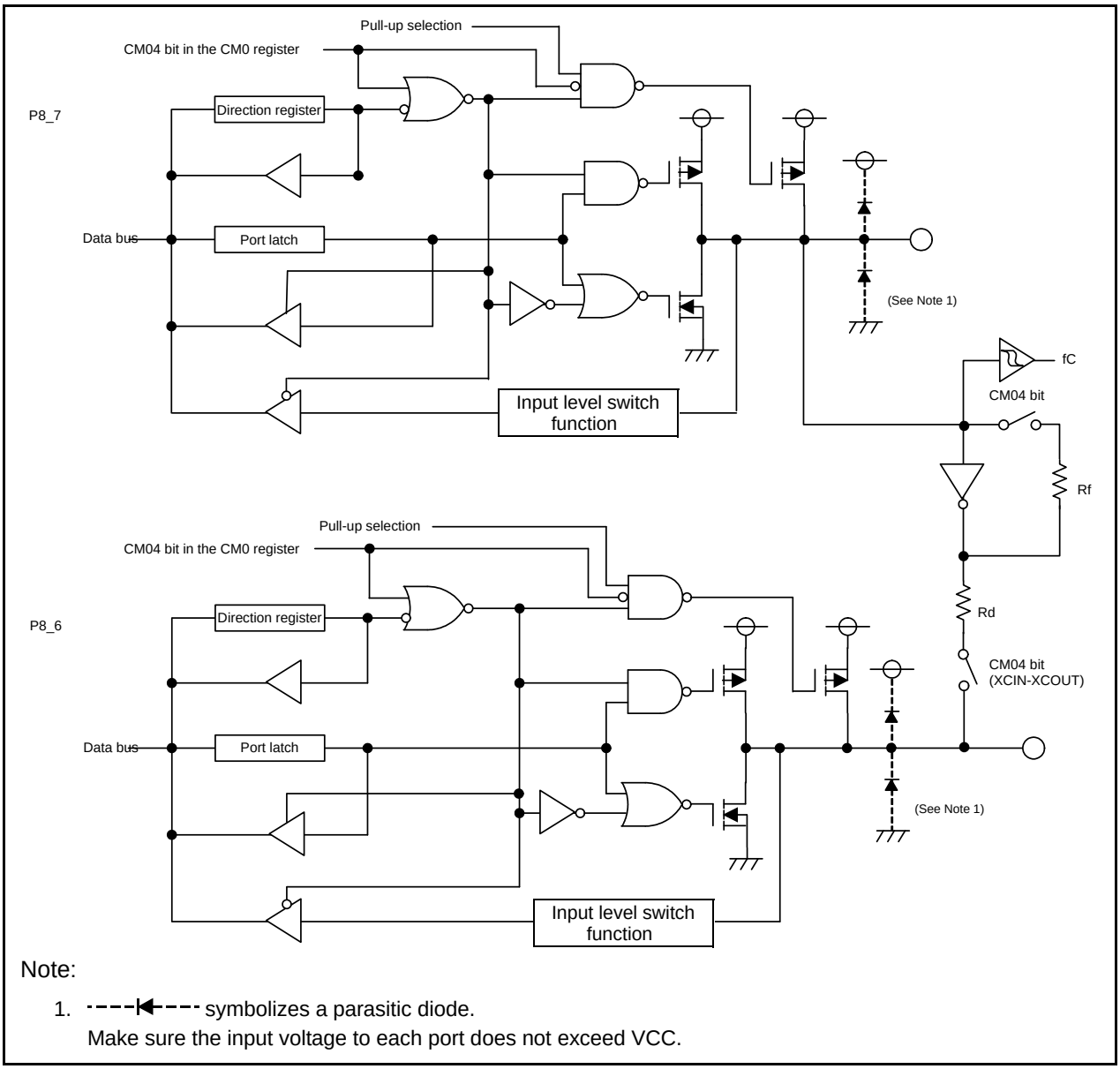
Note:

1. ----|◄---- symbolizes a parasitic diode.
   Make sure the input voltage to each port does not exceed VCC.

Figure 11.5 I/O Ports ($\overline{\text{NMI}}$)

Table 11.7 I/O Ports ($\overline{\text{NMI}}$)

Port	Peripheral Function I/O	
	Peripheral function input	Analog input
P8_5	Available	N/A



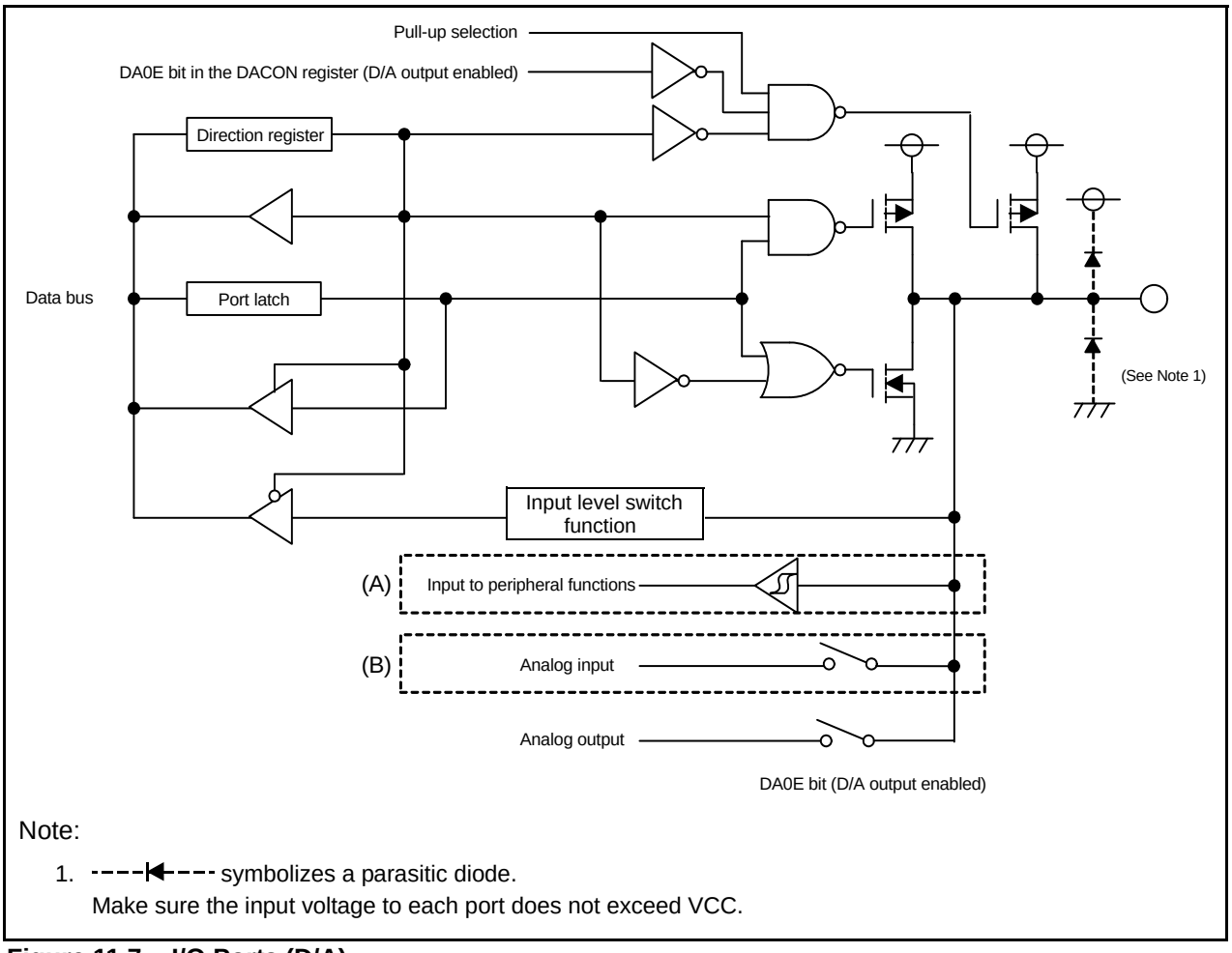
Note:

1. ----|◄---- symbolizes a parasitic diode.
   Make sure the input voltage to each port does not exceed VCC.

Figure 11.6 I/O Ports (XC)

Table 11.8 I/O Ports (XC)

Port	Peripheral Function I/O	
	Peripheral function input	Analog input
P8_6, P8_7	N/A	N/A



Note:

1. ----|◄|---- symbolizes a parasitic diode.
   Make sure the input voltage to each port does not exceed VCC.

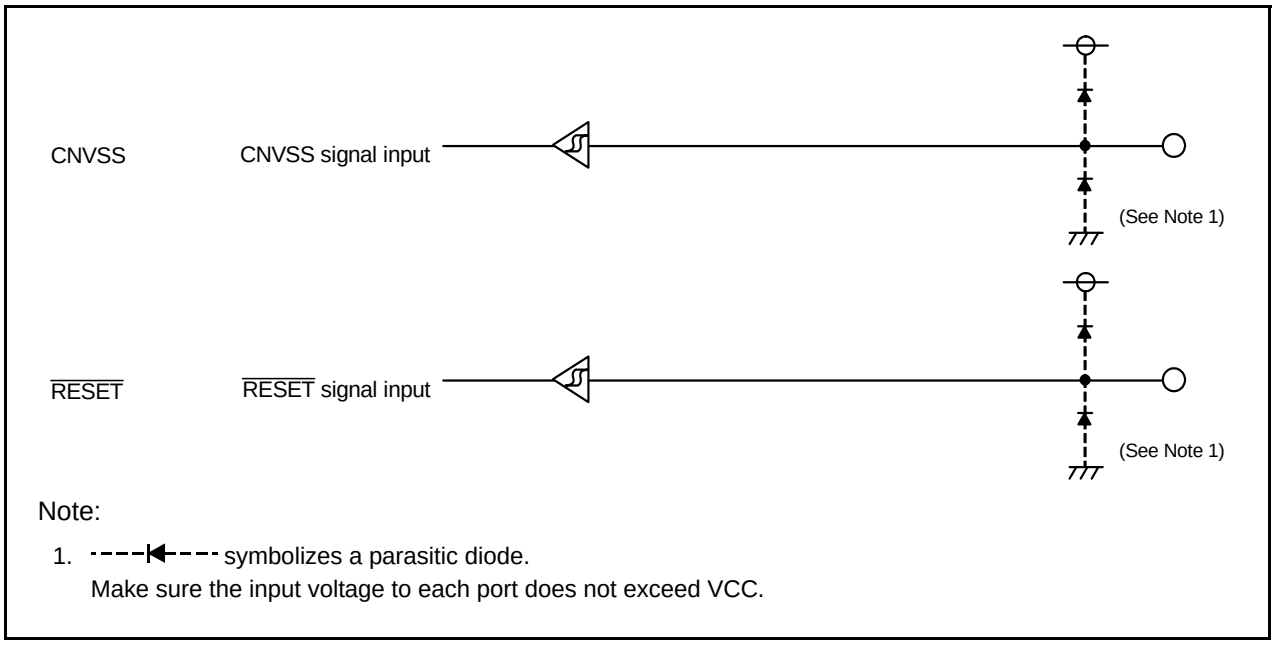
Figure 11.7 I/O Ports (D/A)

Table 11.9 I/O Ports (D/A)

Port	Peripheral Function I/O	
	Peripheral function input (A) in Figure 11.7	Analog input (B) in Figure 11.7
P9_1 (1)	Available	Available
P9_3 (2)	Available	N/A

Notes:

1. P9_1 is for the 80-pin package and 64-pin package of the M16C/5M, M16C/57 Group
2. P9_3 is for the 100-pin package of the M16C/5M, M16C/57 Group



Note:

1. ----|◄---- symbolizes a parasitic diode.
   Make sure the input voltage to each port does not exceed VCC.

Figure 11.8 Pins

11.3 Registers

Table 11.10 Registers

Address	Register Name	Register Symbol	Reset Value
02FEh	$\overline{\text{NMI}}$ Digital Debounce Register	NDDR	FFh
02FFh	P1_7 Digital Debounce Register	P17DDR	FFh
0360h	Pull-Up Control Register 0	PUR0	00h
0361h	Pull-Up Control Register 1	PUR1	00h
0362h	Pull-Up Control Register 2	PUR2	00h
0366h	Port Control Register	PCR	0XX0 0XX0b
036Ch	Input Threshold Select Register 0	VLT0	00h
036Dh	Input Threshold Select Register 1	VLT1	00h
036Eh	Input Threshold Select Register 2	VLT2	XX00 0000b
0370h	Pin Assignment Control Register	PACR	0XXX X000b
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h	Port P4 Register	P4	XXh
03E9h	Port P5 Register	P5	XXh
03EAh	Port P4 Direction Register	PD4	00h
03EBh	Port P5 Direction Register	PD5	00h
03ECh	Port P6 Register	P6	XXh
03EDh	Port P7 Register	P7	XXh
03EEh	Port P6 Direction Register	PD6	00h
03EFh	Port P7 Direction Register	PD7	00h
03F0h	Port P8 Register	P8	XXh
03F1h	Port P9 Register	P9	XXh
03F2h	Port P8 Direction Register	PD8	00h
03F3h	Port P9 Direction Register	PD9	00h
03F4h	Port P10 Register	P10	XXh
03F6h	Port P10 Direction Register	PD10	00h

11.3.1 $\overline{\text{NMI}}$ Digital Debounce Register (NDDR)

$\overline{\text{NMI}}$ Digital Debounce Register

b7 b0

Symbol	Address	Reset Value
NDDR	02FEh	FFh

Function	Setting Range	RW
With n being the setting value: • n = 00h to FEh: A signal with larger pulse width than $\frac{(n + 1) \times 8}{f1}$ is input to $\overline{\text{NMI}}/\overline{\text{SD}}$. • n = FFh: Digital debounce filter function is disabled and all signals will be input directly.	00h to FFh	RW

When using the $\overline{\text{NMI}}$ interrupt to exit from stop mode, set FFh to the NDDR register before entering stop mode. The NDDR register should be written immediately after the instruction to set the PRC2 bit in the PRCR register to 1 (write enabled). No interrupt or DMA transfer should be generated between these two instructions.

11.3.2 P1_7 Digital Debounce Register (P17DDR)

P1_7 Digital Debounce Register

b7 b0

Symbol	Address	Reset Value
P17DDR	02FFh	FFh

Function	Setting Range	RW
With n being the setting value: • n = 00h to FEh: A signal with larger pulse width than $\frac{(n + 1) \times 8}{f1}$ is input to INPC1_7/$\overline{\text{INT5}}$. • n = FFh: Digital debounce filter function is disabled and all signals will be input directly.	00h to FFh	RW

When using the $\overline{\text{INT5}}$ interrupt to exit from stop mode, set FFh to the P17DDR register before entering stop mode.

11.3.3 Pull-Up Control Register 0 (PUR0)

Pull-Up Control Register 0

b7	b6	b5	b4	b3	b2	b1	b0

Symbol: PUR0 — Address: 0360h — Reset Value: 00h

Bit Symbol	Bit Name	Function	RW
PU00	P0_0 to P0_3 pull-up	0 : Not pulled high 1 : Pulled high	RW
PU01	P0_4 to P0_7 pull-up		RW
PU02	P1_0 to P1_3 pull-up		RW
PU03	P1_4 to P1_7 pull-up		RW
PU04	P2_0 to P2_3 pull-up		RW
PU05	P2_4 to P2_7 pull-up		RW
PU06	P3_0 to P3_3 pull-up		RW
PU07	P3_4 to P3_7 pull-up		RW

The pin for which the bit in the PUR0 register is 1 (pulled high) and the direction bit is 0 (input mode) is pulled high.

11.3.4 Pull-Up Control Register 1 (PUR1)

Pull-Up Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0

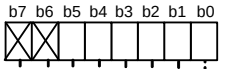
Symbol: PUR1 — Address: 0361h — Reset Value: 00h

Bit Symbol	Bit Name	Function	RW
PU10	P4_0 to P4_3 pull-up	0 : Not pulled high 1 : Pulled high	RW
PU11	P4_4 to P4_7 pull-up		RW
PU12	P5_0 to P5_3 pull-up		RW
PU13	P5_4 to P5_7 pull-up		RW
PU14	P6_0 to P6_3 pull-up		RW
PU15	P6_4 to P6_7 pull-up		RW
PU16	P7_0 to P7_3 pull-up		RW
PU17	P7_4 to P7_7 pull-up		RW

The pin for which the bit in the PUR1 register is 1 (pulled high) and the direction bit is 0 (input mode) is pulled high.

11.3.5 Pull-Up Control Register 2 (PUR2)

Pull-Up Control Register 2



Symbol: PUR2 | Address: 0362h | Reset Value: 00h

Bit Symbol	Bit Name	Function	RW
PU20	P8_0 to P8_3 pull-up	0 : Not pulled high 1 : Pulled high	RW
PU21	P8_4, P8_6, P8_7 pull-up		RW
PU22	P9_0 to P9_3 pull-up		RW
PU23	P9_4 to P9_7 pull-up		RW
PU24	P10_0 to P10_3 pull-up		RW
PU25	P10_4 to P10_7 pull-up		RW
— (b7-b6)	No register bits. If necessary, set to 0. The read value is 0.		—

PU20 (P8_0 to P8_3 pull-up) (b0)
PU22 (P9_0 to P9_3 pull-up) (b2)
PU23 (P9_4 to P9_7 pull-up) (b3)
PU24 (P10_0 to P10_3 pull-up) (b4)
PU25 (P10_4 to P10_7 pull-up) (b5)

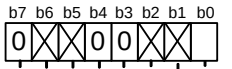
When the PU2i (i = 0, 2 to 5) bit is 1 (pulled high) and the direction bit is 0 (input mode), the corresponding pin is pulled high.

PU21 (P8_4, P8_6, P8_7 pull-up) (b1)

When the PU21 bit is 1 (pulled high) and the direction bit is 0 (input mode), the corresponding pin is pulled high.
The P8_5 pin is not pulled high.

11.3.6 Port Control Register (PCR)

Port Control Register



Symbol	Address	Reset Value
PCR	0366h	0XX0 0XX0b

Bit Symbol	Bit Name	Function	RW
PCR0	Port P1 control bit	Operation performed when the P1 register is read 0: When the port is set to input, the input levels of pins P1_0 to P1_7 are read. When set to output, the port latch is read. 1: The port latch is read regardless of whether the port is set to input or output.	RW
— (b2-b1)	No register bits. If necessary, set to 0. The read value is undefined.		—
— (b4-b3)	Reserved bit	Set to 0.	RW
— (b6-b5)	No register bits. If necessary, set to 0. The read value is undefined.		—
— (b7)	Reserved bit	Set to 0.	RW

PCR0 (Port P1 Control Bit) (b0)

When the P1 register is read after the PCR0 bit is set to 1, the corresponding port latch is read regardless of the PD1 register setting.

11.3.7 Input Threshold Select Register 0 (VLT0)

Input Threshold Select Register 0

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	Reset Value
VLT0	036Ch	00h

Bit Symbol	Bit Name	Function	RW
VLT00	P0 input level select bit	b1 b0 0 0: 0.50 × VCC 0 1: Do not set. 1 0: 0.70 × VCC 1 1: Do not set.	RW
VLT01			RW
VLT02	P1 input level select bit	b3 b2 0 0: 0.50 × VCC 0 1: Do not set. 1 0: 0.70 × VCC 1 1: Do not set.	RW
VLT03			RW
VLT04	P2 input level select bit	b5 b4 0 0: 0.50 × VCC 0 1: Do not set. 1 0: 0.70 × VCC 1 1: Do not set.	RW
VLT05			RW
VLT06	P3 input level select bit	b7 b6 0 0: 0.50 × VCC 0 1: Do not set. 1 0: 0.70 × VCC 1 1: Do not set.	RW
VLT07			RW

The input level of ports can be selected. The input level of peripheral functions is not affected.

11.3.8 Input Threshold Select Register 1 (VLT1)

Input Threshold Select Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	Reset Value
VLT1	036Dh	00h

Bit Symbol	Bit Name	Function	RW
VLT10	P4 input level select bit	b1 b0 0 0: 0.50 × VCC 0 1: Do not set. 1 0: 0.70 × VCC 1 1: Do not set.	RW
VLT11			RW
VLT12	P5 input level select bit	b3 b2 0 0: 0.50 × VCC 0 1: Do not set. 1 0: 0.70 × VCC 1 1: Do not set.	RW
VLT13			RW
VLT14	P6 input level select bit	b5 b4 0 0: 0.50 × VCC 0 1: Do not set. 1 0: 0.70 × VCC 1 1: Do not set.	RW
VLT15			RW
VLT16	P7 input level select bit	b7 b6 0 0: 0.50 × VCC 0 1: Do not set. 1 0: 0.70 × VCC 1 1: Do not set.	RW
VLT17			RW

The input level of ports can be selected. The input level of peripheral functions is not affected.

11.3.9 Input Threshold Select Register 2 (VLT2)

Input Threshold Select Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	Reset Value
VLT2	036Eh	XX00 0000b

Bit Symbol	Bit Name	Function	RW
VLT20	P8 input level select bit	b1 b0 0 0: 0.50 × VCC 0 1: Do not set. 1 0: 0.70 × VCC 1 1: Do not set.	RW
VLT21			RW
VLT22	P9 input level select bit	b3 b2 0 0: 0.50 × VCC 0 1: Do not set. 1 0: 0.70 × VCC 1 1: Do not set.	RW
VLT23			RW
VLT24	P10 input level select bit	b5 b4 0 0: 0.50 × VCC 0 1: Do not set. 1 0: 0.70 × VCC 1 1: Do not set.	RW
VLT25			RW
— (b7-b6)	No register bits. If necessary, set to 0. The read value is undefined.		—

The input level of ports can be selected. The input level of peripheral functions is not affected.

11.3.10 Pin Assignment Control Register (PACR)

Pin Assignment Control Register

b7 b6 b5 b4 b3 b2 b1 b0	Symbol	Address	Reset Value
	PACR	0370h	0XXXX000b

Bit Symbol	Bit Name	Function	RW
PACR0	Pin enable bit	b2 b1 b0 0 1 0: 64-pin version 0 1 1: 80-pin version 1 0 0: 100-pin version Only set the values listed above.	RW
PACR1			RW
PACR2			RW
— (b6-b3)	No register bits. If necessary, set to 0. The read value is undefined.		—
U1MAP	UART1 pin remapping bit	UART1 pin assigned to: 0: P6_7 to P6_4 1: P7_3 to P7_0	RW

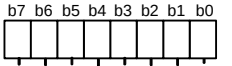
Write to the PACR register in the next instruction after setting the PRC2 bit in the PRCR register to 1 (write enabled).

PACR2 to PACR0 (Pin Enable Bit) (b2 to b0)

Bits PACR2 to PACR0 are 000b after reset. Select either 010b (64-pin package), 011b (80-pin package) or 100b (100-pin package) depending on a product.
Set bits PACR2 to PACR0 before inputting or outputting to each pin. When their value does not change after reset, I/O function of some the pins is disabled.

11.3.11 Port Pi Register (Pi) (i = 0 to 10)

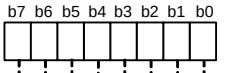
Port Pi Register (i = 0 to 8, 10)



Symbol	Address	Reset Value
P0 to P3	03E0h, 03E1h, 03E4h, 03E5h	XXh
P4	03E8h	XXh
P5	03E9h	XXh
P6 to P7	03ECh, 03EDh	XXh
P8	03F0h	XXh
P10	03F4h	XXh

Bit Symbol	Bit Name	Function	RW
Pi_0	Port Pi_0 bit	The pin level of any I/O port which is set to input mode can be read by reading the corresponding bit in this register. The pin level of any I/O port which is set to output mode can be controlled by writing to the corresponding bit in this register. 0 : Low level 1 : High level	RW
Pi_1	Port Pi_1 bit		RW
Pi_2	Port Pi_2 bit		RW
Pi_3	Port Pi_3 bit		RW
Pi_4	Port Pi_4 bit		RW
Pi_5	Port Pi_5 bit		RW
Pi_6	Port Pi_6 bit		RW
Pi_7	Port Pi_7 bit		RW

Port P9 Register



Symbol	Address	Reset Value
P9	03F1h	XXh

Bit Symbol	Bit Name	Function	RW
P9_0	Port P9_0 bit	The pin level of any I/O port which is set to input mode can be read by reading the corresponding bit in this register. The pin level of any I/O port which is set to output mode can be controlled by writing to the corresponding bit in this register 0 : Low level 1 : High level	RW
P9_1	Port P9_1 bit		RW
P9_2	Port P9_2 bit		RW
P9_3	Port P9_3 bit		RW
P9_4	Port P9_4 bit (1)		RW
P9_5	Port P9_5 bit		RW
P9_6	Port P9_6 bit		RW
P9_7	Port P9_7 bit		RW

Note:
1. No register bit for the 60 and 80 pin packages. If necessary, set to 0. The read value is undefined.

Data input/output to and from external devices are accomplished by reading and writing to the Pi register.

Each bit in the Pi register consists of a port latch to hold the output data and a circuit to read the pin status.

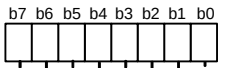
For ports set to input mode, the input level of the pin can be read by reading the corresponding Pi register, and data can be written to the port latch by writing to the Pi register.

For ports set to output mode, the port latch can be read by reading the corresponding Pi register, and data can be written to the port latch by writing to the Pi register. The data written to the port latch is output from the pin. Each bit in the Pi register corresponds to one port.

11.3.12 Port Pi Direction Register (PDi) (i = 0 to 10)

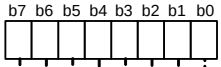
Port Pi Direction Register (i = 0 to 8, 10)

Symbol	Address	Reset Value
PD0 to PD3	03E2h, 03E3h, 03E6h, 03E7h	00h
PD4	03EAh	00h
PD5	03EBh	00h
PD6 to PD7	03EEh, 03EFh	00h
PD8	03F2h	00h
PD10	03F6h	00h



Bit Symbol	Bit Name	Function	RW
PDi_0	Port Pi_0 direction bit	0 : Input mode (functions as an input port) 1 : Output mode (functions as an output port)	RW
PDi_1	Port Pi_1 direction bit		RW
PDi_2	Port Pi_2 direction bit		RW
PDi_3	Port Pi_3 direction bit		RW
PDi_4	Port Pi_4 direction bit		RW
PDi_5	Port Pi_5 direction bit		RW
PDi_6	Port Pi_6 direction bit		RW
PDi_7	Port Pi_7 direction bit		RW

Port P9 Direction Register



Symbol	Address	Reset Value
PD9	03F3h	00h

Bit Symbol	Bit Name	Function	RW
PD9_0	Port P9_0 direction bit	0 : Input mode (functions as an input port) 1 : Output mode (functions as an output port)	RW
PD9_1	Port P9_1 direction bit		RW
PD9_2	Port P9_2 direction bit		RW
PD9_3	Port P9_3 direction bit		RW
PD9_4	Port P9_4 direction bit		RW
PD9_5	Port P9_5 direction bit		RW
PD9_6	Port P9_6 direction bit		RW
PD9_7	Port P9_7 direction bit		RW

Note:
1. No register bit for the 60 and 80 pin packages. If necessary, set to 0. The read value is undefined.

Write to the PD9 register in the next instruction after setting the PRC2 bit in the PRCR register to 1 (write enabled).

These registers select whether I/O ports are to be used for input or output. Each bit in the PDi register corresponds to one port.

To use I/O pins shared with the following peripheral functions, set the corresponding port direction bit to 0 (input mode):

11.4 Peripheral Function I/O

11.4.1 Peripheral Function I/O and Port Direction Bits

Programmable I/O ports can share pins with peripheral function I/O (see Table 1.11 to Table 1.16 Pin Names). Some peripheral function I/O are affected by a port direction bit which shares the same pin. Table 11.11 lists The Setting of Direction Bits Functioning as Peripheral Function I/O. For peripheral function settings, see descriptions of each function.

Table 11.11 The Setting of Direction Bits Functioning as Peripheral Function I/O

Peripheral Function I/O		The Setting of the Port Direction Bit Sharing the Same Pin
Input		Set to 0 (input mode).
Output	D/A Converter	Set to 0 (input mode).
	Others	Set to either 0 or 1 (outputs regardless of the direction bit setting).

11.4.2 Priority Level of Peripheral Function I/O

Multiple peripheral functions can share the same pin.
For example, when peripheral function A and peripheral function B share a pin, input and output are as follows:

- When the pin functions as input for peripheral functions A and B
  The same signal is input as an input signal for each function. However, the timing of accepting the signal differs depending on conditions (e.g. internal delay) of peripheral functions A and B.
- When the pin functions as output for peripheral function A and as input for peripheral function B
  Peripheral function A outputs a signal from the pin, and peripheral function B inputs the signal.

11.4.3 Digital Debounce Filters

The MCU has two digital debounce filters for noise reduction, assigned to $\overline{NMI}$/$\overline{SD}$ and $\overline{INT5}$/INPC1_7. Registers NDDR and P17DDR set the filter widths, respectively.

The digital debounce function is triggered by a rising or falling edge of digital input signal to either $\overline{NMI}$/$\overline{SD}$ and $\overline{INT5}$/INPC1_7. When the input pulse is longer than the filter width set by a program, the signal level is determined. Any noise that is shorter than the filter width is blocked by this function.

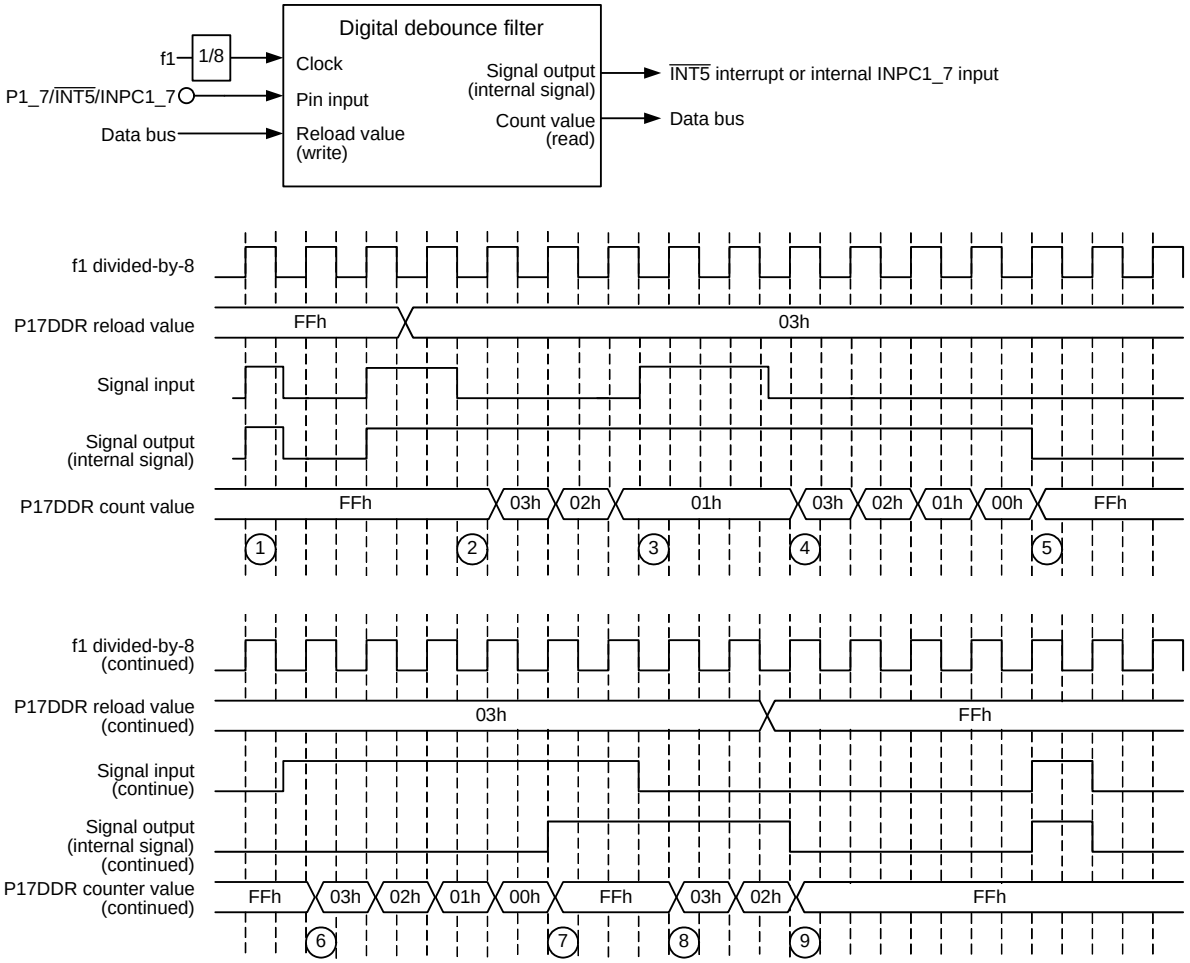
Digital debounce function is disabled to the port P1_7/IDU input and the port P8_5 input.

Filter width: $\frac{(n+1) \times 8}{f1}$ n: the NDDR or P17DDR register setting value

Registers NDDR and P17DDR decrement the setting value as f1 divided-by-8 is the count source. When reading the NDDR or P17DDR register, the count value is returned. The setting value is reloaded at every falling or rising edge of the pin input.

When using the digital debounce function, the programmable value for the NDDR or P17DDR register is 00h to FFh. When setting FFh to the register, digital debounce filter function is not selected. See Figure 11.9 for details.

Example of the P1_7/$\overline{INT5}$ digital debounce filter function, P17DDR = 03h



Notes:
1. After reset, the P17DDR register is FFh. Pin input signal will be output directly to $\overline{INT5}$ circuit as an internal signal.
2. Set the P17DDR register to 03h. When the pin input level and signal output (internal signal) level does not match, the P17DDR register starts decrementing as f1 divided-by-8 is the count source. The pin input level is low and the signal output level is high here.
3. When the pin input level and signal output level matches while counting, the P17DDR register counter stops. Both pin input and signal output levels are high here.
4. When the pin input level and signal output level does not match again, the P17DDR register counter starts decrementing after the setting value is reloaded. The pin input level is low and the signal output level is high here.
5. When the P17DDR register counter underflows, the counter stops and the pin input signal is output directly as an output signal. If the pin input level is high, a high signal is output. A low signal is output here.
6. The pin input level and signal output level does not match again, the P17DDR register counter starts decrementing after the setting value is reloaded. The pin input level is high and the signal output level is low here.
7. When the P17DDR register counter underflows, the counter stops and the pin input signal is output directly as an output signal. A high signal is output here.
8. The pin input level and signal output level does not match again, the P17DDR register counter starts decrementing after the setting value is reloaded. The pin input level is low and the signal output level is high here.
9. When setting the P17DDR register to FFh, the setting value is reloaded to the P17DDR reload register and the P17DDR counter stops counting. The pin input signal is output directly as an internal signal.

Figure 11.9 Digital Debounce Filter Operation

11.5 Unassigned Pin Handling

Table 11.12 Unassigned Pin Handling in Single-Chip Mode

Pin Name	Connection(2)
Ports P0 to P10	One of the following: • Set the pin to input mode and connect a pin to VSS via resistor (pull-down) • Set the pin to input mode and connect a pin to VCC via resistor (pull-up) • Set the pin to output mode and leave the pin open (1)
XOUT(3)	Open
XIN	Connect to VCC via a resistor (pull-up)
AVCC	Connect to VCC
AVSS, VREF	Connect to VSS
NC	Open, Connect to VCC, or Connect to VSS

Notes:
1. When setting a port to output mode and leaving it open, be aware that the port remains in input mode until it is switched to output mode by a program after reset. For this reason, the voltage level on the pin becomes indeterminate, causing the power supply current to increase while the port remains in input mode.
   Furthermore, since the values of the direction registers can be changed by noise or noise-induced loss of control, it is recommended that the contents of the direction registers be regularly reset in software to improve the program reliability.
2. Make sure unused pins are connected with the shortest possible wiring from the MCU pins (maximum 2 cm).
3. Leave the XOUT pin open when inputting an external clock to the XIN pin or when connecting VCC via a resistor.

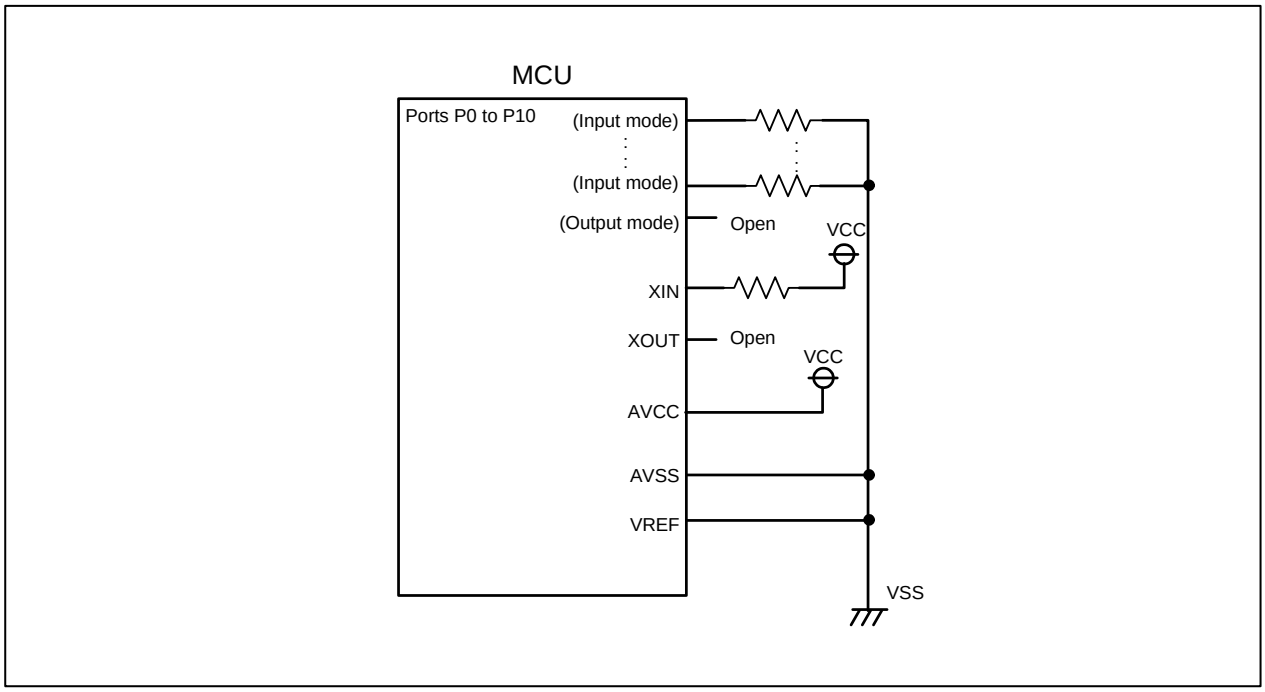


Figure 11.10 Unassigned Pin Handling

11.6 Notes on Programmable I/O Ports

11.6.1 Pin Assignment Control

Bits PACR2 to PACR0 in the PACR register are 000b after reset. Set 010b (64-pin package), 011b (80-pin package) or 100b (100-pin package) to select the pin package, depending on the product.
After setting bits PACR2 to PACR0, set the programmable I/O ports and I/O pins for peripherals.

11.6.2 Influence of $\overline{SD}$

When a low-level signal is applied to the $\overline{SD}$ pin while the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on $\overline{SD}$ pin enabled), the following pins become high-impedance: P7_2/CLK2/TA1OUT/V/RXD1, P7_3/$\overline{CTS2}$/$\overline{RTS2}$/TA1IN/$\overline{V}$/TXD1, P7_4/TA2OUT/W/LIN0OUT, P7_5/TA2IN/$\overline{W}$/LIN0IN, P8_0/TA4OUT/U/TSUDA, P8_1/TA4IN/$\overline{U}$/TSUDB

11.6.3 Input Voltage Threshold

The input threshold voltage differs in the programmable I/O port and peripherals. When the programmable I/O port and peripheral is sharing the same pin, and the pin input level is lower than VIH and higher than VIL (input voltage is neither high or low), the input signal voltage level may be determined differently between the programmable I/O port and peripheral because the input voltage thresholds for those two are not necessarily the same.

12. Interrupts

12.1 Introduction

Table 12.1 lists Types of Interrupts, and Table 12.2 lists I/O Pins. The pins shown in Table 12.2 are external interrupt input pins. Refer to the peripheral functions for the pins related to the peripheral functions.

Table 12.1 Types of Interrupts

Type		Interrupt	Function
Software		Undefined instruction (UND instruction) Overflow (INTO instruction) BRK instruction INT instruction	An interrupt is generated by executing an instruction. Non-maskable interrupt (2)
Hardware	Specific	$\overline{\text{NMI}}$ Watchdog timer Oscillator stop/restart detect Voltage monitor 2 Address match Single step (1) $\overline{\text{DBC}}$ (1)	Interrupt by the MCU hardware Non-maskable interrupt (2)
	Peripheral function	$\overline{\text{INT}}$, timers, etc. (Refer to 12.6.2 “Relocatable Vector Tables”.)	Interrupt by the peripheral functions in the MCU Maskable interrupt (interrupt priority level: 7 levels) (2)

Notes:
1. This interrupt is provided exclusively for developers and should not be used.
2. Maskable interrupt: Interrupt status (enabled or disabled) can be selected by the interrupt enable flag (I flag).
   Interrupt priority can be changed by the interrupt priority level.
   Non-maskable interrupt: Interrupt status (enabled or disabled) cannot be selected by the interrupt enable flag (I flag).
   Interrupt priority cannot be changed by the interrupt priority level.

Table 12.2 I/O Pins

Pin Name	I/O	Function
$\overline{\text{NMI}}$	Input (1)	$\overline{\text{NMI}}$ interrupt input
$\overline{\text{INTi}}$	Input (1)	$\overline{\text{INTi}}$ interrupt input
$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	Input (1)	Key input

i = 0 to 7

Note:
1. Set the port direction bits which share pins to 0 (input mode).

12.2 Registers

Table 12.3 Registers (1/2)

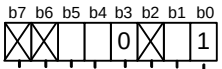
Address	Register	Symbol	Reset Value
001Eh	Processor Mode Register 2	PM2	XX00 0X01b
0041h	E^2dataFlash Interrupt Control Register	E2FIC	XXXX X000b
0042h	$\overline{INT7}$ Interrupt Control Register, Serial Bus Interface 0 Interrupt Control Register	INT7IC, SS0IC	XX00 X000b
0043h	$\overline{INT6}$ Interrupt Control Register, LIN0 Interrupt Control Register	INT6IC, LIN0IC	XX00 X000b
0044h	$\overline{INT3}$ Interrupt Control Register	INT3IC	XX00 X000b
0045h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
0046h	Timer B4 Interrupt Control Register	TB4IC	XXXX X000b
0047h	Timer B3 Interrupt Control Register	TB3IC	XXXX X000b
0048h	$\overline{INT5}$ Interrupt Control Register	INT5IC	XX00 X000b
0049h	$\overline{INT4}$ Interrupt Control Register	INT4IC	XX00 X000b
004Ah	UART2 Bus Collision Detection Interrupt Control Register, Task Monitoring Timer Interrupt Control Register	BCNIC, TMOSIC	XXXX X000b
004Bh	DMA0 Interrupt Control Register	DM0IC	XXXX X000b
004Ch	DMA1 Interrupt Control Register	DM1IC	XXXX X000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXX X000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXX X000b
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXX X000b
0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXX X000b
0051h	UART0 Transmit Interrupt Control Register, LIN0 Low Detection Interrupt Control Register	S0TIC, L0WIC	XXXX X000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXX X000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXX X000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXX X000b
0055h	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
0058h	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
0059h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
005Ah	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
005Bh	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
005Dh	$\overline{INT0}$ Interrupt Control Register	INT0IC	XX00 X000b
005Eh	$\overline{INT1}$ Interrupt Control Register	INT1IC	XX00 X000b
005Fh	$\overline{INT2}$ Interrupt Control Register	INT2IC	XX00 X000b
0069h	DMA2 Interrupt Control Register	DM2IC	XXXX X000b
006Ah	DMA3 Interrupt Control Register	DM3IC	XXXX X000b
006Bh	CAN 1 Reception Complete Interrupt Control Register	C1RIC	XXXX X000b
006Ch	CAN 1 Transmission Complete Interrupt Control Register	C1TIC	XXXX X000b
006Dh	CAN 1 Receive FIFO Interrupt Control Register	C1FRIC	XXXX X000b
006Eh	CAN 1 Transmit FIFO Interrupt Control Register	C1FTIC	XXXX X000b

Table 12.4 Registers (2/2)

Address	Register	Symbol	Reset Value
006Fh	UART4 Transmit Interrupt Control Register, Real-Time Clock Compare Interrupt Control Register	S4TIC, RTCCIC	XXXX X000b
0070h	UART4 Receive Interrupt Control Register	S4RIC	XXXX X000b
0071h	CAN0 Wake-up Interrupt Control Register	C0WIC	XXXX X000b
0072h	UART3 Transmit Interrupt Control Register,CAN0 Error Interrupt Control Register	S3TIC, C0EIC	XXXX X000b
0073h	UART3 Receive Interrupt Control Register, CAN 1 Wake-up Interrupt Control Register	S3RIC, C1WIC	XXXX X000b
0074h	Real-Time Clock Cycle Interrupt Control Register, CAN 1 Error Interrupt Control Register	RTCTIC, C1EIC	XXXX X000b
0075h	CAN0 Reception Complete Interrupt Control Register	C0RIC	XXXX X000b
0076h	CAN0 Transmission Complete Interrupt Control Register	C0TIC	XXXX X000b
0077h	CAN0 Receive FIFO Interrupt Control Register	C0FRIC	XXXX X000b
0078h	CAN0 Transmit FIFO Interrupt Control Register	C0FTIC	XXXX X000b
0079h	IC/OC Interrupt 0 Control Register	ICOC0IC	XXXX X000b
007Ah	IC/OC Channel 0 Interrupt Control Register	ICOCH0IC	XXXX X000b
007Bh	IC/OC Interrupt 1 Control Register I2C-bus Interface Interrupt Control Register	ICOC1IC IICIC	XXXX X000b
007Ch	IC/OC Channel 1 Interrupt Control Register SCL/SDA Interrupt Control Register	ICOCH1IC SCLDAIC	XXXX X000b
007Dh	IC/OC Channel 2 Interrupt Control Register	ICOCH2IC	XXXX X000b
007Eh	IC/OC Channel 3 Interrupt Control Register	ICOCH3IC	XXXX X000b
007Fh	IC/OC Base Timer Interrupt Control Register	BTIC	XXXX X000b
0204h	Interrupt Source Select Register 4	IFSR4A	00h
0205h	Interrupt Source Select Register 3	IFSR3A	00h
0206h	Interrupt Source Select Register 2	IFSR2A	00h
0207h	Interrupt Source Select Register	IFSR	00h
020Eh	Address Match Interrupt Enable Register	AIER	XXXX XX00b
020Fh	Address Match Interrupt Enable Register 2	AIER2	XXXX XX00b
0210h	Address Match Interrupt Register 0	RMAD0	00h
0211h			00h
0212h			X0h
0214h	Address Match Interrupt Register 1	RMAD1	00h
0215h			00h
0216h			X0h
0218h	Address Match Interrupt Register 2	RMAD2	00h
0219h			00h
021Ah			X0h
021Ch	Address Match Interrupt Register 3	RMAD3	00h
021Dh			00h
021Eh			X0h
02FEh	$\overline{\text{NMI}}$ Digital Debounce Register	NDDR	FFh
02FFh	P1_7 Digital Debounce Register	P17DDR	FFh

12.2.1 Processor Mode Register 2 (PM2)

Processor Mode Register 2



Symbol: PM2 | Address: 001Eh | Reset Value: XX00 0X01b

Bit Symbol	Bit Name	Function	RW
— (b0)	Reserved bit	Set to 1.	RW
PM21	System clock protection bit	0 : Clock is protected by PRCR register 1 : Clock change disabled	RW
— (b2)	No register bit. If necessary, set to 0. The read value is undefined.		—
— (b3)	Reserved bit	Set to 0	RW
PM24	$\overline{\text{NMI}}$ interrupt enable bit	0 : $\overline{\text{NMI}}$ interrupt disabled 1 : $\overline{\text{NMI}}$ interrupt enabled	RW
PM25	Peripheral clock fC provide bit	0 : Not provided 1 : Provided	RW
— (b7-b6)	No register bits. If necessary, set to 0. The read value is undefined.		—

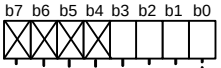
Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting this register.

PM24 ($\overline{\text{NMI}}$ interrupt enable bit) (b4)

Once this bit is set to 1, it cannot be set to 0 by a program (writing 0 has no effect).

12.2.2 Interrupt Control Register 1 (E2FIC, BCNIC/TMOSIC, DM0IC to DM3IC, KUPIC,ADIC, S0TIC/L0WIC, S1TIC, S2TIC, S0RIC to S2RIC, S3RIC/C1WIC, TA0IC to TA4IC, TB0IC to TB5IC, S4TIC/RTCCIC, S4RIC, C0WIC,S3TIC/C0EIC, RTCTIC/C1EIC, C0RIC, C1RIC, C0TIC, C1TIC, C0FRIC, C1FRIC, C0FTIC, C1FTIC, ICOC0IC, ICOCH0IC, ICOC1IC/IICIC, ICOCH1IC/SCLDAIC, ICOCH2IC to ICOCH3IC, BTIC)

Interrupt Control Register 1



Symbol	Address	Reset Value
Refer to the table below for symbols and addresses.		XXXX X000b

Bit Symbol	Bit Name	Function	RW
ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0 : Level 0 (interrupt disabled) 0 0 1 : Level 1 0 1 0 : Level 2 0 1 1 : Level 3 1 0 0 : Level 4 1 0 1 : Level 5 1 1 0 : Level 6 1 1 1 : Level 7	RW
ILVL1			RW
ILVL2			RW
IR	Interrupt request bit	0: Interrupt not requested 1: Interrupt requested	RW
— (b7-b4)	No register bits. If necessary, set to 0. The read value is undefined.		—

Symbol	Address
E2FIC	0041h
BCNIC/TMOSIC	004Ah
DM0IC	004Bh
DM1IC	004Ch
DM2IC	0069h
DM3IC	006Ah
KUPIC	004Dh
ADIC	004Eh
S0TIC/L0WIC	0051h
S1TIC	0053h
S2TIC	004Fh
S0RIC	0052h
S1RIC	0054h
S2RIC	0050h
S3RIC/C1WIC	0073h

Symbol	Address
TA0IC	0055h
TA1IC	0056h
TA2IC	0057h
TA3IC	0058h
TA4IC	0059h
TB0IC	005Ah
TB1IC	005Bh
TB2IC	005Ch
TB3IC	0047h
TB4IC	0046h
TB5IC	0045h
S4TIC/RTCCIC	006Fh
S4RIC	0070h
C0WIC	0071h
S3TIC/C0EIC	0072h

Symbol	Address
RTCTIC/C1EIC	0074h
C0RIC	0075h
C1RIC	006Bh
C0TIC	0076h
C1TIC	006Ch
C0FRIC	0077h
C1FRIC	006Dh
C0FTIC	0078h
C1FTIC	006Eh
ICOC0IC	0079h
ICOCH0IC	007Ah
ICOC1IC/IICIC	007Bh
ICOCH1IC/SCLDAIC	007Ch
ICOCH2IC	007Dh
ICOCH3IC	007Eh
BTIC	007Fh

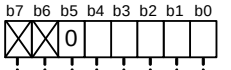
Rewrite these registers at a point where an interrupt request for the corresponding register is not generated.
When multiple interrupt sources share the register, select an interrupt source in registers IFSR2A, IFSR3A or IFSR4A.

IR (Interrupt request bit) (b3)

Do not set the IR bit to 1 when it is 0.

12.2.3 Interrupt Control Register 2 (INT7IC/SS0IC, INT6IC/LIN0IC, INT3IC, INT5IC, INT4IC, INT0IC to INT2IC)

Interrupt Control Register 2



Symbol Address Reset Value

Refer to the table below for symbols and addresses. XX00 X000b

Bit Symbol	Bit Name	Function	RW
ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0 : Level 0 (interrupt disabled) 0 0 1 : Level 1 0 1 0 : Level 2 0 1 1 : Level 3 1 0 0 : Level 4 1 0 1 : Level 5 1 1 0 : Level 6 1 1 1 : Level 7	RW
ILVL1			RW
ILVL2			RW
IR	Interrupt request bit	0: Interrupt not requested 1: Interrupt requested	RW
POL	Polarity select bit	0 : Select falling edge 1 : Select rising edge	RW
— (b5)	Reserved bit	Set to 0	RW
— (b7-b6)	No register bits. If necessary, set to 0. The read value is undefined.		—

Symbol	Address
INT7IC/SS0IC	0042h
INT6IC/LIN0IC	0043h
INT3IC	0044h
INT5IC	0048h
INT4IC	0049h

Symbol	Address
INT0IC	005Dh
INT1IC	005Eh
INT2IC	005Fh

Rewrite these registers at a point where an interrupt request for the corresponding register is not generated.
When multiple interrupt sources share the register, select an interrupt source in the IFSR4 register.

IR (Interrupt request bit) (b3)

Do not set the IR bit to 1 when it is 0.
When the IFSR44 bit in the IFSR4A register is 1 (SS0), the IR bit in the SS0IC register becomes RO. The IR bit does not become 0 even if set to 0.
When the IFSR45 bit in the IFSR4A register is 1 (LIN0), the IR bit in the LIN0IC register becomes RO. The IR bit does not become 0 even if set to 0.

As with other maskable interrupts, the serial bus interface interrupt and a LIN module interrupt are controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, since each interrupt source is generated by a combination of multiple interrupt request sources, the following differences from other maskable interrupts apply:

- When a bit in the status register is 1 and its corresponding bit in the enable register is also 1 (interrupt enabled), the IR bit in the interrupt control register becomes 1 (interrupt requested).

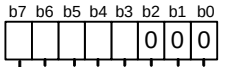
- When either a bit in the status register or its corresponding bit in the enable register becomes 0, or bits in both registers become 0, the IR bit becomes 0 (no interrupt requested). That is, while the IR bit is 1, interrupt requests are not retained even if an interrupt is not accepted. The IR bit does not become 0 even if written to 0.
- Bits in the status register does not become 0 automatically even if an interrupt is accepted. Therefore the IR bit does not become 0 automatically when an interrupt is accepted. Set each bit in the status register to 0 in the interrupt routine. Refer to the status register figure for how to set bits in the status register to 0.
- When setting multiple bits in the enable register to 1, after the IR bit becomes 1 and another request source is confirmed, the IR bit does not change. When setting multiple bits in the enable register to 1, use the status register to determine which request source causes an interrupt.

POL (Polarity select bit) (b4)

When the IFSRi bit in the IFSR register is 1 (both edges), set the POL bit in the INTiIC register to 0 (falling edge) (i = 0 to 5). When bits IFSR30 and IFSR31 in the IFSR3A register are 1 (both edges), set the POL bit in registers INT6IC and INT7IC to 0 (falling edge).
When the IFSR44 bit in the IFSR4A register is 1 (SS0), set the POL bit in the SS0IC register to 0.
When the IFSR45 bit in the IFSR4A register is 1 (LIN0), set the POL bit in the LIN0IC register to 0.

12.2.4 Interrupt Source Select Register 4 (IFSR4A)

Interrupt Source Select Register 4



Symbol	Address	Reset Value
IFSR4A	0204h	00h

Bit Symbol	Bit Name	Function	RW
— (b2-b0)	Reserved bit	Set to 0.	RW
IFSR43	Interrupt source select bit	0: UART0 transmission 1: LIN0 Low Detection	RW
IFSR44	Interrupt source select bit	0: $\overline{\text{INT7}}$ 1: SS0	RW
IFSR45	Interrupt source select bit	0: $\overline{\text{INT6}}$ 1: LIN0	RW
IFSR46	Interrupt source select bit	0: CAN1 receive FIFO interrupt not used 1: CAN1 receive FIFO	RW
IFSR47	Interrupt source select bit	0: Real-time clock cycle 1: CAN1 error	RW

12.2.5 Interrupt Source Select Register 3 (IFSR3A)

Interrupt Source Select Register 3

b7	b6	b5	b4	b3	b2	b1	b0
0							

Symbol	Address	Reset Value
IFSR3A	0205h	00h

Bit Symbol	Bit Name	Function	RW
IFSR30	$\overline{\text{INT6}}$ interrupt priority select bit	0: One edge 1: Both edges	RW
IFSR31	$\overline{\text{INT7}}$ interrupt priority select bit	0: One edge 1: Both edges	RW
IFSR32	Interrupt source select bit	0: UART3 receive 1: CAN1 wake-up	RW
IFSR33	Interrupt source select bit	0: CAN1 Reception Complete interrupt not used 1: CAN1 Reception Complete	RW
IFSR34	Interrupt source select bit	0: CAN1 Transmission Complete interrupt not used 1: CAN1 Transmission Complete	RW
IFSR35	Interrupt source select bit	0: CAN1 transmit FIFO interrupt not used 1: CAN1 transmit FIFO	RW
IFSR36	Interrupt source select bit	0: UART4 transmit 1: Real-time clock compare	RW
— (b7)	Reserved bit	Set to 0.	RW

IFSR31 and IFSR30 ($\overline{\text{INT7}}$ and $\overline{\text{INT6}}$ interrupt polarity select bit) (b1-b0)

When setting this bit to 1 (both edges), make sure the corresponding POL bit in registers INT6IC and INT7IC is set to 0 (falling edge).

12.2.6 Interrupt Source Select Register 2 (IFSR2A)

Interrupt Source Select Register 2

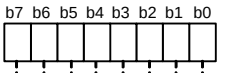
b7	b6	b5	b4	b3	b2	b1	b0
0	0					0	

Symbol	Address	Reset Value
IFSR2A	0206h	00h

Bit Symbol	Bit Name	Function	RW
IFSR20	Interrupt source select bit	0: UART2 bus collision detection 1: Task monitor timer	RW
— (b1)	Reserved bit	Set to 0.	RW
IFSR22	Interrupt source select bit	0: IC/OC interrupt 1 1: I^2C-bus interface	RW
IFSR23	Interrupt source select bit	0: IC/OC channel 1 interrupt 1: SCL/SDA	RW
IFSR24	Interrupt source select bit	0: CAN0 wake-up interrupt not used 1: CAN0 wake-up	RW
IFSR25	Interrupt source select bit	0: UART3 transmission 1: CAN0 error	RW
— (b7-b6)	Reserved bits	Set to 0.	RW

12.2.7 Interrupt Source Select Register (IFSR)

Interrupt Source Select Register



Symbol	Address	Reset Value
IFSR	0207h	00h

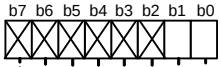
Bit Symbol	Bit Name	Function	RW
IFSR0	$\overline{INT0}$ interrupt polarity select bit	0 : One edge 1 : Both edges	RW
IFSR1	$\overline{INT1}$ interrupt polarity select bit	0 : One edge 1 : Both edges	RW
IFSR2	$\overline{INT2}$ interrupt polarity select bit	0 : One edge 1 : Both edges	RW
IFSR3	$\overline{INT3}$ interrupt polarity select bit	0 : One edge 1 : Both edges	RW
IFSR4	$\overline{INT4}$ interrupt polarity select bit	0 : One edge 1 : Both edges	RW
IFSR5	$\overline{INT5}$ interrupt polarity select bit	0 : One edge 1 : Both edges	RW
IFSR6	Interrupt request source select bit	0 : $\overline{INT4}$ interrupt not used 1 : $\overline{INT4}$	RW
IFSR7	Interrupt request source select bit	0 : $\overline{INT5}$ interrupt not used 1 : $\overline{INT5}$	RW

IFSR5-IFSR0 ($\overline{INT5}$-$\overline{INT0}$ interrupt polarity select bit) (b5-b0)

When setting these bits to 1 (both edges), make sure the corresponding POL bit in registers INT0IC to INT5IC is set to 0 (falling edge).

12.2.8 Address Match Interrupt Enable Register (AIER)

Address Match Interrupt Enable Register

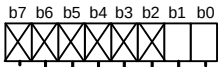


Symbol	Address	Reset Value
AIER	020Eh	XXXX XX00b

Bit Symbol	Bit Name	Function	RW
AIER0	Address match interrupt 0 enable bit	0 : Interrupt disabled 1 : Interrupt enabled	RW
AIER1	Address match interrupt 1 enable bit	0 : Interrupt disabled 1 : Interrupt enabled	RW
— (b7-b2)	No register bits. If necessary, set to 0. The read value is undefined.		—

12.2.9 Address Match Interrupt Enable Register 2 (AIER2)

Address Match Interrupt Enable Register 2

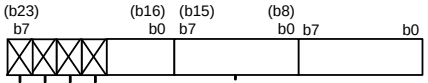


Symbol	Address	Reset Value
AIER2	020Fh	XXXX XX00b

Bit Symbol	Bit Name	Function	RW
AIER20	Address match interrupt 2 enable bit	0 : Interrupt disabled 1 : Interrupt enabled	RW
AIER21	Address match interrupt 3 enable bit	0 : Interrupt disabled 1 : Interrupt enabled	RW
— (b7-b2)	No register bits. If necessary, set to 0. The read value is undefined.		—

12.2.10 Address Match Interrupt Register i (RMADi) (i = 0 to 3)

Address Match Interrupt Register i (i = 0 to 3)



Symbol	Address	Reset Value
RMAD0	0212h to 0210h	X0 0000h
RMAD1	0216h to 0214h	X0 0000h
RMAD2	021Ah to 0218h	X0 0000h
RMAD3	021Eh to 021Ch	X0 0000h

Function	Setting Range	RW
Address setting register for address match interrupt (b19 to b0)	00000h to FFFFFh	RW
No register bits. If necessary, set to 0. The read value is undefined.		—

12.2.11 $\overline{\text{NMI}}$ Digital Debounce Register (NDDR)

$\overline{\text{NMI}}$ Digital Debounce Register

b7 ... b0	Symbol	Address	Reset Value
	NDDR	02FEh	FFh

Function	Setting Range	RW
With n being the setting value: • n = 00h to FEh: A signal with larger pulse width than $\frac{(n + 1) \times 8}{f1}$ is input to $\overline{\text{NMI}}/\overline{\text{SD}}$. • n = FFh: Digital debounce filter function is disabled and all signals will be input directly.	00h to FFh	RW

When using the $\overline{\text{NMI}}$ interrupt to exit from stop mode, set FFh to the NDDR register before entering stop mode. Write to the NDDR register in the next instruction after setting the PRC2 bit in the PRCR register to 1 (write enabled). No interrupt or DMA transfer should be generated between these two instructions.

12.2.12 P1_7 Digital Debounce Register (P17DDR)

P1_7 Digital Debounce Register

b7 ... b0	Symbol	Address	Reset Value
	P17DDR	02FFh	FFh

Function	Setting Range	RW
With n being the setting value: • n = 00h to FEh: A signal with larger pulse width than $\frac{(n + 1) \times 8}{f1}$ is input to INPC1_7/$\overline{\text{INT5}}$. • n = FFh: Digital debounce filter function is disabled and all signals will be input directly.	00h to FFh	RW

When using the $\overline{\text{INT5}}$ interrupt to exit from stop mode, set FFh to the P17DDR register before entering stop mode.

12.3 Types of Interrupts

Figure 12.1 shows Types of Interrupts.

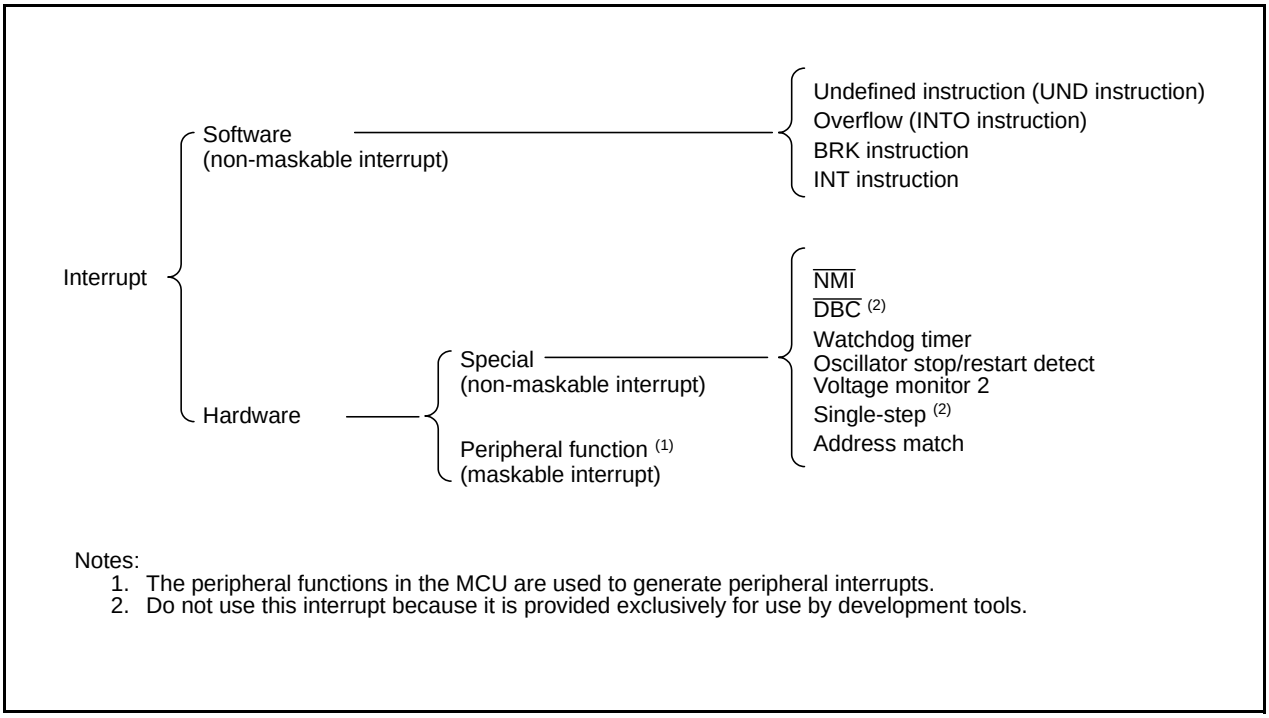


Figure 12.1 Types of Interrupts

- Maskable interrupt : The I flag (interrupt enable flag) **can** enable/disable these interrupts. The interrupt priority order **can be changed** by using the interrupt priority level.
- Non-maskable interrupt : The I flag (interrupt enable flag) **cannot** enable/disable these interrupts. The interrupt priority order **cannot be changed** by using the interrupt priority level.

12.4 Software Interrupts

A software interrupt occurs when executing instructions. Software interrupts are non-maskable interrupts.

12.4.1 Undefined Instruction Interrupt

An undefined instruction interrupt occurs when executing the UND instruction.

12.4.2 Overflow Interrupt

An overflow interrupt occurs when executing the INTO instruction with the O flag in the FLG register set to 1 (the operation resulted in an overflow). The following are instructions whose O flag changes by an arithmetic operation:
ABS, ADC, ADCF, ADD, CMP, DIV, DIVU, DIVX, NEG, RMPA, SBB, SHA, and SUB

12.4.3 BRK Interrupt

A BRK interrupt occurs when the BRK instruction is executed.

12.4.4 INT Instruction Interrupt

An INT instruction interrupt occurs when the INT instruction is executed. Software interrupt numbers 0 to 63 can be specified for the INT instruction. Because software interrupt numbers 0 to 31, 41 to 63 are assigned to peripheral function interrupts, the same interrupt routine used for peripheral function interrupts can be executed by executing the INT instruction.
For software interrupt numbers 0 to 31, the U flag is saved on the stack during instruction execution and is cleared to 0 (ISP selected) before executing an interrupt sequence. The U flag is restored from the stack when returning from the interrupt routine. For software interrupt numbers 32 to 63, the U flag does not change state during instruction execution, and the SP selected at the time is used.

12.5 Hardware Interrupts

Hardware interrupts are classified into two types: special interrupts and peripheral function interrupts.

12.5.1 Special Interrupts

Special interrupts are non-maskable interrupts.

12.5.1.1 $\overline{\text{NMI}}$ Interrupt

An $\overline{\text{NMI}}$ interrupt is generated when input on the $\overline{\text{NMI}}$ pin changes state from high to low. For details on the $\overline{\text{NMI}}$ interrupt, refer to 12.9 “$\overline{\text{NMI}}$ Interrupt”.

12.5.1.2 $\overline{\text{DBC}}$ Interrupt

Do not use this interrupt because it is provided exclusively for use by development tools.

12.5.1.3 Watchdog Timer Interrupt

This interrupt is generated by the watchdog timer. Once a watchdog timer interrupt is generated, be sure to refresh the watchdog timer. For details on the watchdog timer, refer to 13. “Watchdog Timer”.

12.5.1.4 Oscillator Stop/Restart Detect Interrupt

The interrupt is generated by the oscillator stop/restart detect function. For details on this function, refer to 8. “Clock Generator”.

12.5.1.5 Voltage Monitor 2 Interrupt

The interrupt is generated by the voltage detector. For details on the voltage detector, refer to 7. “Voltage Detector”.

12.5.1.6 Single-Step Interrupt

Do not use this interrupt because it is provided exclusively for use by development tools.

12.5.1.7 Address Match Interrupt

When the AIER0 or AIER1 bit in the AIER register, or the AIER20 or AIER21 bit in the AIER2 register is 1 (address match interrupt enabled), an address match interrupt is generated immediately before executing an instruction at the address indicated by the corresponding registers RMAD0 to RMAD3. For details on the address match interrupt, refer to 12.11 “Address Match Interrupt”.

12.5.2 Peripheral Function Interrupts

A peripheral function interrupt occurs when a request from a peripheral function in the MCU is acknowledged. Peripheral function interrupts are maskable interrupts. See Table 12.6 and Table 12.7 “Relocatable Vector Tables”. Refer to the descriptions of each function for details on how the corresponding peripheral function interrupt is generated.

12.6 Interrupts and Interrupt Vectors

One interrupt vector consists of 4 bytes. Set the start address of each interrupt routine in the respective interrupt vectors. When an interrupt request is accepted, the CPU branches to the address set in the corresponding interrupt vector. Figure 12.2 shows an Interrupt Vector.

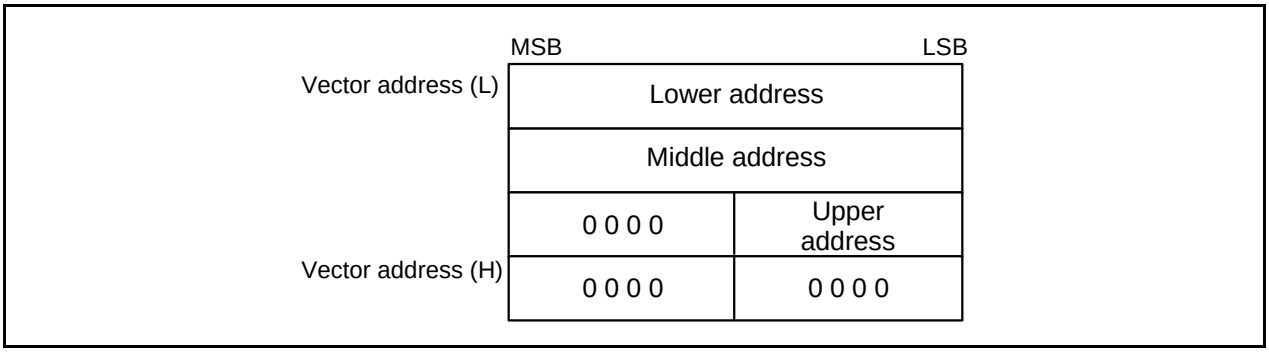


Figure 12.2 Interrupt Vector

12.6.1 Fixed Vector Tables

The fixed vector tables are allocated to addresses from FFFDCh to FFFFFh. Table 12.5 lists the Fixed Vector Tables. In the flash memory MCU version, the vector addresses (H) of fixed vectors are used for the ID code check function and OFS1 address. For details, refer to 29. “Flash Memory”.

Table 12.5 Fixed Vector Tables

Interrupt Source	Vector Table Addresses Address (L) to Address (H)	Reference
Undefined instruction (UND instruction)	FFFDCh to FFFDFh	M16C/60, M16C/20, M16C/Tiny Series Software Manual
Overflow (INTO instruction)	FFFE0h to FFFE3h	
BRK instruction (2)	FFFE4h to FFFE7h	
Address match	FFFE8h to FFFEBh	12.11 “Address Match Interrupt”
Single-step (1)	FFFECh to FFFEFh	-
Watchdog timer, oscillator stop/restart detect, voltage monitor 2	FFFF0h to FFFF3h	13. “Watchdog Timer” 8. “Clock Generator” 7. “Voltage Detector”
$\overline{\text{DBC}}$ (1)	FFFF4h to FFFF7h	-
$\overline{\text{NMI}}$	FFFF8h to FFFFBh	12.9 “$\overline{\text{NMI}}$ Interrupt”
Reset	FFFFCh to FFFFFh	6. “Resets”

Notes:
1. Do not use this interrupt because it is provided exclusively for use by development tools.
2. If the value of address FFFE6h is FFh, program execution starts from the address shown by the vector in the relocatable vector table.

12.6.2 Relocatable Vector Tables

The 256 bytes beginning with the start address set in the INTB register compose a relocatable vector table area. Setting an even address in the INTB register results in the interrupt sequence being executed faster than setting an odd address.

Table 12.6 Relocatable Vector Tables (1/2)

Interrupt Source	Vector Address (1) Address (L) to Address (H)	Software Interrupt Number	Reference
INT instruction interrupt (5)	+0 to +3 (0000h to 0003h) to +252 to +255 (00FCh to 00FFh)	0 to 63	M16C/60, M16C/20, M16C/Tiny Series Software Manual
BRK instruction (5)	+0 to +3 (0000h to 0003h)	0	
E2 Data Flash	+4 to +7 (0004h to 0007h)	1	30. "E2PROM Emulation Data Flash"
$\overline{\text{INT7}}$, SS0 (8)	+8 to +11 (0008h to 000Bh)	2	12.8 "$\overline{\text{INT}}$ Interrupt" 23. "Serial Bus Interface"
$\overline{\text{INT6}}$, LIN0 (9)	+12 to +15 (000Ch to 000Fh)	3	12.8 "$\overline{\text{INT}}$ Interrupt" 24. "LIN Module"
$\overline{\text{INT3}}$	+16 to +19 (0010h to 0013h)	4	12.8 "$\overline{\text{INT}}$ Interrupt"
Timer B5	+20 to +23 (0014h to 0017h)	5	16. "Timer B"
Timer B4	+24 to +27 (0018h to 001Bh)	6	
Timer B3	+28 to +31 (001Ch to 001Fh)	7	
$\overline{\text{INT5}}$ (2)	+32 to +35 (0020h to 0023h)	8	12.8 "$\overline{\text{INT}}$ Interrupt"
$\overline{\text{INT4}}$ (3)	+36 to +39 (0024h to 0027h)	9	
UART2 bus collision detection (6), task monitor timer (7)	+40 to +43 (0028h to 002Bh)	10	21. "Serial Interface UARTi (i = 0 to 4)" 19. "Task Monitor Timer"
DMA0	+44 to +47 (002Ch to 002Fh)	11	14. "DMAC"
DMA1	+48 to +51 (0030h to 0033h)	12	
Key input interrupt	+52 to +55 (0034h to 0037h)	13	12.10 "Key Input Interrupt"
A/D converter	+56 to +59 (0038h to 003Bh)	14	26. "A/D Converter"
UART2 transmit, NACK2 (4)	+60 to +63 (003Ch to 003Fh)	15	21. "Serial Interface UARTi (i = 0 to 4)"
UART2 receive, ACK2 (4)	+64 to +67 (0040h to 0043h)	16	
UART0 Transmit, LIN0 Low Detection (10)	+68 to +71 (0044h to 0047h)	17	21. "Serial Interface UARTi (i = 0 to 4)" 24. "LIN Module"
UART0 receive	+72 to +75 (0048h to 004Bh)	18	21. "Serial Interface UARTi (i = 0 to 4)"
UART1 transmit	+76 to +79 (004Ch to 004Fh)	19	
UART1 receive	+80 to +83 (0050h to 0053h)	20	
Timer A0	+84 to +87 (0054h to 0057h)	21	15. "Timer A"
Timer A1	+88 to +91 (0058h to 005Bh)	22	
Timer A2	+92 to +95 (005Ch to 005Fh)	23	
Timer A3	+96 to +99 (0060h to 0063h)	24	
Timer A4	+100 to +103 (0064h to 0067h)	25	
Timer B0	+104 to +107 (0068h to 006Bh)	26	16. "Timer B"
Timer B1	+108 to +111 (006Ch to 006Fh)	27	
Timer B2	+112 to +115 (0070h to 0073h)	28	

Notes:
1. Address relative to address in INTB.
2. Set the IFSR7 bit in the IFSR register to 1.
3. Set the IFSR6 bit in the IFSR register to 1.
4. In I2C mode, NACK and ACK are interrupt sources.
5. These interrupts cannot be disabled using the I flag.
6. Bus collision detection: In IE mode, bus collision detection is the interrupt source. In I2C mode, however, start condition or a stop condition detection are the interrupt sources.
7. Use the IFSR20 bit in the IFSR2A register to select.
8. Use the IFSR44 bit in the IFSR4A register to select.
9. Use the IFSR45 bit in the IFSR4A register to select.
10. Use the IFSR43 bit in the IFSR4A register to select.

Table 12.7 Relocatable Vector Tables (2/2)

Interrupt Source	Vector Address (1) Address (L) to Address (H)	Software Interrupt Number	Reference
$\overline{\text{INT0}}$	+116 to +119 (0074h to 0077h)	29	12.8 "$\overline{\text{INT}}$ Interrupt"
$\overline{\text{INT1}}$	+120 to +123 (0078h to 007Bh)	30	
$\overline{\text{INT2}}$	+124 to +127 (007Ch to 007Fh)	31	
DMA2	+164 to +167 (00A4h to 00A7h)	41	14. "DMAC"
DMA3	+168 to +171 (00A8h to 00ABh)	42	
CAN1 reception complete (6)	+172 to +175 (00ACh to 0AFh)	43	25. "CAN Module"
CAN1 transmission complete (7)	+176 to +179 (00B0h to 00B3h)	44	
CAN1 receive FIFO (8)	+180 to +183 (00B4h to 00B7h)	45	
CAN1 transmit FIFO (9)	+184 to +187 (00B8h to 00BBh)	46	
UART4 transmit, real-time clock compare (2)	+188 to +191 (00BCh to 00BFh)	47	21. "Serial Interface UARTi (i = 0 to 4)" 20. "Real-Time Clock"
UART4 receive	+192 to +195 (00C0h to 00C3h)	48	
CAN0 wake-up	+196 to +199 (00C4h to 00C7h)	49	25. "CAN Module"
UART3 transmit, CAN0 error (4)	+200 to +203 (00C8h to 00CBh)	50	21. "Serial Interface UARTi (i = 0 to 4)" 25. "CAN Module"
UART3 receive, CAN1 wake-up (10)	+204 to +207 (00CCh to 00CFh)	51	
Real-time clock cycle/CAN1 error (11)	+208 to +211 (00D0h to 00D3h)	52	20. "Real-Time Clock", 25. "CAN Module"
CAN0 reception complete	+212 to +215 (00D4h to 00D7h)	53	25. "CAN Module"
CAN0 transmission complete	+216 to +219 (00D8h to 00DBh)	54	
CAN0 receive FIFO	+220 to +223 (00DCh to 00DFh)	55	
CAN0 transmit FIFO	+224 to +227 (00E0h to 00E3h)	56	
IC/OC interrupt 0 (0 to 7)	+228 to +231 (00E4h to 00E7h)	57	18. "Timer S" 22. "Multi-master I^2C-bus Interface"
IC/OC channel 0	+232 to +235 (00E8h to 00EBh)	58	
IC/OC interrupt 1 (0 to 7), I^2C-bus interrupt (3)	+236 to +239 (00ECh to 00EFh)	59	
IC/OC channel 1, SCL/SDA interrupt (5)	+240 to +243 (00F0h to 00F3h)	60	
IC/OC channel 2	+244 to +247 (00F4h to 00F7h)	61	
IC/OC channel 3	+248 to +251 (00F8h to 00FBh)	62	
IC/OC base timer	+252 to +255 (00FCh to 00FFh)	63	

Notes:
1. Address relative to address in INTB.
2. Use the IFSR36 bit in the IFSR3A register to select.
3. Use the IFSR22bit in the IFSR2A register to select.
4. Use the IFSR25 bit in the IFSR2A register to select.
5. Use the IFSR23 bit in the IFSR2A register to select.
6. Set the IFSR33 bit in the IFSR3A register to 1.
7. Set the IFSR34 bit in the IFSR3A register to 1.
8. Set the IFSR46 bit in the IFSR4A register to 1.
9. Set the IFSR35 bit in the IFSR3A register to 1.
10. Set the IFSR32 bit in the IFSR3A register to 1.
11. Set the IFSR47 bit in the IFSR4A register to 1.

12.7 Interrupt Control

12.7.1 Maskable Interrupt Control

The settings for enabling/disabling the maskable interrupts and of the acceptance priority are explained below. Note that these explanations do not apply to non-maskable interrupts.
Use the I flag in the FLG register, IPL, and bits ILVL2 to ILVL0 in the corresponding interrupt control register to enable or disable a maskable interrupt. Whether an interrupt is requested or not is indicated by the IR bit in the corresponding interrupt control register.

12.7.1.1 I Flag

The I flag enables or disables maskable interrupts. Setting the I flag to 1 (enabled) enables maskable interrupts. Setting the I flag to 0 (disabled) disables all maskable interrupts.

12.7.1.2 IR Bit

The IR bit becomes 1 (interrupt requested) when an interrupt request is generated. Then, when the interrupt request is accepted, the IR bit becomes 0 (interrupt not requested).
The IR bit can be set to 0 by a program. Do not write 1 to this bit.

However, the IR bit behaves differently with interrupts in the serial bus interface and LIN module. Refer to 12.2.3 “Interrupt Control Register 2 (INT7IC/SS0IC, INT6IC/LIN0IC, INT3IC, INT5IC, INT4IC, INT0IC to INT2IC)”.

12.7.1.3 Bits ILVL2 to ILVL0 and IPL

Interrupt priority levels can be selected by setting bits ILVL2 to ILVL0.
Table 12.8 lists the Settings of Interrupt Priority Levels and Table 12.9 lists the Interrupt Priority Levels Enabled by IPL.

An interrupt request is accepted under the following conditions.
- I flag = 1
- IR bit = 1
- Interrupt priority level > IPL

The I flag, IR bit, bits ILVL2 to ILVL0, and IPL are independent of each other. They do not affect one another.

Table 12.8 Settings of Interrupt Priority Levels

Bits ILVL2 to ILVL0	Interrupt Priority Level	Priority
000b	Level 0 (interrupt disabled)	-
001b	Level 1	Low
010b	Level 2	↓
011b	Level 3	↓
100b	Level 4	↓
101b	Level 5	↓
110b	Level 6	↓
111b	Level 7	High

Table 12.9 Interrupt Priority Levels Enabled by IPL

IPL	Enabled Interrupt Priority Levels
000b	Level 1 and above are enabled
001b	Level 2 and above are enabled
010b	Level 3 and above are enabled
011b	Level 4 and above are enabled
100b	Level 5 and above are enabled
101b	Level 6 and above are enabled
110b	Level 7 and above are enabled
111b	All maskable interrupts are disabled

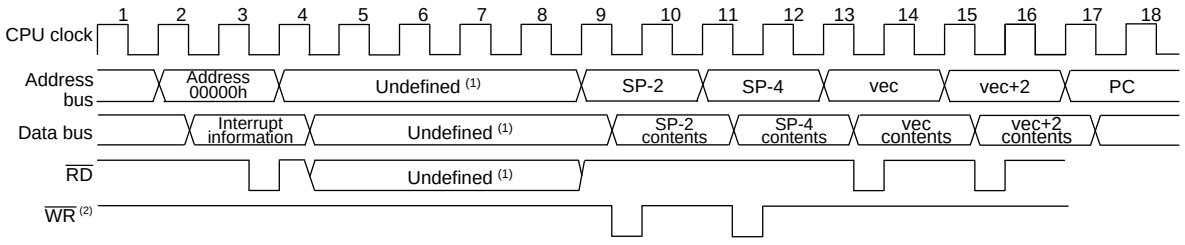
12.7.2 Interrupt Sequence

The interrupt sequence is explained here. The sequence starts when an interrupt request is accepted and ends when the interrupt routine is executed.
When an interrupt request occurs during execution of an instruction, the processor determines its priority after the execution of the instruction is completed, and transfers control to the interrupt sequence from the next cycle. However, if an interrupt occurs during execution of either the SMOVB, SMOVF, SSTR, or RMPA instruction, the processor temporarily suspends the instruction being executed, and transfers control to the interrupt sequence.
The CPU behavior during the interrupt sequence is described below. Figure 12.3 shows Time Required for Executing Interrupt Sequence.

(1) The CPU obtains interrupt information (interrupt number and interrupt request level) by reading address 00000h. Then, the IR bit applicable to the interrupt information is set to 0 (interrupt not requested).
(2) The FLG register, prior to the interrupt sequence, is saved to a temporary register (1) within the CPU.
(3) Flags I, D, and U in the FLG register are set as follows:
The I flag is set to 0 (interrupt disabled)
The D flag is set to 0 (single-step interrupt disabled).
The U flag is set to 0 (ISP selected).
Note that the U flag does not change states when an INT instruction for software interrupt numbers 32 to 63 is executed.
(4) The temporary register (1) within the CPU is saved on the stack.
(5) The PC is saved on the stack.
(6) The interrupt priority level of the acknowledged interrupt is set in the IPL.
(7) The start address of the relevant interrupt routine set in the interrupt vector is stored in the PC.

After the interrupt sequence is completed, an instruction is executed from the starting address of the interrupt routine.

Note:
1. Temporary registers cannot be modified by the user.

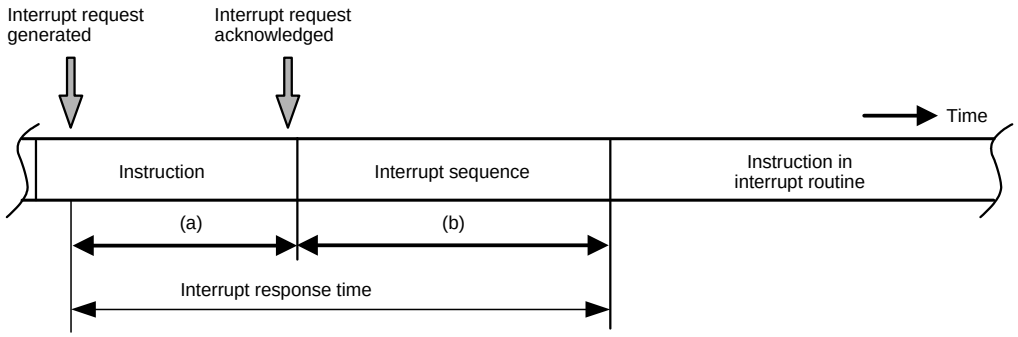


Notes:
1. The undefined state depends on the instruction queue buffer. A read cycle is generated when the instruction queue buffer is ready to prefetch.
2. The $\overline{WR}$ signal timing shown here applies when the stack is located in the internal RAM.

Figure 12.3 Time Required for Executing Interrupt Sequence

12.7.3 Interrupt Response Time

Figure 12.4 shows the Interrupt Response Time. The interrupt response or interrupt acknowledge time denotes the time from when an interrupt request is generated until the first instruction in the interrupt routine is executed. Specifically, it consists of the time from when an interrupt request is generated until the executing instruction is completed ((a) in Figure 12.4) and the time during which the interrupt sequence is executed ((b) in Figure 12.4).



(a) The time from when an interrupt request is generated until the instruction currently executing is completed. The length of this time varies with the instruction being executed. The DIVX instruction requires the longest time, which is equal to 30 cycles (no wait state if the divisor is a register).

(b) The time during which the interrupt sequence is executed. For details, see the table below. Note, however, that the values in this table must be increased by 2 cycles for the $\overline{\text{DBC}}$ interrupt and by 1 cycle for the address match and single-step interrupts.

Interrupt Vector Address	SP Value	No Wait State
Even	Even	18 cycles
Even	Odd	19 cycles
Odd	Even	19 cycles
Odd	Odd	20 cycles

Figure 12.4 Interrupt Response Time

12.7.4 Variation of IPL When Interrupt Request is Accepted

When a maskable interrupt request is accepted, the interrupt priority level of the accepted interrupt is set in the IPL.

When a software interrupt or special interrupt request is accepted, one of the interrupt priority levels listed in Table 12.10 is set in the IPL. Table 12.10 lists the IPL Level Set in IPL When Software or Special Interrupt is Accepted.

Table 12.10 IPL Level Set in IPL When Software or Special Interrupt is Accepted

Interrupt Source	Level Set in IPL
Watchdog timer, $\overline{\text{NMI}}$, oscillator stop/restart detect, voltage monitor 2	7
Software, address match, $\overline{\text{DBC}}$, single-step	Not changed

12.7.5 Saving Registers

In the interrupt sequence, the FLG register and PC are saved on the stack.
At this time, the 4 upper bits of the PC and the 4 upper (IPL) and 8 lower bits in the FLG register, 16 bits in total, are saved on the stack first. Next, the 16 lower bits of the PC are saved. Figure 12.5 shows the Stack Status Before and After Acceptance of Interrupt Request.
The other necessary registers must be saved by a program at the beginning of the interrupt routine. Use the PUSHM instruction, and all registers except SP can be saved with a single instruction.

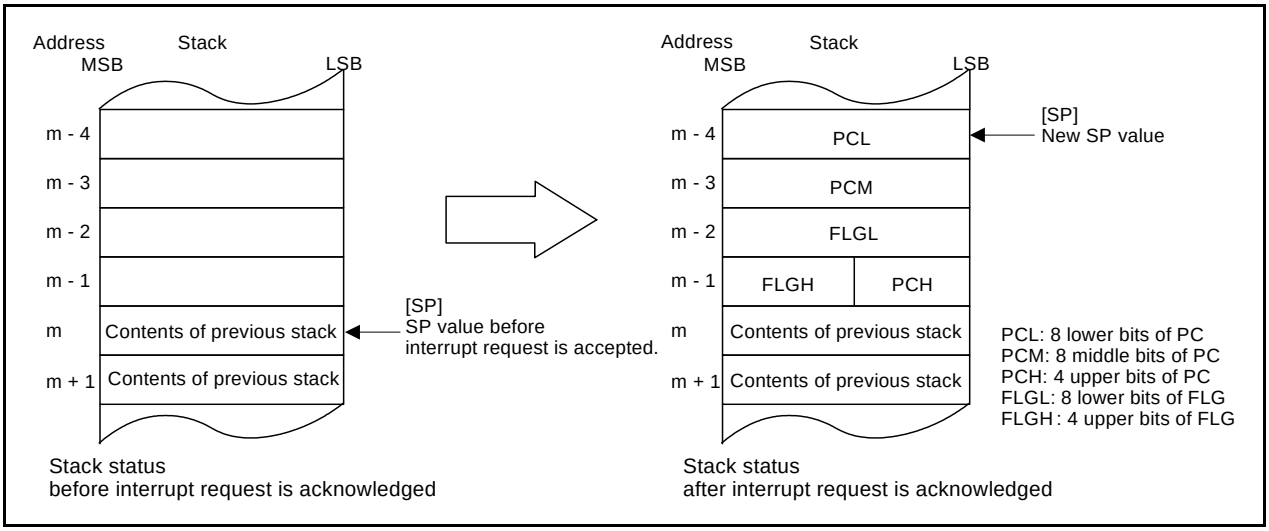


Figure 12.5 Stack Status Before and After Acceptance of Interrupt Request

The register save operation carried out in the interrupt sequence is dependent on whether the SP (1), at the time of acceptance of an interrupt request, is even or odd. If the SP (1) is even, the FLG register and the PC are saved 16 bits at a time. If odd, they are saved in two steps, 8 bits at a time. Figure 12.6 shows the Register Save Operation.

Note:
1. When an INT instruction with software numbers 32 to 63 has been executed, it is the SP indicated by the U flag. Otherwise, it is the ISP.

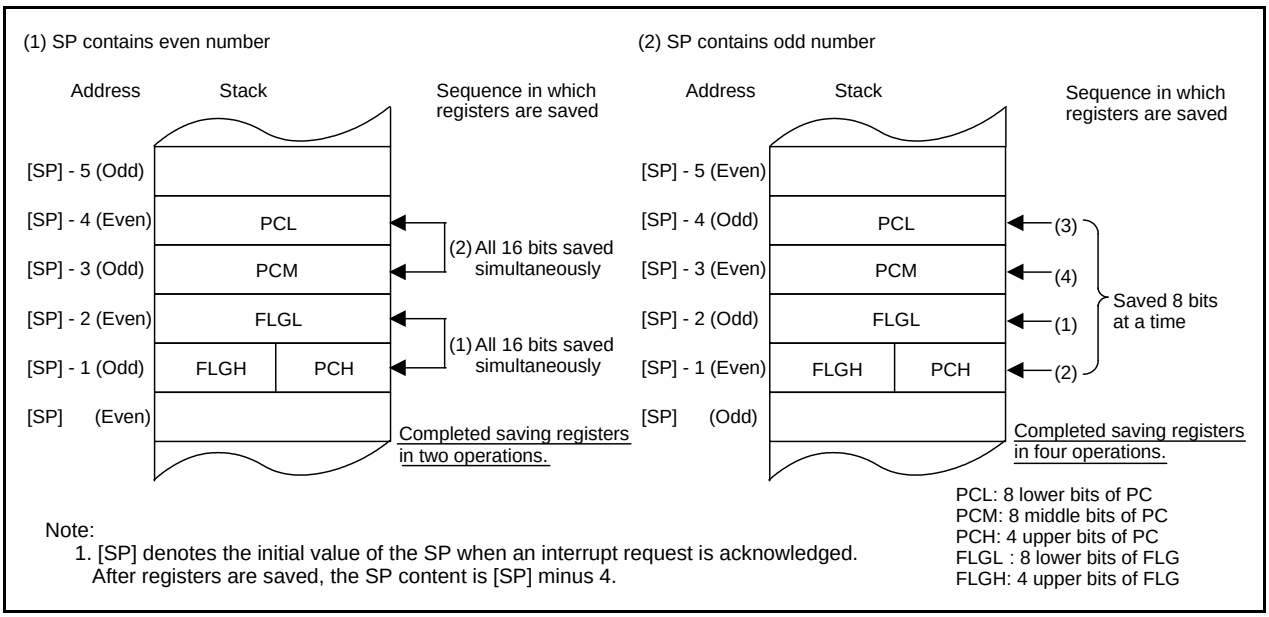


Figure 12.6 Register Save Operation

12.7.6 Returning from an Interrupt Routine

The FLG register and PC saved in the stack immediately before entering the interrupt sequence are restored from the stack by executing the REIT instruction at the end of the interrupt routine. Then, the CPU returns to the program which was being executed before the interrupt request was accepted.
Restore the other registers saved by a program within the interrupt routine using the POPM or a similar instruction before executing the REIT instruction.
The register bank is switched back to the bank used prior to the interrupt sequence by the REIT instruction.

12.7.7 Interrupt Priority

If two or more interrupt requests occur at the same sampling points (the point in time at which interrupt requests are detected), the interrupt with the highest priority is acknowledged.
For maskable interrupts (peripheral function interrupts), any priority level can be selected using bits ILVL2 to ILVL0. However, if two or more maskable interrupts have the same priority level, their interrupt priority is selected by hardware, with the highest priority interrupt accepted.
The watchdog timer interrupt and other special interrupts have their priority levels set in hardware. Figure 12.7 shows the Hardware Interrupt Priority.
Software interrupts are not affected by the interrupt priority. When an instruction is executed, control always branches to the interrupt routine.

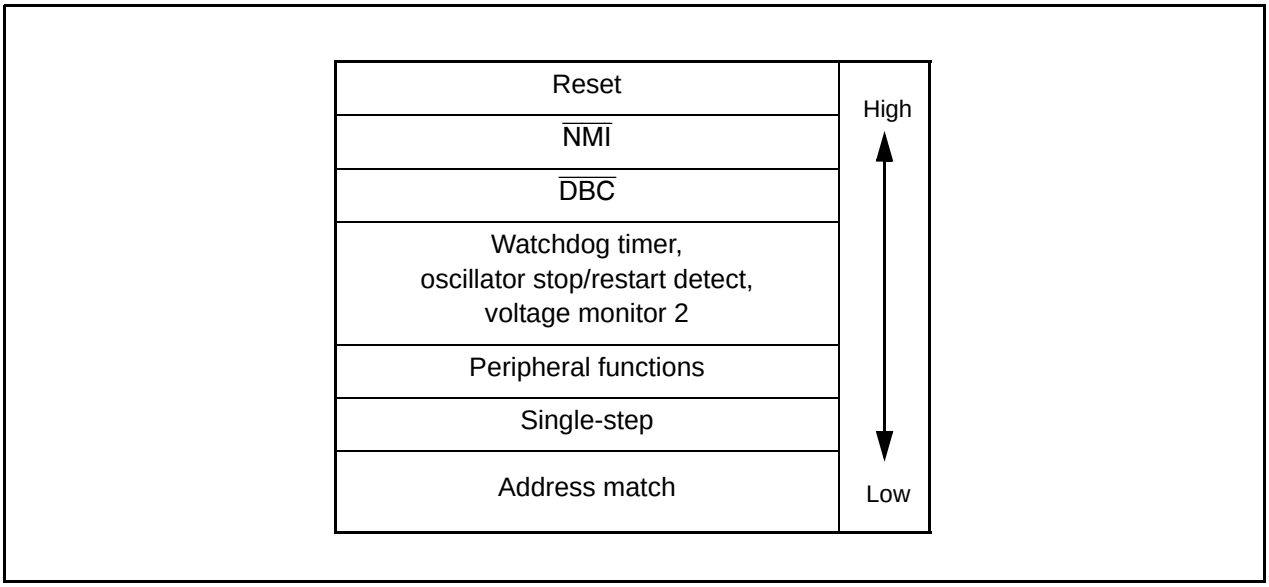


Figure 12.7 Hardware Interrupt Priority

12.7.8 Interrupt Priority Level Select Circuit

The interrupt priority level select circuit selects the highest priority interrupt among sampled interrupt requests at the same sampling point.
Figure 12.8 shows the Interrupt Priority Select Circuit.

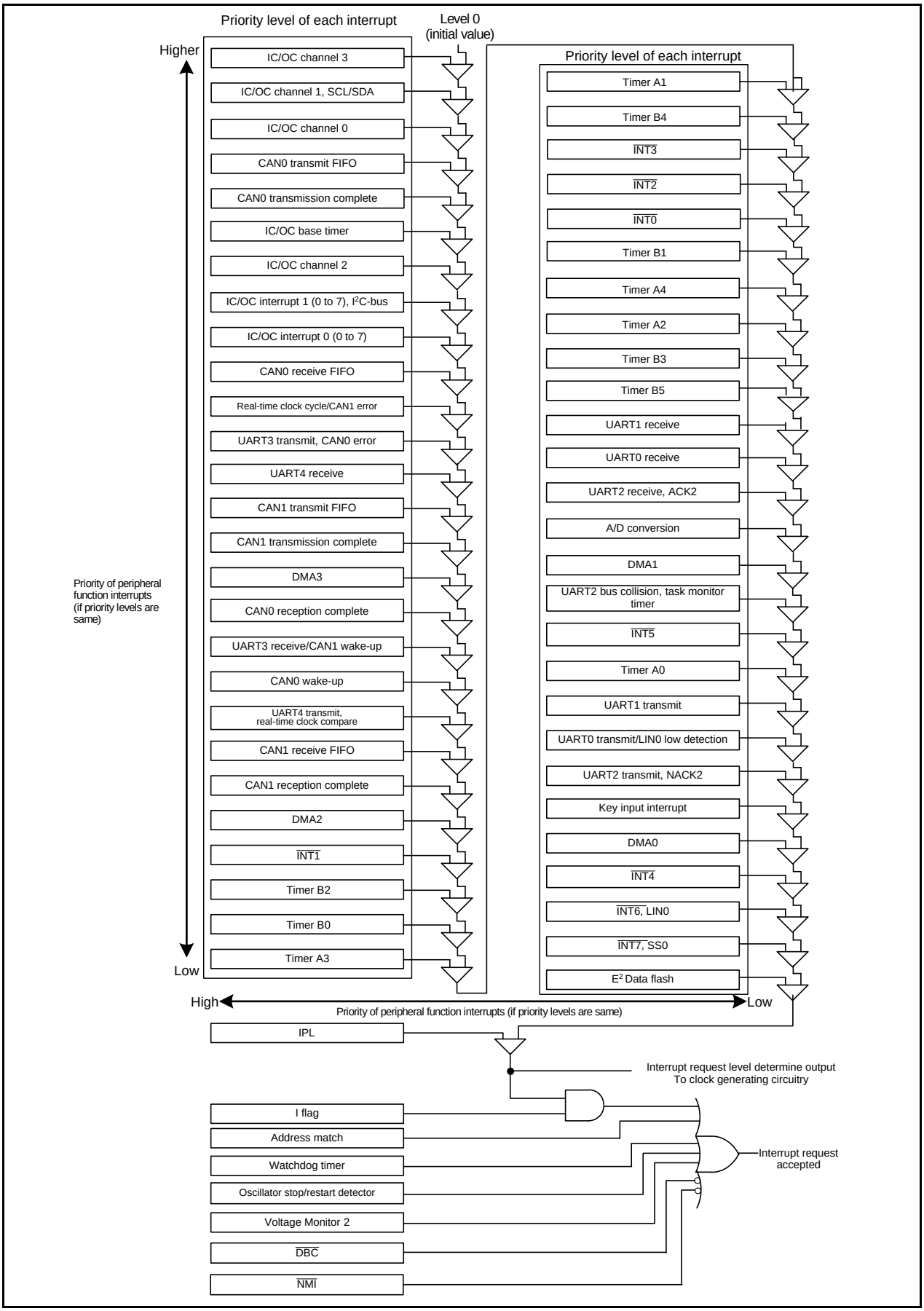


Figure 12.8 Interrupt Priority Select Circuit

12.7.9 Multiple Interrupts

The following shows the internal bit states when control has branched to an interrupt routine.

- I flag = 0 (interrupt disabled)
- IR bit = 0 (interrupt not requested)
- Interrupt priority level = IPL

By setting the I flag to 1 (interrupt enabled) in the interrupt routine, an interrupt request with higher priority than the IPL can be acknowledged.

The interrupt requests not acknowledged because of their low interrupt priority level are kept pending. When the IPL is restored by an REIT instruction and interrupt priority is resolved against it, the pending interrupt request is acknowledged if the following condition is met:

Interrupt priority level of pending interrupt request > Restored IPL

12.8 $\overline{\text{INT}}$ Interrupt

The $\overline{\text{INTi}}$ interrupt (i = 0 to 5) is triggered by the edges of external inputs. The edge polarity is selected using the IFSRi bit in the IFSR register.

To use the $\overline{\text{INT4}}$ interrupt, set the IFSR6 bit in the IFSR register to 1 ($\overline{\text{INT4}}$). To use the $\overline{\text{INT5}}$ interrupt, set the IFSR7 bit in the IFSR register to 1 ($\overline{\text{INT5}}$).

INT6 interrupt and INT7 interrupt are triggered by the edges of external inputs. The edge polarity is selected using the IFSR30 bit and IFSR31bit in the IFSR3A register.

To use the $\overline{\text{INT6}}$ interrupt, set the IFSR45 bit in the IFSR4A register to 0 ($\overline{\text{INT6}}$). To use the $\overline{\text{INT7}}$ interrupt, set the IFSR44 bit in the IFSR4A register to 0 ($\overline{\text{INT7}}$).

12.9 $\overline{\text{NMI}}$ Interrupt

An $\overline{\text{NMI}}$ interrupt is generated when input to the $\overline{\text{NMI}}$ pin changes state from high to low. The $\overline{\text{NMI}}$ interrupt is a non-maskable interrupt. To use the $\overline{\text{NMI}}$ interrupt, set the PM24 bit in the PM2 register to 1 ($\overline{\text{NMI}}$ interrupt enabled). The $\overline{\text{NMI}}$ input uses a digital debounce function. Refer to 11. “Programmable I/O Ports” for the digital debounce function. Figure 12.9 shows $\overline{\text{NMI}}$ Interrupt Block Diagram.

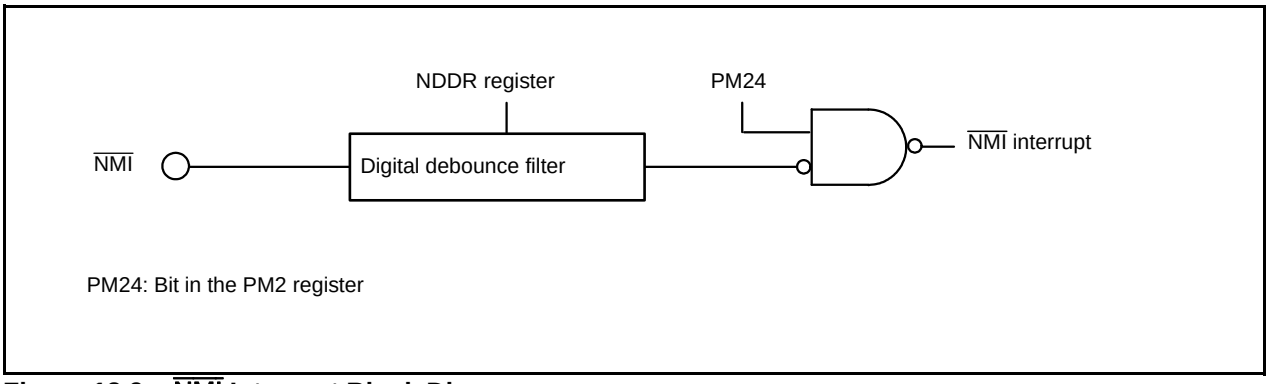


Figure 12.9 $\overline{\text{NMI}}$ Interrupt Block Diagram

12.10 Key Input Interrupt

When input to any pin from P10_4 to P10_7 becomes low where the corresponding PD10_4 to PD10_7 bit in the PD10 register is 0 (input), the IR bit in the KUPIC register becomes 1 (key input interrupt request). When using any pin from $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ for the key input interrupt, do not use all four pins AN4 to AN7 as analog input pins. While input to any pin from P10_4 to P10_7 is low, inputs to all other pins of the port are not detected as interrupts.

Key input interrupts can be used as a key-on wake up function for getting the MCU out of wait or stop mode.

Figure 12.10 shows Block Diagram of Key Input Interrupt.

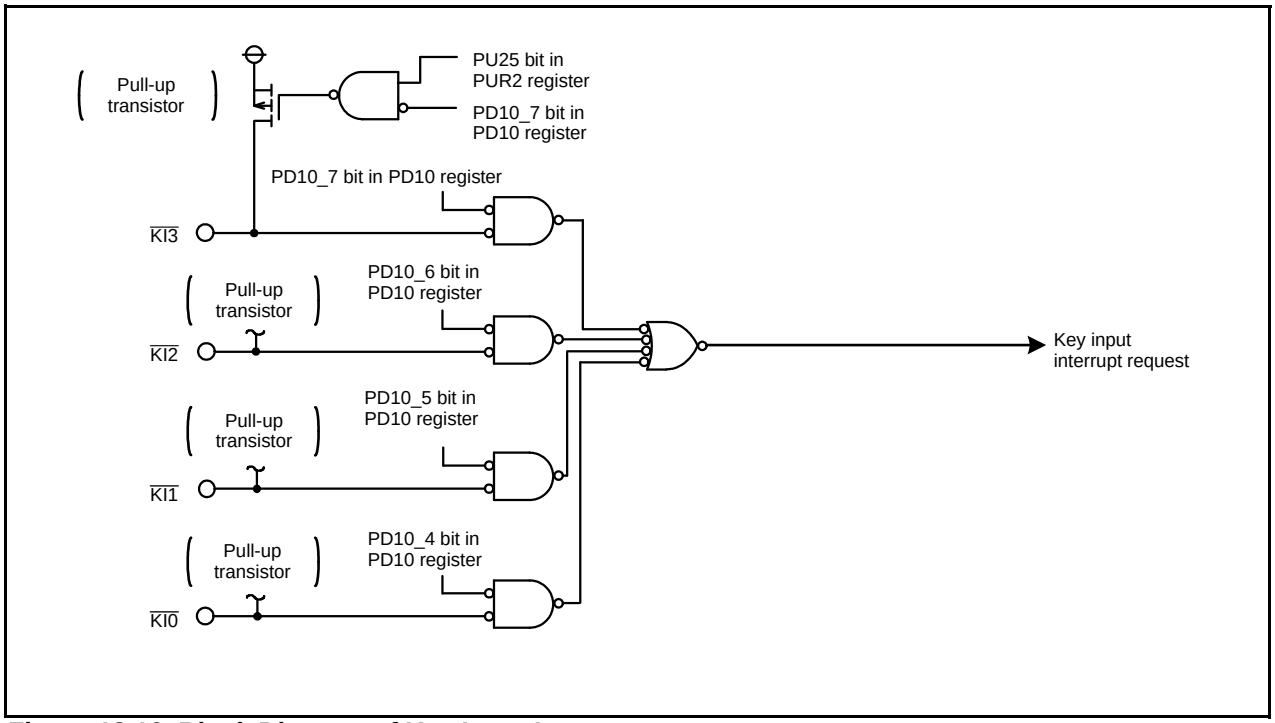


Figure 12.10 Block Diagram of Key Input Interrupt

12.11 Address Match Interrupt

An address match interrupt is generated immediately before executing the instruction at the address indicated by the RMADi register (i = 0 to 3). Set the start address of any instruction in the RMADi register. Use bits AIER0 and AIER1 in the AIER register, and bits AIER20 and AIER21 in the AIER2 register to enable or disable the interrupt. Note that the address match interrupt is unaffected by the I flag and IPL. When an address match interrupt request is acknowledged, the value of the PC that is saved to the stack area (refer to 12.7.5 “Saving Registers”) varies depending on the instruction at the address indicated by the RMADi register. (The value of the PC that is saved to the stack area is not the correct return address.) Therefore, use one of the following methods to return from the address match interrupt:

- Rewrite the values of the stack and then use the REIT instruction to return.
- Restore the stack to its previous state by using the POP or similar instructions before the interrupt request was accepted and then use a jump instruction to return.

Table 12.11 Value of PC Saved on Stack Area When Address Match Interrupt Request Accepted

Instruction at the Address Indicated by the RMADi Register	Value of the PC That Is Saved to the Stack Area
• 16-bit operation code instructions • Instruction shown below among 8-bit operation code instructions ADD.B:S #IMM8, dest SUB.B:S #IMM8, dest AND.B:S #IMM8, dest OR.B:S #IMM8, dest MOV.B:S #IMM8, dest STZ #IMM8, dest STNZ #IMM8, dest STZX #IMM81, #IMM82,dest CMP.B:S #IMM8, dest PUSHM src POPM dest JMPS #IMM8 JSRS #IMM8 MOV.B:S #IMM, dest (however, dest = A0 or A1)	The address indicated by the RMADi register +2
Instructions not listed above	The address indicated by the RMADi register +1

Refer to 12.7.5 “Saving Registers” for PC values saved to the stack area.

Table 12.12 Relationship between Address Match Interrupt Sources and Associated Registers

Address Match Interrupt Sources	Address Match Interrupt Enable Bit	Address Match Interrupt Register
Address match interrupt 0	AIER0	RMAD0
Address match interrupt 1	AIER1	RMAD1
Address match interrupt 2	AIER20	RMAD2
Address match interrupt 3	AIER21	RMAD3

12.12 Non-Maskable Interrupt Source Discrimination

The watchdog timer interrupt, oscillator stop/restart detect interrupt, and voltage monitor 2 interrupt share the same interrupt vector. When using some functions together, read the detect flags of the events in an interrupt processing program, and determine the source of the interrupt. Table 12.13 lists Bits Used for Non-Maskable Interrupt Source Discrimination.

Table 12.13 Bits Used for Non-Maskable Interrupt Source Discrimination

Interrupt	Detect Flag	
	Bit Position	Function
Watchdog timer	VW2C3 bit in the VW2C register (watchdog timer underflow detected)	0: Not detected 1: Detected
Oscillator stop/restart detect	CM22 bit in the CM2 register (oscillator stop/restart detected)	
Voltage monitor 2	VW2C2 bit in the VW2C register (Vdet2 passage detected)	

12.13 Notes on Interrupts

12.13.1 Reading Address 00000h

Do not read address 00000h by a program. When a maskable interrupt request is accepted, the CPU reads interrupt information (interrupt number and interrupt request priority level) from address 00000h during the interrupt sequence. At this time, the IR bit of the accepted interrupt is cleared to 0 (interrupt not requested).

If address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts becomes 0. This may cause problems such as interrupts being canceled or an unexpected interrupt request being generated.

12.13.2 SP Setting

Set a value in the SP (USP, ISP) before accepting an interrupt. The SP (USP, ISP) is set to 0000h after reset. Therefore, if an interrupt is accepted before setting a value in the SP (USP, ISP), the program may go out of control.

Set a value in the ISP at the beginning of the program. For the first instruction after reset only, all interrupts are disabled.

12.13.3 $\overline{\text{NMI}}$ Interrupt

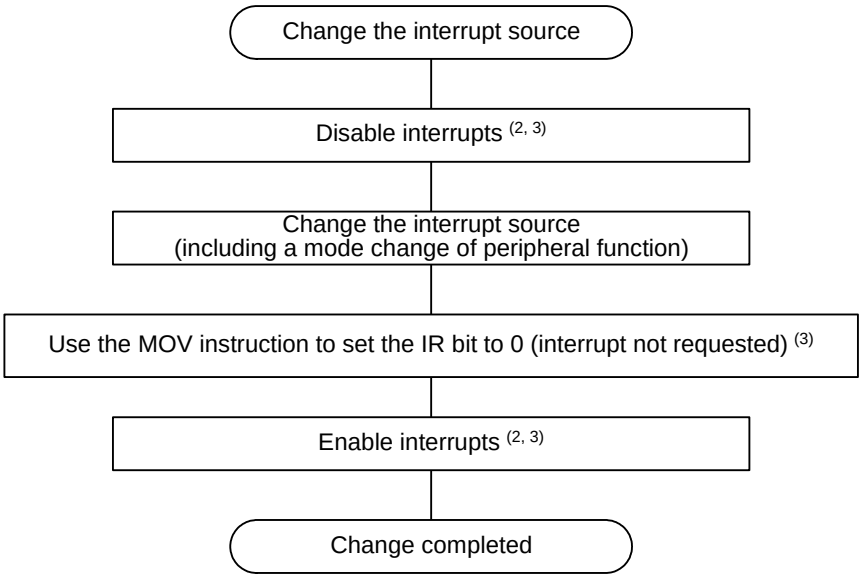
- When not using the $\overline{\text{NMI}}$ interrupt, set the PM24 bit in the PM2 register to 0 ($\overline{\text{NMI}}$ interrupt disabled).
- The $\overline{\text{NMI}}$ interrupt is disabled after reset. The $\overline{\text{NMI}}$ interrupt is enabled by setting the PM24 bit in the PM2 register to 1. Set the PM24 bit to 1 when a high-level signal is applied to the $\overline{\text{NMI}}$ pin. When the PM24 bit is set to 1 while a low-level signal is applied, an $\overline{\text{NMI}}$ interrupt is generated. Once the $\overline{\text{NMI}}$ interrupt is enabled, it cannot be disabled until the MCU is reset.
- The MCU cannot enter stop mode while the PM24 bit is 1 ($\overline{\text{NMI}}$ interrupt enabled) and input on the $\overline{\text{NMI}}$ pin is low. When input on the $\overline{\text{NMI}}$ pin is low, the CM10 bit in the CM1 register is fixed to 0.
- Do not enter wait mode while the PM24 bit is 1 ($\overline{\text{NMI}}$ interrupt enabled) and a low signal is input to the $\overline{\text{NMI}}$ pin. When the $\overline{\text{NMI}}$ pin is driven low, the CPU clock remains active even though the CPU stops, and therefore, the current consumption of the chip does not drop. In this case, the normal condition is restored by the next interrupt generation.
- Set the low- and high-level durations of the input signal to the $\overline{\text{NMI}}$ pin to 2 CPU clock cycles + 300 ns or more.

12.13.4 Changing an Interrupt Source

When the interrupt source is changed, the IR bit in the interrupt control register may become 1 (interrupt requested). To use an interrupt, change the interrupt source, and then set the IR bit to 0 (interrupt not requested).

In this section, the changing of an interrupt source refers to all elements used in changing the interrupt source, polarity, and timing assigned to each software interrupt number. Therefore, if a mode change of any peripheral function involves changing the source, polarity or timing of an interrupt, be sure to clear the IR bit for that interrupt to 0 (interrupt not requested) after making such changes. Refer to the descriptions of the individual peripheral functions for details of the interrupts.

Figure 12.11 shows the Procedure for Changing the Interrupt Generate Source.



IR bit: A bit in the interrupt control register

Notes:
1. Execute the above settings individually. Do not use one instruction to execute two or more settings simultaneously.
2. Use the I flag for the INTi interrupt (i = 0 to 7).
   For the interrupts from peripheral functions other than the INTi interrupt, disable the peripheral function that is the source of the interrupt so as not to generate an interrupt request before changing the interrupt source. In this case, if the maskable interrupts can all be disabled without causing a problem, use the I flag. Otherwise, use corresponding bits ILVL2 to ILVL0 in the interrupt control register whose interrupt source is to be changed.
3. Refer to 12.13.5 “Rewriting the Interrupt Control Register” for details about the instructions to be used and the notes to be taken for instruction execution.

Figure 12.11 Procedure for Changing the Interrupt Generate Source

12.13.5 Rewriting the Interrupt Control Register

To modify the interrupt control register, follow either of the procedures below:

- Modify in places where no interrupt requests corresponding to the interrupt control register may occur.
- If an interrupt request can be generated, disable that interrupt and then rewrite the interrupt control register.

When using the I flag to disable an interrupt, set the I flag as shown in the sample program code below. (Refer to 12.13.6 “Instruction to Rewrite the Interrupt Control Register” for rewriting the interrupt control registers using the sample program code.)

Examples 1 through 3 show how to prevent the I flag from becoming 1 (interrupt enabled) before the contents of the interrupt control register is rewritten, owing to the effects of the internal bus and the instruction queue buffer.

Example 1: Using the NOP instruction to pause the program until the interrupt control register is modified

```
INT_SWITCH1:
    FCLR    I               ; Disable interrupts.
    AND.B   #00H, 0055H     ; Set the TA0IC register to 00h.
    NOP                     ;
    NOP
    FSET    I               ; Enable interrupts.
```

Example 2: Using a dummy read to delay the FSET instruction

```
INT_SWITCH2:
    FCLR    I               ; Disable interrupts.
    AND.B   #00H, 0055H     ; Set the TA0IC register to 00h.
    MOV.W   MEM, R0         ; Dummy read.
    FSET    I               ; Enable interrupts.
```

Example 3: Using the POPC instruction to change the I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I               ; Disable interrupts.
    AND.B   #00H, 0055H     ; Set the TA0IC register to 00h.
    POPC    FLG             ; Enable interrupts.
```

12.13.6 Instruction to Rewrite the Interrupt Control Register

- Do not use the BTSTC and BTSTS instructions to rewrite the interrupt control registers.
- Use the AND, OR, BCLR, BSET, or MOV instruction to rewrite interrupt control registers.
  When an interrupt request is generated for the register being rewritten while executing an AND, OR, BCLR, or BSET instruction, the IR bit becomes 1 (interrupt requested) and remains 1.

12.13.7 $\overline{\text{INT}}$ Interrupt

- Either a low level of at least tw(INL) width or a high level of at least tw(INH) width is necessary for the signal input to pins $\overline{\text{INT0}}$ through $\overline{\text{INT7}}$, regardless of the CPU operation clock.
- If the POL bit in registers INT0IC to INT5IC or bits IFSR7 to IFSR0 in the IFSR register are changed, the IR bit may inadvertently become 1 (interrupt requested). Be sure to set the IR bit to 0 (interrupt not requested) after changing any of these register bits.
- If the POL bit in registers INT6IC to INT7IC, bits IFSR31 to IFSR30 in the IFSR3A register, or bits IFSR45 to IFSR44 in the IFSR4A register are changed, the IR bit may inadvertently become 1 (interrupt requested). Set the IR bit to 0 (interrupt not requested) after changing these bits.

13. Watchdog Timer

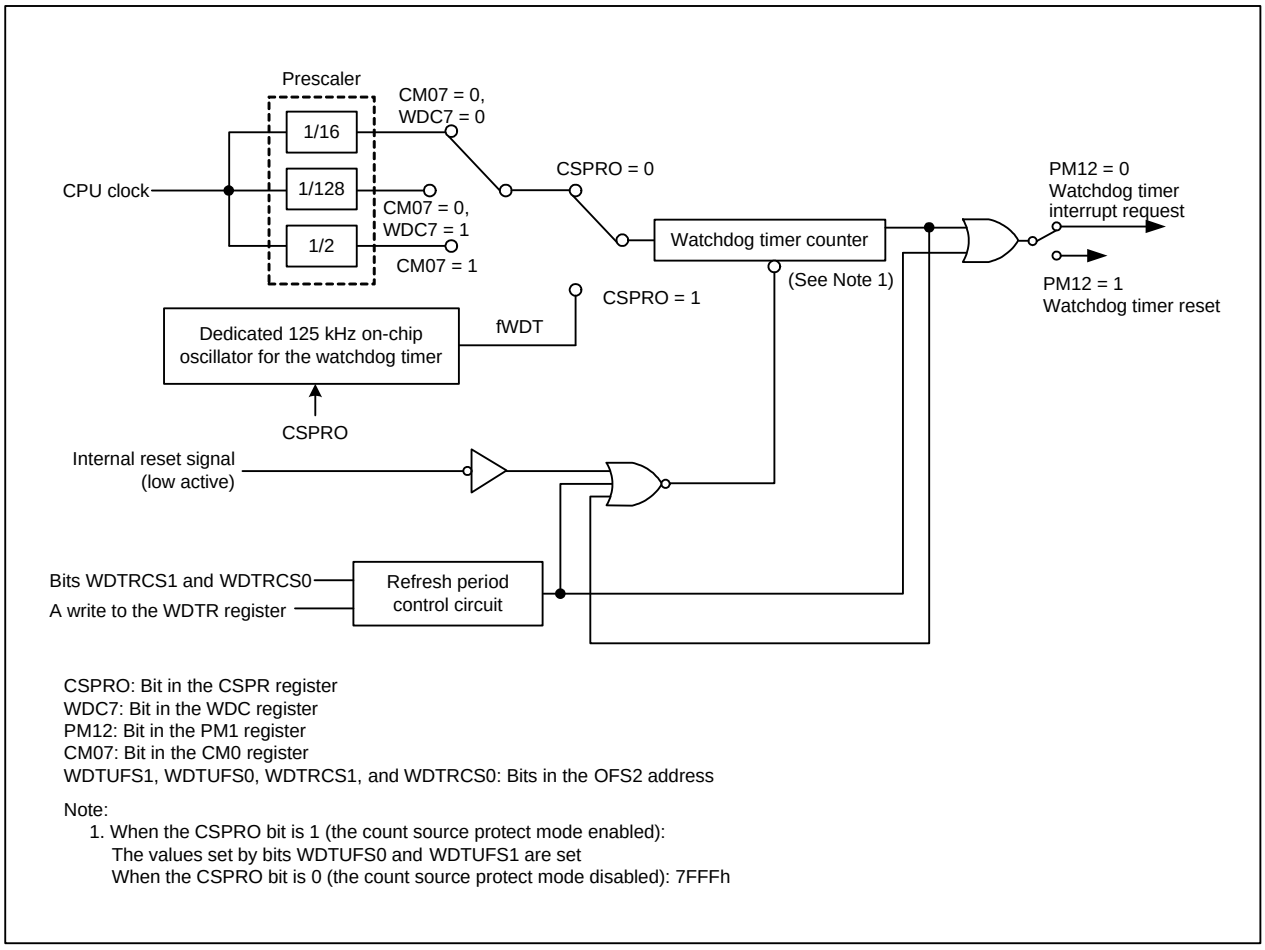
13.1 Introduction

The watchdog timer contains a 15-bit counter, and the count source protection mode can be enabled/disabled.

Table 13.1 shows the watchdog timer specifications and Figure 13.1 shows a block diagram of the watchdog timer. Refer to 6.4.7 “Watchdog Timer Reset” for details on the watchdog timer reset.

Table 13.1 Watchdog Timer Specifications

Item	Count Source Protection Mode Disabled	Count Source Protection Mode Enabled
Count source	CPU clock	Dedicated 125 kHz on-chip oscillator for watchdog timer (fWDT)
Count operation	Decrements	
Count start conditions	One of the following is selectable: (Selected by the WDTON bit in the OFS1 address) • Counting starts automatically after reset. • Counting starts by a write to the WDTS register.	
Count stop conditions	• Stop mode • Wait mode • Software commands executed in EW1 mode, except when executing the suspend function.	None
Watchdog timer counter refresh timing	• Resets (refer to 6. “Resets” for details) • Write 00h followed by FFh to the WDTR register. • Watchdog timer underflow	
Watchdog timer initial value	7FFFh	Selectable by using bits WDTUFS1 and WDTUFS0 in the OFS2 address
When underflows	A watchdog timer interrupt is generated or watchdog timer reset is initiated	Watchdog timer reset is initiated
Selectable functions	• Prescaler divide ratio Divide-by-16 or divide-by-128 (selected by the WDC7 bit in the WDC register) However, divide-by-2 is selected when the CM07 bit in the CM0 register is 1 (sub clock). • Count source protection mode Enabled or disabled (selected by the CSPROINI bit in the OFS1 address and the CSPRO bit in the CSPR register) • Watchdog timer refresh period Selectable by setting bits WDTRCS1 and WDTRCS0 in the OFS2 address.	



CSPRO: Bit in the CSPR register
WDC7: Bit in the WDC register
PM12: Bit in the PM1 register
CM07: Bit in the CM0 register
WDTUFS1, WDTUFS0, WDTRCS1, and WDTRCS0: Bits in the OFS2 address

Note:
1. When the CSPRO bit is 1 (the count source protect mode enabled):
The values set by bits WDTUFS0 and WDTUFS1 are set
When the CSPRO bit is 0 (the count source protect mode disabled): 7FFFh

Figure 13.1 Watchdog Timer Block Diagram

13.2 Registers

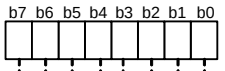
Table 13.2 Registers

Address	Register Names	Register Symbol	Reset Value
002Ch	Voltage Monitor 2 Control Register	VW2C	1000 0X10b
037Ch	Count Source Protection Mode Register	CSPR	00h (1)
037Dh	Watchdog Timer Refresh Register	WDTR	XXh
037Eh	Watchdog Timer Start Register	WDTS	XXh
037Fh	Watchdog Timer Control Register	WDC	00XX XXXXb

Note:
1. When the CSPROINI bit in the OFS1 address is set to 0, the reset value is 1000 0000b.

13.2.1 Voltage Monitor 2 Control Register (VW2C)

Voltage Monitor 2 Control Register



Symbol	Address	Reset Value
VW2C	002Ch	1000 0X10b (hardware reset, power-on reset, voltage monitor 0 reset)

Bit Symbol	Bit Name	Function	RW
VW2C0	Voltage monitor 2 interrupt/ reset enable bit	0 : Disabled 1 : Enabled	RW
VW2C1	Voltage monitor 2 digital filter disable mode select bit	0 : Digital filter enabled 1 : Digital filter disabled	RW
VW2C2	Voltage change detection flag	0 : Not detected 1 : Vdet2 passage detected	RW
VW2C3	Watchdog timer detection flag	0 : Not detected 1 : Watchdog timer underflow detected	RW
VW2F0	Sampling clock select bit	b5 b4 0 0 : fOCO-S divided by 1 0 1 : fOCO-S divided by 2 1 0 : fOCO-S divided by 4 1 1 : fOCO-S divided by 8	RW
VW2F1			
VW2C6	Voltage monitor 2 mode select bit	0 : Voltage monitor 2 interrupt at Vdet2 passage 1 : Voltage monitor 2 reset at Vdet2 passage	RW
VW2C7	Voltage monitor 2 interrupt/ reset generation condition select bit	0: When VCC reaches or goes above Vdet2 1: When VCC reaches or goes below Vdet2	RW

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW2C register.

Bits VW2C2 and VW2C3 do not change at voltage monitor 2 reset, oscillator stop detect reset, watchdog timer reset, or software reset.
When rewriting the VW2C register (excluding the VW2C3 bit), the VW2C2 bit may become 1. Set the VW2C2 bit to 0 after rewriting the VW2C register.

VW2C3 (WDT Detection Flag) (b3)

Use this bit in an interrupt routine to determine the source of the interrupts from the watchdog timer, the oscillator stop/restart detect, and voltage monitor 2.
Conditions to become 0:

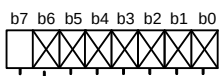
- Writing 0 by a program

Condition to become 1:

- Watchdog timer underflow detected
  This flag remains unchanged even if 1 is written by a program.

13.2.2 Count Source Protection Mode Register (CSPR)

Count Source Protection Mode Register



Symbol	Address	Reset Value
CSPR	037Ch	0000 0000b (when the CSPROINI bit in the OFS1 address is 1) 1000 0000b (when the CSPROINI bit in the OFS1 address is 0)

Bit Symbol	Bit Name	Function	RW
— (b6-b0)	No register bits. If necessary, set to 0. The read value is 0.		—
CSPRO	Count source protection mode select bit	0 : Count source protection mode disabled 1 : Count source protection mode enabled	RW

CSPRO (Count Source Protection Mode Select Bit) (b7)

To set the CSPRO bit to 1, write 1 immediately after writing 0. The CSPRO bit cannot be set to 0 by a program.

When the CSPRO bit in the CSPR register is set to 1 (count source protection mode enabled), the following are automatically set:

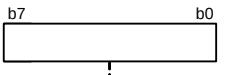
- Dedicated 125 kHz on-chip oscillator for the watchdog timer starts oscillating.
- The PM12 bit in the PM1 register is set to 1 (watchdog timer reset is initiated when the watchdog timer underflows.).
- The initial value of the watchdog timer is a value set by setting bits WDTUFS1 and WDTUFS0 in the OFS2 address.

When the CSPROINI bit in the OFS1 address is 0, the CSPRO bit becomes 1. The CSPROINI bit cannot be changed by a program. In order to set the CSPROINI bit, write 0 to bit 7 of address 0FFFFFh by using a flash programmer.

Do not change the CSPRO bit setting while the watchdog timer is operating.

13.2.3 Watchdog Timer Refresh Register (WDTR)

Watchdog Timer Refresh Register



Symbol	Address	Reset Value
WDTR	037Dh	XXh

Function	RW
The watchdog timer counter is refreshed by writing 00h and then FFh to this register. The default value is indicated by setting bits WDTUFS1 and WDTUFS0 in the OFS2 address.	WO

After the watchdog timer interrupt is generated, refresh the watchdog timer by writing to the WDTR register.

13.2.4 Watchdog Timer Start Register (WDTS)

Watchdog Timer Start Register

b7 b0	Symbol	Address	Reset Value
	WDTS	037Eh	XXh

Function	RW
The watchdog timer starts counting after a write instruction to this register.	WO

The WDTS register is enabled when the WDTON bit in the OFS1 address is 1 (watchdog timer stops after reset).

13.2.5 Watchdog Timer Control Register (WDC)

Watchdog Timer Control Register

b7 b6 b5 b4 b3 b2 b1 b0	Symbol	Address	Reset Value
	WDC	037Fh	00XX XXXXb

Bit Symbol	Bit Name	Function	RW
WDC0		Bits b10 to b5 can be read when the count source protection mode is disabled. When the count source protection mode is enabled, while bits WDTUFS1 and WDTUFS0 in the OFS2 address are: 00b (03FFh), bits b5 to b0 can be read 01b (0FFFh), bits b8 to b3 can be read 10b (1FFFh), bits b9 to b4 can be read 11b (3FFFh), bits b10 to b5 can be read	RO
WDC1			
WDC2			
WDC3			
WDC4			
WDC5			
— (b6)	Reserved bit	The read value is 0.	RO
WDC7	Prescaler select bit	0: Divided by 16 1: Divided by 128	RW

13.3 Optional Function Select Area

In the optional function select area, the MCU state after reset and the function to prevent rewrite in parallel I/O mode are selected.

The optional function select area is not an SFR, and therefore cannot be rewritten by a program. Set an appropriate value when writing a program to flash memory. The entire optional function select area becomes FFh when the block including the optional function select area is erased.

In blank products, the OFS1 and OFS2 address values are FFh when shipped. After a value is written by the user, this address takes on the written value. In programmed products, the OFS1 and OFS2 address values are the value set in the user program prior to shipping.

13.3.1 Optional Function Select Address 1 (OFS1)

Optional Function Select Address 1

b7	b6	b5	b4	b3	b2	b1	b0
		0	1			1	

Symbol: OFS1

Address: FFFFFh

Bit Symbol	Bit Name	Function
WDTON	Watchdog timer start select bit	0 : Watchdog timer starts automatically after reset. 1 : Watchdog timer is in a stopped state after reset.
— (b1)	Reserved bit	Set to 1.
ROMCR	ROM code protect cancel bit	0 : ROM code protection cancelled. 1 : ROMCP1 bit enabled.
ROMCP1	ROM code protect bit	0 : ROM code protection enabled. 1 : ROM code protection cancelled.
— (b4)	Reserved bit	Set to 1.
— (b5)	Reserved bit	Set to 0.
LVDAS	Voltage detector 0 start bit	0 : Voltage monitor 0 reset enabled after hardware reset. 1 : Voltage monitor 0 reset disabled after hardware reset.
CSPROINI	After-reset count source protection mode select bit	0 : Count source protection mode enabled after reset. 1 : Count source protection mode disabled after reset.

WDTON (Watchdog Timer Start Select Bit) (b0)
CSPROINI (After-Reset Count Source Protection Mode Select Bit) (b7)

These bits control the state of watchdog timer after reset.

When setting the CSPROINI bit to 0 (count source protection mode enabled after reset), set the WDTON bit to 0 (watchdog timer starts automatically after reset) as well.

13.3.2 Optional Function Select Address 2 (OFS2)

Optional Function Select Address 2

b7	b6	b5	b4	b3	b2	b1	b0
1	1	1	1				

Symbol: OFS2
Address: FFFDBh

Bit Symbol	Bit Name	Function
WDTUFS0	Watchdog timer initial setting bit	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh
WDTUFS1		
WDTRCS0	Watchdog timer refresh duty cycle setting bit	Refresh period is the last n% of watchdog timer period: b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%
WDTRCS1		
— (b7-b4)	Reserved bits	Set to 1.

WDTUFS1 to WDTUFS0 (Watchdog Timer Initial Setting Bit) (b0-b1)

Enabled when CSPRO bit in the CSPR register is 1 (count source protection mode enabled).

WDTRCS1 to WDTRCS0 (Watchdog Timer Refresh Duty Cycle Setting Bit) (b3-b2)

Assuming the cycle of the watchdog timer underflow is 100%, bits WDTRCS1 and WDTRCS0 select the refresh period for the watchdog timer.
Refer to 13.4.1 “Refresh Operation Period” for details.

13.4 Operations

13.4.1 Refresh Operation Period

To refresh the watchdog timer, the period writing to the WDTR register can be limited to the fixed period before the underflow. The refresh period can be selected by setting bits WDTRCS1 and WDTRCS0 in the OFS2 address. The period specified by these bits assumes that an underflow period of the watchdog timer is 100%. Figure 13.2 shows the refresh operation period for the watchdog timer.

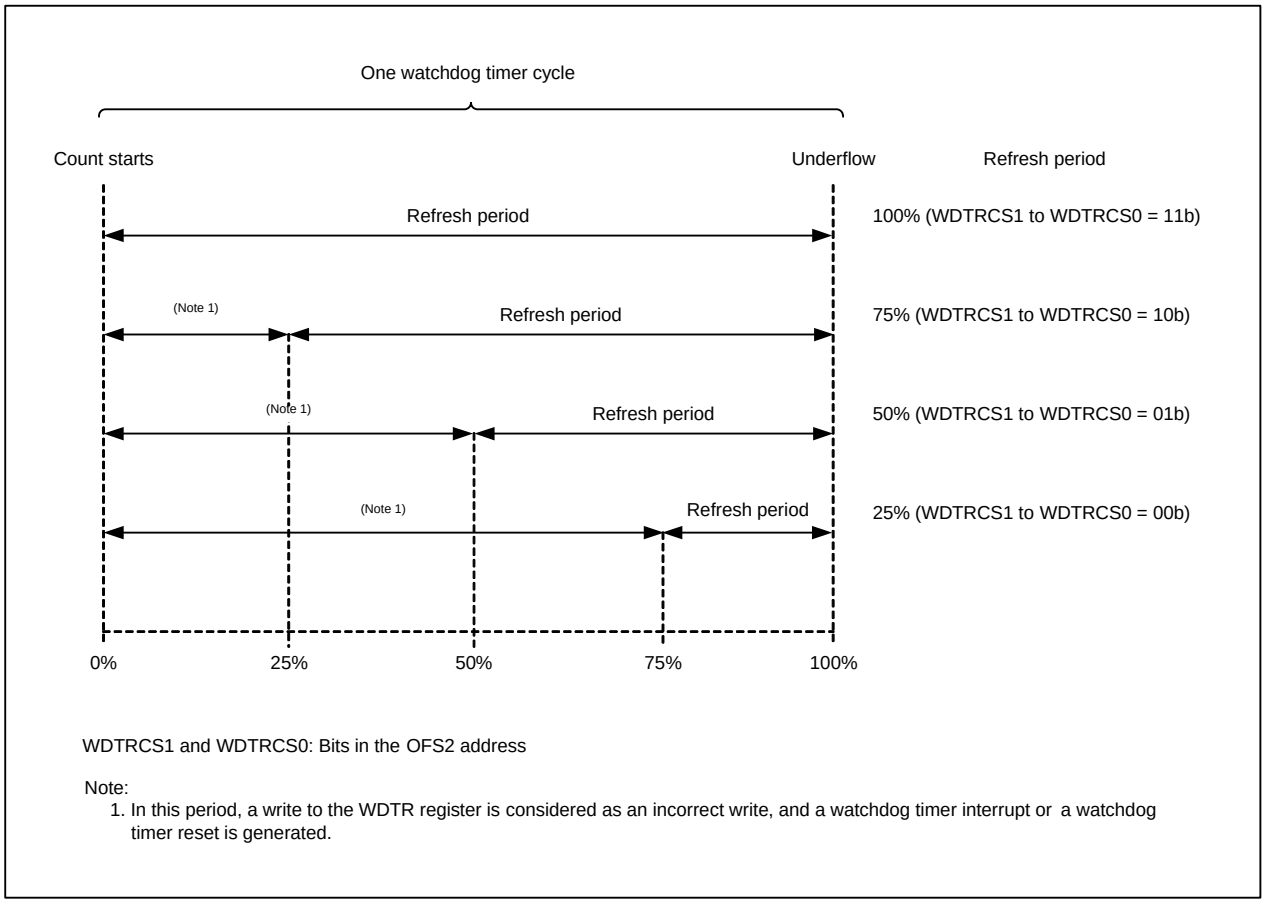


Figure 13.2 Watchdog Timer Refresh Period

13.4.2 Count Source Protection Mode Disabled

The CPU clock is used as the watchdog timer count source when the count source protection mode is disabled.

Table 13.3 lists the specifications of watchdog timer when the count source protection mode is disabled.

Table 13.3 Watchdog Timer Specifications (When Count Source Protection Mode is Disabled)

Item	Specification
Count source	CPU clock
Count operation	Decrements
Watchdog timer cycle	When the CM07 bit in the CM0 register is 0 (main clock, PLL clock, 40 MHz on-chip oscillator clock, 125 kHz on-chip oscillator clock): (1) $\frac{\text{Prescaler divider factor (n)} \times \text{watchdog timer count value (32768)}}{\text{CPU clock}}$ n = 16 or 128, selected by the WDC7 bit in the WDC register Example: When CPU clock frequency is 16 MHz and the prescaler divider factor is 16, the watchdog timer cycle is approximately 32.8 ms. When the CM07 bit is 1 (sub clock): (1) $\frac{\text{Prescaler divider factor (2)} \times \text{watchdog timer count value (32768)}}{\text{CPU clock}}$
Watchdog timer counter refresh timing	• Resets (refer to 6. “Resets” for details) • Write 00h, and then FFh to the WDTR register. • Watchdog timer underflow
Count start conditions	Set the WDTON bit in the OFS1 address to select the watchdog timer state after reset. • When the WDTON bit is 1 (watchdog timer is in a stop state after reset): The watchdog timer and prescaler stop after reset and the watchdog timer starts counting by writing to the WDTS register. • When the WDTON bit is 0 (watchdog timer starts automatically after reset): The watchdog timer and prescaler start counting automatically after reset.
Count stop conditions	• Wait mode • Stop mode • While executing software commands in EW1 mode, except when executing the suspend function. The count resumes from the value held after exiting the modes above.
Operations when the watchdog timer underflows	• When the PM12 bit in the PM1 register is 0, a watchdog timer interrupt is generated. • When the PM12 bit in the PM1 register is 1, the watchdog timer is reset. (refer to 6.4.7 “Watchdog Timer Reset” for details)

Note:

1. Writing 00h and then FFh to the WDTR register refreshes the watchdog timer counter, but not the prescaler. Therefore, marginal differences in the watchdog timer cycle can be expected. The prescaler is initialized by a reset.

13.4.3 Count Source Protection Mode Enabled

When the count source protection mode is enabled, fWDT is used as the watchdog timer count source. Table 13.4 lists the specifications of the watchdog timer when the count source protection mode is enabled.

Table 13.4 Watchdog Timer Specifications (When Count Source Protection Mode is Enabled)

Item	Specification
Count source	fWDT
Count operation	Decrements
Watchdog timer cycle	$\frac{\text{Watchdog timer count value (m)}}{\text{fWDT}}$ m: The value set by setting bits WDTUFS1 and WDTUFS0 in the OFS2 address. Example: When bits WDTUFS1 to WDTUFS0 are 00b (watchdog timer cycle setting is 03FFh), the watchdog timer cycle is approximately 8.2 ms.
Watchdog timer counter refresh timing	• Resets (refer to 6. “Resets” for details) • Write 00h, and then FFh to the WDTR register. • Watchdog timer underflow
Count start conditions	Set the WDTON bit in the OFS1 address to select the watchdog timer operation after reset. • When the WDTON bit is set to 1 (watchdog timer is in stop state after reset): The watchdog timer and prescaler stop after reset and the count starts by writing to the WDTS register. • When the WDTON bit is set to 0 (watchdog timer starts automatically after reset): The watchdog timer and prescaler start counting automatically after reset.
Count stop condition	None. Count continues even in wait mode once the count starts. The MCU does not enter stop mode.
Operations when the watchdog timer underflows	The watchdog timer is reset. (refer to 6.4.7 “Watchdog Timer Reset” for details)

The dedicated 125 kHz on-chip oscillator for the watchdog timer (fWDT) is used as the watchdog timer count source when the count source protection mode is enabled.
The dedicated 125 kHz on-chip oscillator for the watchdog timer (fWDT) automatically oscillates when the CSPRO bit in the CSPR register is 1 (count source protection mode enabled).

13.5 Interrupts

The watchdog timer interrupt is a non-maskable interrupt.

The watchdog timer interrupt, oscillator stop/restart detect interrupt, and voltage monitor 2 interrupt share an vector. When using multiple functions, read the detect flag in an interrupt handler to determine which interrupt factor generates an interrupt request.

- The VW2C3 bit in the VW2C register is the detect flag for the watchdog timer. After the interrupt factor is determined, set the VW2C3 bit to 0 (not detected) by a program.

13.6 Notes on the Watchdog Timer

After the watchdog timer interrupt is generated, use the WDTR register to refresh the watchdog timer counter.

14. DMAC

14.1 Introduction

The direct memory access controller (DMAC) allows data to be transferred without CPU intervention. There are four DMAC channels. Each time a DMA request occurs, the DMAC transfers one (8- or 16-bit) unit of data from the source address to the destination address. The DMAC uses the same data bus used by the CPU. Because the DMAC has higher priority for bus control than the CPU, and because it makes use of a cycle steal method, it can transfer 1 word (16 bits) or 1 byte (8 bits) of data within a very short time after a DMA request is generated. Table 14.1 lists DMAC Specifications, and Figure 14.1 shows the DMAC Block Diagram.

Table 14.1 DMAC Specifications

Item		Specification
Number of channels		4 (cycle steal method)
Transfer memory spaces		• From a given address in a 1 MB space to a fixed address • From a fixed address to a given address in a 1 MB space • From a fixed address to a fixed address
Maximum number of bytes transferred		128 KB (with 16-bit transfers) or 64 KB (with 8-bit transfers)
DMA request sources		50 sources Falling edge of $\overline{INT0}$ to $\overline{INT7}$ (8) Both edge of $\overline{INT0}$ to $\overline{INT7}$ (8) Timer A0 to timer A4 interrupt request (5) Timer B0 to timer B5 interrupt request (6) UART0 to UART4 transmission interrupt request (5) UART0, UART1, UART3, UART4 reception interrupt request (4) UART2 reception/ACK interrupt request (1) IC/OC base timer interrupt request (1) IC/OC channel 0 to IC/OC channel 7 interrupt (8) A/D conversion interrupt request (1) SS0 transmit data register empty interrupt request (1) SS0 receive data register full interrupt request (1) Software trigger (1)
Channel priority		DMA0 > DMA1 > DMA2 > DMA3 (DMA0 takes precedence)
Transfers		8 bits or 16 bits
Transfer address direction		Forward or fixed (The source and destination addresses cannot both be in the forward direction.)
Transfer mode	Single transfer	Transfer is completed when the DMAi transfer counter underflows.
	Repeat transfer	When the DMAi transfer counter underflows, it is reloaded with the value of the DMAi transfer counter reload register, and DMA transfer continues.
DMA interrupt request generation timing		When the DMAi transfer counter underflows
DMA transfer start		Data transfer is initiated each time a DMA request is generated when the DMAE bit in the DMiCON register is 1 (enabled).
DMA transfer stop	Single transfer	• When the DMAE bit is set to 0 (disabled) • After the DMAi transfer counter underflows
	Repeat transfer	When the DMAE bit is set to 0 (disabled)
Reload timing for forward address pointer and DMAi transfer counter		When a data transfer is started after setting the DMAE bit to 1 (enabled), the forward address pointer is reloaded with the value of the SARi or DARi register (whichever is specified to be in the forward direction), and the DMAi transfer counter is reloaded with the value of the DMAi transfer counter reload register.
DMA transfer cycles		Minimum 3 cycles between SFR and internal RAM

i = 0 to 3

Note:

1. The selectable sources of DMA requests differ for each channel.

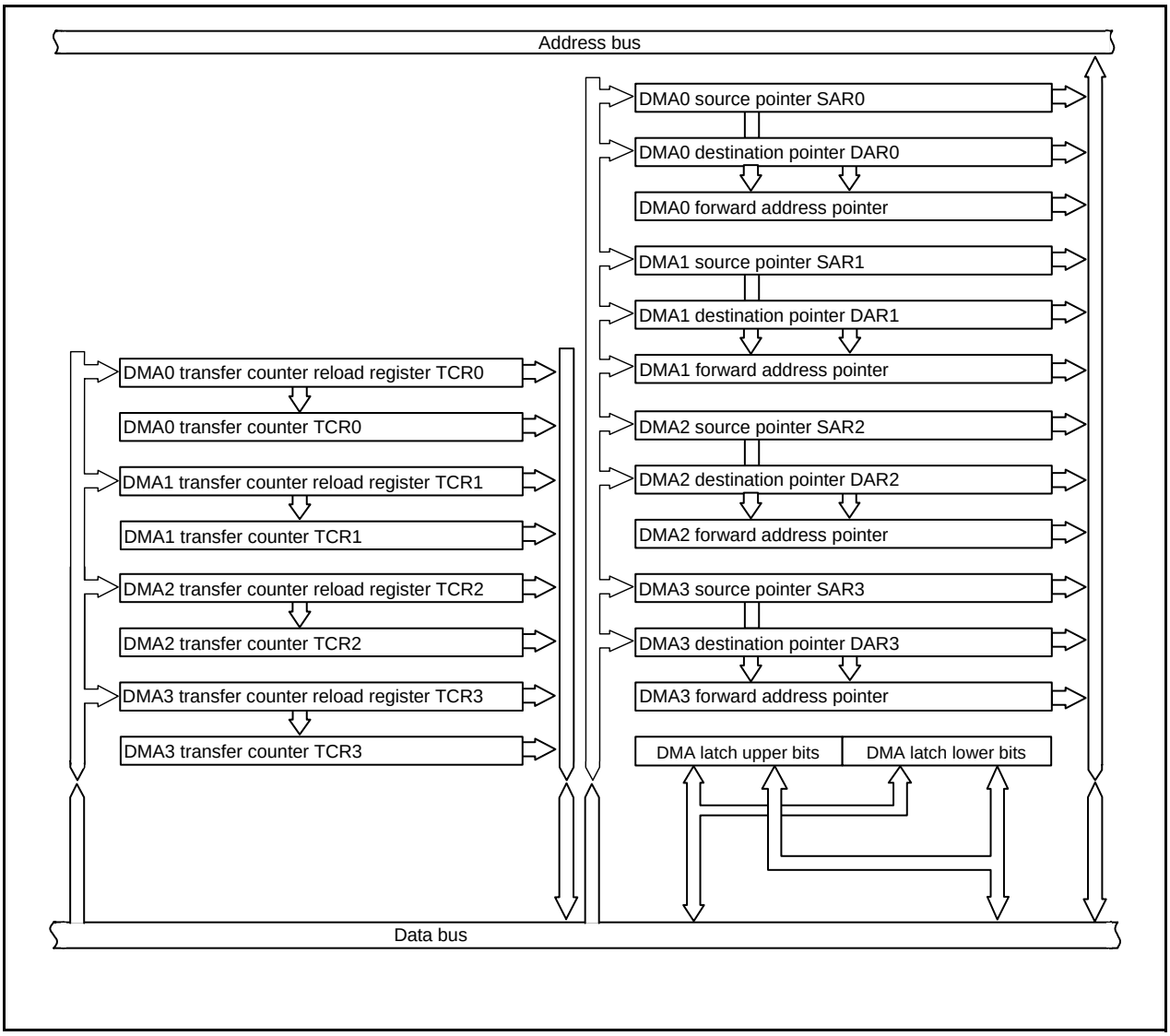


Figure 14.1 DMAC Block Diagram

14.2 Registers

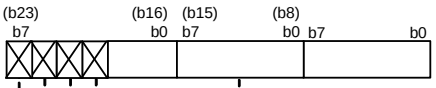
Table 14.2 lists Registers. Do not access these registers using the DMAC.

Table 14.2 Registers

Address	Register	Symbol	Reset Value
0180h	DMA0 Source Pointer	SAR0	XXh
0181h			XXh
0182h			0Xh
0184h	DMA0 Destination Pointer	DAR0	XXh
0185h			XXh
0186h			0Xh
0188h	DMA0 Transfer Counter	TCR0	XXh
0189h			XXh
018Ch	DMA0 Control Register	DM0CON	0000 0X00b
0190h	DMA1 Source Pointer	SAR1	XXh
0191h			XXh
0192h			0Xh
0194h	DMA1 Destination Pointer	DAR1	XXh
0195h			XXh
0196h			0Xh
0198h	DMA1 Transfer Counter	TCR1	XXh
0199h			XXh
019Ch	DMA1 Control Register	DM1CON	0000 0X00b
01A0h	DMA2 Source Pointer	SAR2	XXh
01A1h			XXh
01A2h			0Xh
01A4h	DMA2 Destination Pointer	DAR2	XXh
01A5h			XXh
01A6h			0Xh
01A8h	DMA2 Transfer Counter	TCR2	XXh
01A9h			XXh
01ACh	DMA2 Control Register	DM2CON	0000 0X00b
01B0h	DMA3 Source Pointer	SAR3	XXh
01B1h			XXh
01B2h			0Xh
01B4h	DMA3 Destination Pointer	DAR3	XXh
01B5h			XXh
01B6h			0Xh
01B8h	DMA3 Transfer Counter	TCR3	XXh
01B9h			XXh
01BCh	DMA3 Control Register	DM3CON	0000 0X00b
0390h	DMA2 Source Select Register	DM2SL	00h
0392h	DMA3 Source Select Register	DM3SL	00h
0398h	DMA0 Source Select Register	DM0SL	00h
039Ah	DMA1 Source Select Register	DM1SL	00h

14.2.1 DMAi Source Pointer (SARi) (i = 0 to 3)

DMAi Source Pointer (i = 0 to 3)



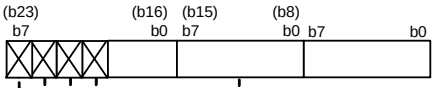
Symbol	Address	Reset Value
SAR0	0182h to 0180h	0X XXXXh
SAR1	0192h to 0190h	0X XXXXh
SAR2	01A2h to 01A0h	0X XXXXh
SAR3	01B2h to 01B0h	0X XXXXh

Function	Setting Range	RW
Set the transfer source	00000h to FFFFFh	RW
No register bits. If necessary, set to 0. The read value is 0		—

If the DSD bit in the DMiCON register is 0 (fixed), write to SARi register when the DMAE bit in the DMiCON register is 0 (DMA disabled).
If the DSD bit is 1 (forward direction), this register can be written to at any time.
If the DSD bit is 1 and the DMAE bit is 1 (DMA enabled), the DMAi forward address pointer can be read from this register. Otherwise, the value written to it can be read.
The forward address pointer increments when a DMA request is accepted.

14.2.2 DMAi Destination Pointer (DARi) (i = 0 to 3)

DMAi Destination Pointer (i = 0 to 3)



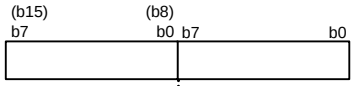
Symbol	Address	Reset Value
DAR0	0186h to 0184h	0X XXXXh
DAR1	0196h to 0194h	0X XXXXh
DAR2	01A6h to 01A4h	0X XXXXh
DAR3	01B6h to 01B4h	0X XXXXh

Function	Setting Range	RW
Set the transfer destination address	00000h to FFFFFh	RW
No register bits. If necessary, set to 0. The read value is 0		—

If the DAD bit in the DMiCON register is 0 (fixed), write to the DARi register when the DMAE bit in the DMiCON register is 0 (DMA disabled).
If the DAD bit is 1 (forward direction), this register can be written to at any time.
If the DAD bit is 1 and the DMAE bit is 1 (DMA enabled), the DMAi forward address pointer can be read from this register. Otherwise, the value written to it can be read.
The forward address pointer increments when a DMA request is accepted.

14.2.3 DMAi Transfer Counter (TCRi) (i = 0 to 3)

DMAi Transfer Counter (i = 0 to 3)



Symbol	Address	Reset Value
TCR0	0189h to 0188h	Undefined
TCR1	0199h to 0198h	Undefined
TCR2	01A9h to 01A8h	Undefined
TCR3	01B9h to 01B8h	Undefined

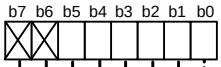
Function	Setting Range	RW
Set the number of transfers minus 1.	0000h to FFFFh	RW

The value written in the TCRi register is stored in the DMAi transfer counter reload register.
The DMAi transfer counter reload register value is transferred to the DMAi transfer counter in either of the following cases:

- The DMAE bit in the DMiCON register is set to 1 (DMA enabled) (single transfer mode, repeat transfer mode).
- The DMAi transfer counter underflows (repeat transfer mode).

14.2.4 DMAi Control Register (DMiCON) (i = 0 to 3)

DMAi Control Register (i = 0 to 3)



Symbol	Address	Reset Value
DM0CON	018Ch	0000 0X00b
DM1CON	019Ch	0000 0X00b
DM2CON	01ACh	0000 0X00b
DM3CON	01BCh	0000 0X00b

Bit Symbol	Bit Name	Function	RW
DMBIT	Transfer unit bit select bit	0 : 16 bits 1 : 8 bits	RW
DMASL	Repeat transfer mode select bit	0 : Single transfer 1 : Repeat transfer	RW
DMAS	DMA request bit	0 : DMA not requested 1 : DMA requested	RW
DMAE	DMA enable bit	0 : DMA disabled 1 : DMA enabled	RW
DSD	Source address direction select bit	0 : Fixed 1 : Forward	RW
DAD	Destination address direction select bit	0 : Fixed 1 : Forward	RW
— (b7-b6)	No register bits. If necessary, set to 0. The read value is 0		—

DMAS (DMA request bit) (b2)

Conditions to become 0:

- Set the bit to 0.
- Start data transfer

Condition to become 1:

- Set the bit to 1.

DMAE (DMA enable bit) (b3)

Conditions to become 0:

- Set the bit to 0.
- The DMA transfer counter underflows (single transfer mode).

Condition to become 1:

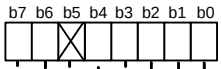
- Set the bit to 1.

DSD (Source address direction select bit) (b4)
DAD (Destination address direction select bit) (b5)

Set the DAD bit and/or DSD bit to 0 (address direction fixed).

14.2.5 DMAi Source Select Register (DMiSL) (i = 0 to 3)

DMAi Source Select Register (i = 0 to 3)



Symbol	Address	Reset Value
DM0SL	0398h	00h
DM1SL	039Ah	00h
DM2SL	0390h	00h
DM3SL	0392h	00h

Bit Symbol	Bit Name	Function	RW
DSEL0	DMA request source select bit	See the bit explanation below.	RW
DSEL1			RW
DSEL2			RW
DSEL3			RW
DSEL4			RW
— (b5)	No register bit. If necessary, set to 0. The read value is undefined.		—
DMS	DMA request source expansion select bit	0: Basic request source 1: Extended request source	RW
DSR	Software DMA request bit	A DMA request is generated by setting this bit to 1 when the DMS bit is 0 (basic source) and bits DSEL4 to DSEL0 are 00001b (software trigger). The read value is 0.	RW

DSEL4-DSEL0 (DMA request source select bit) (b4-b0)

The DMAi request sources can be selected by a combination of the DMS bit and bits DSEL4 to DSEL0 in the manner shown in Table 14.3 to Table 14.6. These tables list the DMAi request sources.

Table 14.3 Sources of DMA Request (DMA0)

DSEL4 to DSEL0	DMS is 0 (Basic Source of Request)	DMS is 1 (Expanded Source of Request)
0 0 0 0 0 b	Falling edge of the $\overline{\text{INT0}}$ pin	IC/OC base timer
0 0 0 0 1 b	Software trigger	–
0 0 0 1 0 b	Timer A0	IC/OC channel 0
0 0 0 1 1 b	Timer A1	IC/OC channel 1
0 0 1 0 0 b	Timer A2	–
0 0 1 0 1 b	Timer A3	–
0 0 1 1 0 b	Timer A4	Both edges of the $\overline{\text{INT0}}$ pin
0 0 1 1 1 b	Timer B0	Timer B3
0 1 0 0 0 b	Timer B1	Timer B4
0 1 0 0 1 b	Timer B2	Timer B5
0 1 0 1 0 b	UART0 transmission	IC/OC channel 2
0 1 0 1 1 b	UART0 reception	IC/OC channel 3
0 1 1 0 0 b	UART2 transmission	IC/OC channel 4
0 1 1 0 1 b	UART2 reception	IC/OC channel 5
0 1 1 1 0 b	A/D converter	IC/OC channel 6
0 1 1 1 1 b	UART1 transmission	IC/OC channel 7
1 0 0 0 0 b	UART1 reception	Falling edge of the $\overline{\text{INT4}}$ pin
1 0 0 0 1 b	–	Both edges of the $\overline{\text{INT4}}$ pin
1 0 0 1 0 b	–	SS0 receive data register full
1 0 0 1 1 b	UART4 transmission	SS0 transmit data register empty
1 0 1 0 0 b	UART4 reception	–
1 0 1 0 1 b	UART3 transmission	–
1 0 1 1 0 b	UART3 reception	–
1 0 1 1 1 b	–	–
1 1 X X X b	–	–

X: 0 or 1 –: Do not set.

Table 14.4 Source of DMA Request (DMA1)

DSEL4 to DSEL0	DMS = 0 (Basic Source of Request)	DMS = 1 (Expanded Source of Request)
0 0 0 0 0 b	Falling edge of the $\overline{\text{INT1}}$ pin	IC/OC base timer
0 0 0 0 1 b	Software trigger	–
0 0 0 1 0 b	Timer A0	IC/OC channel 0
0 0 0 1 1 b	Timer A1	IC/OC channel 1
0 0 1 0 0 b	Timer A2	–
0 0 1 0 1 b	Timer A3	–
0 0 1 1 0 b	Timer A4	–
0 0 1 1 1 b	Timer B0	Both edges of the $\overline{\text{INT1}}$ pin
0 1 0 0 0 b	Timer B1	–
0 1 0 0 1 b	Timer B2	–
0 1 0 1 0 b	UART0 transmission	IC/OC channel 2
0 1 0 1 1 b	UART0 reception	IC/OC channel 3
0 1 1 0 0 b	UART2 transmission	IC/OC channel 4
0 1 1 0 1 b	UART2 reception/ACK2	IC/OC channel 5
0 1 1 1 0 b	A/D converter	IC/OC channel 6
0 1 1 1 1 b	UART1 reception	IC/OC channel 7
1 0 0 0 0 b	UART1 transmission	Falling edge of the $\overline{\text{INT5}}$ pin
1 0 0 0 1 b	–	Both edges of the $\overline{\text{INT5}}$ pin
1 0 0 1 0 b	–	SS0 receive data register full
1 0 0 1 1 b	UART4 transmission	SS0 transmit data register empty
1 0 1 0 0 b	UART4 reception4	–
1 0 1 0 1 b	UART3 transmission	–
1 0 1 1 0 b	UART3 reception	–
1 0 1 1 1 b	–	–
1 1 X X X b	–	–

X: 0 or 1 – Do not set.

Table 14.5 Sources of DMA Request (DMA2)

DSEL4 to DSEL0	DMS is 0 (Basic Source of Request)	DMS is 1 (Expanded Source of Request)
0 0 0 0 0 b	Falling edge of the $\overline{\text{INT2}}$ pin	IC/OC base timer
0 0 0 0 1 b	Software trigger	–
0 0 0 1 0 b	Timer A0	IC/OC channel 0
0 0 0 1 1 b	Timer A1	IC/OC channel 1
0 0 1 0 0 b	Timer A2	–
0 0 1 0 1 b	Timer A3	–
0 0 1 1 0 b	Timer A4	Both edges of the $\overline{\text{INT2}}$ pin
0 0 1 1 1 b	Timer B0	Timer B3
0 1 0 0 0 b	Timer B1	Timer B4
0 1 0 0 1 b	Timer B2	Timer B5
0 1 0 1 0 b	UART0 transmission	IC/OC channel 2
0 1 0 1 1 b	UART0 reception	IC/OC channel 3
0 1 1 0 0 b	UART2 transmission	IC/OC channel 4
0 1 1 0 1 b	UART2 reception	IC/OC channel 5
0 1 1 1 0 b	A/D converter	IC/OC channel 6
0 1 1 1 1 b	UART1 transmission	IC/OC channel 7
1 0 0 0 0 b	UART1 reception	Falling edge of the $\overline{\text{INT6}}$ pin
1 0 0 0 1 b	–	Both edges of the $\overline{\text{INT6}}$ pin
1 0 0 1 0 b	–	SS0 receive data register full
1 0 0 1 1 b	UART4 transmission	SS0 transmit data register empty
1 0 1 0 0 b	UART4 reception	–
1 0 1 0 1 b	UART3 transmission	–
1 0 1 1 0 b	UART3 reception	–
1 0 1 1 1 b	–	–
1 1 X X X b	–	–

X: 0 or 1 – Do not set.

Table 14.6 Source of DMA Request (DMA3)

DSEL4 to DSEL0	DMS is 0 (Basic Source of Request)	DMS is 1 (Expanded Source of Request)
0 0 0 0 0 b	Falling edge of the $\overline{\text{INT3}}$ pin	IC/OC base timer
0 0 0 0 1 b	Software trigger	–
0 0 0 1 0 b	Timer A0	IC/OC channel 0
0 0 0 1 1 b	Timer A1	IC/OC channel 1
0 0 1 0 0 b	Timer A2	–
0 0 1 0 1 b	Timer A3	–
0 0 1 1 0 b	Timer A4	–
0 0 1 1 1 b	Timer B0	Both edges of the $\overline{\text{INT3}}$ pin
0 1 0 0 0 b	Timer B1	–
0 1 0 0 1 b	Timer B2	–
0 1 0 1 0 b	UART0 transmission	IC/OC channel 2
0 1 0 1 1 b	UART0 reception	IC/OC channel 3
0 1 1 0 0 b	UART2 transmission	IC/OC channel 4
0 1 1 0 1 b	UART2 reception/ACK2	IC/OC channel 5
0 1 1 1 0 b	A/D converter	IC/OC channel 6
0 1 1 1 1 b	UART1 reception	IC/OC channel 7
1 0 0 0 0 b	UART1 transmission	Falling edge of the $\overline{\text{INT7}}$ pin
1 0 0 0 1 b	–	Both edges of the $\overline{\text{INT7}}$ pin
1 0 0 1 0 b	–	SS0 receive data register full
1 0 0 1 1 b	UART4 transmission	SS0 transmit data register empty
1 0 1 0 0 b	UART4 reception	–
1 0 1 0 1 b	UART3 transmission	–
1 0 1 1 0 b	UART3 reception	–
1 0 1 1 1 b	–	–
1 1 X X X b	–	–

X: 0 or 1 – Do not set.

14.3 Operations

14.3.1 DMA Enabled

When data transfer starts after setting the DMAE bit in the DMiCON register to 1 (enabled), the DMAC operates as listed below (i = 0 to 3). If 1 is written to the DMAE bit when it is already set to 1, the DMAC also performs the following operations.

- The forward address pointer is reloaded with the SARi register value when the DSD bit in the DMiCON register is 1 (forward), or the DARi register value when the DAD bit in the DMiCON register is 1 (forward).
- The DMAi transfer counter is reloaded with the DMAi transfer counter reload register value.

14.3.2 DMA Request

The DMAC can generate a DMA request as triggered by the request source that is selected with the DMS bit and bits DSEL4 to DSEL0 in the DMiSL register (i = 0 to 3) on each channel. Table 14.7 lists the Timing at Which the DMAS Bit Value Changes.

When a DMA request is generated, the DMAS bit becomes 1 (DMA requested) regardless of the DMAE bit status. If the DMAE bit is 1 (enabled) when this occurs, the DMAS bit becomes 0 (DMA not requested) immediately before a data transfer starts. This bit cannot be set to 1 by a program (writing 1 has no effect).

If the DMAE bit is 1, data transfers start immediately after a DMA request is generated, so the DMAS bit in almost all cases is 0 when read in a program. Read the DMAE bit to determine whether the DMAC is enabled. When a DMA request transfer cycle is shorter than the DMA transfer cycle, the number of transfer requests and the number of transfers do not match.

When a peripheral function is selected as the DMA source, relations with the interrupt control registers are as follows:

- DMA transfers are not affected by the I flag or interrupt control registers. DMA requests are always accepted even when interrupt requests are not accepted.
- The IR bit in the interrupt control register retains its value when a DMA transfer is accepted.

Table 14.7 Timing at Which the DMAS Bit Value Changes

DMA Source	DMAS Bit in the DMiCON Register	
	Timing at which the bit becomes 1	Timing at which the bit becomes 0
Software trigger	When the DSR bit in the DMiSL register is set to 1.	• Immediately before a data transfer starts • When set to 0 by a program
External source	When an input edge of pins $\overline{INT0}$ to $\overline{INT7}$ matches with what is selected by setting bits DSEL4 to DSEL0 and DMS in the DMiSL register.	
Peripheral function	When an interrupt request is generated by the peripheral function selected by setting the DMS bit and bits DSEL4 to DSEL0 in the DMiSL register.(If the IR bit in an interrupt control register is 0, the timing is when the IR bit becomes 1.)	

i = 0 to 3

14.3.3 Transfer Cycles

A transfer cycle is composed of a bus cycle to read data from a source address (source read), and a bus cycle to write data to a destination address (destination write). The number of read and write bus cycles varies with the source and destination addresses.

Figure 14.2 shows Source Read Cycle Example. For convenience, the destination write cycle is shown as one bus cycle and the source read cycles for the different conditions are shown. In reality, the destination write cycle is subject to the same conditions as the source read cycle, with the transfer cycle changing accordingly. When calculating transfer cycles, take into consideration each condition for the source read and the destination write cycle. For example, when data is transferred in 16-bit units, and the source and destination addresses are both odd addresses ((2) in Figure 14.2), two source read bus cycles and two destination write bus cycles are required.

14.3.3.1 Effect of Source and Destination Addresses

When a 16-bit unit of data is transferred and the source address starts with an odd address, the source read cycle increments by one bus cycle, compared to a source address starting with an even address.

When a 16-bit unit of data is transferred and the destination address starts with an odd address, the destination write cycle increments by one bus cycle, compared to a destination address starting with an even address.

14.3.3.2 Effect of Software Wait

For memory or SFR accesses in which one or more software wait states are inserted, the number of bus cycles required increases by an amount equal to the number of software wait states.

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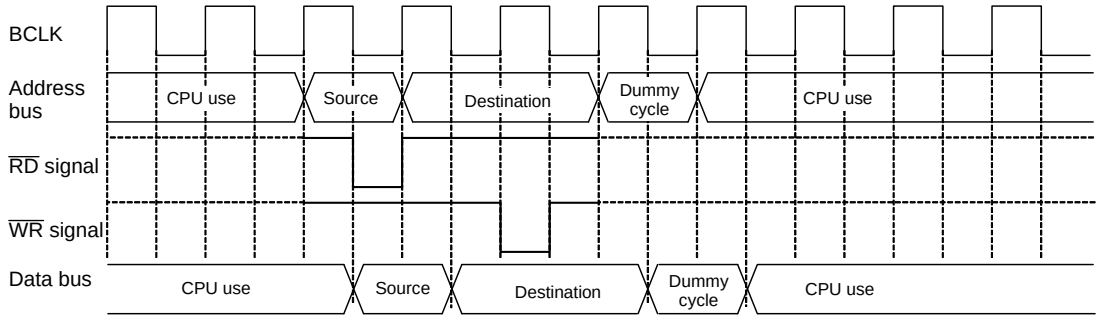
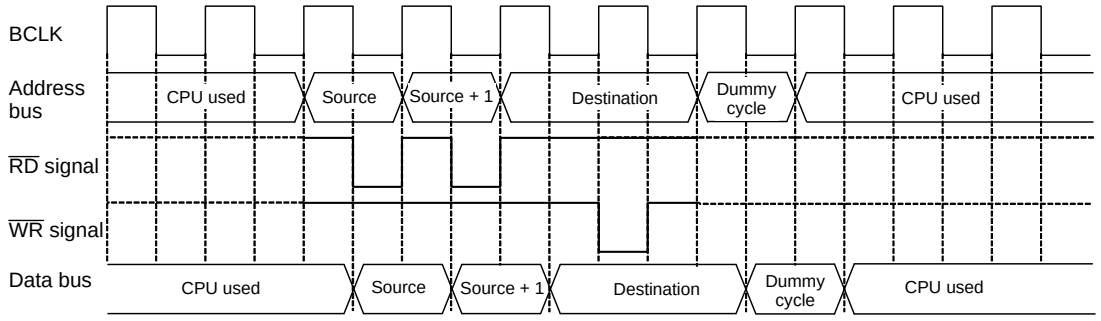
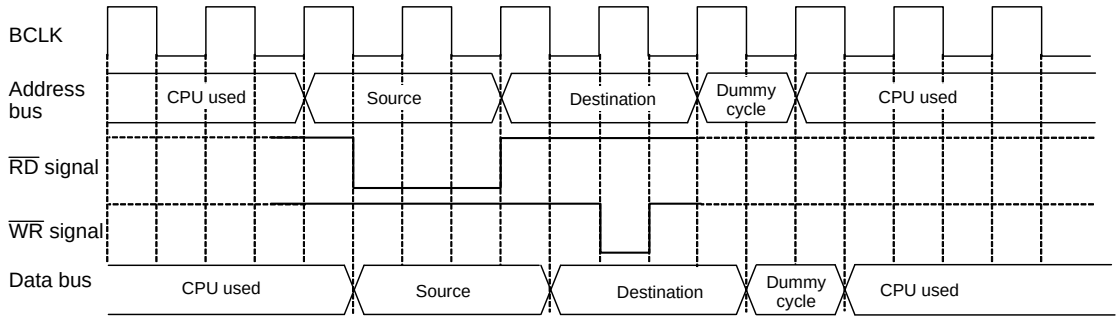
(1) Transfers are performed in 8-bit or 16-bit units, and the transfer source is an even address.



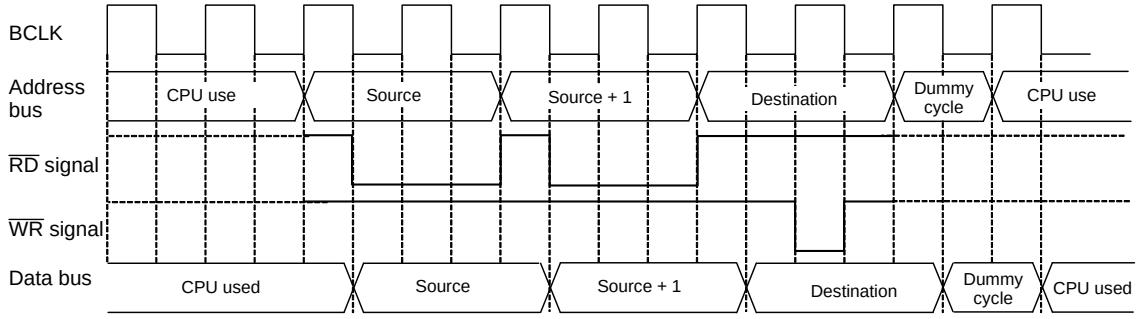
(2) Transfers are performed in 16-bit units, and the transfer source is an odd address.



(3) Conditions listed in (1) with one wait inserted in the source read cycle.



(4) Conditions listed in (2) with one wait inserted in the source read cycle.



Note:
1. The same timing changes occur with the respective conditions at the destination as at the source.

Figure 14.2 Source Read Cycle Example

14.3.4 DMAC Transfer Cycles

The formula for calculating the number of DMAC transfer cycles is shown below.

Number of transfer cycles per transfer unit = Number of read cycles × j + Number of write cycles × k

Table 14.8 DMAC Transfer Cycles

Transfer Unit	Access Address	Single-Chip Mode	
		Number of Read Cycles	Number of Write Cycles
8-bit transfers (DMBIT = 1)	Even	1	1
	Odd	1	1
16-bit transfers (DMBIT = 0)	Even	1	1
	Odd	2	2

DMBIT: Bit in the DMiCON register (i = 0 to 3)

Table 14.9 Coefficients j and k

	Internal Area		
	Internal ROM, RAM		SFR
	No waits inserted	Wait inserted	one wait inserted
j	1	2	2
k	1	2	2

14.3.5 Single Transfer Mode

In single transfer mode, the transfer stops when the DMAi transfer counter underflows. Figure 14.3 shows an Operation Example in Single Transfer Mode.

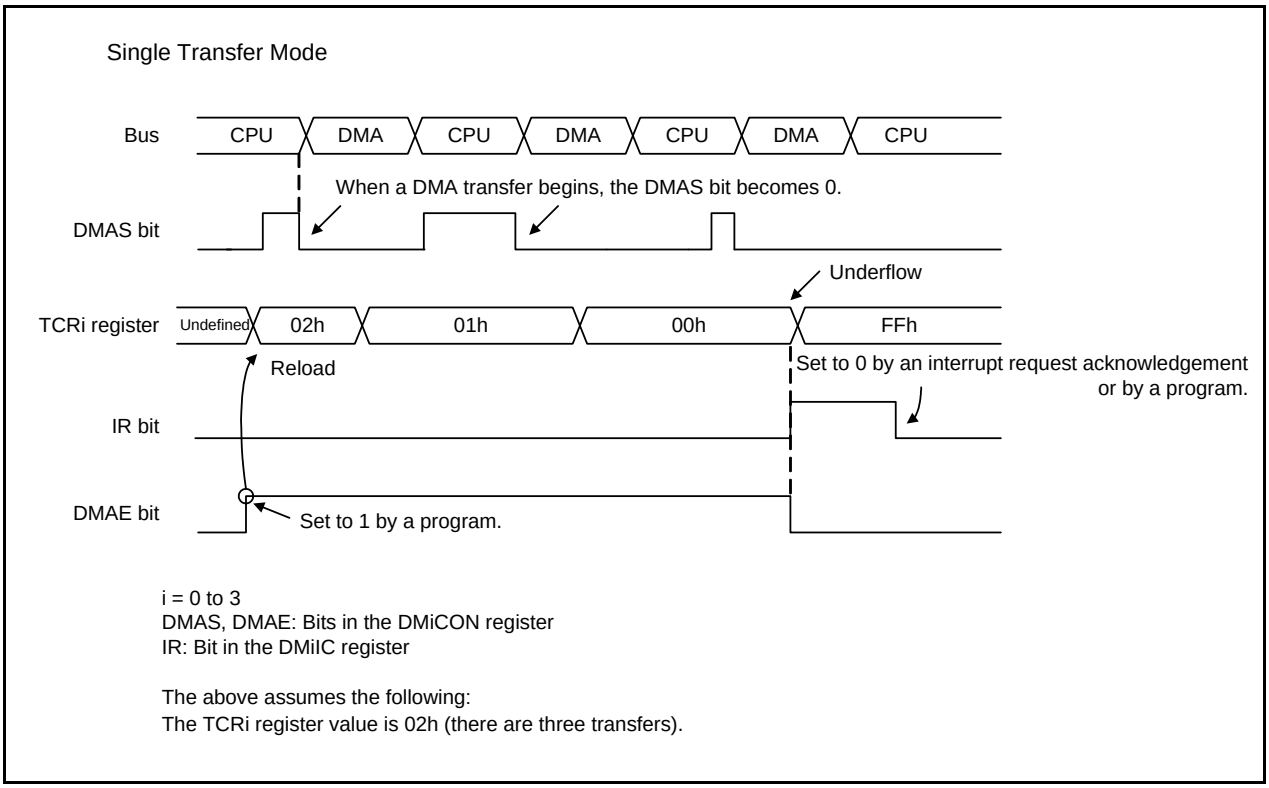


Figure 14.3 Operation Example in Single Transfer Mode

14.3.6 Repeat Transfer Mode

In repeat transfer mode, when the DMAi transfer counter underflows, it is reloaded with the value of the DMAi transfer counter reload register and DMA transfer continues. Figure 14.4 shows an Operation Example in Repeat Transfer Mode.

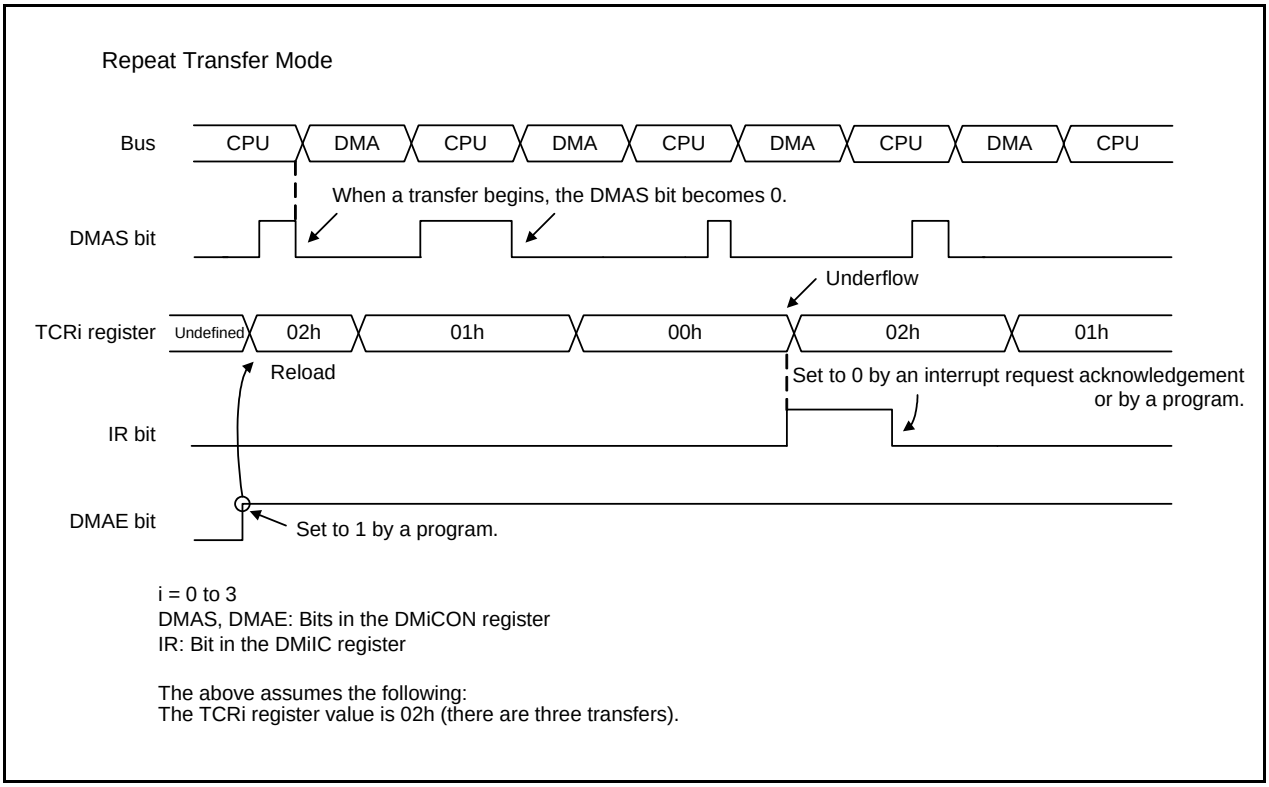


Figure 14.4 Operation Example in Repeat Transfer Mode

14.3.7 Channel Priority and DMA Transfer Timing

If multiple channels among DMA0 to DMA3 are enabled and DMA transfer request signals are detected as active in the same sampling period (one period from a falling edge to the next falling edge of BCLK), the DMAS bit on each channel becomes 1 (DMA requested) at the same time. In this case, the DMA requests are arbitrated according to the following channel priority: DMA0 > DMA1 > DMA2 > DMA3. DMAC operation when DMA0 and DMA1 requests are detected as active in the same sampling period is described below. Figure 14.5 shows an example of DMA Transfer Initiated by External Sources.

In Figure 14.5, as DMA0 and DMA1 requests are generated simultaneously, the higher channel prioritized DMA0 is received first, and data transfer starts. After one DMA0 transfer is completed, the bus access privilege is returned to the CPU. When the CPU has completed one bus access, a DMA1 transfer starts. After one DMA1 transfer is completed, the bus access privilege is again returned to the CPU.

In addition, DMA requests cannot increment since each channel has one DMAS bit. Therefore, when DMA requests, such as DMA1 in Figure 14.5, occur more than once, the DMAS bit is set to 0 after receiving the bus access privilege. The bus access privilege is returned to the CPU when one transfer is completed.

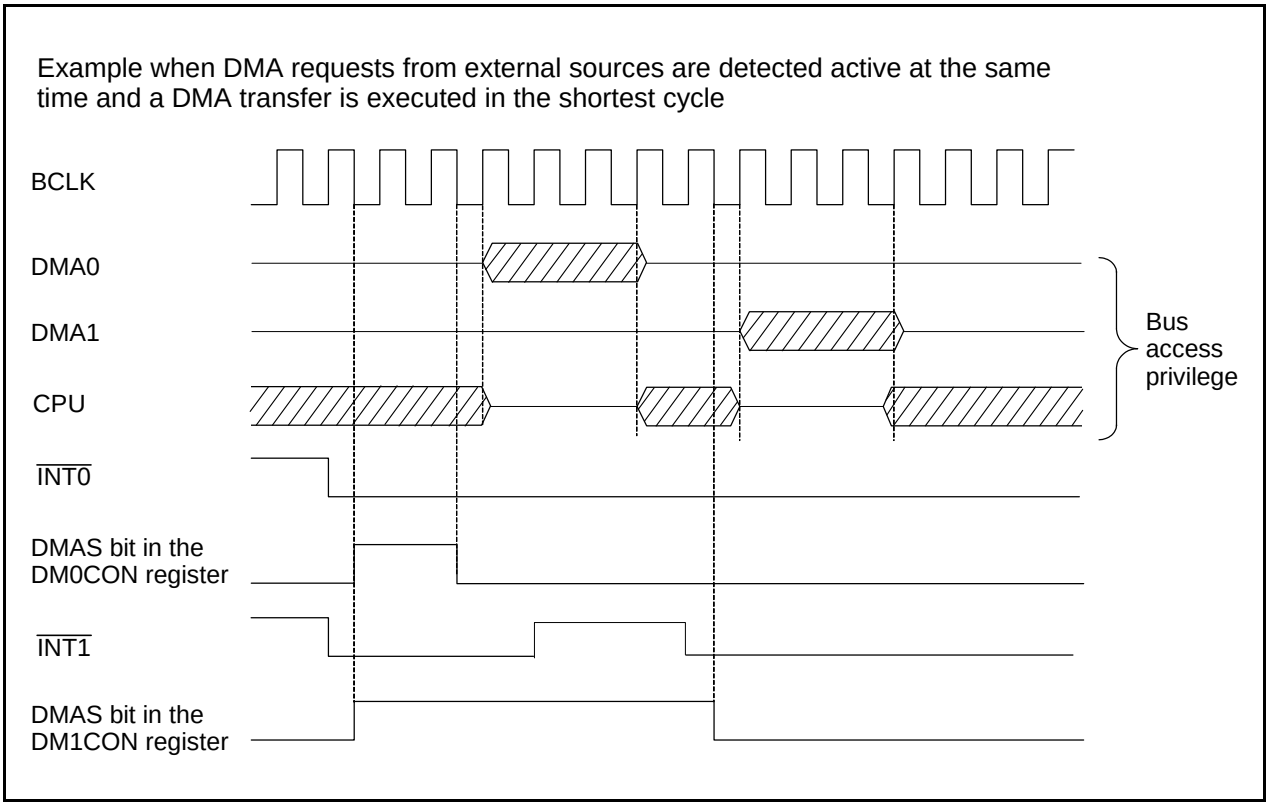


Figure 14.5 DMA Transfer Initiated by External Sources

14.4 Interrupts

Refer to operation examples for interrupt request generation timing.
For details on interrupt control, refer to 12.7 “Interrupt Control”.

Table 14.10 DMAC Interrupt Related Registers

Address	Register	Symbol	Reset Value
004Bh	DMA0 Interrupt Control Register	DM0IC	XXXX X000b
004Ch	DMA1 Interrupt Control Register	DM1IC	XXXX X000b
0069h	DMA2 Interrupt Control Register	DM2IC	XXXX X000b
006Ah	DMA3 Interrupt Control Register	DM3IC	XXXX X000b

When the DMS bit or bits DSEL4 to DSEL0 in the DMiSL register are changed, the DMAS bit in the DMiCON sometimes becomes 1 (DMA requested) (i = 0 to 3). Therefore, set the DMAS bit to 0 (DMA not requested) after the DMS bit or bits DSEL4 to DSEL0 in the DMiSL register are changed. Refer to 12.13 “Notes on Interrupts” for more details.

14.5 Notes on DMAC

14.5.1 Write to the DMAE Bit in the DMiCON Register (i = 0 to 3)

(Technical update number: TN-M16C-92-0306)
When both of the following conditions are met, follow steps (1) and (2) below.

Conditions

- Write 1 (DMAi is in active state) to the DMAE bit when it is 1.
- A DMA request may be generated simultaneously when writing to the DMAE bit.

Steps

(1) Set bits DMAE and DMAS in the DMiCON register to 1 simultaneously. (1)
(2) Make sure the DMAi circuit is in an initialized state (2) by a program.
If DMAi is not in an initialized state, repeat these two steps.

Notes:

1. The DMAS bit does not change even if set to 1. However, it becomes 0 when set to 0 (DMA not requested). Therefore, when writing to the DMiCON register to set the DMAE bit to 1, set the value to be written to the DMAS bit to 1 to retain its state immediately before writing.
Similarly, when writing to the DMAE bit with a read-modify-write instruction, set the DMAS bit to 1 to retain the DMA request that was generated while executing the instruction.
2. Read the TCRi register to verify whether DMAi is in an initialized state.
If the read value is equal to the value that was written to the TCRi register before the DMA transfer started, DMAi is in an initialized state. When a DMA request is generated after writing to the DMAE bit, the read value is a value written to the TCRi register minus 1. If the read value is a value in the middle of a transfer, DMAi is not in an initialized state.

14.5.2 Changing the DMA Request Source

When the DMS bit or any of bits from DSEL4 to DSEL0 in the DMiSL register is changed, the DMAS bit in the DMiCON sometimes becomes 1 (DMA requested). Set the DMAS bit to 0 (DMA not requested) after changing the DMS bit or bits DSEL4 to DSEL0 in the DMiSL register.

15. Timer A

15.1 Introduction

Timers A consists of timers A0 to A4. Each timer operates independently of the others. Table 15.1 lists Timer A Specifications, Table 15.2 lists Differences in Timer A Mode, Figure 15.1 shows Timer A and B Count Sources, Figure 15.2 shows Timer A Configuration, Figure 15.3 shows Timer A Block Diagram, and Table 15.3 lists I/O Ports.

Table 15.1 Timer A Specifications

Item	Specification
Configuration	16-bit timer × 5
Operating modes	• Timer mode The timer counts an internal count source. • Event counter mode The timer counts pulses from an external device, or overflows and underflows of other timers. • One-shot timer mode The timer outputs a single pulse before it reaches the count 0000h. • Pulse width modulation mode (PWM mode) The timer outputs pulses of given width and cycle successively. • Programmable output mode The timer outputs a given pulse width of a high/low level signal (timers A1, A2, and A4).
Interrupt sources	Overflow/underflow × 5

Table 15.2 Differences in Timer A Mode

Item	Timer				
	A0	A1	A2	A3	A4
Event counter mode (two-phase pulse signal processing)	No	No	Yes	Yes	Yes
Programmable output mode	No	Yes	Yes	No	Yes

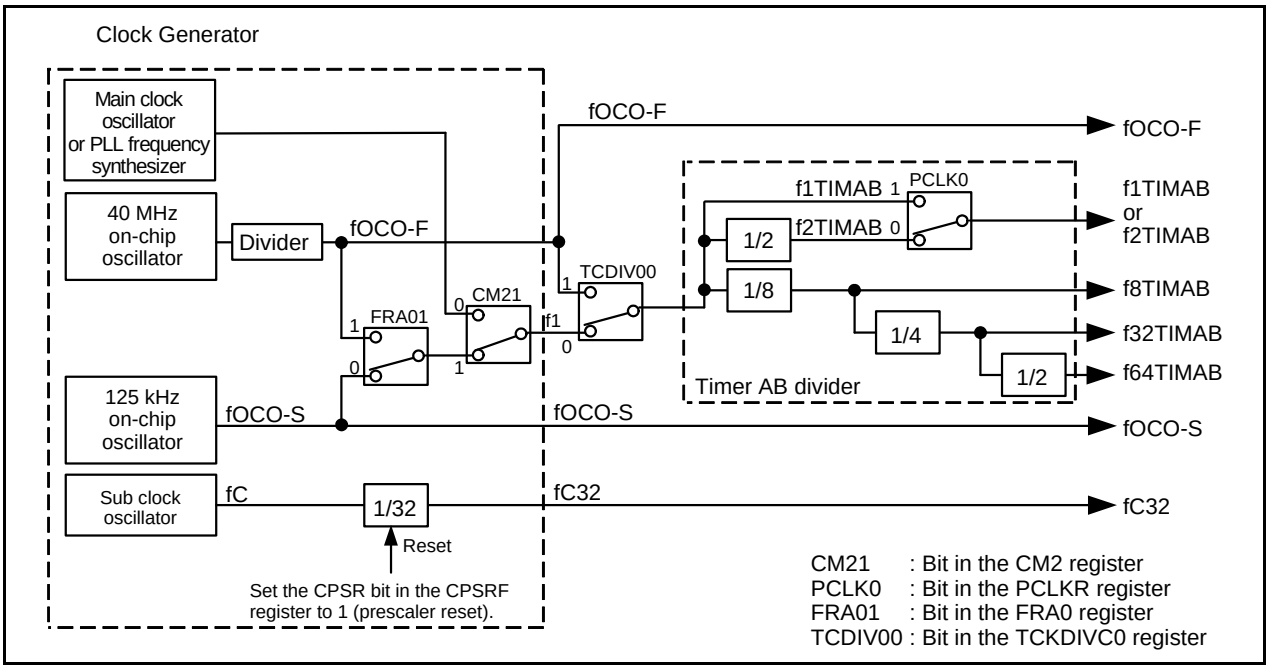
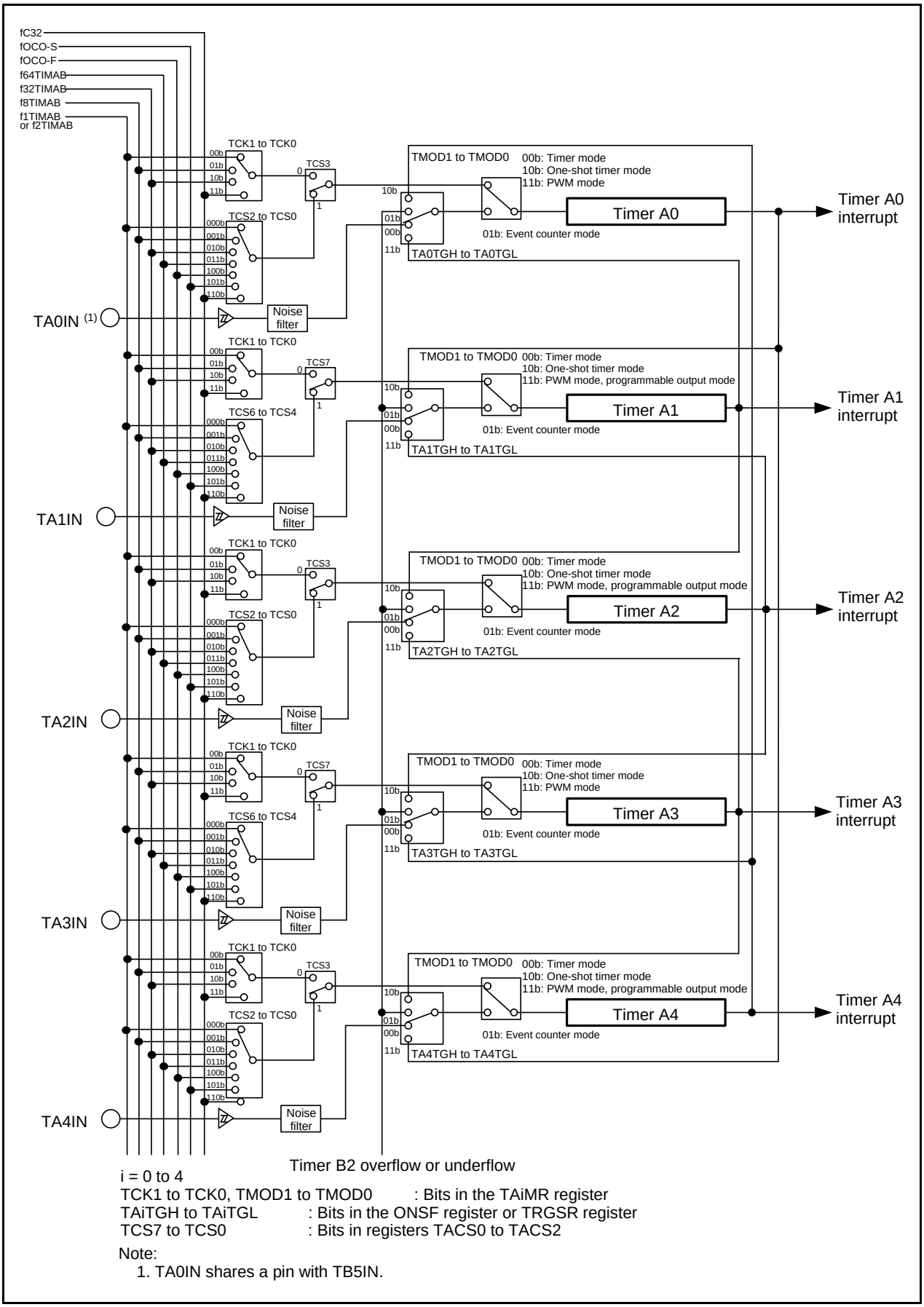


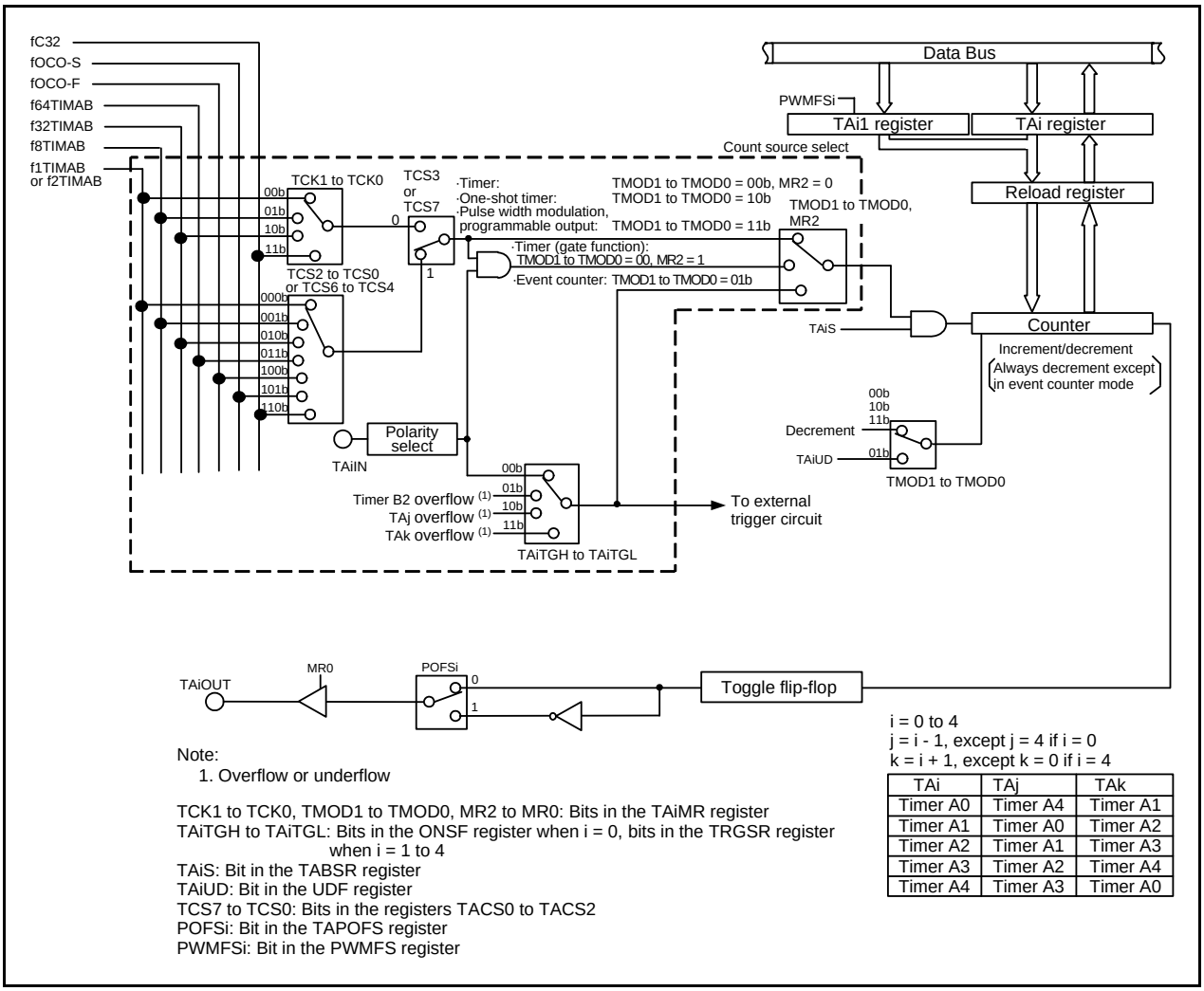
Figure 15.1 Timer A and B Count Sources



i = 0 to 4
TCK1 to TCK0, TMOD1 to TMOD0 : Bits in the TAiMR register
TAiTGH to TAiTGL : Bits in the ONSF register or TRGSR register
TCS7 to TCS0 : Bits in registers TACS0 to TACS2

Note:
1. TA0IN shares a pin with TB5IN.

Figure 15.2 Timer A Configuration



TAi	TAj	TAk
Timer A0	Timer A4	Timer A1
Timer A1	Timer A0	Timer A2
Timer A2	Timer A1	Timer A3
Timer A3	Timer A2	Timer A4
Timer A4	Timer A3	Timer A0

Figure 15.3 Timer A Block Diagram

Table 15.3 I/O Ports

Pin Name	I/O	Function
TAiIN	Input (1)	Gate input (timer mode) Count source input (event counter mode) Two-phase signal input (event counter mode (two-phase pulse signal processing)) Trigger input (one-shot timer mode, PWM mode, programmable output mode)
TAiOUT	Output	Pulse output (timer mode, event counter mode, one-shot timer mode, PWM mode, and programmable output mode)
	Input (1)	Two-phase pulse input (event counter mode (two-phase pulse signal processing))
ZP	Input (1)	Z-phase (counter initialization) input (event counter mode (two-phase pulse signal processing))

i = 0 to 4; however, i = 2, 3, 4 for two-phase pulse input, and i = 1, 2, 4 in programmable output mode

Note:

1. When using pins TAiIN, TAiOUT, and ZP for input, set the port direction bits sharing pins to 0 (input mode).

15.2 Registers

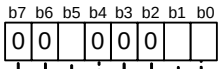
Table 15.4 lists registers associated with timer A.
Set the TCDIV00 bit in the TCKDIVC0 register before setting other registers associated with timer A. After changing the TCDIV00 bit, set other registers associated with timer A again.
Refer to “registers and the setting” in each mode for registers and bit settings.

Table 15.4 Registers

Address	Register	Symbol	Reset Value
0012h	Peripheral Clock Select Register	PCLKR	0000 0011b
0015h	Clock Prescaler Reset Flag	CPSRF	0XXX XXXXb
01CBh	Timer AB Division Control Register 0	TCKDIVC0	0000 X000b
01D0h	Timer A Count Source Select Register 0	TACS0	00h
01D1h	Timer A Count Source Select Register 1	TACS1	00h
01D2h	Timer A Count Source Select Register 2	TACS2	X0h
01D4h	16-bit Pulse Width Modulation Mode Function Select Register	PWMFS	0XX0 X00Xb
01D5h	Timer A Waveform Output Function Select Register	TAPOFS	XXX0 0000b
01D8h	Timer A Output Waveform Change Enable Register	TAOW	XXX0 X00Xb
0302h	Timer A1-1 Register	TA11	XXh
0303h			XXh
0304h	Timer A2-1 Register	TA21	XXh
0305h			XXh
0306h	Timer A4-1 Register	TA41	XXh
0307h			XXh
0320h	Count Start Flag	TABSR	00h
0322h	One-Shot Start Flag	ONSF	00h
0323h	Trigger Select Register	TRGSR	00h
0324h	Increment/Decrement Flag	UDF	00h
0326h	Timer A0 Register	TA0	XXh
0327h			XXh
0328h	Timer A1 Register	TA1	XXh
0329h			XXh
032Ah	Timer A2 Register	TA2	XXh
032Bh			XXh
032Ch	Timer A3 Register	TA3	XXh
032Dh			XXh
032Eh	Timer A4 Register	TA4	XXh
032Fh			XXh
0336h	Timer A0 Mode Register	TA0MR	00h
0337h	Timer A1 Mode Register	TA1MR	00h
0338h	Timer A2 Mode Register	TA2MR	00h
0339h	Timer A3 Mode Register	TA3MR	00h
033Ah	Timer A4 Mode Register	TA4MR	00h

15.2.1 Peripheral Clock Select Register (PCLKR)

Peripheral Clock Select Register



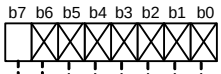
Symbol	Address	Reset Value
PCLKR	0012h	00000011b

Bit Symbol	Bit Name	Function	RW
PCLK0	Timers A, B, S, multi-master I^2C-bus interface clock select bit (clock source for timers A , B, S, dead time timer, and multi-master I^2C-bus interface)	0: f2TIMAB/f2IIC 1: f1TIMAB/f1IIC	RW
PCLK1	SI/O clock select bit (clock source for UART0 to UART4)	0: f2SIO 1: f1SIO	RW
— (b4-b2)	Reserved bits	Set to 0.	RW
PCLK5	Clock output function extension bit	0: Selected by setting bits CM01 and CM00 in the CM0 register 1: Outputs f1	RW
— (b7-b6)	Reserved bits	Set to 0.	RW

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting this register.

15.2.2 Clock Prescaler Reset Flag (CPSRF)

Clock Prescaler Reset Flag

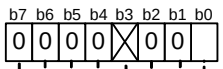


Symbol	Address	Reset Value
CPSRF	0015h	0XXX XXXXb

Bit Symbol	Bit Name	Function	RW
— (b6-b0)	No register bits. If necessary, set to 0. The read values are undefined.		—
CPSR	Clock prescaler reset flag	Setting this bit to 1 initializes the prescaler for the timekeeping clock. (The read value is 0.)	RW

15.2.3 Timer AB Division Control Register 0 (TCKDIVC0)

Timer AB Division Control Register 0



Symbol: TCKDIVC0 | Address: 01CBh | Reset Value: 0000 X000b

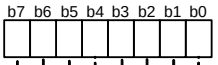
Bit Symbol	Bit Name	Function	RW
TCDIV00	Clock select prior to timer AB division bit	0 : f1 1 : fOCO-F	RW
— (b2-b1)	Reserved bits	Set to 0	RW
— (b3)	No register bit. If necessary, set to 0. The read value is undefined.		—
— (b7-b4)	Reserved bits	Set to 0	RW

TCDIV00 (Clock select prior to timer AB division bit) (b0)

Set the TCDIV00 bit while timers A and B are stopped.
Set the TCDIV00 bit before setting other registers associated with timer A.
After changing the TCDIV00 bit, set other registers associated with timer A again.

15.2.4 Timer A Count Source Select Register i (TACSi) (i = 0 to 2)

Timer A Count Source Select Register 0, Timer A Count Source Select Register 1

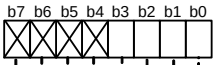


Symbol: TACS0 to TACS1 | Address: 01D0h to 01D1h | Reset Value: 00h

Bit Symbol	Bit Name	Function	RW
TCS0	TAi count source select bit	b2 b1 b0 0 0 0 : f1TIMAB or f2TIMAB 0 0 1 : f8TIMAB 0 1 0 : f32TIMAB 0 1 1 : f64TIMAB 1 0 0 : fOCO-F 1 0 1 : fOCO-S 1 1 0 : fC32 1 1 1 : Do not set	RW
TCS1			RW
TCS2			RW
TCS3	TAi count source option specified bit	0 : TCK0, TCK1 enabled, TCS0 to TCS2 disabled 1 : TCK0, TCK1 disabled, TCS0 to TCS2 enabled	RW
TCS4	TAj count source select bit	b6 b5 b4 0 0 0 : f1TIMAB or f2TIMAB 0 0 1 : f8TIMAB 0 1 0 : f32TIMAB 0 1 1 : f64TIMAB 1 0 0 : fOCO-F 1 0 1 : fOCO-S 1 1 0 : fC32 1 1 1 : Do not set	RW
TCS5			RW
TCS6			RW
TCS7	TAj count source option specified bit	0 : TCK0, TCK1 enabled, TCS4 to TCS6 disabled 1 : TCK0, TCK1 disabled, TCS4 to TCS6 enabled	RW

TACS0 register: i = 0, j = 1 TACS1 register: i = 2, j = 3

Timer A Count Source Select Register 2



Symbol: TACS2 | Address: 01D2h | Reset Value: X0h

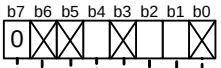
Bit Symbol	Bit Name	Function	RW
TCS0	TA4 count source select bit	b2 b1 b0 0 0 0 : f1TIMAB or f2TIMAB 0 0 1 : f8TIMAB 0 1 0 : f32TIMAB 0 1 1 : f64TIMAB 1 0 0 : fOCO-F 1 0 1 : fOCO-S 1 1 0 : fC32 1 1 1 : Do not set	RW
TCS1			RW
TCS2			RW
TCS3	TA4 count source option specified bit	0 : TCK0 to TCK1 enabled, TCS0 to TCS2 disabled 1 : TCK0 to TCK1 disabled, TCS0 to TCS2 enabled	RW
— (b7-b4)	No register bits. If necessary, set to 0. The read values are undefined.		—

TCS2 to TCS0 (TAi count source select bit) (b2-b0) (i = 0, 2, 4)
TCS6 to TCS4 (TAj count source select bit) (b6-b4) (i = 1, 3)

Select f1TIMAB or f2TIMAB by the PCLK0 bit in the PCLKR register.

15.2.5 16-bit Pulse Width Modulation Mode Function Select Register (PWMFS)

16-bit Pulse Width Modulation Mode Function Select Register



Symbol	Address	Reset Value
PWMFS	01D4h	0XX0 X00Xb

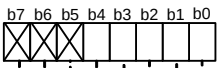
Bit Symbol	Bit Name	Function	RW
— (b0)	No register bit. If necessary, set to 0. The read value is undefined.		—
PWMFS1	Timer A1 programmable output mode select bit	0 : PWM mode 16-bit PWM 1 : Programmable output mode	RW
PWMFS2	Timer A2 programmable output mode select bit	0 : PWM mode 16-bit PWM 1 : Programmable output mode	RW
— (b3)	No register bit. If necessary, set to 0. The read value is undefined.		—
PWMFS4	Timer A4 programmable output mode select bit	0 : PWM mode 16-bit PWM 1 : Programmable output mode	RW
— (b6-b5)	No register bits. If necessary, set to 0. The read value is undefined.		—
— (b7)	Reserved bit	Set to 0	RW

PWMFS1 (Timer A1 programmable output mode select bit) (b1)
PWMFS2 (Timer A2 programmable output mode select bit) (b2)
PWMFS4 (Timer A4 programmable output mode select bit) (b4)

These bits are enabled when bits TMOD1 to TMOD0 in the TAiMR register are 11b (PWM mode or programmable output mode), and the MR3 bit in the TAiMR register is 0 (16-bit PWM mode).

15.2.6 Timer A Waveform Output Function Select Register (TAPOFS)

Timer A Waveform Output Function Select Register



Symbol	Address	Reset Value
TAPOFS	01D5h	XXX0 0000b

Bit Symbol	Bit Name	Function	RW
POFS0	TA0OUT output polar control bit	0 : Output waveform high-level active 1 : Output waveform high-level active (output inverted)	RW
POFS1	TA1OUT output polar control bit		RW
POFS2	TA2OUT output polar control bit		RW
POFS3	TA3OUT output polar control bit		RW
POFS4	TA4OUT output polar control bit		RW
— (b7-b5)	No register bits. If necessary, set to 0. The read value is undefined.		—

15.2.7 Timer A Output Waveform Change Enable Register (TAOW)

Timer A Output Waveform Change Enable Register

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	Reset Value
								TAOW	01D8h	XXX0 X00Xb

Bit Symbol	Bit Name	Function	RW
— (b0)	No register bit. If necessary, set to 0. The read value is undefined.		—
TA1OW	Timer A1 output waveform change enable bit	0 : Change disabled 1 : Change enabled	RW
TA2OW	Timer A2 output waveform change enable bit	0 : Change disabled 1 : Change enabled	RW
— (b3)	No register bit. If necessary, set to 0. The read value is undefined.		—
TA4OW	Timer A4 output waveform change enable bit	0 : Change disabled 1 : Change enabled	RW
— (b7-b5)	No register bits. If necessary, set to 0. The read value is undefined.		—

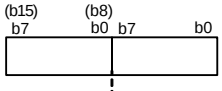
The TAOW register is enabled in programmable output mode.
To change cycles or width of the output waveform, follow the instructions below.

(1)Set the TAiOW bit to 0 (output waveform change disabled). (i = 1, 2, 4)
(2)Write to the TAi register and/or the TAi1 register.
(3)Set the TAiOW bit to 1 (output waveform change enabled).

The updated value is reloaded when the TAiOW bit is 1 (output waveform change enabled) at one cycle before the rising edge of the TAiOUT output (the falling edge when the POFSi bit is 1). The value before the update is reloaded when the TAiOW bit is 0 (output waveform change disabled).

15.2.8 Timer Ai Register (TAi) (i = 0 to 4)

Timer Ai Register (i = 0 to 4)



Symbol	Address	Reset Value
TA0	0327h to 0326h	XXXXh
TA1	0329h to 0328h	XXXXh
TA2	032Bh to 032Ah	XXXXh
TA3	032Dh to 032Ch	XXXXh
TA4	032Fh to 032Eh	XXXXh

Mode	Function	Setting Range	RW
Timer mode	When n is a setting value, counter cycle: $\frac{(n + 1)}{fj}$	0000h to FFFFh	RW
Event counter mode	When n is a set value, FFFFh - n + 1 count (at increment) n + 1 count (at decrement)	0000h to FFFFh	RW
One-shot timer mode	When n is a set value, pulse width: $\frac{n}{fj}$	0000h to FFFFh	WO
Pulse width modulation mode (16-bit PWM mode)	When n is a set value, PWM period: $\frac{(2^{16} - 1)}{fj}$ PWM pulse width: $\frac{n}{fj}$	0000h to FFFEh	WO
Pulse width modulation mode (8-bit PWM mode)	When n is an upper address setting value, and m is a lower address setting value, PWM period: $\frac{(2^8 - 1) \times (m + 1)}{fj}$ PWM pulse width: $\frac{(m + 1)n}{fj}$	00h to FEh (upper address) 00h to FFh (lower address)	WO
Programmable output mode	When n is a setting value of TAi1 register, and m is a setting value of TAi register, high-level duration: $\frac{m}{fj}$ low-level duration: $\frac{n}{fj}$	0000h to FFFFh	WO

fj : Count source frequency

Access the register in 16-bit units. Use the MOV instruction to write to the TAi register.

Event Counter Mode

The timer counts pulses from an external device, or the overflows/underflows of other timers.

One-Shot Timer Mode

If the TAi register is set to 0000h, the counter does not work and timer Ai interrupt requests are not generated. Furthermore, if pulse output is selected, no pulses are output from the TAiOUT pin.

Pulse Width Modulation Mode (16-bit PWM mode)

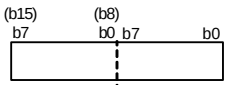
When the TAi register is set to 0000h, the counter does not work, the output level on the TAiOUT pin remains low, and timer Ai interrupt requests are not generated.

Pulse Width Modulation Mode (8-bit PWM mode)

This mode operates as an 8-bit prescaler (lower 8 bits) and an 8-bit pulse width modulator (upper 8 bits). When the upper 8 bits of the TAi register are set to 00h, the counter does not work, the output level on the TAiOUT pin remains low, and a timer Ai interrupt request is not generated.

15.2.9 Timer Ai-1 Register (TAi1) (i = 1, 2, 4)

Timer Ai-1 Register (i = 1, 2, 4)



Symbol	Address	Reset Value
TA11	0303h to 0302h	XXXXh
TA21	0305h to 0304h	XXXXh
TA41	0307h to 0306h	XXXXh

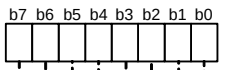
Mode	Function	Setting Range	RW
Programmable output mode	When n is a setting value of TAi1 register, and m is a setting value of TAi register, high-level duration: $\frac{m}{fj}$ low-level duration: $\frac{n}{fj}$	0001h to FFFFh	WO

fj: Count source frequency

Access the register in 16-bit units. Use the MOV instruction to write to the TAi1 register.

15.2.10 Count Start Flag (TABSR)

Count Start Flag



Symbol	Address	Reset Value
TABSR	0320h	00h

Bit Symbol	Bit Name	Function	RW
TA0S	Timer A0 count start flag	0 : Count stopped 1 : Count started	RW
TA1S	Timer A1 count start flag		RW
TA2S	Timer A2 count start flag		RW
TA3S	Timer A3 count start flag		RW
TA4S	Timer A4 count start flag		RW
TB0S	Timer B0 count start flag		RW
TB1S	Timer B1 count start flag		RW
TB2S	Timer B2 count start flag		RW

15.2.11 One-Shot Start Flag (ONSF)

One-Shot Start Flag

b7 b6 b5 b4 b3 b2 b1 b0	Symbol	Address	Reset Value
	ONSF	0322h	00h

Bit Symbol	Bit Name	Function	RW
TA0OS	Timer A0 one-shot start flag	The timer starts counting by setting this bit to 1. The read values are 0.	RW
TA1OS	Timer A1 one-shot start flag		RW
TA2OS	Timer A2 one-shot start flag		RW
TA3OS	Timer A3 one-shot start flag		RW
TA4OS	Timer A4 one-shot start flag		RW
TAZIE	Z-phase input enable bit	0 : Z-phase input disabled 1 : Z-phase input enabled	RW
TA0TGL	Timer A0 event/trigger select bit	b7 b6 0 0 : Input on TA0IN pin selected 0 1 : Timer B2 selected 1 0 : Timer A4 selected 1 1 : Timer A1 selected	RW
TA0TGH			RW

TAiOS (Timer Ai one-shot start flag) (b4-b0) (i = 0 to 4)

This bit is enabled in one-shot timer mode. When the MR2 bit in the TAi register is 0 (TAiOS bit enabled), the timer Ai count starts by setting the TAiOS bit to 1 after setting the TAiS bit in the TABSR register to 1 (start counting).

TAZIE (Z-phase input enable bit) (b5)

This bit is used in event counter mode (two-phase pulse signal processing) of timer A3. Refer to 15.3.4.3 “Counter Initialization Using Two-Phase Pulse Signal Processing” for details.

TA0TGH-TA0TGL (Timer A0 event/trigger select bit) (b7-b6)

These bits are used to select an event or a trigger in the following modes:

- An event in event counter mode (when not using two-phase pulse signal processing)
- A trigger in one-shot timer mode or PWM mode

  The above applies when the MR2 bit in the TA0MR register is 1 (trigger selected by setting bits TA0TGH to TA0TGL).

When bits TA0TGH to TA0TGL are 00b, the active edge of input signals can be selected by setting the MR1 bit in the TA0MR register.

When bits TA0TGH to TA0TGL are set to 01b, 10b, or 11b, an event or a trigger occurs when an interrupt request for the selected timer is generated. An event or trigger can occur while interrupts are disabled because an interrupt request signal is generated regardless of the I flag, IPL, or interrupt control registers.

15.2.12 Trigger Select Register (TRGSR)

Trigger Select Register

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	Reset Value
								TRGSR	0323h	00h

Bit Symbol	Bit Name	Function	RW
TA1TGL	Timer A1 event/trigger select bit	b1 b0 0 0 : Input on TA1IN selected 0 1 : TB2 selected 1 0 : TA0 selected 1 1 : TA2 selected	RW
TA1TGH			RW
TA2TGL	Timer A2 event/trigger select bit	b3 b2 0 0 : Input on TA2IN selected 0 1 : TB2 selected 1 0 : TA1 selected 1 1 : TA3 selected	RW
TA2TGH			RW
TA3TGL	Timer A3 event/trigger select bit	b5 b4 0 0 : Input on TA3IN selected 0 1 : TB2 selected 1 0 : TA2 selected 1 1 : TA4 selected	RW
TA3TGH			RW
TA4TGL	Timer A4 event/trigger select bit	b7 b6 0 0 : Input on TA4IN selected 0 1 : TB2 selected 1 0 : TA3 selected 1 1 : TA0 selected	RW
TA4TGH			RW

TA1TGH-TA1TGL (Timer A1 event/trigger select bit) (b1-b0)
TA2TGH-TA2TGL (Timer A2 event/trigger select bit) (b3-b2)
TA3TGH-TA3TGL (Timer A3 event/trigger select bit) (b5-b4)
TA4TGH-TA4TGL (Timer A4 event/trigger select bit) (b7-b6)

These bits are used to select an event or a trigger of the following modes:

- An event in event counter mode (when not using two-phase pulse signal processing)
- A trigger in one-shot timer mode, PWM mode, or programmable output mode
  The above applies when the MR2 bit in the TAiMR register is 1 (trigger selected by setting bits TAiTGH to TAiTGL).

When bits TAiTGH to TAiTGL are 00b, the active edge of input signals can be selected by setting the MR1 bit in the TAiMR register.

When bits TAiTGH to TAiTGL are set to 01b, 10b, or 11b, an event or a trigger occurs when an interrupt request of the selected timer is generated. An event or trigger can occur while interrupts are disabled because an interrupt request signal is generated regardless of the I flag, IPL, or interrupt control registers.

15.2.13 Increment/Decrement Flag (UDF)

Increment/Decrement Flag

b7 b6 b5 b4 b3 b2 b1 b0

Symbol: UDF
Address: 0324h
Reset Value: 00h

Bit Symbol	Bit Name	Function	RW
TA0UD	Timer A0 increment/ decrement flag	0 : Decrement 1 : Increment	RW
TA1UD	Timer A1 increment/ decrement flag		RW
TA2UD	Timer A2 increment/ decrement flag		RW
TA3UD	Timer A3 increment/ decrement flag		RW
TA4UD	Timer A4 increment/ decrement flag		RW
TA2P	Timer A2 two-phase pulse signal processing select bit	0 : Two-phase pulse signal processing disabled 1 : Two-phase pulse signal processing enabled	RW
TA3P	Timer A3 two-phase pulse signal processing select bit		RW
TA4P	Timer A4 two-phase pulse signal processing select bit		RW

TAiUD (Timer Ai increment/decrement flag) (b4 to b0) (i = 0 to 4)

Enabled in event counter mode (when not using two-phase pulse signal processing).

TA2P (Timer A2 two-phase pulse signal processing select bit) (b5)
TA3P (Timer A3 two-phase pulse signal processing select bit) (b6)
TA4P (Timer A4 two-phase pulse signal processing select bit) (b7)

Set these bits to 0 when not using two-phase pulse signal processing.

15.2.14 Timer Ai Mode Register (TAiMR) (i = 0 to 4)

Timer Ai Mode Register (i = 0 to 4)

b7 b6 b5 b4 b3 b2 b1 b0	Symbol	Address	Reset Value
	TA0MR to TA4MR	0336h to 033Ah	00h

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 0 0 : Timer mode 0 1 : Event counter mode 1 0 : One-shot timer mode 1 1 : Pulse width modulation (PWM) mode or programmable output mode	RW
TMOD1			RW
MR0	Function varies with the operation mode		RW
MR1			RW
MR2			RW
MR3			RW
TCK0	Function varies with operation mode		RW
TCK1			RW

15.3 Operations

15.3.1 Common Operations

15.3.1.1 Operating Clock

The count source for each timer acts as a clock, controlling such timer operations as counting and reloading.

If the conditions to start counting are met, the stopped counter starts counting at the count timing of the first count source. For this reason, a delay exists between when the count start conditions are met and the counter starts counting. Figure 15.4 shows Output Example of One-Shot Timer Mode.

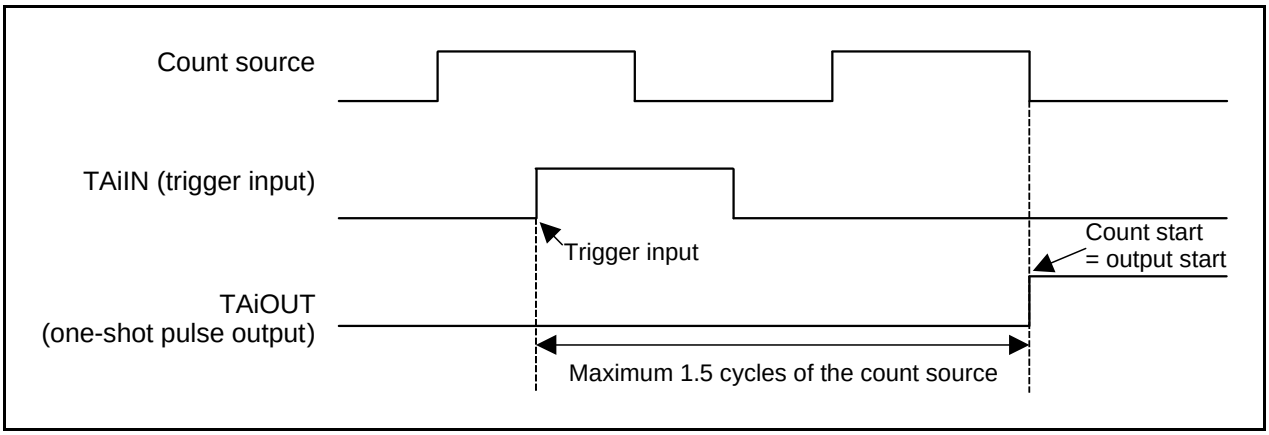


Figure 15.4 Output Example of One-Shot Timer Mode

15.3.1.2 Counter Reload Timing

Timer Ai starts counting from the value set (n) in the TAi register. The TAi register consists of a counter and a reload register. The counter starts decrementing the count source from n, reloads a value in the reload register at the next count source after the value becomes 0000h, and continues decrementing. When incrementing, the counter reloads a value in the reload register at the next count source after the value becomes FFFFh.

The value written in the TAi register is reflected in the counter and the reload register at the following timings:

- When the count is stopped
- Between when the count starts and when the first count source is input
  A value written to the TAi register is immediately written to the counter and the reload register.

- After the count starts and the first count source is input
  A value written to the TAi register is immediately written to the reload register. The counter continues counting and reloads the value in the reload register at the next count source after the value becomes 0000h (or FFFFh).

15.3.1.3 Count Source

Internal clocks are counted in timer mode, one-shot timer mode, PWM mode, and programmable output mode. Refer to Figure 15.1 “Timer A and B Count Sources” for details. Table 15.5 lists the Timer A Count Sources.

f1 is any of the clocks listed below (refer to 8. “Clock Generator” for details).

- Main clock divided by 1 (no division)
- PLL clock divided by 1 (no division)
- fOCO-S divided by 1 (no division)
- fOCO-F divided by 1 (no division)

Table 15.5 Timer A Count Sources

Count Source	Bit Setting Value				Remarks
	PCLK0	TCS3 TCS7	TCS2 to TCS0 TCS6 to TCS4	TCK1 to TCK0	
f1TIMAB	1	0	-	00b	f1 or fOCO-F (1)
		1	000b	-	
f2TIMAB	0	0	-	00b	f1 divided by 2 or fOCO-F divided by 2 (1)
		1	000b	-	
f8TIMAB	-	0	-	01b	f1 divided by 8 or fOCO-F divided by 8 (1)
		1	001b	-	
f32TIMAB	-	0	-	10b	f1 divided by 32 or fOCO-F divided by 32 (1)
		1	010b	-	
f64TIMAB	-	1	011b	-	f1 divided by 64 or fOCO-F divided by 64 (1)
fOCO-F	-	1	100b	-	fOCO-F
fOCO-S	-	1	101b	-	fOCO-S
fC32	-	0	-	11b	fC32
		1	110b	-	

PCLK0: Bit in the PCLKR register

TCS7 to TCS0: Bits in registers TACS0 to TACS2

TCK1 to TCK0: Bits in the TAiMR register (i = 0 to 4)

Note:

1. Set the TCDIV00 bit in the TCKDIVC0 register to select f1 or fOCO-F.

15.3.2 Timer Mode

In timer mode, the timer counts an internally generated count source. Table 15.6 lists Timer Mode Specifications, Table 15.7 lists Registers and the Setting in Timer Mode, and Figure 15.5 shows an Operation Example in Timer Mode.

Table 15.6 Timer Mode Specifications

Item	Specification
Count source	f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32
Count operation	• Decrement • When the timer underflows, it reloads the reload register value and continues counting.
Counter cycles	$\frac{(n+1)}{fj}$ n: set value of TAi register, 0000h to FFFFh fj: frequency of count source
Count start condition	Set the TAiS bit in the TABSR register to 1 (start counting).
Count stop condition	Set the TAiS bit to 0 (stop counting).
Interrupt request generation timing	Timer underflow
TAiIN pin function	I/O port or gate input
TAiOUT pin function	I/O port or pulse output
Read from timer	The count value can be read by reading the TAi register.
Write to timer	• When not counting Value written to the TAi register is written to both the reload register and counter. • When counting Value written to the TAi register is only written to reload register (transferred to counter when reloaded next).
Selectable functions	• Gate function Counting can be started and stopped by an input signal to the TAiIN pin. • Pulse output function Whenever the timer underflows, the output polarity of the TAiOUT pin is inverted. When the TAiS bit is set to 0 (stop counting), the pin outputs a low-level signal. • Output polarity control The output polarity of the TAiOUT pin is inverted. (While the TAiS bit is set to 0 (stop counting), a high-level signal is output.)

i = 0 to 4

Table 15.7 Registers and Settings in Timer Mode (1)

Register	Bit	Function and Setting
PCLKR	PCLK0	Select the count source.
CPSRF	CPSR	Write 1 to reset the clock prescaler.
TCKDIVC0	TCDIV00	Select the clock used prior to timer AB frequency dividing.
PWMFS	PWMFSi	Set to 0.
TACS0 to TACS2	7 to 0	Select the count source.
TAPOFS	POFSi	Select the output polarity when the MR0 bit in the TAiMR register is 1 (pulse output).
TAOW	TAiOW	Set to 0.
TAi1	15 to 0	- (does not need to be set)
TABSR	TAiS	Set to 1 when starting counting. Set to 0 when stopping counting.
ONSF	TAiOS	Set to 0.
	TAZIE	Set to 0.
	TA0TGH to TA0TGL	Set to 00b.
TRGSR	TAiTGH to TAiTGL	Set to 00b.
UDF	TAiUD	Set to 0.
	TAiP	Set to 0.
TAi	15 to 0	Set the counter value.
TAiMR	7 to 0	Refer to the TAiMR register below

i = 0 to 4

Note:

1. This table does not describe a procedure.

Timer Mode

Timer Ai Mode Register (i = 0 to 4)

b7	b6	b5	b4	b3	b2	b1	b0
		0				0	0

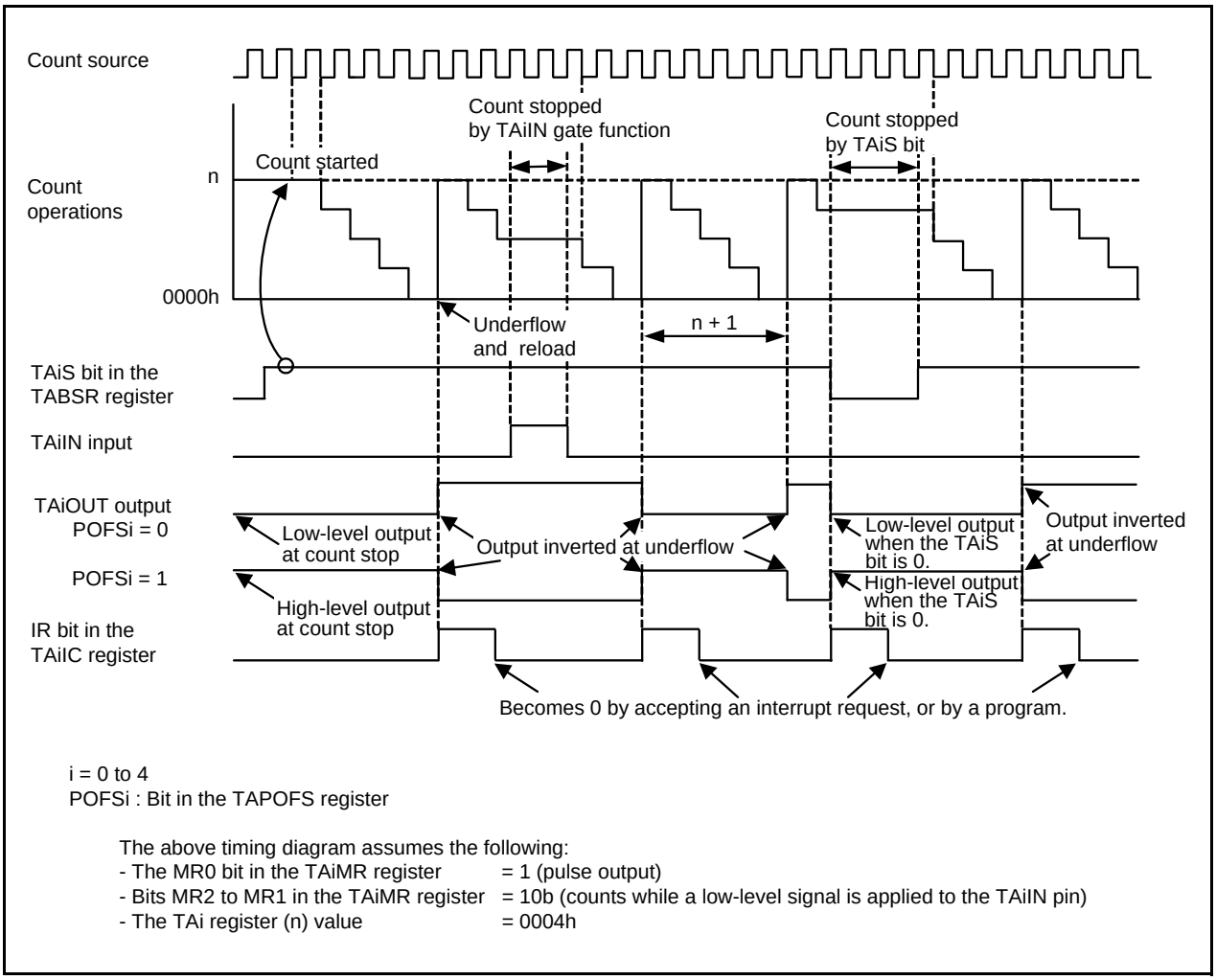
Symbol	Address	Reset Value
TA0MR to TA4MR	0336h to 033Ah	00h

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 0 0 : Timer mode	RW
TMOD1			RW
MR0	Pulse output function select bit	0 : No pulse output (TAiOUT pin functions as I/O port) 1 : Pulse output (TAiOUT pin functions as a pulse output pin)	RW
MR1	Gate function select bit	b4 b3 0 0 : } Gate function not available 0 1 : } (TAiIN pin functions as I/O port) 1 0 : Counts while input on the TAiIN pin is low 1 1 : Counts while input on the TAiIN pin is high	RW
MR2			RW
MR3	Set to 0 in timer mode		RW
TCK0	Count source select bit	b7 b6 0 0 : f1TIMAB or f2TIMAB 0 1 : f8TIMAB 1 0 : f32TIMAB 1 1 : fC32	RW
TCK1			RW

TCK1-TCK0 (Count source select bit) (b7-b6)

These bits are enabled when the TCS3 bit or TCS7 bit in registers TACS0 to TACS2 is set to 0 (TCK0 to TCK1 enabled).

Set the PCLK0 bit in the PCLKR register to select f1TIMAB or f2TIMAB.



i = 0 to 4
POFSi : Bit in the TAPOFS register

The above timing diagram assumes the following:
- The MR0 bit in the TAiMR register = 1 (pulse output)
- Bits MR2 to MR1 in the TAiMR register = 10b (counts while a low-level signal is applied to the TAiIN pin)
- The TAi register (n) value = 0004h

Figure 15.5 Operation Example in Timer Mode

15.3.3 Event Counter Mode (When Not Using Two-Phase Pulse Signal Processing)

In event counter mode, the timer counts pulses from an external device, or overflows/underflows of other timers. Timers A2, A3, and A4 can count two-phase external signals. Refer to 15.3.4 “Event Counter Mode (When Processing Two-Phase Pulse Signal)” for details. Table 15.8 lists Event Counter Mode Specifications (When Not Using Two-Phase Pulse Signal Processing). Table 15.9 lists Registers and the Setting in Event Counter Mode (When Not Processing Two-Phase Pulse Signal). Figure 15.6 shows Operation Example in Event Counter Mode.

Table 15.8 Event Counter Mode Specifications (When Not Using Two-Phase Pulse Signal Processing)

Item	Specification
Count source	• External signals input to the TAiIN pin (active edge can be selected) • Timer B2 overflows or underflows • Timer Aj overflows or underflows (j = i - 1, except j = 4 if i = 0) • Timer Ak overflows or underflows (k = i + 1, except k = 0 if i = 4)
Count operations	• Increment or decrement can be selected by a program. • When the timer overflows or underflows, it reloads the reload register value and continues counting. When selecting free-run type, the timer continues counting without reloading.
Number of counts	When selecting reload type: • FFFFh - n + 1 for increment • n + 1 for decrement n: setting value of the TAi register, 0000h to FFFFh
Count start condition	Set the TAiS bit in the TABSR register to 1 (start counting).
Count stop condition	Set the TAiS bit to 0 (stop counting).
Interrupt request generation timing	Timer overflow or underflow
TAiIN pin function	I/O port or count source input
TAiOUT pin function	I/O port or pulse output
Read from timer	Count value can be read by reading the TAi register.
Write to timer	• When not counting Value written to the TAi register is written to both the reload register and counter. • When counting Value written to the TAi register is written to only reload register (transferred to counter when reloaded next).
Selectable functions	• Free-run count function Even when the timer overflows or underflows, the reload register content is not reloaded. • Pulse output function Whenever the timer underflows or underflows, the output polarity of the TAiOUT pin is inverted. When the TAiS bit is set to 0 (stop counting), the pin outputs a low-level signal. • Output polarity control The output polarity of the TAiOUT pin is inverted. (While the TAiS bit is set to 0 (stop counting), a high-level signal is output.)

i = 0 to 4

Table 15.9 Registers and Settings in Event Counter Mode (When Not Using Two-Phase Pulse Signal Processing) (1)

Register	Bit	Function and Setting
PCLKR	PCLK0	- (setting unnecessary)
CPSRF	CPSR	Write 1 to reset the clock prescaler.
TCKDIVC0	TCDIV00	- (setting unnecessary)
PWMFS	PWMFSi	Set to 0.
TACS0 to TACS2	7 to 0	- (setting unnecessary)
TAPOFS	POFSi	Select the output polarity when the MR0 bit in the TAiMR register is 1 (pulse output).
TAOW	TAiOW	Set to 0.
TAi1	15 to 0	- (setting unnecessary)
TABSR	TAiS	Set to 1 when starting counting. Set to 0 when stopping counting.
ONSF	TAiOS	Set to 0.
	TAZIE	Set to 0.
	TA0TGH to TA0TGL	Select a count source.
TRGSR	TAiTGH to TAiTGL	Select a count source.
UDF	TAiUD	Select a count operation.
	TAiP	Set to 0.
TAi	15 to 0	Set the counter value.
TAiMR	7 to 0	Refer to the TAiMR register below.

i = 0 to 4

Note:

1. This table does not describe a procedure.

Event Counter Mode (When Not Using Two-Phase Pulse Signal Processing)

Timer Ai Mode Register (i = 0 to 4)

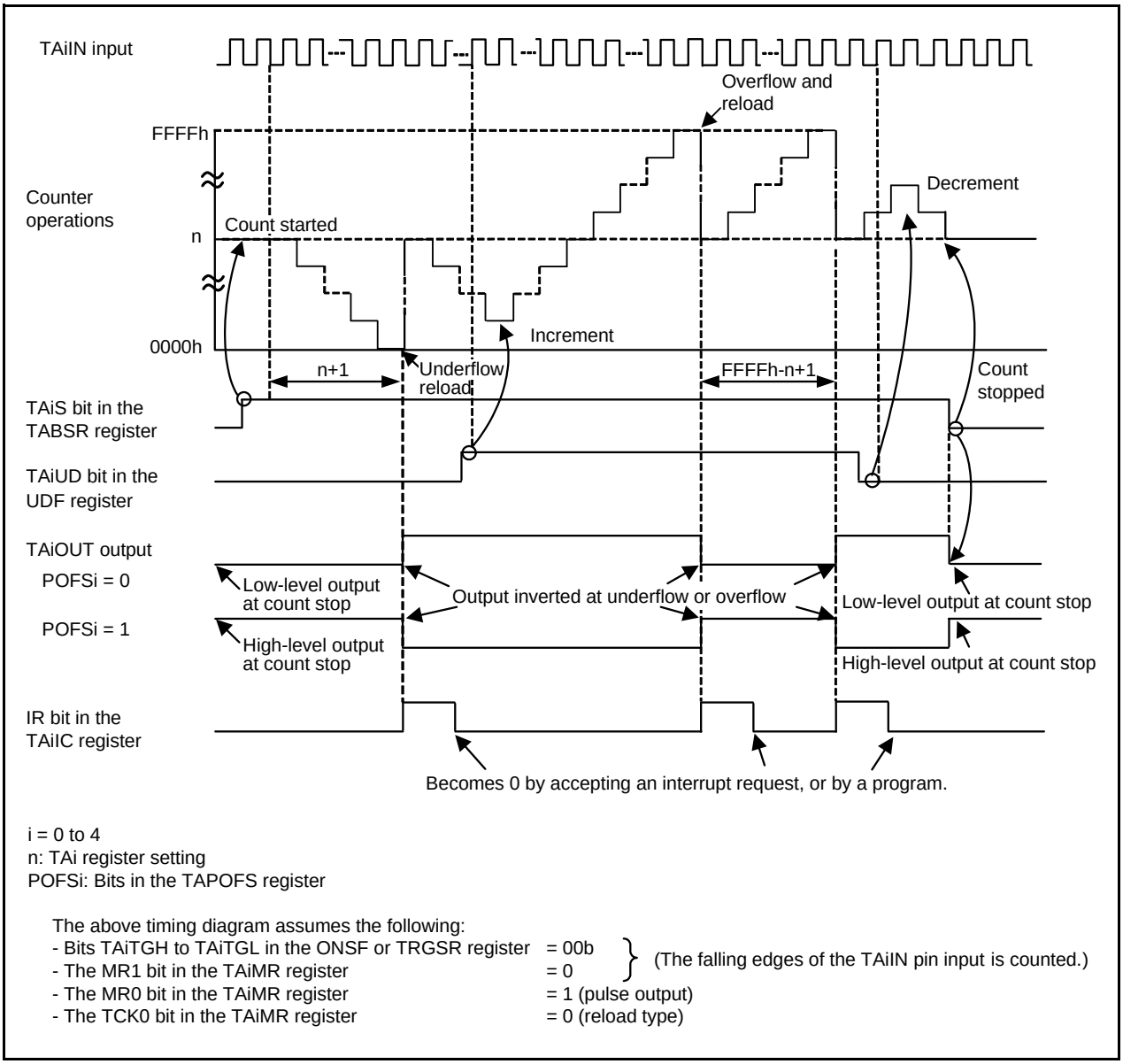
b7	b6	b5	b4	b3	b2	b1	b0
		0	0			0	1

Symbol	Address	Reset Value
TA0MR to TA4MR	0336h to 033Ah	00h

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 0 1 : Event counter mode	RW
TMOD1			RW
MR0	Pulse output function select bit	0 : Pulse is not output (TAiOUT pin functions as I/O port) 1 : Pulse is output (TAiOUT pin functions as pulse output pin)	RW
MR1	Count polarity select bit	0 : Counts falling edge of an external signal 1 : Counts rising edge of an external signal	RW
MR2	Set to 0 in event counter mode		RW
MR3	Set to 0 in event counter mode		RW
TCK0	Count operation type select bit	0 : Reload type 1 : Free-run type	RW
TCK1	Can be 0 or 1 when not using two-phase pulse signal processing		RW

MR1 (Count polarity select bit) (b3)

This bit is enabled when bits TAiTGH to TAiTGL in the ONSF or TRGSR register are 00b (TAiIN pin input).



i = 0 to 4
n: TAi register setting
POFSi: Bits in the TAPOFS register

The above timing diagram assumes the following:
- Bits TAiTGH to TAiTGL in the ONSF or TRGSR register = 00b
- The MR1 bit in the TAiMR register = 0

} (The falling edges of the TAiIN pin input is counted.)

- The MR0 bit in the TAiMR register = 1 (pulse output)
- The TCK0 bit in the TAiMR register = 0 (reload type)

Figure 15.6 Operation Example in Event Counter Mode

15.3.4 Event Counter Mode (When Processing Two-Phase Pulse Signal)

Timers A2, A3, and A4 can be used to count two-phase pulse signals. Table 15.10 lists Event Counter Mode Specifications (When Processing Two-Phase Pulse Signal with Timers A2, A3, and A4). Table 15.11 lists Registers and the Setting in Event Counter Mode (When Processing Two-Phase Pulse Signal).

Table 15.10 Event Counter Mode Specifications (When Processing Two-Phase Pulse Signal with Timers A2, A3, and A4)

Item	Specification
Count source	Two-phase pulse signals input to the TAiIN or TAiOUT pin
Count operations	• Increment or decrement can be selected by a two-phase pulse signal. • When the timer overflows or underflows, it reloads the reload register value and continues counting. When selecting free-run type, the timer continues counting without reloading.
Number of counts	When selecting reload type: • FFFFh - n + 1 when incrementing • n + 1 when decrementing n: setting value of the TAi register, 0000h to FFFFh
Count start condition	Set the TAiS bit in the TABSR register to 1 (start counting).
Count stop condition	Set the TAiS bit to 0 (stop counting).
Interrupt request generation timing	Timer overflow or underflow
TAiIN pin function	Two-phase pulse input
TAiOUT pin function	Two-phase pulse input
Read from timer	Count value can be read by reading timer A2, A3, or A4 register.
Write to timer	• When not counting Value written to the TAi register is written to both the reload register and counter. • When counting Value written to the TAi register is written to only reload register (transferred to counter when reloaded next).
Selectable functions	• Select normal or multiply-by-4 processing operation (timer A3). • Counter initialization by Z-phase input (timer A3) The timer count value is initialized to 0 by Z-phase input.

i = 2 to 4

Table 15.11 Registers and Settings in Event Counter Mode (When Processing Two-Phase Pulse Signal) (1)

Register	Bit	Function and Setting
PCLKR	PCLK0	- (setting unnecessary)
CPSRF	CPSR	Write 1 to reset the clock prescaler.
TCKDIVC0	TCDIV00	- (setting unnecessary)
PWMFS	PWMFSi	Set to 0.
TACS0 to TACS2	7 to 0	- (setting unnecessary)
TAPOFS	POFSi	Set to 0.
TAOW	TAiOW	Set to 0.
TAi1	15 to 0	- (setting unnecessary)
TABSR	TAiS	Set to 1 when starting counting. Set to 0 when stopping counting.
ONSF	TAiOS	Set to 0.
	TAZIE	Set to 1 when using Z-phase input with timer A3.
	TA0TGH to TA0TGL	- (setting unnecessary)
TRGSR	TAiTGH to TAiTGL	Set to 00b.
UDF	TAiUD	Set to 0.
	TAiP	Set to 1.
TAi	15 to 0	Set the counter value.
TAiMR	7 to 0	Refer to the TAiMR register below.

i = 2 to 4

Note:

1. This table does not describe a procedure.

Event Counter Mode (When Using Two-Phase Pulse Signal Processing)
Timer Ai Mode Register (i = 2 to 4)

b7	b6	b5	b4	b3	b2	b1	b0
		0	1	0	0	0	1

Symbol: TA2MR to TA4MR
Address: 0338h to 033Ah
Reset Value: 00h

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 0 1 : Event counter mode	RW
TMOD1			RW
MR0	Set to 0 to use two-phase signal processing		RW
MR1	Set to 0 to use two-phase signal processing		RW
MR2	Set to 1 to use two-phase signal processing		RW
MR3	Set to 0 to use two-phase signal processing		RW
TCK0	Count operation type select bit	0 : Reload type 1 : Free-run type	RW
TCK1	Two-phase pulse signal processing operation type select bit	0 : Normal processing operation 1 : Multiply-by-4 processing operation	RW

TCK1 (Two-phase pulse signal processing operation type select bit) (b7)

The TCK1 bit can be set only for timer A3. No matter how this bit is set, timers A2 and A4 always operate in normal processing mode and multiply-by-4 processing mode, respectively.

15.3.4.1 Normal Processing

The timer increments at rising edges or decrements at falling edges on the TAjIN pin when input signals to the TAjOUT (j = 2, 3) pin is high level.

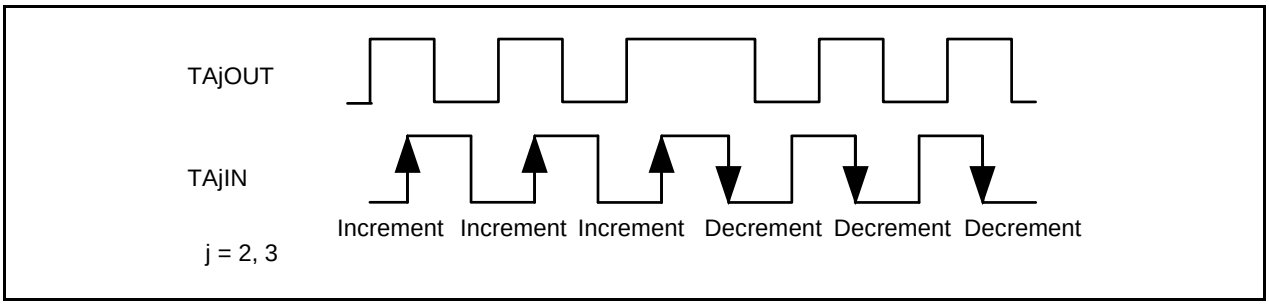


Figure 15.7 Normal Processing

15.3.4.2 Multiply-by-4 Processing

If the phase relationship is such that the input signal to the TAkIN pin goes high while the input signal to the TAkOUT pin (k = 3, 4) is high, the timer increments at both rising and falling edges of the input signal to pins TAkOUT and TAkIN. If the phase relationship is such that the input signal to the TAkIN pin goes low while the input signal to the TAkOUT pin is high, the timer decrements at both rising and falling edges of the input signal to pins TAkOUT and TAkIN.

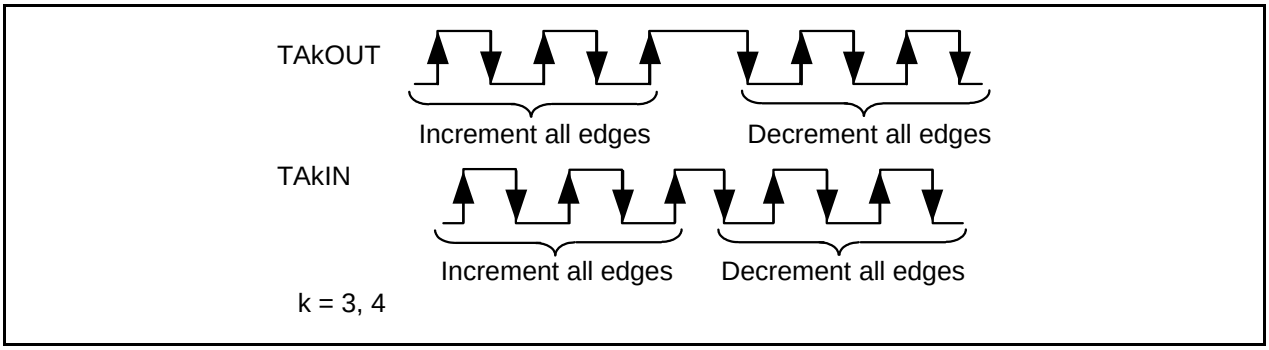


Figure 15.8 Multiply-by-4 Processing

15.3.4.3 Counter Initialization Using Two-Phase Pulse Signal Processing

This function initializes the timer count value to 0000h using Z-phase (counter initialization) input during two-phase pulse signal processing.

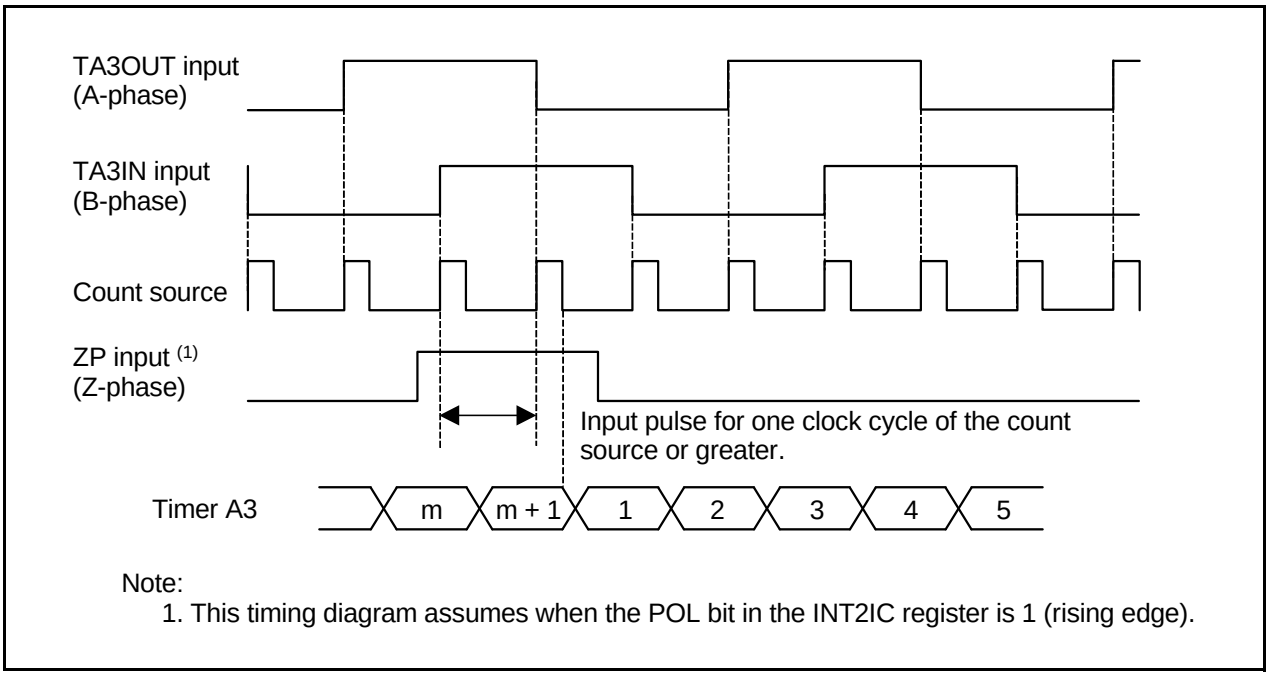
This function can only be used in timer A3 event counter mode during two-phase pulse signal processing, free-running type, multiply-by-4 processing, with Z-phase entered from the ZP pin.

Counter initialization by Z-phase input is enabled by writing 0000h to the TA3 register and setting the TAZIE bit in the ONSF register to 1 (Z-phase input enabled).

Counter initialization is accomplished by Z-phase input edge detection. The rising or falling edge can be selected as the active edge by setting the POL bit in the INT2IC register. The Z-phase pulse width must be equal to or greater than one clock cycle of the timer A3 count source.

The counter is initialized at the next count timing after accepting Z-phase input. Figure 15.9 shows the Relationship between the Two-Phase Pulse (A-Phase and B-Phase) and the Z-Phase.

When timer A3 overflow or underflow coincides with counter initialization by Z-phase input, a timer A3 interrupt request is generated twice in succession. Do not use the timer A3 interrupt when using this function.



Note:
1. This timing diagram assumes when the POL bit in the INT2IC register is 1 (rising edge).

Figure 15.9 Relationship between the Two-Phase Pulse (A-Phase and B-Phase) and the Z-Phase

15.3.5 One-Shot Timer Mode

In one-shot timer mode, the timer is activated only once per trigger. When the trigger occurs, the timer starts and continues operating for a given period. Table 15.12 lists One-Shot Timer Mode Specifications. Table 15.13 lists Registers and the Setting in One-Shot Timer Mode. Figure 15.10 shows Operation Example in One-Shot Timer Mode.

Table 15.12 One-Shot Timer Mode Specifications

Item	Specification
Count source	f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32
Count operations	• Decrement • When the timer counter reaches 0000h, it stops running after the reload register value is reloaded • When a trigger occurs while counting, the reload register value is reloaded into the counter to continue counting
Pulse width	$\frac{n}{fj}$  n: Set value of the TAi register, 0000h to FFFFh However, the counter does not run if 0000h is set. fj: Count source frequency
Count start condition	The TAiS bit in the TABSR register is 1 (start counting) and one of the following triggers occurs: • External trigger input from the TAiIN pin • Timer B2 overflow or underflow • Timer Aj overflow or underflow (j = i - 1, except j = 4 if i = 0) • Timer Ak overflow or underflow (k = i + 1, except k = 0 if i = 4) • The TAiOS bit in the ONSF register is set to 1 (one-shot timer start).
Count stop condition	• When the counter is reloaded after reaching 0000h • The TAiS bit is set to 0 (stop counting)
Interrupt request generation timing	When the counter reaches 0000h
TAiIN pin function	I/O port or trigger input
TAiOUT pin function	I/O port or pulse output
Read from timer	An undefined value is read when reading the TAi register.
Write to timer	• When not counting and until the first count source is input after counting starts, the value written to the TAi register is written to both the reload register and counter. • When counting (after the first count source input), the value written to the TAi register is written to only the reload register (transferred to the counter when reloaded next time).
Selectable functions	• Pulse output function The timer outputs a low-level signal when not counting and a high-level signal when counting. • Output polarity control The output polarity of the TAiOUT pin is inverted. (While the TAiS bit is set to 0 (stop counting), a high-level signal is output.)

i = 0 to 4

Table 15.13 Registers and Settings in One-Shot Timer Mode (1)

Register	Bit	Setting
PCLKR	PCLK0	Select the count source.
CPSRF	CPSR	Write 1 to reset the clock prescaler.
TCKDIVC0	TCDIV00	Select a clock used prior to dividing timer AB frequency.
PWMFS	PWMFSi	Set to 0.
TACS0 to TACS2	7 to 0	Select the count source.
TAPOFS	POFSi	Select the output polarity when the MR0 bit in the TAiMR register is 1 (pulse output).
TAOW	TAiOW	Set to 0.
TAi1	15 to 0	- (setting unnecessary)
TABSR	TAiS	Set to 1 when starting counting. Set to 0 when stopping counting.
ONSF	TAiOS	Set to 1 when starting counting while the MR2 bit is 0.
	TAZIE	Set to 0.
	TA0TGH to TA0TGL	Select a count trigger.
TRGSR	TAiTGH to TAiTGL	Select a count trigger.
UDF	TAiUD	Set to 0.
	TAiP	Set to 0.
TAi	15 to 0	Set a high-level pulse width. (2)
TAiMR	7 to 0	Refer to the TAiMR register below.

i = 0 to 4

Notes:

1. This table does not describe a procedure.
2. This applies when the POFSi bit in the TAPOFS register is 0.

One-Shot Timer Mode

Timer Ai Mode Register (i = 0 to 4)

b7	b6	b5	b4	b3	b2	b1	b0
		0				1	0

Symbol	Address	Reset Value
TA0MR to TA4MR	0336h to 033Ah	00h

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 1 0 : One-shot timer mode	RW
TMOD1			RW
MR0	Pulse output function select bit	0 : No pulse output (TAiOUT pin functions as an I/O port) 1 : Pulse output (TAiOUT pin functions as a pulse output pin)	RW
MR1	External trigger select bit	0 : Falling edge of input signal to TAiIN pin 1 : Rising edge of input signal to TAiIN pin	RW
MR2	Trigger select bit	0 : TAiOS bit enabled 1 : Selected by bits TAiTGH and TAiTGL	RW
MR3	Set to 0 in one-shot timer mode		RW
TCK0	Count source select bit	b7 b6 0 0 : f1TIMAB or f2TIMAB 0 1 : f8TIMAB 1 0 : f32TIMAB 1 1 : fC32	RW
TCK1			

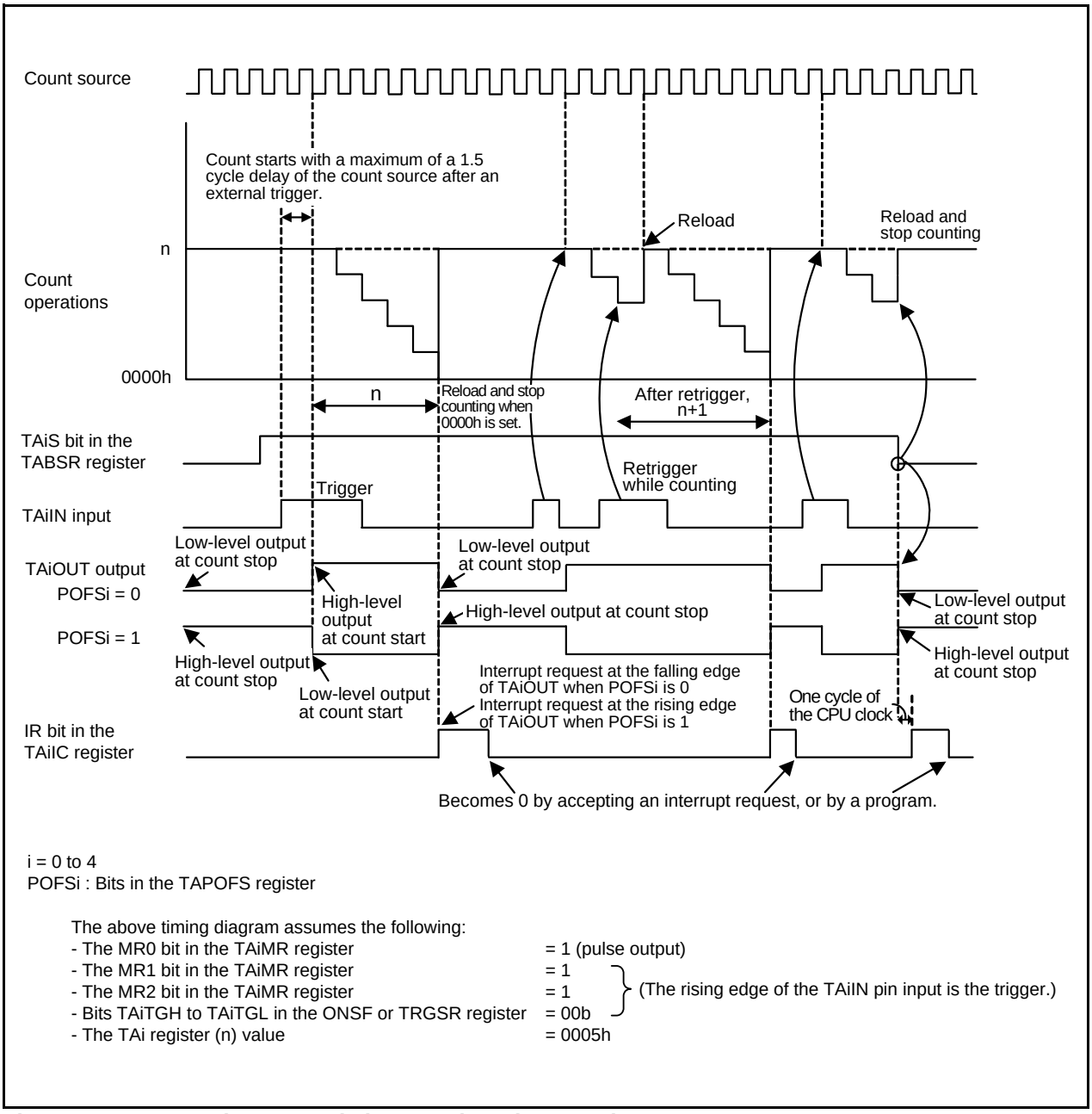
MR1 (External trigger select bit) (b3)

This bit is enabled when the MR2 bit is 1 and bits TAiTGH to TAiTGL in the ONSF register or TRGSR register are set to 00b (TAiIN pin input).

TCK1 and TCK0 (Count source select bit) (b7-b6)

These bits are enabled when the TCS3 bit or TCS7 bit in registers TACS0 to TACS2 is set to 0 (TCK0 to TCK1 enabled).

Set the PCLK0 bit in the PCLKR register to select f1TIMAB or f2TIMAB.



i = 0 to 4
POFSi : Bits in the TAPOFS register

The above timing diagram assumes the following:

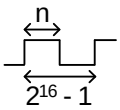
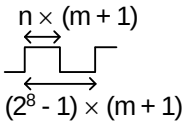
- The MR0 bit in the TAiMR register	= 1 (pulse output)	
- The MR1 bit in the TAiMR register	= 1	(The rising edge of the TAiIN pin input is the trigger.)
- The MR2 bit in the TAiMR register	= 1	
- Bits TAiTGH to TAiTGL in the ONSF or TRGSR register	= 00b	
- The TAi register (n) value	= 0005h	

Figure 15.10 Operation Example in One-Shot Timer Mode

15.3.6 Pulse Width Modulation (PWM) Mode

In PWM mode, the timer outputs pulses of a given width in succession. The counter functions as either a 16-bit pulse width modulator or 8-bit pulse width modulator. Table 15.14 lists PWM Mode Specifications. Table 15.15 lists Registers and the Setting in PWM Mode. Figure 15.11 and Figure 15.12 show Operation Example in 16-Bit Pulse Width Modulation Mode and Operation Example in 8-Bit Pulse Width Modulation Mode, respectively.

Table 15.14 PWM Mode Specifications

Item	Specification
Count sources	f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32
Count operations	• Decrement (operating as an 8-bit or a 16-bit pulse width modulator) • The timer reloads the reload register value at a rising edge of PWM pulse and continues counting. • The timer is not affected by a trigger that occurs during counting.
16-bit PWM	• Pulse width $\frac{n}{fj}$  • Cycle time $\frac{(2^{16}-1)}{fj}$ n: set value of the TAi register fj: count source frequency
8-bit PWM	• Pulse width $\frac{n \times (m+1)}{fj}$  • Cycle time $\frac{(2^8-1) \times (m+1)}{fj}$ m: set value of the TAi register lower address n: set value of the TAi register upper address fj: count source frequency
Count start condition	• The TAiS bit of the TABSR register is set to 1 (start counting). • The TAiS bit is 1 and external trigger input from the TAiIN pin • The TAiS bit is 1 and one of the following triggers occurs Timer B2 overflow or underflow Timer Aj overflow or underflow (j = i - 1, except j = 4 if i = 0) Timer Ak overflow or underflow (k = i + 1, except k = 0 if i = 4)
Count stop condition	The TAiS bit is set to 0 (stop counting).
Interrupt request generation timing	On the falling edge of the PWM pulse
TAiIN pin function	I/O port or trigger input
TAiOUT pin function	Pulse output
Read from timer	An undefined value is read when reading the TAi register.
Write to timer	• When not counting Value written to the TAi register is written to both the reload register and counter. • When counting Value written to the TAi register is written to only the reload register (transferred to counter when reloaded next time).
Selectable functions	• Output polarity control The output polarity of the TAiOUT pin is inverted. (While the TAiS bit is set to 0 (stop counting), a high-level signal is output).

i = 0 to 4

Table 15.15 Registers and Settings in PWM Mode (1)

Register	Bit	Setting
PCLKR	PCLK0	Select the count source.
CPSRF	CPSR	Write 1 to reset the clock prescaler.
TCKDIVC0	TCDIV00	Select the clock used prior to dividing timer AB frequency.
PWMFS	PWMFSi	Set to 0.
TACS0 to TACS2	7 to 0	Select the count source.
TAPOFS	POFSi	Select the output polarity.
TAOW	TAiOW	Set to 0.
TAi1	15 to 0	- (setting unnecessary)
TABSR	TAiS	Set to 1 when starting counting. Set to 0 when stopping counting.
ONSF	TAiOS	Set to 0.
	TAZIE	Set to 0.
	TA0TGH to TA0GL	Select a count trigger.
TRGSR	TAiTGH to TAiTGL	Select a count trigger.
UDF	TAiUD	Set to 0.
	TAiP	Set to 0.
TAi	15 to 0	Select the PWM pulse width and cycles.
TAiMR	7 to 0	Refer to the TAiMR register below.

i = 0 to 4

Note:

1. This table does not describe a procedure.

Pulse Width Modulation (PWM) Mode

Timer Ai Mode Register (i = 0 to 4)

b7	b6	b5	b4	b3	b2	b1	b0
						1	1

Symbol	Address	Reset Value
TA0MR to TA4MR	0336h to 033Ah	00h

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 1 1 : PWM mode or programmable output mode	RW
TMOD1			RW
MR0	Pulse output function select bit	0 : No pulse output (TAiOUT pin functions as I/O port) 1 : Pulse output (TAiOUT pin functions as a pulse output pin)	RW
MR1	External trigger select bit	0 : Falling edge of input signal to TAiIN pin 1 : Rising edge of input signal to TAiIN pin	RW
MR2	Trigger select bit	0 : Write 1 to the TAiS bit in the TABSR register 1 : Selected by bits TAiTGH to TAiTGL	RW
MR3	16-/8-bit PWM mode select bit	0 : 16-bit PWM mode 1 : 8-bit PWM mode	RW
TCK0	Count source select bit	b7 b6 0 0 : f1TIMAB or f2TIMAB 0 1 : f8TIMAB 1 0 : f32TIMAB 1 1 : fC32	RW
TCK1			

MR1 (External trigger select bit) (b3)

This bit is enabled when the MR2 bit is 1, and bits TAiTGH to TAiTGL in the ONSF register or TRGSR register are set to 00b (TAiIN pin input).

TCK1 and TCK0 (Count source select bit) (b7-b6)

These bits are enabled when the TCS3 bit or TCS7 bit in registers TACS0 to TACS2 is set to 0 (TCK0 to TCK1 enabled).

Set the PCLK0 bit in the PCLKR register to select f1TIMAB or f2TIMAB.

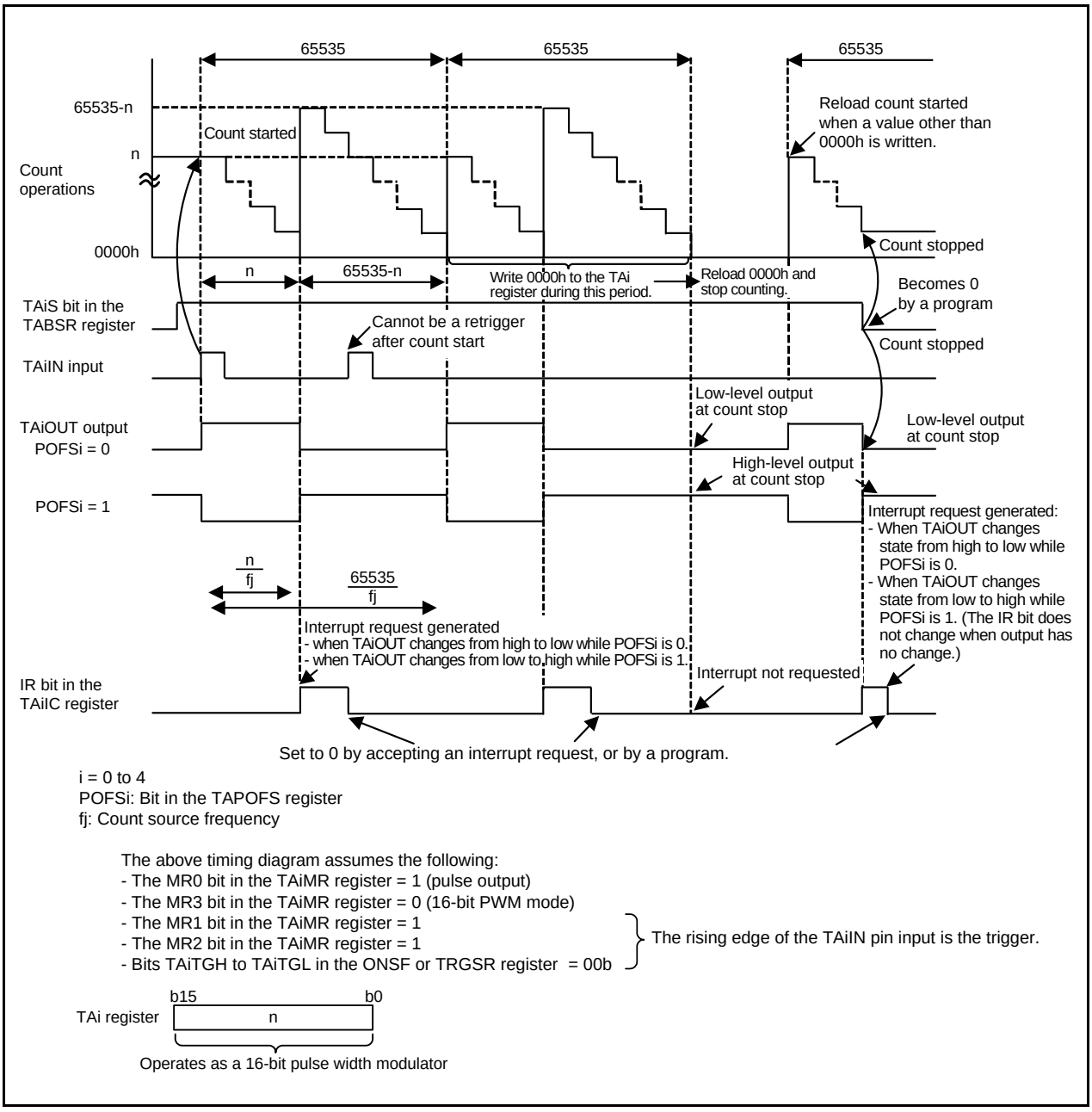


Figure 15.11 Operation Example in 16-Bit Pulse Width Modulation Mode

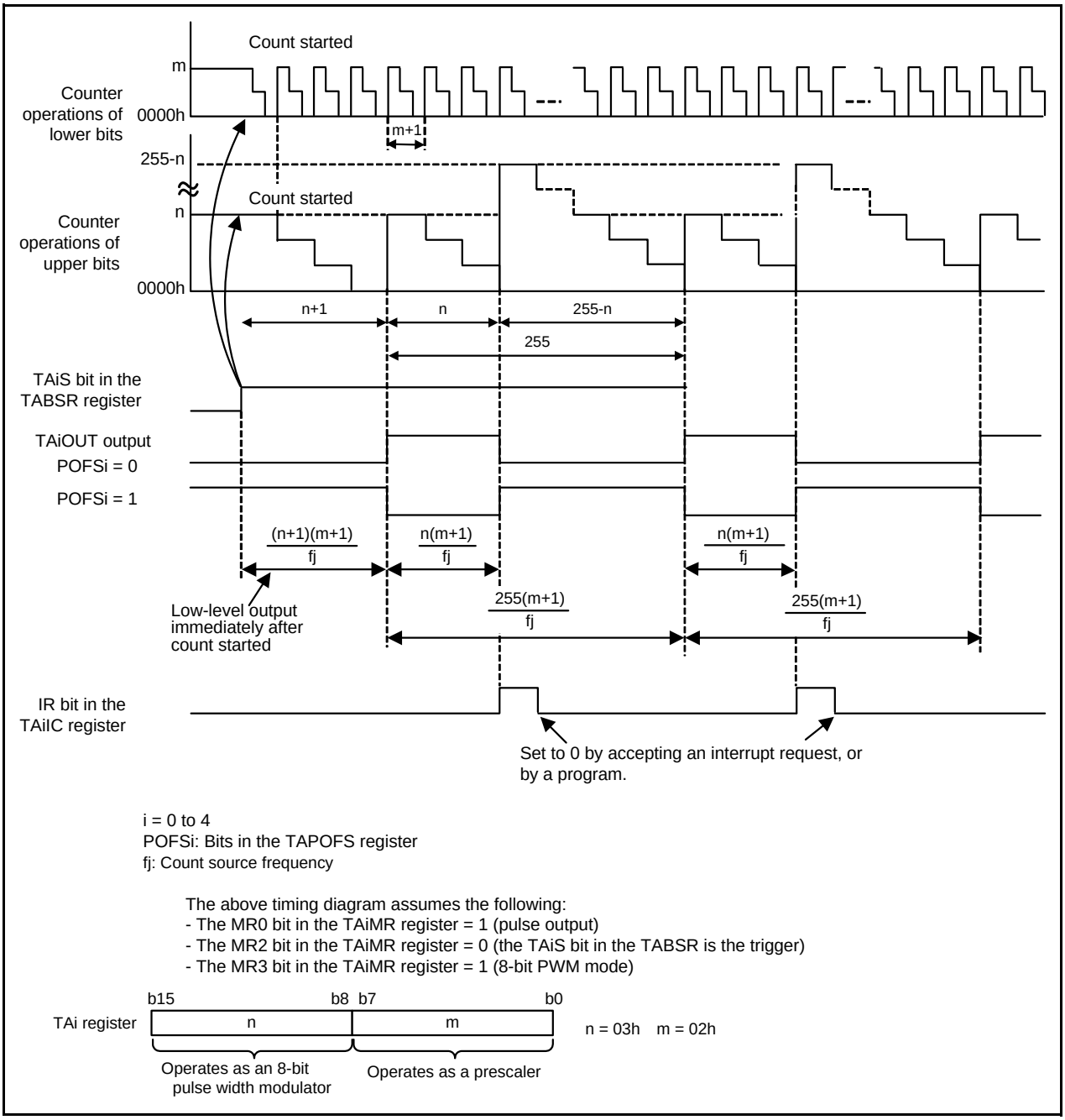
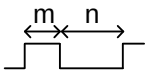


Figure 15.12 Operation Example in 8-Bit Pulse Width Modulation Mode

15.3.7 Programmable Output Mode (Timers A1, A2, and A4)

In programmable output mode, the timer outputs low- and high-levels of pulse width successively. Table 15.16 lists Programmable Output Mode Specifications. Table 15.17 lists Registers and the Setting in Programmable Output Mode. Figure 15.13 shows Operation Example in Programmable Output Mode.

Table 15.16 Programmable Output Mode Specifications

Item	Specification
Count sources	f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32
Count operations	• Decrement • The timer reloads the reload register value at the rising edge of pulse and continues counting • When a trigger occurs while counting, the timer is not affected.
Pulse width	• High-level pulse width $\frac{m}{fj}$  • Low-level pulse width $\frac{n}{fj}$ m: set value of the TAi register n: set value of the TAi1 register fj: count source frequency
Count start conditions	• The TAiS bit of the TABSR register is set to 1 (start counting). • The TAiS bit is 1 and external trigger input from the TAiIN pin • The TAiS bit is 1 and one of the following external triggers occurs: Timer B2 overflow or underflow Timer Aj overflow or underflow (j = i - 1) Timer Ak overflow or underflow (k = i + 1, except k = 0 if i = 4)
Count stop condition	The TAiS bit is set to 0 (stop counting).
Interrupt request generation timing	At the rising edge of pulse
TAiIN pin function	I/O port or trigger input
TAiOUT pin function	Pulse output
Read from timer	An undefined value is read when reading registers TAi and TAi1.
Write to timer	• When writing to registers TAi and TAi1 while not counting, the value is written to both reload register and counter. • When writing to registers TAi and TAi1 while counting, the value is written to the reload register. (transferred to the counter when reloaded next time).
Selectable functions	Output polarity control The output polarity of the TAiOUT pin is inverted. (While the TAiS bit is set to 0 (stop counting), a high-level signal is output.)

i = 1, 2, and 4

Table 15.17 Registers and Settings in Programmable Output Mode (1)

Register	Bit	Function and Setting
PCLKR	PCLK0	Select the count source.
CPSRF	CPSR	Write 1 to reset the clock prescaler.
TCKDIVC0	TCDIV00	Select a clock used prior to dividing timer AB frequency.
PWMFS	PWMFSi	Set to 1.
TACS0 to TACS2	7 to 0	Select the count source.
TAPOFS	POFSi	Select the output polarity.
TAOW	TAiOW	Set to 0 to disable output waveform change, and set to 1 to enable output waveform change.
TAi1	15 to 0	Set a low-level pulse width. (2)
TABSR	TAiS	Set to 1 when starting counting. Set to 0 when stopping counting.
ONSF	TAiOS	Set to 0.
	TAZIE	Set to 0.
	TA0TGH to TA0TGL	Select a count trigger.
TRGSR	TAiTGH to TAiTGL	Select a count trigger.
UDF	TAiUD	Set to 0.
	TAiP	Set to 0.
TAi	15 to 0	Set a high-level pulse width. (2)
TAiMR	7 to 0	Refer to the TAiMR register below.

i = 1, 2, and 4

Notes:

1. This table does not describe a procedure.
2. This applies when the POFSi bit in the TAPOFS register is 0.

Programmable Output Mode

Timer Ai Mode Register (i = 1, 2, 4)

b7	b6	b5	b4	b3	b2	b1	b0
		0				1	1

Symbol	Address	Reset Value
TA0MR to TA4MR	0336h to 033Ah	00h

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 1 1 : PWM mode or programmable output mode	RW
TMOD1			RW
MR0	Pulse output function select bit	0 : No pulse output (TAiOUT pin functions as an I/O port) 1 : Pulse output (TAiOUT pin functions as a pulse output pin)	RW
MR1	External trigger select bit	0 : Falling edge of input signal to TAiIN pin 1 : Rising edge of input signal to TAiIN pin	RW
MR2	Trigger select bit	0 : Write 1 to the TAiS bit in the TABSR register 1 : Selected by bits TAiTGH to TAiTGL	RW
MR3	Set to 0 in programmable output mode		RW
TCK0	Count source select bit	b7 b6 0 0 : f1TIMAB or f2TIMAB 0 1 : f8TIMAB 1 0 : f32TIMAB 1 1 : fC32	RW
TCK1			

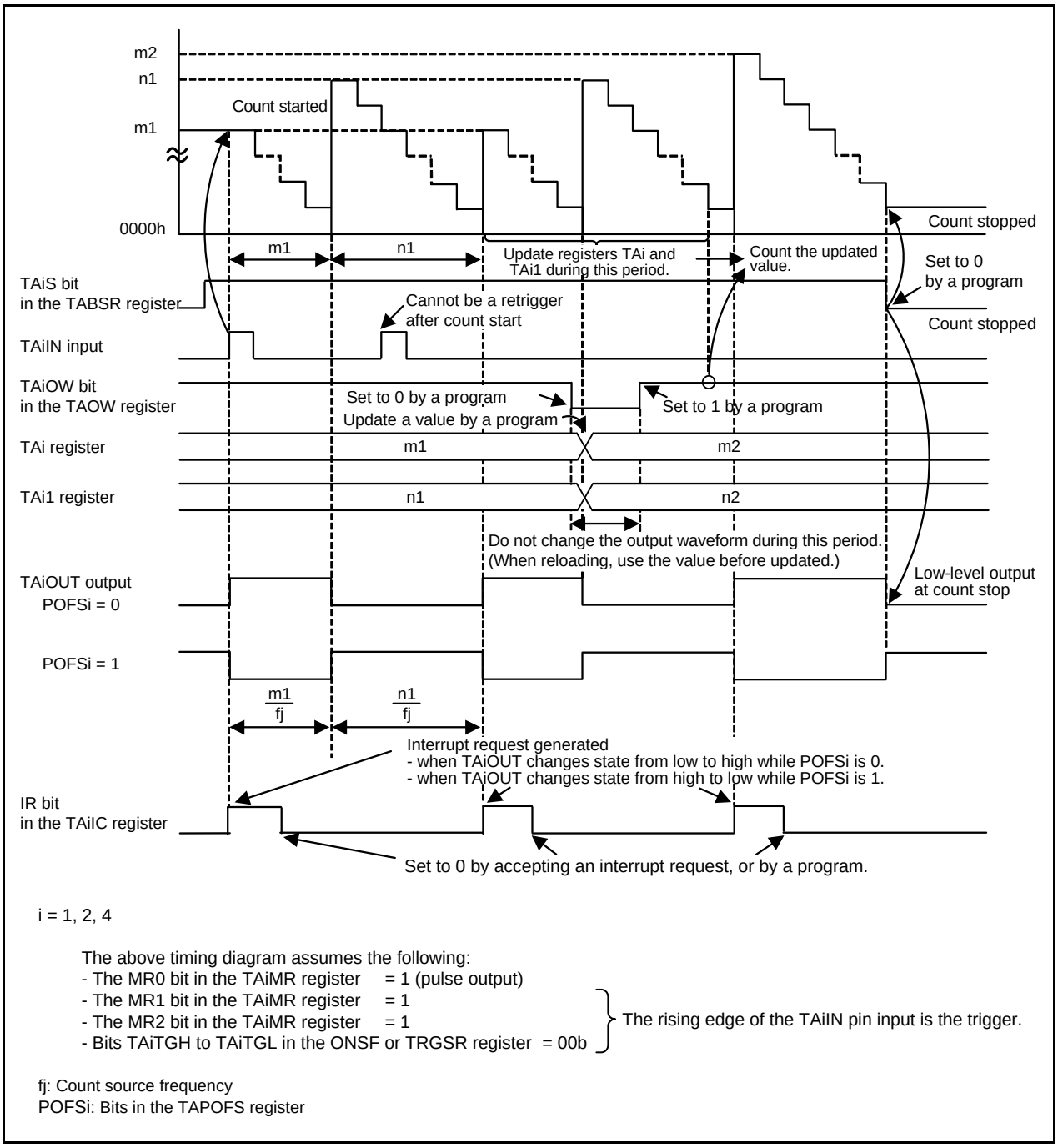
MR1 (External trigger select bit) (b3)

This bit is enabled when the MR2 bit is 1, and bits TAiTGH to TAiTGL in the ONSF register or TRGSR register are set to 00b (TAiIN pin input).

TCK1 and TCK0 (Count source select bit) (b7-b6)

These bits are enabled when the TCS3 bit or TCS7 bit in registers TACS0 to TACS2 is set to 0 (TCK0 to TCK1 enabled).

Set the PCLK0 bit in the PCLKR register to select f1TIMAB or f2TIMAB.



i = 1, 2, 4

The above timing diagram assumes the following:
- The MR0 bit in the TAiMR register = 1 (pulse output)
- The MR1 bit in the TAiMR register = 1
- The MR2 bit in the TAiMR register = 1
- Bits TAiTGH to TAiTGL in the ONSF or TRGSR register = 00b

} The rising edge of the TAiIN pin input is the trigger.

fj: Count source frequency
POFSi: Bits in the TAPOFS register

Figure 15.13 Operation Example in Programmable Output Mode

15.4 Interrupts

Refer to individual operation examples for interrupt request generating timing.
Refer to 12.7 “Interrupt Control” for details of interrupt control. Table 15.18 lists Timer A Interrupt Related Registers.

Table 15.18 Timer A Interrupt Related Registers

Address	Register	Symbol	Reset Value
0055h	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
0058h	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
0059h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b

The IR bit in the TAiIC register may become 1 (interrupt requested) when the TMOD1 bit in the TAiMR register is changed from 0 to 1 (change from timer mode or event counter mode to one-shot timer mode, PWM mode, or programmable output mode). Make sure to follow the procedure below when setting the TMOD1 bit to 1. Refer to 12.13 “Notes on Interrupts” for details.

(1) Set bits ILVL2 to ILVL0 in the TAiIC register to 000b (interrupt disabled).
(2) Set the TAiMR register.
(3) Set the IR bit in the TAiIC register to 0 (interrupt not requested).

15.5 Notes on Timer A

15.5.1 Common Notes on Multiple Modes

15.5.1.1 Register Setting

The timer stops after reset. Set the mode, count source, counter value, etc., using registers TAiMR, TAi, TAi1, UDF, TRGSR, PWMFS, TACS0 to TACS2, TAPOFS, TCKDIVC0, PCLKR, and bits TAZIE, TA0TGL, and TA0TGH in the ONSF register before setting the TAiS bit in the TABSR register to 1 (count started) (i = 0 to 4).

Set the TCDIV00 bit in the TCKDIVC0 register before setting other registers associated with timer A. After changing the TCDIV00 bit, set other registers associated with timer A again.

Always make sure registers TAiMR, UDF, TRGSR, PWMFS, TACS0 to TACS2, TAPOFS, TCKDIVC0, PCLKR, and bits TAZIE, TA0TGL, TA0TGH in the ONSF register are modified while the TAiS bit is 0 (count stopped), regardless of whether after reset or not.

15.5.1.2 Event or Trigger

When bits TAiTGH to TAiTGL in the registers ONSF or TRGSR are 01b, 10b, or 11b, an event or a trigger occurs when an interrupt request of the selected timer is generated. An event or trigger occurs while an interrupt is disabled because an interrupt request signal is generated regardless of the I flag, IPL, or interrupt control registers.

For some modes of the timers selected using bits TAiTGH to TAiTGL, an interrupt request is generated by a source other than overflow or underflow.

For example, when using pulse-period measurement mode or pulse-width measurement mode in timer B2, an interrupt request is generated at an active edge of the measurement pulse. For details, refer to the “Interrupt request generation timing” in each mode’s specification table.

15.5.1.3 Influence of $\overline{SD}$

When a low-level signal is applied to the $\overline{SD}$ pin while the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on $\overline{SD}$ pin enabled), the following pins become high-impedance: P7_2/CLK2/TA1OUT/V/RXD1, P7_3/$\overline{CTS2}$/$\overline{RTS2}$/TA1IN/$\overline{V}$/TXD1, P7_4/TA2OUT/W/LIN0OUT, P7_5/TA2IN/$\overline{W}$/LIN0IN, P8_0/TA4OUT/U/TSUDA, P8_1/TA4IN/$\overline{U}$/TSUDB

15.5.2 Timer A (Timer Mode)

15.5.2.1 Reading the Timer

The counter value can be read from the TAi register at any time while counting. However, if the counter is read at the same time as it is reloaded, the read value is FFFFh. Also, if the counter is read before it starts counting, or after a value is set in the TAi register while not counting, the set value is read.

15.5.3 Timer A (Event Counter Mode)

15.5.3.1 Reading the Timer

While counting, the counter value can be read at any time by reading the TAi register. However, while reloading, FFFFh can be read in underflow, and 0000h in overflow. When the counter is read before it starts counting and after a value is set in the TAi register while not counting, the set value is read.

15.5.4 Timer A (One-Shot Timer Mode)

15.5.4.1 Stop While Counting

When setting the TAiS bit to 0 (count stopped), the following occurs:

- The counter stops counting and reload register values are reloaded.
- The TAiOUT pin outputs a low-level signal when the POFSi bit in the TAPOFS register is 0, and outputs a high-level signal when it is 1.
- After one cycle of the CPU clock, the IR bit in the TAiIC register becomes 1 (interrupt requested).

15.5.4.2 Delay between the Trigger Input and Timer Output

As the one-shot timer output is synchronized with an internally generated count source, when an external trigger is selected, a maximum 1.5 cycle delay of the count source occurs between the trigger input to the TAiIN pin and timer output.

15.5.4.3 Changing Operating Modes

The IR bit becomes 1 when the timer operating mode is set by any of the following:

- Selecting one-shot timer mode after reset
- Changing the operating mode from timer mode to one-shot timer mode
- Changing the operating mode from event counter mode to one-shot timer mode

To use the timer Ai interrupt (IR bit), set the IR bit to 0 after the changes listed above are made.

15.5.4.4 Retrigger

When a trigger occurs while counting, the counter reloads the reload register to continue counting after generating a retrigger and decrementing once. To generate a trigger while counting, generate a retrigger after at least one cycle of the timer count source has elapsed following the previous trigger. When an external trigger is generated, do not generate a retrigger for 300 ns before the count value becomes 0000h. The one-shot timer may stop counting.

15.5.5 Timer A (Pulse Width Modulation Mode)

15.5.5.1 Changing Operating Modes

The IR bit becomes 1 when setting a timer operating mode with any of the following:

- Selecting PWM mode or programmable output mode after reset
- Changing the operating mode from timer mode to PWM mode or programmable output mode
- Changing the operating mode from event counter mode to PWM mode or programmable output mode

To use the timer Ai interrupt (IR bit), set the IR bit to 0 by a program after the changes listed above are made.

15.5.5.2 Stop While Counting

When setting the TAiS bit to 0 (count stopped) during PWM pulse output, the following occur:

When the POFSi bit in the TAPOFS register is 0:

- Counting stops
- When the TAiOUT pin is high, the output level goes low and the IR bit becomes 1.
- When the TAiOUT pin is low, both the output level and the IR bit remain unchanged.

When the POFSi bit in the TAPOFS register is 1:

- Counting stops.
- When the TAiOUT pin output is low, the output level goes high and the IR bit is set to 1.
- When the TAiOUT pin output is high, both the output level and the IR bit remain unchanged.

15.5.6 Timer A (Programmable Output Mode)

15.5.6.1 Changing the Operating Mode

The IR bit becomes 1 when setting a timer operating mode with any of the following:

- Selecting PWM mode or programmable output mode after reset
- Changing the operating mode from timer mode to PWM mode or programmable output mode
- Changing the operating mode from event counter mode to PWM mode or programmable output mode

To use the timer Ai interrupt (IR bit), set the IR bit to 0 by a program after the changes listed above are made.

15.5.6.2 Stop While Counting

When setting the TAiS bit to 0 (count stopped) during pulse output, the following occur:
When the POFSi bit in the TAPOFS register is 0:

- Counting stops.
- When the TAiOUT pin is high, the output level goes low.
- When the TAiOUT pin is low, the output level remains unchanged.
- The IR bit remains unchanged.

When the POFSi bit in the TAPOFS register is 1:

- Counting stops
- When the TAiOUT pin output is low, the output level goes high.
- When the TAiOUT pin output is high, the output level remains unchanged.
- The IR bit remains unchanged.

16. Timer B

Note

Timers B3 to B5 are not available in the 64-pin and 80-pin packages. Do not use these timers with the 64-pin and 80-pin packages.

16.1 Introduction

Timer B consists of timers B0 to B5. Each timer operates independently of the others. Table 16.1 lists Timer B Specifications, Figure 16.1 shows Timer A and B Count Sources, Figure 16.2 shows the Timer B Configuration, Figure 16.3 shows the Timer B Block Diagram, and Table 16.2 lists the I/O Ports.

Table 16.1 Timer B Specifications

Item	Specification
Configuration	16-bit timer × 6
Operating modes	• Timer mode The timer counts an internal count source. • Event counter mode The timer counts pulses from an external device, or overflows and underflows of other timers. • Pulse period/pulse width measurement modes The timer measures pulse periods or pulse widths of an external signal.
Interrupt source	Overflow/underflow/active edge of measurement pulse × 6

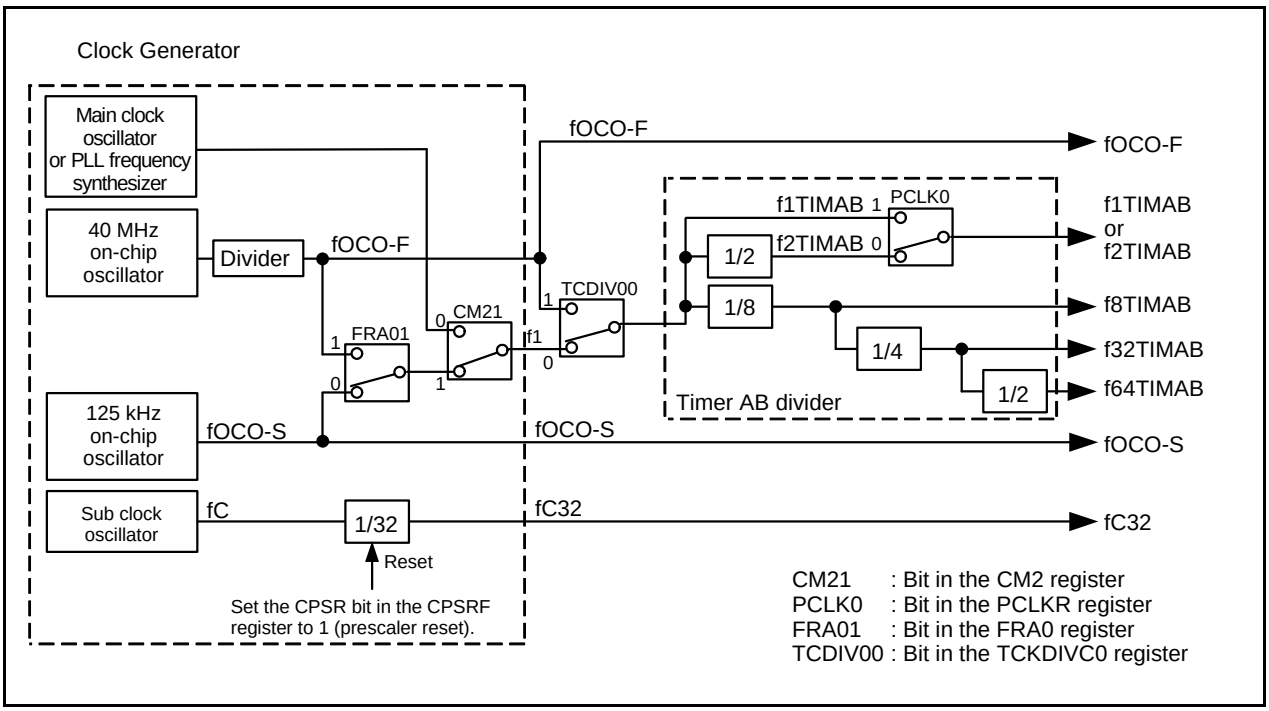


Figure 16.1 Timer A and B Count Sources

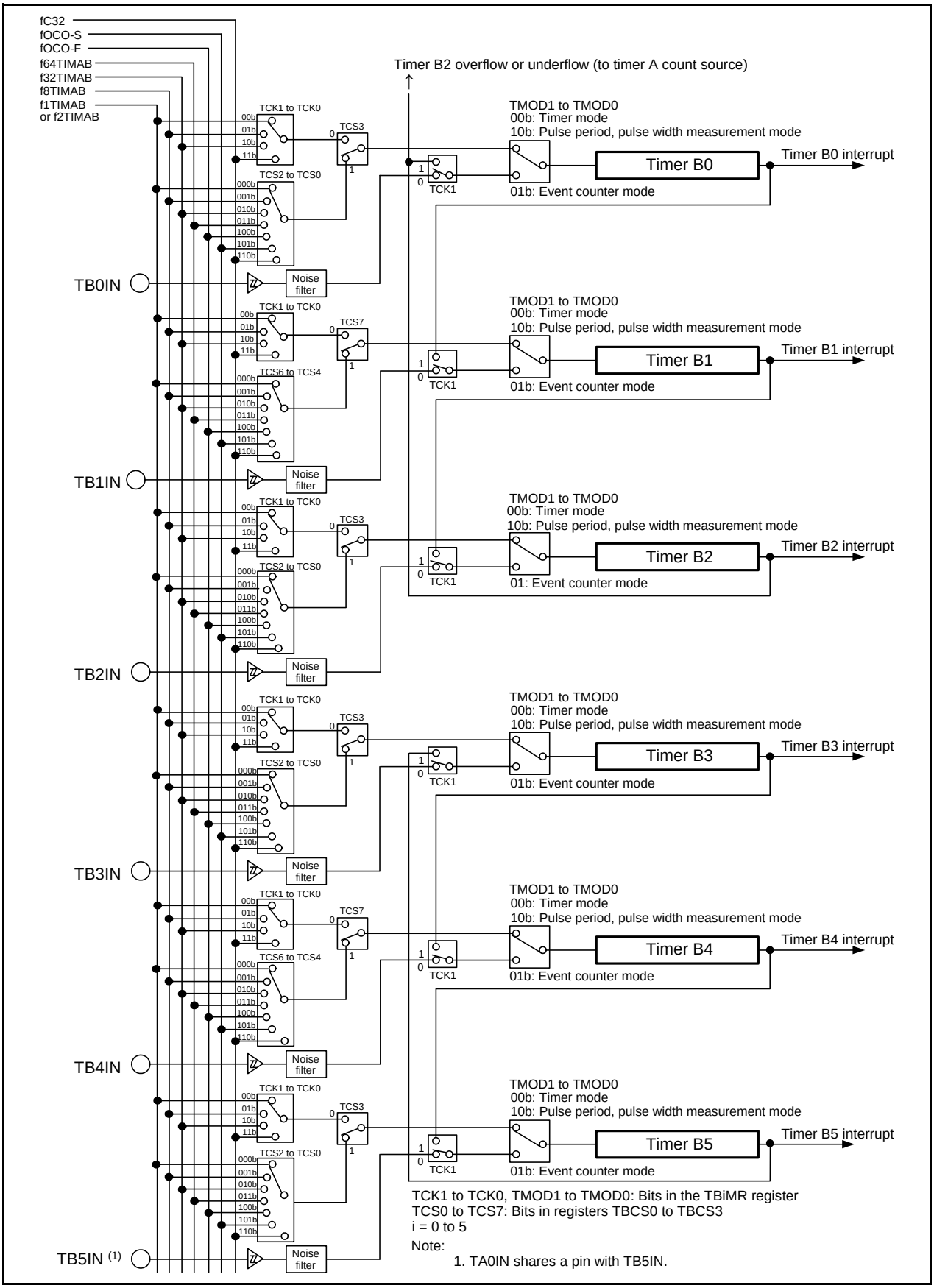
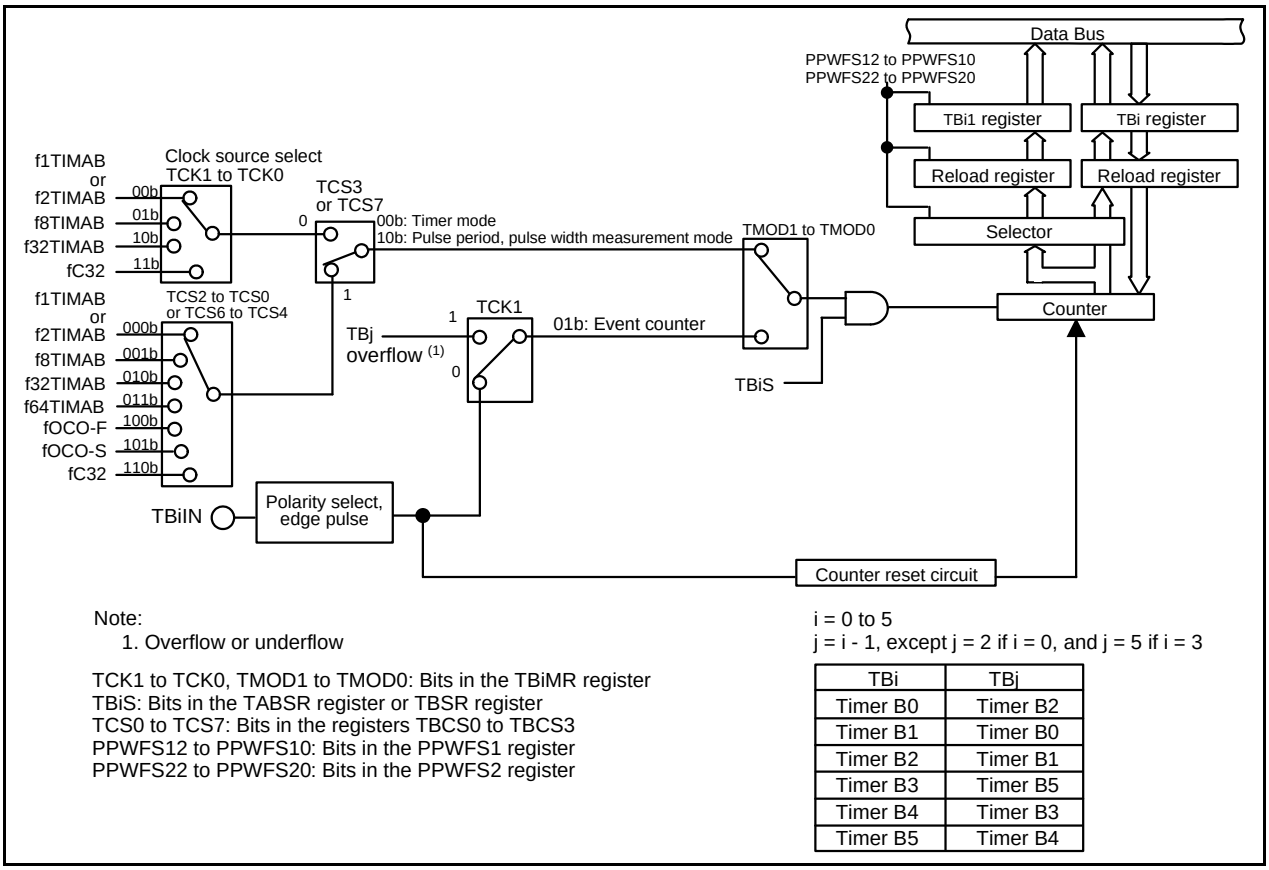


Figure 16.2 Timer B Configuration



TBi	TBj
Timer B0	Timer B2
Timer B1	Timer B0
Timer B2	Timer B1
Timer B3	Timer B5
Timer B4	Timer B3
Timer B5	Timer B4

Figure 16.3 Timer B Block Diagram

Table 16.2 I/O Ports

Pin Name	I/O	Function
TBiIN	Input (1)	Count source input (event counter mode) Measurement pulse input (pulse period measurement mode, pulse width measurement mode)

i = 0 to 5

Note:

1. When using the TBiIN pin for input, set the port direction bit sharing the same pin to 0 (input mode).

16.2 Registers

Table 16.3 lists registers associated with timer B.
Set the TCDIV00 bit in the TCKDIVC0 register before setting other registers associated with timer B. After changing the TCDIV00 bit, set other registers associated with timer B again.
Refer to “registers and the setting” in each mode for registers and bit settings.

Table 16.3 Registers

Address	Register	Symbol	Reset Value
0012h	Peripheral Clock Select Register	PCLKR	0000 0011b
0015h	Clock Prescaler Reset Flag	CPSRF	0XXX XXXXb
01C0h	Timer B0-1 Register	TB01	XXh
01C1h			XXh
01C2h	Timer B1-1 Register	TB11	XXh
01C3h			XXh
01C4h	Timer B2-1 Register	TB21	XXh
01C5h			XXh
01C6h	Pulse Period/Pulse Width Measurement Mode Function Select Register 1	PPWFS1	XXXX X000b
01C8h	Timer B Count Source Select Register 0	TBCS0	00h
01C9h	Timer B Count Source Select Register 1	TBCS1	X0h
01CBh	Timer AB Division Control Register 0	TCKDIVC0	0000 X000b
01E0h	Timer B3-1 Register	TB31	XXh
01E1h			XXh
01E2h	Timer B4-1 Register	TB41	XXh
01E3h			XXh
01E4h	Timer B5-1 Register	TB51	XXh
01E5h			XXh
01E6h	Pulse Period/Pulse Width Measurement Mode Function Select Register 2	PPWFS2	XXXX X000b
01E8h	Timer B Count Source Select Register 2	TBCS2	00h
01E9h	Timer B Count Source Select Register 3	TBCS3	X0h
0300h	Timer B3/B4/B5 Count Start Flag	TBSR	000X XXXXb
0310h	Timer B3 Register	TB3	XXh
0311h			XXh
0312h	Timer B4 Register	TB4	XXh
0313h			XXh
0314h	Timer B5 Register	TB5	XXh
0315h			XXh
031Bh	Timer B3 Mode Register	TB3MR	00XX 0000b
031Ch	Timer B4 Mode Register	TB4MR	00XX 0000b
031Dh	Timer B5 Mode Register	TB5MR	00XX 0000b
0320h	Count Start Flag	TABSR	00h
0330h	Timer B0 Register	TB0	XXh
0331h			XXh
0332h	Timer B1 Register	TB1	XXh
0333h			XXh
0334h	Timer B2 Register	TB2	XXh
0335h			XXh
033Bh	Timer B0 Mode Register	TB0MR	00XX 0000b
033Ch	Timer B1 Mode Register	TB1MR	00XX 0000b
033Dh	Timer B2 Mode Register	TB2MR	00XX 0000b

16.2.1 Peripheral Clock Select Register (PCLKR)

Peripheral Clock Select Register

b7	b6	b5	b4	b3	b2	b1	b0
0	0		0	0	0		

Symbol	Address	Reset Value
PCLKR	0012h	00000011b

Bit Symbol	Bit Name	Function	RW
PCLK0	Timers A, B, S, multi-master I^2C-bus interface clock select bit (clock source for timers A , B, S, dead time timer, and multi-master I^2C-bus interface)	0: f2TIMAB/f2IIC 1: f1TIMAB/f1IIC	RW
PCLK1	SI/O clock select bit (clock source for UART0 to UART4)	0: f2SIO 1: f1SIO	RW
— (b4-b2)	Reserved bits	Set to 0.	RW
PCLK5	Clock output function extension bit	0: Selected by setting bits CM01 and CM00 in the CM0 register 1: Outputs f1	RW
— (b7-b6)	Reserved bits	Set to 0.	RW

Write to the PCLKR register after setting the PRC0 bit in the PRCR register to 1 (write enabled).

16.2.2 Clock Prescaler Reset Flag (CPSRF)

Clock Prescaler Reset Flag

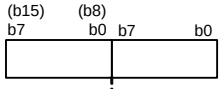
b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	Reset Value
CPSRF	0015h	0XXX XXXXb

Bit Symbol	Bit Name	Function	RW
— (b6-b0)	No register bits. If necessary, set to 0. The read values are undefined.		—
CPSR	Clock prescaler reset flag	Setting this bit to 1 initializes the prescaler for the timekeeping clock. (The read value is 0.)	RW

16.2.3 Timer Bi Register (TBi) (i = 0 to 5)

Timer Bi Register (i = 0 to 5)



Symbol	Address	Reset Value
TB0	0331h to 0330h	XXXXh
TB1	0333h to 0332h	XXXXh
TB2	0335h to 0334h	XXXXh
TB3	0311h to 0310h	XXXXh
TB4	0313h to 0312h	XXXXh
TB5	0315h to 0314h	XXXXh

Mode	Function	Setting Range	RW
Timer mode	When n = setting value, counter cycle: $\frac{(n + 1)}{fj}$	0000h to FFFFh	RW
Event counter mode	When n = setting value, n + 1 count	0000h to FFFFh	RW
Pulse period measurement mode, Pulse width measurement mode	Set an initial value. Measures a pulse period or width. Read the counter value while counting.	0000h to FFFFh	RW

fj : Count source frequency

Access this register in 16-bit units.

Event Counter Mode

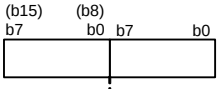
The timer counts pulses from an external device, or overflows or underflows of other timers.

Pulse Period Measurement Mode, Pulse Width Measurement Mode

Set these modes when the TBiS bit in the TABSR or TBSR register is 0 (count stopped).
These modes become read only (RO) when the TBiS bit in the TABSR or TBSR register is 1 (count started).
The counter starts counting the count source at an active edge of the measurement pulse, transfers the count value to a register at the next active edge, and continues counting.
The measurement result can be read by reading the TBi register when bits PPWFS12 to PPWFS10 in the PPWFS1 register and bits PPWFS22 to PPWFS20 in the PPWFS2 register are 0.
While counting, the counter value can be read by reading the TBi register when bits PPWFS12 to PPWFS10 and bits PPWFS22 to PPWFS20 are 1.

16.2.4 Timer Bi-1 Register (TBi1) (i = 0 to 5)

Timer Bi-1 Register (i = 0 to 5)



Symbol	Address	Reset Value
TB01	01C1h to 01C0h	XXXXh
TB11	01C3h to 01C2h	XXXXh
TB21	01C5h to 01C4h	XXXXh
TB31	01E1h to 01E0h	XXXXh
TB41	01E3h to 01E2h	XXXXh
TB51	01E5h to 01E4h	XXXXh

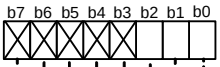
Mode	Function	Setting Range	RW
Pulse period measurement mode Pulse width measurement mode	Measures a pulse period or width	0000h to FFFFh	RO

Access this register in 16-bit units.

When bits PPWFS12 to PPWFS10 in the PPWFS1 register and bits PPWFS22 to PPWFS20 in the PPWFS2 register are 1, the measurement result can be read by reading the TBi-1 register. When these bits are 0, the value in this register is undefined.

16.2.5 Pulse Period/Pulse Width Measurement Mode Function Select Register i (PPWFSi) (i = 1, 2)

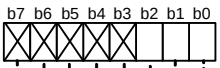
Pulse Period/Pulse Width Measurement Mode Function Select Register 1



Symbol	Address	Reset Value
PPWFS1	01C6h	XXXX X000b

Bit Symbol	Bit Name	Function	RW
PPWFS10	Timer B0 pulse period/pulse width measurement mode function select bit	0 : Measurement result is stored in the TB0 register. The TB01 register is not used 1 : The counter value is read from the TB0 register. Measurement result is stored in the TB01 register	RW
PPWFS11	Timer B1 pulse period/pulse width measurement mode function select bit	0 : Measurement result is stored in the TB1 register. The TB11 register is not used 1 : The counter value is read from the TB1 register. Measurement result is stored in the TB11 register	RW
PPWFS12	Timer B2 pulse period/pulse width measurement mode function select bit	0 : Measurement result is stored in the TB2 register. The TB21 register is not used 1 : The counter value is read from the TB2 register. Measurement result is stored in the TB21 register	RW
— (b7-b3)	No register bits. If necessary, set to 0. The read value is undefined.		—

Pulse Period/Pulse Width Measurement Mode Function Select Register 2



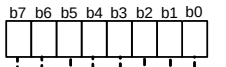
Symbol	Address	Reset Value
PPWFS2	01E6h	XXXX X000b

Bit Symbol	Bit Name	Function	RW
PPWFS20	Timer B3 pulse period/pulse width measurement mode function select bit	0 : Measurement result is stored in the TB3 register. The TB31 register is not used 1 : The counter value is read from the TB3 register. Measurement result is stored in the TB31 register	RW
PPWFS21	Timer B4 pulse period/pulse width measurement mode function select bit	0 : Measurement result is stored in the TB4 register. The TB41 register is not used 1 : The counter value is read from the TB4 register. Measurement result is stored in the TB41 register	RW
PPWFS22	Timer B5 pulse period/pulse width measurement mode function select bit	0 : Measurement result is stored in the TB5 register. The TB51 register is not used 1 : The counter value is read from the TB5 register. Measurement result is stored in the TB51 register	RW
— (b7-b3)	No register bits. If necessary, set to 0. The read value is undefined.		—

Enabled in pulse period measurement mode or pulse width measurement mode.

16.2.6 Timer B Count Source Select Register i (TBCSi) (i = 0 to 3)

Timer B Count Source Select Register 0, Timer B Count Source Select Register 2

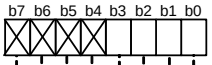


Symbol	Address	Reset Value
TBCS0	01C8h	00h
TBCS2	01E8h	00h

Bit Symbol	Bit Name	Function	RW
TCS0	TBi count source select bit	b2 b1 b0 0 0 0 : f1TIMAB or f2TIMAB 0 0 1 : f8TIMAB 0 1 0 : f32TIMAB 0 1 1 : f64TIMAB 1 0 0 : fOCO-F 1 0 1 : fOCO-S 1 1 0 : fC32 1 1 1 : Do not set	RW
TCS1			RW
TCS2			RW
TCS3	TBi count source option specified bit	0 : TCK0 to TCK1 enabled, TCS0 to TCS2 disabled 1 : TCK0 to TCK1 disabled, TCS0 to TCS2 enabled	RW
TCS4	TBj count source select bit	b6 b5 b4 0 0 0 : f1TIMAB or f2TIMAB 0 0 1 : f8TIMAB 0 1 0 : f32TIMAB 0 1 1 : f64TIMAB 1 0 0 : fOCO-F 1 0 1 : fOCO-S 1 1 0 : fC32 1 1 1 : Do not set	RW
TCS5			RW
TCS6			RW
TCS7	TBj count source option specified bit	0 : TCK0 to TCK1 enabled, TCS4 to TCS6 disabled 1 : TCK0 to TCK1 disabled, TCS4 to TCS6 enabled	RW

TBCS0 register: i = 0, j = 1; TBCS2 register: i = 3, j = 4

Timer B Count Source Select Register 1, Timer B Count Source Select Register 3



Symbol	Address	Reset Value
TBCS1	01C9h	X0h
TBCS3	01E9h	X0h

Bit Symbol	Bit Name	Function	RW
TCS0	TBi count source select bit	b2 b1 b0 0 0 0: f1TIMAB or f2TIMAB 0 0 1: f8TIMAB 0 1 0: f32TIMAB 0 1 1: f64TIMAB 1 0 0: fOCO-F 1 0 1: fOCO-S 1 1 0: fC32 1 1 1: Do not set	RW
TCS1			RW
TCS2			RW
TCS3	TBi count source option specified bit	0: TCK0 to TCK1 enabled, TCS0 to TCS2 disabled 1: TCK0 to TCK1 disabled, TCS0 to TCS2 enabled	RW
— (b7-b4)	No register bits. If necessary, set to 0. The read value is undefined.		—

TBCS1 register: i = 2; TBCS3 register: i = 5

TCS2-TCS0 (TBi count source select bit) (b2-b0)
TCS6-TCS4 (TBj count source select bit) (b6-b4)

Select f1TIMAB or f2TIMAB by setting the PCLK0 bit in the PCLKR register.

16.2.7 Timer AB Division Control Register 0 (TCKDIVC0)

Timer AB Division Control Register 0

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	X	0	0	

Symbol: TCKDIVC0 | Address: 01CBh | Reset Value: 0000 X000b

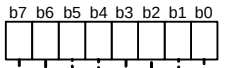
Bit Symbol	Bit Name	Function	RW
TCDIV00	Clock select prior to timer AB division bit	0 : f1 1 : fOCO-F	RW
— (b2-b1)	Reserved bits	Set to 0	RW
— (b3)	No register bit. If necessary, set to 0. The read value is undefined.		—
— (b7-b4)	Reserved bits	Set to 0	RW

TCDIV00 (Clock select prior to timer AB division bit) (b0)

Set the TCDIV00 bit while timers A and B are stopped.
Set the TCDIV00 bit before setting other registers associated with timer B.
After changing the TCDIV00 bit, set other registers associated with timer B again.

16.2.8 Count Start Flag (TABSR)
Timer B3/B4/B5 Count Start Flag (TBSR)

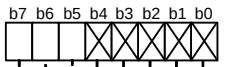
Count Start Flag



Symbol	Address	Reset Value
TABSR	0320h	00h

Bit Symbol	Bit Name	Function	RW
TA0S	Timer A0 count start flag	0 : Count stopped 1 : Count started	RW
TA1S	Timer A1 count start flag		RW
TA2S	Timer A2 count start flag		RW
TA3S	Timer A3 count start flag		RW
TA4S	Timer A4 count start flag		RW
TB0S	Timer B0 count start flag		RW
TB1S	Timer B1 count start flag		RW
TB2S	Timer B2 count start flag		RW

Timer B3/B4/B5 Count Start Flag

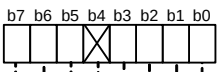


Symbol	Address	Reset Value
TBSR	0300h	000X XXXXb

Bit Symbol	Bit Name	Function	RW
— (b4-b0)	No register bits. If necessary, set to 0. The read value is undefined.		—
TB3S	Timer B3 count start flag	0 : Stop counting 1 : Start counting	RW
TB4S	Timer B4 count start flag		RW
TB5S	Timer B5 count start flag		RW

16.2.9 Timer Bi Mode Register (TBiMR) (i = 0 to 5)

Timer Bi Mode Register (i = 0 to 5)



Symbol	Address	Reset Value
TB0MR to TB2MR	033Bh to 033Dh	00XX 0000b
TB3MR to TB5MR	031Bh to 031Dh	00XX 0000b

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 0 0 : Timer mode 0 1 : Event counter mode 1 0 : Pulse period measurement mode Pulse width measurement mode 1 1 : Do not set	RW
TMOD1			RW
MR0	Function varies with the operation mode		RW
MR1			RW
— (b4)	No register bit. If necessary, set to 0. The read value is undefined.		—
MR3	Function varies with the operation mode		RO
TCK0	Count source select bit (function varies with the operation mode)		RW
TCK1			RW

16.3 Operations

16.3.1 Common Operations

16.3.1.1 Operating Clock

The count source for each timer acts as a clock, controlling such timer operations as counting and reloading.

16.3.1.2 Counter Reload Timing

Timer Bi starts counting from the value (n) set in the TBi register. The TBi register consists of a counter and a reload register. The counter starts decrementing the count source from n, reloads a value in the reload register at the next count source after the value becomes 0000h, and continues decrementing. The value written in the TBi register is reflected in the counter and the reload register at the following timings.

- When the count is stopped
- Between when the count starts and the first count source is input
  The value written to the TBi register is immediately written to the counter and the reload register.

- After the count starts and the first count source is input
  The value written to the TBi register is immediately written to the reload register.
  The counter continues counting and reloads the value in the reload register at the next count source after the value becomes 0000h.

16.3.1.3 Count Source

Internal clocks are counted in timer mode, pulse period measurement mode, and pulse width measurement mode. Refer to Figure 16.1 “Timer A and B Count Sources” for details. Table 16.4 lists Timer B Count Sources.

f1 is any of the clocks listed below. Refer to 8. “Clock Generator” for details.

- Main clock divided by 1 (no division)
- PLL clock divided by 1 (no division)
- fOCO-S divided by 1 (no division)
- fOCO-F divided by 1 (no division)

Table 16.4 Timer B Count Sources

Count Source	Bit Setting Value				Remarks
	PCLK0	TCS3 TCS7	TCS2 to TCS0 TCS6 to TCS4	TCK1 to TCK0	
f1TIMAB	1	0	-	00b	f1 or fOCO-F (1)
		1	000b	-	
f2TIMAB	0	0	-	00b	f1 divided by 2 or fOCO-F divided by 2 (1)
		1	000b	-	
f8TIMAB	-	0	-	01b	f1 divided by 8 or fOCO-F divided by 8 (1)
		1	001b	-	
f32TIMAB	-	0	-	10b	f1 divided by 32 or fOCO-F divided by 32 (1)
		1	010b	-	
f64TIMAB	-	1	011b	-	f1 divided by 64 or fOCO-F divided by 64 (1)
fOCO-F	-	1	100b	-	fOCO-F
fOCO-S	-	1	101b	-	fOCO-S
fC32	-	0	-	11b	fC32
		1	110b	-	

PCLK0: Bit in the PCLKR register

TCS7 to TCS0: Bits in registers TBCS0 toTBCS3

TCK1 to TCK0: Bits in the TBiMR register (i = 0 to 5)

Note:

1. Select f1 or fOCO-F by setting the TCDIV00 bit in the TCKDIVC0 register.

16.3.2 Timer Mode

In timer mode, the timer counts an internally generated count source. Table 16.5 lists Timer Mode Specifications, Table 16.6 lists Registers and Setting in Timer Mode, and Figure 16.4 shows an Operation Example in Timer Mode.

Table 16.5 Timer Mode Specifications

Item	Specification
Count sources	f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32
Count operations	• Decrement • When the timer underflows, it reloads the reload register value and continues counting.
Counter cycles	$\frac{1}{(n+1)}$ n: setting value of the TBi register 0000h to FFFFh
Count start condition	Set the TBiS bit to 1 (start counting).
Count stop condition	Set the TBiS bit to 0 (stop counting).
Interrupt request generation timing	Timer underflow
TBiIN pin function	I/O port
Read from timer	Count value can be read by reading the TBi register.
Write to timer	• When not counting The value written to the TBi register is written to both the reload register and the counter. • When counting The value written to the TBi register is only written to the reload register (transferred to the counter when reloaded next).

i = 0 to 5
TBiS: Bit in the TABSR or TBSR register

Table 16.6 Registers and Settings in Timer Mode (1)

Register	Bit	Function and Setting
PCLKR	PCLK0	Select the count source.
CPSRF	CPSR	Write 1 to reset the clock prescaler.
TBi1	15 to 0	- (setting unnecessary)
PPWFS1 to PPWFS2	PPWFS12 to PPWFS10 PPWFS22 to PPWFS20	Set to 0.
TCKDIVC0	TCDIV00	Select the clock used prior to timer AB frequency dividing.
TBCS0 to TBCS3	7 to 0	Select the count source.
TABSR TBSR	TBiS	Set to 1 when starting counting. Set to 0 when stopping counting.
TBi	15 to 0	Set the count value.
TBiMR	7 to 0	Refer to the TBiMR register below.

i = 0 to 5
Note:
1. This table does not describe a procedure.

Timer Mode

Timer Bi Mode Register (i = 0 to 5)

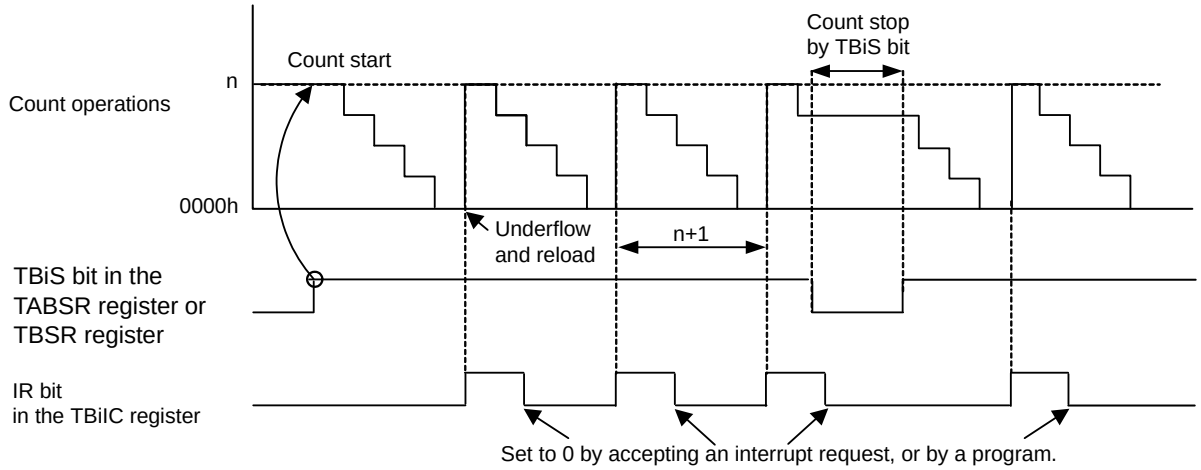
b7	b6	b5	b4	b3	b2	b1	b0
			X	0	0	0	0

Symbol	Address	Reset Value
TB0MR to TB2MR	033Bh to 033Dh	00XX 0000b
TB3MR to TB5MR	031Bh to 031Dh	00XX 0000b

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 0 0 : Timer mode	RW
TMOD1			RW
MR0	Set to 0 in timer mode.		RW
MR1			RW
— (b4)	No register bit. If necessary, set to 0. The read value is undefined.		—
MR3	Write 0 in timer mode. The read value is undefined in timer mode.		RO
TCK0	Count source select bit	b7 b6 0 0 : f1TIMAB or f2TIMAB 0 1 : f8TIMAB 1 0 : f32TIMAB 1 1 : fC32	RW
TCK1			RW

TCK1 and TCK0 (Count source select bit) (b7-b6)

These bits are enabled when the TCS3 or TCS7 bit in registers TBCS0 to TBCS3 is set to 0 (bits TCK0 to TCK1 enabled).
Select f1TIMAB or f2TIMAB by the PCLK0 bit in the PCLKR register.



i = 0 to 5

The above assumes the following:

- The value in the TBi register (n) = 0004h

Figure 16.4 Operation Example in Timer Mode

16.3.3 Event Counter Mode

In event counter mode, the timer counts pulses from an external device, or overflows and underflows of other timers. Table 16.7 lists Event Counter Mode Specifications, Table 16.8 lists Registers and Settings in Event Counter Mode, and Figure 16.5 shows an Operation Example in Event Counter Mode.

Table 16.7 Event Counter Mode Specifications

Item	Specification
Count sources	• External signals input to TBiIN pin (active edge can be selected by a program: rising edge, falling edge, or both rising and falling edges) • Timer Bj overflow or underflow
Count operations	• Decrement • When the timer underflows, it reloads the reload register value and continues counting.
Number of counts	$\frac{1}{(n+1)}$ n: setting value of the TBi register 0000h to FFFFh
Count start condition	Set the TBiS bit to 1 (start counting).
Count stop condition	Set the TBiS bit to 0 (stop counting).
Interrupt request generation timing	Timer underflow
TBiIN pin function	Count source input
Read from timer	Count value can be read by reading the TBi register.
Write to timer	• When not counting The value written to the TBi register is written to both the reload register and the counter. • When counting The value written to the TBi register is written to only reload register (transferred to counter when reloaded next).

i = 0 to 5 j = i - 1, except j = 2 if i = 0; j = 5 if i = 3
TBiS: Bit in the TABSR or TBSR register

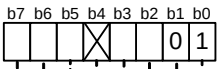
Table 16.8 Registers and Settings in Event Counter Mode (1)

Register	Bit	Function and Setting
PCLKR	PCLK0	- (setting unnecessary)
CPSRF	CPSR	Write 1 to reset the clock prescaler.
TBi1	15 to 0	- (setting unnecessary)
PPWFS1 to PPWFS2	PPWFS12 to PPWFS10 PPWFS22 to PPWFS20	Set to 0.
TCKDIVC0	TCDIV00	- (setting unnecessary)
TBCS0 to TBCS3	7 to 0	- (setting unnecessary)
TABSR TBSR	TBiS	Set to 1 when starting counting. Set to 0 when stopping counting.
TBi	15 to 0	Set the count value.
TBiMR	7 to 0	Refer to the TBiMR register below.

i = 0 to 5
Note:
1. This table does not describe a procedure.

Event Counter Mode

Timer Bi Mode Register (i = 0 to 5)



Symbol	Address	Reset Value
TB0MR to TB2MR	033Bh to 033Dh	00XX 0000b
TB3MR to TB5MR	031Bh to 031Dh	00XX 0000b

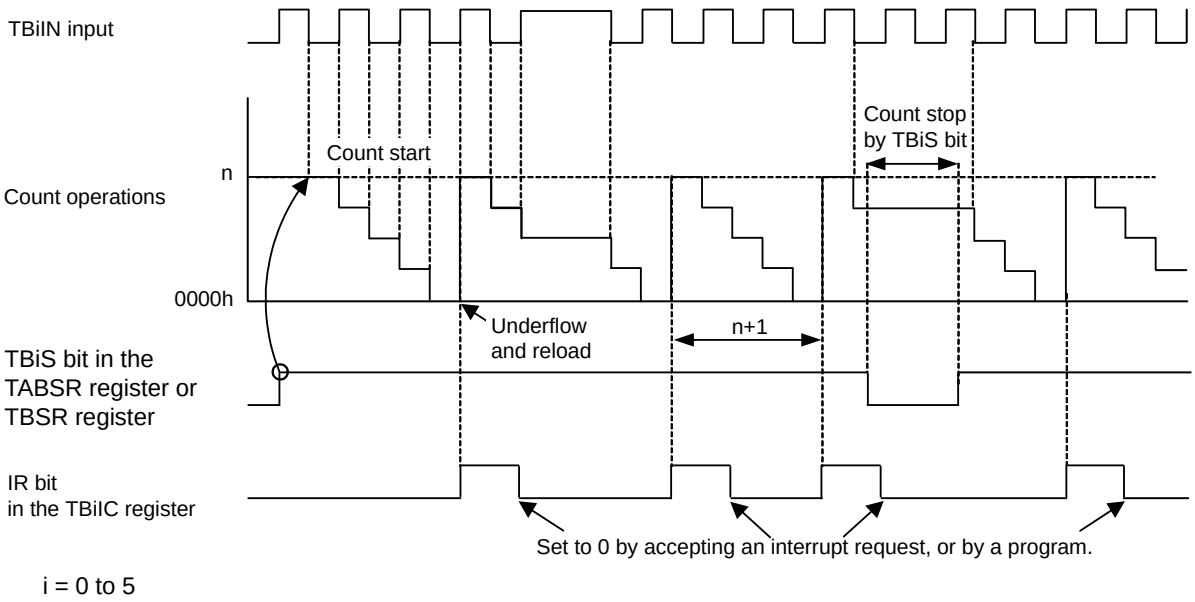
Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 0 1 : Event counter mode	RW
TMOD1			RW
MR0	Count polarity select bit	b3 b2 0 0 : Counts falling edges of an external signal 0 1 : Counts rising edges of an external signal 1 0 : Counts falling and rising edges of an external signal 1 1 : Do not set	RW
MR1			RW
— (b4)	No register bit. If necessary, set to 0. The read value is undefined.		—
MR3	Write 0 in event counter mode. The read value is undefined in event counter mode		RO
TCK0	Disabled in event counter mode. Set 0 or 1.		RW
TCK1	Event clock select bit	0 : Input from TBiIN pin 1 : Timer Bj (j = i - 1; however, j = 2 if i = 0, j = 5 if i = 3)	RW

MR1 and MR0 (Count polarity select bit) (b3-b2)

These bits are enabled when the TCK1 bit is 0 (input from TBiIN pin). When the TCK1 bit is 1 (timer Bj), these bits can be set to 0 or 1.

TCK1 (Event clock select bit) (b7)

When the TCK1 bit is 1, an event occurs when an interrupt request of timer Bj (j = i - 1; however, j = 2 if i = 0, j = 5 if i = 3) is generated. An event occurs while an interrupt is disabled because an interrupt request signal is generated regardless of the I flag, IPL, or interrupt control registers



i = 0 to 5

The above assumes the following:

- Bits MR1 to MR0 in the TBiMR register = 10b (the falling edge and rising edge of an external signal).
- The TCK1 bit in the TBiMR register = 0 (input signals from the TBiIN pin counted).
- The value in the TBi register (n) = 0004h.

Figure 16.5 Operation Example in Event Counter Mode

16.3.4 Pulse Period/Pulse Width Measurement Modes

In pulse period and pulse width measurement modes, the timer measures the pulse period or pulse width of an external signal. Table 16.9 lists Specifications of Pulse Period/Pulse Width Measurement Modes, Table 16.10 lists Registers and Settings in Pulse Period/Pulse Width Measurement Modes, Figure 16.6 shows Operation Example in Pulse Period Measurement Mode, and Figure 16.7 shows an Operation Example in Pulse Width Measurement Mode.

Table 16.9 Specifications of Pulse Period/Pulse Width Measurement Modes

Item	Specification
Count sources	f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32
Count operations	• Increment • The counter value is transferred to the reload register at an active edge of the measurement pulse. The counter value becomes 0000h and count continues.
Count start condition	Set the TBiS bit to 1 (start counting).
Count stop condition	Set the TBiS bit to 0 (stop counting).
Interrupt request generation timing (3)	• When an active edge of measurement pulse is input (1) • Timer overflow. The MR3 bit in the TBiMR register becomes 1 (overflowed) at the same time an overflow occurs.
TBiIN pin function	Measurement pulse input
Read from timer	When bits PPWFS12 to PPWFS10 and PPWFS22 to PPWFS20 in registers PPWFS1 and PPWFS2 are 0 • Value of the reload register (measurement result) can be read by reading the TBi register. (2) When bits PPWFS12 to PPWFS10 and PPWFS22 to PPWFS20 in registers PPWFS1 and PPWFS2 register are 1 • Value of the counter (counter value) can be read by reading the TBi register. • Value of the reload register (measurement result) can be read by reading the TBi1 register.
Write to timer	When not counting, the value written to the TBi register is written to both the reload register and counter.

i = 0 to 5

TBiS: Bit in the TABSR or TBSR register

Notes:

1. No interrupt request is generated when the first active edge is input after the timer starts counting.
2. The value read from the TBi register is undefined until the second active edge is input after the timer starts counting.
3. When timer Bi in pulse-period measurement mode or pulse-width measurement mode is used as an event or trigger for timer A or timer B other than timer Bi, an event or trigger occurs at both the overflow and active edge of the measurement pulse.

Table 16.10 Registers and Settings in Pulse Period/Pulse Width Measurement Modes (1)

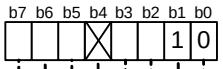
Register	Bit	Function and Setting
PCLKR	PCLK0	Select the count source.
CPSRF	CPSR	Write 1 to reset the clock prescaler.
TBi1	15 to 0	Measurement result can be read when the bits in the PPWFS1 or PPWFS2 register corresponding to timer Bi are 1.
PPWFS1 to PPWFS2	PPWFS12 to PPWFS10 PPWFS22 to PPWFS20	Set to 1 to read the counter value while counting.
TCKDIVC0	TCDIV00	Select the clock used prior to timer AB frequency dividing.
TBCS0 to TBCS3	7 to 0	Select the count source.
TABSR TBSR	TBiS	Set to 1 when starting counting. Set to 0 when stopping counting.
TBi	15 to 0	Set the initial value. The measurement result can be read when the bits in the PPWFS1 or PPWFS2 register corresponding to timer Bi are 0. The counter value can be read when the bits in the PPWFS1 or PPWFS2 register corresponding to timer Bi are 1.
TBiMR	7 to 0	Refer to the TBiMR register below.

i = 0 to 5

Note:

1. This table does not describe a procedure.

Pulse Period/Pulse Width Measurement Modes
Timer Bi Mode Register (i = 0 to 5)



Symbol	Address	Reset Value
TB0MR to TB2MR	033Bh to 033Dh	00XX 0000b
TB3MR to TB5MR	031Bh to 031Dh	00XX 0000b

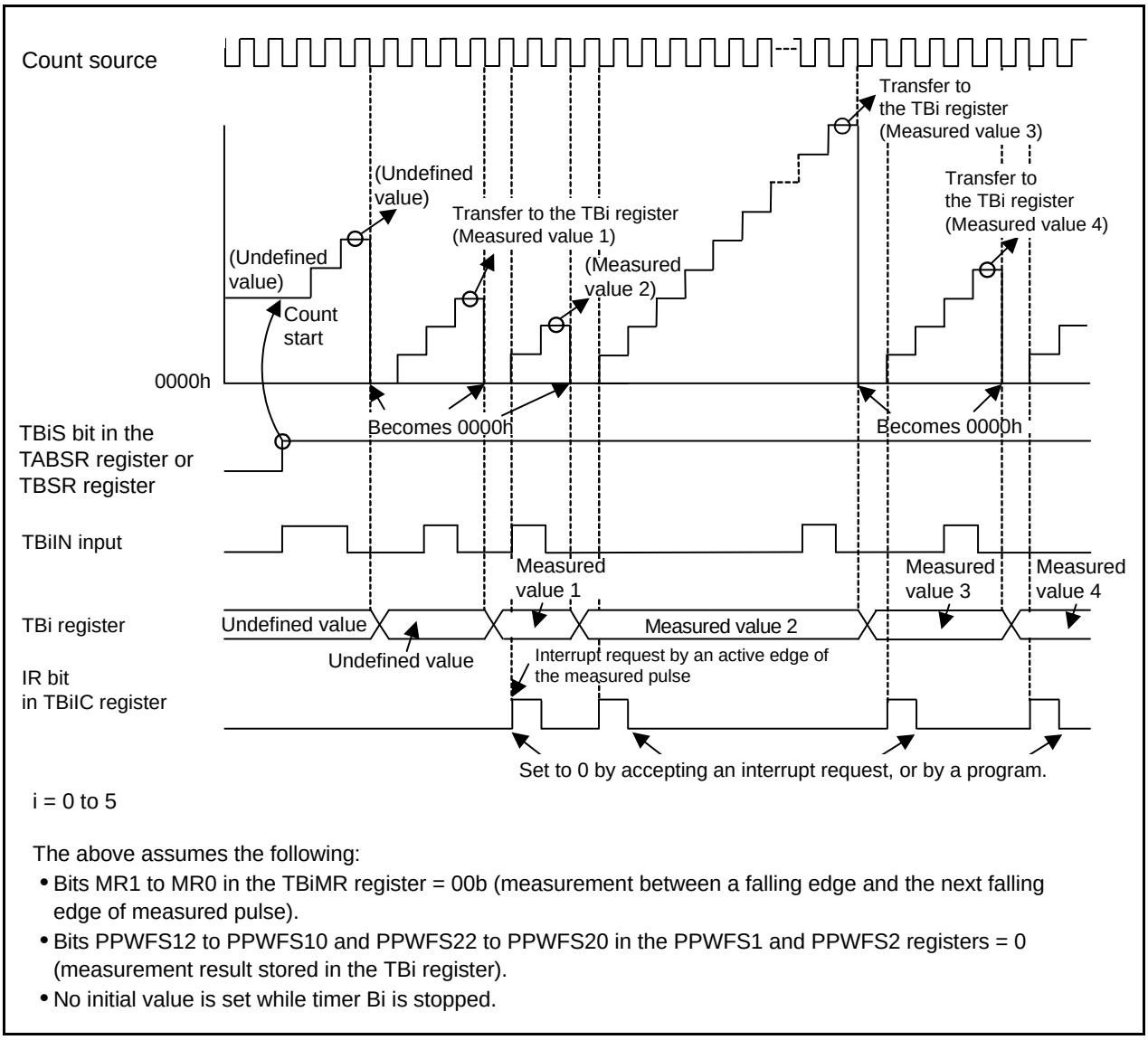
Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 1 0 : Pulse period/pulse width measurement modes	RW
TMOD1			RW
MR0	Measurement mode select bit	b3 b2 0 0 : Pulse period measurement (measurement between a falling edge and the next falling edge of measured pulse) 0 1 : Pulse period measurement (measurement between a rising edge and the next rising edge of measured pulse) 1 0 : Pulse width measurement (measurement between a falling edge and the next rising edge of measured pulse and between a rising edge and the next falling edge) 1 1 : Do not set	RW
MR1			RW
— (b4)	No register bit. If necessary, set to 0. The read value is undefined.		—
MR3	Timer Bi overflow flag	0 : No overflow 1 : Overflow	RO
TCK0	Count source select bit	b7 b6 0 0 : f1TIMAB or f2TIMAB 0 1 : f8TIMAB 1 0 : f32TIMAB 1 1 : fC32	RW
TCK1			RW

MR3 (Timer Bi overflow flag) (b5)

This bit is undefined after reset. The MR3 bit becomes 0 (no overflow) by writing to the TBiMR register. The MR3 bit cannot be set to 1 by a program.

TCK1 and TCK0 (Count source select bit) (b7-b6)

These bits are enabled when the TCS3 bit or TCS7 bit in registers TBCS0 to TBCS3 is set to 0 (TCK0, TCK1 enabled).
Set the PCLK0 bit in the PCLKR register to select f1TIMAB or f2TIMAB.

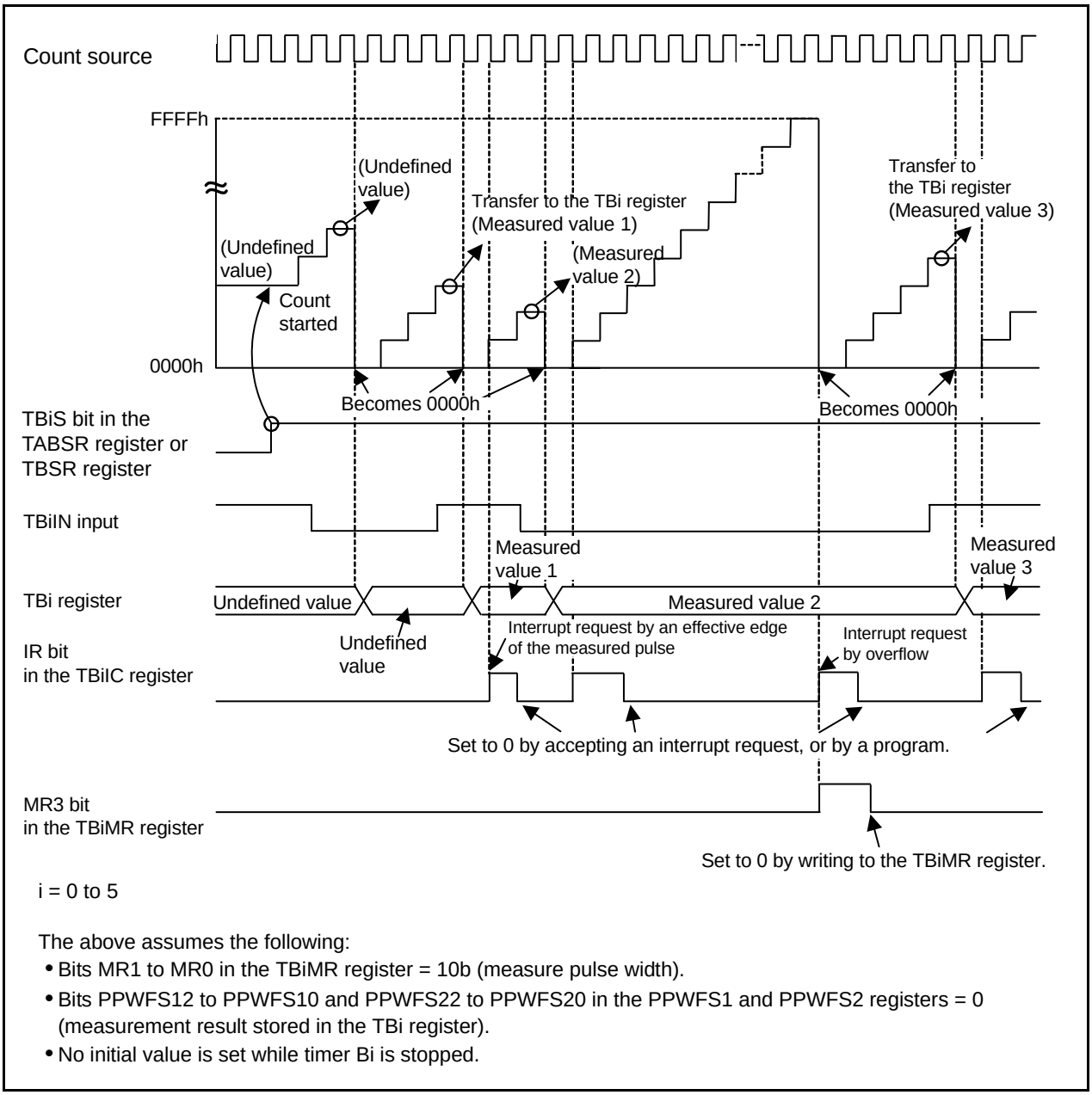


i = 0 to 5

The above assumes the following:

- Bits MR1 to MR0 in the TBiMR register = 00b (measurement between a falling edge and the next falling edge of measured pulse).
- Bits PPWFS12 to PPWFS10 and PPWFS22 to PPWFS20 in the PPWFS1 and PPWFS2 registers = 0 (measurement result stored in the TBi register).
- No initial value is set while timer Bi is stopped.

Figure 16.6 Operation Example in Pulse Period Measurement Mode



i = 0 to 5

The above assumes the following:

- Bits MR1 to MR0 in the TBiMR register = 10b (measure pulse width).
- Bits PPWFS12 to PPWFS10 and PPWFS22 to PPWFS20 in the PPWFS1 and PPWFS2 registers = 0 (measurement result stored in the TBi register).
- No initial value is set while timer Bi is stopped.

Figure 16.7 Operation Example in Pulse Width Measurement Mode

16.4 Interrupts

Refer to individual operation examples for interrupt request generating timing.
Refer to 12.7 “Interrupt Control” for details of interrupt control. Table 16.11 lists Timer B Interrupt Related Registers.

Table 16.11 Timer B Interrupt Related Registers

Address	Register	Symbol	Reset Value
0045h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
0046h	Timer B4 Interrupt Control Register	TB4IC	XXXX X000b
0047h	Timer B3 Interrupt Control Register	TB3IC	XXXX X000b
005Ah	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
005Bh	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b

16.5 Notes on Timer B

16.5.1 Common Notes on Multiple Modes

16.5.1.1 Register Setting

The timer is stopped after reset. Set the mode, count source, etc., using registers TBiMR, TBCS0 to TBCS3, TBi, TCKDIVC0, PCLKR, PPWFS1, and PPWFS2 before setting the TBiS bit in the TABSR or TBSR register to 1 (count started) (i = 0 to 5).
Rewrite registers TBiMR, TBCS0 to TBCS3, TCKDIVC0, PCLKR, PPWFS1, and PPWFS2 while the TBiS bit is 0 (count stopped), regardless of whether after reset or not.

16.5.2 Timer B (Timer Mode)

16.5.2.1 Reading the Timer

While counting, the counter value can be read at any time by reading the TBi register. However, FFFFh is read while reloading. When the counter is read before it starts counting and after a value is set in the TBi register while not counting, the set value is read.

16.5.3 Timer B (Event Counter Mode)

16.5.3.1 Reading the Timer

While counting, the counter value can be read at any time by reading the TBi register. However, FFFFh is read while reloading. When the counter is read before it starts counting and after a value is set in the TBi register while not counting, the set value is read.

16.5.3.2 Event

When the TCK1 bit in the TBiMR register is 1, an event occurs when an interrupt request of the selected timer is generated. An event or trigger occurs while an interrupt is disabled because an interrupt request signal is generated regardless of the I flag, IPL, or interrupt control registers.
When the timer selected by the TCK1 bit uses pulse-period measurement mode or pulse-width measurement mode, an interrupt request is generated at an active edge of the measurement pulse.

16.5.4 Timer B (Pulse Period/Pulse Width Measurement Modes)

16.5.4.1 MR3 Bit in the TBiMR Register

To clear the MR3 bit to 0 by writing to the TBiMR register while the TBiS bit is 1 (count started), be sure to set the same value as previously set to bits TMOD0, TMOD1, MR0, MR1, TCK0, and TCK1, and set bit 4 to 0.

16.5.4.2 Interrupts

The IR bit in the TBiIC register becomes 1 (interrupt requested) when an active edge of a measurement pulse is input, or timer Bi overflows (i = 0 to 5). The source of an interrupt request can be determined by setting the MR3 bit in the TBiMR register within the interrupt routine.
Use the IR bit in the TBiIC register to detect overflows only. Use the MR3 bit only to determine the interrupt source.

16.5.4.3 Event or Trigger

When timer Bi in pulse-period measurement mode or pulse-width measurement mode is used as an event or trigger for timer A or timer B other than timer Bi, an event or trigger occurs at both the overflow and active edge of the measurement pulse.

16.5.4.4 Operations between Count Start and the First Measurement

When a count is started and the first active edge is input, an undefined value is transferred to the reload register. At this time, a timer Bi interrupt request is not generated.

The value of the counter is undefined after reset. If the count is started in this state, the MR3 bit may become 1 and a timer Bi interrupt request may be generated after the count starts before an active edge is input. When a value is set in the TBi register while the TBiS bit is 0 (count stopped), the same value is written to the counter.

16.5.4.5 Pulse Period Measurement Mode

When an active edge and overflow are generated simultaneously, input is not recognized at the active edge because an interrupt request is generated only once. Use this mode so an overflow is not generated, or use pulse width measurement mode.

16.5.4.6 Pulse Width Measurement Mode

In pulse width measurement, pulse widths are measured successively. Check whether the measurement result is a high-level width or a low-level width in the user program.
When an interrupt request is generated, read the TBiIN pin level in the interrupt routine, and check whether it is the edge of an input pulse or overflow. The TBiIN pin level can be read from bits in the register of ports sharing a pin.

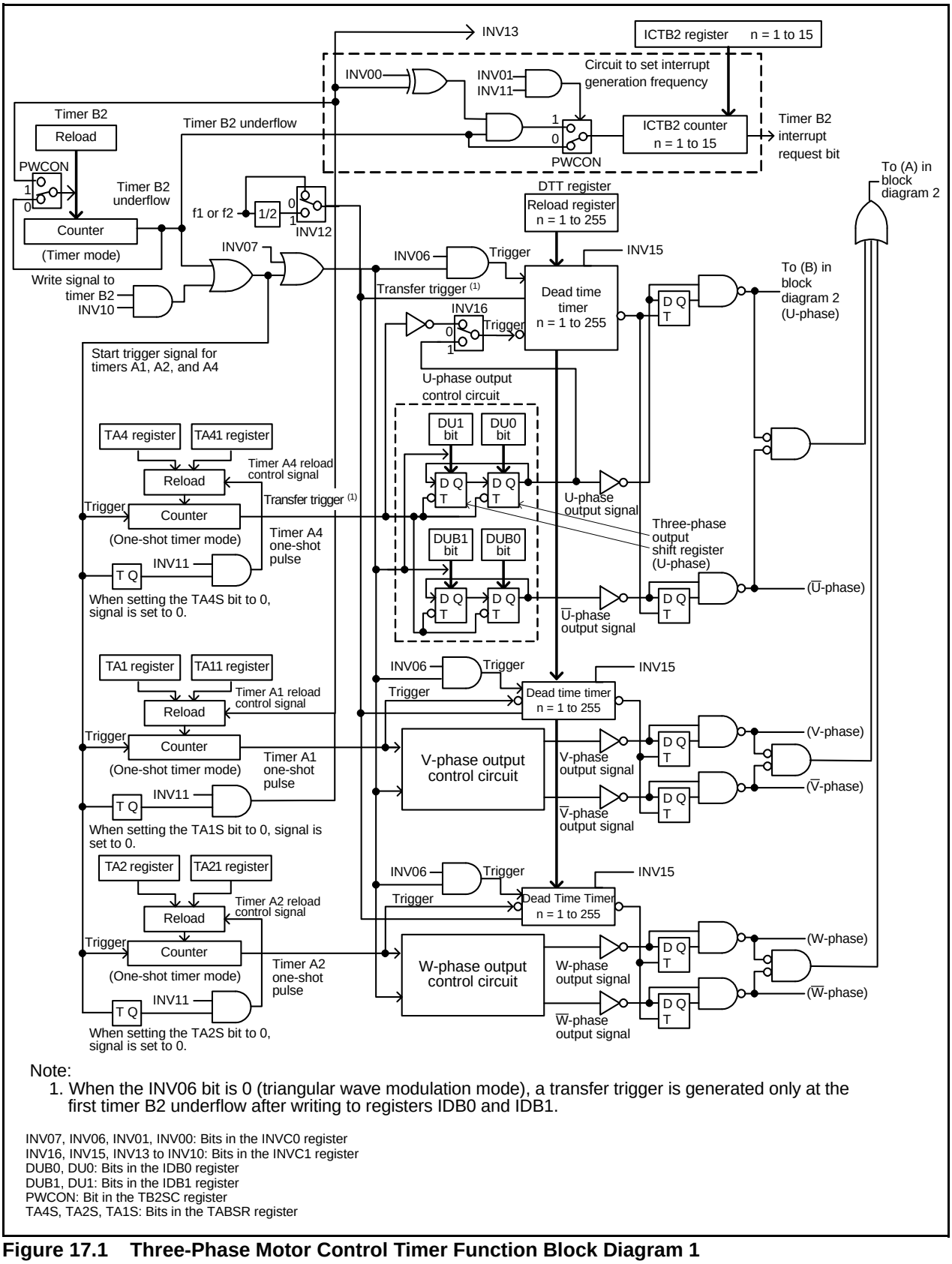
17. Three-Phase Motor Control Timer Function

17.1 Introduction

Timers A1, A2, A4, and B2 can be used to output three-phase motor drive waveforms.
Table 17.1 lists Three-Phase Motor Control Timer Function Specifications. Three-Phase Motor Control Timer Function Block Diagrams are shown in Figure 17.1 and Figure 17.2. Table 17.2 lists I/O Ports.

Table 17.1 Three-Phase Motor Control Timer Function Specifications

Item	Specification
Operation modes	• Triangular wave modulation three-phase mode 0 Three-phase PWM waveform of triangular wave modulation is output. Output data is updated every half cycle of the carrier wave, and an output waveform is generated. • Triangular wave modulation three-phase mode 1 Three-phase PWM waveform of triangular wave modulation is output. Output data is updated every cycle of the carrier wave, and an output waveform is generated. • Sawtooth wave modulation mode Three-phase PWM waveform of sawtooth wave modulation is output.
Three-phase PWM waveform output pins	6 (U, $\overline{U}$, V, $\overline{V}$, W, $\overline{W}$)
Forced cutoff input	Input a low-level signal to the $\overline{SD}$ pin
Used timers	Timers A4, A1, A2 (used in one-shot timer mode) Timer A4: U-/$\overline{U}$-phase waveform control Timer A1: V-/$\overline{V}$-phase waveform control Timer A2: W-/$\overline{W}$-phase waveform control Timer B2 (used in timer mode) Carrier wave cycle control Dead time timer (three 8-bit timers and shared reload register) Dead time control
Output waveform	Triangular wave modulation, sawtooth wave modulation • All high or low outputs for one cycle supported • Output logic of high- and low-side turn-on signals can be set separately.
Carrier wave cycle	Triangular wave modulation : $\frac{(m+1)\times 2}{fi}$ Sawtooth wave modulation : $\frac{m+1}{fi}$ m: Setting value of the TB2 register, 0000h to FFFFh fi: Count source frequency (f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32)
Three-phase PWM output width	Triangular wave modulation : $\frac{n\times 2}{fi}$ Sawtooth wave modulation : $\frac{n}{fi}$ n: Setting value of registers TA4, TA1, and TA2 (of registers TA4, TA41, TA1, TA11, TA2, and TA21 when setting the INV11 bit to 1), 0001h to FFFFh fi: Count source frequency (f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32)
Dead time (width)	$\frac{p}{fi}$ or no dead time p: Setting value of the DTT register, 01h to FFh fi: Count source frequency (f1TIMAB, f2TIMAB, f1TIMAB divided by 2, f2TIMAB divided by 2)
Active level	Selectable either active high or active low
Simultaneous conduction prevention function	Simultaneous conduction prevention Simultaneous conduction detection
Interrupt frequency	A timer B2 interrupt is generated every carrier wave cycle to every 15 carrier wave cycles.



Note:
1. When the INV06 bit is 0 (triangular wave modulation mode), a transfer trigger is generated only at the first timer B2 underflow after writing to registers IDB0 and IDB1.

INV07, INV06, INV01, INV00: Bits in the INVC0 register
INV16, INV15, INV13 to INV10: Bits in the INVC1 register
DUB0, DU0: Bits in the IDB0 register
DUB1, DU1: Bits in the IDB1 register
PWCON: Bit in the TB2SC register
TA4S, TA2S, TA1S: Bits in the TABSR register

Figure 17.1 Three-Phase Motor Control Timer Function Block Diagram 1

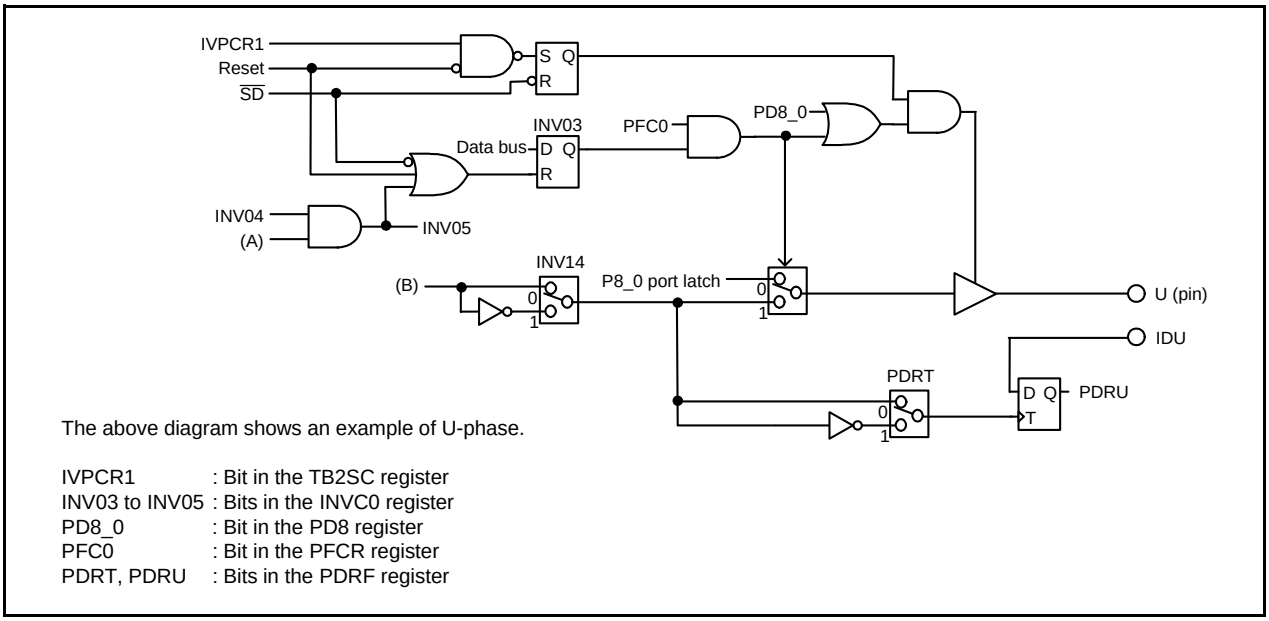


Figure 17.2 Three-Phase Motor Control Timer Function Block Diagram 2

Table 17.2 I/O Ports

Pin Name	I/O	Function
U, $\overline{U}$, V, $\overline{V}$, W, $\overline{W}$	Output	Three-phase PWM waveform output
$\overline{SD}$	Input (1)	Forced cutoff input
IDU, IDV, IDW	Input (2)	Position-data-retain function input

Notes:
1. Set the port direction bits which share pins to 0 (input mode). When not using the three-phase output forced cutoff function, input a high-level signal to the $\overline{SD}$ pin.
2. Set the port direction bits which share pins to 0 (input mode).

17.2 Registers

Refer to “registers and settings” in each mode for register and bit settings.
Three-phase motor control timer function uses timers A1, A2, A4, and B2. For other registers related to timers A1, A2, A4, and B2, refer to 15. “Timer A” and 16. “Timer B”.

Table 17.3 Registers

Address	Register	Symbol	Reset Value
01DAh	Three-Phase Protect Control Register	TPRC	00h
0302h	Timer A1-1 Register	TA11	XXh
0303h			XXh
0304h	Timer A2-1 Register	TA21	XXh
0305h			XXh
0306h	Timer A4-1 Register	TA41	XXh
0307h			XXh
0308h	Three-Phase PWM Control Register 0	INVC0	00h
0309h	Three-Phase PWM Control Register 1	INVC1	00h
030Ah	Three-Phase Output Buffer Register 0	IDB0	XX11 1111b
030Bh	Three-Phase Output Buffer Register 1	IDB1	XX11 1111b
030Ch	Dead Time Timer	DTT	XXh
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XXh
030Eh	Position-Data-Retain Function Control Register	PDRF	XXXX 0000b
0318h	Port Function Control Register	PFCR	0011 1111b
0328h	Timer A1 Register	TA1	XXh
0329h			XXh
032Ah	Timer A2 Register	TA2	XXh
032Bh			XXh
032Eh	Timer A4 Register	TA4	XXh
032Fh			XXh
0334h	Timer B2 Register	TB2	XXh
0335h			XXh
033Eh	Timer B2 Special Mode Register	TB2SC	X000 0000b

17.2.1 Timer B2 Register (TB2)

Timer B2 Register

(b15) (b8)
b7 b0 b7 b0

Symbol	Address	Reset Value
TB2	0335h to 0334h	Undefined

Function	Setting Range	RW
If the setting value is n, the counter frequency is $\frac{n+1}{fj}$ Timers A1, A2, and A4 start each time an underflow occurs.	0000h to FFFFh	RW

fj : Count source frequency

Read and write in 16-bit units.
The carrier wave cycle is determined by this counter. Timer B2 underflow is a one-shot trigger of timers A1, A2, and A4.
In three-phase mode 1, the reload timing of the TB2 register can be selected by setting the PWCON bit in the TB2SC register.

17.2.2 Timer Ai, Ai-1 Register (TAi, TAi1) (i = 1, 2, 4)

Timer Ai, Ai-1 Register (i = 1, 2, 4)

(b15) (b8)
b7 b0 b7 b0

Symbol	Address	Reset Value
TA1, TA2, TA4	0329h to 0328h, 032Bh to 032Ah, 032Fh to 032Eh	Undefined
TA11, TA21, TA41	0303h to 0302h, 0305h to 0304h, 0307h to 0306h	Undefined

Function	Setting Range	RW
If the setting value is n, the timer stops when the nth count source is counted after a start trigger is generated. Output signals of each phase change when timers A1, A2, and A4 stop.	0000h to FFFFh	WO

Write to these registers in 16-bit units. Use the MOV instruction to set registers TAi and TAi1. If the TAi or TAi1 register is set to 0000h, no counters start and no timer Ai interrupt is generated.
The TAi or TAi1 register is used to determine waveforms of U-, V-, and W-phases. It is triggered by timer B2 underflow, and operates in one-shot timer mode.
Registers TA1, TA2, and TA4 are used in sawtooth wave modulation mode and three-phase mode 0 of triangular wave modulation mode.
Registers TA1, TA2, TA4, TA11, TA21, and TA41 are used in three-phase mode 1 of triangular wave modulation mode.
When the INV15 bit in the INVC1 register is set to 0 (dead time enabled), some high- and low-side turn-on signals, whose output level changes from inactive to active, switch the output level when the dead time timer stops.
In three-phase mode 1, the value of the TAi1 register is counted first. Then, the values of registers TAi and TAi1 are counted alternately.

17.2.3 Three-Phase PWM Control Register 0 (INVC0)

Three-Phase PWM Control Register 0

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	Reset Value
INVC0	0308h	00h

Bit Symbol	Bit Name	Function	RW
INV00	ICTB2 count condition select bit	b1 b0 0 0 : Timer B2 underflow 0 1 : 1 0 : Timer B2 underflow when timer A1 reload control signal is 0 1 1 : Timer B2 underflow when timer A1 reload control signal is 1	RW
INV01			RW
INV02	Three-phase motor control timer function enable bit	0 : Three-phase motor control timer function not used 1 : Three-phase motor control timer function used	RW
INV03	Three-phase motor control timer output control bit	0 : Three-phase motor control timer output disabled 1 : Three-phase motor control timer output enabled	RW
INV04	High- and low-side simultaneous turn-on disable bit	0 : Simultaneous turn-on enabled 1 : Simultaneous turn-on disabled	RW
INV05	High- and low-side simultaneous turn-on detect flag	0 : Not detected 1 : Detected	RW
INV06	Modulation mode select bit	0 : Triangular wave modulation mode 1 : Sawtooth wave modulation mode	RW
INV07	Software trigger select bit	A transfer trigger is generated when the INV07 bit is set to 1. A trigger to the dead time timer is also generated when setting the INV06 bit to 1. The read value is 0.	RW

Set the INVC0 register after the PRC1 bit in the PRCR register is set to 1 (write enabled). Rewrite bits INV00 to INV02, INV04, and INV06 when timers A1, A2, A4, and B2 are stopped.

INV01 and INV00 (ICTB2 count condition select bit) (b1-b0)

Bits INV00 and INV01 are enabled only when the INV11 bit in the INVC1 register is 1 (three-phase mode 1).

To set the INV01 bit to 1, set the ICTB2 register first, and then set the INV01 bit to 1. Set the TA1S bit in the TABSR register (timer A1 count start flag) to 1 prior to the first timer B2 underflow.

When the INV11 bit is 0 (three-phase mode 0), the timer B2 underflow is counted regardless of the values of bits INV01 to INV00.

INV02 (Three-phase motor control timer function enable bit) (b2)

Set the INV02 bit to 1 to operate the dead time timer, U-, V- and, W-phase output control circuits, and the ICTB2 counter.

INV03 (Three-phase motor control timer output control bit) (b3)

Conditions to become 0:

- The INV04 bit is 1 (simultaneous turn-on disabled) and the INV05 bit is 1 (simultaneous turn-on detected).
- The INV03 bit is set to 0 by a program.
- The signal applied to the $\overline{SD}$ pin is low.

INV05 (High- and low-side simultaneous turn-on detect flag) (b5)

The INV05 bit cannot be set to 1 by a program. Set the INV04 bit to 0 when setting the INV05 bit to 0.

INV06 (Modulation mode select bit) (b6)

The following table lists items influenced by the INV06 bit.

Table 17.4 Influence of the INV06 Bit

Item	INV06 is 0	INV06 is 1
Mode	Triangular wave modulation mode	Sawtooth wave modulation mode
Transfer timing from registers IDB0 and IDB1 to three-phase output shift register	Transferred once by generating a transfer trigger after setting registers IDB0 and IDB1	Transferred every time a transfer trigger is generated
Trigger timing of the dead time timer when the INV16 bit is 0	Falling edge of a one-shot pulse of the timers A1, A2, or A4	• Falling edge of a one-shot pulse of the timer A1, A2, or A4 • Transfer trigger
INV13 bit	Enabled when the INV11 bit is 1 and the INV06 bit is 0	Disabled

One of the following conditions must be met to trigger a transfer:

- Timer B2 underflows.
- A value is written to the INV07 bit.
- A value is written to the TB2 register during timer B2 stop when the INV10 bit is 1.

INV16, INV13, INV11: Bits in the INVC1 register

17.2.4 Three-Phase PWM Control Register 1 (INVC1)

Three-Phase PWM Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	Reset Value
0								INVC1	0309h	00h

Bit Symbol	Bit Name	Function	RW
INV10	Timer A1, A2 and A4 start trigger select bit	0 : Timer B2 underflow 1 : Timer B2 underflow and write to the TB2 register when timer B2 stops	RW
INV11	Timer A1-1, A2-1 and A4-1 control bit	0 : Three-phase mode 0 1 : Three-phase mode 1	RW
INV12	Dead time timer count source select bit	0 : f1TIMAB or f2TIMAB 1 : f1TIMAB divided by 2 or f2TIMAB divided by 2	RW
INV13	Carrier wave rise/fall detect flag	0 : Timer A1 reload control signal is 0 1 : Timer A1 reload control signal is 1	RO
INV14	Active level control bit	0 : Active low 1 : Active high	RW
INV15	Dead time disable bit	0 : Dead time enabled 1 : Dead time disabled	RW
INV16	Dead time timer trigger select bit	0 : Falling edge of one-shot pulse of timer (A4, A1, and A2) 1 : Rising edge of the three-phase output shift register (U-, V-, W-phase) output	RW
— (b7)	Reserved bit	Set to 0	RW

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting this register.
Rewrite the INVC1 register while timers A1, A2, A4, and B2 are stopped.

INV11 (Timer A1, A2, and A4 start trigger select bit) (b1)

The following table lists items influenced by the INV11 bit.

Table 17.5 INV11 Bit

Item	INV11 = 0	INV11 = 1
Mode	Three-phase mode 0	Three-phase mode 1
Registers TA11, TA21 and TA41	Not used	Used
Bits INV00 to INV01 in the INVC0 register	Disabled The ICTB2 counter decrements whenever timer B2 underflows.	Enabled
INV13 bit	Disabled	Enabled when INV11 is 1 and INV06 is 0

When the INV06 bit is 1 (sawtooth wave modulation mode), set the INV11 bit to 0 (three-phase mode 0). Also, when the INV11 bit is 0, set the PWCON bit in the TB2SC register to 0 (timer B2 is reloaded when timer B2 underflows).

INV13 (Carrier wave rise/fall detect flag) (b3)

The INV13 bit is enabled only when the INV06 bit is set to 0 (triangular wave modulation mode) and the INV11 bit to 1 (three-phase mode 1).

INV16 (Dead time timer trigger select bit) (b6)

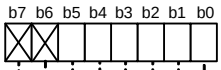
If both of the following conditions are met, set the INV16 bit to 1 (rising edge of the three-phase output shift register output).

- The INV15 bit is 0 (dead time timer enabled)
- Bits Dij and DiBj always have different values when the INV03 bit is set to 1 (three-phase control timer output enabled). The high- and low-side signals always output opposite level signals at any time except dead time. (i = U, V, or W; j = 0, 1).

If either of the above conditions is not met, set the INV16 bit to 0 (dead time timer is triggered on the falling edge of a one-shot pulse of timers).

17.2.5 Three-Phase Output Buffer Register i (IDBi) (i = 0, 1)

Three-Phase Output Buffer Register i (i = 0, 1)



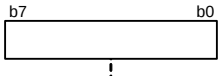
Symbol	Address	Reset Value
IDB0	030Ah	XX11 1111b
IDB1	030Bh	XX11 1111b

Bit Symbol	Bit Name	Function	RW
DUi	U-phase output buffer i	Set the output logical value of the three-phase output shift registers. The set value is reflected in each turn-on signal as follows: 0 : Active (on) 1 : Inactive (off) When read, the values of the three-phase output shift registers are read.	RW
DUBi	$\overline{U}$-phase output buffer i		RW
DVi	V-phase output buffer i		RW
DVBi	$\overline{V}$-phase output buffer i		RW
DWi	W-phase output buffer i		RW
DWBi	$\overline{W}$-phase output buffer i		RW
— (b7-b6)	No register bits. If necessary, set to 0. The read value is undefined.		—

Values of registers IDB0 and IDB1 are transferred to the three-phase output shift registers in response to a transfer trigger. After the transfer trigger occurs, the IDB0 register value determines each phase output signal (internal signal) first. Then, the IDB1 register value on the falling edge of timers A1, A2, and A4 one-shot pulse determines each phase output signal (internal signal).

17.2.6 Dead Time Timer (DTT)

Dead Time Timer



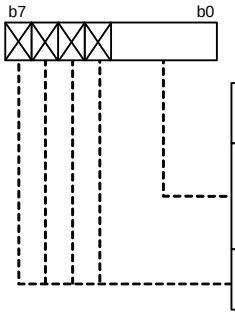
Symbol	Address	Reset Value
DTT	030Ch	Undefined

Function	Setting Range	RW
If a setting value is n, the count source is counted n times after the start trigger occurs, and then the timer stops.	1 to 255	WO

Use the MOV instruction to set the DTT register.
The DTT register acts as a one-shot timer which delays the timing for a turn-on signal to be switched to its active level in order to prevent the upper and lower transistors from being turned on simultaneously.
The DTT register is enabled when the INV15 bit in the INVC1 register is set to 0 (dead time enabled). No dead time can be set when the INV15 bit is set to 1 (dead time disabled).
Select a trigger by the INV16 bit in the INVC1 register, and a count source by the INV12 bit in the INVC1 register.

17.2.7 Timer B2 Interrupt Generation Frequency Set Counter (ICTB2)

Timer B2 Interrupt Generation Frequency Set Counter



Symbol	Address	Reset Value
ICTB2	030Dh	Undefined

Function	Setting Range	RW
When a setting value is n, timer B2 interrupt is generated every nth count timer B2 underflow meets the condition selected by bits INV01 to INV00 in the INVC0 register.	1 to 15	WO
No register bits. If necessary, set to 0		—

Use the MOV instruction to set the ICTB2 register.

If the INV01 bit in the INVC0 register is 1, set the ICTB2 register when the TB2S bit in the TABSR register is set to 0 (timer B2 counter stopped). If the INV01 bit is 0 and the TB2S bit to 1 (timer B2 counter start), do not set the ICTB2 register when timer B2 underflows.

When bits INV01 to INV00 are 11b, the first interrupt is generated when timer B2 underflows n-1 times if a setting value in the ICTB2 counter is n. Subsequent interrupts are generated every n times timer B2 underflows.

17.2.8 Timer B2 Special Mode Register (TB2SC)

Timer B2 Special Mode Register

b7	b6	b5	b4	b3	b2	b1	b0
X	0	0	0	0	0		

Symbol	Address	Reset Value
TB2SC	033Eh	X000 0000b

Bit Symbol	Bit Name	Function	RW
PWCON	Timer B2 reload timing switch bit	0 : Timer B2 underflow 1 : Timer A output at odd-numbered occurrences	RW
IVPCR1	Three-phase output port $\overline{SD}$ control bit 1	0 : Three-phase output forced cutoff by $\overline{SD}$ input (high-impedance) disabled 1 : Three-phase output forced cutoff by $\overline{SD}$ input (high-impedance) enabled	RW
— (b6-b2)	Reserved bits	Set to 0	RW
— (b7)	No register bit. If necessary, set to 0. The read value is undefined.		—

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting this register.

PWCON (Timer B2 reload timing switch bit) (b0)

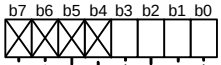
If the INV11 bit in the INVC1 register is 0 (three-phase mode 0) or the INV06 bit in the INVC0 register is 1 (sawtooth wave modulation mode), set the PWCON bit to 0 (timer B2 underflow).

IVPCR1 (Three-phase output port $\overline{SD}$ control bit 1) (b1)

Related pins are U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$.
If a low-level signal is applied to the $\overline{SD}$ pin when the IVPCR1 bit is 1, three-phase motor control timer output is disabled (INV03 bit in the INVC0 register becomes 0). Then, the target pins become high-impedance regardless of the functions those pins are using.
After a forced cutoff, input a high-level signal to the $\overline{SD}$ pin and set the IVPCR1 bit to 0 to cancel the forced cutoff.

17.2.9 Position-Data-Retain Function Control Register (PDRF)

Position-Data-Retain Function Control Register



Symbol	Address	Reset Value
PDRF	030Eh	XXXX 0000b

Bit Symbol	Bit Name	Function	RW
PDRW	W-phase position data retain bit	Input level at IDW pin is retained. 0: Low level 1: High level	RO
PDRV	V-phase position data retain bit	Input level at IDV pin is retained. 0: Low level 1: High level	RO
PDRU	U-phase position data retain bit	Input level at IDU pin is retained. 0: Low level 1: High level	RO
PDRT	Retain-trigger polarity select bit	Select polarity of a retain-trigger When the INV14 bit is 0 (active low): 0: Falling edge of high-side output signal 1: Rising edge of high-side output signal When the INV14 bit is 1 (active high): 0: Rising edge of high-side output signal 1. Falling edge of high-side output signal	RW
— (b7-b4)	No register bits. If necessary, set to 0. The read value is undefined.		—

This register is only enabled in three-phase mode.

17.2.10 Port Function Control Register (PFCR)

Port Function Control Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	Reset Value
PFCR	0318h	0011 1111b

Bit Symbol	Bit Name	Function	RW
PFC0	Port P8_0 output function select bit	0: I/O port P8_0 1: Three-phase PWM output (U-phase output)	RW
PFC1	Port P8_1 output function select bit	0: I/O port P8_1 1: Three-phase PWM output ($\overline{U}$-phase output)	RW
PFC2	Port P7_2 output function select bit	0: I/O port P7_2 1: Three-phase PWM output (V-phase output)	RW
PFC3	Port P7_3 output function select bit	0: I/O port P7_3 1: Three-phase PWM output ($\overline{V}$-phase output)	RW
PFC4	Port P7_4 output function select bit	0: I/O port P7_4 1: Three-phase PWM output (W-phase output)	RW
PFC5	Port P7_5 output function select bit	0: I/O port P7_5 1: Three-phase PWM output ($\overline{W}$-phase output)	RW
— (b7-b6)	No register bits. If necessary, set to 0. The read value is 0.		—

This register is enabled only when the INV03 bit in the INVC0 register is set to 1 (three-phase motor control timer output enabled). Set the TPRC0 bit in the TPRC register to 1 (write enabled) before rewriting this register.

17.2.11 Three-Phase Protect Control Register (TPRC)

Three-Phase Protect Control Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	Reset Value
TPRC	01DAh	00h

Bit Symbol	Bit Name	Function	RW
TPRC0	Three-phase protect control bit	Enable write to the PFCR register 0: Write disabled 1: Write enabled	RW
— (b7-b1)	No register bits. If necessary, set to 0. The read value is 0.		—

Once the TPRC0 bit is set to 1 (write enabled) by a program, the set value 1 is retained. To change the register protected by this bit, follow these steps:

(1) Set the TPRC0 bit to 1.
(2) Set a value to the PFCR register.
(3) Set the TPRC0 bit to 0 (write disabled).

17.3 Operations

17.3.1 Common Operations in Multiple Modes

17.3.1.1 Carrier Wave Cycle Control

Timer B2 controls the cycle of the carrier wave. In triangular wave modulation mode, the cycle of the carrier wave is double the cycle of timer B2 underflow. In sawtooth wave modulation mode, the cycle of the carrier wave is equal to the cycle of timer B2 underflow. Figure 17.3 shows the Relationship between the Carrier Wave Cycle and Timer B2.

Timer B2 underflow is a start trigger for timers A1, A2, and A4, which control the three-phase PWM waveform. However, when the INV10 bit in the INVC1 register is 1, writing to the TB2 register while timer B2 is stopped also generates a trigger for timers A1, A2, and A4.

The frequency of timer B2 interrupt requests can be selected for three-phase motor control timers.

In triangular wave modulation three-phase mode 0 and sawtooth wave modulation mode, when the setting value in the ICTB2 register is n, a timer B2 interrupt request is generated every nth count of timer B2 underflow.

In triangular wave modulation three-phase mode 1, when the setting value in the ICTB2 register is n, a timer B2 interrupt request is generated every nth time of the timing selected by bits INV01 to INV00 in the INVC0 register. However, when bits INV01 to INV00 are 11b, the first interrupt is generated at the n-1 time of timer B2 underflow.

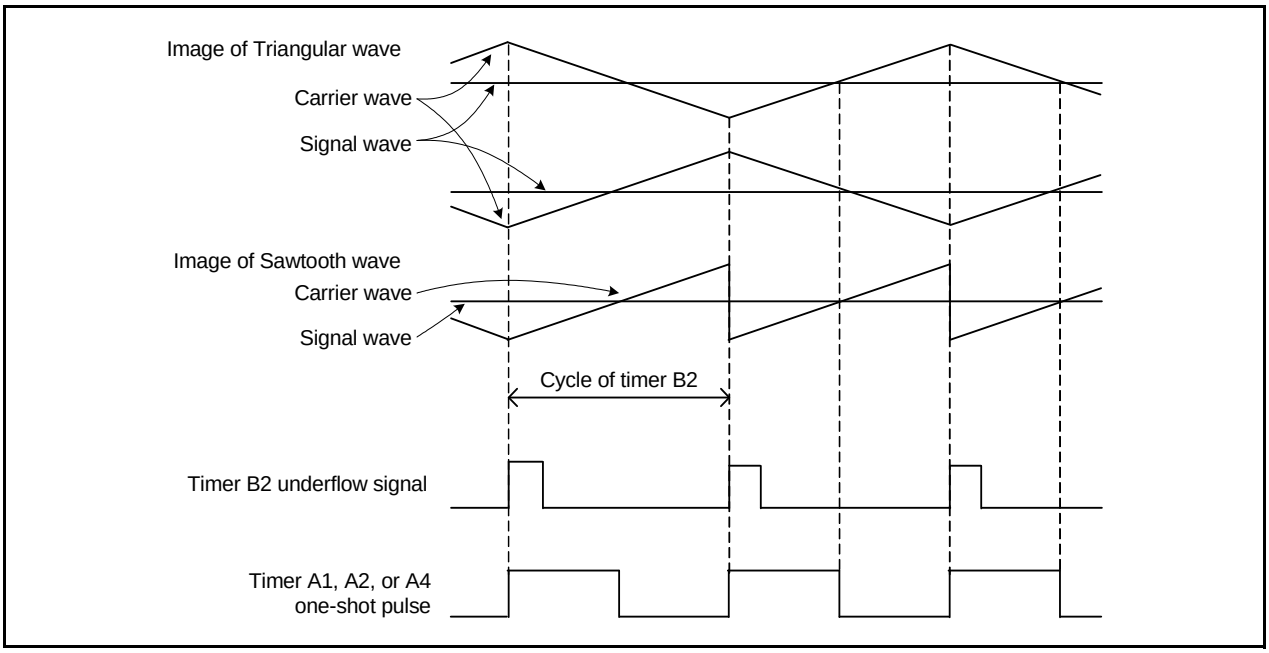


Figure 17.3 Relationship between the Carrier Wave Cycle and Timer B2

17.3.1.2 Three-Phase PWM Wave Control

Timer A4 controls U- and $\overline{U}$-phase waveforms, timer A1 controls V- and $\overline{V}$-phase waveforms, and timer A2 controls W- and $\overline{W}$-phase waveforms. Timer Ai (i = 1, 2, 4) starts counting by a trigger selected by the INV10 bit in the INVC1 register, and generates a one-shot pulse (internal signal). The output signal of each phase changes at the falling edge of the one-shot pulse.

Triangular wave modulation three-phase mode 1 counts values in the TAi1 register and TAi register alternately, and generates a one-shot pulse.

17.3.1.3 Dead Time Control

Due to delays in the transistors turning off, the upper and lower transistors are turned on simultaneously. To prevent this, there are three 8-bit dead time timers, one in each phase. The reload resistor is shared. When the INV15 bit in the INVC1 register is 0 (dead time enabled), the dead time set in the DTT register is enabled. When the INV15 bit is 1 (dead time disabled), no dead time is set.

Select a count source for the dead time timer by setting the INV12 bit in the INVC1 register.

A trigger for the dead time timer can be selected by setting the INV16 bit in the INVC1 register.

When both of the following conditions are met, set the INV16 bit to 1 (the rising edge of the three-phase output shift register is a trigger for the dead time timer):

- The INV15 bit is 0 (dead time enabled).
- Bits Dij and DiBj in the IDBj register have different values when the INV03 bit in the INVC0 register is 1 (three-phase motor control timer output enabled) (i = U, V or W; j = 0, 1). (During the period other than dead time, the high- and low-side output signals always output opposite level signals.)

If either of the conditions above is not met, set the INV16 bit to 0 (a trigger for the dead time timer is the falling edge of one-shot pulse of the timer).

In sawtooth wave modulation mode, the generation of a transfer trigger causes a trigger for the dead time timer.

17.3.1.4 Output Level of Three-Phase PWM Output Pins

Set values to registers IDB0 and IDB1 to select the state of each high- or low-side output signal (either active (on) or not active (off)). The values of registers IDB0 and IDB1 are transferred to the three-phase output shift registers by a transfer trigger. After a transfer trigger is generated, the value set in the IDB0 register becomes the first output signal of each phase (internal signal), and then at the falling edge of a timer A1, A2, or A4 (internal signal) one-shot pulse, the value set in the IDB1 register becomes the output signal of each phase.

A transfer trigger is generated under any of the following conditions:

- At the first timer B2 underflow after registers IDB0 and IDB1 are written (in triangular wave modulation mode)
- Each time timer B2 underflows (in sawtooth wave modulation mode)
- Writing to the TB2 register while timer B2 is stopped (when the INV10 bit in the INVC1 register is 1)
- Setting the INV07 bit in the INVC0 register to 1 (software trigger)

The active level can be selected by the INV14 bit in the INVC1 register.

Table 17.6 Output Level of Three-Phase PWM Output Pins

Value Set in Registers IDB0 and IDB1	Output Signal of Each Phase (Internal Signal)	Value Set to the INV14 Bit in the INVC1 Register	
		0 (active, low level)	1 (active, high level)
0 (active (on))	0	Low	High
1 (not active (off))	1	High	Low

17.3.1.5 Simultaneous Conduction Prevention

This function prevents the upper and lower output signals from being active simultaneously due to program errors or unexpected program operation. When the high- and low-side output signals become active at the same time while the simultaneous conduction is disabled by the INV04 bit in the INVC0 register, the following occur:

- The INV03 bit in the INVC0 register becomes 0 (three-phase motor control timer output disabled).
- The INV05 bit in the INVC0 register becomes 1 (simultaneous conduction detected).
- Pins U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$ become high-impedance.

17.3.1.6 Three-Phase PWM Waveform Output Pins

Pins U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$ output a PWM waveform under the following conditions:

- The INVC02 bit in the INVC0 register is 1 (three-phase motor control timer function).
- The INVC03 bit in the INVC0 register is 1 (three-phase motor control timer output enabled).
- Bits PFC5 to PFC0 in the PFCR register are 1 (three-phase PWM output (selected independently for each pin)).

The three-phase output forced cutoff by the $\overline{SD}$ pin is available.

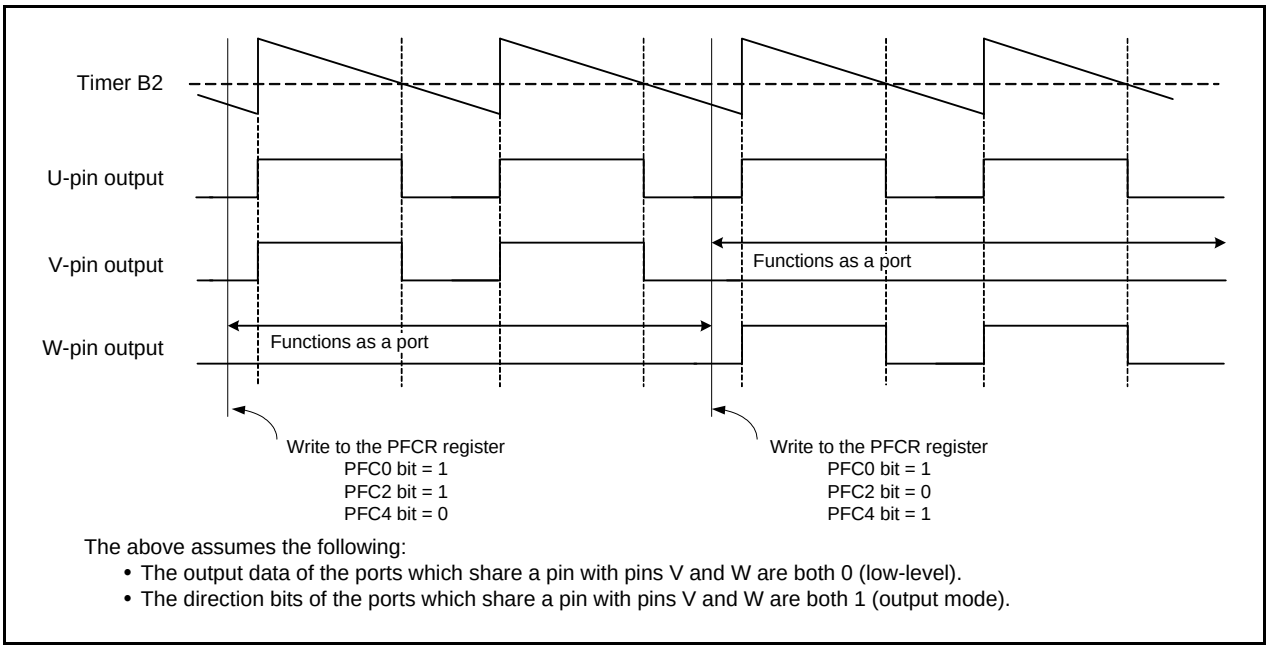
17.3.1.7 Three-Phase PWM Output Pin Select

Pins U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$ output a three-phase PWM waveform when the PFCi bit (i = 0 to 5) in the PFCR register is 1 (three-phase PWM output). When the PFCi bit is 0 (I/O port), these pins are used as I/O ports (or other peripheral function I/O ports). Therefore, while some of the six pins output a three-phase PWM waveform, the other pins can be used as I/O ports (or other peripheral function I/O ports).

The PFCR register can be rewritten when the TPRC0 bit in the TPRC register is 1 (write to the PFCR register enabled). The functions of the three-phase PWM waveform output pins can be protected from being rewritten due to an unexpected program operation. To prevent rewrite, follow these steps:

(1) Set the TPRC0 bit to 1.
(2) Rewrite the PFCR register.
(3) Set the TPRC0 bit to 0 (write to the PFCR register disabled).

Figure 17.4 shows Three-Phase Output and I/O Port Switch Function Operation.



The above assumes the following:

- The output data of the ports which share a pin with pins V and W are both 0 (low-level).
- The direction bits of the ports which share a pin with pins V and W are both 1 (output mode).

Figure 17.4 Three-Phase Output and I/O Port Switch Function Operation

17.3.1.8 Three-Phase Output Forced Cutoff Function

While the INV02 bit in the INVC0 register is 1 (three-phase motor control timer function) and the INV03 bit is 1 (three-phase motor control timer output enabled), when a low-level signal is applied to the $\overline{SD}$ pin, the INV03 bit in the INVC0 register becomes 0 (three-phase motor control timer output disabled), and pins corresponding to U, $\overline{U}$, V, $\overline{V}$, W and $\overline{W}$ outputs change concurrently as follows:

- When the IVPCR1 bit in the TB2SC register is 1 (three-phase output forced cutoff enabled)
  High-impedance
- When the IVPCR1 bit in the TB2SC register is 0 (three-phase output forced cutoff disabled)
  I/O ports or other peripheral function I/O ports

However, applying a low-level signal to the $\overline{SD}$ pin while the IVPCR1 bit is 1 places the pins in a high-impedance state even when the pins are used as functions other than U, $\overline{U}$, V, $\overline{V}$, W and $\overline{W}$ outputs. Table 17.7 lists State of Pins U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$.

Table 17.7 State of Pins U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$ (1)

State of Bit and Pin		Function or State of Pins U, $\overline{U}$, V, $\overline{V}$, W and $\overline{W}$
IVPCR1 bit in the TB2SC register	$\overline{SD}$ pin input	
1	High	Three-phase PWM output
	Low	High-impedance
0	High	Three-phase PWM output
	Low	I/O port or other peripheral functions

Note:
1. The above assumes bits INVC02, INVC03, and PFCi are all 1.

The digital debounce filter is available for the $\overline{SD}$ pin. When the $\overline{SD}$ pin level remains at a level longer than the width of the digital debounce filter, the level is transferred to the internal circuit. The NDDR register can be set the digital debounce filter width. Refer to 13.4.3 “$\overline{NMI}$/$\overline{SD}$ Digital Filter” for details.

To return the pin function to three-phase PWM output after a forced cutoff, follow these steps:
(1) Apply a high-level signal to the $\overline{SD}$ pin.
(2) Wait for more than width of the digital debounce filter (digital debounce filter enabled).
(3) Set the INV03 bit in the INVC0 register to 1 (three-phase motor control timer output enabled).
(4) Confirm that the INV03 bit is 1. If the bit is 0, return to step (3).
(5) Set the IVPCR1 bit to 0 (three-phase output forced cutoff disabled).
(6) Set the IVPCR1 bit to 1 (when enabling three-phase output forced cutoff again).

When not using the three-phase output forced cutoff function, set a port direction bit which shares the pin with $\overline{SD}$ input to 0 (input port), and apply a high-level signal to the $\overline{SD}$ pin.
The same pin is used for both $\overline{SD}$ input and $\overline{NMI}$ input. To disable the $\overline{NMI}$ interrupt, set the PM24 bit in the PM2 register to 0 ($\overline{NMI}$ interrupt disabled).

17.3.1.9 Position-Data-Retain Function

The position-data-retain function employs three position-data input pins: U-, V-, and W-phase. Input levels of IDU, IDV, and IDW inputs are retained. The falling edge or rising edge of the high-side output signal of each phase can be selected by setting the PDRT bit in the PDRF register as a position-data-retain trigger.

For example, in the case of U-phase, when the U-phase trigger is generated, the state of the IDU pin is transferred to the PDRU bit in the PDRF register. The value is retained until the next trigger of the U-phase waveform output.

Figure 17.5 shows Position-Data-Retain Function (U-Phase) Operation.

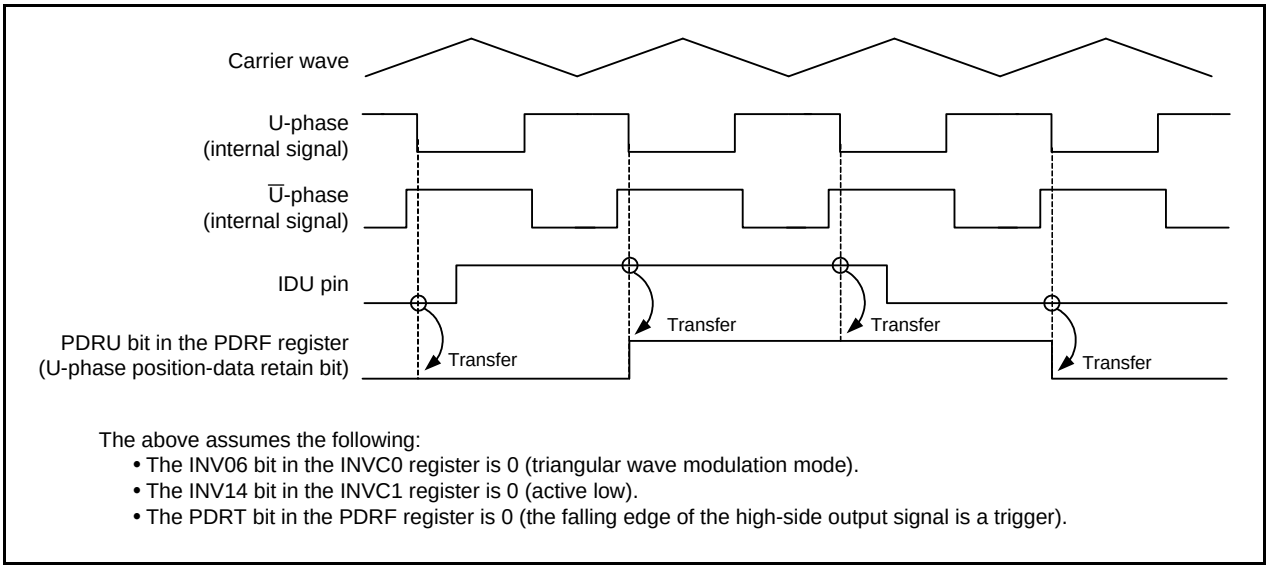


Figure 17.5 Position-Data-Retain Function (U-Phase) Operation

17.3.2 Triangular Wave Modulation Three-Phase Mode 0

Triangular wave modulation uses the timer B2 cycle as a reference cycle. Table 17.8 lists Three-Phase Mode 0 Specifications, and Figure 17.6 shows Example of Three-Phase Mode 0 Operation.

Table 17.8 Three-Phase Mode 0 Specifications

Item		Specification
Carrier wave cycle		$\frac{(m+1)\times 2}{fi}$ m: Setting value of the TB2 register, 0000h to FFFFh fi: Count source frequency (f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32)
Three-phase PWM output width		$\frac{n\times 2}{fi}$ n: Setting value of the TAi register, 0001h to FFFFh fi: Count source frequency (f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32)
Differences from three-phase mode 1	Reference cycle	Timer B2 cycle (one-half cycle of the carrier wave)
	Timer B2 reload timing	Timer B2 underflow
	Three-phase PWM waveform control	Counts the value of the TAi register every time a timer Ai start trigger is generated (the TAi1 register is not used).
	Timer B2 interrupt	When the setting value in the ICTB2 register is n, a timer B2 interrupt request is generated every nth time of timer B2 underflow (not influenced by bits INV00 and INV01 in the INVC0 register).
	Detection of a carrier wave cycle (first half or last half)	Not detected (the INV13 bit in the INVC1 register is disabled).

i = 1, 2, 4

Table 17.9 Registers and Settings in Three-Phase Mode 0 (1/2) (1)

Register	Bit	Function and Setting
INVC0	INV00	Disabled (Despite the setting, the ICTB2 register counts timer B2 underflow.)
	INV01	
	INV02	Set to 1 (three-phase motor control timer function used).
	INV03	Set to 1 (three-phase motor control timer output enabled).
	INV04	Select simultaneous conduction enabled or disabled.
	INV05	Simultaneous conduction detect flag
	INV06	Set to 0 (triangular wave modulation mode).
	INV07	Software trigger bit
INVC1	INV10	Select a start trigger for timers A1, A2, and A4.
	INV11	Set to 0 (three-phase mode 0).
	INV12	Select a count source for the dead time timer.
	INV13	Disabled
	INV14	Select the active level (either active high or active high).
	INV15	Select dead time enabled or disabled.
	INV16	Select a trigger for the dead time timer.
	7	Set to 0.
IDB0, IDB1	5 to 0	Set the output logic of the three-phase output shift registers.
DTT	7 to 0	Set the dead time.
ICTB2	3 to 0	Set the frequency of the timer B2 interrupt request.
TB2SC	PWCON	Set to 0 (timer B2 underflow).
	IVPCR1	Select three-phase output forced cutoff enabled or disabled.
	b7 to b2	Set to 0.
PDRF	PDRU, PDRV, PDRW	Position-data-retain bit
	PDRT	Select a position-data-retain trigger.
PFCR	PFC5 to PFC0	Select I/O port or three-phase PWM output.
TPRC	TPRC0	Set to 1 when writing to the PFCR register, or to 0 when not writing to it.
TA1, TA2, TA4	15 to 0	Set the one-shot pulse width.
TA11, TA21, TA41	15 to 0	Not used.
TB2	15 to 0	Set one-half cycle of the carrier wave.
TRGSR	TA1TGH to TA1TGL	Set to 01b (when using V-phase output control circuit).
	TA2TGH to TA2TGL	Set to 01b (when using W-phase output control circuit).
	TA3TGH to TA3TGL	Not used for three-phase motor control timer.
	TA4TGH to TA4TGL	Set to 01b (when using U-phase output control circuit).

Note:
1. This table does not describe a procedure.

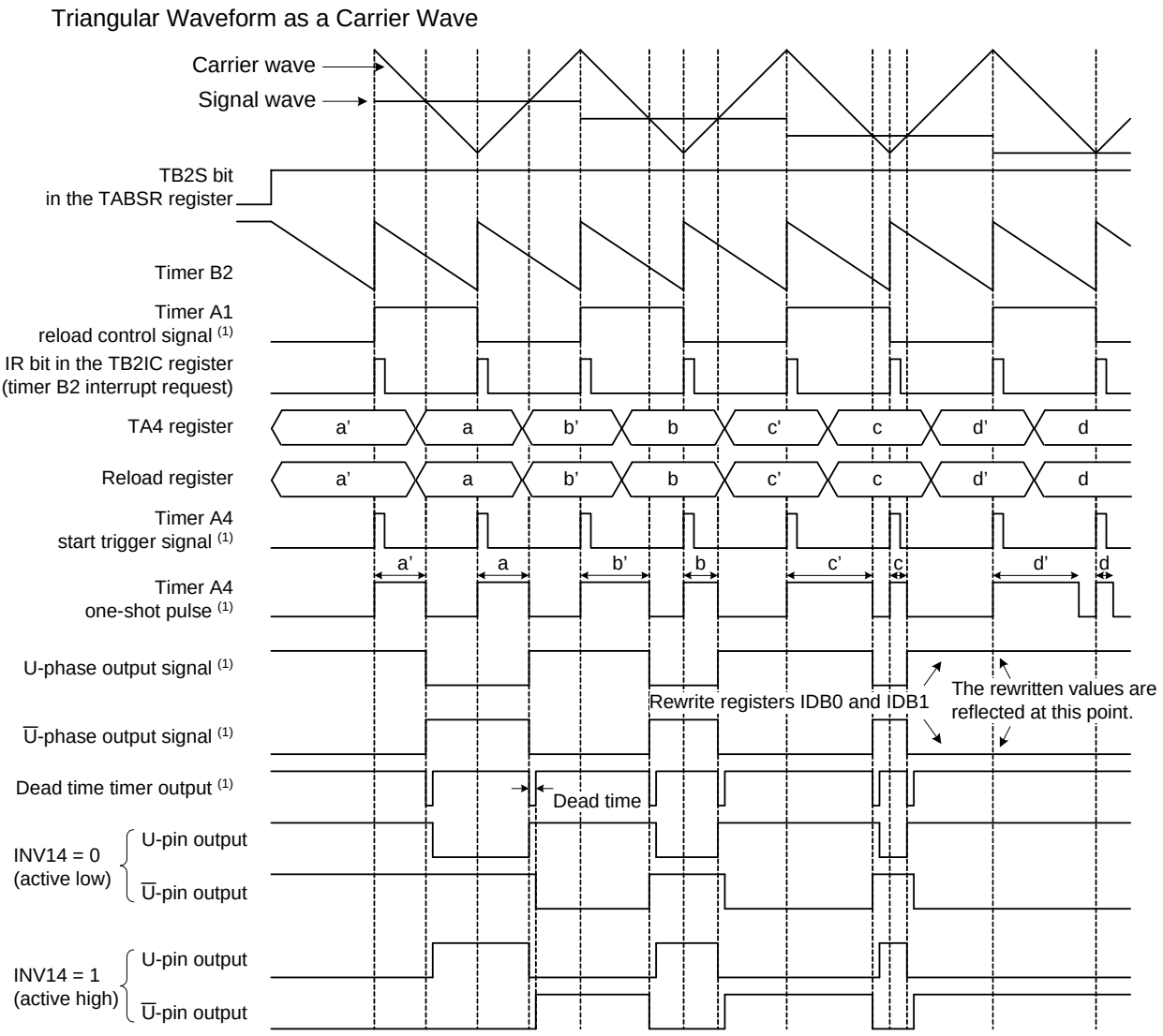
Table 17.10 Registers and Settings in Three-Phase Mode 0 (2/2) (1)

Register	Bit	Function and Setting
TABSR	TA0S	Not used for three-phase motor control timer.
	TA1S	Set to 1 when starting counting, and to 0 when stopping counting.
	TA2S	Set to 1 when starting counting, and to 0 when stopping counting.
	TA3S	Not used for three-phase motor control timer.
	TA4S	Set to 1 when starting counting, and to 0 when stopping counting.
	TB0S	Not used for three-phase motor control timer.
	TB1S	Not used for three-phase motor control timer.
	TB2S	Set to 1 when starting counting, and to 0 when stopping counting.
TA1MR, TA2MR, TA4MR	TMOD1 to TMOD0	Set to 10b (one-shot timer mode).
	MR0	Set to 0.
	MR1	Set to 0.
	MR2	Set to 1 (select a trigger by setting bits TAiTGH and TAiTGL).
	MR3	Set to 0.
	TCK1 to TCK0	Select a count source.
TB2MR	TMOD1 to TMOD0	Set to 00b (timer mode).
	MR1 to MR0	Set to 00b.
	4	Set to 0.
	MR3	Set to 0.
	TCK1 to TCK0	Select a count source.
PCLKR	PCLK0	Select a count source.
TCKDIVC0	TCDIV00	Select the clock prior to timer AB division.
TACS0 to TACS2	7 to 0	Select a count source.
TBCS1	TCS3 to TCS0	Select a count source.
TAPOFS	POFSi	Set to 0.
UDF	TAiP	Set to 0.

i = 1, 2, 4

Note:

1. This table does not describe a procedure.



The above assumes the following:
In the INVC1 register
- The INV16 bit is 1 (the dead time timer is triggered on the rising edge of the three-phase output shift register).
- The INV15 bit is 0 (dead time timer enabled).
- The INV10 bit is 0 (timer B2 underflow is a start trigger for timers A1, A2, and A4).

The ICTB2 register is 1h (timer B2 interrupt request is generated at every timer B2 underflow).
Bits PFC1 to PFC0 in the PFCR register are 11b (U-, U-phase outputs).
In the TA4 register
- Initial value : a'
- Changes at every timer B2 interrupt
  1st : a; 2nd : b'; 3rd : b; 4th: c'; 5th : c; 6th : d'; 7th : d

Registers IDB0 and IDB1
- Initial values: DU0 = 1; DUB0 = 0; DU1 = 0; DUB1 = 1
- At the sixth timer B2 interrupt, the values are changed to: DU0 = 1; DUB0 = 0; DU1 = 1; DUB1 = 0.

Note:
1. Internal signal. Refer to Figure 17.1.

Figure 17.6 Example of Three-Phase Mode 0 Operation

17.3.2.1 Three-Phase PWM Wave Output Timing Control

In three-phase mode 0, when a start trigger for timers A1, A2, and A4 is generated, the counter starts counting the value of the TAi register (i = 1, 2, 4).

17.3.2.2 Three-Phase PWM Waveform Output Level Control

In triangular wave modulation mode, the output levels set in registers IDB0 and IDB1 are transferred to the three-phase output shift registers by a transfer trigger. After a transfer trigger is generated, first the value set in the IDB0 register becomes the output signal for each phase (internal signal), then at the falling edge of one-shot pulse for timers A1, A2, and A4, followed by the values set in the IDB1 register. Consequently, the three-phase PWM output changes. Afterward, the values in registers IDB0 and IDB1 alternately become output signals for each phase at every falling edge of the one-shot pulse for timers A1, A2, and A4.
When the INV15 bit in the INVC1 register is 0 (dead time enabled), a phase changing from active to nonactive changes simultaneously with output signals for each phase (internal signal), while a phase changing from nonactive to active changes when the dead time timer stops.

A transfer trigger is generated under the following conditions:

- The first timer B2 underflow after registers IDB0 and IDB1 are written.
- Writing to the TB2 register when timer B2 is stopped (when the INV10 bit in the INVC1 register is 1).
- Setting the INV07 bit in the INVC0 register to 1 (software trigger).

17.3.3 Triangular Wave Modulation Three-Phase Mode 1

Triangular wave modulation uses twice the cycles of timer B2 as a reference cycle. Table 17.11 lists Three-Phase Mode 1 Specifications, and Figure 17.7 shows Example of Three-Phase Mode 1 Operation.

Table 17.11 Three-Phase Mode 1 Specifications

Item		Specification
Carrier wave cycle		$\frac{(m+1)\times 2}{fi}$ m: Setting value of the TB2 register, 0000h to FFFFh fi: Count source frequency (f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32)
Three-phase PWM output width		$\frac{n\times 2}{fi}$ n: Setting value of the TAi register, 0001h to FFFFh fi: Count source frequency (f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32)
Differences from three-phase mode 0	Reference cycle	Twice the cycle of timer B2 (cycle of the carrier wave)
	Timer B2 reload timing	Select either of the following: • Timer B2 underflow • Timer A output at an odd number of times
	Three-phase PWM waveform control	Counts the values of registers TAi and TAi1 alternately every time a timer Ai start trigger is generated
	Timer B2 interrupt	Select a count timing for the ICTB2 register by bits INV01 to INV00 in the INVC0 register: • Timer B2 underflow (each time) • Timer B2 underflow when the INV13 bit in the INVC1 register is 0 • Timer B2 underflow when the INV13 bit is 1 When the setting value in the ICTB2 register is n, a timer B2 interrupt request is generated every nth time of the timing selected by setting bits INV01 to INV00.
	Detection of a carrier wave cycle (first half or last half)	Detected (The INV13 bit in the INVC1 register is enabled.)

i = 1, 2, 4

Table 17.12 Registers and Settings in Three-Phase Mode 1 (1/2) (1)

Register	Bit	Functions and Setting
INVC0	INV00	Select the timing that the ICTB2 register starts counting.
	INV01	
	INV02	Set to 1 (three-phase motor control timer function used).
	INV03	Set to 1 (three-phase motor control timer output enabled).
	INV04	Select simultaneous conduction enabled or disabled.
	INV05	Simultaneous conduction detect flag
	INV06	Set to 0 (triangular wave modulation mode).
	INV07	Software trigger bit
INVC1	INV10	Select a start trigger for timers A1, A2, and A4.
	INV11	Set to 1 (three-phase mode 1).
	INV12	Select a count source for the dead time timer.
	INV13	Carrier wave state detect flag
	INV14	Select the active level (either active high or active high).
	INV15	Select dead time enabled or disabled.
	INV16	Select a trigger for the dead time timer.
	7	Set to 0.
IDB0, IDB1	5 to 0	Set an output logic of the three-phase output shift registers.
DTT	7 to 0	Set the dead time.
ICTB2	3 to 0	Set the frequency of the timer B2 interrupt request.
TB2SC	PWCON	Select timer B2 reload timing.
	IVPCR1	Select three-phase output forced cutoff enabled or disabled.
	b7 to b2	Set to 0.
PDRF	PDRU, PDRV, PDRW	Position-data-retain bit
	PDRT	Select a position-data-retain trigger.
PFCR	PFC5 to PFC0	Select I/O port or three-phase PWM output.
TPRC	TPRC0	Set to 1 when writing to the PFCR register, or to 0 when not writing to it.
TA1, TA2, TA4	15 to 0	Set the one-shot pulse width.
TA11, TA21, TA41	15 to 0	Set the one-shot pulse width.
TB2	15 to 0	Set one-half cycle of the carrier wave.

i = 1, 2, 4

Note:

1. This table does not describe a procedure.

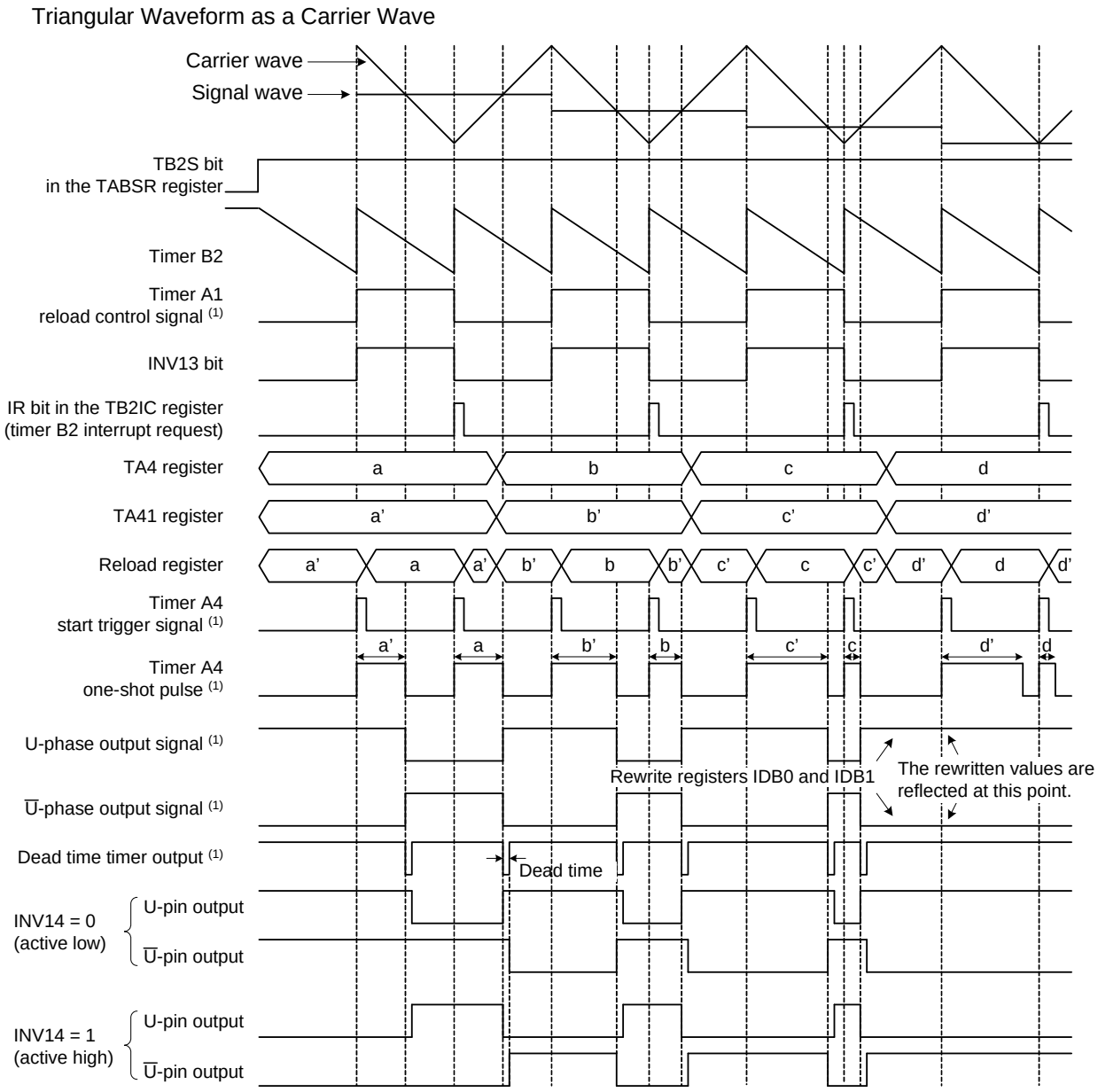
Table 17.13 Registers and Settings in Three-Phase Mode 1 (2/2) (1)

Register	Bit	Function and Setting
TRGSR	TA1TGH to TA1TGL	Se to 01b (when using V-phase output control circuit).
	TA2TGH to TA2TGL	Set to 01b (when using W-phase output control circuit).
	TA3TGH to TA3TGL	(Not used for three-phase motor control timer.)
	TA4TGH to TA4TGL	Set to 01b (when using U-phase output control circuit).
TABSR	TA0S	Not used for three-phase motor control timer.
	TA1S	Set to 1 when starting counting, and to 0 when stopping counting.
	TA2S	Set to 1 when starting counting, and to 0 when stopping counting.
	TA3S	Not used for three-phase motor control timer.
	TA4S	Set to 1 when starting counting, and to 0 when stopping counting.
	TB0S	Not used for three-phase motor control timer.
	TB1S	Not used for three-phase motor control timer.
	TB2S	Set to 1 when starting counting, and to 0 when stopping counting.
TA1MR, TA2MR, TA4MR	TMOD1 to TMOD0	Set to 10b (one-shot timer mode).
	MR0	Set to 0.
	MR1	Set to 0.
	MR2	Set to 1 (select a trigger by setting bits TAiTGH and TAiTGL.).
	MR3	Set to 0.
	TCK1 to TCK0	Select a count source.
TB2MR	TMOD1 to TMOD0	Set to 00b (timer mode).
	MR1 to MR0	Set to 00b.
	4	Set to 0.
	MR3	Set to 0.
	TCK1 to TCK0	Select a count source.
PCLKR	PCLK0	Select a count source.
TCKDIVC0	TCDIV00	Select the clock prior to timer AB division.
TACS0 to TACS2	7 to 0	Select a count source.
TBCS1	TCS3 to TCS0	Select a count source.
TAPOFS	POFSi	Set to 0.
UDF	TAiP	Set to 0.

i = 1, 2, 4

Note:

1. This table does not describe a procedure.



The above assumes the following:
In the INVC0 register
- The INV01 bit is 0 and the ICTB2 register is 2h (timer B2 interrupt at every second timer B2 underflow) or bits INV01 to INV00 are 11b and the ICTB2 register is 1h (timer B2 interrupt at timer B2 underflow while the timer A1 reload control signal is 1).

In the INVC1 register
- The INV16 bit is 1 (the dead time timer is triggered on the rising edge of the three-phase output shift register).
- The INV15 bit is 0 (dead time timer enabled).
- The INV10 bit is 0 (timer B2 underflow is a start trigger for timers A1, A2 and A4).

The PWCON bit in the TB2SC register is 0 (timer B2 reload at the timing of timer B2 underflow).
Bits PFC1 to PFC0 in the PFCR register are 11b (U-, $\overline{U}$-phase outputs).
In registers TA4 and TA41
- Initial value: TA41 = a', TA4 = a
- Registers TA4 and TA41 change at every timer B2 interrupt
  1st : TA41 = b'; TA4 = b; 2nd : TA41 = c'; TA4 = c; 3rd: TA41 = d'; TA4 = d

In registers IDB0 and IDB1
- Initial values: DU0 = 1; DUB0 = 0; DU1 = 0; DUB1 = 1
- At the third timer B2 interrupt, the values are changed to: DU0 = 1; DUB0 = 0; DU1 = 1; DUB1 = 0 .

Note:
1. Internal signal. Refer to Figure 17.1.

Figure 17.7 Example of Three-Phase Mode 1 Operation

17.3.3.1 INV13 Bit in the INVC1 Register

In three-phase mode 1, the INV13 bit can be used to detect whether the cycle of the carrier wave is the first half or the last half. The INV13 bit is a flag which checks the state of timer A1 reload control signals. The timer A1 reload control signal becomes 0 while timer A1 is stopped, and the value is inverted at every start trigger signal for timers A1, A2, and A4. Thus, if the cycle of the carrier wave starts at the first timer B2 underflow, the first half comes when the INV13 bit is 1, and the last half comes when it is 0. Table 17.14 lists Relations of the INV13 Bit with Other Factors.

Table 17.14 Relations of the INV13 Bit with Other Factors

INV13 bit / Timer A1 reload control signal	1	0
One-shot pulse count value	TAi1 register value	TAi register value
Timer B2 underflow	At an odd number of times	At an even number of times
Carrier wave	First half	Last half

i = 1, 2, 4

17.3.3.2 Three-Phase PWM Waveform Output Timing Control

In three-phase mode 1, when a start trigger for timers A1, A2, and A4 is generated, the value set in the TAi1 register is counted first. Afterward, the values in registers TAi1 and TAi are alternately counted every time a start trigger for timers A1, A2, and A4 is generated.

When the values in registers TAi1 and TAi are rewritten during processing, the updated value is output from the next carrier wave cycle. Figure 17.8 shows Update Timing of Registers TAi and TAi1 in Three-Phase Mode 1.

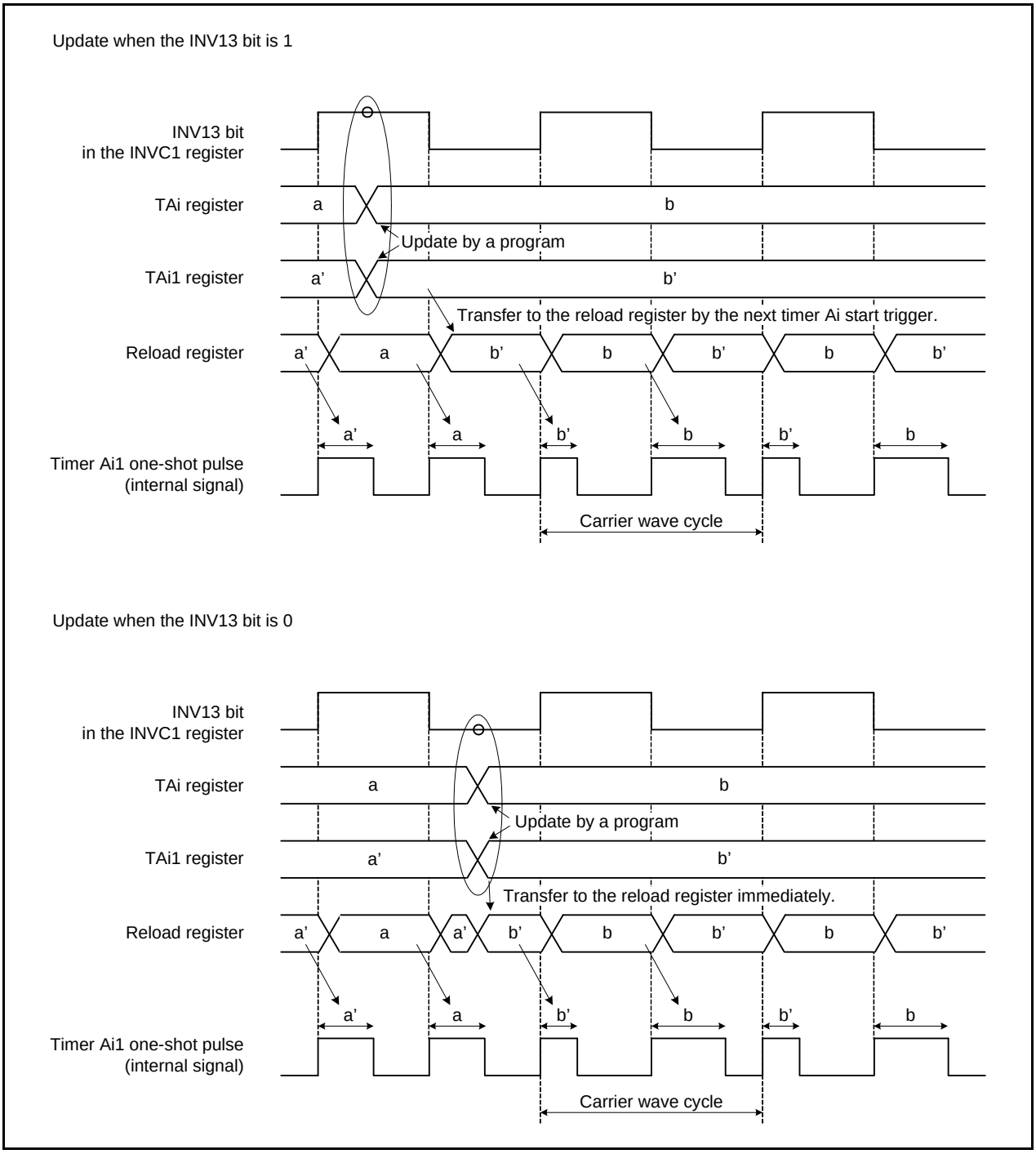


Figure 17.8 Update Timing of Registers TAi and TAi1 in Three-Phase Mode 1

17.3.3.3 Carrier Wave Control

In three-phase mode 1, the reload timing of the TB2 register can be selected by setting the PWCON bit in the TB2SC register.

17.3.3.4 Three-Phase PWM Waveform Output Level Control

In triangular wave modulation mode, the output levels set in registers IDB0 and IDB1 are transferred to the three-phase output shift registers by a transfer trigger. After a transfer trigger is generated, first the value set in the IDB0 register, and then, at the falling edge of one-shot pulse for timers A1, A2, and A4, the values set in the IDB1 register become output signals for each phase (internal signal) and consequently the three-phase PWM output changes. Afterward, the values in registers IDB0 and IDB1 alternately become an output signal for each phase at every falling edge of one-shot pulse for timers A1, A2, and A4.
When the INV15 bit in the INVC1 register is 0 (dead time enabled), a phase changing from active to nonactive changes simultaneously with output signals for each phase (internal signal), while a phase changing from nonactive to active changes when the dead time timer stops.

A transfer trigger is generated under the following conditions:

- The first timer B2 underflow after registers IDB0 and IDB1 are written.
- Writing to the TB2 register when timer B2 is stopped (when the INV10 bit in the INVC1 register is 1).
- Setting the INV07 bit in the INVC0 register to 1 (software trigger).

17.3.4 Sawtooth Wave Modulation Mode

In this mode, the sawtooth wave is modulated. Table 17.15 lists Sawtooth Wave Modulation Mode Specifications, and Figure 17.9 shows Example of Sawtooth Wave Modulation Mode Operation.

Table 17.15 Sawtooth Wave Modulation Mode Specifications

Item		Specification
Carrier wave cycle		$\frac{m+1}{fi}$ m: Setting value of the TB2 register, 0000h to FFFFh fi: Count source frequency (f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32)
Three-phase PWM output width		$\frac{n}{fi}$ n: Setting value of the TAi register, 0001h to FFFFh fi: Count source frequency (f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32)
Differences from triangular wave modulation mode	Reference cycle	Timer B2 cycle (cycle of the carrier wave)
	Timer B2 reload timing	Timer B2 underflow
	Three-phase PWM waveform control	Counts the value of the TAi register every time a timer Ai start trigger is generated (the TAi1 register is not used).
		The output levels set in registers IDB0 and IDB1 are transferred to the three-phase output shift register at every timer B2 underflow.
	Timer B2 interrupt	When the setting value in the ICTB2 register is n, a timer B2 interrupt request is generated every nth time of timer B2 underflow (not influenced by bits INV00 and INV01 in the INVC0 register).
	Dead time timer trigger	Both of the following: • Transfer trigger (generated at every timer B2 underflow) • Falling edge of timer Ai one-shot pulse
	Detection of a carrier wave cycle (first half or last half)	-

i = 1, 2, 4

Table 17.16 Registers and Settings in Sawtooth Wave Modulation Mode (1/2) (1)

Register	Bit	Function and Setting
INVC0	INV00	Disabled (Despite the settings, the ICTB2 register counts timer B2 underflow.)
	INV01	
	INV02	Set to 1 (three-phase motor control timer function used).
	INV03	Set to 1 (three-phase motor control timer output enabled).
	INV04	Select simultaneous conduction enabled or disabled.
	INV05	Simultaneous conduction detect flag
	INV06	Set to 1 (sawtooth wave modulation mode).
	INV07	Software trigger bit
INVC1	INV10	Select a start trigger for timers A1, A2, and A4.
	INV11	Set to 0.
	INV12	Select a count source for the dead time timer.
	INV13	Disabled
	INV14	Select the active level (either active high or active high).
	INV15	Select dead time enabled or disabled.
	INV16	Select a trigger for the dead time timer.
	7	Set to 0.
IDB0, IDB1	5 to 0	Set an output logic of the three-phase output shift register.
DTT	7 to 0	Set the dead time.
ICTB2	3 to 0	Set the frequency of timer B2 interrupt request.
TB2SC	PWCON	Set to 0 (timer B2 underflow).
	IVPCR1	Select three-phase output forced cutoff enabled or disabled.
	b7 to b2	Set to 0.
PDRF	PDRU, PDRV, PDRW	Position-data-retain bit
	PDRT	Select a position-data-retain trigger.
PFCR	PFC5 to PFC0	Select I/O port or three-phase PWM output.
TPRC	TPRC0	Set to 1 when writing to the PFCR register, or to 0 when not writing to it.
TA1, TA2, TA4	15 to 0	Set the one-shot pulse width.
TA11, TA21, TA41	15 to 0	Not used
TB2	15 to 0	Set the cycle of the carrier wave.

i = 1, 2, 4

Note:

1. This table does not describe a procedure.

Table 17.17 Registers and Settings in Sawtooth Wave Modulation Mode (2/2) (1)

Register	Bit	Function and Setting
TRGSR	TA1TGH to TA1TGL	Set to 01b (when using V-phase output control circuit).
	TA2TGH to TA2TGL	Set to 01b (when using W-phase output control circuit).
	TA3TGH to TA3TGL	(Not used for three-phase motor control timer.)
	TA4TGH to TA4TGL	Set to 01b (when using U-phase output control circuit).
TABSR	TA0S	Not used for three-phase motor control timer.
	TA1S	Set to 1 when starting counting, and to 0 when stopping counting.
	TA2S	Set to 1 when starting counting, and to 0 when stopping counting.
	TA3S	Not used for three-phase motor control timer.
	TA4S	Set to 1 when starting counting, and to 0 when stopping counting.
	TB0S	Not used for three-phase motor control timer.
	TB1S	Not used for three-phase motor control timer.
	TB2S	Set to 1 when starting counting, and to 0 when stopping counting.
TA1MR, TA2MR, TA4MR	TMOD1 to TMOD0	Set to 10b (one-shot timer mode).
	MR0	Set to 0.
	MR1	Set to 0.
	MR2	Set to 1 (select a trigger by setting bits TAiTGH and TAiTGL).
	MR3	Set to 0.
	TCK1 to TCK0	Select a count source.
TB2MR	TMOD1 to TMOD0	Set to 00b (timer mode).
	MR1 to MR0	Set to 00b.
	4	Set to 0.
	MR3	Set to 0.
	TCK1 to TCK0	Select a count source.
PCLKR	PCLK0	Select a count source.
TCKDIVC0	TCDIV00	Select the clock prior to timer AB division.
TACS0 to TACS2	7 to 0	Select a count source.
TBCS1	TCS3 to TCS0	Select a count source.
TAPOFS	POFSi	Set to 0.
UDF	TAiP	Set to 0.

i = 1, 2, 4

Note:

1. This table does not describe a procedure.

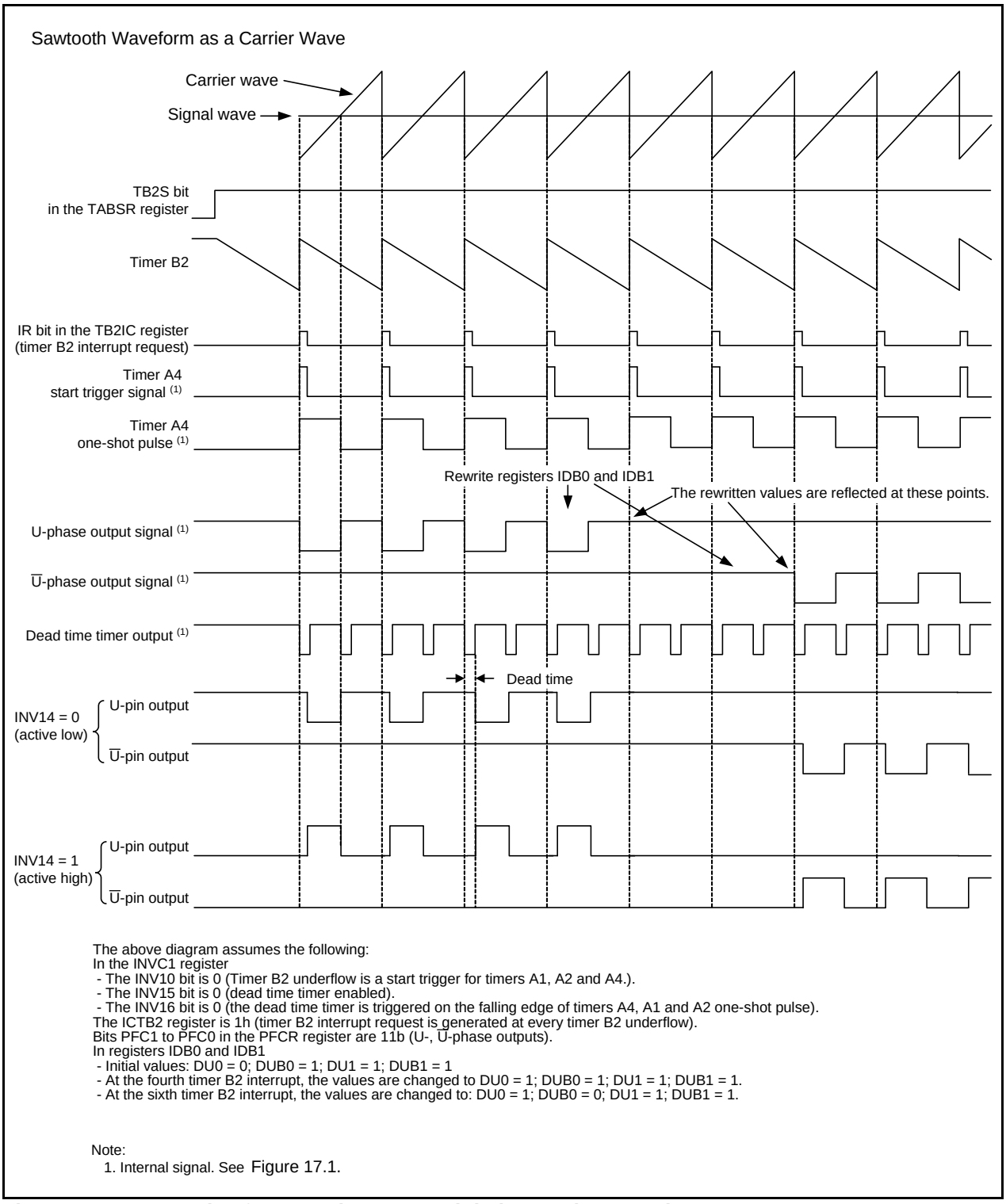


Figure 17.9 Example of Sawtooth Wave Modulation Mode Operation

17.3.4.1 Three-Phase PWM Waveform Output Timing Control

In sawtooth wave modulation mode, when a start trigger for timers A1, A2, and A4 is generated, the counter starts counting the value in the TAi register (i = 1, 2, 4).

17.3.4.2 Three-Phase PWM Waveform Output Level Control

In sawtooth wave modulation mode, the output levels set in registers IDB0 and IDB1 are transferred to the three-phase output shift register by a transfer trigger. After a transfer trigger is generated, first the value set in the IDB0 register, and then at the falling edge of one-shot pulse for timers A1, A2, and A4, the value set in the IDB1 register become output signals for each phase (internal signal) and consequently the three-phase PWM output changes. Then, the following two actions are repeated:
(1) The setting levels are transferred to the three-phase output shift register by a transfer trigger generated at timer B2 underflow, and therefore, the value in the IDB0 register becomes output signals for each phase. (2) The values set in the IDB1 register become output signals for each phase at the falling edge of one-shot pulse for timers A1, A2, and A4.
When the INV15 bit in the INVC1 register is 0 (dead time enabled), a phase changing from active to nonactive changes simultaneously with output signals for each phase (internal signal), while a phase changing from nonactive to active changes when the dead time timer stops.

A transfer trigger is generated under the following conditions:

- Timer B2 underflow (each time).
- Writing to the TB2 register when timer B2 is stopped (when the INV10 bit in the INVC1 register is 1).
- Setting the INV07 bit in the INVC0 register to 1 (software trigger).

17.4 Interrupts

The timer B2 interrupt and timer A1, A2, and A4 interrupts can be used with the three-phase motor control timer.

17.4.1 Timer B2 Interrupt

When the setting value in the ICTB2 register is n, a timer B2 interrupt request is generated at the timings below. For details, refer to the specifications and usage examples of each mode.
In triangular wave modulation three-phase mode 0 and sawtooth wave modulation mode, an interrupt request is generated at the nth count of timer B2 underflow.
In triangular wave modulation three-phase mode 1, an interrupt request is generated at the nth count of timing selected by setting bits INV01 to INV00 in the INVC0 register.

Refer to 12.7 “Interrupt Control” for details of interrupt control. Table 17.18 lists the Timer B2 Interrupt Related Register.

Table 17.18 Timer B2 Interrupt Related Register

Address	Register	Symbol	Reset Value
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b

17.4.2 Timer A1, A2, and A4 Interrupts

A timer Ai interrupt request is generated at the falling edge of timer Ai one-shot pulse (internal signal) (i = 1, 2, 4). Refer to 12.7 “Interrupt Control” for details of interrupt control. Table 17.19 lists Timer A1, A2, and A4 Interrupt Related Registers.

Table 17.19 Timer A1, A2, and A4 Interrupt Related Registers

Address	Register	Symbol	Reset Value
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
0059h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b

In the timer Ai interrupt, when the TMOD1 bit in the TAiMR register is changed from 0 to 1 (from timer mode or event counter mode to one-shot timer mode, PWM mode, or programmable output mode), the IR bit in the TAiIC register is occasionally becomes 1 (interrupt requested). Thus, when changing the TMOD1 bit, follow the steps below. Also refer to 12.13 “Notes on Interrupts”.

(1) Set bits ILVL2 to ILVL0 in the TAiIC register to 000b (interrupt disabled).
(2) Set the TAiMR register.
(3) Set the IR bit in the TAiIC register to 0 (interrupt not requested).

17.5 Notes on Three-Phase Motor Control Timer Function

17.5.1 Timer A and Timer B

Refer to 15.5 “Notes on Timer A” and 16.5 “Notes on Timer B”.

17.5.2 Influence of $\overline{SD}$

When a low-level signal is applied to the $\overline{SD}$ pin while the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on $\overline{SD}$ pin enabled), the following pins become high-impedance: P7_2/CLK2/TA1OUT/V/RXD1, P7_3/$\overline{CTS2}$/$\overline{RTS2}$/TA1IN/$\overline{V}$/TXD1, P7_4/TA2OUT/W/LIN0OUT, P7_5/TA2IN/$\overline{W}$/LIN0IN, P8_0/TA4OUT/U/TSUDA, P8_1/TA4IN/$\overline{U}$/TSUDB

18. Timer S

18.1 Introduction

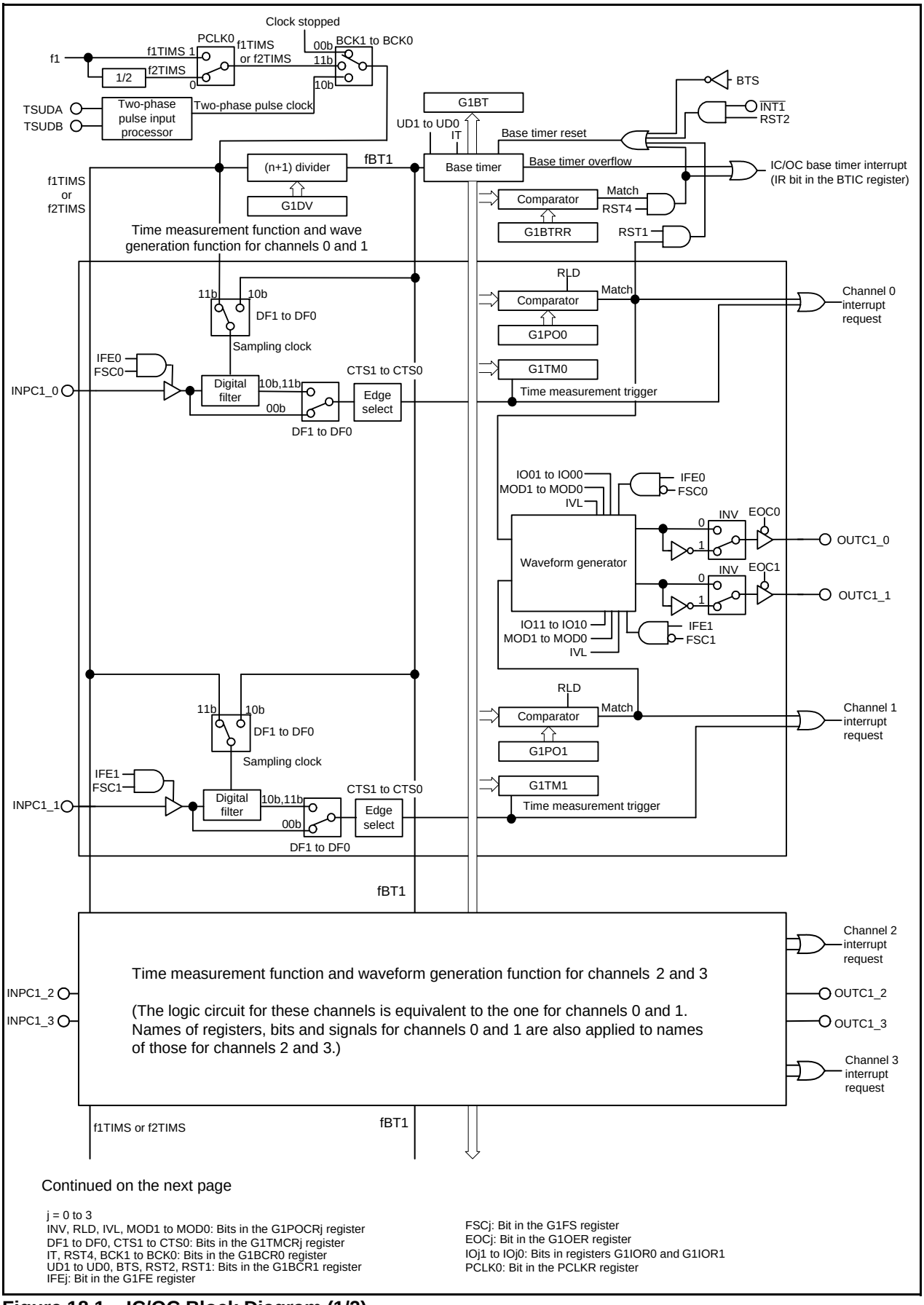
Timer S has an input capture/output compare function (IC/OC). The input capture (IC) is used for time measurement and the output compare (OC) is used for waveform generation. The IC/OC has one 16-bit free-running base timer and eight channels for time measurement and waveform generation.
Table 18.1 lists the specifications of the IC/OC.

Table 18.1 IC/OC Specifications

Item		Specification
Time measurement function (1)	Measurement channels	8 channels (channels 0 to 7)
	Trigger input edges	Selectable from rising edge, falling edge, or both edges of the INPC1_j pin
	Digital filter function	8 channels (channels 0 to 7)
	Prescaler function	2 channels (channels 6 and 7)
	Gate function	2 channels (channels 6 and 7)
	Digital debounce filter	1 channel (channel 7)
Waveform generation function (1)	Waveform generating channels	8 channels (channels 0 to 7)
	Waveform generation functions	Single-phase waveform output, inverted waveform output, and SR waveform output
	Output level select function when there is a compare-match	The output level can be changed from low to high or high to low.
	Selectable port function	Waveform output port or programmable I/O port selectable
	Other functions	Selectable initial output level Invertible output waveform
Base timer	Bit length	16 bits
	Count sources	f1TIMS or f2TIMS divided by (n + 1), two-phase pulse input divided by (n + 1) n is a G1DV register setting value from 0 to 255. There is no division when n = 0.
	Count operations	Increment, increment/decrement, two-phase pulse signal processing
	Base timer reset conditions	• Base timer value matches the G1PO0 register value (RST1) • Low is input to external interrupt pin $\overline{\text{INT1}}$ (RST2) • Base timer value matches the G1BTRR register value (RST4)
Interrupts	IC/OC channel interrupts	6 (IC/OC channel 0 interrupt, IC/OC channel 1 interrupt, IC/OC channel 2 interrupt, IC/OC channel 3 interrupt, IC/OC interrupt 0 (channels 0 to 7), IC/OC interrupt 1 (channels 0 to 7))
	IC/OC base timer interrupts	1 (The base timer interrupt is generated by base timer overflow, or by a base timer reset request that occurs when the G1BTRR register matches the base timer.)

j = 0 to 7

Note:
1. The time measurement function shares pins with the waveform generation function. Either the time measurement function or waveform generation function is selectable for each channel.



Continued on the next page

j = 0 to 3
INV, RLD, IVL, MOD1 to MOD0: Bits in the G1POCRj register
DF1 to DF0, CTS1 to CTS0: Bits in the G1TMCRj register
IT, RST4, BCK1 to BCK0: Bits in the G1BCR0 register
UD1 to UD0, BTS, RST2, RST1: Bits in the G1BCR1 register
IFEj: Bit in the G1FE register

FSCj: Bit in the G1FS register
EOCj: Bit in the G1OER register
IOj1 to IOj0: Bits in registers G1IOR0 and G1IOR1
PCLK0: Bit in the PCLKR register

Figure 18.1 IC/OC Block Diagram (1/2)

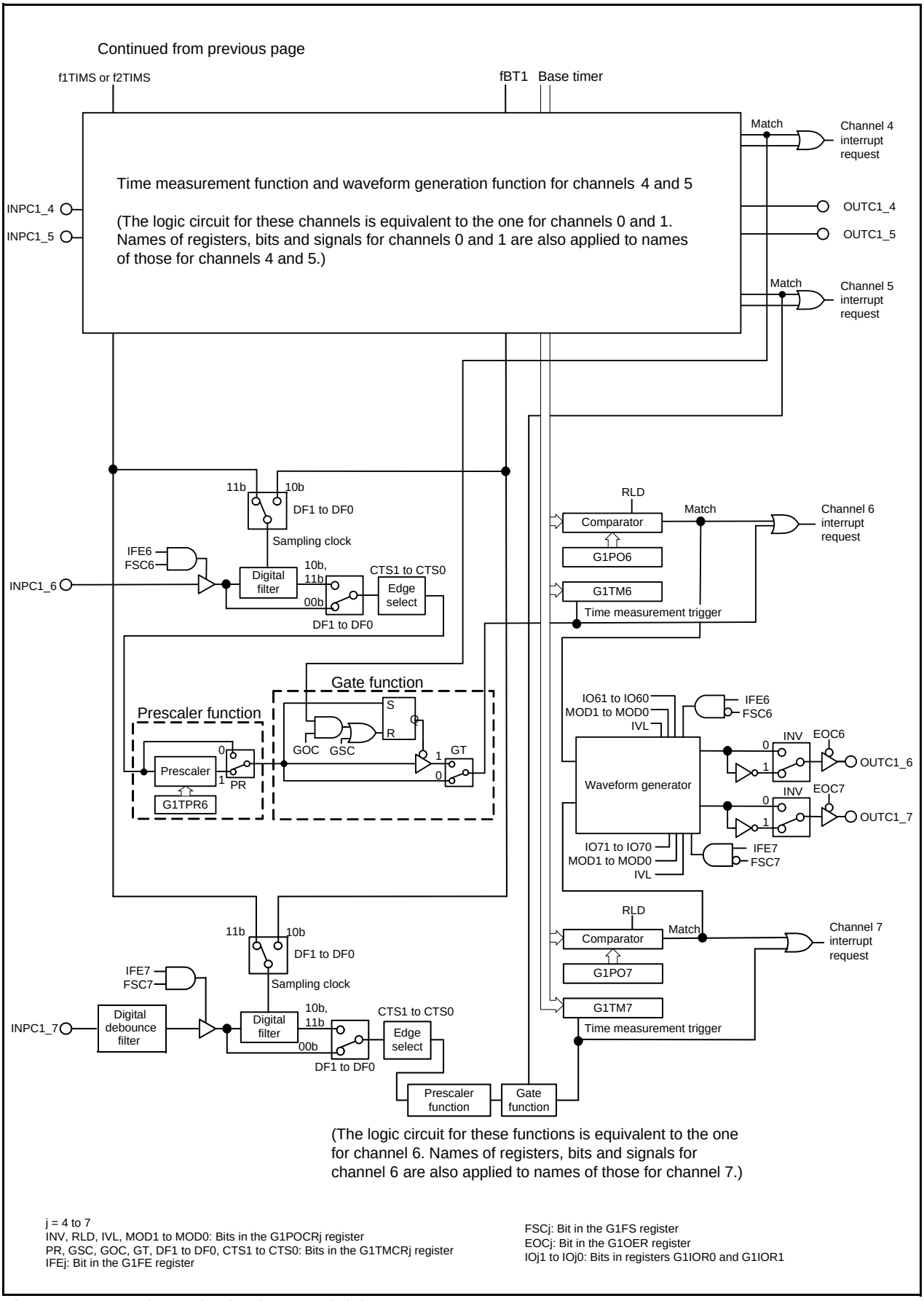


Figure 18.2 IC/OC Block Diagram (2/2)

Table 18.2 I/O Pins

Pin Name	I/O	Function
INPC1_0	Input (1)	Input pins for the time measurement function
INPC1_1	Input (1)	
INPC1_2	Input (1)	
INPC1_3	Input (1)	
INPC1_4	Input (1)	
INPC1_5	Input (1)	
INPC1_6	Input (1)	
INPC1_7	Input (1)	
OUTC1_0	Output	Output pins for the waveform generation function
OUTC1_1	Output	
OUTC1_2	Output	
OUTC1_3	Output	
OUTC1_4	Output	
OUTC1_5	Output	
OUTC1_6	Output	
OUTC1_7	Output	
TSUDA	Input (1)	A-phase input of two-phase pulse input signal processing
TSUDB	Input (1)	B-phase input of two-phase pulse input signal processing
$\overline{\text{INT1}}$	Input (1)	Z-phase input of two-phase pulse input signal processing

Notes:
1. When pins are used as input, set the port direction bits sharing pins to 0 (input mode).
2. Refer to 18.3.4 “I/O Port Select Function” for details on selecting the INPC1_j or OUTC1_j pin (j = 0 to 7).

18.2 Registers

Table 18.3 Registers (1/2)

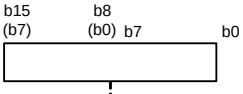
Address	Register Name	Register Symbol	Reset Value
02C0h	Time Measurement Register 0, Waveform Generation Register 0	G1TM0, G1PO0	XXh
02C1h			XXh
02C2h	Time Measurement Register 1, Waveform Generation Register 1	G1TM1, G1PO1	XXh
02C3h			XXh
02C4h	Time Measurement Register 2, Waveform Generation Register 2	G1TM2, G1PO2	XXh
02C5h			XXh
02C6h	Time Measurement Register 3, Waveform Generation Register 3	G1TM3, G1PO3	XXh
02C7h			XXh
02C8h	Time Measurement Register 4, Waveform Generation Register 4	G1TM4, G1PO4	XXh
02C9h			XXh
02CAh	Time Measurement Register 5, Waveform Generation Register 5	G1TM5, G1PO5	XXh
02CBh			XXh
02CCh	Time Measurement Register 6, Waveform Generation Register 6	G1TM6, G1PO6	XXh
02CDh			XXh
02CEh	Time Measurement Register 7, Waveform Generation Register 7	G1TM7, G1PO7	XXh
02CFh			XXh
02D0h	Waveform Generation Control Register 0	G1POCR0	0X00 XX00b
02D1h	Waveform Generation Control Register 1	G1POCR1	0X00 XX00b
02D2h	Waveform Generation Control Register 2	G1POCR2	0X00 XX00b
02D3h	Waveform Generation Control Register 3	G1POCR3	0X00 XX00b
02D4h	Waveform Generation Control Register 4	G1POCR4	0X00 XX00b
02D5h	Waveform Generation Control Register 5	G1POCR5	0X00 XX00b
02D6h	Waveform Generation Control Register 6	G1POCR6	0X00 XX00b
02D7h	Waveform Generation Control Register 7	G1POCR7	0X00 XX00b
02D8h	Time Measurement Control Register 0	G1TMCR0	00h
02D9h	Time Measurement Control Register 1	G1TMCR1	00h
02DAh	Time Measurement Control Register 2	G1TMCR2	00h
02DBh	Time Measurement Control Register 3	G1TMCR3	00h
02DCh	Time Measurement Control Register 4	G1TMCR4	00h
02DDh	Time Measurement Control Register 5	G1TMCR5	00h
02DEh	Time Measurement Control Register 6	G1TMCR6	00h
02DFh	Time Measurement Control Register 7	G1TMCR7	00h
02E0h	Base Timer Register	G1BT	XXh
02E1h			XXh
02E2h	Base Timer Control Register 0	G1BCR0	00h
02E3h	Base Timer Control Register 1	G1BCR1	00h
02E4h	Time Measurement Prescaler Register 6	G1TPR6	00h
02E5h	Time Measurement Prescaler Register 7	G1TPR7	00h
02E6h	Function Enable Register	G1FE	00h
02E7h	Function Select Register	G1FS	00h
02E8h	Base Timer Reset Register	G1BTRR	XXh
02E9h			XXh
02EAh	Count Source Divide Register	G1DV	00h
02ECh	Waveform Output Master Enable Register	G1OER	00h
02EEh	Timer S I/O Control Register 0	G1IOR0	00h

Table 18.4 Registers (2/2)

Address	Register Name	Register Symbol	Reset Value
02EFh	Timer S I/O Control Register 1	G1IOR1	00h
02F0h	Interrupt Request Register	G1IR	XXh
02F1h	Interrupt Enable Register 0	G1IE0	00h
02F2h	Interrupt Enable Register 1	G1IE1	00h

18.2.1 Time Measurement Register j (G1TMj) (j = 0 to 7)

Time Measurement Register j (j = 0 to 7)



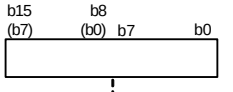
Symbol	Address	Reset Value
G1TM0 to G1TM2	02C1h to 02C0h, 02C3h to 02C2h, 02C5h to 02C4h	XXXXh
G1TM3 to G1TM5	02C7h to 02C6h, 02C9h to 02C8h, 02CBh to 02CAh	XXXXh
G1TM6 to G1TM7	02CDh to 02CCh, 02CFh to 02CEh	XXXXh

Function	RW
Data register for the base timer. The base timer value is stored at every measurement timing.	RO

Read the G1TMj register in 16-bit units.

18.2.2 Waveform Generation Register j (G1POj) (j = 0 to 7)

Waveform Generation Register j (j = 0 to 7)



Symbol	Address	Reset Value
G1PO0 to G1PO2	02C1h to 02C0h, 02C3h to 02C2h, 02C5h to 02C4h	XXXXh
G1PO3 to G1PO5	02C7h to 02C6h, 02C9h to 02C8h, 02CBh to 02CAh	XXXXh
G1PO6 to G1PO7	02CDh to 02CCh, 02CFh to 02CEh	XXXXh

Function	Setting Range	RW
• When the RLD bit in the G1POCRj register is 0, the value written to the G1POj register is immediately reloaded to an internal buffer and reflected in the output waveform. • When the RLD bit in the G1POCRj register is 1 and the base timer is reset, the value is reloaded.	0000h to FFFFh	RW

Write to the G1POj register in 16-bit units.

The value written to this register is reflected to the internal buffer when the clock is synchronized with the base timer count source (fBT1). When the waveform generation function is used, the output waveform is changed when this register matches with the base timer. Refer to 18.3.3.1 “Single-Phase Waveform Output Mode”, 18.3.3.2 “Inverted Waveform Output Mode” and 18.3.3.3 “Set/Reset Waveform Output Mode (SR Waveform Output Mode)” for details.

When the base timer value matches the G1PO0 register value while the RST1 bit in the G1BCR1 register is 1, the base timer becomes 0000h. When this function is used, the value of the G1POj register (j = 1 to 7) used to generate output waveforms should be smaller than the value of the G1PO0 register. Do not set the G1PO0 register to 0000h. While the RST1 bit is 1, rewrite the G1PO0 register when the BTS bit in the G1BCR1 register is 0 (base timer reset). Refer to 18.3.1.4 “Base Timer Reset While the Base Timer is Counting” for details.

When the base timer value matches the G1POk register value (k = j - 2), while bits GT and GOC in the G1TMCRj register (j = 6, 7) are both 1 (GT = 1: gate function used), the gate function is released. When this function is used, the value set in the G1POk register should be smaller than the maximum value of the base timer.

When the base timer reset is used with the G1BTRR register, set the register values as follows:

G1POk value < G1BTTR value

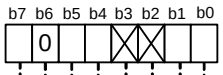
When the base timer reset is used with the G1PO0 register, set the register values as follows:

G1POk value < G1PO0 value

Refer to 18.3.2.1 “Gate Function (Channel 6 and 7)” for details.

18.2.3 Waveform Generation Control Register j (G1POCRj) (j = 0 to 7)

Waveform Generation Control Register j (j = 0 to 7)



Symbol	Address	Reset Value
G1POCR0 to G1POCR3	02D0h, 02D1h, 02D2h, 02D3h	0X00 XX00b
G1POCR4 to G1POCR7	02D4h, 02D5h, 02D6h, 02D7h	0X00 XX00b

Bit Symbol	Bit Name	Function	RW
MOD0	Operating mode select bit	b1 b0 0 0: Single waveform output mode 0 1: SR waveform output mode 1 0: Inverted waveform output mode 1 1: Do not set.	RW
MOD1			RW
— (b3-b2)	No register bits. If necessary, set to 0. The read value is undefined.		—
IVL	Default output value select bit	0: Output low as default value 1: Output high as default value	RW
RLD	G1POj register value reload timing select bit	0: Reload the G1POj register on a write access 1: Reload the G1POj register when the base timer is reset	RW
— (b6)	Reserved	Set to 0.	RW
INV	Output level inversion select bit	0: Output level not inverted 1: Output level inverted	RW

Rewrite the G1POCRj register when the BTS bit in the G1BCR1 is 0 (base timer reset), the FSCj bit in the G1FS register is 0 (waveform generation function selected), and the IFEj bit in the G1FE register is 0 (channel j function disabled). When the G1POCRj register is rewritten, set the BTS bit to 1 after one or more fBT1 cycles.

MOD1 and MOD0 (Operating mode select bit) (b1-b0)

To select SR waveform output mode, set bits MOD1 and MOD0 of an even channel (channel j (j = 0, 2, 4, or 6)) and bits MOD1 and MOD0 of the next odd channel (channel j + 1) both to 01b. The waveform is output from the OUT1_j pin of an even channel. In SR waveform output mode, set EOCj + 1 bit in the G1OER register to 1 (output disabled).

IVL (Output default select bit) (b4)

When a value is written to the IVL bit, the FSCj bit (j = 0 to 7) in the G1FS register is set to 0 (waveform generation function selected), and the IFEj bit in the G1FE register is set to 1 (channel j function enabled), the set level is output.

RLD (G1POj register value reload timing select bit) (b5)

For SR waveform output mode, set both even channels (channel j (j = 0, 2, 4, or 6)) and odd channels (channel j+1).
When writing a value to the G1POj register (j = 0 to 7) while the BTS bit is 0 (base timer reset) and the RLD bit is 1 (reload the G1POj register when the base timer is reset), the written value will not be reloaded to a buffer.
Therefore, when the BTS bit is 0, set the RLD bit to 0 (reload on a write access), write a value to the G1POj register, and then set the RLD bit to 1 after one or more fBT1 cycles.
When the RLD bit is set to 1, the value will not be reloaded at the following timings:

- When the base timer counter changes from FFFFh to 0000h immediately after writing FFFFh to the base timer while incrementing in increment mode or increment/decrement mode.
- When the base timer counter changes from 0000h to FFFFh immediately after writing 0000h to the base timer while decrementing in increment/decrement mode.

INV (Output level inversion select bit) (b7)

The output level inversion function is located at the final step of waveform generation circuit. When the INV bit is set to 1 (output level inverted), the default output value becomes high if the IVL bit is set to 0, and the default output value becomes low if the IVL bit is set to 1.

18.2.4 Time Measurement Control Register j (G1TMCRj) (j = 0 to 7)

Time Measurement Control Register j (j = 0 to 7)

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	Reset Value
G1TMCR0 to G1TMCR3	02D8h, 02D9h, 02DAh, 02DBh	00h
G1TMCR4 to G1TMCR7	02DCh, 02DDh, 02DEh, 02DFh	00h

Bit Symbol	Bit Name	Function	RW
CTS0	Time measurement trigger select bit	b1 b0 0 0: No time measurement 0 1: Rising edge 1 0: Falling edge 1 1: Both edges	RW
CTS1			RW
DF0	Digital filter select bit	b3 b2 0 0: No digital filter 0 1: Do not set. 1 0: Digital filter used. Sampling clock is fBT1. 1 1: Digital filter used Sampling clock is f1TIMS or f2TIMS.	RW
DF1			RW
GT	Gate function select bit	0: Gate function not used 1: Gate function used	RW
GOC	Gate function release select bit	0: Gate function release is disabled. 1: Gate function release is enabled by matching the base timer with the G1POk register. k = 4 when j = 6, k = 5 when j = 7	RW
GSC	Gate function release bit	No gating when 1 is written to this bit	RW
PR	Prescaler select bit	0: Prescaler not used 1: Prescaler used	RW

When writing to registers G1TMCR6 and G1TMCR7, use the MOV instruction. To release the gate during a write access, set the GSC bit to 1; otherwise, set it to 0.

CTS1 and CTS0 (Time measurement trigger select bit) (b1-b0)

Rewrite these bits when the BTS bit in the G1BCR1 register is 0 (base timer reset).

DF1 and DF0 (Digital filter select bit) (b3-b2)

Rewrite these bits when the BTS bit is 0.
When the PCLK0 bit in the PCLKR register is 0 while bits DF1 and DF0 are 11b, f2TIMS is selected as the sampling clock, and when the PCLK0 bit is 1, f1TIMS is selected as the sampling clock.
The two-phase pulse clock does not become a sampling clock of digital filter even if bits BCK1 and BCK0 are 10b (two-phase pulse clock).

GT (Gate function select bit) (b4)

The GT bit is only available in registers G1TMCR6 and G1TMCR7. Set bits 7 to 4 in registers G1MCR0 to G1TMCR5 to 0000b.
The value written to this bit is reflected to the internal circuit when the clock is synchronized with the base timer count source (fBT1).

GOC (Gate function release select bit) (b5)

The GOC bit is only available in registers G1TMCR6 and G1TMCR7. Set bits 7 to 4 in registers G1MCR0 to G1TMCR5 to 0000b.
The GOC bit is enabled only when the GT bit is 1.
Refer to 18.2.2 “Waveform Generation Register j (G1POj) (j = 0 to 7)” for details on the G1POk register (k = 4 when j = 6; k = 5 when j = 7).
The value written to this bit is reflected to the internal circuit when the clock is synchronized with the base timer count source (fBT1).

GSC (Gate function release bit) (b6)

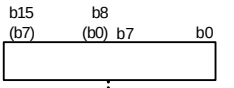
The GSC bit is only available in registers G1TMCR6 and G1TMCR7. Set bits 7 to 4 in registers G1MCR0 to G1TMCR5 to 0000b.
The GSC bit is enabled only when the GT bit is 1.
Set this bit to 1 when the gate function is released; otherwise set it to 0.
The value written to this bit is reflected to the internal circuit when the clock is synchronized with the base timer count source (fBT1).

PR (Prescaler select bit) (b7)

Rewrite the PR bit when bits BCK1 and BCK0 in the G1BCR0 register are 00b (clock stops).
The PR bit is only available in registers G1TMCR6 and G1TMCR7. Set bits 7 to 4 in registers G1MCR0 to G1TMCR5 to 0000b.

18.2.5 Base Timer Register (G1BT)

Base Timer Register



Symbol	Address	Reset Value
G1BT	02E1h to 02E0h	XXXXh

Function	RW
- While the base timer is running (when the BTS bit in the G1BCR1 register is 1 and bits BCK1 and BCK0 in the G1BCR0 register are values other than 00b): When reading this register, the current base timer value is returned. When the base timer is reset, this register becomes 0000h. - When the BTS bit in the G1BCR1 register is 0: This register becomes 0000h. When reading this register, an undefined value is returned.	RW

Read the G1BT register in 16-bit units. Do not write to this register.

While the base timer is counting, the base timer value is stored to this register, and synchronized with the base timer count source (fBT1).

The base timer stops counting only when bits BCK1 and BCK0 in the G1BCR0 register are 00b (clock stopped). When bits BCK1 and BCK0 are not 00b, the base timer operates.

When the BTS bit in the G1BCR1 register is 0 (base timer reset), the G1BT register is held in the reset state (0000h). The counter stays in this state without counting. When the BTS bit is set to 1, the state is released and the base timer starts counting.

18.2.6 Base Timer Control Register 0 (G1BCR0)

Base Timer Control Register 0

b7	b6	b5	b4	b3	b2	b1	b0
		0	0	0			

Symbol: G1BCR0 | Address: 02E2h | Reset Value: 00h

Bit Symbol	Bit Name	Function	RW
BCK0	Count source select bit	b1 b0 0 0: Clock stopped 0 1: Do not set. 1 0: Two-phase pulse clock 1 1: f1TIMS or f2TIMS	RW
BCK1			RW
RST4	Base timer reset source select bit 4	0: The base timer is not reset when the base timer and G1BTRR register values match. 1: The base timer is reset when the base timer and G1BTRR register values match.	RW
— (b5-b3)	Reserved	Set to 0.	RW
CH7INSEL	Channel 7 input select bit	0: P2_7/OUTC1_7/INPC1_7 pin 1: P1_7/INPC1_7 pin	RW
IT	Base timer interrupt select bit	0: Overflow of bit 15 1: Overflow of bit 14	RW

Rewrite the G1BCR0 register when the BTS bit in the G1BCR1 register is 0 (base timer reset).

BCK1 and BCK0 (Count source select bit) (b1-b0)

After rewriting bits BCK1 and BCK0 from 00b (clock stopped) to another value, before rewriting these bits to another value, first set them to 00b, wait four or more cycles of the previous count source, and then rewrite the bits.

The two-phase pulse clock (10b) can be used only when bits UD1 and UD0 in the G1BCR1 register are 10b (two-phase pulse signal processing). Do not set bits BCK1 and BCK0 to 10b with other count operations.

When bits BCK1 and BCK0 are 11b and the PCLK0 bit in the PCLKR register is 0, f2TIMS is selected. When the PCLK0 bit is 1, f1TIMS is selected. Change the PCLK0 bit when bits BCK1 and BCK0 are 00b.

RST4 (Base timer reset source select bit 4) (b2)

When the RST4 bit is 1, set the RST1 bit in the G1BCR1 register to 0.

IT (Base timer interrupt select bit) (b7)

While the IT bit is 0 (overflow of bit 15), when incrementing, if b15 of the base timer becomes 0 from 1 (i.e. the base timer value becomes 0000h from FFFFh) during counting, the base timer overflows. When decrementing, the base timer overflows if b15 of the base timer becomes 1 from 0 (i.e. 7FFFh from 8000h).

While the IT bit is 1 (overflow of bit 14), when incrementing, if b14 of the base timer becomes 0 from 1 during counting, the base timer overflows. When decrementing, the base timer overflows if b14 of the base timer becomes 1 from 0.

When the base timer overflows, the IR bit in the BTIC register becomes 1 (IC/OC base timer interrupt requested).

18.2.7 Base Timer Control Register 1 (G1BCR1)

Base Timer Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0
0				0			0

Symbol: G1BCR1 | Address: 02E3h | Reset Value: 00h

Bit Symbol	Bit Name	Function	RW
— (b0)	Reserved	Set to 0.	RW
RST1	Base timer reset source select bit 1	0: The base timer is not reset when the base timer and G1PO0 register values match. 1: The base timer is reset when the base timer and G1PO0 register values match.	RW
RST2	Base timer reset source select bit 2	0: The base timer is not reset when low is input to the $\overline{INT1}$ pin. 1: The base timer is reset when low is input to the $\overline{INT1}$ pin.	RW
— (b3)	Reserved	Set to 0.	RW
BTS	Base timer start bit	0: Base timer reset 1: Base timer starts counting	RW
UD0	Increment/decrement control bit	b6 b5 0 0: Increment 0 1: Increment/decrement 1 0: Two-phase pulse signal processing 1 1: Do not set.	RW
UD1			
— (b7)	Reserved	Set to 0.	RW

RST1 (Base timer reset source select bit 1) (b1)

To rewrite the RST1 bit, rewrite it while the BTS bit is 0 (base timer reset) and then change the BTS bit to 1 (base timer starts counting).

When the base timer value matches the G1PO0 register value while the RST1 bit is 1, the base timer is reset after two fBT1 cycles. Refer to 18.3.1.4 “Base Timer Reset While the Base Timer is Counting” for details. When the RST1 bit is 1, set the RST4 bit in the G1BCR0 register to 0 (the base timer is not reset when the base timer and G1BTRR register values match).

RST2 (Base timer reset source select bit 2) (b2)

To rewrite the RST2 bit, rewrite it while the BTS bit is 0 and then rewrite the BTS bit to 1.

BTS (Base timer start bit) (b4)

The value written to this bit is reflected to the internal circuit when the clock is synchronized with the base timer count source (fBT1).

UD1 and UD0 (Increment/decrement control bit) (b6-b5)

To rewrite bits UD1 and UD0, rewrite them while the BTS bit is 0 and then rewrite the BTS bit to 1.

When single-waveform output mode or SR waveform output mode is selected, set bits UD1 and UD0 to 00b (increment). When inverted waveform output mode is selected, set these bits to 00b (increment) or 01b (increment/decrement).

18.2.8 Time Measurement Prescaler Register j (G1TPRj) (j = 6 and 7)

Time Measurement Prescaler Register j (j = 6 and 7)

b7 b0

Symbol	Address	Reset Value
G1TPR6	02E4h	00h
G1TPR7	02E5h	00h

Function	Set Value	RW
If the setting value is n, time measurement is performed every time a trigger input is counted (n + 1) times.	00h to FFh	RW

The value written to this register is reflected to the internal circuit when the clock is synchronized with the base timer count source (fBT1).
After rewriting the PR bit in the G1TMCRj register to 1 (prescaler function used) from 0 (prescaler function not used), the first prescaler cycle may remain as n instead of being counted as (n + 1). In the subsequent prescaler cycles, the setting value n becomes (n + 1).

18.2.9 Function Enable Register (G1FE)

Function Enable Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	Reset Value
G1FE	02E6h	00h

Bit Symbol	Bit Name	Function	RW
IFE0	Channel 0 function enable bit	0: Channel j function disabled 1: Channel j function enabled (j = 0 to 7)	RW
IFE1	Channel 1 function enable bit		RW
IFE2	Channel 2 function enable bit		RW
IFE3	Channel 3 function enable bit		RW
IFE4	Channel 4 function enable bit		RW
IFE5	Channel 5 function enable bit		RW
IFE6	Channel 6 function enable bit		RW
IFE7	Channel 7 function enable bit		RW

The value written to this register is reflected to the internal circuit when the clock is synchronized with the base timer count source (fBT1). When the channel j (j = 0 to 7) function is disabled, the corresponding pins become programmable I/O ports.

18.2.10 Function Select Register (G1FS)

Function Select Register

b7	b6	b5	b4	b3	b2	b1	b0

Symbol: G1FS
Address: 02E7h
Reset Value: 00h

Bit Symbol	Bit Name	Function	RW
FSC0	Channel 0 time measurement/ waveform generation function select bit	0: Waveform generation function selected 1: Time measurement function selected	RW
FSC1	Channel 1 time measurement/ waveform generation function select bit		RW
FSC2	Channel 2 time measurement/ waveform generation function select bit		RW
FSC3	Channel 3 time measurement/ waveform generation function select bit		RW
FSC4	Channel 4 time measurement/ waveform generation function select bit		RW
FSC5	Channel 5 time measurement/ waveform generation function select bit		RW
FSC6	Channel 6 time measurement/ waveform generation function select bit		RW
FSC7	Channel 7 time measurement/ waveform generation function select bit		RW

Rewrite the G1FS register when the BTS bit in the G1BCR1 register is 0 (base timer reset).

18.2.11 Base Timer Reset Register (G1BTRR)

Base Timer Reset Register

b15 (b7) b8 (b0) b7 b0

Symbol	Address	Reset Value
G1BTRR	02E9h to 02E8h	XXXXh

Function	Setting Range	RW
When the RST4 bit in the G1BCR0 register is 1, the base timer is reset by matching the G1BTRR register value and base timer value.	0001h to FFFFh	RW

Write to the G1BTRR register in 16-bit units. The value written to this register is reflected to the internal circuit when the clock is synchronized with the base timer count source (fBT1).
While the RST4 bit in the G1BCR0 register is 1, rewrite the G1BTRR register when the BTS bit in the G1BCR1 register is 0 (base timer reset).

18.2.12 Count Source Divide Register (G1DV)

Count Source Divide Register

b7 b0

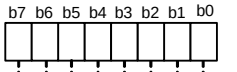
Symbol	Address	Reset Value
G1DV	02EAh	00h

Function	Setting Range	RW
Divide f1TIMS, f2TIMS, or the two-phase input pulse clock by (n + 1) to generate fBT1. n: G1DV setting value	00h to FFh	RW

Rewrite the G1DV register when bits BCK1 and BCK0 in the G1BCR0 register are 00b (clock stopped).

18.2.13 Waveform Output Master Enable Register (G1OER)

Waveform Output Master Enable Register



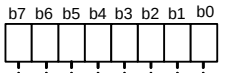
Symbol	Address	Reset Value
G1OER	02ECh	00h

Bit Symbol	Bit Name	Function	RW
EOC0	OUTC1_0 output disable bit	0: Output enabled 1: Output disabled (OUTC1_0 pin is used as a programmable I/O port)	RW
EOC1	OUTC1_1 output disable bit	0: Output enabled 1: Output disabled (OUTC1_1 pin is used as a programmable I/O port)	RW
EOC2	OUTC1_2 output disable bit	0: Output enabled 1: Output disabled (OUTC1_2 pin is used as a programmable I/O port)	RW
EOC3	OUTC1_3 output disable bit	0: Output enabled 1: Output disabled (OUTC1_3 pin is used as a programmable I/O port)	RW
EOC4	OUTC1_4 output disable bit	0: Output enabled 1: Output disabled (OUTC1_4 pin is used as a programmable I/O port)	RW
EOC5	OUTC1_5 output disable bit	0: Output enabled 1: Output disabled (OUTC1_5 pin is used as a programmable I/O port)	RW
EOC6	OUTC1_6 output disable bit	0: Output enabled 1: Output disabled (OUTC1_6 pin is used as a programmable I/O port)	RW
EOC7	OUTC1_7 output disable bit	0: Output enabled 1: Output disabled (OUTC1_7 pin is used as a programmable I/O port)	RW

The EOCj bit (j = 0 to 7) is enabled only when the FSCj bit in the G1FS register is 0 (waveform generation function is selected) and the IFEj bit in the G1FE register is 1 (channel j function enabled). When an odd channel is selected in SR waveform output mode or the FSCj bit in the G1FS register is 1 (time measurement function is selected), set the EOCj bit to 1. The value written to the EOCj bit is immediately reflected in output waveforms, independently of fBT1.

18.2.14 Timer S I/O Control Register 0 (G1IOR0)

Timer S I/O Control Register 0



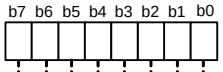
Symbol: G1IOR0 | Address: 02EEh | Reset Value: 00h

Bit Symbol	Bit Name	Function	RW
IO00	OUTC1_0 output control bit	b1 b0 0 0: Outputs high or low, depending on the mode selected by bits MOD1 and MOD0 in the G1POCR0 register. 0 1: Outputs low by compare match with the G1PO0 register. 1 0: Outputs high by compare match with the G1PO0 register. 1 1: Do not set.	RW
IO01			RW
IO10	OUTC1_1 output control bit	b3 b2 0 0: Outputs high or low, depending on the mode selected by bits MOD1 and MOD0 in the G1POCR1 register. 0 1: Outputs low by compare match with the G1PO1 register. 1 0: Outputs high by compare match with the G1PO1 register. 1 1: Do not set.	RW
IO11			RW
IO20	OUTC1_2 output control bit	b5 b4 0 0: Outputs high or low, depending on the mode selected by bits MOD1 and MOD0 in the G1POCR2 register. 0 1: Outputs low by compare match with the G1PO2 register. 1 0: Outputs high by compare match with the G1PO2 register. 1 1: Do not set.	RW
IO21			RW
IO30	OUTC1_3 output control bit	b7 b6 0 0: Outputs high or low, depending on the mode selected by bits MOD1 and MOD0 in the G1POCR3 register. 0 1: Outputs low by compare match with the G1PO3 register. 1 0: Outputs high by compare match with the G1PO3 register. 1 1: Do not set.	RW
IO31			RW

The value written to this register is reflected to the internal circuit when the clock is synchronized with the base timer count source (fBT1).
Set the corresponding output control bits IOj1 and IOj0 to 00b for the input channels selected by setting the FSCj bit (j = 0 to 3) in the G1FS register to 1 (time measurement function is selected).
In SR waveform output mode, set bits IOj1 and IOj0 to 00b for both odd and even channels.

18.2.15 Timer S I/O Control Register 1 (G1IOR1)

Timer S I/O Control Register 1



Symbol	Address	Reset Value
G1IOR1	02EFh	00h

Bit Symbol	Bit Name	Function	RW
IO40	OUTC1_4 output control bit	b1 b0 0 0: Outputs high or low, depending on the mode selected by bits MOD1 and MOD0 in the G1POCR4 register. 0 1: Output low by compare match with the G1PO4 register. 1 0: Outputs high by compare match with the G1PO4 register. 1 1: Do not set.	RW
IO41			RW
IO50	OUTC1_5 output control bit	b3 b2 0 0: Outputs high or low, depending on the mode selected by bits MOD1 and MOD0 in the G1POCR5 register. 0 1: Outputs low by compare match with the G1PO5 register. 1 0: Outputs high by compare match with the G1PO5 register. 1 1: Do not set.	RW
IO51			RW
IO60	OUTC1_6 output control bit	b5 b4 0 0: Outputs high or low, depending on the mode selected by bits MOD1 and MOD0 in the G1POCR6 register. 0 1: Outputs low by compare match with the G1PO6 register. 1 0: Outputs high by compare match with the G1PO6 register. 1 1: Do not set.	RW
IO61			RW
IO70	OUTC1_7 output control bit	b7 b6 0 0: Outputs high or low, depending on the mode selected by bits MOD1 and MOD0 in the G1POCR7 register. 0 1: Outputs low by compare match with the G1PO7 register. 1 0: Outputs high by compare match with the G1PO7 register. 1 1: Do not set.	RW
IO71			RW

The value written to this register is reflected to the internal circuit when the clock is synchronized with the base timer count source (fBT1).
Set the corresponding output control bits IOj1 and IOj0 to 00b for the input channels determined by setting the FSCj bit (j = 4 to 7) in the G1FS register to 1 (time measurement function is selected).
In SR waveform output mode, set bits IOj1 and IOj0 to 00b for both odd and even channels.

18.2.16 Interrupt Request Register (G1IR)

Interrupt Request Register

b7	b6	b5	b4	b3	b2	b1	b0

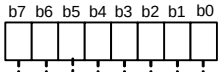
Symbol: G1IR
Address: 02F0h
Reset Value: XXh

Bit Symbol	Bit Name	Function	RW
G1IR0	Channel 0 interrupt request bit	0: Interrupt not requested 1: Interrupt requested	RW
G1IR1	Channel 1 interrupt request bit		RW
G1IR2	Channel 2 interrupt request bit		RW
G1IR3	Channel 3 interrupt request bit		RW
G1IR4	Channel 4 interrupt request bit		RW
G1IR5	Channel 5 interrupt request bit		RW
G1IR6	Channel 6 interrupt request bit		RW
G1IR7	Channel 7 interrupt request bit		RW

The G1IRj bit does not become 0 (interrupt not requested) automatically when an interrupt is received (j = 0 to 7).
To set the bit to 0, wait one or more fBT1 cycles after the G1IRj bit becomes 1 (interrupt requested), and perform the operation shown in 18.5.2 “Changing the G1IR Register”.
The value written to these bits is reflected to the internal circuit in synchronization with the CPU clock.

18.2.17 Interrupt Enable Register 0 (G1IE0)

Interrupt Enable Register 0

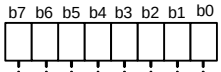


Symbol	Address	Reset Value
G1IE0	02F1h	00h

Bit Symbol	Bit Name	Function	RW
G1IE00	Channel 0 interrupt enable 0 bit	0: IC/OC interrupt 0 request disabled 1: IC/OC interrupt 0 request enabled	RW
G1IE01	Channel 1 interrupt enable 0 bit		RW
G1IE02	Channel 2 interrupt enable 0 bit		RW
G1IE03	Channel 3 interrupt enable 0 bit		RW
G1IE04	Channel 4 interrupt enable 0 bit		RW
G1IE05	Channel 5 interrupt enable 0 bit		RW
G1IE06	Channel 6 interrupt enable 0 bit		RW
G1IE07	Channel 7 interrupt enable 0 bit		RW

18.2.18 Interrupt Enable Register 1 (G1IE1)

Interrupt Enable Register 1



Symbol: G1IE1 | Address: 02F2h | Reset Value: 00h

Bit Symbol	Bit Name	Function	RW
G1IE10	Channel 0 interrupt enable 1 bit	0: IC/OC interrupt 1 request disabled 1: IC/OC interrupt 1 request enabled	RW
G1IE11	Channel 1 interrupt enable 1 bit		RW
G1IE12	Channel 2 interrupt enable 1 bit		RW
G1IE13	Channel 3 interrupt enable 1 bit		RW
G1IE14	Channel 4 interrupt enable 1 bit		RW
G1IE15	Channel 5 interrupt enable 1 bit		RW
G1IE16	Channel 6 interrupt enable 1 bit		RW
G1IE17	Channel 7 interrupt enable 1 bit		RW

18.3 Operations

18.3.1 Base Timer

The base timer is a free-running counter which counts an internally generated count source.
Table 18.5 lists the specifications of the base timer, Figure 18.3 shows the block diagram of the base timer, Table 18.6 lists the base timer associated registers and their settings, Figure 18.4 shows an operation example with incrementing, Figure 18.5 shows an operation example with incrementing/decrementing, and Figure 18.7 shows an operation example with two-phase pulse signal processing.

Table 18.5 Base Timer Specifications

Item	Specification
Count source (fBT1)	f1TIMS or f2TIMS divided by (n + 1), two-phase pulse clock divided by (n + 1) n is a G1DV register setting value from 0 to 255. However, when n is 0, there is no division.
Count operations	• Increment • Increment/decrement • Two-phase pulse signal processing
Count start condition	Set the BTS bit in the G1BCR1 register to 1 (base timer starts counting).
Count stop condition	Set the BTS bit in the G1BCR1 register to 0 (base timer reset).
Base timer reset conditions	• The base timer value matches the G1BTRR register value. • The base timer value matches the G1PO0 register value. • A low signal is input to the $\overline{\text{INT1}}$ external interrupt pin. • The BTS bit in the G1BCR1 register is 0 (base timer reset).
Base timer reset value	0000h
Interrupt requests	• Bit 14 or bit 15 in the G1BT register overflows. • The base timer value matches the G1BTRR register value.
Read from base timer	• The count value is returned when reading the G1BT register while the base timer is counting. • An undefined value is returned when reading the G1BT register while the base timer is being reset and the BTS bit is 0.

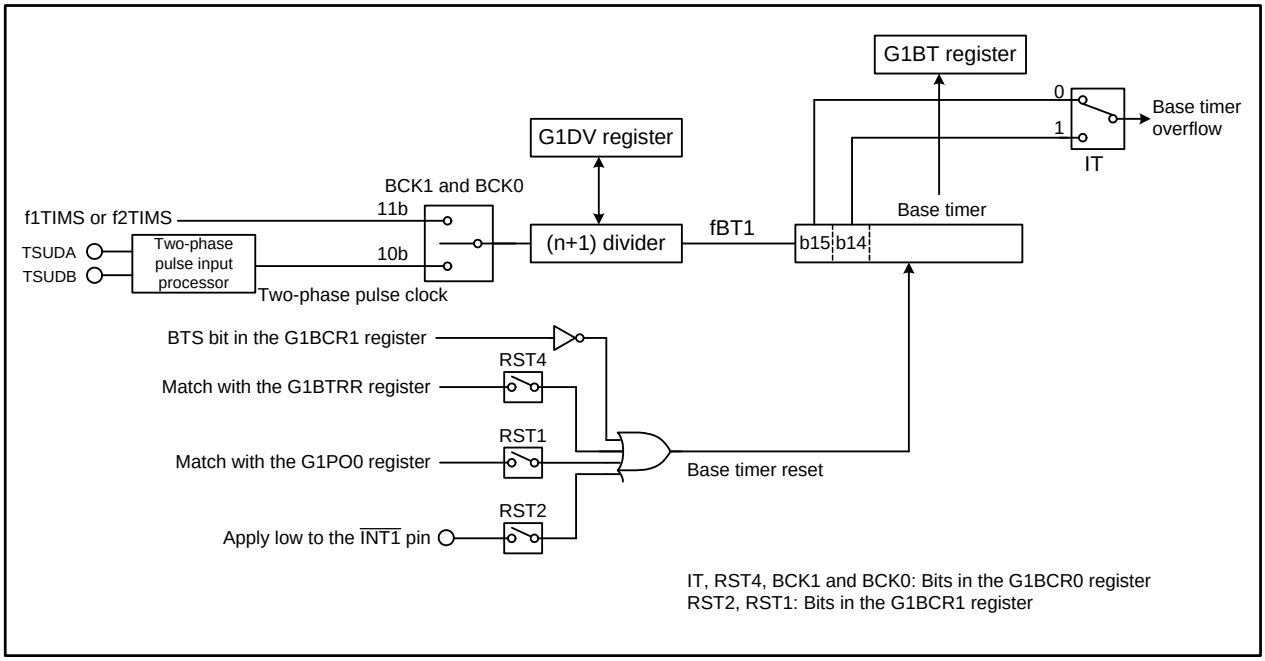


Figure 18.3 Base Timer Block Diagram

Table 18.6 Base Timer Associated Register Settings (1)

Register	Bit	Function and Setting Value		
		Base timer reset not used	Base timer reset by matching with the G1BTRR register	Base timer reset by matching with the G1PO0 register
G1BCR0	BCK1 and BCK0	Select a count source.	Select a count source.	Select a count source.
	RST4	Set to 0.	Set to 1.	Set to 0.
	IT	Select a timing of IC/OC base timer interrupt request.	Select a timing of IC/OC base timer interrupt request.	Select a timing of IC/OC base timer interrupt request.
G1BCR1	RST1	Set to 0.	Set to 0.	Set to 1.
	RST2	Select whether the $\overline{\text{INT1}}$ pin is used for base timer reset.	Select whether the $\overline{\text{INT1}}$ pin is used for base timer reset.	Select whether the $\overline{\text{INT1}}$ pin is used for base timer reset.
	BTS	Set to 1 to start the base timer count. Set to 0 to reset the base timer count.	Set to 1 to start the base timer count. Set to 0 to reset the base timer count.	Set to 1 to start the base timer count. Set to 0 to reset the base timer count.
	UD1 and UD0	Select a count operation.	Select a count operation.	Select a count operation.
G1BT	—	Base timer value can be read.	Base timer value can be read.	Base timer value can be read.
G1DV	—	Set a divide ratio of the count source.	Set a divide ratio of the count source.	Set a divide ratio of the count source.
G1BTRR	—	— (Do not use)	Set a base timer reset timing	— (Do not use)
G1POCR0	MOD1 and MOD0	— (Do not use for the base timer)		Set to 00b
G1PO0	—	— (Do not use for the base timer)		Set a base timer reset timing
G1FS	FSC0	— (Do not use for the base timer)		Set to 0.
G1FE	IFE0	— (Do not use for the base timer)		Set to 1.
G1IOR0	IO01 and IO00	— (Do not use for the base timer)		Set to 00b.

Note:
1. This table does not describe a procedure.

18.3.1.1 Increment

The counter starts incrementing from 0000h to FFFFh, then returns back to 0000h, and continues to increment.

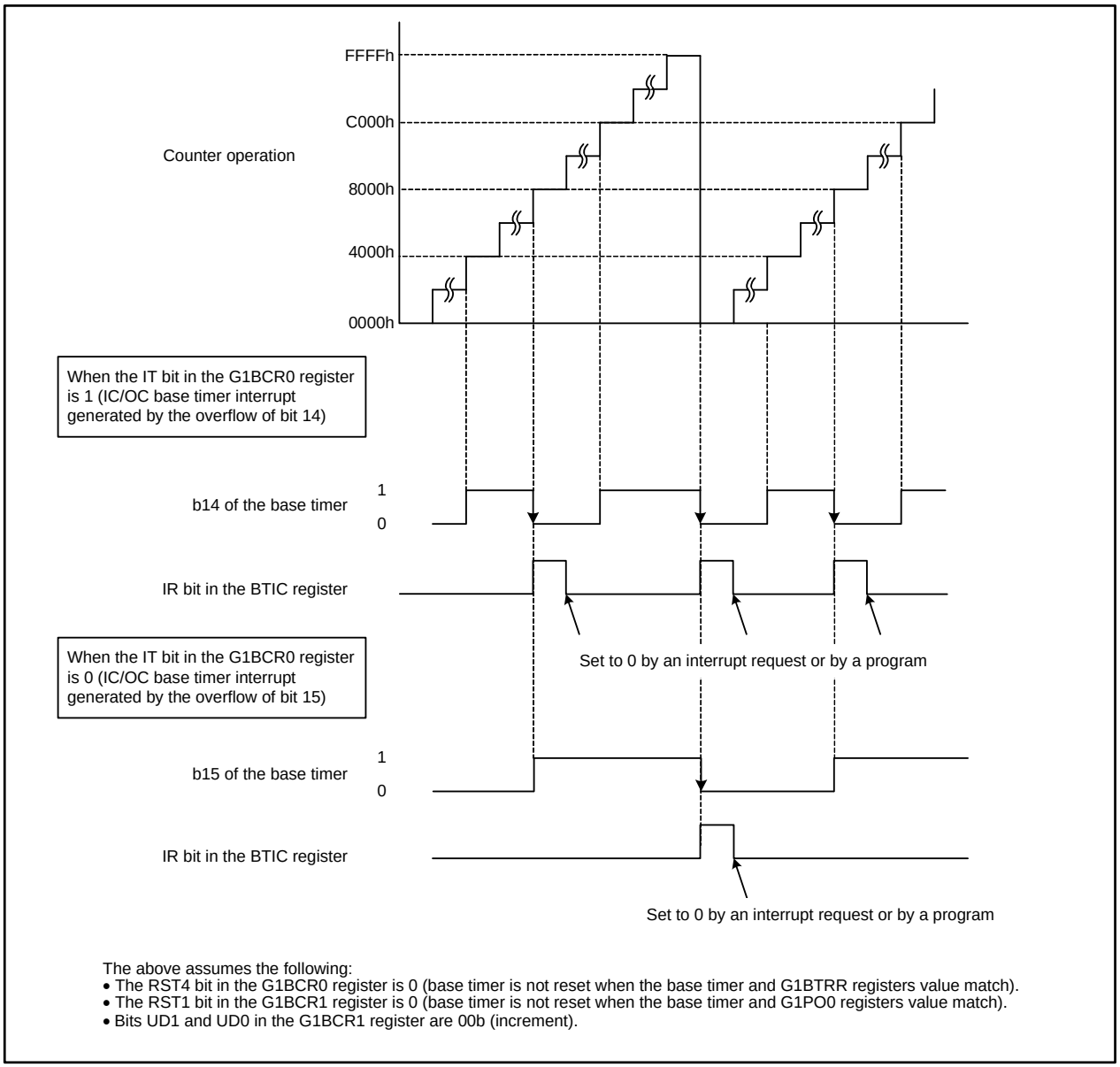


Figure 18.4 Increment

18.3.1.2 Increment/Decrement

The counter starts incrementing from 0000h to FFFFh, then decrements from FFFFh to 0000h. When the counter reaches 0000h, the base timer increments again.

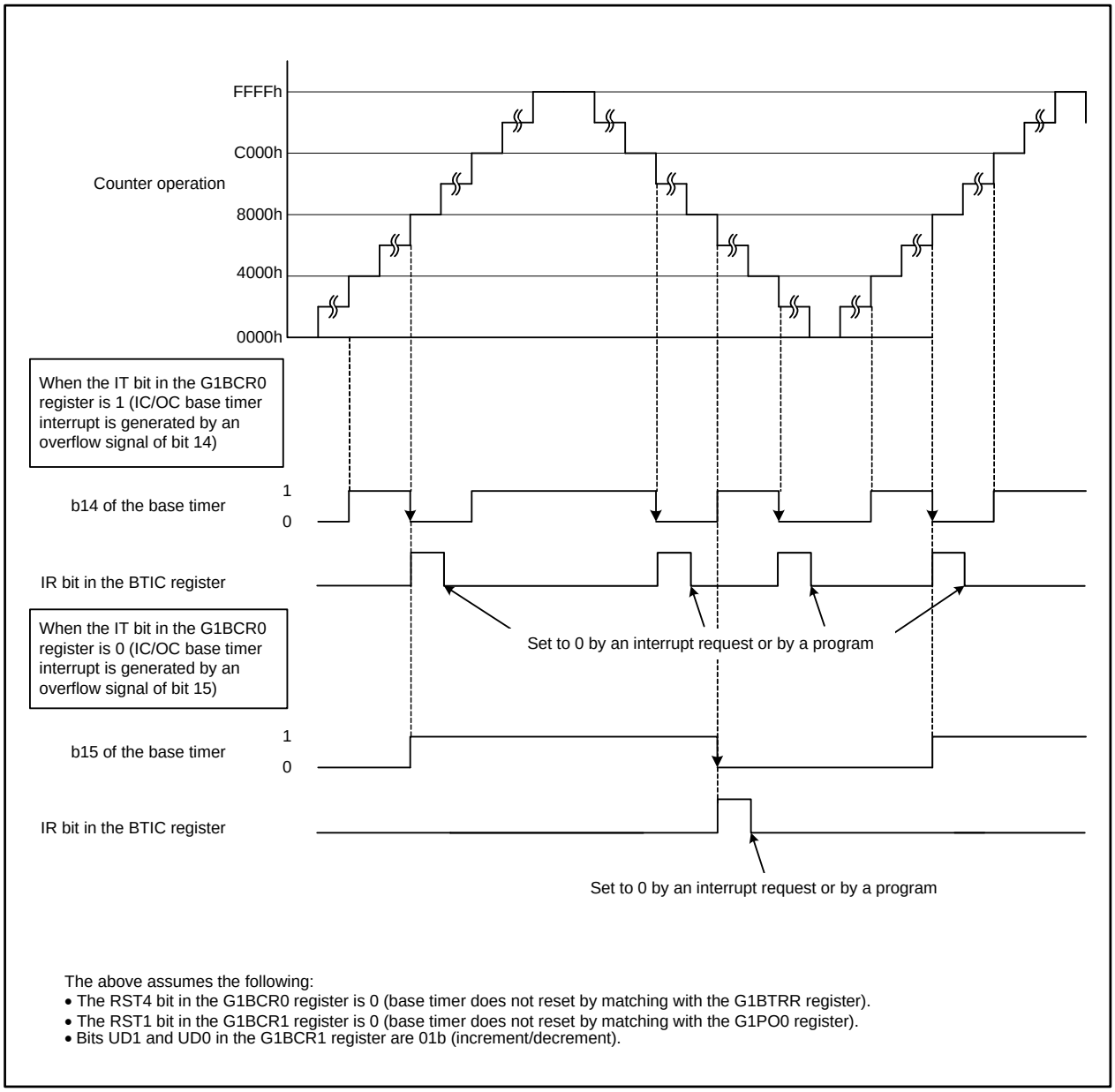


Figure 18.5 Increment/Decrement

18.3.1.3 Two-Phase Pulse Signal Processing

This count operation counts two-phase pulse input from pins TSUDA and TSUDB.
Set the following bits as shown below for two-phase pulse signal processing.

Bits BCK1 and BCK0 in the G1BCR0 register: 10b (two-phase pulse clock)
RST2 bit in the G1BCR1 register: 1 (the base timer is reset when low is input to the $\overline{\text{INT1}}$ pin.)
Bits UD1 to UD0 in the G1BCR1 register (two-phase pulse signal processing)

Figure 18.6 shows Two-Phase Pulse Signal Processing, and Figure 18.7 shows Two-Phase Pulse Signal Processing (When Using the Base Timer Reset).

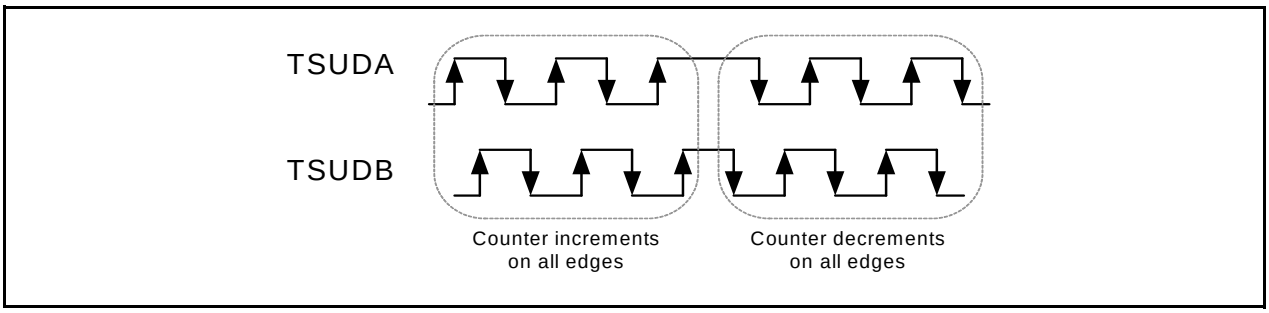
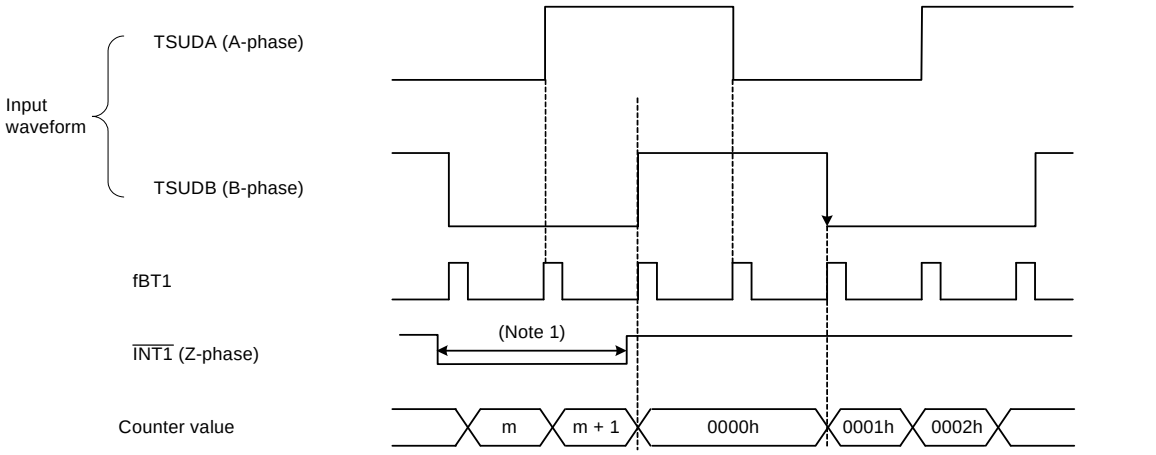
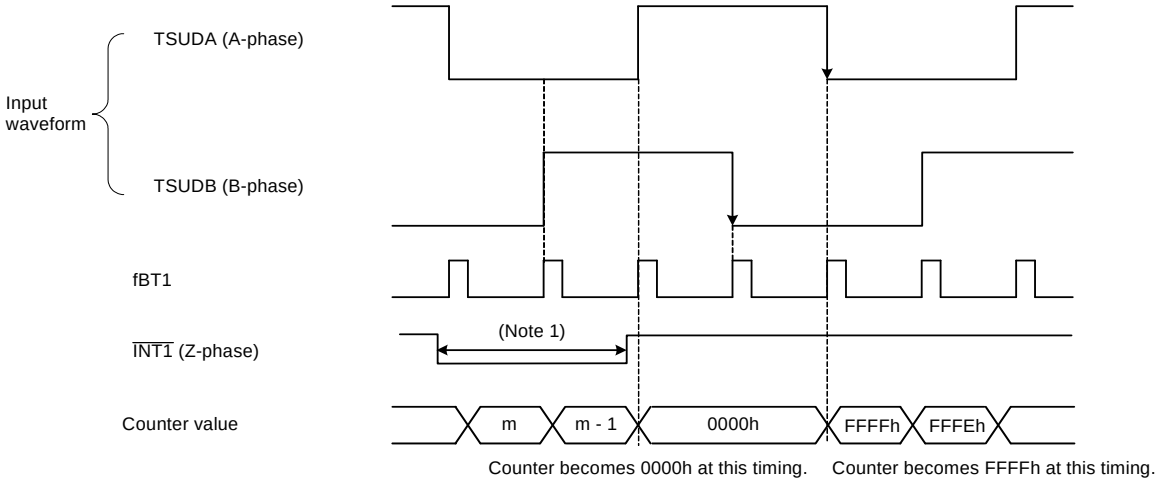


Figure 18.6 Two-Phase Pulse Signal Processing

(1) The base timer is reset while it is incrementing.



(2) The base timer is reset while it is decrementing.



The above assumes the following:
- The RST2 bit in the G1BCR1 register is 1 (base timer is reset by applying low to the INT1 pin).
- The G1DV register is 00b (no division).

Note:
1. The INT1 pin should be driven low for at least 1.5 fBT1 cycles.

Figure 18.7 Two-Phase Pulse Signal Processing (When Using the Base Timer Reset)

18.3.1.4 Base Timer Reset While the Base Timer is Counting

The base timer is reset by one of the following conditions:

- The G1BTRR register value matches the base timer value after setting the RST4 in the G1BCR0 register to 1 (the base timer is reset by matching with the G1BTRR register).
- The G1PO0 register value matches the base timer value after setting the RST1 bit in the G1BCR1 register to 1 (the base timer is reset by matching with the G1PO0 register).
- Apply a low signal to the $\overline{\text{INT1}}$ external interrupt pin after setting the RST2 bit in the G1BCR1 register to 1 (the base timer is reset by applying a low signal to the $\overline{\text{INT1}}$ pin).

Do not set bits RST4 and RST1 to 1 at the same time.
When the base timer counter is running, but not free-running, and the base timer is reset by matching the G1BTRR register, channel 0 can be used for the waveform generation function.

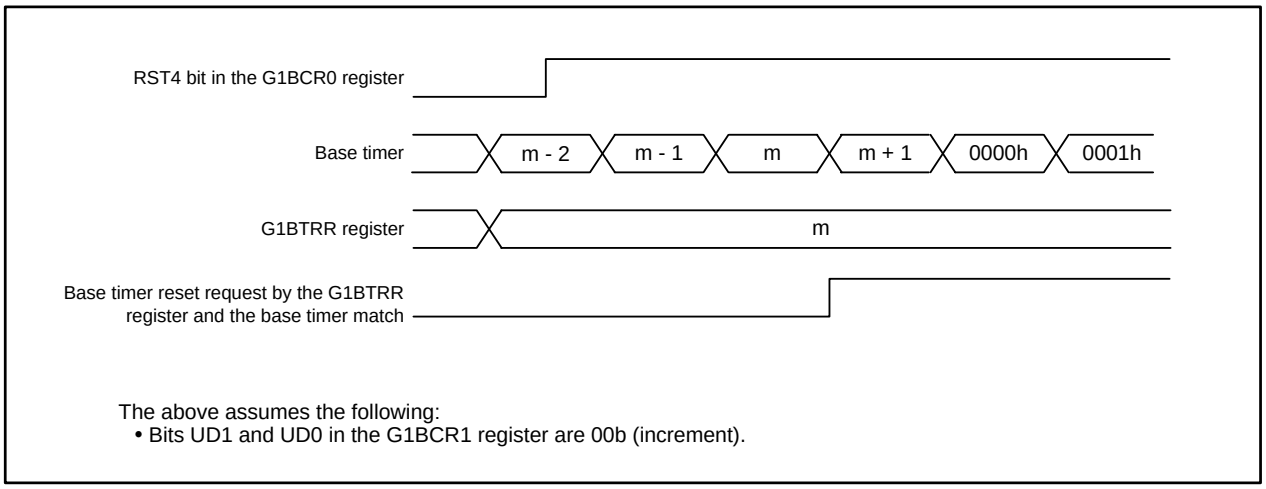


Figure 18.8 Base Timer Reset with the G1BTRR Register

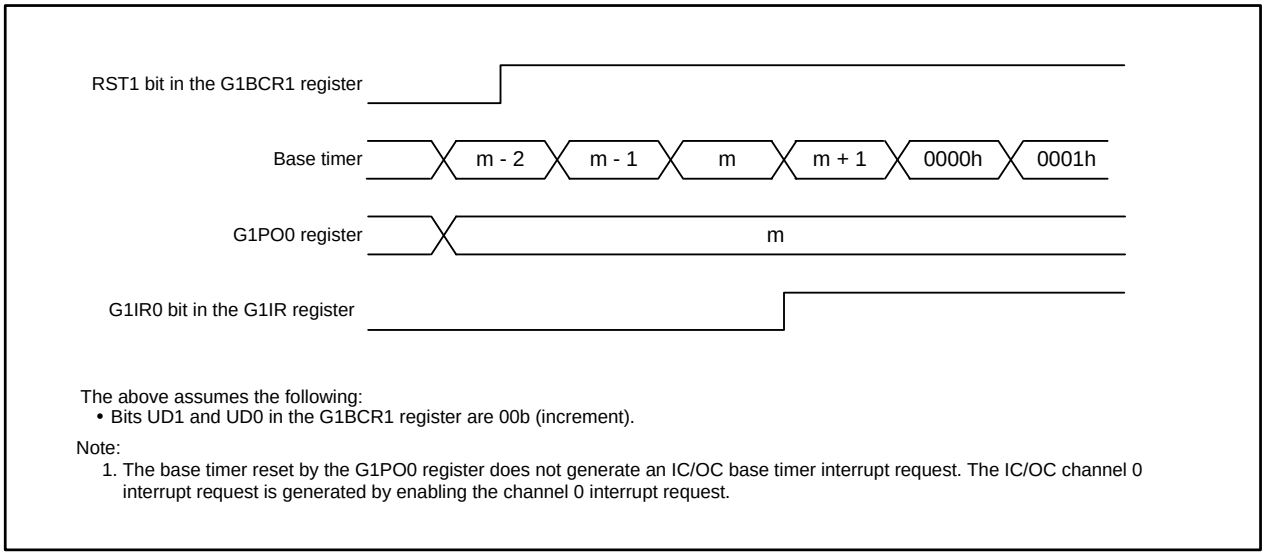
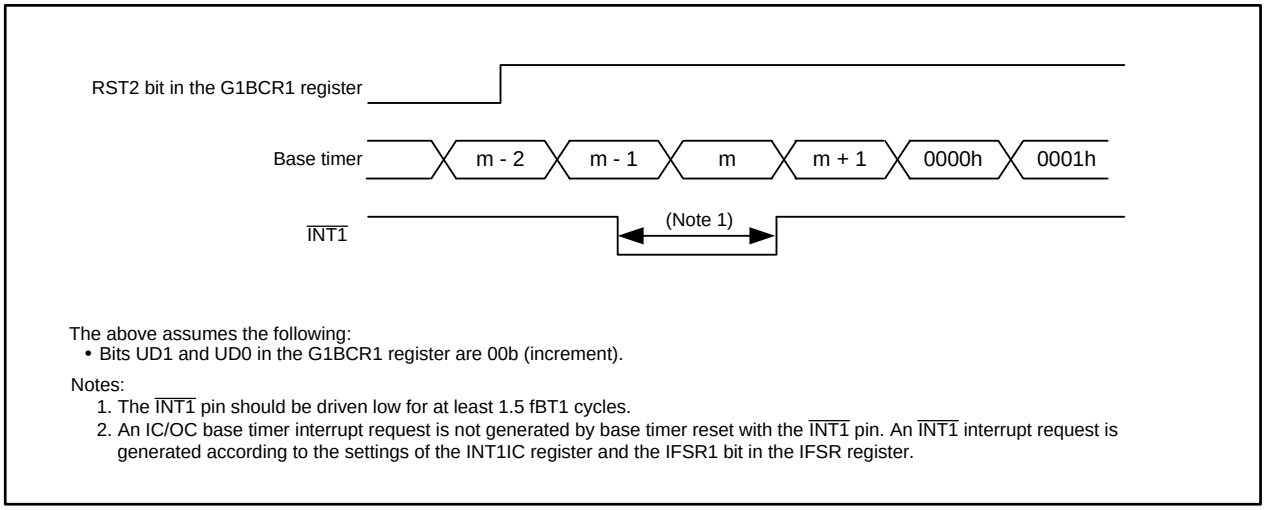


Figure 18.9 Base Timer Reset with the G1PO0 Register



The above assumes the following:
- Bits UD1 and UD0 in the G1BCR1 register are 00b (increment).

Notes:
1. The $\overline{INT1}$ pin should be driven low for at least 1.5 fBT1 cycles.
2. An IC/OC base timer interrupt request is not generated by base timer reset with the $\overline{INT1}$ pin. An $\overline{INT1}$ interrupt request is generated according to the settings of the INT1IC register and the IFSR1 bit in the IFSR register.

Figure 18.10 Base Timer Reset with $\overline{INT1}$ Pin Input

Table 18.7 to Table 18.9 list the relationship between base timer count operation and the count value when the base timer is reset.

Table 18.7 Increment

Reset Source	Count Direction	Count Value
RST1 reset	No change (increments)	0000h
RST2 reset	No change (increments)	0000h
RST4 reset	No change (increments)	0000h

Table 18.8 Increment/Decrement

Reset Source	Increment Operation		Decrement Operation	
	Count direction	Count value	Count direction	Count value
RST1 reset	Increment to decrement	— (count continues)	No change (decrements)	— (count continues)
RST2 reset	Increment to decrement	— (count continues)	No change (decrements)	— (count continues)
RST4 reset	Increment to decrement	— (count continues)	No change (decrements)	— (count continues)

Table 18.9 Two-Phase Pulse Signal Processing

Reset Source	Increment Operation		Decrement Operation	
	Count direction	Count value	Count direction	Count value
RST1 reset	No change (increments)	0000h	No change (decrements)	— (count continues)
RST2 reset	No change (increments)	0000h	No change (decrements)	0000h
RST4 reset	No change (increments)	0000h	No change (decrements)	— (count continues)

18.3.2 Time Measurement Function

The base timer value is stored in the G1TMj register (j = 0 to 7) using an external input as a trigger. Table 18.10 lists the specifications of the time measurement function. Table 18.11 lists the time measurement function associated registers and their settings. Figure 18.11 to Figure 18.12 show the operation examples of the time measurement function.
Figure 18.13 shows the operation example of the prescaler function and gate function.

Table 18.10 Time Measurement Function Specifications

Item	Specification
Measurement channels	Channels 0 to 7
Trigger input polarity	Selectable from rising edge, falling edge, or both edges of the INPC1_j pin input.
Measurement start condition	While the FSCj bit in the G1FS register is 1 (time measurement function selected), set the IFEj bit in the G1FE register to 1 (channel j function enabled).
Measurement stop condition	Set the IFEj bit to 0 (channel j function disabled).
Time measurement timing	• Without prescaler: every trigger input • With prescaler (channels 6 and 7): every (G1TPRk register value + 1) time a trigger is input
Interrupt request occurrence timing	At the time measurement timing
INPC1_ j pin function	Trigger input
Selectable functions	• Digital filter The digital filter judges a trigger input level at each sampling clock (f1TIMS, f2TIMS, or fBT1) and passes the pulse that matches its signal level three times. • Prescaler (channels 6 and 7) Time measurement is executed every (G1TPRk register value + 1) times a trigger is input. • Gate function (channels 6 and 7) After a time measurement is performed by the first trigger input, subsequent trigger inputs are disabled. • Digital debounce filter (channel 7) When P1_7/INPC1_7 is selected, the digital debounce filter is enabled.

j = 0 to 7; k = 6 and 7

Table 18.11 Time Measurement Function Associated Registers (1)

Register	Bit	Function
G1TMj	—	Time measurement result can be read.
G1TMCRj	CTS1 and CTS0	Select a time measurement trigger.
	DF1 and DF0	Select whether the digital filter function is used. If used, select a sampling clock to use for the function.
G1TMCRk	GT, GOC, GSC	Select if the gate function is used.
	PR	Select whether the prescaler function is used.
G1TPRk	—	Set a value if the prescaler function is used.
G1FS	FSCj	Set to 1 (time measurement function selected).
G1FE	IFEj	Set to 1 (channel j function enabled).
G1POCRp	MOD1 and MOD0	Set to 00b. (2)
G1POp	—	Set a gate release timing. (2)
G1FS	FSCp	Set to 0. (2)
G1FE	IFEp	Set to 1. (2)
G1OER	EOCp	Set to 1. (2)
G1IOR1	IOp1 and IOp0	Set to 00b. (2)
G1CBR0	CH7INSEL	Select a pin to allocate INPC1_7.

j = 0 to 7; k = 6 and 7; p = k - 2

Notes:
1. This table does not describe a procedure.
2. Set when bits GT and GOC in the G1TMCRk register are 1.

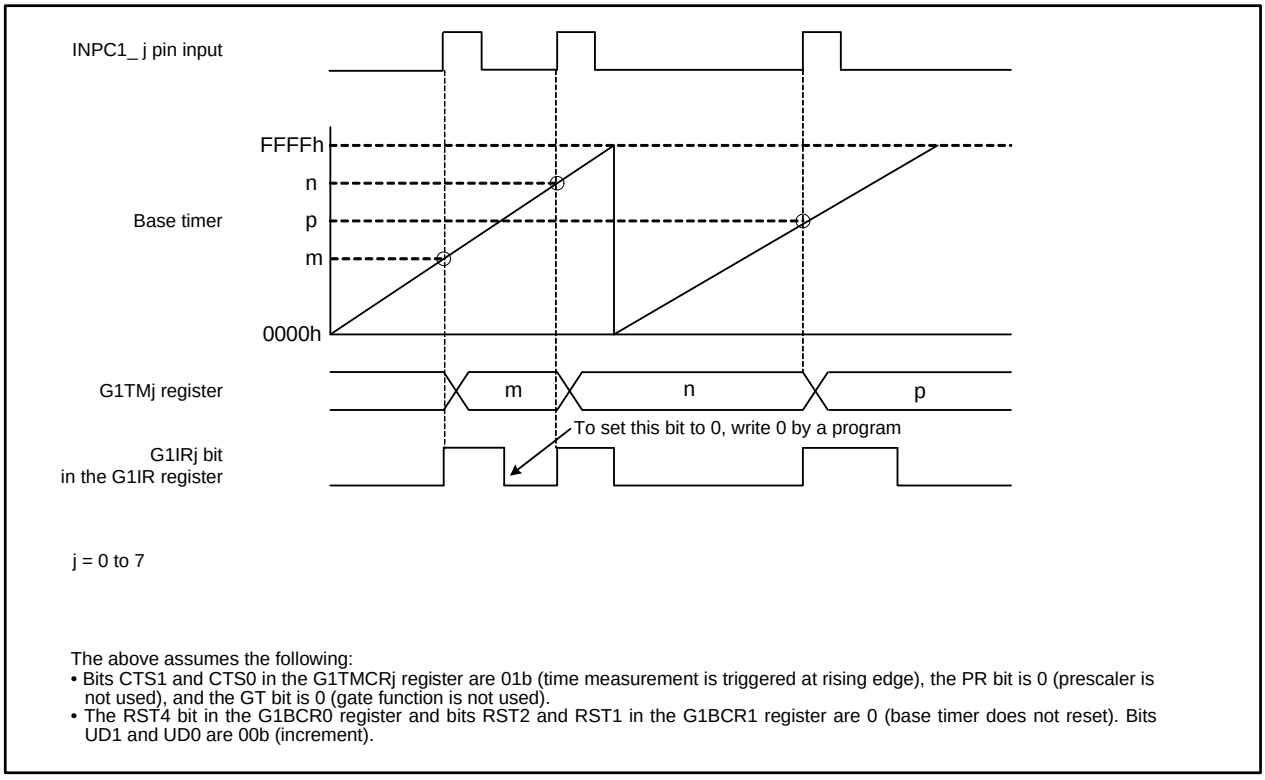
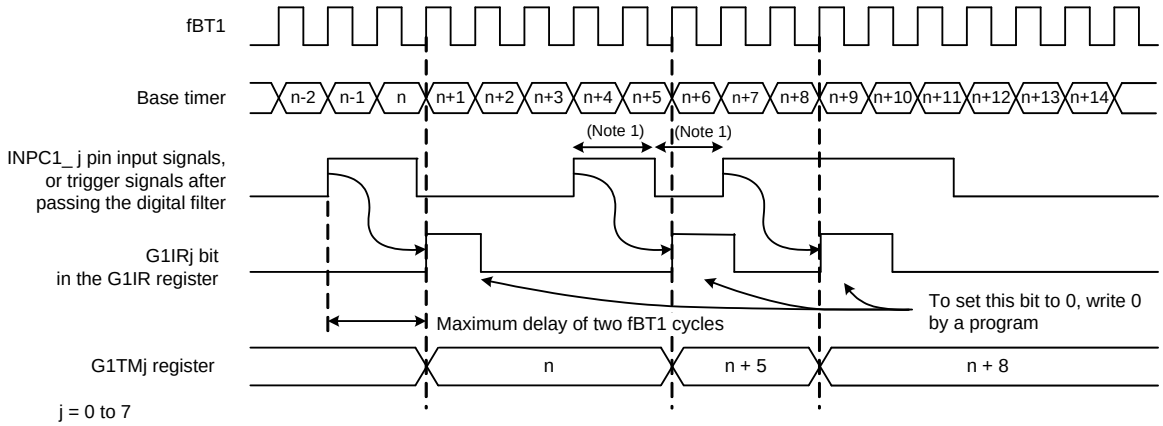


Figure 18.11 Time Measurement Function (1/2)

(1) The rising edge is selected as a time measurement trigger (bits CTS1 and CTS0 in the G1TMCRj register are 01b).

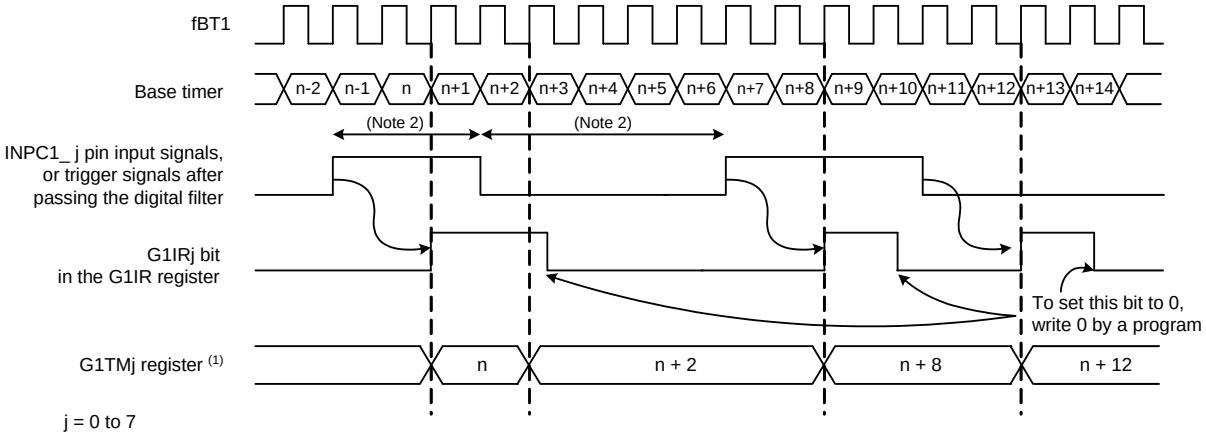


j = 0 to 7

Note:

1. Input pulse applied to the INPC1_ j pin requires at least 1.5 fBT1 cycles for both high and low widths.

(2) Both the rising and falling edges are selected as a time measurement trigger (bits CTS1 and CTS0 are 11b).

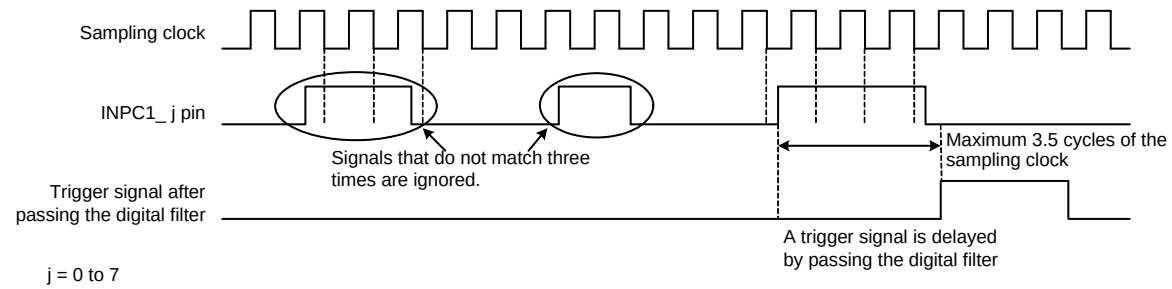


j = 0 to 7

Notes:

1. When the G1IRj bit is 1 and a trigger signal is generated, the IC/OC interrupt 0 and IC/OC interrupt 1 requests are not generated. However, values in the G1TMj register change.
2. Input pulse applied to the INPC1_j pin requires at least 2.5 fBT1 cycles for both the high and low widths.

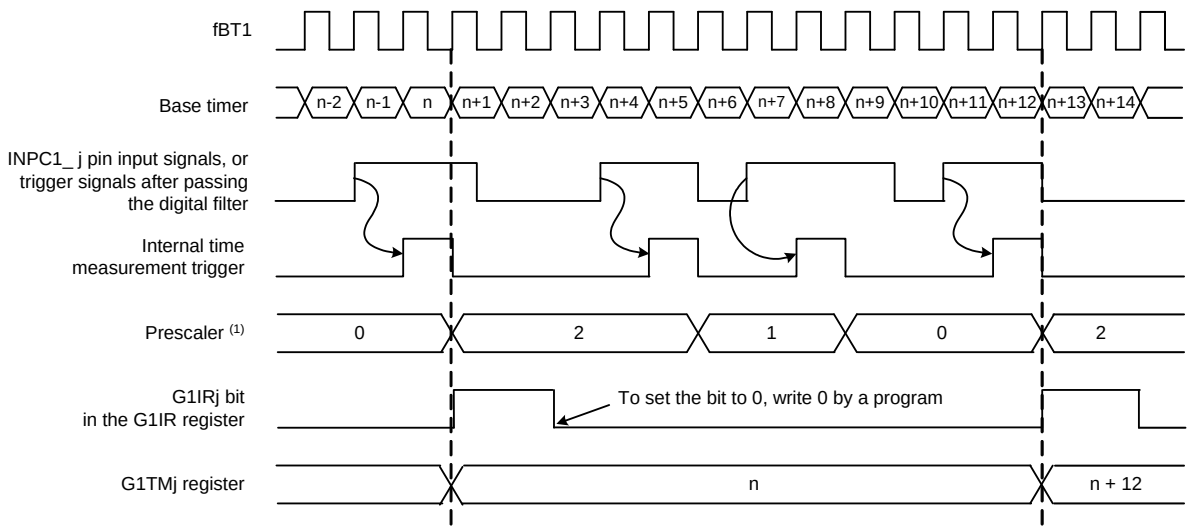
(3) Trigger signal when the digital filter function is used (bits DF1 and DF0 in the G1TMCRj register are 10b or 11b).



j = 0 to 7

Figure 18.12 Time Measurement Function (2/2)

(1) Example using the prescaler function (G1TPRj register is 02h and the PR bit in the G1TMCRj register is 1)

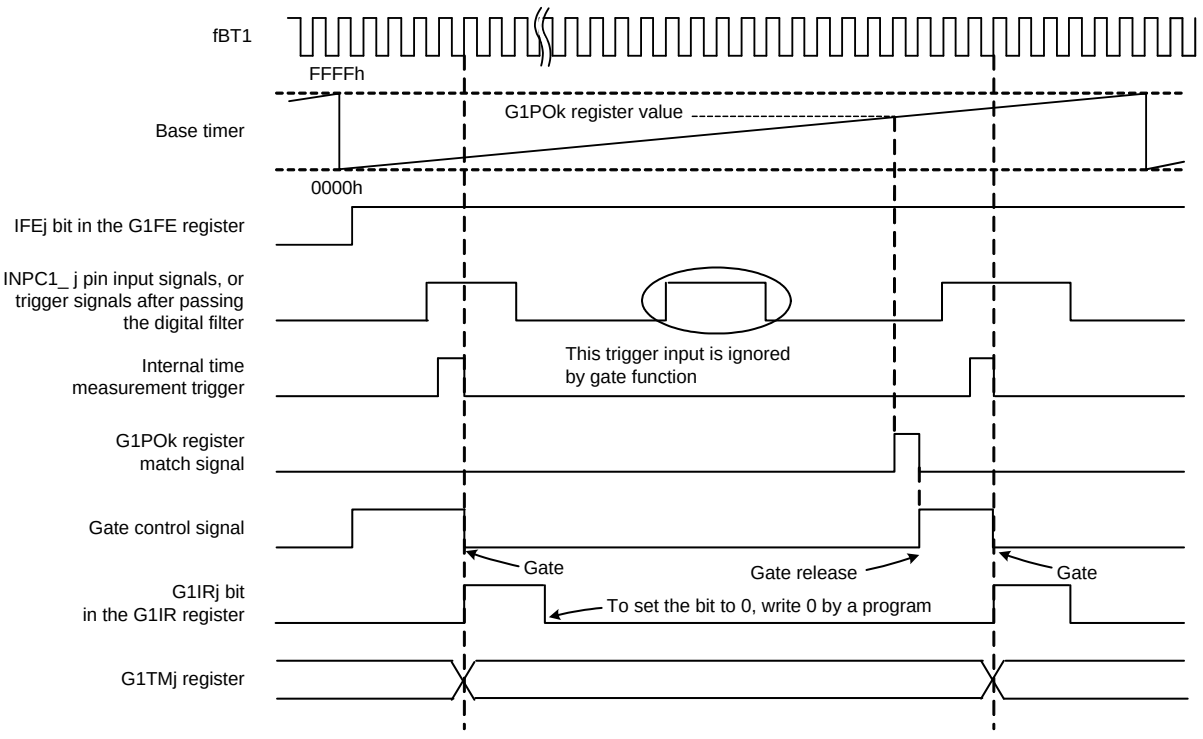


j = 6 and 7

Note:

1. This applies to the second or later prescaler cycle after the PR bit in the G1TMCRj register is set to 1 (prescaler function is used).

(2) Example using the gate function (bits GT and GOC in the G1TMCRj register are 1, and the gate function is disabled by matching with the G1POk register)



j = 6 and 7; k = j - 2

Figure 18.13 Prescaler and Gate Functions

18.3.2.1 Gate Function (Channel 6 and 7)

When the GT bit in the G1TMCRj register (j = 6 and 7) is 1 (gate function used), acceptance of trigger inputs is disabled after the time measurement by the first trigger input.

When 1 is written to the GSC bit in the G1TMCRj register, acceptance of trigger inputs becomes enabled again.

When the GOC bit in the G1TMCRj register is 1, acceptance of trigger inputs also becomes enabled again by matching the base timer with the G1POk register (k = j - 2).

"(2) Example using the gate function" in Figure 18.13 "Prescaler and Gate Functions" shows the operation example of this function.

18.3.3 Waveform Generation Function

A waveform is generated using the base timer value and the G1POj register value (j = 0 to 7). The waveform generation function has the following three modes:

- Single-phase waveform output mode
- Inverted waveform output mode
- Set/reset (SR) waveform output mode

In single-phase waveform output mode and inverted waveform output mode, compare match output is selectable.

In all three modes, each channel output can be temporarily disabled and used as a programmable I/O port when the waveform generation is in progress.

18.3.3.1 Single-Phase Waveform Output Mode

The OUTC1_j pin outputs high when the base timer value matches the G1POj register value (j = 0 to 7) and the INV bit in the G1POCRj register is 0 (output level is not inverted).
The OUTC1_j pin outputs low when the base timer reaches 0000h. When bits MOD1 and MOD0 in the G1POCRj register are 00b (single-phase waveform output mode), set bits UD1 and UD0 in the G1BCR register to 00b (increment). Table 18.12 lists the specifications of single-phase waveform output mode, Figure 18.14 to Figure 18.15 show operational examples in single-phase waveform output mode.

Table 18.12 Single-Phase Waveform Output Mode Specifications

Item	Specification
Output waveform	• Free-running operation (when bits RST2 and RST1 in the G1BCR1 register and the RST4 bit in the G1BCR0 register are all 0 (base timer is not reset)) Cycle: $\frac{65536}{fBT1}$ Initial output level width: $\frac{m}{fBT1}$ Inverted output level width: $\frac{65536 - m}{fBT1}$ • When the base timer matches either of following registers, the base timer is reset to 0000h. • G1PO0 register (when the RST1 bit is 1, and bits RST4 and RST2 are 0) • G1BTRR register (when the RST4 bit is 1, and bits RST2 and RST1 are 0) Cycle: $\frac{n + 2}{fBT1}$ Initial output level width: $\frac{m}{fBT1}$ Inverted output level width: $\frac{n + 2 - m}{fBT1}$ m: G1POj register setting value n: G1PO0 register or G1BTRR register setting value 0001h ≤ m < n ≤ FFFDh
Waveform output start condition	Set the IFEj bit in the G1FE register to 1 (channel j function enabled).
Waveform output stop condition	Set the IFEj bit to 0 (channel j function disabled).
Interrupt request occurrence timing	When the base timer value matches the G1POj register value.
OUTC1_ j pin	Pulse output or I/O port
Selectable functions	• Default value setting Select the starting waveform output level. • Output level inversion Output an inverted waveform from the OUTC1_j pin. • Compare match output When using the compare match output function, the output level is fixed to high or low from when the base timer value matches the G1POj register value. If the compare match output function is released, a single-phase waveform is output again when the base timer next matches the G1POj register. • Output disabled function When the EOCj bit in the G1OER register is 1 (output disabled), the OUTC1_j pin stops waveform output and becomes a programmable I/O port. When the EOCj bit is 0 (output enabled), the OUTC1_j pin outputs a single-phase waveform again.

j = 0 to 7

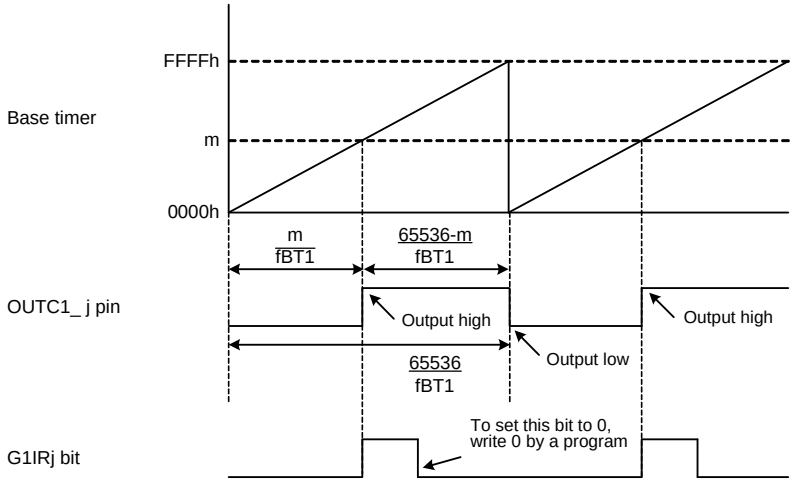
Table 18.13 Registers and Settings in Single-Phase Waveform Output Mode (1)

Register	Bit	Function
G1POj	—	Set the timing for an output level to become high. (2)
G1FS	FSCj	Set to 0 (waveform generation function selected).
G1FE	IFEj	Set to 1 (channel j function enabled).
G1POCRj	MOD1 and MOD0	Set to 00b.
	IVL	Select a default value of an output level.
	RLD	Select the reload timing for the G1POj register value.
	INV	Select whether an output level is inverted.
G1OER	EOCj	Set to 1 when the OUTC1_j output is disabled.
G1IOR0 G1IOR1	IOj1 and IOj0	Select an output level when compare results match.
G1BCR1	UD1 and UD0	Set to 00b.

j = 0 to 7, however, when the RST1 bit in the G1BCR1 register is 1 (the base timer is reset when the base timer and G1PO0 register values match), then j = 1 to 7.

Notes:
1. This table does not describe a procedure.
2. When the INV bit in the G1POCRj register is 0 (output level not inverted).

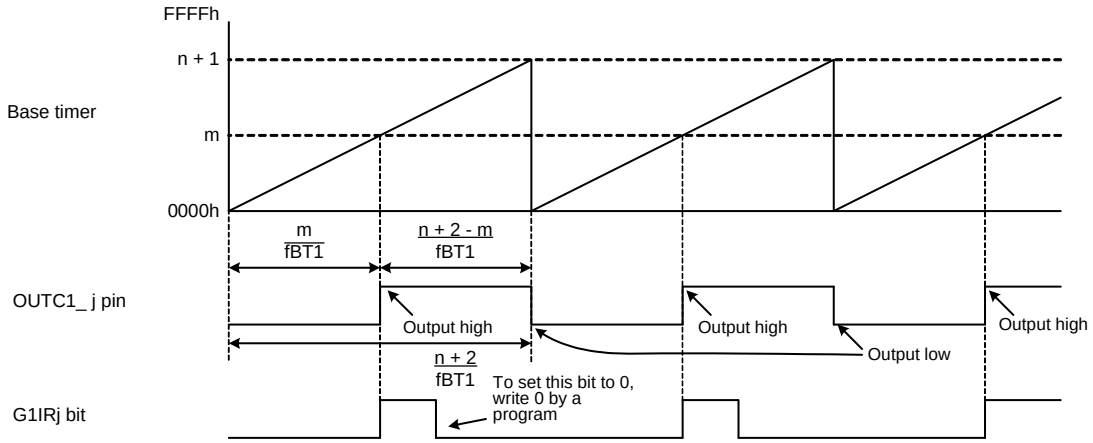
(1) Free-running operation (when bits RST2 and RST1 in the G1BCR1 register and the RST4 bit in the G1BCR0 register are all 0).



j = 0 to 7
m: G1POj register value
G1IRj: Bit in the G1IR register

The diagram above applies under the following conditions:
- The IVL bit in the G1POCRj register is 0 (output low as default) and the INV bit is 0 (output is not inverted).
- Bits IOj1 and IOj0 in registers G1IOR0 and G1IOR1 are 00b (outputs high or low depending on the mode selected by bits MOD1 and MOD0 in the G1POCRj register).
- The EOCj bit in the G1OER register is 0 (output enabled).

(2) When the base timer matches either of the following registers, the base timer is reset:
(a) G1PO0 register (when the RST1 bit is 1 and bits RST4 and RST2 are 0)
(b) G1BTRR register (when the RST4 bit is 1 and bits RST2 and RST1 are 0)

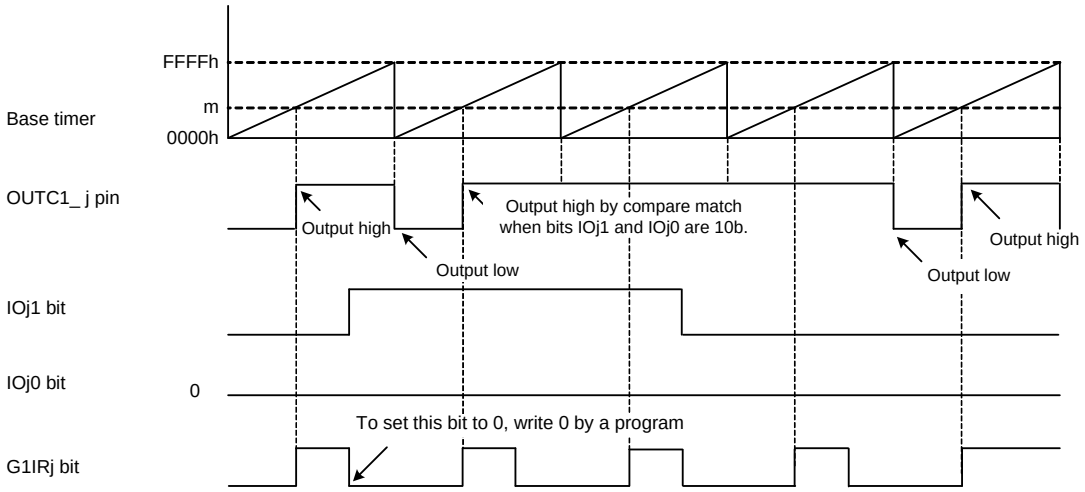


When (a), j = 1 to 7. When (b), j = 0 to 7.
m: G1POj register value
n: G1PO0 register or G1BTRR register setting value
G1IRj: Bit in the G1IR register

The above assumes the following:
- The IVL bit in the G1POCRj register is 0 (output low as default) and the INV bit is 0 (output is not inverted).
- Bits IOj1 and IOj0 in registers G1IOR0 and G1IOR1 are 00b (outputs high or low depending on the mode selected by bits MOD1 and MOD0 in the G1POCRj register).
- The EOCj bit in the G1OER register is 0 (output enabled).

Figure 18.14 Single-Phase Waveform Output Mode Operation (1/2)

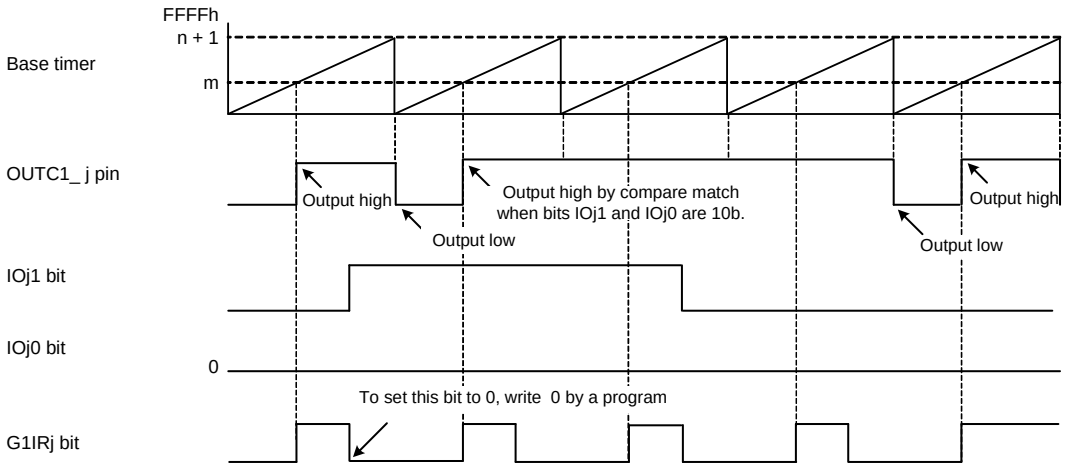
(3) Free-running operation (when bits RST2 and RST1 in the G1BCR1 register and the RST4 bit in the G1BCR0 register are all 0).



j = 0 to 7
m: G1POj register value
IOj1 and IOj0: Bits in registers G1IOR1 and G1IOR0
G1IRj: Bit in the G1IR register

The above assumes the following:
· IVL bit in the G1POCRj register is 0 (output low as default) and the INV bit is 0 (output is not inverted).
· EOCj bit in the G1OER register is 0 (output enabled).

(4) When the base timer matches either of following registers, the base timer is reset:
(a) G1PO0 register (when the RST1 bit is 1 and bits RST4 and RST2 are 0)
(b) G1BTRR register (when the RST4 bit is 1 and bits RST2 and RST1 are 0)



When (a), j = 1 to 7. When (b), j = 0 to 7.
m: G1POj register value
n: G1PO0 register or G1BTRR register setting value
G1IRj: Bit in the G1IR register

The above assumes the following:
· The IVL bit in the G1POCRj register is 0 (output low as default) and the INV bit is 0 (output is not inverted).
· The EOCj bit in the G1OER register is 0 (output enabled).

Figure 18.15 Single-Phase Waveform Output Mode Operation (2/2)

18.3.3.2 Inverted Waveform Output Mode

The output level at the OUTC1_j pin is inverted every time the base timer value matches the G1POj register value (j = 0 to 7). When bits MOD1 and MOD0 in the G1POCRj register are 10b (inverted waveform output mode), set bits UD1 and UD0 in the G1BCR1 register to 00b (increment) or 01b (increment/decrement).

Table 18.14 lists the specifications of inverted waveform output mode. Figure 18.16 and Figure 18.17 show the operational examples of inverted waveform output mode.

Table 18.14 Inverted Waveform Output Mode Specifications

Item	Specification
Output waveform	• Free-running operation (when bits RST2 and RST1 in the G1BCR1 register and the RST4 bit in the G1BCR0 register are all 0 (the base timer is not reset)) Cycle: $\frac{65536 \times 2}{fBT1}$ High or low width: $\frac{65536}{fBT1}$ • When the base timer matches either of the following registers, the base timer is set to 0000h: • G1PO0 register (when the RST1 bit is 1, and bits RST4 and RST2 are 0) • G1BTRR register (when the RST4 bit is 1, and bits RST2 and RST1 are 0) Cycle: $\frac{2(n+2)}{fBT1}$ High or low width: $\frac{n+2}{fBT1}$ m: G1POj register setting value n: G1PO0 register or G1BTRR register setting value 0000h ≤ m < n ≤ FFFDh
Waveform output start condition	Set the IFEj bit in the G1FE register to 1 (channel j function enabled).
Waveform output stop condition	Set the IFEj bit to 0 (channel j function disabled).
Interrupt request occurrence timing	When the base timer value matches the G1POj register value.
OUTC1_j pin	Pulse output or I/O port
Selectable functions	• Default value setting Select the starting waveform output level. • Output level inversion Select if the waveform level output from the OUTC1_j pin is inverted. • Compare match output function When the compare match output function is set, the output level is fixed to high or low from when the base timer value matches the G1POj register value. When the compare match output function is disabled, an inverted waveform is output again from the next compare match timing. • Output disabled function When the EOCj bit in the G1OER register is 1 (output disabled), the OUTC1_j pin stops waveform output and becomes a programmable I/O port. When the EOCj bit is 0 (output enabled), the OUTC1_j pin outputs inverted waveform again.

j = 0 to 7

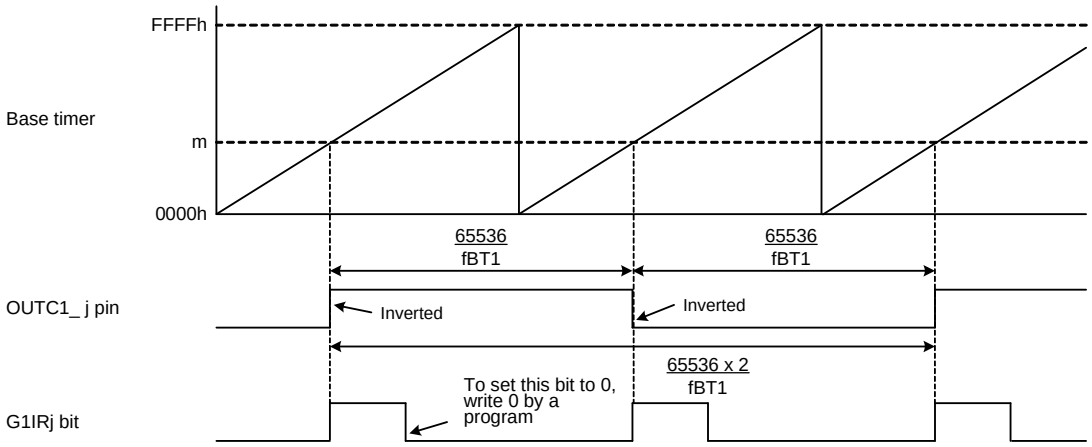
Table 18.15 Registers and Settings in Inverted Waveform Output Mode (1)

Register	Bit	Function
G1POj	—	Set the timing for the waveform to be inverted.
G1FS	FSCj	Set to 0 (waveform generation function selected).
G1FE	IFEj	Set to 1 (channel j function enabled).
G1POCRj	MOD1 and MOD0	Set to 10b.
	IVL	Select a default value of an output level.
	RLD	Select the reload timing for the G1POj register value.
	INV	Select whether an output level is inverted.
G1OER	EOCj	Set to 1 when the OUTC1_j output is disabled.
G1IOR0 G1IOR1	IOj1 and IOj0	Select an output level when compare results match.
G1BCR1	UD1 and UD0	Set to 00b or 01b.

j = 0 to 7, however, when the RST1 bit in the G1BCR1 register is 1 (the base timer is reset when the base timer and G1PO0 register values match), then j = 1 to 7.

Note:
1. This table does not describe a procedure.

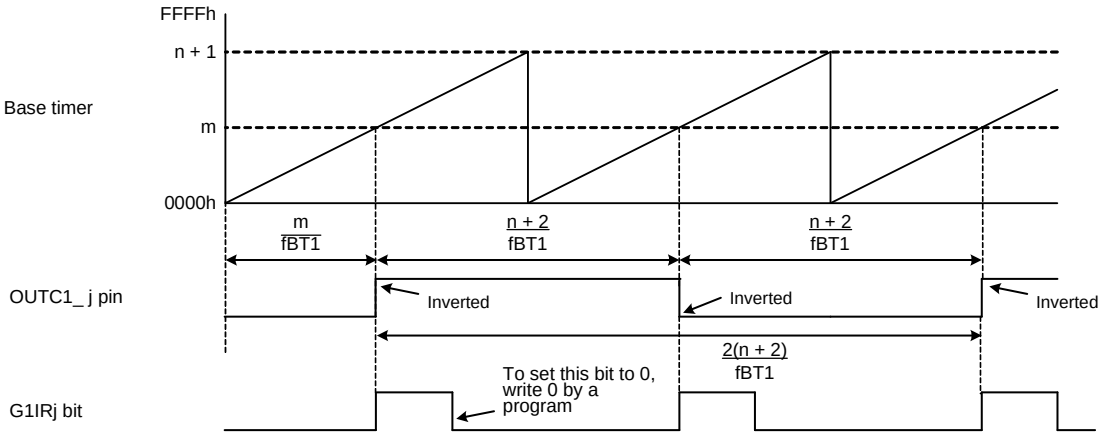
(1) Free-running operation (when bits RST2 and RST1 in the G1BCR1 register and the RST4 bit in the G1BCR0 register are all 0)



j = 0 to 7
m: G1POj register value
G1IRj: Bit in the G1IR register

The above assumes the following:
- The IVL bit in the G1POCRj register is 0 (output low as default) and the INV bit is 0 (output is not inverted).
- Bits UD1 and UD0 in the G1BCR1 register are 00b (increment).
- Bits IOj1 and IOj0 in registers G1IOR0 and G1IOR1 are 00b (outputs high or low depending on the mode selected by bits MOD1 and MOD0 in the G1POCRj register).
- The EOCj bit in the G1OER register is 0 (output enabled).

(2) When the base timer matches either of following registers, the base timer is reset:
(a) G1PO0 register (when the RST1 bit is 1 and bits RST4 and RST2 are 0)
(b) G1BTRR register (when the RST4 bit is 1 and bits RST2 and RST1 are 0)

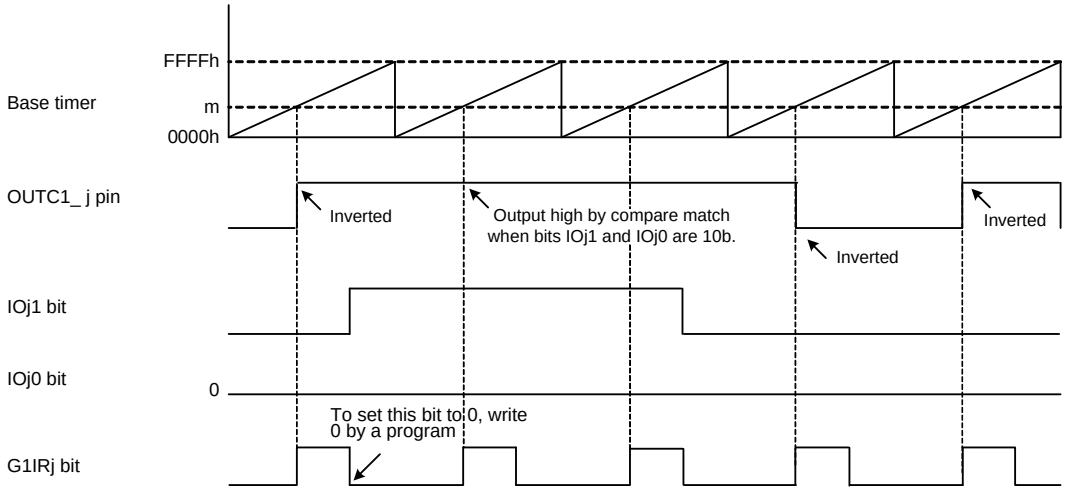


When (a), j = 1 to 7. When (b), j = 0 to 7.
m: G1POj register value
n: G1PO0 register or G1BTRR register value
G1IRj: Bit in the G1IR register

The above assumes the following:
- The IVL bit in the G1POCRj register is 0 (output low as default) and the INV bit is 0 (output is not inverted).
- Bits UD1 and UD0 in the G1BCR1 register are 00b (increment).
- Bits IOj1 and IOj0 in registers G1IOR0 and G1IOR1 are 00b (outputs high or low depending on the mode selected by bits MOD1 and MOD0 in the G1POCRj register).
- The EOCj bit in the G1OER register is 0 (output enabled).

Figure 18.16 Inverted Waveform Output Mode Operation (1/2)

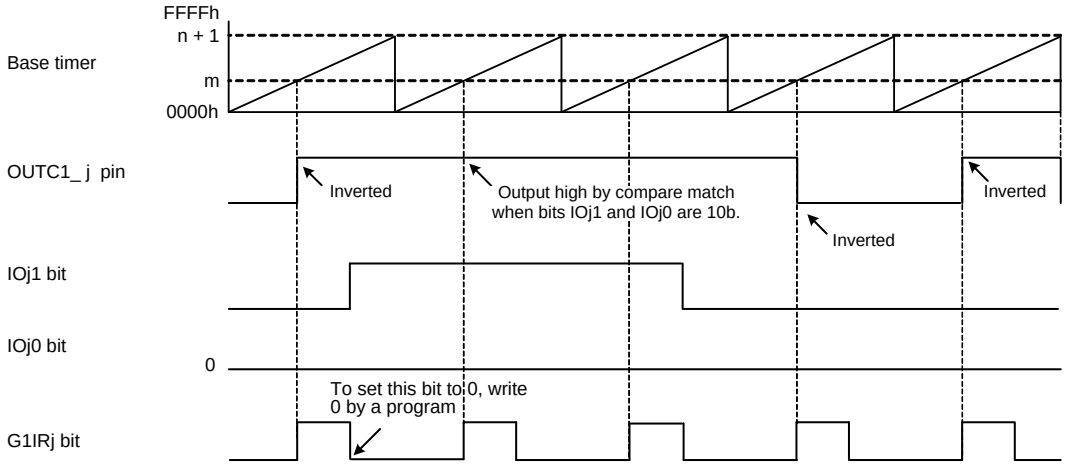
(3) Free-running operation (when bits RST2 and RST1 in the G1BCR1 register and the RST4 bit in the G1BCR0 register are all 0):



j = 0 to 7
m: G1POj register value
IOj1 and IOj0: Bits in registers G1IOR1 and G1IOR0
G1IRj: Bit in the G1IR register

The above assumes the following:
- The IVL bit in the G1POCRj register is 0 (Output low as default) and the INV bit is 0 (output is not inverted).
- Bits UD1 and UD0 in the G1BCR1 register are 00b (increment).
- The EOCj bit in the G1OER register is 0 (output enabled).

(4) When the base timer matches either of following registers, the base timer is reset:
(a) G1PO0 register (when the RST1 bit is 1 and bits RST4 and RST2 are 0)
(b) G1BTRR register (when the RST4 bit is 1 and bits RST2 and RST1 are 0)



When (a), j = 1 to 7. When (b), j = 0 to 7.
m: G1POj register value, n: G1PO0 register or G1BTRR register value
IOj1 and IOj0: Bits in registers G1IOR1 and G1IOR0
G1IRj: Bit in the G1IR register

The above assumes the following:
- The IVL bit in the G1POCRj register is 0 (output low as default) and the INV bit is 0 (output is not inverted).
- Bits UD1 and UD0 in the G1BCR1 register are 00b (increment).
- The EOCj bit in the G1OER register is 0 (output enabled).

Figure 18.17 Inverted Waveform Output Mode Operation (2/2)

18.3.3.3 Set/Reset Waveform Output Mode (SR Waveform Output Mode)

The OUTC1_j pin outputs high when the INV bit in the G1POCRj register (j = 0, 2, 4, 6) is 0 (output level is not inverted) and the base timer value matches the G1POj register value. When the base timer value matches the G1POk register value (k = j + 1), the OUTC1_j pin outputs low.

When bits MOD1 and MOD0 in registers G1POCRj and G1POCRk are 01b (SR waveform output mode), set bits UD1 and UD0 in the G1BCR register to 00b (increment).

Table 18.16 lists the specifications of SR waveform output mode and Figure 18.18 shows the operational example of SR waveform output mode.

Table 18.16 SR Waveform Output Mode Specifications

Item	Specification
Output waveform	• Free-running operation (when bits RST2 and RST1 in the G1BCR1 register and the RST4 bit in the G1BCR0 register are all 0 (the base timer is not reset)) Cycle: $\frac{65536}{fBT1}$ Inverted output level width: $\frac{n-m}{fBT1}$ • When the base timer matches either of following registers, the base timer is reset to 0000h: • G1PO0 register (when the RST1 bit is 1, and bits RST4 and RST2 are 0) (1) • G1BTRR register (when the RST4 bit is 1, and bits RST2 and RST1 are 0) Cycle: $\frac{p+2}{fBT1}$ Inverted output level width: $\frac{n-m}{fBT1}$ m: G1POj register setting value n: G1POk register setting value p: G1PO0 register or G1BTRR register value 0000h ≤ m < n < p ≤ FFFDh
Waveform output start condition	Set bits IFEj and IFEk in the G1FE register to 1 (channel j function enabled).
Waveform output stop condition	Set bits IFEj and IFEk to 0 (channel j function disabled).
Interrupt request occurrence timing	• Channel j When the base timer value matches the G1POj register value. • Channel k When the base timer value matches the G1POk register value.
OUTC1_ j pin	Pulse output or I/O port
Selectable functions	• Default value setting Select the starting waveform output level. • Output level inversion Select if the waveform level output from the OUTC1_j pin is inverted. • Output disabled When the EOCj bit in the G1OER register is 1 (output disabled), the OUTC1_j pin stops waveform output and becomes a programmable I/O port. When the EOCj bit is 0 (output enabled), the OUTC1_j pin outputs SR waveform again.

j = 0, 2, 4, 6; k = j + 1

Note:

1. When the RST1 bit in the G1BCR1 register is 1 (the base timer is reset by the G1PO0 register), SR waveform output mode is disabled for channels 0 and 1.

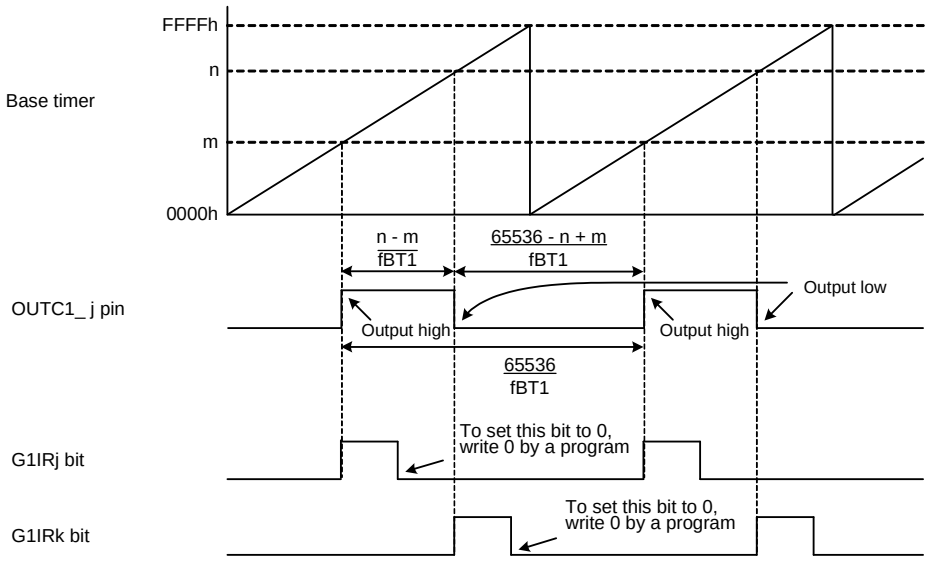
Table 18.17 Registers and Settings in SR Waveform Output Mode (1)

Register	Bit	Function	
		Even channel (channel j)	Odd channel (channel k)
G1POj	—	Set the timing for an output level to become high. (2)	Set the timing for an output level to become low. (2)
G1FS	FSCj	Set to 0 (waveform generation function selected).	Set to 0 (waveform generation function selected).
G1FE	IFEj	Set to 1 (channel j function enabled).	Set to 1 (channel k function enabled).
G1POCRj	MOD1 and MOD0	Set to 01b.	Set to 01b.
	IVL	Select a default value of an output level.	— (invalid)
	RLD	Select the reload timing for the G1POj register value.	Select the reload timing for the G1POk register value.
	INV	Select whether an output level is inverted.	— (invalid)
G1OER	EOCj	Set to 1 when the OUTC1_j is disabled.	Set to 1.
G1IOR0 G1IOR1	IOj1 and IOj0	Set to 00b.	Set to 00b.
G1BCR1	UD1 and UD0	Set to 00b.	

j = 0, 2, 4, 6; k = j + 1, however, when the RST1 bit in the G1BCR1 register is 1 (the base timer is reset when the base timer and G1PO0 register values match), then j = 2, 4, 6.

Notes:
1. This table does not describe a procedure.
2. When the INV bit in the G1POCRj register is 0 (output level not inverted).

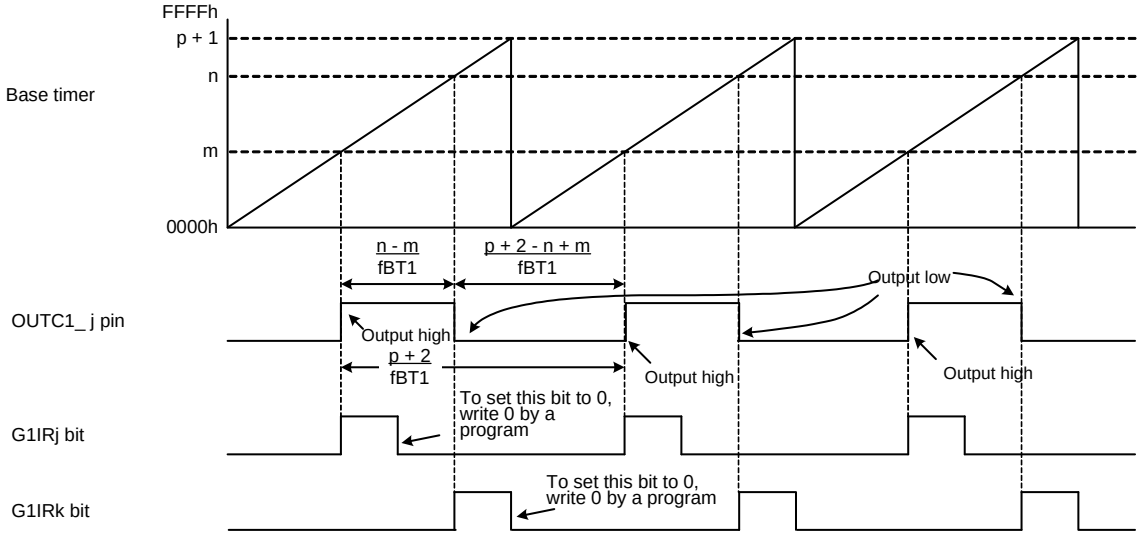
(1) Free-running operation (when bits RST2 and RST1 in the G1BCR1 register and the RST4 bit in the G1BCR0 register are all 0)



j = 0, 2, 4, 6; k = j + 1
m: G1POj register value
n: G1POk register value
G1IRj and G1IRk: Bits in the G1IR register

The above assumes the following:
· The IVL bit in the G1POCRj register is 0 (output low as default) and the INV bit is 0 (output is not inverted).
· The EOCj bit in the G1OER register is 0 (output enabled).

(2) When the base timer matches either of following registers, the base timer is reset:
(a) G1PO0 register (when the RST1 bit is 1 and bits RST4 and RST2 are 0)
(b) G1BTRR register (when the RST4 bit is 1 and bits RST2 and RST1 are 0)



When (a), j = 2, 4, 6. When (b), j = 0, 2, 4, 6.
k = j + 1
m: G1POj register value
p: Either G1PO0 or G1BTRR register value
G1IRj and G1IRk: Bits in the G1IR register

The above assumes the following:
· The IVL bit in the G1POCRj register is 0 (output low as default) and the INV bit is 0 (output is not inverted).
· The EOCj bit in the G1OER register is 0 (output enabled).

Figure 18.18 Operation Example in SR Waveform Output Mode

18.3.4 I/O Port Select Function

The I/O direction of IC/OC pins is determined by registers G1FE, G1FS, and G1OER.
In SR waveform output mode, an even channel and an odd channel are used for each output waveform, but a waveform is output only from the even channel. In this case, the corresponding pin for the odd channel can be used as an I/O port.

Table 18.18 Pin Settings for Time Measurement and Waveform Generation

Pin	Pin Settings				Pin Function
	IFE	FSC	MOD1 and MOD0	EOC	
P2_j/ INPC1_j/ OUTC1_j	0	—	—	—	P2_j used as I/O port
	1	1	—	—	INPC1_j (1)
	1	0	00b	0	Single-phase waveform output from OUTC1_j
	1	0	00b	1	P2_j used as I/O port
	1	0	01b	0	SR waveform output from OUTC1_j
	1	0	01b	1	P2_j used as I/O port
	1	0	10b	0	Inverted waveform output from OUTC1_j
	1	0	10b	1	P2_j used as I/O port

j = 0 to 7
—: 0 or 1
IFE: IFEj bit in the G1FE register
FSC: FSCj bit in the G1FS register
MOD1 and MOD0: Bits in the G1POCRj register
EOC: EOCj bit in the G1OER register

Note:
1. Set the port direction bits sharing pins to 0 (input mode).

The P2_7/OUTC1_7/INPC1_7 pin or P1_7/INPC1_7 pin can be selected as a time measurement pin for IC/OC channel 7 by the CH7INSEL bit in the G1BCR0 register (channel 7 input select bit).

The digital debounce filter for noise reduction can be used with an input to the INP1_7 pin from the P1_7/INP1_7 pin. Refer to 11.4.3 “Digital Debounce Filters” for details.

18.4 Interrupts

Refer to each operation example for interrupt request occurrence timings.

Refer to 12.7 “Interrupt Control” for details on interrupt control. Table 18.19 lists Timer S Interrupt Associated Registers.

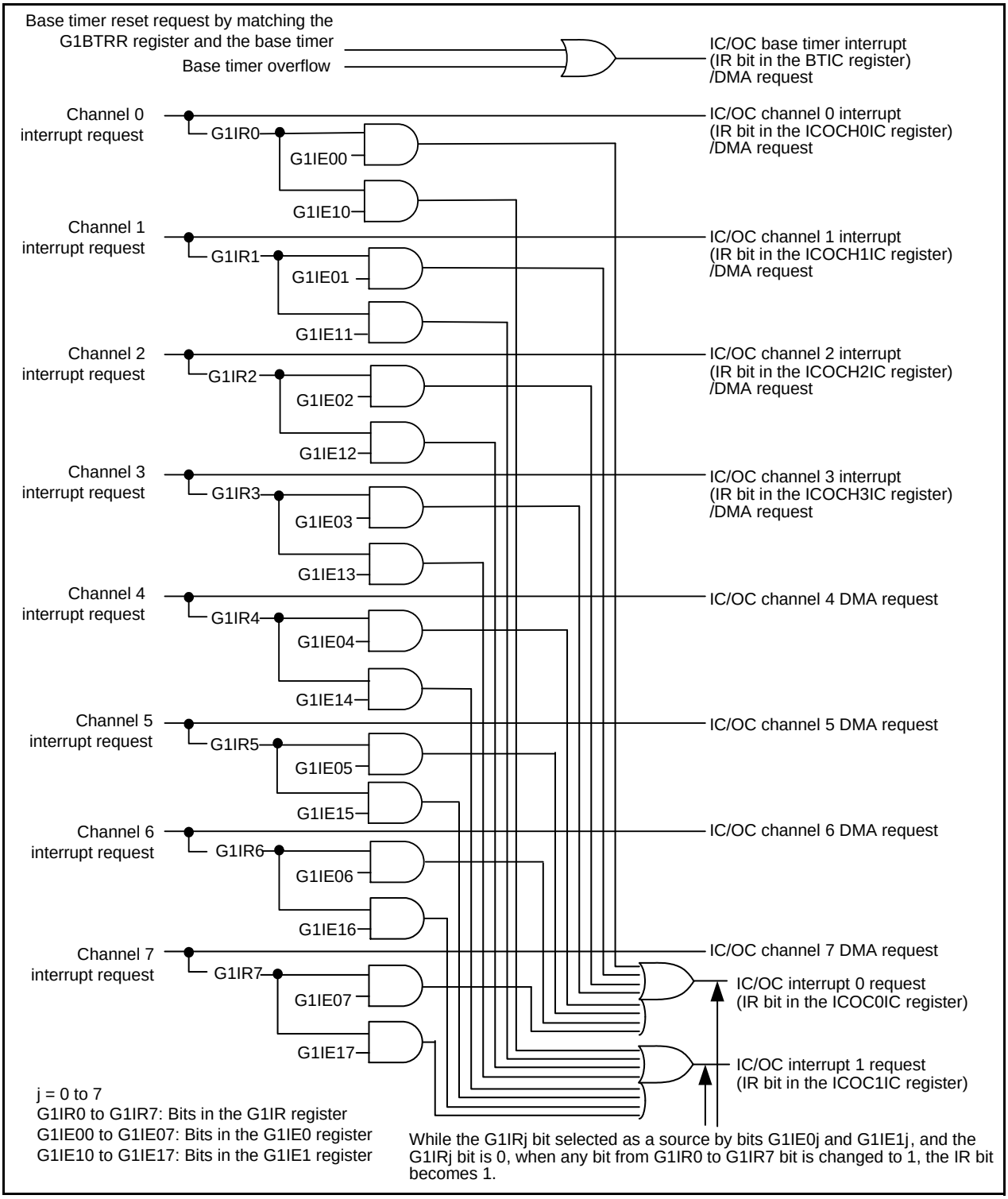


Figure 18.19 Timer S Interrupt and DMA Requests

Table 18.19 Timer S Interrupt Associated Registers

Address	Register	Symbol	Reset Value
0079h	IC/OC Interrupt 0 Control Register	ICOC0IC	XXXX X000b
007Ah	IC/OC Channel 0 Interrupt Control Register	ICOCH0IC	XXXX X000b
007Bh	IC/OC Interrupt 1 Control Register	ICOC1IC	XXXX X000b
007Ch	IC/OC Channel 1 Interrupt Control Register	ICOCH1IC	XXXX X000b
007Dh	IC/OC Channel 2 Interrupt Control Register	ICOCH2IC	XXXX X000b
007Eh	IC/OC Channel 3 Interrupt Control Register	ICOCH3IC	XXXX X000b
007Fh	IC/OC Base Timer Interrupt Control Register	BTIC	XXXX X000b

18.4.1 IC/OC Base Timer Interrupt

When the base timer reset request by matching the G1BTRR register and the base timer, or the base timer overflow is generated, the IR bit in the BTIC register becomes 1 (interrupt requested).

18.4.2 IC/OC Channel 0 Interrupt to IC/OC Channel 3 Interrupt

When interrupt requests for channels 0 to 3 are generated, the corresponding IR bit in registers ICOCH0IC to ICOCH3IC becomes 1 (interrupt requested).

18.4.3 IC/OC Interrupt 0 and IC/OC Interrupt 1

An interrupt request for IC/OC interrupt i (i = 0, 1) is generated in combination with the channel j interrupt request (j = 0 to 7). When the G1IEij bit in the G1IEi register is set to 1 (IC/OC interrupt i request enabled), the interrupt request for channel j becomes the IC/OC interrupt i source.

When the channel j interrupt request is generated, the G1IRj bit in the G1IR register becomes 1 (interrupt requested). While bits in the G1IR register corresponding to the channels selected as sources with the G1IEi register are all 0 (interrupt not requested), when any bit in the G1IR register becomes 1, the IR bit in the ICOCiIC register becomes 1 (interrupt requested).

The IR bit in the ICOCiIC register becomes 0 automatically when an interrupt request is received (interrupt not requested). However, the G1IRj bit does not become 0 automatically with an interrupt request reception. Thus, set the G1IRj bit to 0 by a program. If the G1IRj bit remains 1 when the IR bit is 0, the IR bit in the ICOCiIC register does not become 1 anymore. This means the IC/OC interrupt i request is no longer generated.

18.5 Notes on Timer S

18.5.1 Register Access

The explanation for some bits and registers states, “the value written to this register or this bit is reflected to the internal circuit when the clock is synchronized with the base timer count source (fBT1)”. When writing these bits or registers, the written value is not reflected to the internal circuits immediately. After writing the value, prewrite operations are performed for up to one fBT1 cycle. When reading these bits or registers immediately after writing the value, the value before writing may be read.

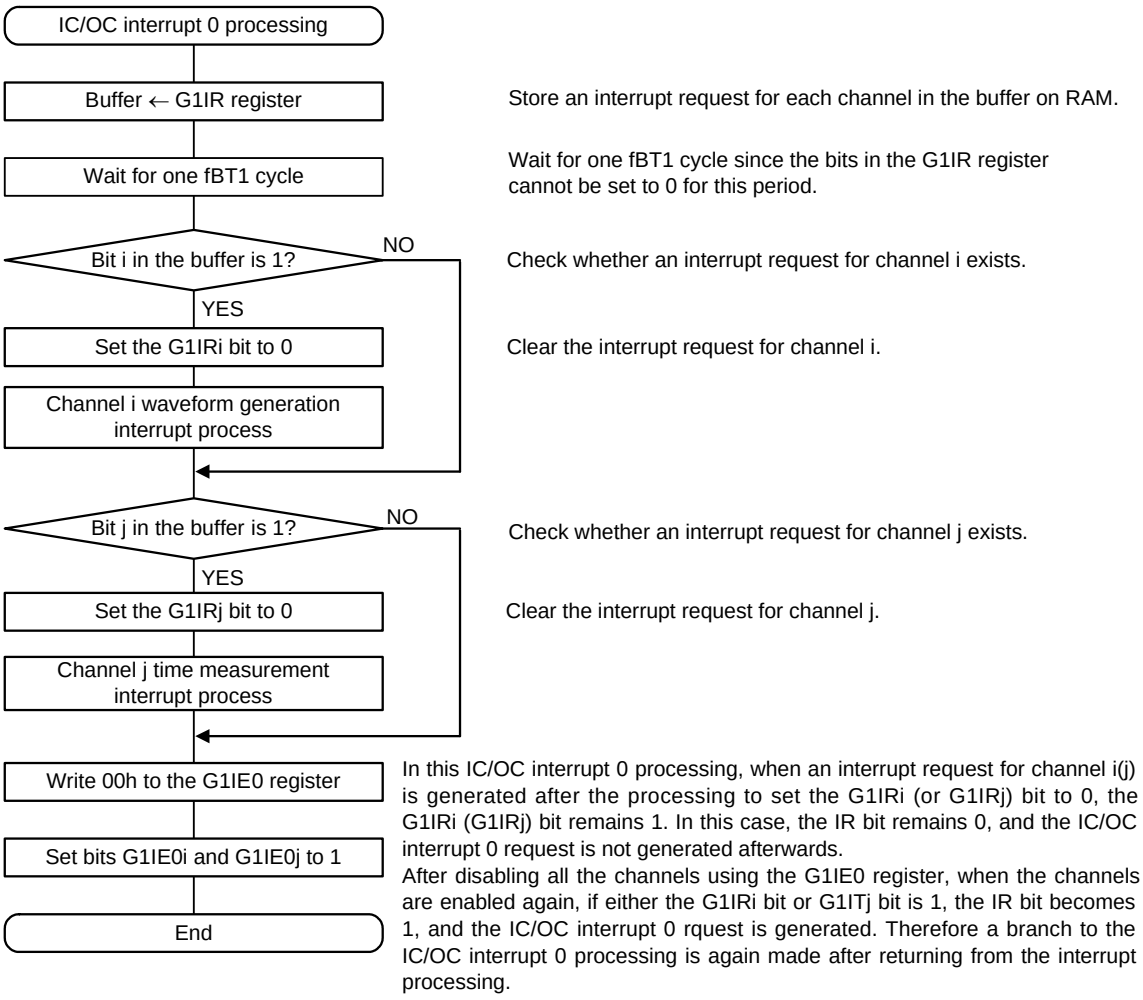
18.5.2 Changing the G1IR Register

Set the G1IRj bit in the G1IR register (j = 0 to 7) to 0 by a program since it does not become 0 automatically with an interrupt request reception.

However, the G1IRj bit cannot be set to 0 for one fBT1 cycle after this bit becomes 1. Wait for one or more fBT1 cycles after the G1IRj bit becomes 1, then set this bit to 0.

To write 0 to the G1IRj bit, use the AND and BCLR instructions to avoid deleting requests for other channels.

Figure 18.20 shows “IC/OC Interrupt 0 Operation Example”. As shown in the operation example, disable interrupt requests for all channels once at the last part of an interrupt process, then enable them again.



i = 0 to 7; j = 0 to 7 (however, j and i cannot be the same value)
G1IRi, G1IRj: Bits in the G1IR register
G1IE0i, G1IE0j: Bits in the G1IE0 register

The above assumes the following:
With IC/OC interrupt 0, a waveform generation interrupt is processed for channel i, and a time measurement interrupt for channel j.
Interrupt requests for the other channels are disabled with the G1IE0 register.

Figure 18.20 IC/OC Interrupt 0 Operation Example

18.5.3 Changing Registers ICOCiIC (i = 0, 1)

While the G1IEij bit in the G1IEi register is 1 (IC/OC interrupt 1 request enabled), use the AND, OR, BCLR, or BSET instruction to change bits ILVL2 to ILVL0 in the ICOCiIC register at the point where a channel j interrupt request may be generated (j = 0 to 7). The IR bit becomes 1 (interrupt requested) if a channel j interrupt is generated while executing these instructions.
If the MOV instruction is used to perform the above, when a channel j interrupt request is generated while executing the MOV instruction, the IR bit does not become 1, and the interrupt request is ignored. The G1IRj bit in the G1IR register becomes 1 (interrupt requested) at this timing. If the G1IRj remains 1, subsequent IC/OC interrupt i requests are not generated.

When timer S is initialized, change registers ICOCiIC after registers ICOCiIC and G1IR are both set to 00h.

18.5.4 Output Waveform During the Base Timer Reset with the BTS bit

When the BTS bit in the G1BCR1 register is set to 0 (base timer reset), the waveform output pin level remains as it is at that point. This output level is held until the base timer value matches the G1POj register value after the BTS bit is set to 1 (base timer starts counting).

18.5.5 OUTC1_0 Pin Output During the Base Timer Reset with the G1PO0 register

While the RST1 bit in the G1BCR1 register is set to 1 (the base timer is reset when the base timer matches the G1PO0 register), when the base timer matches the G1PO0 register, the base timer is reset after two fBT1 cycles. During the two fBT1 cycles from when the base timer value matches the G1PO0 register value to the base timer being reset, the OUTC1_0 pin is driven high. Thus set the EOC0 bit in the G1OER register to 1 (output disabled).

18.5.6 Interrupt Request When Selecting Time Measurement Function

When the FSCj bit (j = 0 to 7) in the G1FS register is set to 1, and the IFEj bit in the G1FE register is also set to 1, the G1IRj bit in the G1IR register, or the IR bits in registers ICOCiIC (i = 0, 1) or ICOCHjIC (j = 0 to 3) may become 1 (interrupt requested) after a maximum of two fBT1 cycles.
When using IC/OC interrupt i or IC/OC channel j interrupt, set bits FSCj and IFEj to 1, then perform the following:

(1) Wait for two or more fBT1 cycles.
(2) Set the IR bit in the ICOCiIC register and/or the ICOCHjIC register to 0.
(3) Wait for three or more fBT1 cycles after the time measurement function is selected. Set the G1IR register to 00h after setting the IR bit in the ICOCiIC register to 0.

19. Task Monitor Timer

19.1 Introduction

The task monitor timer has one 16-bit timer to count internal count sources. The TMOSPR register (task monitor timer protect register) has the ability to protect other task monitor timer associated registers.

Table 19.1 Task Monitor Timer Specifications

Item	Specification
Count sources	f1, f1 divided-by-8, f1 divided-by-32, f1 divided-by-128
Count operations	• Decrement • Reloads the value in the reload register and continues counting when the timer underflows.
Counter cycle	(n+1)/fj n: TMOS register setting 0000h to FFFFh, fj: count source frequency
Count start condition	Set the TMOS0S bit in the TMOSSR register to 1 (start counting)
Count stop condition	Set the TMOS0S bit to 0 (stop counting)
Interrupt request generation timing	At timer underflow
Read from timer	The timer's count value is read by reading the TMOS register
Write to task monitor timer	• When the value is written to the TMOS register while the task monitor timer counter stops, the value is written to both the reload register and the counter. • When the value is written to the TMOS register while the task monitor timer is counting (after setting the TMOS0S bit in the TMOSSR register to 1 (start counting)), the value is written to the reload register and transferred at the next reload timing.

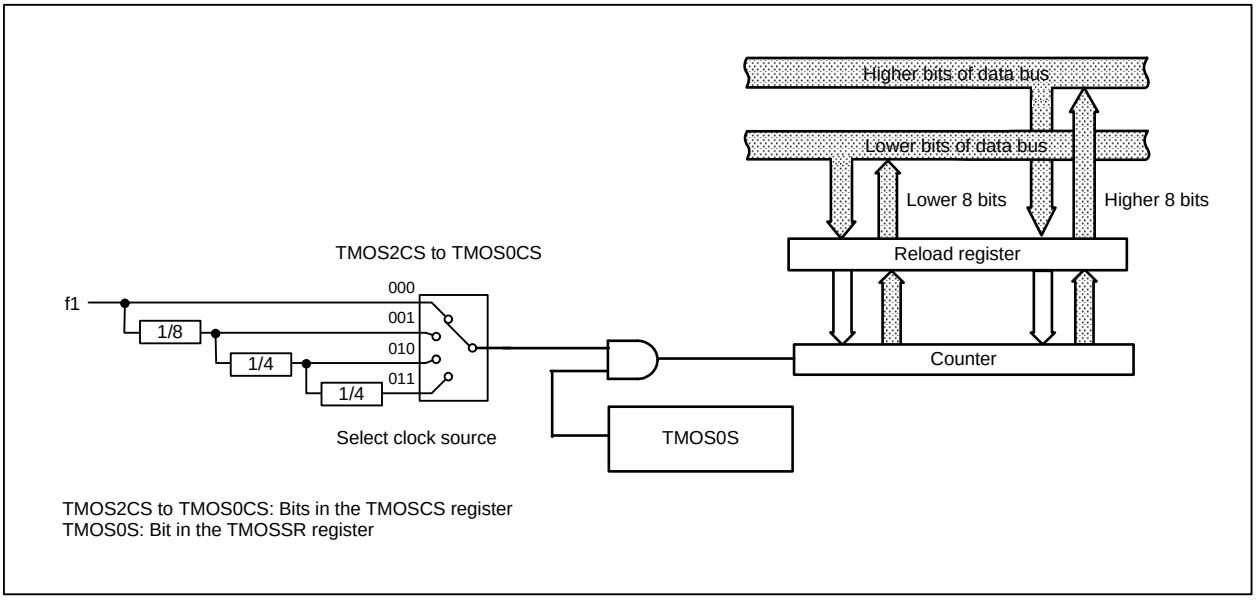


Figure 19.1 Task Monitor Timer Block Diagram

19.2 Registers

Table 19.2 Registers

Address	Register Name	Register symbol	Reset Value
01F0h	Task Monitor Timer Register	TMOS	XXh
01F1h			XXh
01F2h	Task Monitor Timer Count Start Flag	TMOSSR	XXXX XXX0b
01F3h	Task Monitor Timer Count Source Select Register	TMOSCS	XXXX 0000b
01F4h	Task Monitor Timer Protect Register	TMOSPR	00h

19.2.1 Task Monitor Timer Register (TMOS)

Task Monitor Timer Register

(b15) (b8) b7 b0 b7 b0

Symbol: TMOS

Address: 01F1h, 01F0h

Reset Value: Undefined

Function	Setting Range	RW
When setting range is n, the counter frequency: (n + 1)/fj	0000h to FFFFh	RW

fj: count source frequency

Access the TMOS register in 16-bit units.

19.2.2 Task Monitor Timer Count Start Flag (TMOSSR)

Task Monitor Timer Count Start Flag

b7 b6 b5 b4 b3 b2 b1 b0

Symbol: TMOSSR

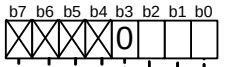
Address: 01F2h

Reset Value: XXXX XXX0b

Bit Symbol	Bit Name	Function	RW
TMOS0S	Task monitor timer count start flag	0: Stop counting 1: Start counting	RW
— (b7-b1)	No register bits. If necessary, set to 0. The read value is undefined.		—

19.2.3 Task Monitor Timer Count Source Select Register (TMOSCS)

Task Monitor Timer Count Source Select Register

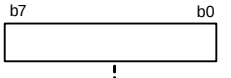


Symbol	Address	Reset Value
TMOSCS	01F3h	XXXX 0000b

Bit Symbol	Bit Name	Function	RW
TMOS0CS TMOS1CS TMOS2CS	Task monitor timer count source select bit	b2 b1 b0 0 0 0: f1 0 0 1: f1 divided by 8 0 1 0: f1 divided by 32 0 1 1: f1 divided by 128 Do not set other than the above.	RW
— (b3)	Reserved	Set to 0.	RW
— (b7-b4)	No register bits. If necessary, set to 0. The read value is undefined.		—

19.2.4 Task Monitor Timer Protect Register (TMOSPR)

Task Monitor Timer Protect Register



Symbol	Address	Reset Value
TMOSPR	01F4h	00h

Function	RW
When the setting value is 55h, registers TMOS, TMOSSR, and TMOSCS are writable. Registers TMOS, TMOSSR, and TMOSCS are readable regardless of the TMOSPR register settings.	RW

When changing the TMOS, TMOSSR, or TMOSCS register, follow the steps below:

(1) Write 55h (write enabled) to the TMOSPR register.
(2) Write a value to the TMOS, TMOSSR, or TMOSCS register as required.
(3) Write a value other than 55h to the TMOSPR register (write disabled)

19.3 Operation

Figure 19.2 shows the Task Monitor Timer Operation.

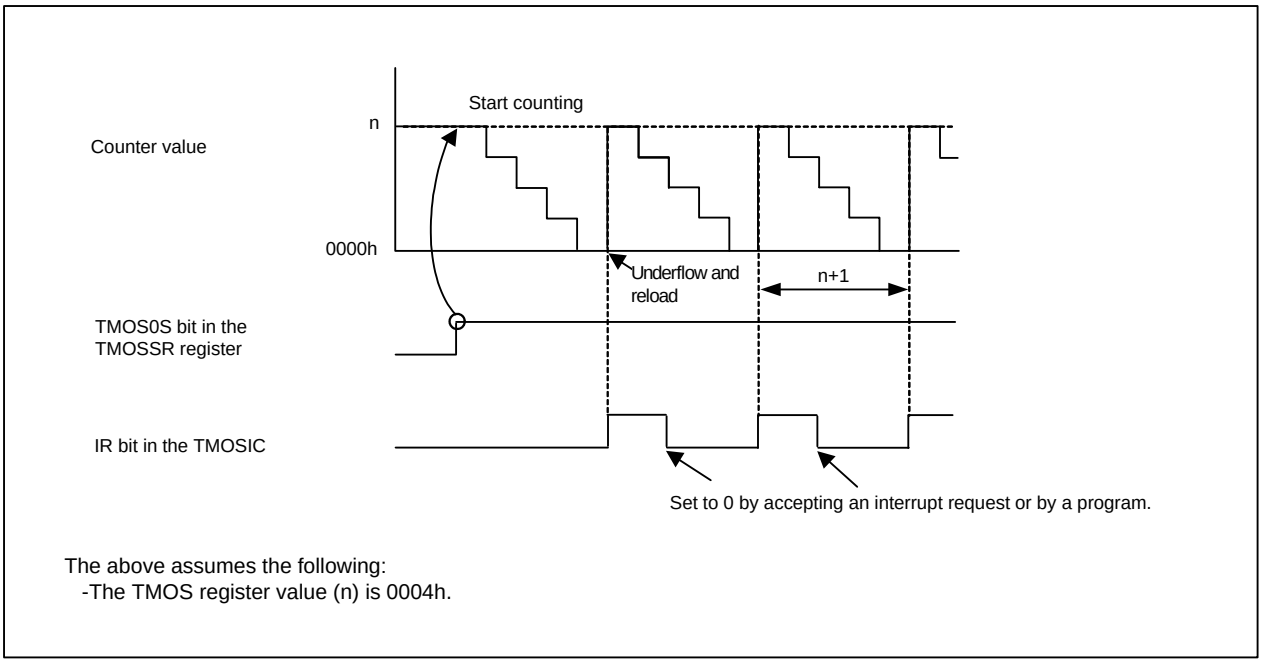


Figure 19.2 Task Monitor Timer Operation

19.4 Interrupt

Table 19.3 lists the Task Monitor Timer Interrupt Associated Register.

Table 19.3 Task Monitor Timer Interrupt Associated Register

Address	Register Name	Register Symbol	Reset Value
004Ah	Task Monitoring Timer Interrupt Control Register	TMOSIC	XXXX X000b

Task monitor timer shares the interrupt vectors and interrupt control registers with other peripheral functions. When using task monitor timer interrupt, set the IFSR20 bit in the IFSR2A register to 1 (task monitor timer).

19.5 Notes on Task Monitor Timer

19.5.1 Register Settings

After reset, the task monitor timer counter is stopped. After setting the counter value and count source by setting registers TMOS register and TMOSCS, set the TMOS0S bit in the TMOSSR register to 1 (start counting).
Change the TMOSCS register value when the TMOS0S bit is 0 (stop counting).

19.5.2 Reading the Timer

While the task monitor timer is counting, the counter value can be read at any given time by reading the TMOS register. However, when reading the counter at its reload timing, the value is read as FFFFh. When the task monitor timer stops counting and after setting the value to the TMOS register, the setting value can be read until the counter starts counting.

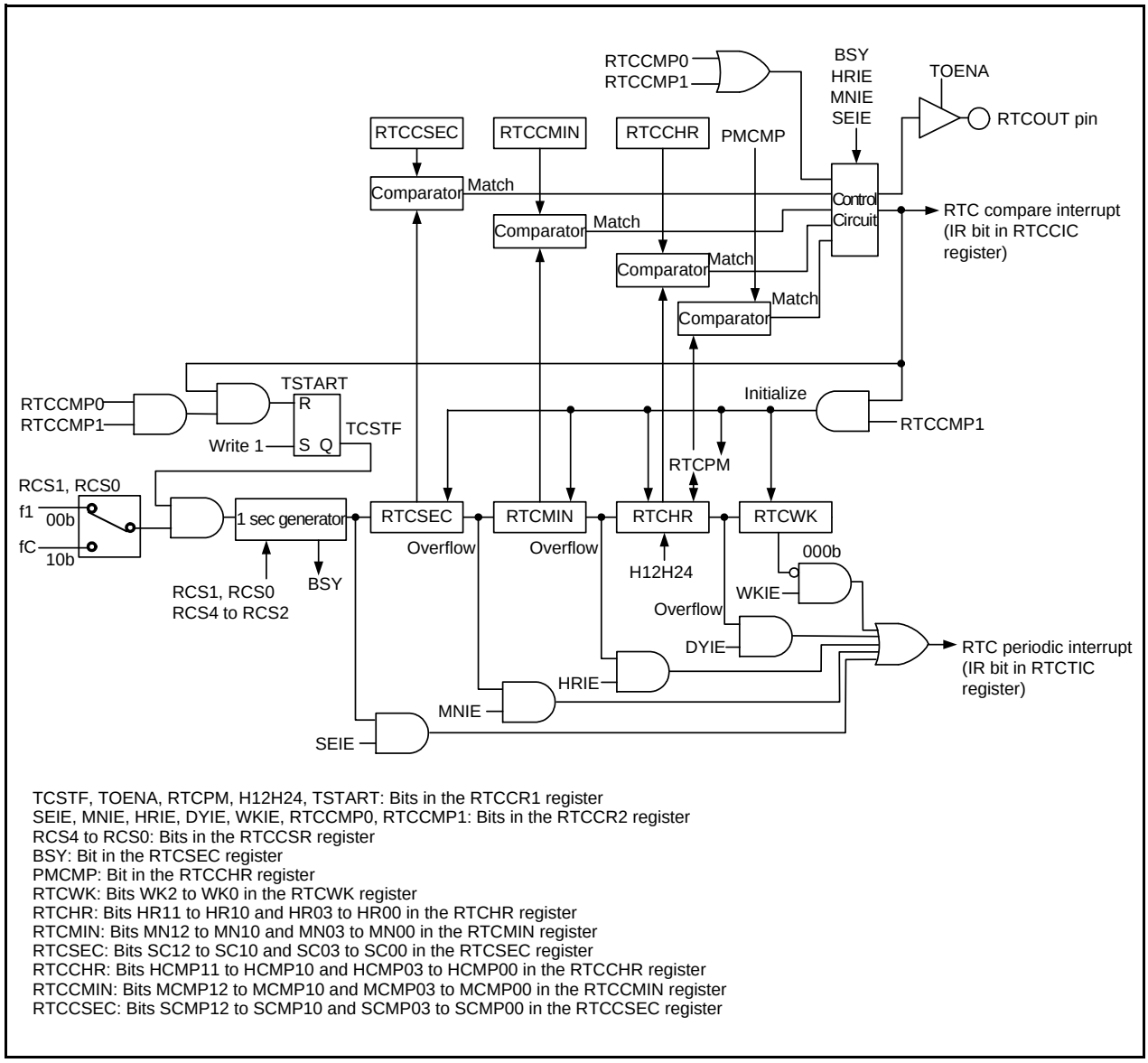
20. Real-Time Clock

20.1 Introduction

The real-time clock generates a 1-second signal from a count source and counts seconds, minutes, hours, a.m./p.m., a day, and a week. It also detects matches with specified seconds, minutes, and hours. Table 20.1 lists Real-Time Clock Specifications, Figure 20.1 shows a Real-Time Clock Block Diagram, and Table 20.2 lists the I/O Port.

Table 20.1 Real-Time Clock Specifications

Item	Specification
Count source	f1, fC
Count operation	• Increment • Compare mode 1 or not using compare mode The count value is continuously used, and the count continues. • Compare mode 2 When a compare match is detected, the count value is set to 0 and the count continues. • Compare mode 3 When a compare match is detected, the count value is set to 0 and the count stops.
Count start condition	1 (count started) is written to the TSTART bit in the RTCCR1 register.
Count stop condition	0 (count stopped) is written to the TSTART bit in the RTCCR1 register.
Interrupt request generation timing	Select one of the following: • Update second data • Update minute data • Update hour data • Update day data • When day data is set to 000b • When time data and compare data match
RTCOUT pin function	Programmable I/O port or compare output
Read from timer	When the RTCSEC, RTCMIN, RTCHR, or RTCWK register is read, the count value can be read. The values read from registers RTCSEC, RTCMIN, and RTCHR are represented by the BCD code.
Write to timer	When bits TSTART and TCSTF in the RTCCR1 register are 0 (count stopped), the RTCSEC, RTCMIN, RTCHR, and RTCWK registers are write enabled. Values written to registers RTCSEC, RTCMIN, and RTCHR are represented by the BCD code.
Selectable functions	• 12-/24-hour mode switch function • Compare output



TCSTF, TOENA, RTCPM, H12H24, TSTART: Bits in the RTCCR1 register
SEIE, MNIE, HRIE, DYIE, WKIE, RTCCMP0, RTCCMP1: Bits in the RTCCR2 register
RCS4 to RCS0: Bits in the RTCCSR register
BSY: Bit in the RTCSEC register
PMCMP: Bit in the RTCCHR register
RTCWK: Bits WK2 to WK0 in the RTCWK register
RTCHR: Bits HR11 to HR10 and HR03 to HR00 in the RTCHR register
RTCMIN: Bits MN12 to MN10 and MN03 to MN00 in the RTCMIN register
RTCSEC: Bits SC12 to SC10 and SC03 to SC00 in the RTCSEC register
RTCCHR: Bits HCMP11 to HCMP10 and HCMP03 to HCMP00 in the RTCCHR register
RTCCMIN: Bits MCMP12 to MCMP10 and MCMP03 to MCMP00 in the RTCCMIN register
RTCCSEC: Bits SCMP12 to SCMP10 and SCMP03 to SCMP00 in the RTCCSEC register

Figure 20.1 Real-Time Clock Block Diagram

Table 20.2 I/O Port

Pin Name	I/O	Function
RTCOUT	Output	Compare output

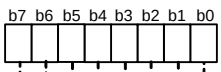
20.2 Registers

Table 20.3 Registers

Address	Register	Symbol	Reset Value
0340h	Real-Time Clock Second Data Register	RTCSEC	00h
0341h	Real-Time Clock Minute Data Register	RTCMIN	X000 0000b
0342h	Real-Time Clock Hour Data Register	RTCHR	XX00 0000b
0343h	Real-Time Clock Day Data Register	RTCWK	XXXX X000b
0344h	Real-Time Clock Control Register 1	RTCCR1	0000 X00Xb
0345h	Real-Time Clock Control Register 2	RTCCR2	X000 0000b
0346h	Real-Time Clock Count Source Select Register	RTCCSR	XXX0 0000b
0348h	Real-Time Clock Second Compare Data Register	RTCCSEC	X000 0000b
0349h	Real-Time Clock Minute Compare Data Register	RTCCMIN	X000 0000b
034Ah	Real-Time Clock Hour Compare Data Register	RTCCHR	X000 0000b

20.2.1 Real-Time Clock Second Data Register (RTCSEC)

Real-Time Clock Second Data Register



Symbol	Address	Reset Value
RTCSEC	0340h	00h

Bit Symbol	Bit Name	Function	Setting Range	RW
SC00	First digit of second count bit	Count 0 to 9 every second. When the digit increments, 1 is added to the 2nd digit of second.	0 to 9	RW
SC01				RW
SC02				RW
SC03				RW
SC10	Second digit of second count bit	When counting 0 to 5, 60 seconds are counted.	0 to 5	RW
SC11				RW
SC12				RW
BSY	Real-time clock busy flag	This bit is 1 while registers RTCSEC, RTCMIN, RTCHR or RTCWK are updated.		RO

SC03 to SC00 (First digit of second count bit) (b3-b0)
SC12 to SC10 (Second digit of second count bit) (b6-b4)

Set a value between 00 and 59 by the BCD code.
These bits become 00 at compare match in compare mode 2 and compare mode 3.
Write to bits SC12 to SC10 and SC03 to SC00 in the RTCSEC register when bits TSTART and TCSTF in the RTCCR1 register are both 0 (count stopped). Read these bits when the BSY bit is 0 (not while data is updated).

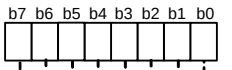
BSY (Real-time clock busy flag) (b7)

This bit is 1 while data is updated. Read the following bits when the BSY bit is 0 (not while data is updated):

- Bits SC12 to SC10 and SC03 to SC00 in the RTCSEC register
- Bits MN12 to MN10 and MN03 to MN00 in the RTCMIN register
- Bits HR11 to HR10 and HR03 to HR00 in the RTCHR register
- Bits WK2 to WK0 in the RTCWK register
- The RTCPM bit in the RTCCR1 register

20.2.2 Real-Time Clock Minute Data Register (RTCMIN)

Real-Time Clock Minute Data Register



Symbol	Address	Reset Value
RTCMIN	0341h	X000 0000b

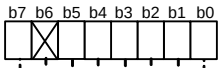
Bit Symbol	Bit Name	Function	Setting Range	RW
MN00	First digit of minute count bit	Count 0 to 9 every minute. When the digit increments, 1 is added to the 2nd digit of minute.	0 to 9	RW
MN01				RW
MN02				RW
MN03				RW
MN10	Second digit of minute count bit	When counting 0 to 5, 60 minutes are counted.	0 to 5	RW
MN11				RW
MN12				RW
$\overline{\text{(b7)}}$	Reserved bit	The read value is undefined.		RO

MN03 to MN00 (First digit of minute count bit) (b3-b0)
MN12 to MN10 (Second digit of minute count bit) (b6-b4)

Set a value between 00 and 59 by the BCD code.
When the digit increments from the RTCSEC register, 1 is added.
These bits become 00 at compare match in compare mode 2 and compare mode 3.
Write to bits MN12 to MN10 and MN03 to MN00 in the RTCMIN register when bits TSTART and TCSTF in the RTCCR1 register are both 0 (count stopped). Read these bits when the BSY bit in the RTCSEC is 0 (not while data is updated).

20.2.3 Real-Time Clock Hour Data Register (RTCHR)

Real-Time Clock Hour Data Register



Symbol	Address	Reset Value
RTCHR	0342h	XX00 0000b

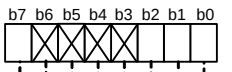
Bit Symbol	Bit Name	Function	Setting Range	RW
HR00	First digit of hour count bit	Count 0 to 9 every hour. When the digit increments, 1 is added to the 2nd digit of hour.	0 to 9	RW
HR01				RW
HR02				RW
HR03				RW
HR10	Second digit of hour count bit	Count 0 to 1 when the H12H24 bit is set to 0 (12-hour mode). Count 0 to 2 when the H12H24 bit is set to 1 (24-hour mode).	0 to 2	RW
HR11				RW
— (b6)	No register bit. If necessary, set to 0. The read value is undefined.			—
— (b7)	Reserved bit	The read value is undefined.		RO

HR03 to HR00 (First digit of hour count bit) (b3-b0)
HR11 and HR10 (Second digit of hour count bit) (b5-b4)

When the H12H24 bit in the RTCCR1 register is 0 (12-hour mode), set a value between 00 and 11 by BCD code. When the H12H24 bit in the RTCCR1 register is 1 (24-hour mode), set a value between 00 and 23 by the BCD code.
When the digit increments from the RTCMIN register, 1 is added.
These bits become 00 at compare match in compare mode 2 and compare mode 3.
Write to bits HR11 to HR10 and HR03 to HR00 in the RTCHR register when bits TSTART and TCSTF in the RTCCR1 register are both 0 (count stopped). Read these bits when the BSY bit in the RTCSEC register is 0 (not while data is updated).

20.2.4 Real-Time Clock Day Data Register (RTCWK)

Real-Time Clock Day Data Register



Symbol	Address	Reset Value
RTCWK	0343h	XXXX X000b

Bit Symbol	Bit Name	Function	RW
WK0	Day count bit	b2 b1 b0 0 0 0 : Day 1 0 0 1 : Day 2 0 1 0 : Day 3 0 1 1 : Day 4 1 0 0 : Day 5 1 0 1 : Day 6 1 1 0 : Day 7 1 1 1 : Do not set	RW
WK1			RW
WK2			RW
— (b6-b3)	No register bits. If necessary, set to 0. The read value is undefined.		—
— (b7)	Reserved bit	The read value is undefined.	RO

WK2 to WK0 (Day count bit) (b2-b0)

A week is counted by counting from 000b (Day 1) to 110b (Day 7) repeatedly. Do not set these bits to 111b.

When the digit increments from the RTCHR register, 1 is added.

These bits become 000b at compare match in compare mode 2 and compare mode 3.

Write to bits WK2 to WK0 in the RTCWK register when bits TSTART and TCSTF in the RTCCR1 register are both 0 (count stopped). Read these bits when the BSY bit in the RTCSEC register is 0 (not while data is updated).

20.2.5 Real-Time Clock Control Register 1 (RTCCR1)

Real-Time Clock Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0
				0			0

Symbol	Address	Reset Value
RTCCR1	0344h	0000 X00Xb

Bit Symbol	Bit Name	Function	RW
— (b0)	Reserved bit	Set to 0	RW
TCSTF	Real-time clock count status flag	0 : Count stopped 1 : Counting	RO
TOENA	RTCOUT pin output bit	0 : Compare output disabled 1 : Compare output enabled	RW
— (b3)	Reserved bit	Set to 0	RW
RTCRST	Real-time clock reset bit	Setting this bit to 0 after setting it to 1 resets the real-time clock.	RW
RTCPM	a.m./p.m. bit	0 : a.m. 1 : p.m.	RW
H12H24	Operating mode select bit	0 : 12-hour mode 1 : 24-hour mode	RW
TSTART	Real-time clock count start bit	0 : Count stopped 1 : Count started	RW

TCSTF (Real-time clock count status flag) (b1)
TSTART (Real-time clock count start bit) (b7)

The real-time clock uses the TSTART bit to instruct the count to start or stop, and use the TCSTF bit to indicate count start or stop.

The real-time clock starts counting and the TCSTF bit becomes 1 (count started) when the TSTART bit is set to 1 (count started). It takes up to two cycles of the count source until the TCSTF bit becomes 1 after setting the TSTART bit to 1. During this time, do not access registers associated with the real-time clock (1) other than the TCSTF bit.

Also, when setting the TSTART bit to 0 (count stopped), the real-time clock stops counting and the TCSTF bit becomes 0 (count stopped). It takes the time for up to three cycles of the count source until the TCSTF bit becomes 0 after setting the TSTART bit to 0. During this time, do not access registers associated with the real-time clock (1) other than the TCSTF bit.

Note:
1. Registers associated with the real-time clock: RTCSEC, RTCMIN, RTCHR, RTCWK, RTCCR1, RTCCR2, RTCCSR, RTCCSEC, RTCCMIN, and RTCCHR.

RTCRST (Real-Time clock reset bit) (b4)

When setting this bit to 0 after setting it to 1, the following are set automatically:

- The values are reset in registers RTCSEC, RTCMIN, RTCHR, RTCWK, RTCCR2, RTCCSR, RTCCSEC, RTCCMIN, and RTCCHR.
- Bits TCSTF, RTCPM, H12H24, and TSTART in the RTCCR1 register become 0.

RTCPM (a.m./p.m. bit) (b5)

Write to the RTCPM bit when bits TSTART and TCSTF in the RTCCR1 register are both 0 (count stopped). Read this bit when the BSY bit in the RTCSEC register is 0 (not while data is updated).
The RTCPM bit is enabled when the H12H24 bit is 0 (12-hour mode) or 1 (24-hour mode). Set the RTCPM bit as shown below to set the time while the H12H24 bit is 1:

- Set the RTCPM bit to 0 when bits HR11 to HR10 and HR03 to HR00 in the RTCHR register are 00 to 11.
- Set the RTCPM bit to 1 when bits HR11 to HR10 and HR03 to HR00 in the RTCHR register are 12 to 23.

The RTCPM bit changes as follows while counting:

- Becomes 0 when the RTCPM bit is 1 (p.m.) while the clock increments from 11:59:59 (23:59:59 for 24-hour mode) to 00:00:00.
- Becomes 1 when the RTCPM bit is 0 (a.m.) while the clock increments from 11:59:59 to 00:00:00 (12:00:00 for 24-hour mode).

Figure 20.2 shows Time Representation.

Noon

Contents of RTCHR Register	H12H24 bit = 1 (24-hour mode)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
	H12H24 bit = 0 (12-hour mode)	0	1	2	3	4	5	6	7	8	9	10	11	0	1	2	3	4	5
Contents of RTCPM bit		0 (a.m.)												1 (p.m.)					
Contents in RTCWK register		000 (Day 1)																	

Date changes

Contents of RTCHR Register	H12H24 bit = 1 (24-hour mode)	18	19	20	21	22	23	0	1	2	3	...
	H12H24 bit = 0 (12-hour mode)	6	7	8	9	10	11	0	1	2	3	...
Contents of RTCPM bit		1 (p.m.)						0 (a.m.)				...
Contents in RTCWK register		000 (Day 1)						001 (Day 2)				...

Bits RTCPM and H12H24 : Bits in the RTCCR1 register.
The above assumes the count starts from 00:00 (12 a.m.) of day 1.

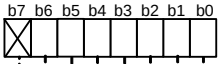
Figure 20.2 Time Representation

H12H24 (Operating mode select bit) (b6)

Write to the H12H24 bit when bits TSTART and TCSTF in the RTCCR1 register are both 0 (count stopped).

20.2.6 Real-Time Clock Control Register 2 (RTCCR2)

Real-Time Clock Control Register 2



Symbol	Address	Reset Value
RTCCR2	0345h	X000 0000b

Bit Symbol	Bit Name	Function	RW
SEIE	Periodic interrupt triggered every second enable bit	0 : Disable periodic interrupt triggered every second 1 : Enable periodic interrupt triggered every second	RW
MNIE	Periodic interrupt triggered every minute enable bit	0 : Disable periodic interrupt triggered every minute 1 : Enable periodic interrupt triggered every minute	RW
HRIE	Periodic interrupt triggered every hour enable bit	0 : Disable periodic interrupt triggered every hour 1 : Enable periodic interrupt triggered every hour	RW
DYIE	Periodic interrupt triggered every day enable bit	0 : Disable periodic interrupt triggered every day 1 : Enable periodic interrupt triggered every day	RW
WKIE	Periodic interrupt triggered every week enable bit	0 : Disable periodic interrupt triggered every week 1 : Enable periodic interrupt triggered every week	RW
RTCCMP0	Compare mode select bit	b6 b5 0 0 : No compare mode 0 1 : Compare mode 1 1 0 : Compare mode 2 1 1 : Compare mode 3	RW
RTCCMP1			RW
— (b7)	No register bit. If necessary, set to 0. The read value is undefined.		—

Write to the RTCCR2 register when bits TSTART and TCSTF in the RTCCR1 register are both 0 (count stopped).

While bits RTCCMP1 to RTCCMP0 are 00b (no compare mode), an interrupt request can be generated every second, minute, hour, day, or week. To generate an interrupt request, set one of the following bits to 1 (interrupt enabled): SEIE, MNIE, HRIE, DAYIE, or WKIE. (Do not set more than one bit to 1.) Table 20.4 lists Periodic Interrupt Sources.

Table 20.4 Periodic Interrupt Sources

Factor	Interrupt Source	Interrupt Enable Bit
Periodic interrupt triggered every week	Value in RTCWK register is set to 000b (1-week period)	WKIE
Periodic interrupt triggered every day	RTCWK register is updated (1-day period)	DYIE
Periodic interrupt triggered every hour	RTCHR register is updated (1-hour period)	HRIE
Periodic interrupt triggered every minute	RTCMIN register is updated (1-minute period)	MNIE
Periodic interrupt triggered every second	RTCSEC register is updated (1-second period)	SEIE

When bits RTCCMP1 to RTCCMP0 are 01b, 10b, or 11b (any compare mode), set the following according to which registers are compared:

- When comparing to the RTCCSEC register, set the SEIE bit to 1 (interrupt enabled).
- When comparing to the RTCCMIN register, set bits SEIE and MNIE to 1.
- When comparing to the RTCCHR register, set bits SEIE, MNIE, and HRIE to 1.

20.2.7 Real-Time Clock Count Source Select Register (RTCCSR)

Real-Time Clock Count Source Select Register

b7	b6	b5	b4	b3	b2	b1	b0
0	X	X					

Symbol	Address	Reset Value
RTCCSR	0346h	XXX0 0000b

Bit Symbol	Bit Name	Function	RW
RCS0	Count source select bit	b1 b0 0 0 : f1 0 1 : Do not set 1 0 : fC 1 1 : Do not set	RW
RCS1			RW
RCS2	Count source frequency select bit	b4 b3 b2 0 0 0 : f1 = fC or 4 MHz 0 0 1 : f1 = 6 MHz 0 1 0 : f1 = 8 MHz 0 1 1 : f1 = 16 MHz 1 0 0 : f1 = 20 MHz 1 0 1 : f1 = 24 MHz 1 1 0 : f1 = 32 MHz 1 1 1 : Do not set	RW
RCS3			RW
RCS4			RW
— (b6-b5)	No register bits. If necessary, set to 0. The read value is undefined.		—
— (b7)	Reserved bit	Set to 0	RW

When bits RCS1 to RCS0 are 10b (fC), set bits RCS4 to RCS2 to 000b.
When bits RCS1 to RCS0 are 00b (f1), select a frequency matched to f1 by bits RCS4 to RCS2.
Write to the RTCCSR register when both bits TSTART and TCSTF in the RTCCR1 register are 0 (count stopped).

When using fC, set the PM25 bit in the PM2 register to 1 (peripheral clock fC provided). Refer to 8. “Clock Generator” for details on fC.

20.2.8 Real-Time Clock Second Compare Data Register (RTCCSEC)

Real-Time Clock Second Compare Data Register

b7 b6 b5 b4 b3 b2 b1 b0	Symbol	Address	Reset Value
	RTCCSEC	0348h	X000 0000b

Bit Symbol	Bit Name	Function	Setting Range	RW
SCMP00	First digit of second compare data bit	Store compare data	0 to 9	RW
SCMP01				RW
SCMP02				RW
SCMP03				RW
SCMP10	Second digit of second compare data bit	Store compare data	0 to 5	RW
SCMP11				RW
SCMP12				RW
— (b7)	No register bit. If necessary, set to 0. The read value is undefined value.			—

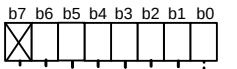
The RTCCSEC register is enabled when bits RTCCMP1 to RTCCMP0 in the RTCCR2 register are 01b, 10b, or 11b (any compare mode).

SCMP03 to SCMP00 (First digit of second compare data bit) (b3-b0)
SCMP12 to SCMP10 (Second digit of second compare data bit) (b6-b4)

Set a value between 00 and 59 by the BCD code.
Write to these bits when the BSY bit in the RTCSEC register is 0 (not while data is updated).

20.2.9 Real-Time Clock Minute Compare Data Register (RTCCMIN)

Real-Time Clock Minute Compare Data Register



Symbol	Address	Reset Value
RTCCMIN	0349h	X000 0000b

Bit Symbol	Bit Name	Function	Setting Range	RW
MCMP00	First digit of minute compare data bit	Store compare data	0 to 9	RW
MCMP01				RW
MCMP02				RW
MCMP03				RW
MCMP10	Second digit of minute compare data bit	Store compare data	0 to 5	RW
MCMP11				RW
MCMP12				RW
— (b7)	No register bit. If necessary, set to 0. The read value is undefined.			—

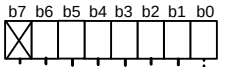
The RTCCMIN register is enabled when bits RTCCMP1 to RTCCMP0 in the RTCCR2 register are 01b, 10b, or 11b (any compare mode).

MCMP03 to MCMP00 (First digit of minute compare data bit) (b3-b0)
MCMP12 to MCMP10 (Second digit of minute compare data bit) (b6-b4)

Set a value between 00 and 59 by the BCD code.
Write to these bits when the BSY bit in the RTCSEC register is 0 (not while data is updated).

20.2.10 Real-Time Clock Hour Compare Data Register (RTCCHR)

Real-Time Clock Hour Compare Data Register



Symbol	Address	Reset Value
RTCCHR	034Ah	X000 0000b

Bit Symbol	Bit Name	Function	Setting Range	RW
HCMP00	First digit of hour compare data bit	Store compare data	0 to 9	RW
HCMP01				RW
HCMP02				RW
HCMP03				RW
HCMP10	Second digit of hour compare data bit	Store compare data	0 to 2	RW
HCMP11				RW
PMCMP	a.m./p.m. compare bit	0 : a.m. 1 : p.m.		RW
— (b7)	No register bit. If necessary, set to 0. The read value is undefined.			—

The RTCCHR register is enabled when bits RTCCMP1 to RTCCMP0 in the RTCCR2 register are 01b, 10b, or 11b (any compare mode).

HCMP03-HCMP00 (First digit of hour compare data bit) (b3-b0)
HCMP11-HCMP10 (Second digit of hour compare data bit) (b5-b4)

When the H12H24 bit in the RTCCR1 register is 0 (12-hour mode), set a value between 00 and 11 by the BCD codes. When the H12H24 bit in the RTCCR1 register is 1 (24-hour mode), set a value between 00 and 23 by the BCD codes.
Write to these bits when the BSY bit in the RTCSEC register is 0 (not while data is updated).

PMCMP (a.m./p.m compare bit) (b6)

This bit is enabled when the H12H24 bit in the RTCCR1 register is either 0 (12-hour mode) or 1 (24-hour mode). When the H12H24 bit is 1, set the following:

- When bits HCMP11 to HCMP10 and HCMP03 to HCMP00 are 00 to 11, set the PMCMP bit to 0.
- When bits HCMP11 to HCMP10 and HCMP03 to HCMP00 are 12 to 23, set the PMCMP bit to 1.

Write to this bit when the BSY bit in the RTCSEC register is 0 (not while data is updated).

20.3 Operations

20.3.1 Basic Operation

The real-time clock generates a 1-second signal from the count source selected in the RTCCSR register and counts seconds, minutes, hours, a.m./p.m., a day, and a week.

The day and time to start the count can be set using registers RTCSEC, RTCMIN, RTCHR, RTCWK, and the RTCPM bit in the RTCCR1 register. Current time and day are read from registers RTCSEC, RTCMIN, RTCHR, RTCWK, and the RTCPM bit in the RTCCR1 register. However, do not read these registers when the BSY bit in the RTCSEC register is 1 (while data is updated).

An interrupt request can be generated every second, minute, hour, day, or week. While bits RTCCMP1 to RTCCMP0 in the RTCCR2 register are 00b (no compare mode), use the RTCCR2 register to enable one of the periodic interrupts triggered every second, minute, hour, day and week. When a periodic interrupt is generated, the IR bit in the RTCTIC register becomes 1 (interrupt request).

Figure 20.3 shows Real-Time Clock Basic Operating Example, Figure 20.4 shows Time and Day Change Procedure (No Compare Mode or Compare Mode 1), and Figure 20.5 shows Time and Day Change Procedure (Compare Mode 2 or Compare Mode 3).

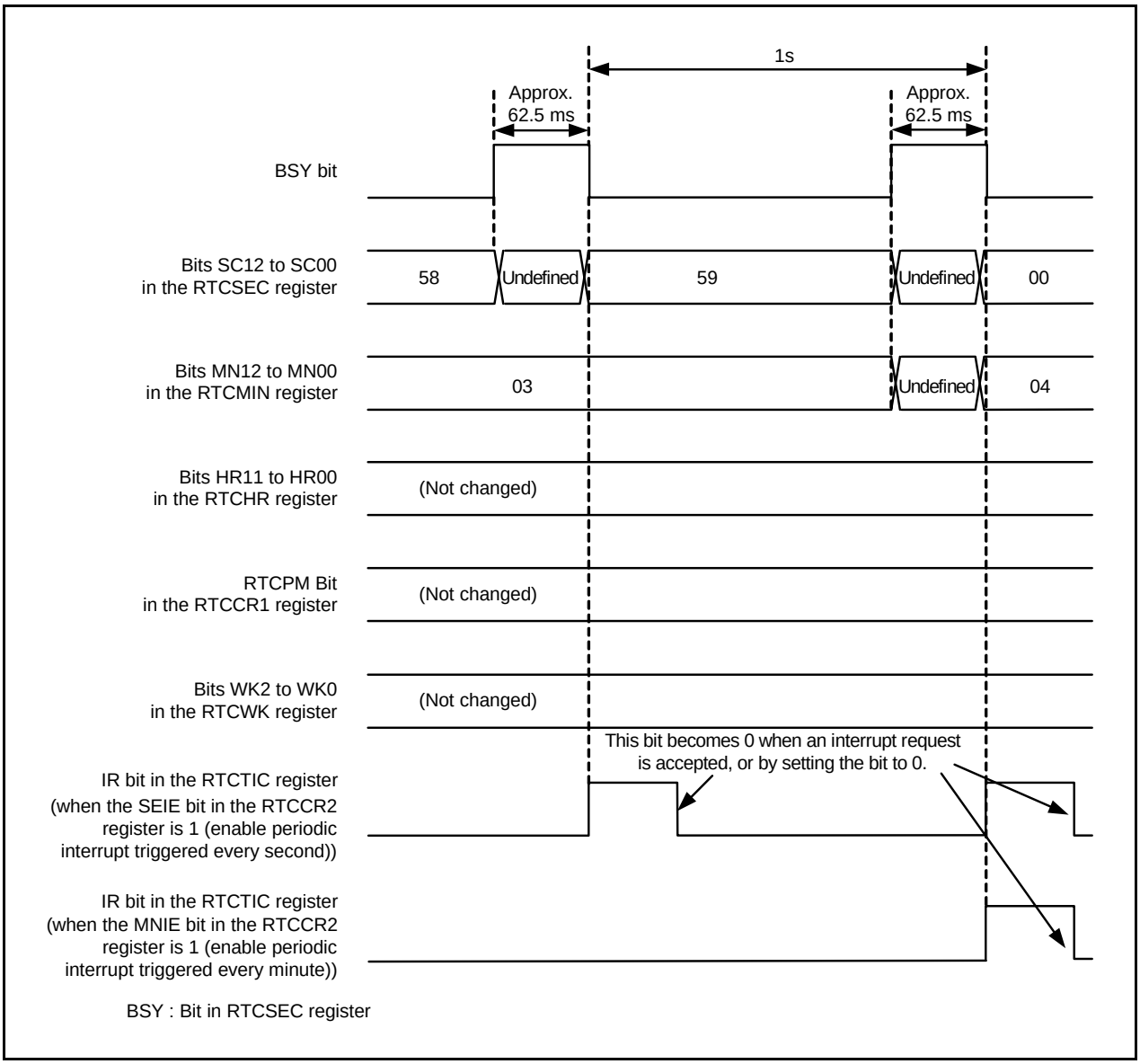


Figure 20.3 Real-Time Clock Basic Operating Example

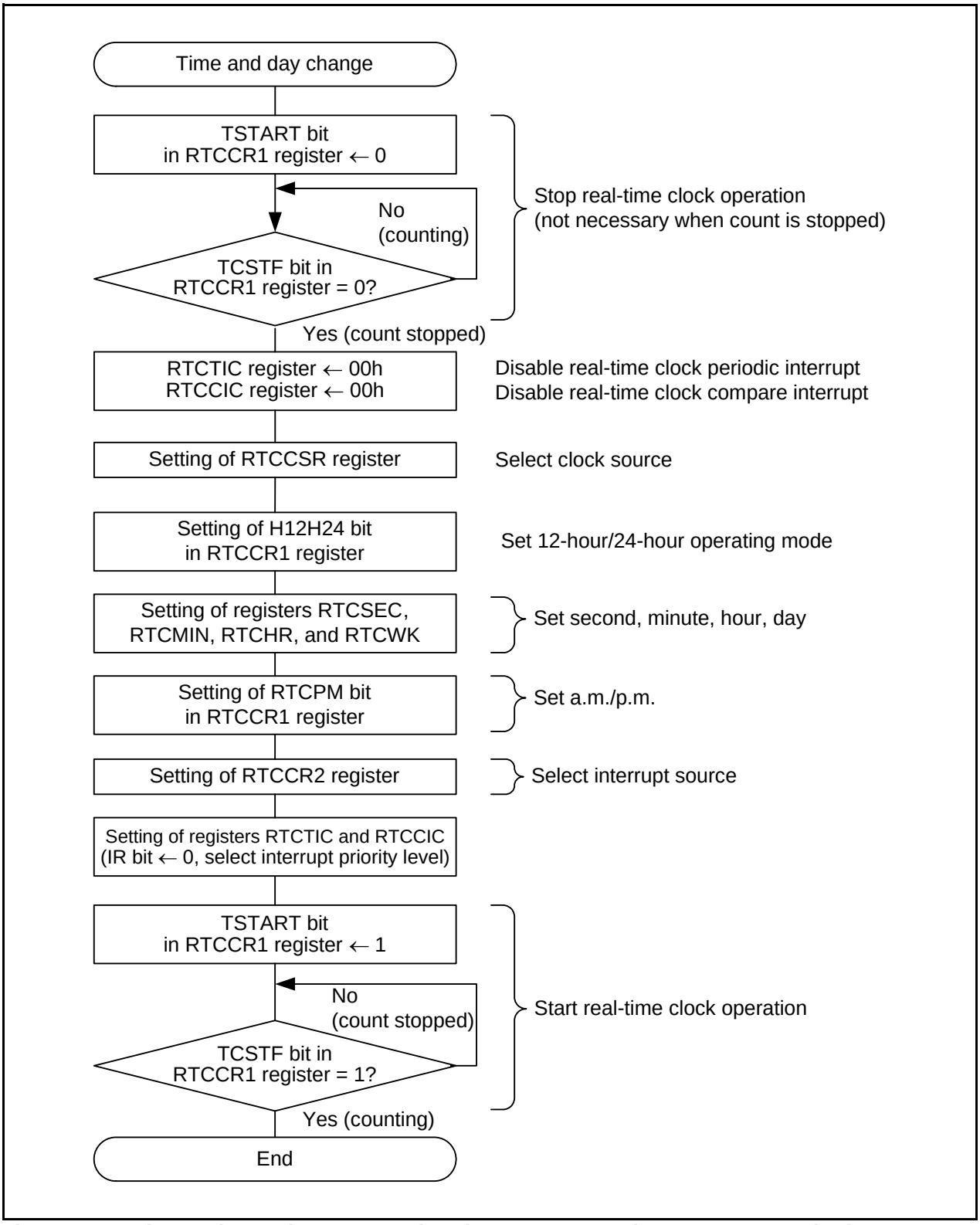
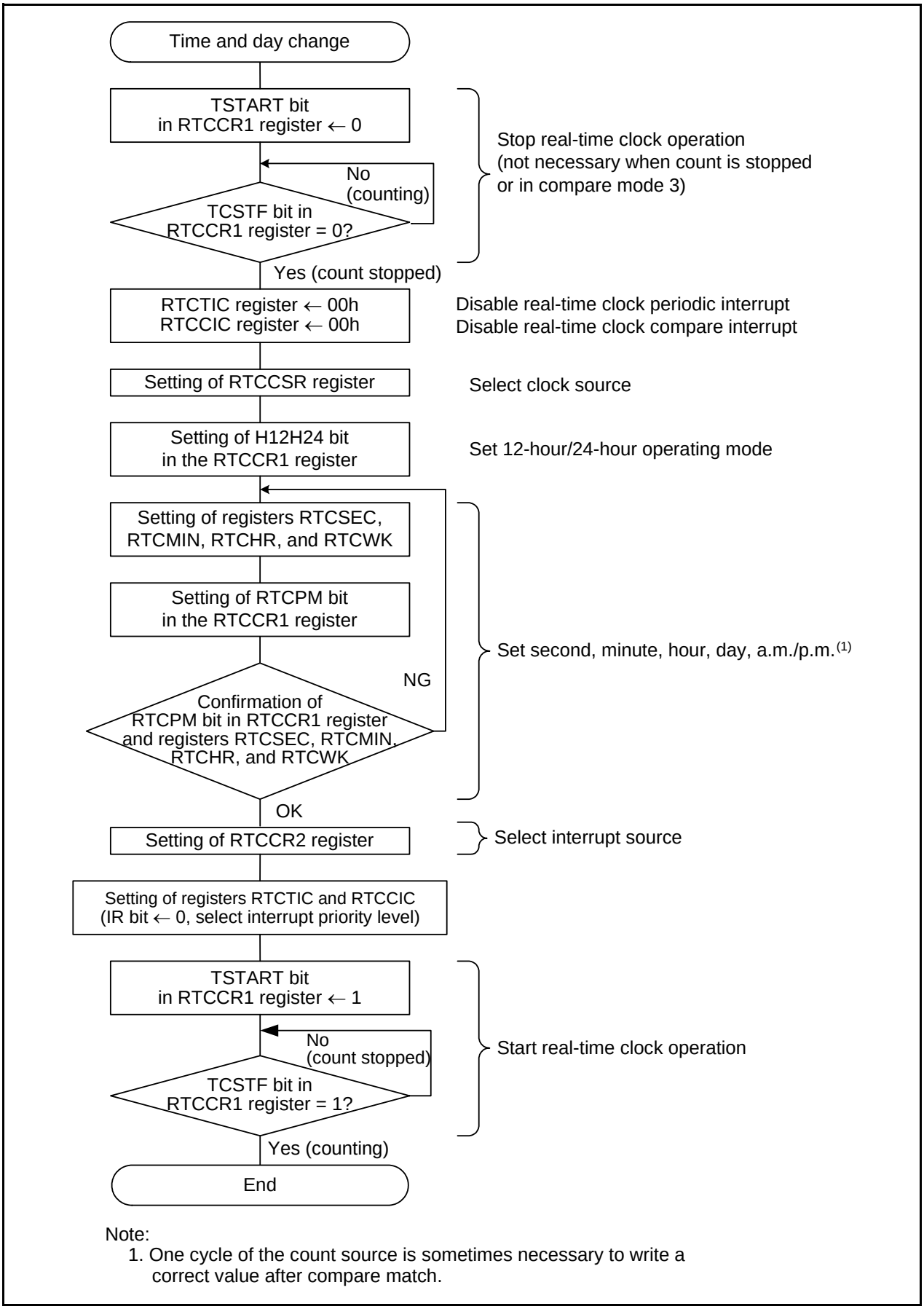


Figure 20.4 Time and Day Change Procedure (No Compare Mode or Compare Mode 1)



Note:
1. One cycle of the count source is sometimes necessary to write a correct value after compare match.

Figure 20.5 Time and Day Change Procedure (Compare Mode 2 or Compare Mode 3)

20.3.2 Compare Mode

In compare mode, time data (1) and compare data (2) are compared, and a compare match is detected. When a match is detected, the following occur:

- Compare interrupt request
  Refer to 20.4 “Interrupts” for details.
- RTCOUT pin output level inversion
  When the TOENA bit in the RTCCR1 register is 1 (compare output enabled), if a compare match is detected, the RTCOUT pin output level is inverted.

Notes:

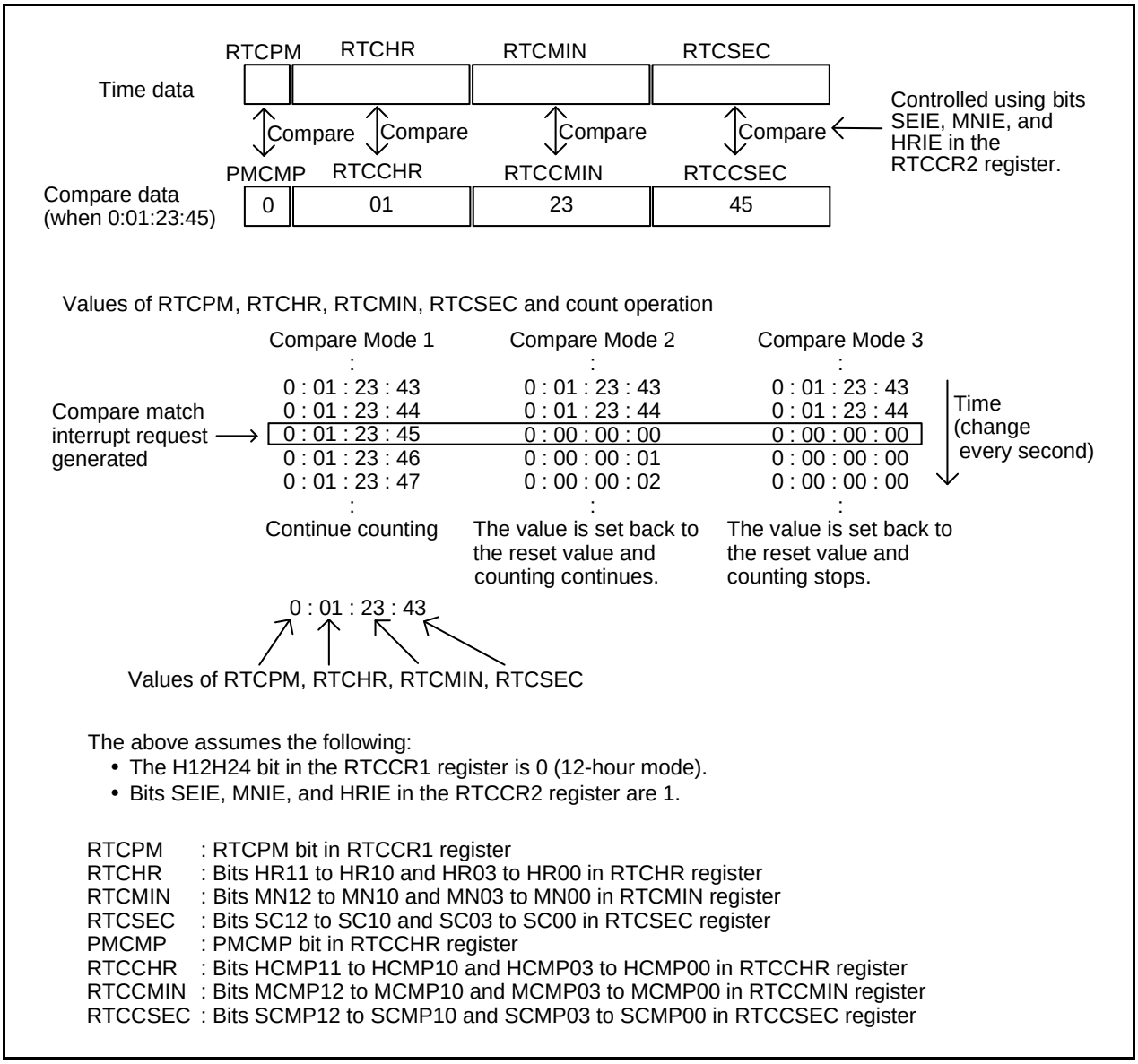
1. Bits for time data are as follows:
   Bits SC12 to SC10 and SC03 to SC00 in the RTCSEC register
   Bits MN12 to MN10 and MN03 to MN00 in the RTCMIN register
   Bits HR11 to HR10 and HR03 to HR00 in the RTCHR register
   The RTCPM bit in the RTCCR1 register

2. Bits for compare data are as follows:
   Bits SCMP12 to SCMP10 and SCMP03 to SCMP00 in the RTCCSEC register
   Bits MCMP12 to MCMP10 and MCMP03 to MCMP00 in the RTCCMIN register
   Bits HCMP11 to HCMP10 and HCMP03 to HCMP00 in the RTCCHR register
   The PMCMP bit in the RTCCHR register

In compare mode, set the SEIE, MNIE, or HRIE bit in the RTCCR2 register to 1 (interrupt enabled) according to compare data (second, minute, or hour). Refer to 20.2.6 “Real-Time Clock Control Register 2 (RTCCR2)” for details.
Compare mode has three modes: compare mode 1, compare mode 2, and compare mode 3. Operation after a compare match differs depending on the compare mode.

- Compare mode 1
  The time data is used continuously and counting continues.
- Compare mode 2
  The reset value is used as the time data and counting continues.
- Compare mode 3
  The reset value is used as the time data and counting stops.

Figure 20.6 shows Difference between Compare Modes, Figure 20.7 shows Count Start/Stop Operating Example, Figure 20.8 shows Compare Mode 1 Operating Example, Figure 20.9 shows Compare Mode 2 Operating Example, and Figure 20.10 shows Compare Mode 3 Operating Example.

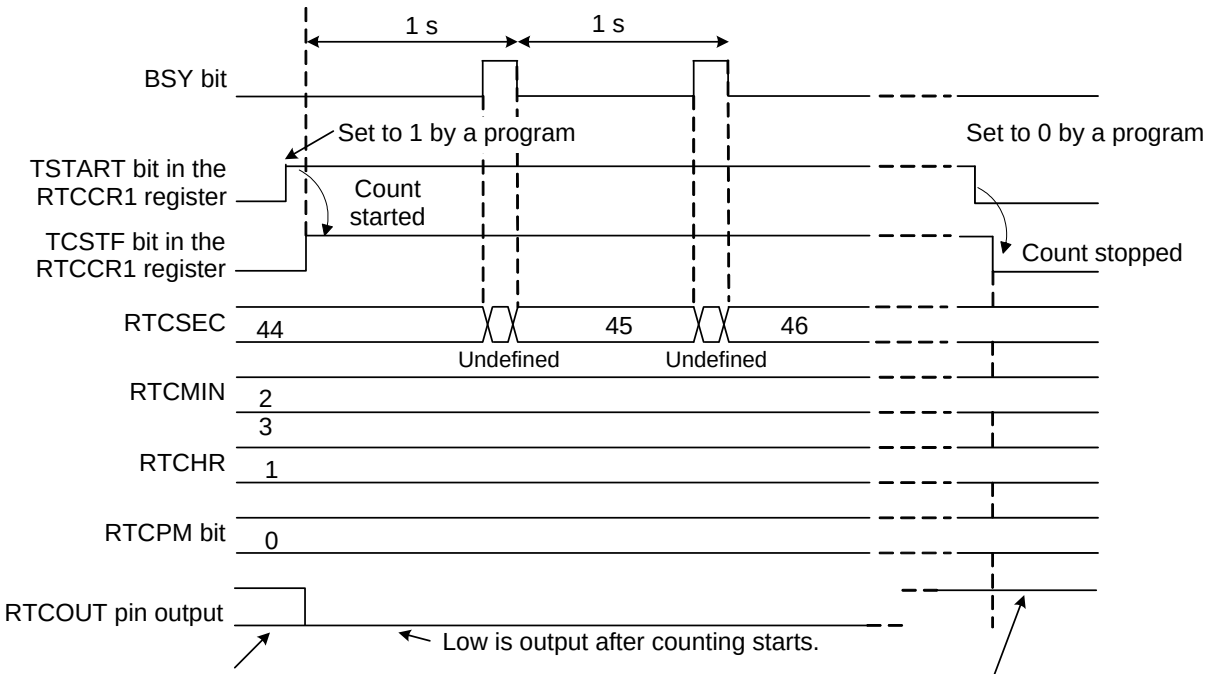


The above assumes the following:

- The H12H24 bit in the RTCCR1 register is 0 (12-hour mode).
- Bits SEIE, MNIE, and HRIE in the RTCCR2 register are 1.

RTCPM : RTCPM bit in RTCCR1 register
RTCHR : Bits HR11 to HR10 and HR03 to HR00 in RTCHR register
RTCMIN : Bits MN12 to MN10 and MN03 to MN00 in RTCMIN register
RTCSEC : Bits SC12 to SC10 and SC03 to SC00 in RTCSEC register
PMCMP : PMCMP bit in RTCCHR register
RTCCHR : Bits HCMP11 to HCMP10 and HCMP03 to HCMP00 in RTCCHR register
RTCCMIN : Bits MCMP12 to MCMP10 and MCMP03 to MCMP00 in RTCCMIN register
RTCCSEC : Bits SCMP12 to SCMP10 and SCMP03 to SCMP00 in RTCCSEC register

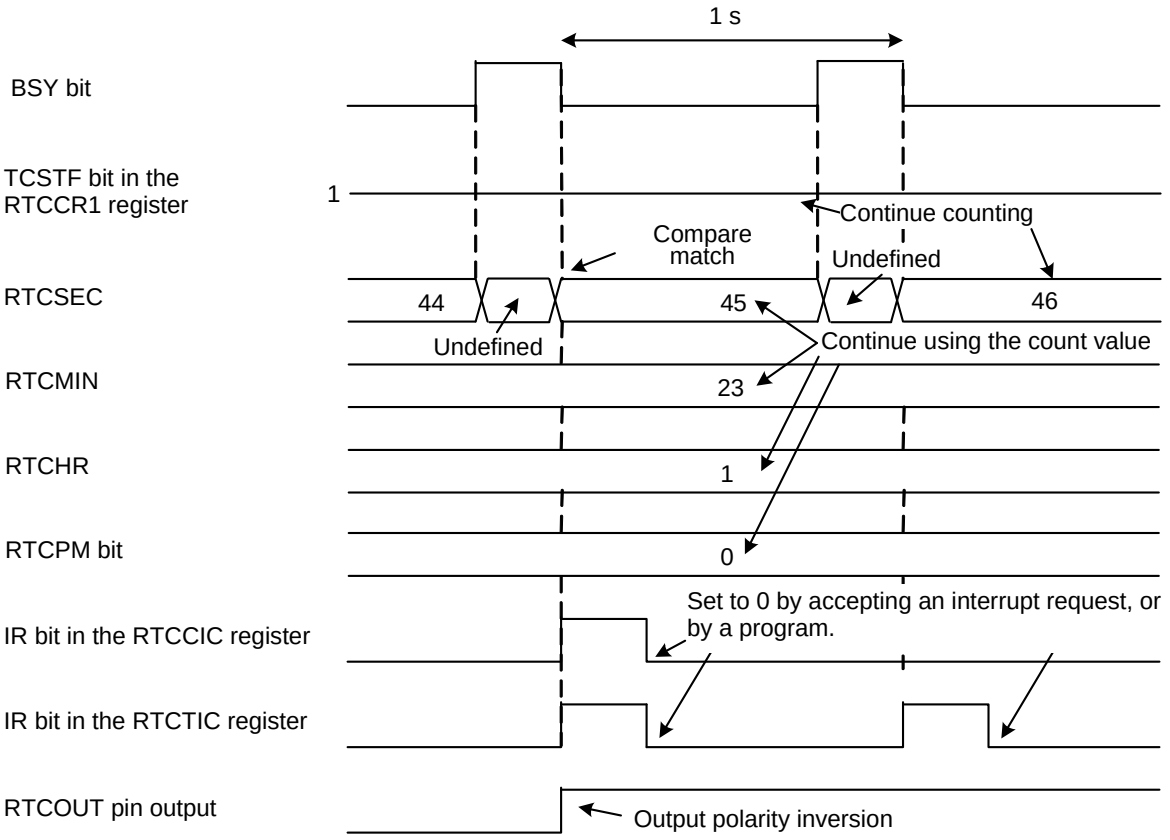
Figure 20.6 Difference between Compare Modes



The above assumes the following:
- The TOENA bit in the RTCCR1 register is 1 (compare output enabled).
- Bits RTCCMP1 to RTCCMP0 in the RTCCR2 register are 01b (compare mode 1).

BSY bit: Bit in RTCSEC register
RTCSEC: Bits SC12 to SC10 and SC03 to SC00 in RTCSEC register
RTCMIN: Bits MN12 to MN10 and MN03 to MN00 in RTCMIN register
RTCHR: Bits HR11 to HR10 and HR03 to HR00 in RTCHR register
RTCPM bit: Bit in RTCCR1 register

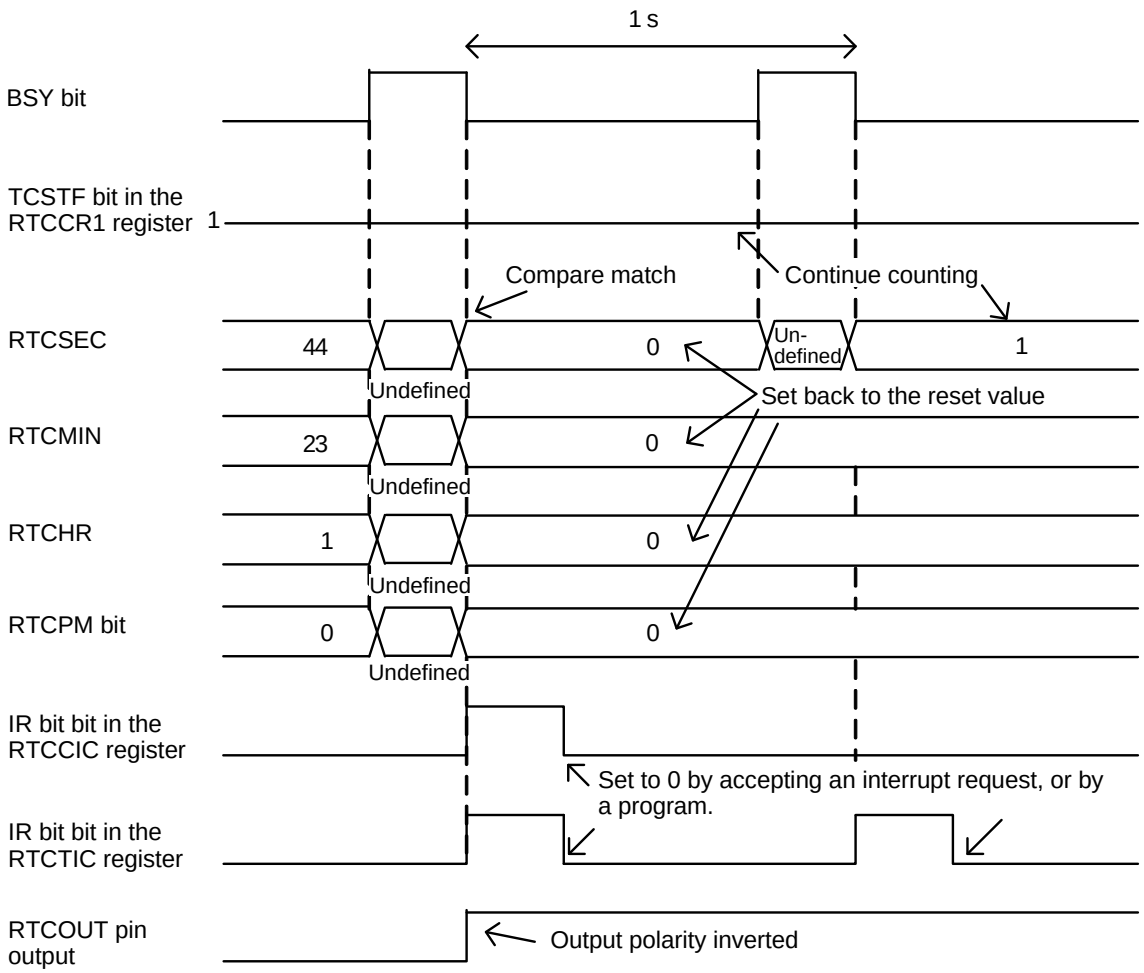
Figure 20.7 Count Start/Stop Operating Example



The above assumes the following:
- The TOENA bit in the RTCCR1 register is 1 (compare output enabled).
- Bits RTCCMP1 to RTCCMP0 in the RTCCR2 register are 01b (compare mode 1).
- Bits SEIE, MNIE, and HRIE in the RTCCR2 are 1 (compare by seconds, minutes, and hours. Interrupt enabled).
- Bits SCMP12 to SCMP10 and SCMP03 to SCMP00 in the RTCCSEC register are 4 and 5, respectively (second setting: 45).
  Bits MCMP12 to MCMP10 and MCMP03 to MCMP00 in the RTCCMIN register are 2 and 3, respectively (minute setting: 23).
  Bits HCMP11 to HCMP10 and HCMP03 to HCMP00 in the RTCCHR register are 0 and 1, respectively (hour setting: 1).
  The PMCMP bit in the RTCCHR register is 0 (a.m.).

BSY bit: Bit in RTCSEC register
RTCSEC: Bits SC12 to SC10 and SC03 to SC00 in RTCSEC register
RTCMIN: Bits MN12 to MN10 and MN03 to MN00 in RTCMIN register
RTCHR: Bits HR11 to HR10 and HR03 to HR00 in RTCHR register
RTCPM bit: Bit in RTCCR1 register

Figure 20.8 Compare Mode 1 Operating Example

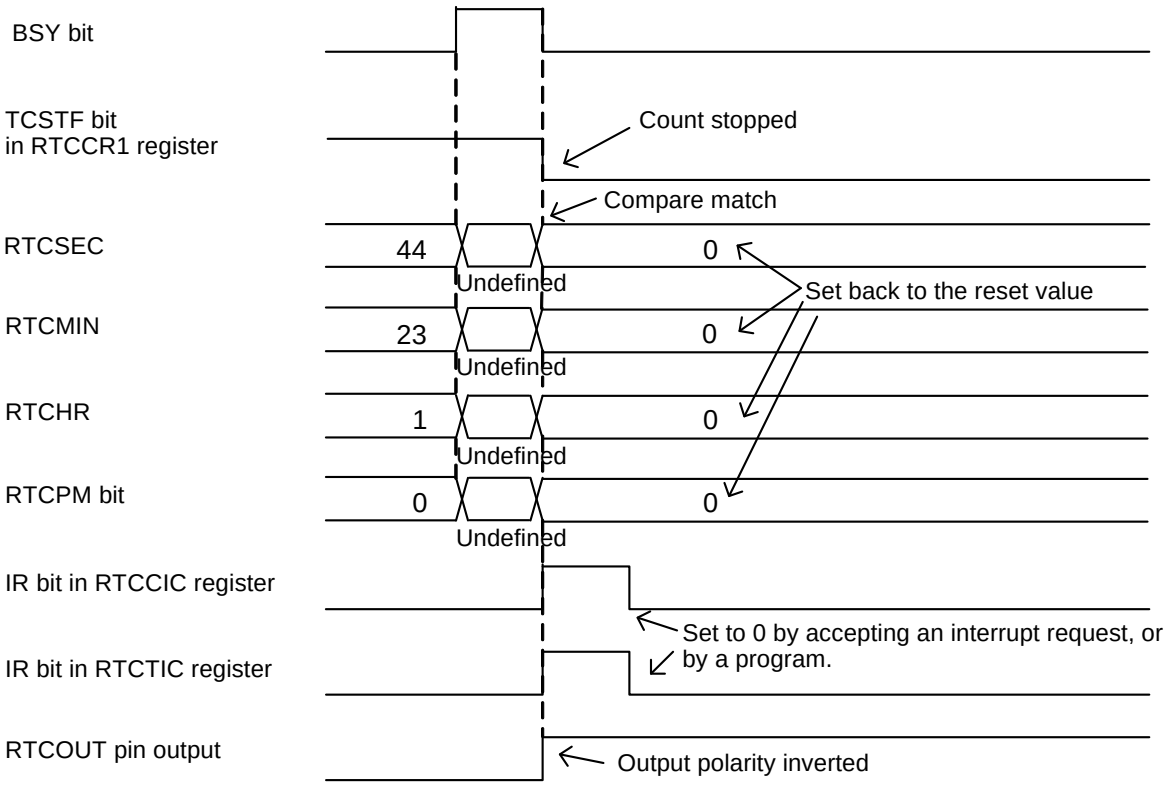


The above assumes the following:

- The TOENA bit in the RTCCR1 register is 1 (compare output enabled).
- Bits RTCCMP1 to RTCCMP0 in the RTCCR2 register are 10b (compare mode 2).
- Bits SEIE, MNIE, and HRIE in the RTCCR2 register are 1 (compare by seconds, minutes, and hours. Interrupt enabled).
- Bits SCMP12 to SCMP10 and SCMP03 to SCMP00 in the RTCCSEC register are 4 and 5, respectively (second setting: 45).
  Bits MCMP12 to MCMP10 and MCMP03 to MCMP00 in the RTCCMIN register are 2 and 3, respectively (minute setting: 23).
  Bits HCMP11 to HCMP10 and HCMP03 to HCMP00 in the RTCCHR register are 0 and 1, respectively (hour setting: 1).
  The PMCMP bit in the RTCCHR register is 0 (a.m.).

BSY bit : Bit in RTCSEC register
RTCSEC : Bits SC12 to SC10 and SC03 to SC00 in RTCSEC register
RTCMIN : Bits MN12 to MN10 and MN03 to MN00 in RTCMIN register
RTCHR : Bits HR11 to HR10 and HR03 to HR00 in RTCHR register
RTCPM bit : Bit in RTCCR1 register

Figure 20.9 Compare Mode 2 Operating Example



The above assumes the following:

- The TOENA bit in the RTCCR1 register is 1 (compare output enabled).
- Bits RTCCMP1 to RTCCMP0 in the RTCCR2 register are 11b (compare mode 3).
- Bits SEIE, MNIE, and HRIE in the RTCCR2 register are 1 (compare by seconds, minutes, and hours. Interrupt enabled).
- Bits SCMP12 to SCMP10 and SCMP03 to SCMP00 in the RTCCSEC register are 4 and 5, respectively (second setting: 45).
  Bits MCMP12 to MCMP10 and MCMP03 to MCMP00 in the RTCCMIN register are 2 and 3, respectively (minute setting: 23).
  Bits HCMP11 to HCMP10 and HCMP03 to HCMP00 in the RTCCHR register are 0 and 1, respectively (hour setting: 1).
  The PMCMP bit in the RTCCHR register is 0 (a.m.).

BSY bit: Bit in RTCSEC register
RTCSEC: Bits SC12 to SC10 and SC03 to SC00 in RTCSEC register
RTCMIN: Bits MN12 to MN10 and MN03 to MN00 in RTCMIN register
RTCHR: Bits HR11 to HR10 and HR03 to HR00 in RTCHR register
RTCPM bit: Bit in RTCCR1 register

Figure 20.10 Compare Mode 3 Operating Example

20.4 Interrupts

The real-time clock generates two types of interrupt:

- Periodic interrupts triggered every second, minute, hour, day, and week
- Compare match interrupt

See Table 20.4 Periodic Interrupt Sources for details on periodic interrupt sources, individual mode specifications and an operating example for the interrupt request generating timing. Refer to 12.7 “Interrupt Control” for details of interrupt control. Table 20.5 lists Real-Time Clock Interrupt-Associated Registers.

Table 20.5 Real-Time Clock Interrupt-Associated Registers

Address	Register	Symbol	Reset Value
006Fh	Real-Time Clock Compare Interrupt Control Register	RTCCIC	XXXX X000b
0074h	Real-Time Clock Cycle Interrupt Control Register	RTCTIC	XXXX X000b
0204h	Interrupt Source Select Register 4	IFSR4A	00h
0205h	Interrupt Source Select Register 3	IFSR3A	00h

The real-time clock shares interrupt vectors and interrupt control registers with other peripheral functions. To use period interrupts, set the IFSR47 bit in the IFSR4A register to 0 (real-time clock cycle). To use compare interrupts, set the IFSR36 bit in the IFSR3A register to 1 (real-time clock compare).

20.5 Notes on Real-Time Clock

20.5.1 Starting and Stopping the Count

The real-time clock uses the TSTART bit for instructing the count to start or stop, and the TCSTF bit which indicates count started or stopped. Bits TSTART and TCSTF are in the RTCCR1 register.

The real-time clock starts counting and the TCSTF bit becomes 1 (count started) when the TSTART bit is set to 1 (count started). It takes up to two cycles of the count source until the TCSTF bit becomes 1 after setting the TSTART bit to 1. During this time, do not access registers associated with the real-time clock (1) other than the TCSTF bit.

Similarly, when setting the TSTART bit to 0 (count stopped), the real-time clock stops counting and the TCSTF bit becomes 0 (count stopped). It takes up to three cycles of the count source until the TCSTF bit becomes 0 after setting the TSTART bit to 0. During this time, do not access registers associated with the real-time clock other than the TCSTF bit.

Note:

1. Registers associated with the real-time clock: RTCSEC, RTCMIN, RTCHR, RTCWK, RTCCR1, RTCCR2, RTCCSR, RTCCSEC, RTCCMIN, and RTCCHR.

20.5.2 Register Settings (Time Data, etc.)

Write to the following registers/bits when the real-time clock is stopped:

- Registers RTCSEC, RTCMIN, RTCHR, RTCWK, and RTCCR2
- Bits H12H24 and RTCPM in the RTCCR1 register
- Bits RCS0 to RCS4 in the RTCCSR register

The real-time clock is stopped when bits TSTART and TCSTF in the RTCCR1 register are 0 (real-time clock stopped).

Set the RTCCR2 register after setting the registers and bits mentioned above (immediately before the real-time clock count starts).

Figure 20.4 shows Time and Day Change Procedure (No Compare Mode or Compare Mode 1), and Figure 20.5 shows Time and Day Change Procedure (Compare Mode 2 or Compare Mode 3).

20.5.3 Register Settings (Compare Data)

Write to the following registers when the BSY bit in the RTCSEC register is 0 (not while data is updated).

- Registers RTCCSEC, RTCCMIN, and RTCCHR

20.5.4 Time Reading Procedure in Real-Time Clock Mode

In real-time clock mode, read time data bits (1) when the BSY bit in the RTCSEC register is 0 (not while data is updated).

When reading multiple registers, if data is rewritten between reading registers, an errant time will be read. To prevent this, use one of the following steps when reading:

- Using an interrupt
  In the real-time clock periodic interrupt routine, read the values necessary from the appropriate time data bits.
- Monitoring by a program 1
  Monitor the IR bit in the RTCTIC register by a program and read necessary values of time data bits after the IR bit becomes 1 (periodic interrupt requested).
- Monitoring by a program 2
  Read the time data according to Figure 20.11 “Time Data Reading”.

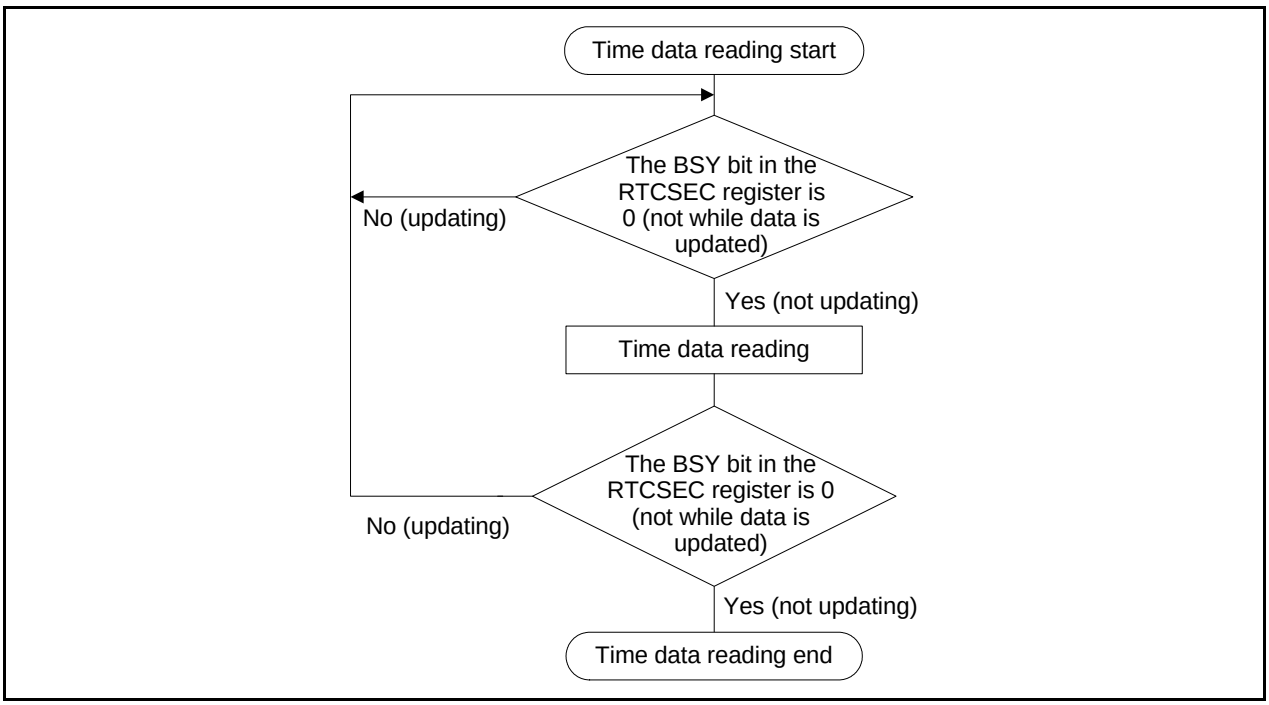


Figure 20.11 Time Data Reading

Also, when reading multiple registers, read them as continuously as possible.

Note:

1. Time data bits are as follows:
   Bits SC12 to SC10 and SC03 to SC00 in the RTCSEC register
   Bits MN12 to MN10 and MN03 to MN00 in the RTCMIN register
   Bits HR11 to HR10 and HR03 to HR00 in the RTCHR register
   Bits WK2 to WK0 in the RTCWK register
   The RTCPM bit in the RTCCR1 register

21. Serial Interface UARTi (i = 0 to 4)

Note

Pins CLK4, RXD4, and TXD4 do not exist in the 64-pin package. Do not access the UART4 associated registers.

21.1 Introduction

Serial interfaces consist of five channels: UART0 to UART4.

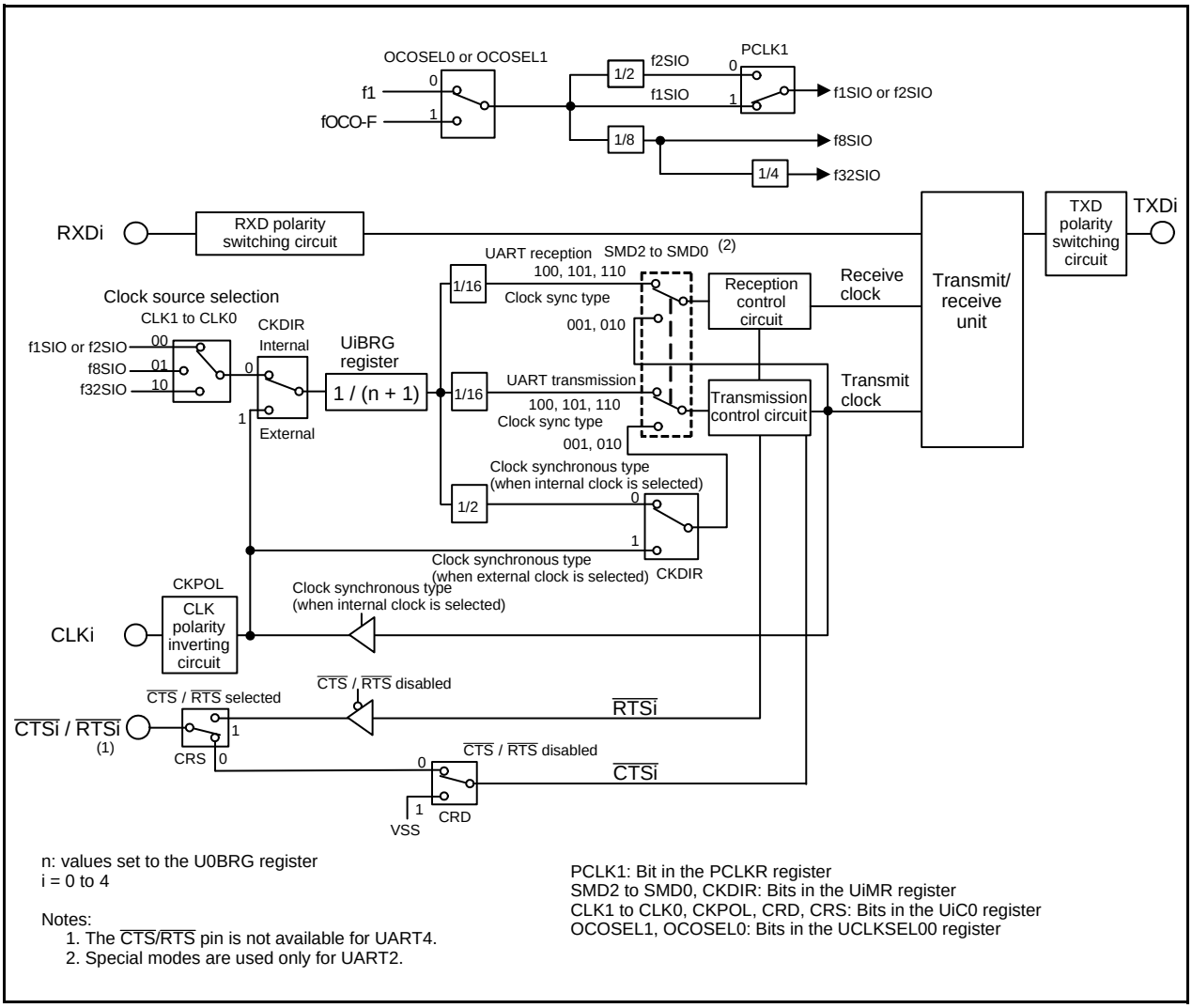
Each UART has a dedicated timer to generate a transmit/receive clock, and operates independently of the others.
Table 21.1 lists UARTi Specifications (i = 0 to 4). Table 21.2 lists Specification Differences between UART0 to UART4. Figure 21.1 shows the block diagram of UARTi. Figure 21.2 shows UARTi Transmit/Receive Unit Block Diagram.

Table 21.1 UARTi Specifications (i = 0 to 4)

Item	Specification
Operational mode	• Clock synchronous serial I/O mode • Clock asynchronous serial I/O mode (UART mode) • Special mode 1 (I^2C mode) Can be used with UART2. The simplified I^2C-bus interface is supported. • Special mode 2 Can be used with UART2. The transmit/receive clock polarity and phase are selectable. • Special mode 3 (bus collision detection function, IE mode) Can be used with UART2. A 1-byte wave of the UART mode approximates 1-bit of the IEBus. • Special mode 4 (SIM mode) Can be used with UART2. The SIM interface is supported.

Table 21.2 Specification Differences between UART0 to UART4

Mode	UART0	UART1	UART2	UART3	UART4
Clock synchronous serial I/O mode	Available		Available	Available	
Clock asynchronous serial I/O mode (UART mode)	Available		Available	Available	
Special mode 1 (I^2C mode)	Not available		Available	Not available	
Special mode 2	Not available		Available	Not available	
Special mode 3 (IE mode)	Not available		Available	Not available	
Special mode 4 (SIM mode)	Not available		Available	Not available	
$\overline{CTS}/\overline{RTS}$ pin	Available		Available	Available	Not available

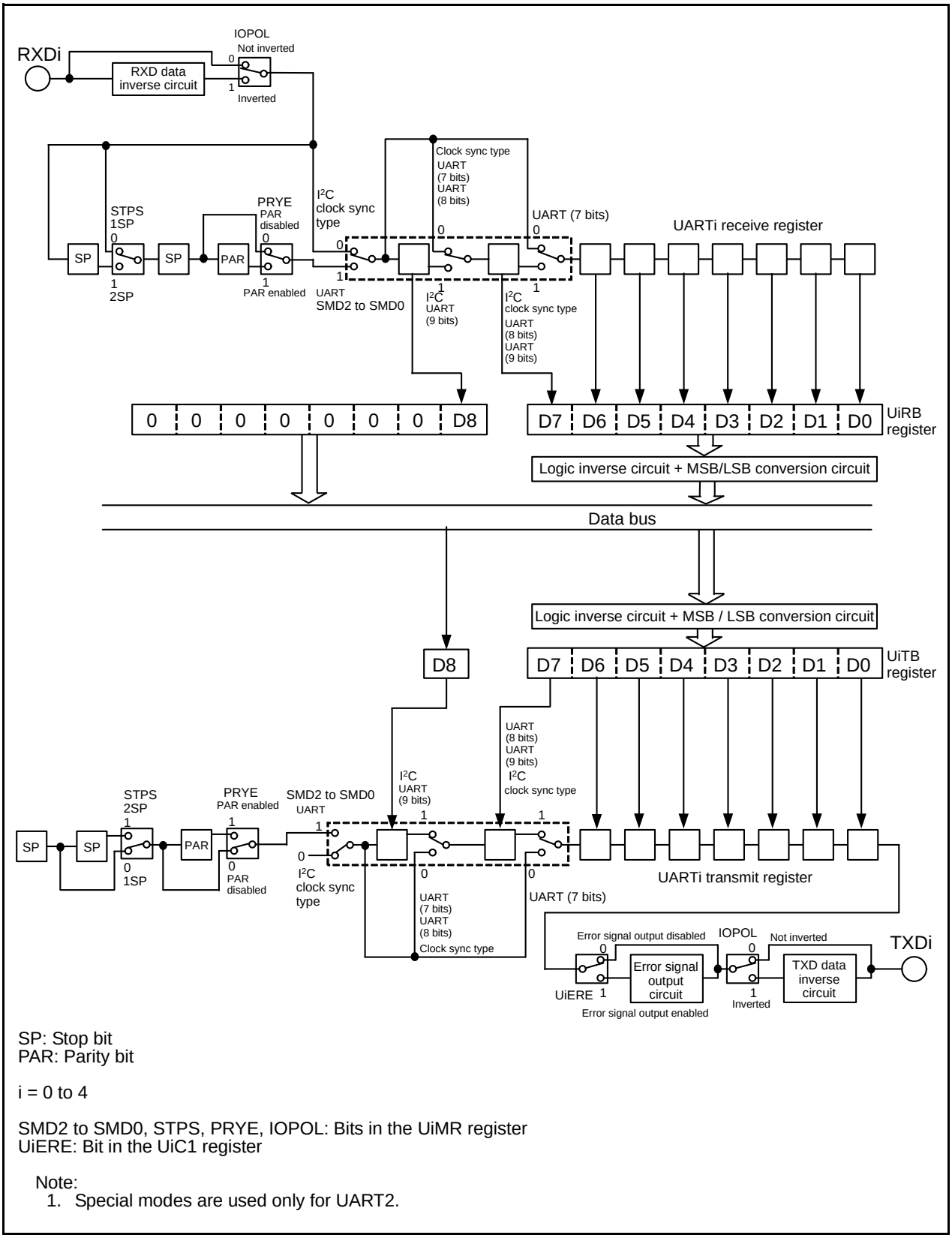


n: values set to the U0BRG register
i = 0 to 4

Notes:
1. The $\overline{CTS}/\overline{RTS}$ pin is not available for UART4.
2. Special modes are used only for UART2.

PCLK1: Bit in the PCLKR register
SMD2 to SMD0, CKDIR: Bits in the UiMR register
CLK1 to CLK0, CKPOL, CRD, CRS: Bits in the UiC0 register
OCOSEL1, OCOSEL0: Bits in the UCLKSEL00 register

Figure 21.1 UARTi Block Diagram



SP: Stop bit
PAR: Parity bit

i = 0 to 4

SMD2 to SMD0, STPS, PRYE, IOPOL: Bits in the UiMR register
UiERE: Bit in the UiC1 register

Note:
1. Special modes are used only for UART2.

Figure 21.2 UARTi Transmit/Receive Unit Block Diagram

21.2 Registers

Table 21.3 and Table 21.4 list registers associated with UART0 to UART4.
Set the OCOSEL0 or OCOSEL1 bit in the UCLKSEL0 register before setting other registers associated with UART0 to UART4. After changing the OCOSEL0 or OCOSEL1 bit, set other registers associated with UART0 to UART4 again.
Refer to “Registers Used and Settings” in each mode for the settings of registers and bits.

Table 21.3 Registers (1/2)

Address	Register	Symbol	Reset Value
0012h	Peripheral Clock Select Register	PCLKR	0000 0011b
0248h	UART0 Transmit/Receive Mode Register	U0MR	00h
0249h	UART0 Bit Rate Register	U0BRG	XXh
024Ah	UART0 Transmit Buffer Register	U0TB	XXh
024Bh			XXh
024Ch	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000b
024Dh	UART0 Transmit/Receive Control Register 1	U0C1	0000 0010b
024Eh	UART0 Receive Buffer Register	U0RB	XXh
024Fh			XXh
0252h	UART Clock Select Register	UCLKSEL0	X0h
0258h	UART1 Transmit/Receive Mode Register	U1MR	00h
0259h	UART1 Bit Rate Register	U1BRG	XXh
025Ah	UART1 Transmit Buffer Register	U1TB	XXh
025Bh			XXh
025Ch	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000b
025Dh	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010b
025Eh	UART1 Receive Buffer Register	U1RB	XXh
025Fh			XXh
0264h	UART2 Special Mode Register 4	U2SMR4	00h
0265h	UART2 Special Mode Register 3	U2SMR3	000X 0X0Xb
0266h	UART2 Special Mode Register 2	U2SMR2	X000 0000b
0267h	UART2 Special Mode Register	U2SMR	X000 0000b
0268h	UART2 Transmit/Receive Mode Register	U2MR	00h
0269h	UART2 Bit Rate Register	U2BRG	XXh
026Ah	UART2 Transmit Buffer Register	U2TB	XXh
026Bh			XXh
026Ch	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000b

Table 21.4 Registers (2/2)

Address	Register	Symbol	Reset Value
026Dh	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010b
026Eh	UART2 Receive Buffer Register	U2RB	XXh
026Fh			XXh
0298h	UART4 Transmit/Receive Mode Register	U4MR	00h
0299h	UART4 Bit Rate Register	U4BRG	XXh
029Ah	UART4 Transmit Buffer Register	U4TB	XXh
029Bh			XXh
029Ch	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000b
029Dh	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010b
029Eh	UART4 Receive Buffer Register	U4RB	XXh
029Fh			XXh
02A8h	UART3 Transmit/Receive Mode Register	U3MR	00h
02A9h	UART3 Bit Rate Register	U3BRG	XXh
02AAh	UART3 Transmit Buffer Register	U3TB	XXh
02ABh			XXh
02ACh	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000b
02ADh	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010b
02AEh	UART3 Receive Buffer Register	U3RB	XXh
02AFh			XXh
0370h	Pin Assignment Control Register	PACR	0XXX X000b

21.2.1 UART Clock Select Register (UCLKSEL0)

UART Clock Select Register

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X			0	0

Symbol	Address	Reset Value
UCLKSEL0	0252h	X0h

Bit Symbol	Bit Name	Function	RW
— (b1-b0)	Reserved bits	Set to 0	RW
OCOSEL0	UART0 to UART2 clock prior to division select bit	0 : f1 1 : fOCO-F	RW
OCOSEL1	UART3 to UART4 clock prior to division select bit	0 : f1 1 : fOCO-F	RW
— (b7-b4)	No register bits. If necessary, set to 0. The read value is undefined.		—

OCOSEL0 (UART0 to UART2 clock prior to division select bit) (b2)
OCOSEL1 (UART3 to UART4 clock prior to division select bit) (b3)

Set bits OCOSEL0 and OCOSEL1 while transmission/reception of UART0 to UART2 and UART3 to UART4 stops.

Set the OCOSEL0 or OCOSEL1 bit before setting other registers associated with UART0 to UART2 and UART3 to UART4. After changing the OCOSEL0 or OCOSEL1 bit, set other registers associated with UART0 to UART2 and UART3 to UART4 again.

21.2.2 Peripheral Clock Select Register (PCLKR)

Peripheral Clock Select Register

b7	b6	b5	b4	b3	b2	b1	b0
0	0		0	0	0		

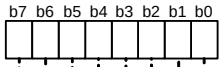
Symbol	Address	Reset Value
PCLKR	0012h	00000011b

Bit Symbol	Bit Name	Function	RW
PCLK0	Timers A, B, S, multi-master I²C-bus interface clock select bit (clock source for timers A , B, S, dead time timer, and multi-master I²C-bus interface)	0: f2TIMAB/f2IIC 1: f1TIMAB/f1IIC	RW
PCLK1	SI/O clock select bit (clock source for UART0 to UART4)	0: f2SIO 1: f1SIO	RW
— (b4-b2)	Reserved bits	Set to 0.	RW
PCLK5	Clock output function extension bit	0: Selected by setting bits CM01 and CM00 in the CM0 register 1: Outputs f1	RW
— (b7-b6)	Reserved bits	Set to 0.	RW

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting this register.

21.2.3 UARTi Transmit/Receive Mode Register (UiMR) (i = 0 to 4)

UARTi Transmit/Receive Mode Register (i = 0 to 4)



Symbol	Address	Reset Value
U0MR, U1MR, U2MR	0248h, 0258h, 0268h	00h
U4MR, U3MR	0298h, 02A8h	00h

Bit Symbol	Bit Name	Function	RW
SMD0	Serial I/O mode select bit	b2 b1 b0 0 0 0 : Serial interface disabled 0 0 1 : Clock synchronous serial I/O mode 0 1 0 : I²C mode 1 0 0 : UART mode character bit length is 7 bits 1 0 1 : UART mode character bit length is 8 bits 1 1 0 : UART mode character bit length is 9 bits Only set the values listed above.	RW
SMD1			RW
SMD2			RW
CKDIR	Internal/external clock select bit	0 : Internal clock 1 : External clock	RW
STPS	Stop bit length select bit	0 : 1 stop bit 1 : 2 stop bit	RW
PRY	Odd/even parity select bit	Enabled when PRYE is 1 0 : Odd parity 1 : Even parity	RW
PRYE	Parity enable bit	0 : Parity disabled 1 : Parity enabled	RW
IOPOL	TXD, RXD I/O polarity inverse bit	0 : Not inverted 1 : Inverted	RW

Write to the U4MR register in the next instruction after setting the PRC2 bit in the PRCR register to 1 (write enabled)

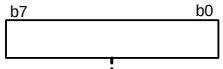
SMD2 to SMD0 (Serial I/O mode select bit) (b2 to b0)

When setting bits SMD2 to SMD0 to 000b (serial interface disabled), set the TE bit in the UiC1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).

010b (I²C mode) is selected by the U2MR register. Do not select 010b by the U0MR, U1MR, U3MR, or U4MR register.

21.2.4 UARTi Bit Rate Register (UiBRG) (i = 0 to 4)

UARTi Bit Rate Register (i = 0 to 4)



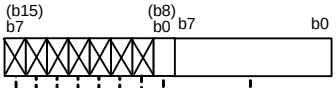
Symbol	Address	Reset Value
U0BRG, U1BRG, U2BRG	0249h, 0259h, 0269h	XXh
U4BRG, U3BRG	0299h, 02A9h	XXh

Function	Setting Range	RW
If set value is n, UiBRG divides the count source by n + 1.	00h to FFh (other than I^2C mode) 03h to FFh (I^2C mode)	WO

Write to the UiBRG register while the serial interface is neither transmitting nor receiving.
Use the MOV instruction to write to the UiBRG register.
Write to the UiBRG register after setting bits CLK1 to CLK0 in the UiC0 register.

21.2.5 UARTi Transmit Buffer Register (UiTB) (i = 0 to 4)

UARTi Transmit Buffer Register (i = 0 to 4)



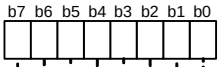
Symbol	Address	Reset Value
U0TB	024Bh to 024Ah	XXXXh
U1TB	025Bh to 025Ah	XXXXh
U2TB	026Bh to 026Ah	XXXXh
U4TB	029Bh to 029Ah	XXXXh
U3TB	02ABh to 02AAh	XXXXh

Function	RW
Transmit data	WO
No register bits. If necessary, set to 0. The read value is undefined.	—

Use the MOV instruction to write to this register.
When character length is 9 bits long or I^2C mode, write to this register in 16-bit units, or in 8-bit units from upper byte to lower byte.

21.2.6 UARTi Transmit/Receive Control Register 0 (UiC0) (i = 0 to 4)

UARTi Transmit/Receive Control Register 0 (i = 0 to 4)



Symbol	Address	Reset Value
U0C0, U1C0, U2C0	024Ch, 025Ch, 026Ch	0000 1000b
U4C0, U3C0	029Ch, 02ACh	0000 1000b

Bit Symbol	Bit Name	Function	RW
CLK0	UiBRG count source select bit	b1 b0 0 0 : f1SIO or f2SIO selected 0 1 : f8SIO selected 1 0 : f32SIO selected 1 1 : Do not set	RW
CLK1			RW
CRS	$\overline{CTS}$/$\overline{RTS}$ function select bit	Enabled when CRD is 0 0 : $\overline{CTS}$ function selected 1 : $\overline{RTS}$ function selected	RW
TXEPT	Transmit register empty flag	0 : Data present in transmit register (transmission in progress) 1 : No data present in transmit register (transmission completed)	RO
CRD	$\overline{CTS}$/$\overline{RTS}$ disable bit	0 : $\overline{CTS}$/$\overline{RTS}$ function enabled 1 : $\overline{CTS}$/$\overline{RTS}$ function disabled	RW
NCH	Data output select bit	0 : Pins TXDi/SDAi and SCLi are CMOS output 1 : Pins TXDi/SDAi and SCLi are N-channel open drain output	RW
CKPOL	CLK polarity select bit	0 : Transmit data is output at the falling edge of transmit/receive clock and receive data is input at the rising edge 1 : Transmit data is output at the rising edge of transmit/receive clock and receive data is input at the falling edge	RW
UFORM	Bit order select bit	0 : LSB first 1 : MSB first	RW

CLK1 to CLK0 (UiBRG count source select bit) (b1-b0)

When bits CLK1 to CLK0 are 00b (f1SIO or f2SIO selected), select f1SIO or f2SIO by the PCLK1 bit in the PCLKR register.
Set bits CLK1 to CLK0 after setting registers UCLKSEL0 and PCLKR.
If bits CLK1 to CLK0 are changed, set the UiBRG register.

CRD ($\overline{CTS}$/$\overline{RTS}$ disable bit) (b4)

When the CRD bit is 1 ($\overline{CTS}$/$\overline{RTS}$ function disabled), the $\overline{CTSi}$/$\overline{RTSi}$ pin can be used as an I/O port.
Set the CRD bit in the U4C0 register to 1 ($\overline{CTS}$/$\overline{RTS}$ function disabled).

NCH (Data output select bit) (b5)

When the clock synchronous serial I/O mode, the I^2C mode, or the UART mode is selected by setting the bits SMD2 to SMD0 in the UiMR register, the output method of pins TXDi/SDAi can be selected with the NCH bit. When bits SMD2 to SMD0 is 000b (serial interface disabled), the output method of pins TXDi/SDAi is CMOS.

When the IICM bit in the U2SMR register is 1 (I^2C mode) and bits SMD2 to SMD0 is 010b (I^2C mode), the output method of the SCL2 pin is N-channel open drain with the NCH bit set to 1. When the IICM bit is 0 (other than I^2C mode), or bits SMD2 to SMD0 is other than 010b, the output method of the SCL2 pin is CMOS.

This function is used to set the P-channel transistor of the CMOS output buffer always off, but not to change pins TXDi, SDA2 and SCL2 to open drain output completely.

Refer to the electrical characteristics for the input voltage range.

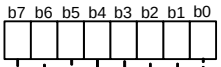
UFORM (Bit order select bit) (b7)

The UFORM bit is enabled when bits SMD2 to SMD0 in the UiMR register are 001b (clock synchronous serial I/O mode), or 101b (UART mode, 8-bit character data).

Set the UFORM bit to 1 when bits SMD2 to SMD0 are 010b (I^2C mode), and to 0 when bits SMD2 to SMD0 are 100b (UART mode, 7-bit character data) or 110b (UART mode, 9-bit character data).

21.2.7 UARTi Transmit/Receive Control Register 1 (UiC1) (i = 0 to 4)

UARTi Transmit/Receive Control Register 1 (i = 0 to 4)



Symbol	Address	Reset Value
U0C1, U1C1, U2C1 U4C1, U3C1	024Dh, 025Dh, 026Dh 029Dh, 02ADh	0000 0010b 0000 0010b

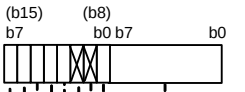
Bit symbol	Bit Name	Function	RW
TE	Transmit enable bit	0 : Transmission disabled 1 : Transmission enabled	RW
TI	Transmit buffer empty flag	0 : Data present in UiTB register 1 : No data present in UiTB register	RO
RE	Receive enable bit	0 : Reception disabled 1 : Reception enabled	RW
RI	Receive complete flag	0 : No data present in UiRB register 1 : Data present in UiRB register	RO
UilRS	UARTi transmit interrupt source select bit	0 : UiTB register empty (TI = 1) 1 : Transmission completed (TXEPT = 1)	RW
UiRRM	UARTi continuous receive mode enable bit	0 : Continuous receive mode disabled 1 : Continuous receive mode enabled	RW
UiLCH	Data logic select bit	0 : Not inverted 1 : Inverted	RW
UiERE	Error signal output enable bit	0 : Output disabled 1 : Output enabled	RW

UiLCH (Data logic select bit) (b6)

The UiLCH bit is enabled when bits SMD2 to SMD0 in the UiMR register are 001b (clock synchronous serial I/O mode), 100b (UART mode, 7-bit character), or 101b (UART mode, 8-bit character). Set this bit to 0 when bits SMD2 to SMD0 are set to 010b (I^2C mode) or 110b (UART mode, 9-bit character).

21.2.8 UARTi Receive Buffer Register (UiRB) (i = 0 to 4)

UARTi Receive Buffer Register (i = 0 to 4)



Symbol	Address	Reset Value
U0RB	024Fh to 024Eh	XXXXh
U1RB	025Fh to 025Eh	XXXXh
U2RB	026Fh to 026Eh	XXXXh
U4RB	029Fh to 029Eh	XXXXh
U3RB	02AFh to 02AEh	XXXXh

Bit Symbol	Bit Name	Function	RW
— (b7-b0)	——	Receive data (D7 to D0)	RO
— (b8)	——	Receive data (D8)	RO
— (b10-b9)	No register bits. If necessary, set to 0. The read value is undefined.		—
ABT	Arbitration lost detect flag	0 : Not detected 1 : Detected	RW
OER	Overrun error flag	0 : No overrun error 1 : Overrun error found	RO
FER	Framing error flag	0 : No framing error 1 : Framing error found	RO
PER	Parity error flag	0 : No parity error 1 : Parity error found	RO
SUM	Error sum flag	0 : No error 1 : Error found	RO

When bits SMD2 to SMD0 in the UiMR register are 100b, 101b, or 110b, read this register in 16-bit units, or in 8-bit units from upper byte to lower byte.
Bits FER and PER in the upper byte become 0 when the lower byte of the UiRB register is read.
If an overrun error occurs, the receive data of the UiRB register is undefined.

ABT (Arbitration lost detect flag) (b11)

The ABT bit is set to 0 by a program. (It remains unchanged even if 1 is written.)

OER (Overrun error flag) (b12)

Conditions to become 0:

- Bits SMD2 to SMD0 in the UiMR register are 000b (serial interface disabled).
- The RE bit in the UiC1 register is 0 (reception disabled).

Condition to become 1:

- The RI bit in the UiC1 register is 1 (data present in UiRB register), and the last bit of the next data is received.

FER (Framing error flag) (b13)

The FER bit is disabled when bits SMD2 to SMD0 are set to 001b (clock synchronous serial I/O mode) or to 010b (I^2C mode). The read value is undefined.

Conditions to become 0:

- Bits SMD2 to SMD0 in the UiMR register are 000b (serial interface disabled).
- The RE bit in the UiC1 register is 0 (reception disabled).
- The lower bytes of the UiRB register are read.

Condition to become 1:

- The set number of stop bits is not detected.
  (detected when the received data is transferred from the UARTi receive register to the UiRB register.)

PER (Parity error flag) (b14)

The PER bit is disabled when bits SMD2 to SMD0 are set to 001b (clock synchronous serial I/O mode) or to 010b (I^2C mode). The read value is undefined.

Conditions to become 0:

- Bits SMD2 to SMD0 in the UiMR register are 000b (serial interface disabled).
- The RE bit in the UiC1 register is 0 (reception disabled).
- The lower bytes of the UiRB register are read.

Condition to become 1:

- The number of 1's of the parity bit and character bits do not match the set value of the PRY bit in the UiMR register.
  (detected when the received data is transferred from the UARTi receive register to the UiRB register.)

SUM (Error sum flag) (b15)

The SUM bit is disabled when bits SMD2 to SMD0 are set to 001b (clock synchronous serial I/O mode) or to 010b (I^2C mode). The read value is undefined.

Conditions to become 0:

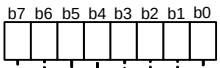
- Bits SMD2 to SMD0 in the UiMR register are 000b (serial interface disabled).
- The RE bit in the UiC1 register is 0 (reception disabled).
- Bits PER, FER and OER are all 0 (no error).

Condition to become 1:

- At least two bits out of PER, FER, or OER are 1 (error found).

21.2.9 UART2 Special Mode Register 4 (U2SMR4)

UART2 Special Mode Register 4



Symbol: U2SMR4 | Address: 0264h | Reset Value: 00h

Bit Symbol	Bit Name	Function	RW
STAREQ	Start condition generate bit	0 : Clear 1 : Start	RW
RSTAREQ	Restart condition generate bit	0 : Clear 1 : Start	RW
STPREQ	Stop condition generate bit	0 : Clear 1 : Start	RW
STSPSEL	SCL, SDA output select bit	0 : Select serial I/O circuit 1 : Select start condition/stop condition generate circuit	RW
ACKD	ACK data bit	0 : ACK 1 : NACK	RW
ACKC	ACK data output enable bit	0 : Serial data output 1 : ACK data output	RW
SCLHI	SCL output stop bit	If stop condition is detected, 0 : Do not stop SCL2 output 1 : Stop SCL2 output	RW
SWC9	SCL wait auto insert bit 3	0 : No wait-state/wait-state cleared 1 : Hold the SCL2 pin low after the ninth bit of the SCL2 is received	RW

STAREQ (Start condition generate bit) (b0)

The STAREQ bit becomes 0 when a start condition is generated.

This bit is used in master mode of I^2C mode. To set this bit to 1, preset the IICM bit in the U2SMR register to 1 (I^2C mode). Do not set this bit to 1 when the IICM bit is 0.

RSTAREQ (Restart condition generate bit) (b1)

The RSTAREQ bit becomes 0 when a restart condition is generated.

This bit is used in master mode of I^2C mode. To set this bit to 1, preset the IICM bit in the U2SMR register to 1 (I^2C mode). Do not set this bit to 1 when the IICM bit is 0.

STPREQ (Stop condition generate bit) (b2)

The STPREQ bit becomes 0 when a stop condition is generated.

This bit is used in master mode of I^2C mode. To set this bit to 1, preset the IICM bit in the U2SMR register to 1 (I^2C mode). Do not set this bit to 1 when the IICM bit is 0.

STSPSEL (SCL, SDA output select bit) (b3)

This bit is used in master mode of I^2C mode. To set this bit to 1, preset the IICM bit in the U2SMR register to 1 (I^2C mode). Do not set this bit to 1 when the IICM bit is 0.

Set the STSPSEL bit to 1 (select start condition/stop condition generate circuit) after setting the STARREQ, RSTAREQ, or STPREQ bit to 1 (start).

ACKD (ACK data bit) (b4)
ACKC (ACK data output enable bit) (b5)
SWC9 (SCL wait auto insert bit 3) (b7)

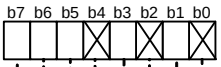
This bit is used in slave mode of I^2C mode. To set this bit to 1, preset the IICM bit in the U2SMR register to 1 (I^2C mode). Do not set this bit to 1 when the IICM bit is 0.

SCLHI (SCL output stop bit) (b6)

This bit is used in master mode of I^2C mode. To set this bit to 1, preset the IICM bit in the U2SMR register to 1 (I^2C mode). Do not set this bit to 1 when the IICM bit is 0.

21.2.10 UART2 Special Mode Register 3 (U2SMR3)

UART2 Special Mode Register 3



Symbol	Address	Reset Value
U2SMR3	0265h	000X 0X0Xb

Bit Symbol	Bit Name	Function	RW
— (b0)	No register bit. If necessary, set to 0. The read value is undefined.		—
CKPH	Clock phase set bit	0 : No clock delay 1 : With clock delay	RW
— (b2)	No register bit. If necessary, set to 0. The read value is undefined.		—
NODC	Clock output select bit	0 : CLK2 is CMOS output 1 : CLK2 is N-channel open drain output	RW
— (b4)	No register bit. If necessary, set to 0. The read value is undefined.		—
DL0	SDA2 digital delay setup bit	b7 b6 b5 0 0 0 : No delay 0 0 1 : 1 to 2 cycles of U2BRG count source 0 1 0 : 2 to 3 cycles of U2BRG count source 0 1 1 : 3 to 4 cycles of U2BRG count source 1 0 0 : 4 to 5 cycles of U2BRG count source 1 0 1 : 5 to 6 cycles of U2BRG count source 1 1 0 : 6 to 7 cycles of U2BRG count source 1 1 1 : 7 to 8 cycles of U2BRG count source	RW
DL1			RW
DL2			RW

NODC (Clock output select bit) (b3)

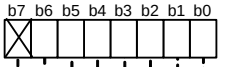
This function is used to set P-channel transistor of the CMOS output buffer always off, but not to change the CLK2 pin to open drain output completely.
Refer to the electrical characteristics for the input voltage range.

DL2-DL0 (SDA2 digital delay setup bit) (b7-b5)

Bits DL2 to DL0 are used to generate a digital delay in SDA2 output in I^2C mode. Except in I^2C mode, set these bits to 000b (no delay).
The delay length varies with the load on pins SCL2 and SDA2. Also, when using an external clock, the delay length increases by about 100 ns.

21.2.11 UART2 Special Mode Register 2 (U2SMR2)

UART2 Special Mode Register 2



Symbol	Address	Reset Value
U2SMR2	0266h	X000 0000b

Bit Symbol	Bit Name	Function	RW
IICM2	I^2C mode select bit 2	0 : Use NACK/ACK interrupt 1 : Use transmit/receive interrupt	RW
CSC	Clock synchronization bit	0 : Clock synchronization disabled 1 : Clock synchronization enabled	RW
SWC	SCL wait auto insert bit	0 : No wait-state/wait-state cleared 1 : Hold the SCL2 pin low after the eighth bit is received	RW
ALS	SDA output auto stop bit	When arbitration lost is detected, 0 : Do not stop the SDA2 output 1 : Stop the SDA2 output	RW
STAC	UART2 auto initialize bit	When the start condition is detected, 0 : Do not initialize the circuit 1 : Initialize the circuit	RW
SWC2	SCL wait output bit 2	0: Output the transmit/receive clock at the SCL2 pin 1: Hold the SCL2 pin low	RW
SDHI	SDA output disable bit	0: Output data 1: Stop the output (high-impedance)	RW
— (b7)	No register bit. If necessary, set to 0. The read value is undefined.		—

21.2.12 UART2 Special Mode Register (U2SMR)

UART2 Special Mode Register

b7	b6	b5	b4	b3	b2	b1	b0
X				0			

Symbol	Address	Reset Value
U2SMR	0267h	X000 0000b

Bit Symbol	Bit Name	Function	RW
IICM	I^2C mode select bit	0 : Other than I^2C mode 1 : I^2C mode	RW
ABC	Arbitration lost detect flag control bit	0 : Update every bit 1 : Update every byte	RW
BBS	Bus busy flag	0 : Stop-condition detected 1 : Start-condition detected (busy)	RW
— (b3)	Reserved bit	Set to 0	RW
ABSCS	Bus collision detect sampling clock select bit	0 : Rising edge of transmit/receive clock 1 : Underflow signal of timer A0	RW
ACSE	Auto clear function select bit of transmit enable bit	0 : No auto clear function 1 : Auto clear at bus collision	RW
SSS	Transmit start condition select bit	0 : Not synchronized to RXD2 1 : Synchronized to RXD2	RW
— (b7)	No register bit. If necessary, set to 0. Read as undefined value		—

BBS (Bus busy flag) (b2)

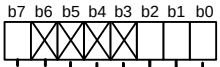
The BBS bit is set to 0 by a program. (It remains unchanged even if 1 is written.)

SSS (Transmit start condition select bit) (b6)

When a transmission starts, the SSS bit becomes 0 (not synchronized to RXD2).

21.2.13 Pin Assignment Control Register (PACR)

Pin Assignment Control Register



Symbol	Address	Reset Value
PACR	0370h	0XXXX000b

Bit Symbol	Bit Name	Function	RW
PACR0	Pin enable bit	b2 b1 b0 0 1 0: 64-pin version 0 1 1: 80-pin version 1 0 0: 100-pin version Only set the values listed above.	RW
PACR1			RW
PACR2			RW
— (b6-b3)	No register bits. If necessary, set to 0. The read value is undefined.		—
U1MAP	UART1 pin remapping bit	UART1 pin assigned to: 0: P6_7 to P6_4 1: P7_3 to P7_0	RW

Write to the PACR register in the next instruction after setting the PRC2 bit in the PRCR register to 1 (write enabled).

21.3 Operations

21.3.1 Clock Synchronous Serial I/O Mode

The clock synchronous serial I/O mode uses a transmit/receive clock to transmit/receive data. Table 21.5 lists the Clock Synchronous Serial I/O Mode Specifications.

Table 21.5 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Data format	Character length: 8 bits
Transmit/receive clock	• CKDIR bit in the UiMR register = 0 (internal clock): $\frac{fj}{2(n+1)}$ fj = f1SIO, f2SIO, f8SIO, f32SIO n = setting value of UiBRG register (00h to FFh) • CKDIR bit = 1 (external clock): input from CLKi pin
Transmit/receive control	Selectable from $\overline{CTS}$, $\overline{RTS}$, or $\overline{CTS}/\overline{RTS}$ function disabled (UART0 to UART3)
Transmission start conditions	To start transmission, satisfy the following requirements (1) • The TE bit in the UiC1 register is 1 (transmission enabled) • The TI bit in the UiC1 register is 0 (data presents in UiTB register) • When $\overline{CTS}$ function is selected, input on the $\overline{CTSi}$ pin is low
Reception start conditions	To start reception, satisfy the following requirements (1) • The RE bit in the UiC1 register is 1 (reception enabled) • The TE bit in the UiC1 register is 1 (transmission enabled) • The TI bit in the UiC1 register is 0 (data presents in the UiTB register)
Interrupt request generation timing	For transmission, one of the following conditions can be selected • The UiIRS bit in the UiC1 register is 0 (transmit buffer empty): When transferring data from the UiTB register to the UARTi transmit register (at start of transmission) • The UiIRS bit is 1 (transfer completed): When the serial interface completes sending data from the UARTi transmit register For reception • When transferring data from the UARTi receive register to the UiRB register (at completion of reception)
Error detection	Overrun error (2) This error occurs if the serial interface starts receiving the next unit of data before reading the UiRB register and receiving the seventh bit of the next unit of data
Selectable functions	• CLK polarity selection Data input/output can be selected to occur synchronously with the rising or falling edge of the transmit/receive clock • LSB first, MSB first selection Whether to start transmitting/receiving the data from bit 0 or from bit 7 can be selected • Continuous receive mode selection Reception is enabled immediately by reading the UiRB register • Switching serial data logic This function inverts the logic value of the transmit/receive data

i = 0 to 4

Notes:

1. These requirements do not have to be set in any particular order. If transmission/reception is started while an external clock is selected and the TXEPT bit in the UiC0 register is 1 (no data present in transmit register), meet the last requirement at either of the following timings:
   - The CKPOL bit in the UiC0 register is 0 (transmit data is output at the falling edge of transmit/receive clock and receive data is input at the rising edge) and the external clock is high.
   - The CKPOL bit is 1 (transmit data is output at the rising edge of transmit/receive clock and receive data is input at the falling edge) and the external clock is low.
2. If an overrun error occurs, the receive data of the UiRB register will be undefined. The IR bit in the SiRIC register remains unchanged.

Table 21.6 lists Pin Functions in Clock Synchronous Serial I/O Mode.
Note that for a period from when UARTi operating mode is selected to when transmission starts, the TXDi pin outputs a high-level signal. (If N-channel open drain output is selected, this pin is high-impedance.)

Table 21.6 Pin Functions in Clock Synchronous Serial I/O Mode

Pin Name	I/O	Function	Method of Selection
TXDi	Output	Serial data output	(Outputs dummy data only when receiving)
RXDi	Input	Serial data input	Set the port direction bit sharing pin to 0.
	Input	Input port	Set the port direction bit sharing pin to 0. (can be used as an input port only when transmitting)
CLKi	Output	Transmit/receive clock output	The CKDIR bit in the UiMR register = 0
	Input	Transmit/receive clock input	The CKDIR bit in the UiMR register = 1 Set the port direction bit sharing pin to 0.
$\overline{\text{CTSi}}$/$\overline{\text{RTSi}}$	Input	$\overline{\text{CTS}}$ input	The CRD bit in the UiC0 register = 0 The CRS bit in the UiC0 register = 0 Set the port direction bit sharing pin to 0.
	Output	$\overline{\text{RTS}}$ output	The CRD bit in the UiC0 register = 0 The CRS bit in the UiC0 register = 1
	I/O	I/O port	The CRD bit in the UiC0 register = 1

i = 0 to 4

Note:

1. The CTS/RTS pin is not available for UART4.

Table 21.7 Registers Used and Settings in Clock Synchronous Serial I/O Mode (1)

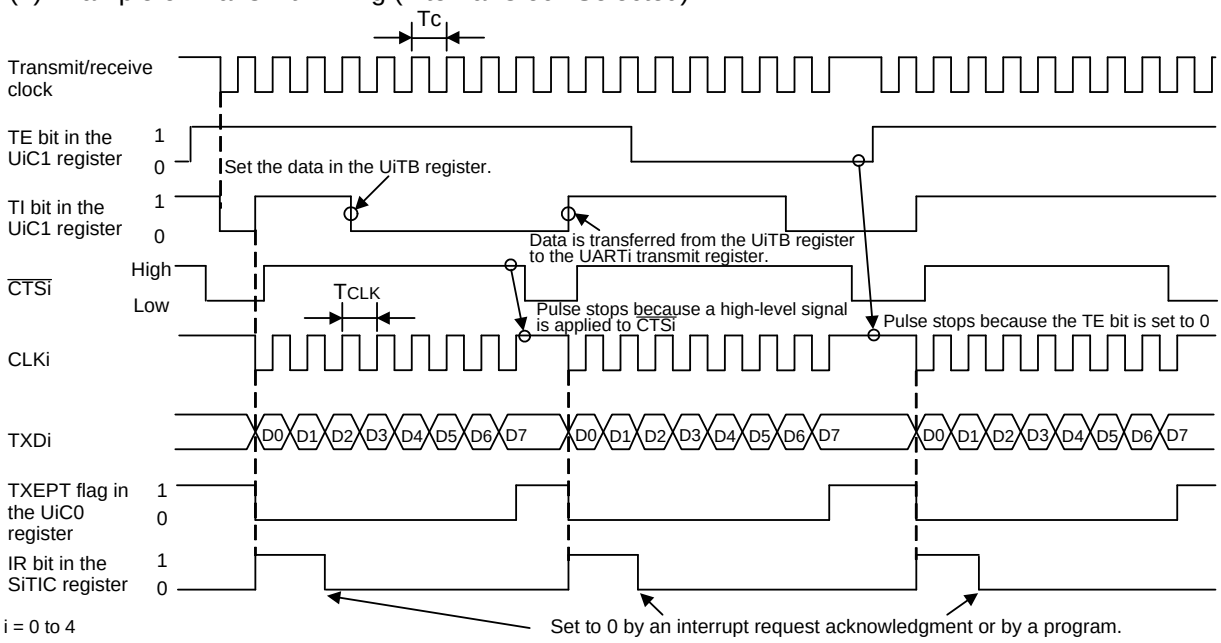
Register	Bits	Function
UCLKSEL0	OCOSEL0	Select clock prior to division for UART0 to UART2.
	OCOSEL1	Select clock prior to division for UART3 to UART4.
PCLKR	PCLK1	Select the count source for the UiBRG register.
UiTB	0 to 7	Set transmission data.
	8	- (does not need to be set) If necessary, set to 0.
UiRB	0 to 7	Reception data can be read.
	8, 11, 13 to 15	When read, the read value is undefined.
	OER	Overrun error flag
UiBRG	0 to 7	Set bit rate.
UiMR	SMD2 to SMD0	Set to 001b.
	CKDIR	Select internal clock or external clock.
	4 to 6	Set to 0.
	IOPOL	Set to 0.
UiC0	CLK1 to CLK0	Select the count source for the UiBRG register.
	CRS	If $\overline{CTS}$ or $\overline{RTS}$ is used, select which function to use.
	TXEPT	Transmit register empty flag
	CRD	Enable or disable the $\overline{CTS}$ or $\overline{RTS}$ function. Set this bit to 1 (disabled) when using UART4.
	NCH	Select TXDi pin output mode.
	CKPOL	Select the transmit/receive clock polarity.
	UFORM	Select LSB first or MSB first.
UiC1	TE	Set to 1 to enable transmission/reception.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	UiIRS	Select source of UARTi transmit interrupt.
	UiRRM	Set to 1 to use continuous receive mode.
	UiLCH	Set to 1 to use inverted data logic.
	UiERE	Set to 0.
U2SMR (2)	0 to 7	Set to 0.
U2SMR2 (2)	0 to 7	Set to 0.
U2SMR3 (2)	0 to 2	Set to 0.
	NODC	Select clock output mode.
	4 to 7	Set to 0.
U2SMR4 (2)	0 to 7	Set to 0.

i = 0 to 4

Notes:

1. This table does not describe a procedure.
2. In case of UART2

(1) Example of Transmit Timing (Internal Clock Selected)



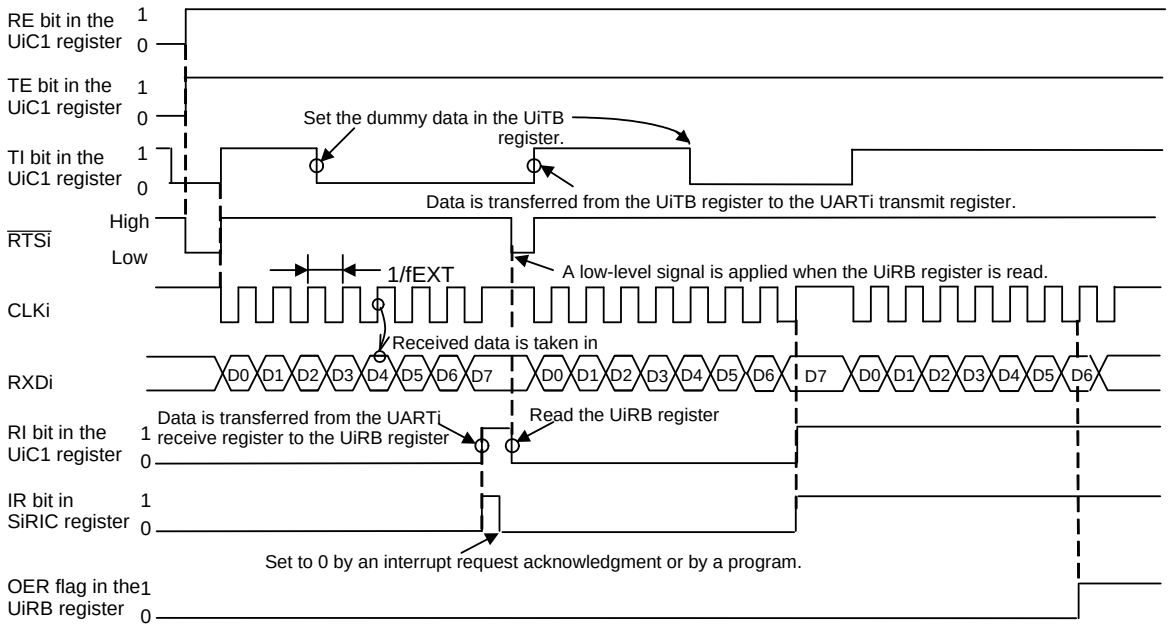
i = 0 to 4

The above assumes the following:
- The CKDIR bit in the UiMR register is 0 (internal clock).
- The CRD bit in the UiC0 register is 0 ($\overline{CTS}/\overline{RTS}$ enabled), the CRS bit is 0 ($\overline{CTS}$ selected).
- The CKPOL bit in the UiC0 register is 0 (transmit data output at the falling edge and receive data taken in at the rising edge of the transmit/receive clock).
- The UiIRS bit in the UiC1 register is 0 (an interrupt request occurs when the UiTB register becomes empty).

$T_C = T_{CLK} = 2(n + 1)/fj$

fj: Frequency of UiBRG count source (f1SIO, f2SIO, f8SIO, f32SIO)
n: Value set to the UiBRG register

(2) Example of Receive Timing (External Clock Selected)



i = 0 to 4

The above assumes the following:
- The CKDIR bit in the UiMR register is 1 (external clock).
- The CRD bit in the UiC0 register is 0 ($\overline{CTS}/\overline{RTS}$ enabled), the CRS bit is 1 ($\overline{RTS}$ selected).
- The CKPOL bit in the UiC0 register is 0 (transmit data output at the falling edge and receive data taken in at the rising edge of the transmit/receive clock).

fEXT: Frequency of the external clock

Make sure the following conditions are met when input to the CLKi pin before receiving data is high:
- The TE bit in the UiC1 register = 1 (transmit enabled)
- The RE bit in the UiC1 register = 1 (receive enabled)
- Write dummy data to the UiTB register

Figure 21.3 Transmit and Receive Operation during Clock Synchronous Serial I/O Mode

21.3.1.1 CLK Polarity Select Function

Use the CKPOL bit in the UiC0 register (i = 0 to 4) to select the transmit/receive clock polarity. Figure 21.4 shows the Transmit/Receive Clock Polarity.

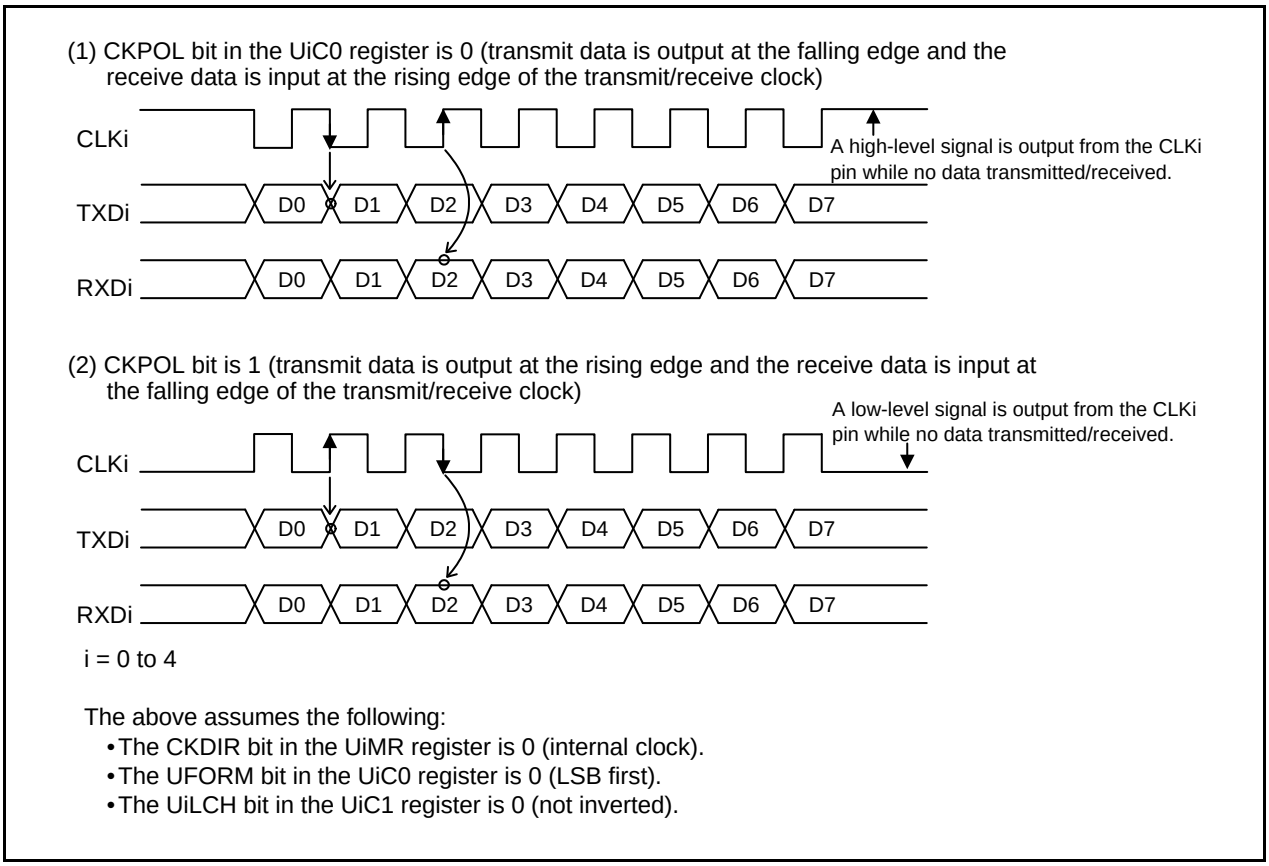
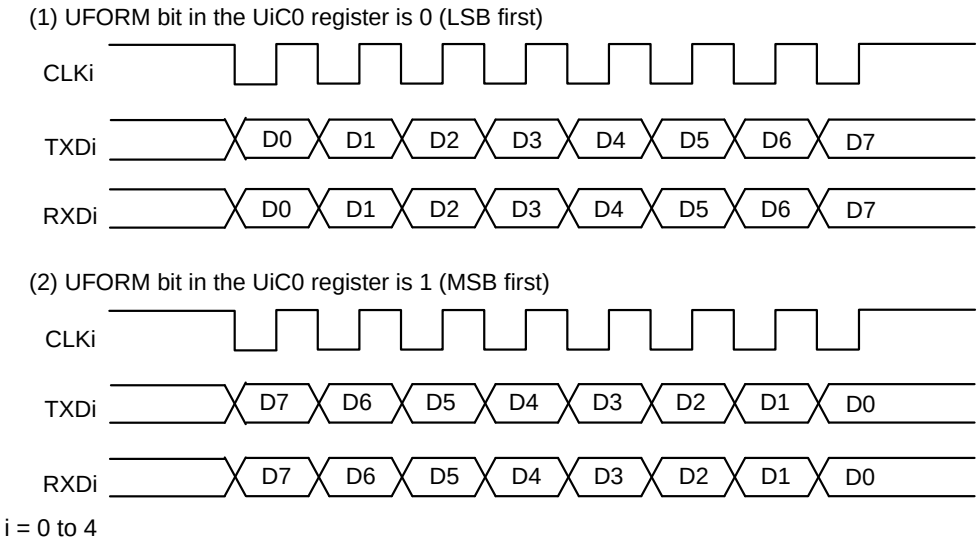


Figure 21.4 Transmit/Receive Clock Polarity

21.3.1.2 LSB First/MSB First Select Function

Use the UFORM bit in the UiC0 register (i = 0 to 4) to select the bit order. Figure 21.5 shows the Bit Order.



The above assumes the following:

- The CKPOL bit in the UiC0 register is 0 (transmit data is output at the falling edge and the receive data is input at the rising edge of the transmit/receive clock).
- The UiLCH bit in the UiC1 register is 0 (not inverted).

Figure 21.5 Bit Order

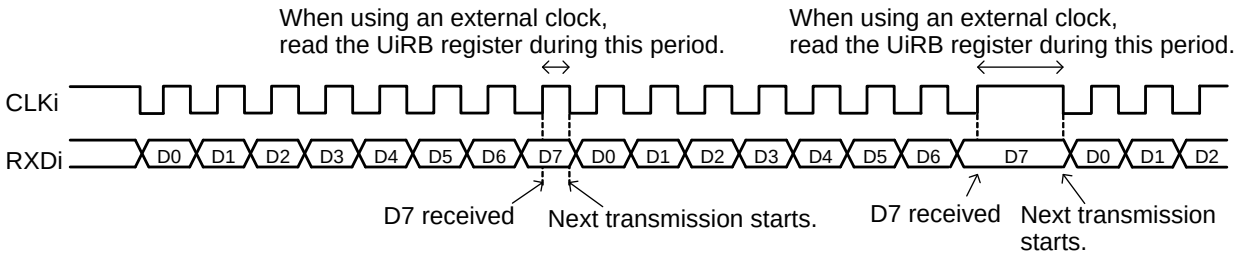
21.3.1.3 Continuous Receive Mode

In continuous receive mode, the receive operation is enabled when the receive buffer register is read. Thus, a dummy write to the transmit buffer register to enable the receive operation is unnecessary in this mode. However, a dummy read of the receive buffer register is required when start receiving.

When setting the UiRRM bit in the UiC1 (i = 0 to 4) to 1 (continuous receive mode), the TI bit in the UiC1 register is set to 0 (data present in the UiTB register) by reading the UiRB register. When the UiRRM bit is 1, do not write dummy data to the UiTB register by a program.

When using an external clock, read the UiRB register between receiving the eighth bit of data and starting the next transmission.

Figure 21.6 shows Operation Example in Continuous Receive Mode.



i = 0 to 4

The above diagram assumes the following:

- The CKPOL bit in the UiC0 register is 0 (receive data input at the rising edge of the transmit/receive clock).
- The UFORM bit in the UiC0 register is 0 (LSB first).
- The CKDIR bit in the UiMR register is 1 (external clock).

Figure 21.6 Operation Example in Continuous Receive Mode

21.3.1.4 Serial Data Logic Switching Function

When the UiLCH bit in the UiC1 register (i = 0 to 4) is 1 (inverted), the data written to the UiTB register has its logic inverted before being transmitted. Similarly, the inverted data has its logic inverted when read from the UiRB register. Figure 21.7 shows Serial Data Logic.

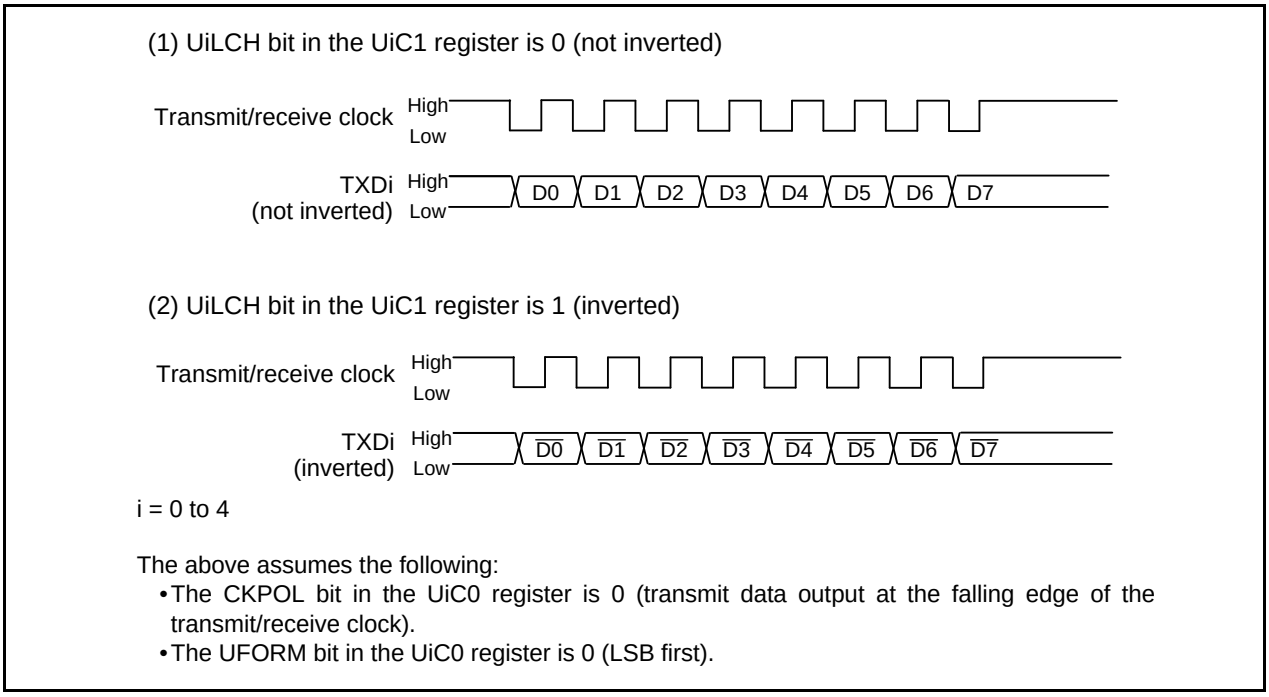


Figure 21.7 Serial Data Logic

21.3.1.5 $\overline{\text{CTS}}/\overline{\text{RTS}}$ Function

The $\overline{\text{CTS}}$ function is used to start transmit/receive operation when a low signal is applied to the $\overline{\text{CTS}}$i/$\overline{\text{RTS}}$i (i = 0 to 3) pin. Transmit/receive operation begins when input to the $\overline{\text{CTS}}$i/$\overline{\text{RTS}}$i pin becomes low. If the low signal is switched to high during a transmit or receive operation, the operation stops before the next data.

For the $\overline{\text{RTS}}$ function, the $\overline{\text{CTS}}$i/$\overline{\text{RTS}}$i pin outputs a low signal when the MCU is ready to receive. The output level becomes high at the detection of the start bit.

See Table 21.6 “Pin Functions in Clock Synchronous Serial I/O Mode”.

21.3.1.6 Processing When Terminating Communication or When an Error Occurs

When communication is terminated in clock synchronous serial I/O mode, or when a communication error occurs, use the following procedure to reset communication:

(1) Set the TE bit in the UiC1 (i = 0 to 4) register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the UiMR register to 001b (clock synchronous serial I/O mode).
(4) Set the TE bit in the UiC1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

21.3.2 Clock Asynchronous Serial I/O (UART) Mode

The UART mode allows data to be transmitted/received after setting the desired bit rate and bit order. Table 21.8 lists the UART Mode Specifications.

Table 21.8 UART Mode Specifications

Item	Specification
Data format	• Character bit: selectable from 7, 8, or 9 bits • Start bit: 1 bit • Parity bit: selectable from odd, even, or none • Stop bit: selectable from 1 bit or 2 bits
Transmit/receive clock	• The CKDIR bit in the UiMR register = 0 (internal clock): $\frac{fj}{16(n+1)}$ fj = f1SIO, f2SIO, f8SIO, f32SIO n: Setting value of UiBRG register 00h to FFh • CKDIR bit = 1 (external clock): $\frac{fEXT}{16(n+1)}$ fEXT: Input from CLKi pin n: Setting value of UiBRG register 00h to FFh
Transmit/receive control	Selectable from $\overline{CTS}$, $\overline{RTS}$, or $\overline{CTS}$/$\overline{RTS}$ function disabled (UART0 to UART3)
Transmission start conditions	To start transmission, satisfy the following requirements: • The TE bit in the UiC1 register is 1 (transmission enabled) • The TI bit in the UiC1 register is 0 (data present in the UiTB register) • If $\overline{CTS}$ function is selected, input on the $\overline{CTSi}$ pin = low
Reception start conditions	To start reception, satisfy the following requirements: • The RE bit in the UiC1 register is 1 (reception enabled) • Start bit detection
Interrupt request generation timing	For transmission, one of the following conditions can be selected: • The UiIRS bit in the UiC1 register is 0 (transmit buffer empty): When transferring data from the UiTB register to the UARTi transmit register (at start of transmission) • The UiIRS bit is 1 (transmission completed): When the serial interface completes sending data from the UARTi transmit register For reception: • When transferring data from the UARTi receive register to the UiRB register (at completion of reception)
Error detection	• Overrun error (1) This error occurs if the serial interface starts receiving the next unit of data before reading the UiRB register and receives the bit before the last stop bit of the next unit of data. • Framing error This error occurs when the number of stop bits set is not detected. • Parity error This error occurs when the number of 1's of the parity bit and character bit does not match the set value of the PRY bit in the UiMR register. • Error sum flag This flag becomes 1 when any of the overrun, framing, or parity errors occur.
Selectable functions	• LSB first, MSB first selection Whether to start transmitting/receiving the data from bit 0 or from bit 7 can be selected. • Serial data logic switch This function inverts the logic of the transmit/receive data. The start and stop bits are not inverted. • TXD, RXD I/O polarity switch This function inverts the polarities of the TXD pin output and RXD pin input. The logic levels of all I/O data are inverted.

i = 0 to 4

Note:

1. If an overrun error occurs, the receive data of the UiRB register will be undefined. The IR bit in the SiRIC register remains unchanged.

Table 21.9 lists I/O Pin Functions in UART Mode. Note that for a period from when the UARTi operating mode is selected to when transmission starts, the TXDi pin outputs a high-level signal. (If N-channel open drain output is selected, this pin becomes high-impedance.)

Table 21.9 I/O Pin Functions in UART Mode

Pin Name	I/O	Function	Method of Selection
TXDi	Output	Serial data output	(High-level output only when receiving.)
RXDi	Input	Serial data input	Set the port direction bit sharing pin to 0.
CLKi	I/O	Input/output port	The CKDIR bit in the UiMR register = 0
	Input	Transmit/receive clock input	The CKDIR bit in the UiMR register = 1 Set the port direction bit sharing pin to 0.
$\overline{\text{CTS}}$i/$\overline{\text{RTS}}$i (1)	Input	$\overline{\text{CTS}}$ input	The CRD bit in the UiC0 register = 0 The CRS bit in the UiC0 register = 0 Set the port direction bit sharing pin to 0.
	Output	$\overline{\text{RTS}}$ output	The CRD bit in the UiC0 register = 0 The CRS bit in the UiC0 register = 1
	I/O	I/O port	The CRD bit in the UiC0 register = 1

i = 0 to 4

Note:

1. The $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ pin is not available for UART4.

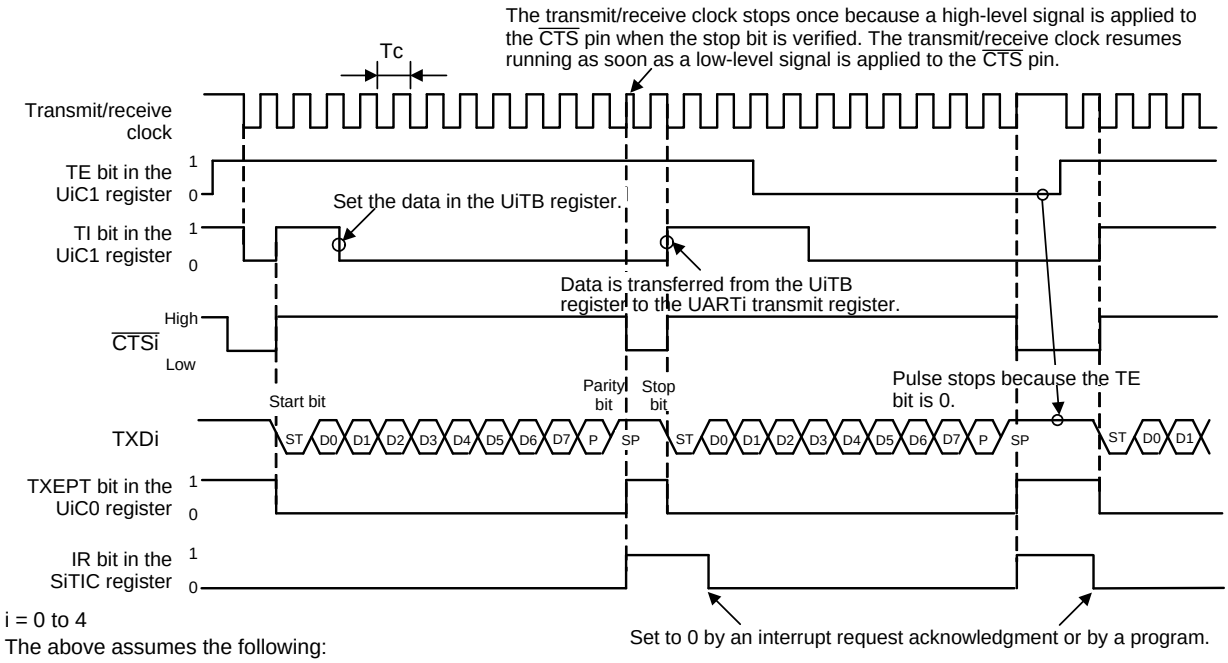
Table 21.10 Registers Used and Settings in UART Mode (1)

Register	Bits	Function
UCLKSEL0	OCOSEL0	Select clock prior to division for UART0 to UART2.
	OCOSEL1	Select clock prior to division for UART3 to UART4.
PCLKR	PCLK1	Select the count source for the UiBRG register.
UiTB	0 to 8	Set transmission data. (2)
UiRB	0 to 8	Reception data can be read. (2, 4)
	OER, FER, PER, SUM	Error flag
	11	When read, the read value is undefined.
UiBRG	0 to 7	Set bit rate.
UiMR	SMD2 to SMD0	Set to 100b when character bit length is 7 bits.
		Set to 101b when character bit length is 8 bits.
		Set to 110b when character bit length is 9 bits.
	CKDIR	Select the internal clock or external clock.
	STPS	Select number of stop bits.
	PRY, PRYE	Select whether parity is included and whether odd or even.
	IOPOL	Select the TXD/RXD input/output polarity.
UiC0	CLK0, CLK1	Select the count source for the UiBRG register.
	CRS	If $\overline{CTS}$ or $\overline{RTS}$ is used, select which function to use.
	TXEPT	Transmit register empty flag
	CRD	Enable or disable the $\overline{CTS}$ or $\overline{RTS}$ function. Set this bit to 1 (disabled) when using UART4.
	NCH	Select TXDi pin output mode.
	CKPOL	Set to 0.
	UFORM	LSB first or MSB first can be selected when character bit length is 8 bits. Set to 0 when character bit length is 7 or 9 bits.
UiC1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	UiIRS	Select source of UARTi transmit interrupt.
	UiRRM	Set to 0.
	UiLCH	Set to 1 to use reversed data logic.
	UiERE	Set to 0.
U2SMR (3)	0 to 7	Set to 0.
U2SMR2 (3)	0 to 7	Set to 0.
U2SMR3 (3)	0 to 7	Set to 0.
U2SMR4 (3)	0 to 7	Set to 0.

i = 0 to 4

Notes:
1. This table does not describe a procedure.
2. The bits used for transmit/receive data are as follows: Bits 0 to 6 when character bit length is 7 bits; bits 0 to 7 when character bit length is 8 bits; bits 0 to 8 when character bit length is 9 bits.
3. In case of UART2.
4. The values of bits 7 and 8 are undefined when character bit length is 7 bits.
   The values of bit 8 is undefined when character bit length is 8 bits.

(1) 8-bit Data Transmit Timing (with a Parity Bit and 1 Stop Bit)



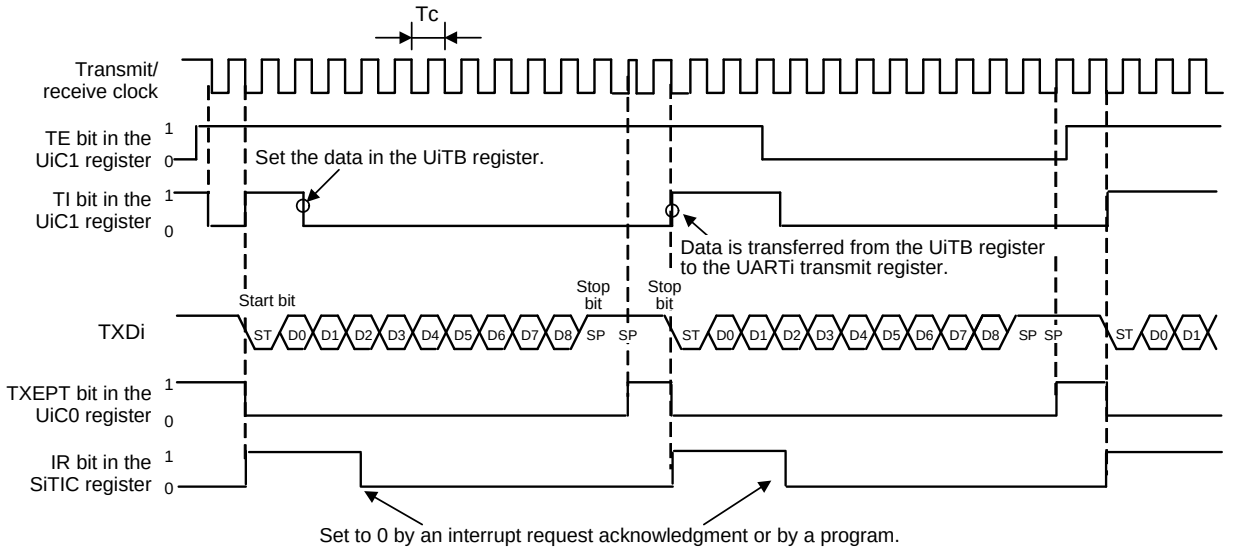
i = 0 to 4

The above assumes the following:

- The PRYE bit in the UiMR register is 1 (parity enabled).
- The STPS bit in the UiMR register is 0 (1 stop bit).
- The CRD bit in the UiC0 register is 0 (CTS/RTS enabled)
- The CRS bit in the UiC0 register is 0 (CTS selected).
- The UiIRS bit in the UiC1 register is 1
  (an interrupt request occurs when transmit completed)

Tc = 16(n + 1)/fj or 16(n + 1)/fEXT
fj: Frequency of UiBRG count source (f1SIO, f2SIO, f8SIO, f32SIO)
fEXT: Frequency of UiBRG count source (external clock)
n: Value set to UiBRG

(2) 9-bit Data Transmit Timing (with No Parity Bit and 2 Stop Bits)



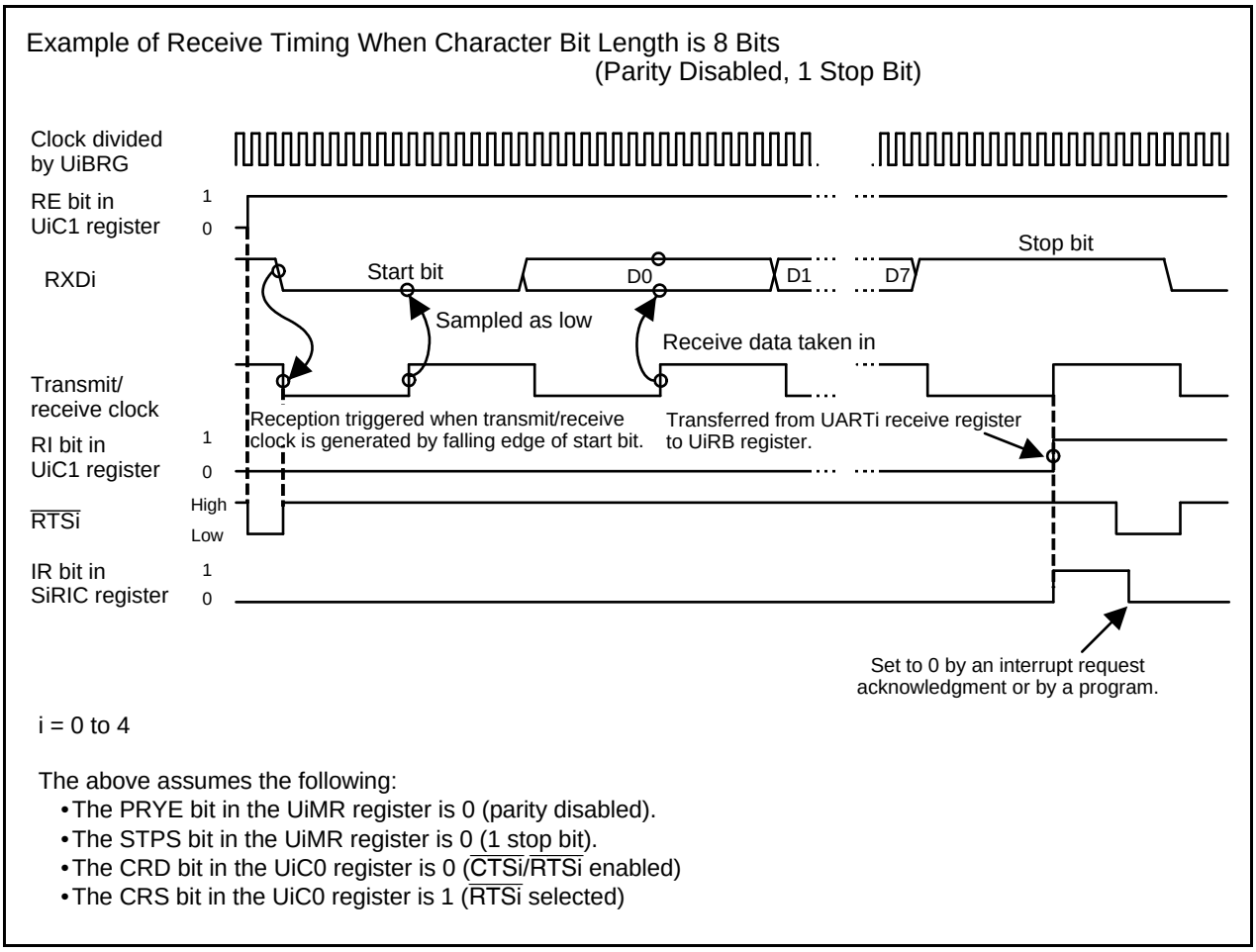
i = 0 to 4

The above assumes the following:

- The PRYE bit in the UiMR register is 0 (parity disabled).
- The STPS bit in the UiMR register is 1 (two stop bit).
- The CRD bit in the UiC0 register is 1 (CTS/RTS disabled)
- The UiIRS bit in the UiC1 register is 0
  (an interrupt request occurs when transmit buffer becomes empty)

TC = 16(n + 1)/fj or 16(n + 1)/fEXT
fj: Frequency of UiBRG count source (f1SIO, f2SIO, f8SIO, f32SIO)
fEXT: Frequency of UiBRG count source (external clock)
n: Value set to UiBRG

Figure 21.8 Transmit Timing in UART Mode



i = 0 to 4

The above assumes the following:

- The PRYE bit in the UiMR register is 0 (parity disabled).
- The STPS bit in the UiMR register is 0 (1 stop bit).
- The CRD bit in the UiC0 register is 0 ($\overline{\text{CTSi}}$/$\overline{\text{RTSi}}$ enabled)
- The CRS bit in the UiC0 register is 1 ($\overline{\text{RTSi}}$ selected)

Figure 21.9 Receive Timing in UART Mode

21.3.2.1 Bit Rate

In UART mode, the frequency set by the UiBRG register (i = 0 to 4) divided by 16 becomes a bit rate.

The setting value (n) of the UiBRG register is calculated by the following formula:

$$n = \frac{fj}{bitrate(bps) \times 16} - 1$$

fj = f1SIO, f2SIO, f8SIO, f32SIO

n = 00h to FFh

Table 21.11 lists Example Bit Rates and Settings.

Table 21.11 Example of Bit Rates and Settings (1)

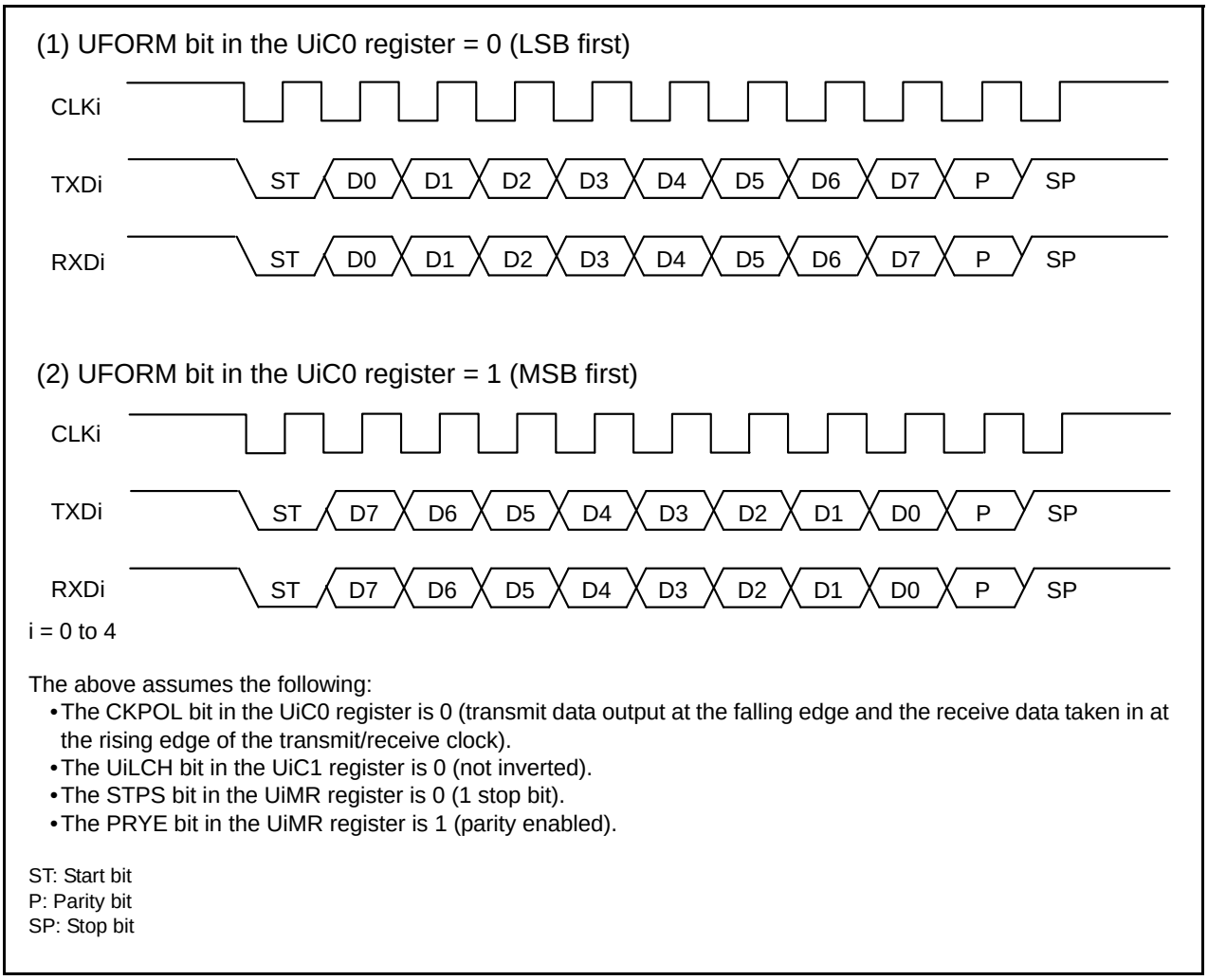
Bit Rate (bps)	Count Source of UiBRG	Peripheral Function Clock f1: 16 MHz		Peripheral Function Clock f1: 24 MHz	
		Set Value of UiBRG: n	Bit Rate (bps)	Set value of UiBRG: n	Bit Rate (bps)
1200	f8SIO	103 (67h)	1202	155 (9Bh)	1202
2400	f8SIO	51 (33h)	2404	77 (4Dh)	2404
4800	f8SIO	25 (19h)	4808	38 (26h)	4808
9600	f1SIO	103 (67h)	9615	155 (9Bh)	9615
14400	f1SIO	68 (44h)	14493	103 (67h)	14423
19200	f1SIO	51 (33h)	19231	77 (4Dh)	19231
28800	f1SIO	34 (22h)	28571	51 (33h)	28846
31250	f1SIO	31 (1Fh)	31250	47 (2Fh)	31250
38400	f1SIO	25 (19h)	38462	38 (26h)	38462
51200	f1SIO	19 (13h)	50000	28 (1Ch)	51724

Note:

1. Assumed that either the OCOSEL0 bit or OCOSEL1 bit in the UCLKSEL0 register is 0 (f1).

21.3.2.2 LSB First/MSB First Select Function

As shown in Figure 21.10, the bit order can be selected by setting the UFORM bit in the UiC0 register. This function is enabled when the character bit length is 8 bits.



i = 0 to 4

The above assumes the following:

- The CKPOL bit in the UiC0 register is 0 (transmit data output at the falling edge and the receive data taken in at the rising edge of the transmit/receive clock).
- The UiLCH bit in the UiC1 register is 0 (not inverted).
- The STPS bit in the UiMR register is 0 (1 stop bit).
- The PRYE bit in the UiMR register is 1 (parity enabled).

ST: Start bit
P: Parity bit
SP: Stop bit

Figure 21.10 Bit Order

21.3.2.3 Serial Data Logic Switching Function

The logic of the data written to the UiTB register is inverted and then transmitted. Similarly, the inverted logic of the received data is read when the UiRB register is read.

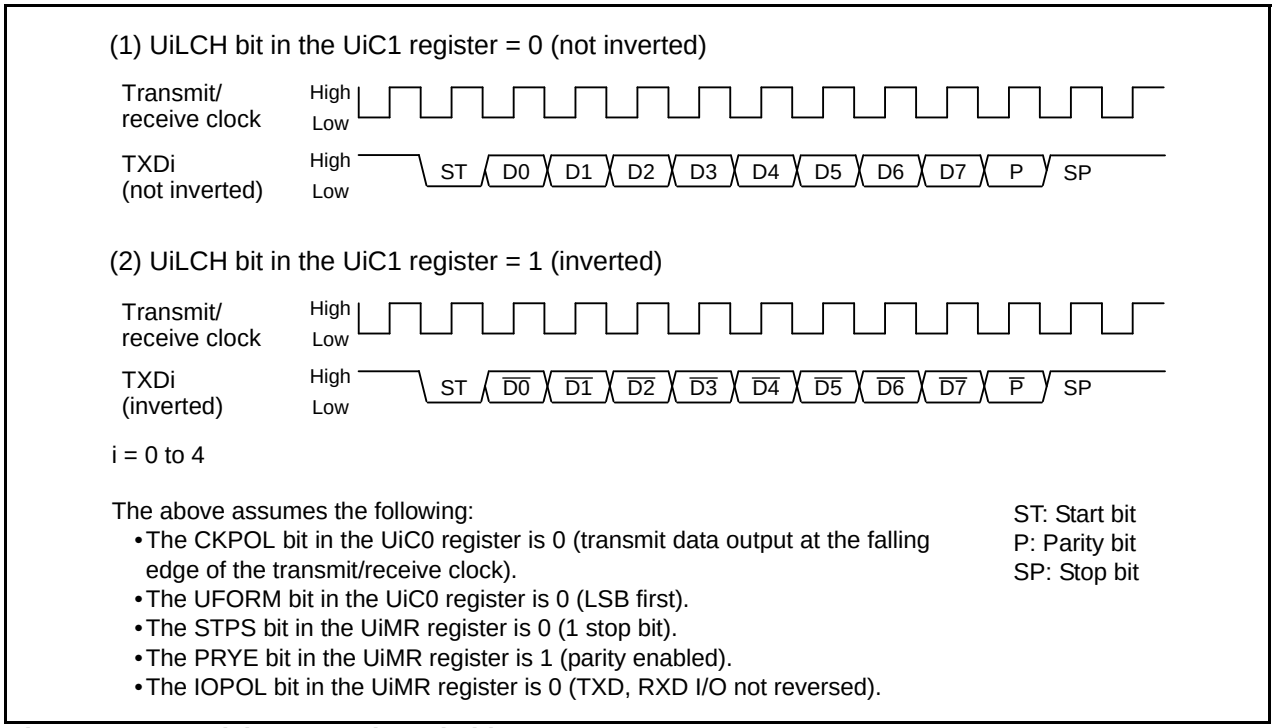


Figure 21.11 Serial Data Logic Switching

21.3.2.4 TXD and RXD I/O Polarity Reverse Function

This function reverses the polarities of the TXDi pin output and RXDi pin input. The logic levels of all I/O data (including bits for start, stop, and parity) are inverted.

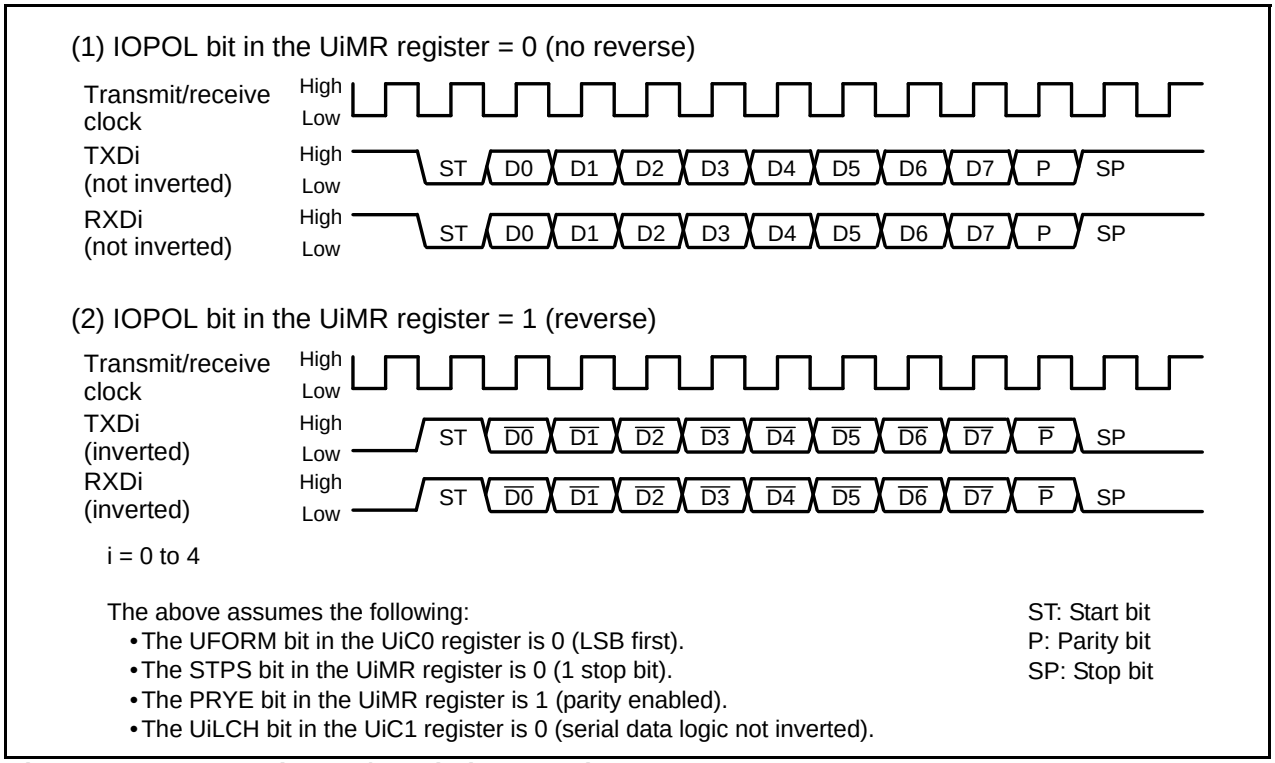


Figure 21.12 TXD and RXD I/O Polarity Inversion

21.3.2.5 $\overline{\text{CTS}}/\overline{\text{RTS}}$ Function

The $\overline{\text{CTS}}$ function is used to start transmit operation when a low signal is applied to the $\overline{\text{CTSi}}/\overline{\text{RTSi}}$ (i = 0 to 3) pin. Transmit operation begins when input to the $\overline{\text{CTSi}}/\overline{\text{RTSi}}$ pin becomes low. If the input level is switched from low to high during transmit operation, the operation stops after the ongoing transmit/receive operation is completed.

When the $\overline{\text{RTS}}$ function is selected, the $\overline{\text{CTSi}}/\overline{\text{RTSi}}$ pin outputs a low signal when the MCU is ready to receive. The output level becomes high when a start bit is detected.

See Table 21.9 “I/O Pin Functions in UART Mode”.

21.3.2.6 Processing When Terminating Communication or When an Error Occurs

If communication is terminated in UART mode, or a communication error occurs, use following procedure reset communication:

(1) Set the TE bit in the UiC1 (i = 0 to 4) register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the UiMR register to 100b (UART mode character bit length is 7 bits), 101b (UART mode character bit length is 8 bits), and 110b (UART mode character bit length is 9 bits).
(4) Set the TE bit in the UiC1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

21.3.3 Special Mode 1 (I^2C Mode) (UART2)

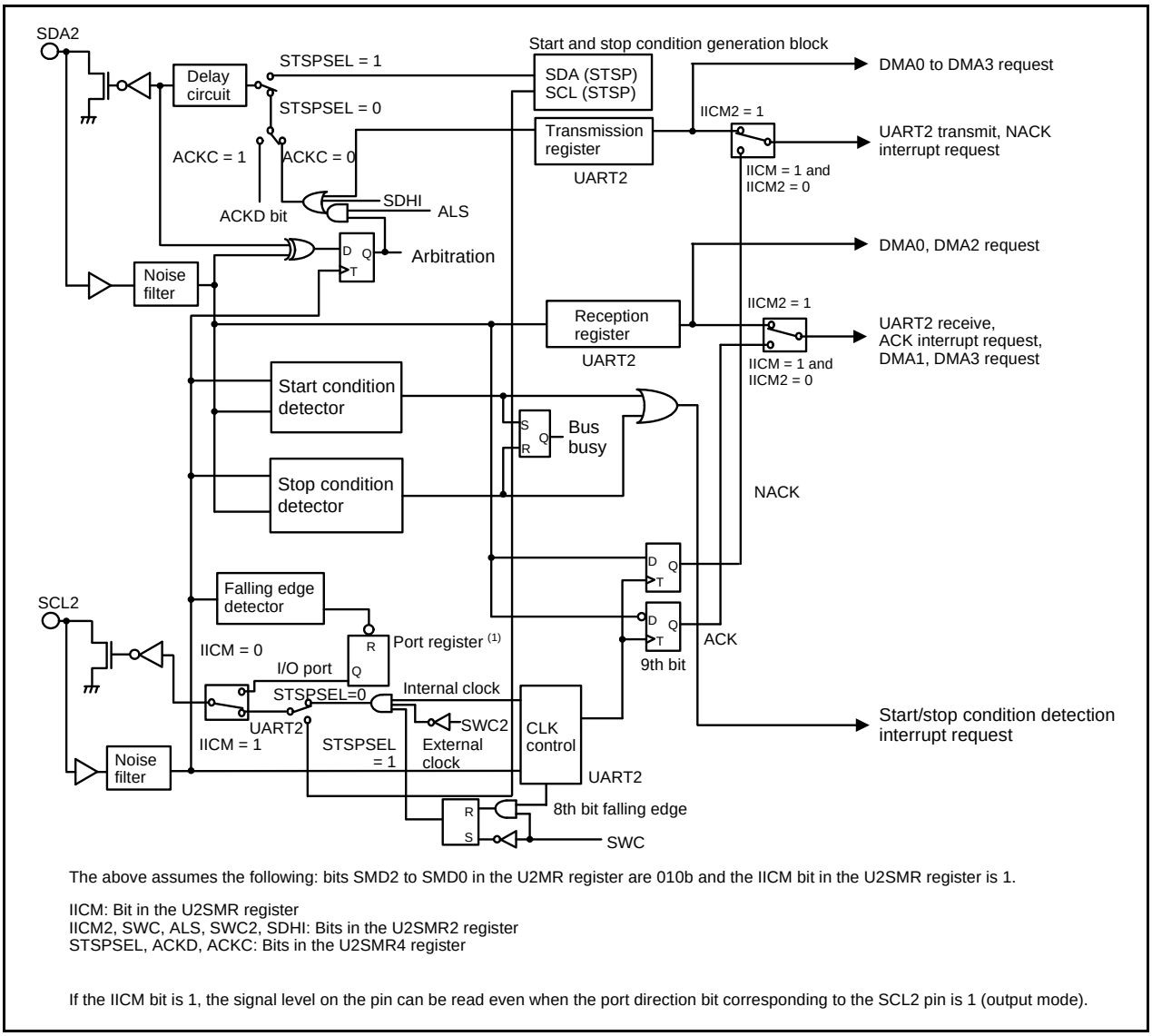
I^2C mode is compatible with the simplified I^2C interface. Table 21.12 lists the I^2C Mode Specifications. Table 21.14 and Table 21.15 list the Registers Used and Settings in I^2C Mode. Table 21.16 lists the I^2C Mode Functions. Figure 21.13 shows the I^2C Mode Block Diagram.

As shown in Table 21.16, the MCU is placed in I^2C mode by setting bits SMD2 to SMD0 in the U2MR register to 010b and the IICM bit in the U2SMR register to 1. Because SDA2 transmit output has a delay circuit attached, SDA2 output does not change state until SCL2 goes low and remains stably low.

Table 21.12 I^2C Mode Specifications

Item	Specification
Data format	Character bit length: 8 bits
Transfer clock	• Master mode The CKDIR bit in the U2MR register is 0 (internal clock): fj / (2(n+1)) fj = f1SIO, f2SIO, f8SIO, f32SIO n = setting value of the U2BRG register (03h to FFh) • Slave mode The CKDIR bit is 1 (external clock): input from the SCL2 pin
Transmit/receive clock	To start transmission, satisfy the following requirements (1) • The TE bit in the U2C1 register is 1 (transmission enabled) • The TI bit in the U2C1 register is 0 (data present in U2TB register)
Reception start conditions	To start reception, satisfy the following requirements (1) • The RE bit in the U2C1 register is 1 (reception enabled) • The TE bit in the U2C1 register is 1 (transmission enabled) • The TI bit in the U2C1 register is 0 (data present in the U2TB register)
Interrupt request generation timing	When a start condition, stop condition, ACK (acknowledge), or NACK (not-acknowledge) is detected.
Error detection	Overrun error (2) This error occurs if the serial interface starts receiving the next unit of data before reading the U2RB register and receives the eighth bit of the unit of next data.
Selectable functions	• Arbitration lost Timing at which the ABT bit in the U2RB register is updated can be selected. • SDA2 digital delay No digital delay or a delay of 2 to 8 U2BRG count source clock cycles can be selected. • Clock phase setting With or without clock delay can be selected.

Notes:
1. These requirements do not have to be set in any particular order. When transmission/reception is started as a slave and the TXEPT bit in the U2C0 register is 1 (no data present in transmit register), meet the last requirement when the external clock is high.
2. If an overrun error occurs, the received data of the U2RB register will be undefined.



The above assumes the following: bits SMD2 to SMD0 in the U2MR register are 010b and the IICM bit in the U2SMR register is 1.

IICM: Bit in the U2SMR register
IICM2, SWC, ALS, SWC2, SDHI: Bits in the U2SMR2 register
STSPSEL, ACKD, ACKC: Bits in the U2SMR4 register

If the IICM bit is 1, the signal level on the pin can be read even when the port direction bit corresponding to the SCL2 pin is 1 (output mode).

Figure 21.13 I²C Mode Block Diagram

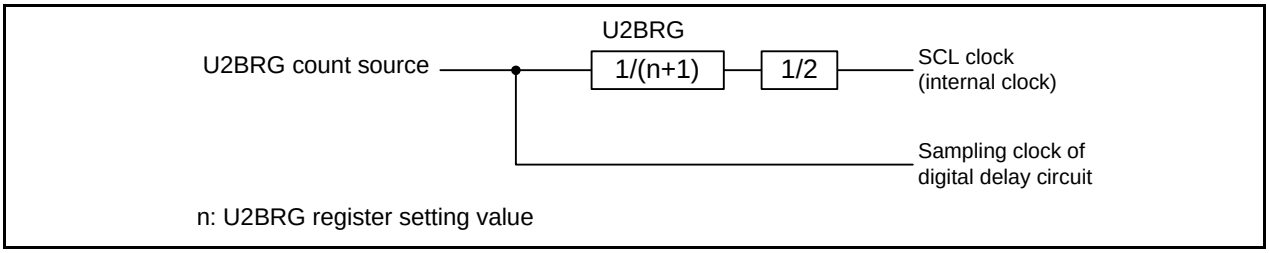


Figure 21.14 Internal Clock Configuration

Table 21.13 I/O Pin Functions in I²C Mode

Pin Name	I/O	Function
SCL2 (1, 2)	I/O	Clock input or output
SDA2 (1, 2)	I/O	Data input or output

Note:
1. Set the port direction bit sharing pin to 0.
2. Pins CLK2 and $\overline{CTS2}$/$\overline{RTS2}$ are not used (they can be used as I/O ports).

Table 21.14 Registers Used and Settings in I²C Mode (1/2) (1)

Register	Bits	Function	
		Master	Slave
UCLKSEL0	OCOSEL0	Select clock prior to division for UART0 to UART2.	Select clock prior to division for UART0 to UART2.
PCLKR	PCLK1	Select the count source for the U2BRG register.	Select the count source for the U2BRG register.
U2TB	0 to 7	When transmitting, set the transmission data. When receiving, set FFh.	When transmitting, set the transmission data. When receiving, set FFh.
	8	When transmitting, set to 1. When receiving, set the value in the ACK bit.	When transmitting, set to 1. When receiving, set the value in the ACK bit.
U2RB	0 to 7	Reception data can be read.	Reception data can be read.
	8	ACK or NACK is set in this bit.	ACK or NACK is set in this bit.
	ABT	Arbitration lost detection flag	Disabled
	OER	Overrun error flag	Overrun error flag
	13 to 15	When read, the read value is undefined.	When read, the read value is undefined.
U2BRG	0 to 7	Set a bit rate.	Disabled
U2MR	SMD2 to SMD0	Set to 010b.	Set to 010b.
	CKDIR	Set to 0.	Set to 1.
	4 to 6	Set to 0.	Set to 0.
	IOPOL	Set to 0.	Set to 0.
U2C0	CLK1, CLK0	Select the count source for the UiBRG register.	Disabled
	CRS	Disabled because CRD is 1	Disabled because CRD is 1
	TXEPT	Transmit register empty flag	Transmit register empty flag
	CRD	Set to 1.	Set to 1.
	NCH	Set to 1.	Set to 1.
	CKPOL	Set to 0.	Set to 0.
	UFORM	Set to 1.	Set to 1.
U2C1	TE	Set to 1 to enable transmission.	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag	Transmit buffer empty flag
	RE	Set to 1 to enable reception.	Set to 1 to enable reception.
	RI	Reception complete flag	Reception complete flag
	UjIRS	Set to 1.	Set to 1.
	UjRRM, UiLCH, UiERE	Set to 0.	Set to 0.
U2SMR	IICM	Set to 1.	Set to 1.
	ABC	Select the timing that arbitration lost is detected.	Disabled
	BBS	Bus busy flag	Bus busy flag
	3 to 7	Set to 0.	Set to 0.

Note:
1. This table does not describe a procedure.

Table 21.15 Registers Used and Settings in I²C Mode (2/2) (1)

Register	Bits	Function	
		Master	Slave
U2SMR2	IICM2	See Table 21.16 "I²C Mode Functions".	See Table 21.16 "I²C Mode Functions".
	CSC	Set to 1 to enable clock synchronization.	Set to 0.
	SWC	Set to 1 to fix SCL2 output to low after receiving the eighth bit of the clock.	Set to 1 to fix SCL2 output to low after receiving the eighth bit of the clock.
	ALS	Set to 1 to stop SDA2 output when arbitration lost is detected.	Set to 0.
	STAC	Set to 0.	Set to 1 to initialize UART2 at start condition detection.
	SWC2	Set to 1 to forcibly pull SCL2 output low.	Set to 1 to forcibly pull SCL2 output low.
	SDHI	Set to 1 to disable SDA2 output.	Set to 1 to disable SDA2 output.
	7	Set to 0.	Set to 0.
U2SMR3	0, 2, 4 NODC	Set to 0.	Set to 0.
	CKPH	Set to 1.	Set to 1.
	DL2 to DL0	Set the amount of SDA2 digital delay.	Set the amount of SDA2 digital delay.
U2SMR4	STAREQ	Set to 1 to generate start condition.	Set to 0.
	RSTAREQ	Set to 1 to generate restart condition.	Set to 0.
	STPREQ	Set to 1 to generate stop condition.	Set to 0.
	STSPSEL	Set to 1 to output each condition.	Set to 0.
	ACKD	Select ACK or NACK.	Select ACK or NACK.
	ACKC	Set to 1 to output ACK data.	Set to 1 to output ACK data.
	SCLHI	Set to 1 to stop SCL2 output when stop condition is detected.	Set to 0.
	SWC9	Set to 0.	Set to 1 to set SCL2 to remain low at the falling edge of the ninth bit of clock.

Note:
1. This table does not describe a procedure.

In I²C mode, functions and timings vary depending on the IICM2 bit setting in the U2SMR2 register. Figure 21.15 shows Transfer to U2RB Register and Interrupt Timing. See Figure 21.15 for the timing of transferring data to the U2RB register, the bit position of the data stored in the U2RB register, types of interrupts, interrupt requests, and DMA request generation timing.

Table 21.16 lists a comparison of other functions in clock synchronous serial I/O mode with I²C mode.

Table 21.16 I²C Mode Functions

Function	Clock Synchronous Serial I/O Mode (SMD2 to SMD0 = 001b, IICM = 0)	I²C Mode (SMD2 to SMD0 = 010b, IICM = 1)	
		IICM2 = 0 (NACK/ACK interrupt)	IICM2 = 1 (UART transmit/receive interrupt)
		CKPH = 1 (Clock delay)	CKPH = 1 (Clock delay)
Start and stop condition detect interrupts (3)	-	Start condition or stop condition detection (See Figure 21.17 “STSPSEL Bit Functions”)	
Transmission, NACK interrupt (2, 3)	UART2 transmission Transmission started or completed (selected by U2IRS)	No acknowledgment detection (NACK) Rising edge of the 9th bit of SCL2	UART2 transmission Falling edge of the 9th bit of SCL2
Reception, ACK interrupt (2, 3)	UART2 reception When 8th bit received CKPOL = 0 (rising edge) CKPOL = 1 (falling edge)	Acknowledgment detection (ACK) Rising edge of the 9th bit of SCL2	UART2 reception Falling edge of the 9th bit of SCL2
Timing for transferring data from UART reception shift register to U2RB register	CKPOL = 0 (rising edge) CKPOL = 1 (falling edge)	Rising edge of the 9th bit of SCL2	Falling edges of the 8th bit of SCL2 and rising edges of the 9th bit of SCL2
UART2 transmission output delay	Not delayed	Delayed	Delayed
Read RXD2 and SCL2 pin levels	Possible when the corresponding port direction bit = 0	Always possible no matter how the corresponding port direction bit is set	Always possible no matter how the corresponding port direction bit is set
Initial value of TXD2 and SDA2 outputs	CKPOL = 0 (high) CKPOL = 1 (low)	The value set in the port register before setting I²C mode (1)	The value set in the port register before setting I²C mode (1)
Initial and end values of SCL2	-	Low	Low
DMA1, DMA3 factor (2)	UART2 reception	Acknowledgment detection (ACK)	UART2 reception Falling edge of the 9th bit of SCL2
Read received data	1st to 8th bits of the received data are stored in bits 0 to 7 in the U2RB register.	1st to 8th bits of the received data are stored in bits 7 to 0 in the U2RB register.	Refer to Figure 21.15 “Transfer to U2RB Register and Interrupt Timing”.

SMD2 to SMD0: Bits in the U2MR register
CKPOL: Bit in the U2C0 register
IICM: Bit in the U2SMR register
IICM2: Bit in the U2SMR2 register
CKPH: Bit in the U2SMR3 register
U2IRS: Bit in the U2C1 register

Notes:
1. Set the initial value of SDA2 output while bits SMD2 to SMD0 in the UiMR register are 000b (serial interface disabled).
2. See Figure 21.15 “Transfer to U2RB Register and Interrupt Timing”.
3. The procedure to change interrupt sources is as follows:
   (1) Disable the interrupt to be changed the source.
   (2) Change the source of interrupt.
   (3) Set the IR bit in the interrupt control register of that interrupt to 0 (no interrupt requested).
   (4) Set bits ILVL2 to ILVL0 in the interrupt control register of that interrupt.

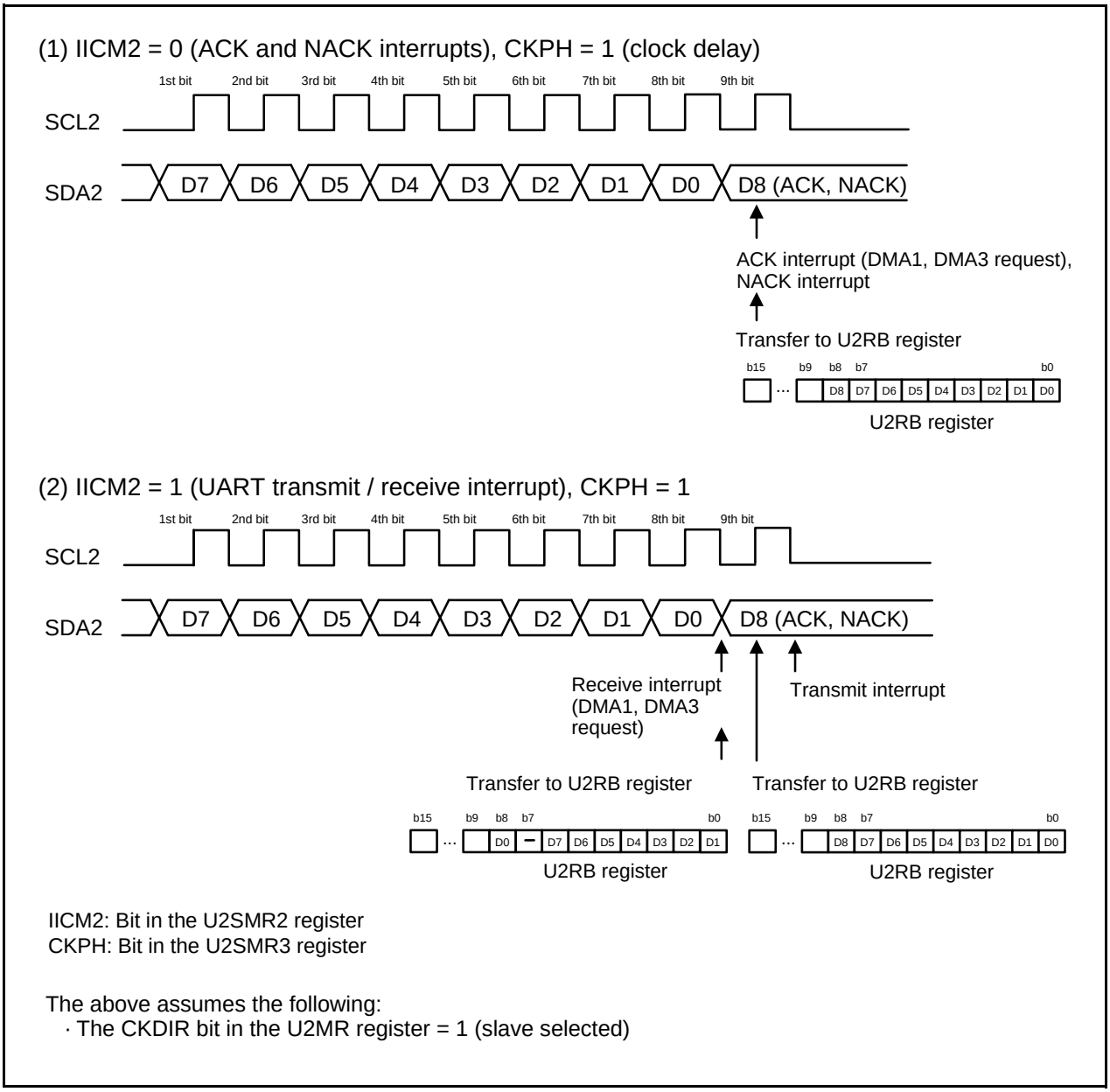
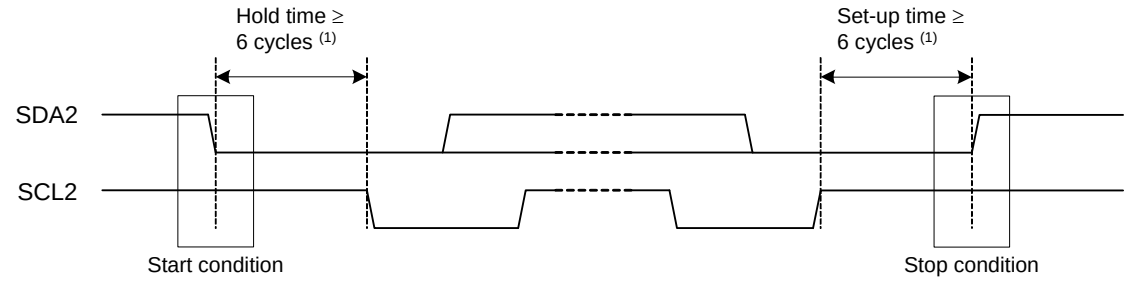


Figure 21.15 Transfer to U2RB Register and Interrupt Timing

21.3.3.1 Detecting Start and Stop Conditions

Start and stop conditions are detected by their respective detectors.
Whether a start or a stop condition has been detected is determined.
A start condition detect interrupt request is generated when the SDA2 pin changes state from high to low while the SCL2 pin is in the high state. A stop condition detect interrupt request is generated when the SDA2 pin changes state from low to high while the SCL2 pin is in the high state.
Because the start and stop condition detect interrupts share the interrupt control register and vector, check the BBS bit in the U2SMR register to determine which interrupt source is requesting the interrupt.
To detect a start or stop condition, both the set-up and hold times require at least six cycles of the BRG2 count source as shown in Figure 21.16. To meet the condition for the Fast-mode specification, the BRG2count source must be at least 10 MHz.



Note:
1. The number of cycles are the BRG2 count source cycles.

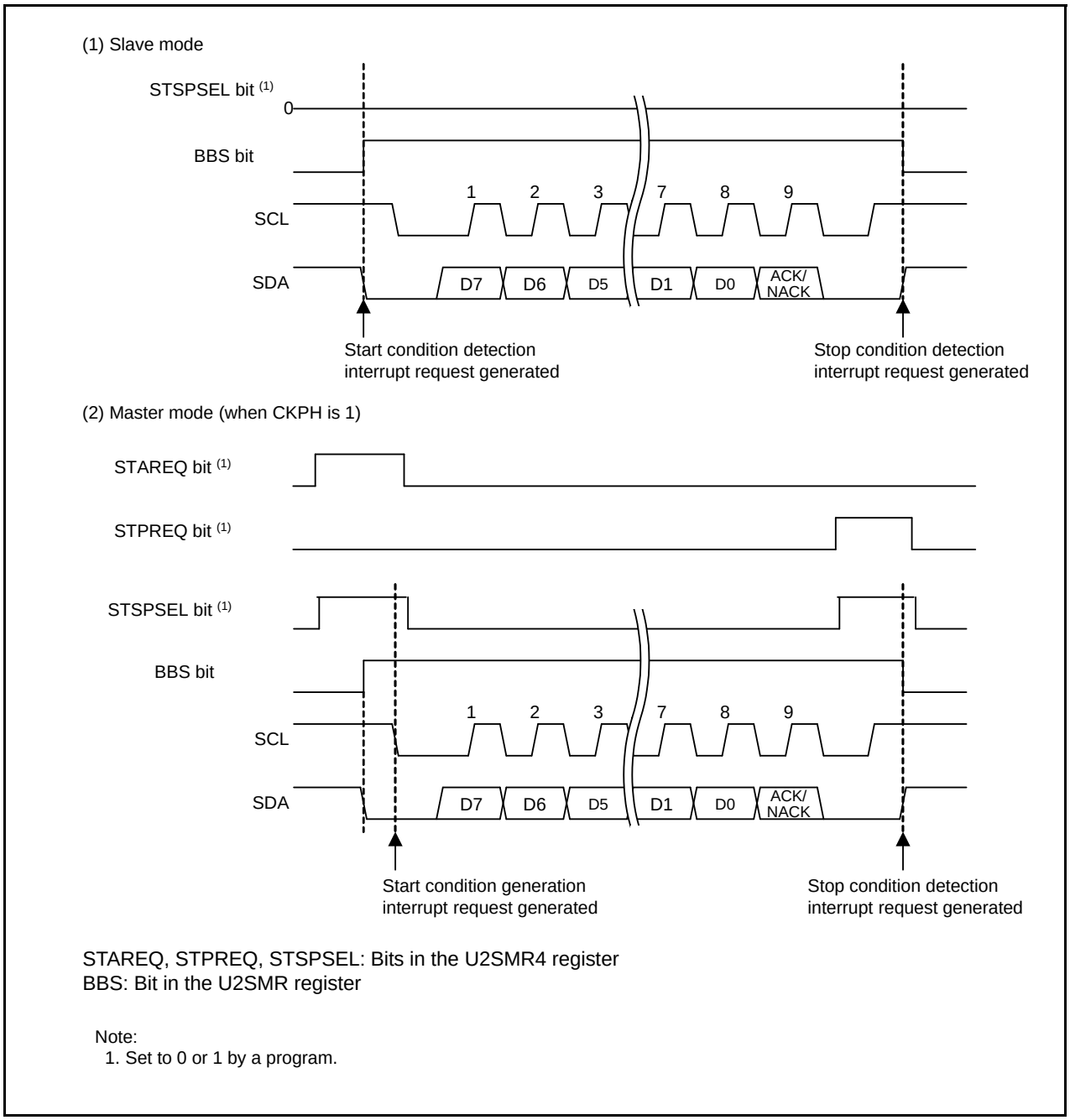
Figure 21.16 Detecting Start and Stop Conditions

21.3.3.2 Generating Start and Stop Conditions

A start condition is generated by setting the STAREQ bit in the U2SMR4 register to 1 (start).
A restart condition is generated by setting the RSTAREQ bit in the U2SMR4 register to 1 (start).
A stop condition is generated by setting the STPREQ bit in the U2SMR4 register to 1 (start).
The output procedure is described below.
(1) Set the STAREQ bit, RSTAREQ bit or STPREQ bit to 1 (start).
(2) Set the STSPSEL bit in the U2SMR4 register to 1 (output).
The functions of the STSPSEL bit are shown in Table 21.17 and Figure 21.17.

Table 21.17 STSPSEL Bit Functions

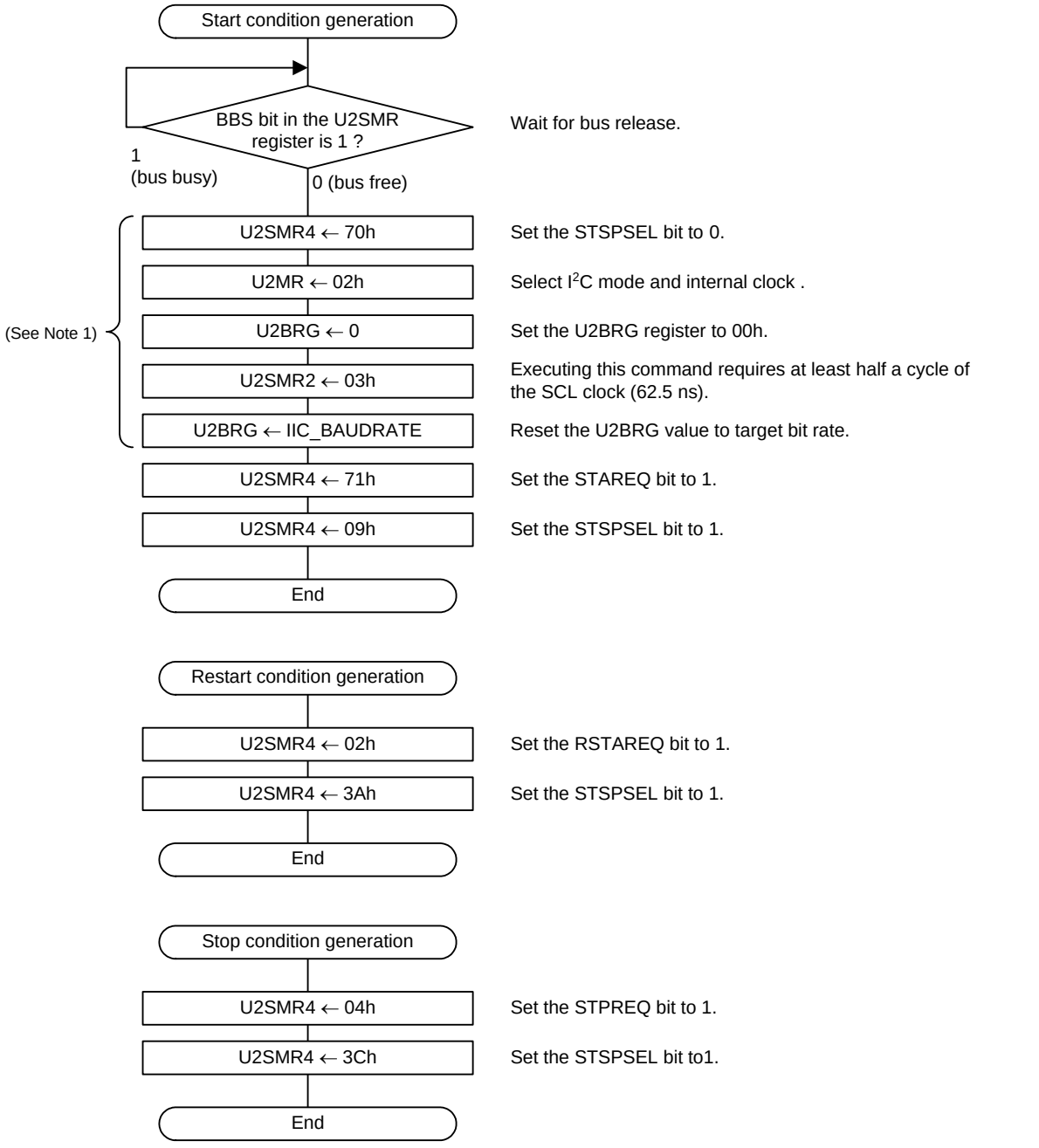
Function	STSPSEL = 0	STSPSEL = 1
Output of pins SCL2 and SDA2	Output of transmit/receive clock and data Output of start/stop condition is accomplished by a program using ports (not automatically generated in hardware)	Output of a start/stop condition according to bits STAREQ, RSTAREQ, and STPREQ
Start/stop condition Interrupt request generation timing	Detection of start/stop condition	Completion of generating start/stop condition



STAREQ, STPREQ, STSPSEL: Bits in the U2SMR4 register
BBS: Bit in the U2SMR register

Note:
1. Set to 0 or 1 by a program.

Figure 21.17 STSPSEL Bit Functions



The above assumes the following:
XIN = 16 MHz, main clock divided by 1 (no division), U2BRG count source = f1

Note:
1. After a stop condition is generated, when generating the next start condition, after setting the STSPSEL bit in the U2SMR4 register to 0 and waiting at least half a cycle of the SCL clock, then set the STAREQ bit to 1.

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Figure 21.18 Register Setting Procedures for Condition Generation

21.3.3.3 Arbitration

The MCU determines whether the transmit data matches data input to the SDA2 pin on the rising edge of SCL2. If it does not match the input data, arbitration takes place at the SDA2 pin by stopping data output.

The ABC bit in the U2SMR register determines the update timing for the ABT bit in the U2RB register.

When the ABC bit is 0 (update per bit), the ABT bit becomes 1 as soon as a data discrepancy is detected. If not detected, the ABT bit becomes 0. When the ABC bit is 1 (update per byte), the ABT bit becomes 1 on the falling edge of the eighth bit of SCL2 if any discrepancy is detected. In this ABC bit setting, the ABT bit should be set to 0 after ACK detection of 1-byte is completed to start the next 1-byte transmission/reception.

When the ALS bit in the U2SMR2 register is set to 1 (SDA output stop enabled), an arbitration lost occurs. As soon as the ABT bit becomes 1, the SDA2 pin becomes high-impedance.

21.3.3.4 SCL Control and Clock Synchronization

Data transmission/reception in I^2C mode uses the transmit/receive clock as shown in Figure 21.15 “Transfer to U2RB Register and Interrupt Timing”. The clock speed increase makes it difficult to secure the required time for ACK generation and data transmit procedure. The I^2C mode supports a function of wait-state insertion to secure this required time and a function of clock synchronization with a wait-state inserted by other devices.

The SWC bit in the U2SMR2 register is used to insert a wait-state for ACK generation. When the SWC bit is set to 1 (the SCL2 pin is held low after the eighth bit of SCL2 is received), the SCL2 pin is held low on the falling edge of the eighth bit of SCL2. When the SWC bit is set to 0 (no wait-state/wait-state cleared), the SCL2 line is released.

When the SWC2 bit in the U2SMR2 register is set to 1 (the SCL2 pin is held low), the SCL2 pin is forced low even during transmission or reception. When the SWC2 bit is set to 0 (transmit/receive clock is output at the SCL2 pin), the SCL2 line is released to output the transmit/receive clock.

The SWC9 bit in the U2SMR4 register is used to insert a wait-state for checking received acknowledge bits. While the CKPH bit in the U2SMR3 register is 1 (clock delayed), when the SWC9 bit is set to 1 (the SCL2 pin is held low after the ninth bit of the SCL2 is received), the SCL2 pin is held low on the falling edge of the ninth bit of SCL2. When the SWC9 bit is set to 0 (no wait-state/wait-state cleared), the SCL2 line is released.

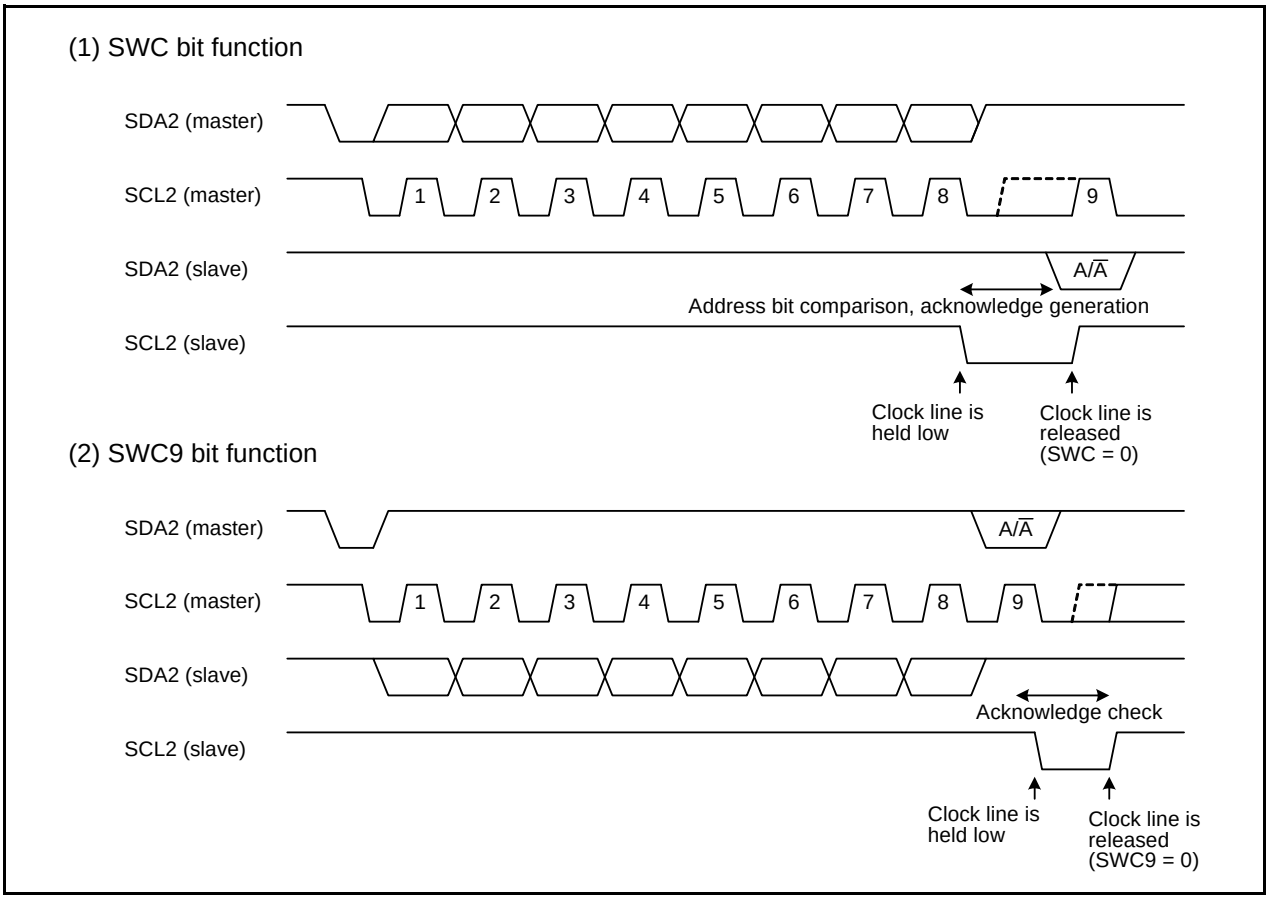


Figure 21.19 Inserting Wait-States Using Bits SWC and SWC9

The CSC bit in the U2SMR2 register synchronizes an internally generated clock with the clock applied to the SCL2 pin. For example, if a wait-state is inserted from other devices, the two clocks are not synchronized. While the CSC bit is 1 (clock synchronization enabled) and the internal clock is held high, when a high at the SCL2 pin changes to low, the internal clock becomes low in order to reload the U2BRG register value and resume counting. While the SCL2 pin is held low, when the internal clock changes from low to high, the count is stopped until the SCL2 pin becomes high. That is, the UART2 transmit/receive clock is the logical AND of the internal clock and SCL2. The synchronized period starts from one clock prior to an internally generated clock and ends when the ninth clock is completed. The CSC bit can be set to 1 only when the CKDIR bit in the U2MR register is set to 0 (internal clock selected).

The SCLHI bit in the U2SMR4 register is used to leave the SCL2 pin open when another master generates a stop condition while the master is performing a transmit/receive operation. While the SCLHI bit is set to 1 (output stopped), the SCL2 pin is open (the pin is high-impedance) when a stop condition is detected and the clock output is stopped.

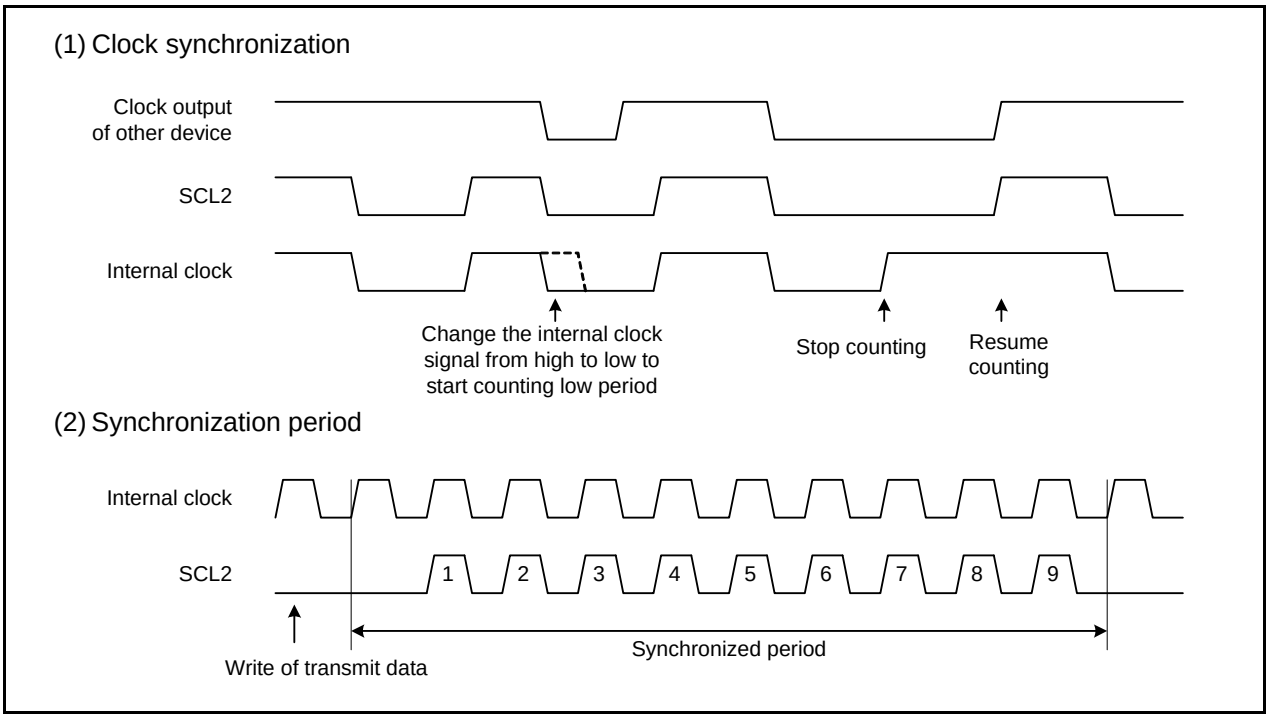


Figure 21.20 Clock Synchronization

21.3.3.5 SCL Clock Frequency

The SCL clock duty generated in I²C mode is 50%. The low-level width of the SCL clock is 1.25 μs when the I²C-bus setting is Fast-mode maximum SCL clock (400 kbps). This value does not satisfy the Fast-mode I²C-bus specification (f_{LOW} = minimum 1.3 μs). Set the SCL clock to 384.6 kbps or less to satisfy the SCL clock low-level width of 1.3 μs or more.
When the clock synchronous function (Figure 21.20 “Clock Synchronization”) is enabled, there is a sampling delay of the noise filter plus 1 to 1.5 cycles of U2BRG count source.
There is also a delay of the SCL clock when high is determined and the SCL clock high width is extended. Therefore, the actual SCL clock becomes slower than SCL clock bit rate setting.
To calculate the effective value of SCL clock, take the SCL clock rise time (t_R) into consideration.
The following is an example of an SCL clock calculation.

Example of an effective value of SCL clock calculation at 384.6 kbps

- U2BRG count source: f1 = 20 MHz
- U2BRG register setting value: n = 26 - 1
- SCL clock rise time: t_R = 100 ns
- SCL clock fall time: t_F = 0 ns
- Noise filter width: t_{NF} = 100 ns (1)
- Sampling delay: t_{SD} = 1 cycle

f_{SCL} (theoretical value) = f1 / (2(n + 1)) = 20 MHz / (2(25 + 1)) = 384.6 kbps
t_{LOW} = 1 / ($2f_{SCL}$ (theoretical value)) = 1 / (2 × 384.6 kbps) = 1.3 μs
t_{HIGH} = 1 / ($2f_{SCL}$ (theoretical value)) + t_{NF} + (t_{SD} × 1 / f1)
= 1 / (2 × 384.6 kbps) + 100 ns + (1 × 1 / 20 MHz)
= 1.45 μs
f_{SCL} (actual value) = 1 / (t_F + t_{LOW} + t_R + t_{HIGH}) = 1 / (0 ns + 1.3 μs + 100 ns + 1.45 μs) ≈ 350.8 kbps

Note:
1. Maximum 200 ns.

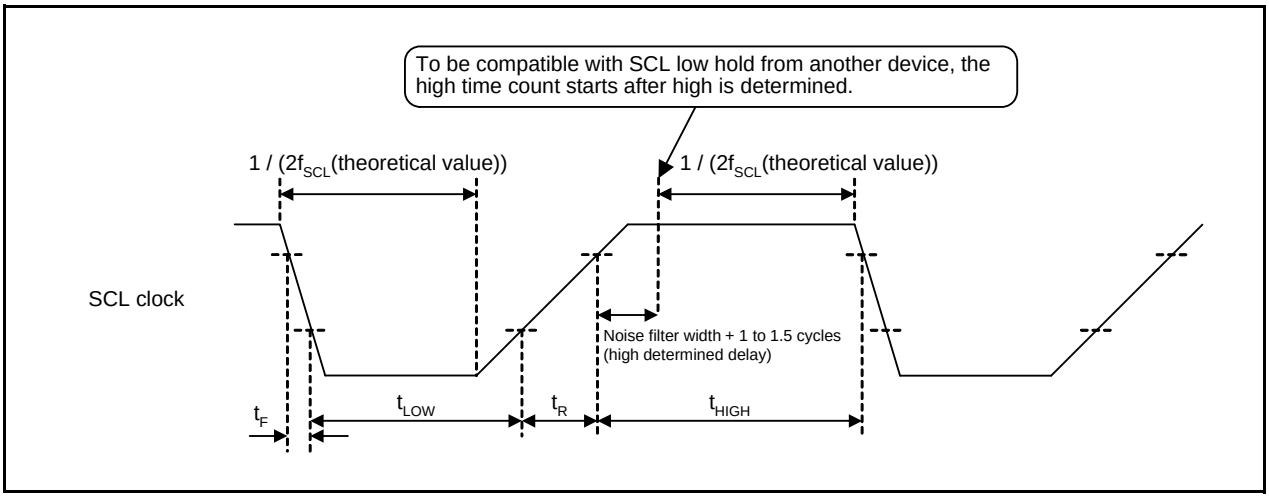


Figure 21.21 SCL Clock

21.3.3.6 SDA Output Control

When transmitting byte data, the SDA2 pin outputs transmit data for the first to eighth bits, and it is released to receive an acknowledgment for the ninth bit.

In I^2C mode, set 9-bit data to the U2TB register. In 9-bit data, set the transmit data to bits b7 to b0 and set b8 to 1. By setting the UFORM bit in the U2C0 register to 1 (MSB first) and 9-bit data to the U2TB register, transmit data is output from the SDA2 pin in the following order: b7, b6, b5, b4, b3, b2, b1, b0 and b8. As b8 is 1, the SDA2 pin becomes high-impedance at the ninth bit and an acknowledgment can be received.

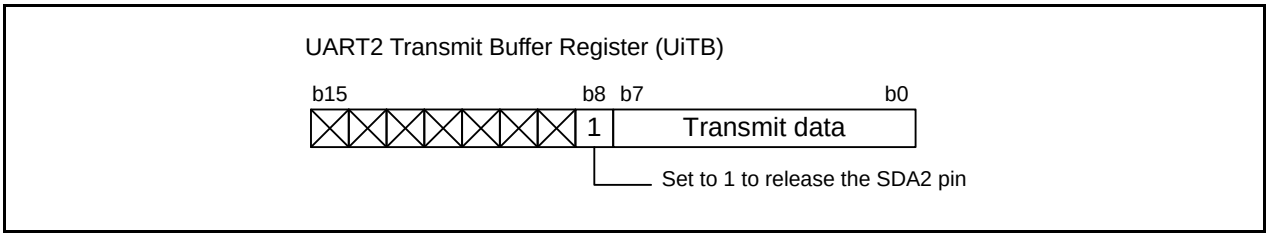


Figure 21.22 U2TB Register Setting (SDA Output)

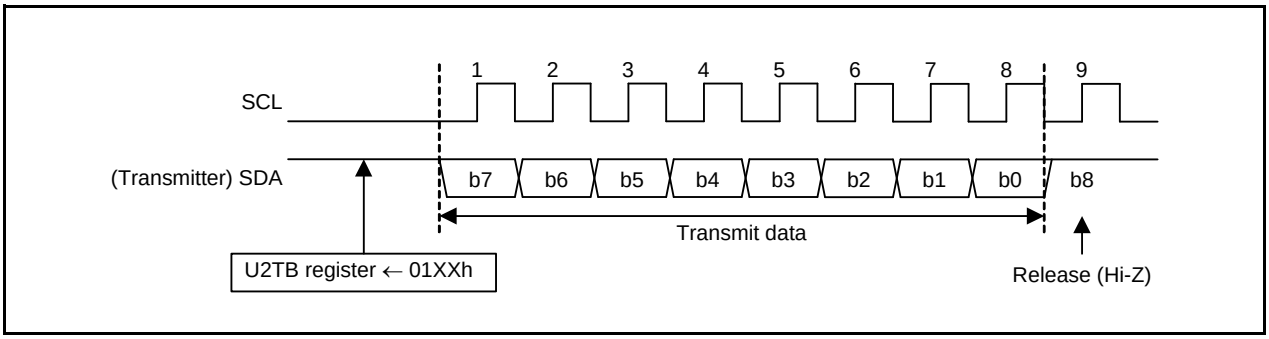


Figure 21.23 Byte Data Transmission

Set bits DL2 to DL0 in the U2SMR3 register to add no delays or a delay of one to eight U2BRG count source clock cycles to SDA2 output.

Setting the SDHI bit in the U2SMR2 register to 1 (SDA output disabled) forcibly places the SDA2 pin in a high-impedance state. Do not write to the SDHI bit at the rising edge of the UART2 transmit/receive clock as the ABT bit in the U2RB register may inadvertently become 1 (detected).

21.3.3.7 SDA Digital Delay

When transferring data with the I2C-bus, change the data while the SCL clock is low. When SDA is changed while the SCL clock is a high, the change is recognized as one of the corresponding conditions (see 21.5.3.3 “Setup and Hold Times When Generating a Start/Stop Condition”).
This function delays output from the SDA2 pin. By delaying the change of the SDA, the data can be changed while the SCL clock is low. This function is enabled by setting bits DL2 to DL0 in the U2SMR3 register to 001b to 111b, and disabled by setting them to 000b.

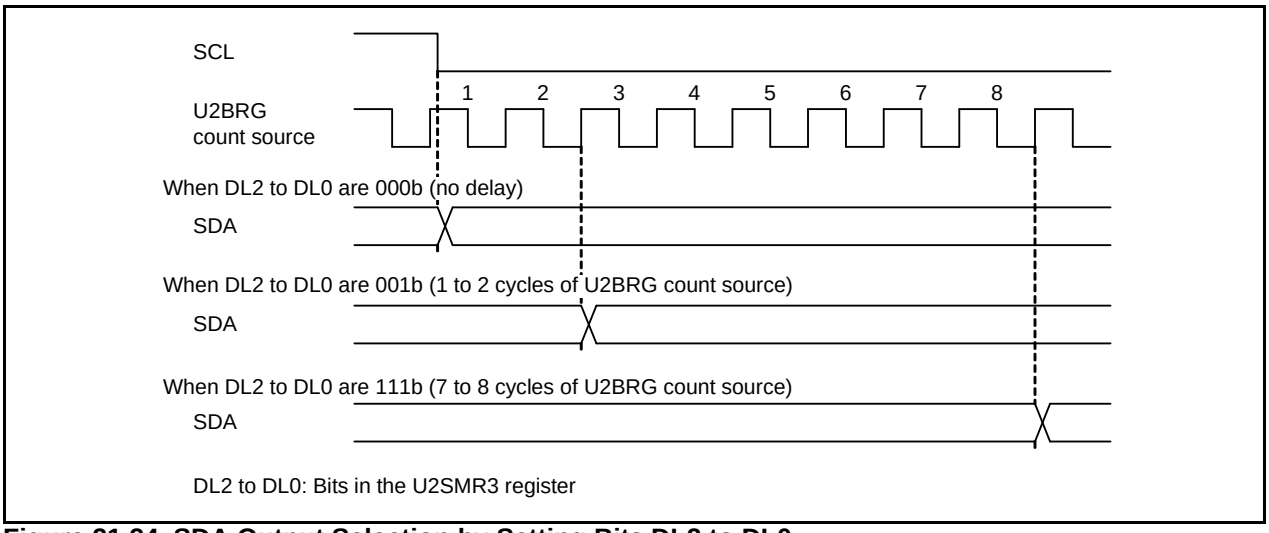


Figure 21.24 SDA Output Selection by Setting Bits DL2 to DL0

21.3.3.8 SDA Input

When the IICM2 bit in the U2SMR2 register is set to 0, the first 8 bits of received data (D7 to D0) are stored in bits 7 to 0 in the U2RB register and the ninth bit (ACK/NACK) is stored in bit 8.
When the IICM2 bit is 1, the first to seventh bits (D7 to D1) of the received data are stored in bits 6 to 0 in the U2RB register and the eighth bit (D0) is stored in bit 8 in the U2RB register. Even when the IICM2 bit is 1, if the CKPH bit in the U2SMR3 register is 1, the same data as when the IICM2 bit is 0 can be read. To read the data, read the U2RB register after the rising edge of ninth bit of the corresponding clock pulse.

When receiving byte data, the SDA2 pin is released for the first to eighth bits to receive data, and an acknowledgment is generated for the ninth bit. NACK is generated when the last byte data is received in master mode, or when the slave address does not match in slave mode. In all other cases, ACK is generated.
In I2C mode, set 9-bit data to the U2TB register. In 9-bit data, set FFh to b7 to b0 to release the SDA2 pin and set b8 to 0 to generate ACK or 1 to generate NACK.
By setting 00FFh or 01FFh as 9-bit data to the U2TB register, the SDA2 pin becomes high-impedance for the first to eighth bits, and data can be received. ACK or NACK is generated at the ninth bit.
Read the received data from the U2RB register. When the clock delay function is used, data transfer to the U2RB register occurs twice and each U2RB register value is different. Refer to Figure 21.15 “Transfer to U2RB Register and Interrupt Timing” for details.

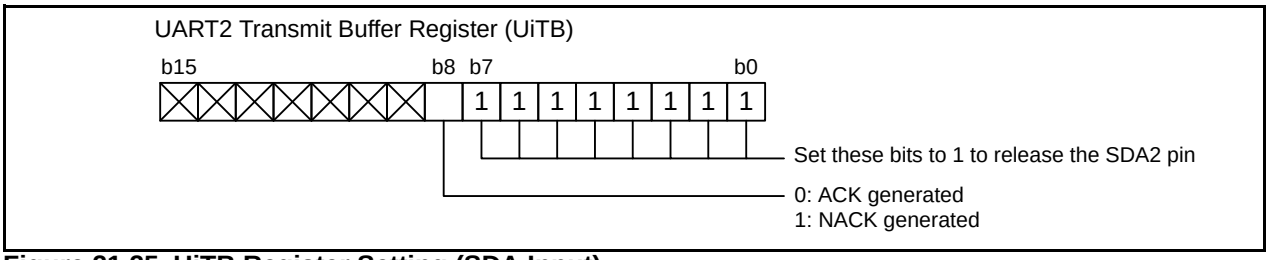


Figure 21.25 UiTB Register Setting (SDA Input)

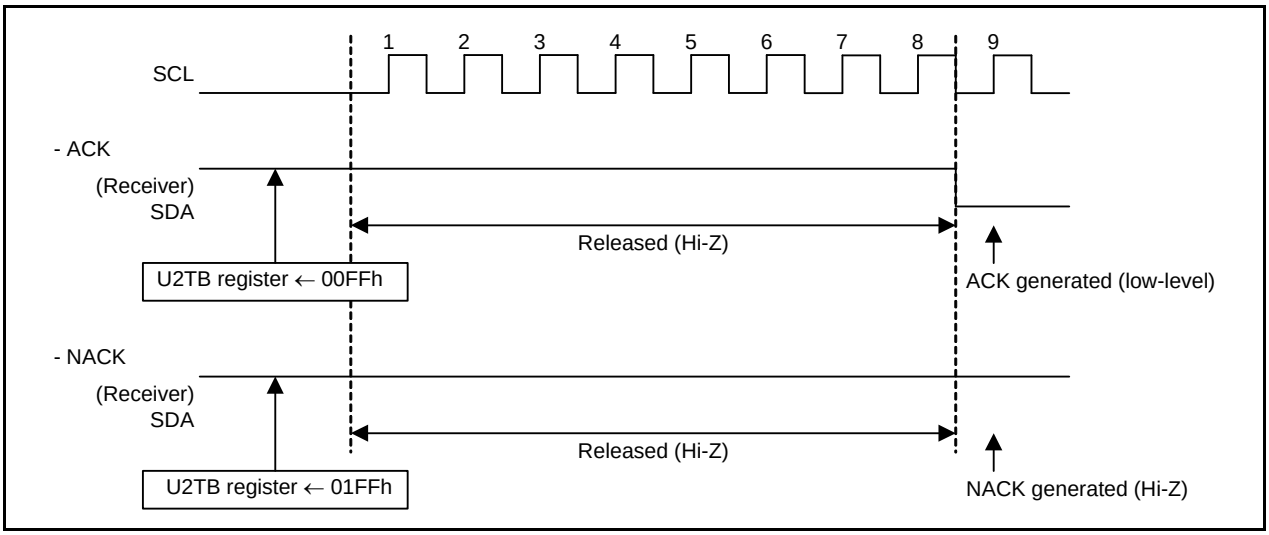


Figure 21.26 Byte Data Reception

21.3.3.9 ACK and NACK

When data is to be received, ACK is output after 8 bits are received by setting the U2TB register to 00FFh as dummy data. When the STSPSEL bit in the U2SMR4 register is set to 0 (serial I/O circuit selected) and the ACKC bit is set to 1 (ACK data output), the value of the ACKD bit is output at the SDA2 pin.

If the IICM2 bit is 0, a NACK interrupt request is generated when the SDA2 pin is held high at the rising edge of the ninth bit of SCL2. An ACK interrupt request is generated when the SDA2 pin is held low.

If the DMA request source is “UART2 receive interrupt request or ACK interrupt request”, the DMA transfer is activated when ACK is detected.

21.3.3.10 Initialization of Transmission/Reception

Select the external clock as the transmit/receive clock when using this function.

If a start condition is detected while the STAC bit in the U2SMR2 register is 1 (initialize the circuit if the start condition is detected), the serial interface operates as follows:

- The transmit shift register is initialized, and the U2TB register value is transferred to the transmit shift register. Doing so starts the data transmission when the next clock pulse is applied. However, the UART2 output value does not change until the first bit of data is output synchronously with the input clock. It remains the same as when a start condition was detected.
- The receive shift register is initialized, and the serial interface starts receiving data when the next clock pulse is applied.
- The SWC bit becomes 1 (hold the SCL2 pin low after the eighth bit of SCL2 is received). Consequently, the SCL2 pin is pulled low at the falling edge of the ninth clock pulse.

When UART2 transmission/reception is started using this function, the TI bit does not change.

When the UART2 initializing function is used in slave mode, UART2 is initialized automatically when a start condition is detected. Therefore, an interrupt is unnecessary for detecting a start condition.

21.3.4 Special Mode 2 (UART2)

In special mode 2, the serial interface module allows serial communication between one master and multiple slaves. The transmit/receive clock polarity and phase are selectable. Table 21.18 lists Special Mode 2 Specifications.

Table 21.18 Special Mode 2 Specifications

Item	Specification
Data format	Character data length: 8 bits
Transmit/receive clock	• Master mode The CKDIR bit in the U2MR register = 0 (internal clock): $\frac{fj}{2(n+1)}$ fj = f1SIO, f2SIO, f8SIO, f32SIO n: Setting value of U2BRG register 00h to FFh
Transmit/receive control	Controlled by I/O ports
Transmission start conditions	To start transmission, satisfy the following requirements: • The TE bit in the U2C1 register is 1 (transmission enabled) • The TI bit in the U2C1 register is 0 (data present in U2TB register)
Reception start conditions	To start reception, satisfy the following requirements: • The RE bit in the U2C1 register is 1 (reception enabled) • The TE bit is 1 (transmission enabled) • The TI bit is 0 (data present in the U2TB register)
Interrupt request generation timing	For transmit interrupt, one of the following conditions can be selected • The U2IRS bit in the U2C1 register is 0 (transmit buffer empty): When transferring data from the U2TB register to the UART2 transmit register (at start of transmission) • The U2IRS bit is 1 (transfer completed): When the serial interface completed sending data from the UART2 transmit register For receive interrupt • When transferring data from the UART2 receive register to the U2RB register (at completion of reception)
Error detection	Overrun error (1) This error occurs if the serial interface starts receiving the next data before reading the U2RB register and receives the 7th bit of the next data
Selectable functions	• CLK polarity selection Whether transfer data is output/input at the rising or falling edge of the transfer clock can be selected. • LBS first, MSB first selection Whether to start sending/receiving data beginning with bit 0 or beginning with bit 7. • Continuous receive mode selection Reception is enabled by reading the U2RB register • Serial data logic switching Function to invert the logic value of the transmit/receive data. • Clock phase setting Selectable from four combinations of transmit/receive clock polarities and phases.

Note:
1. If an overrun error occurs, the received data of the U2RB register will be undefined. The IR bit in the S2RIC register does not change.

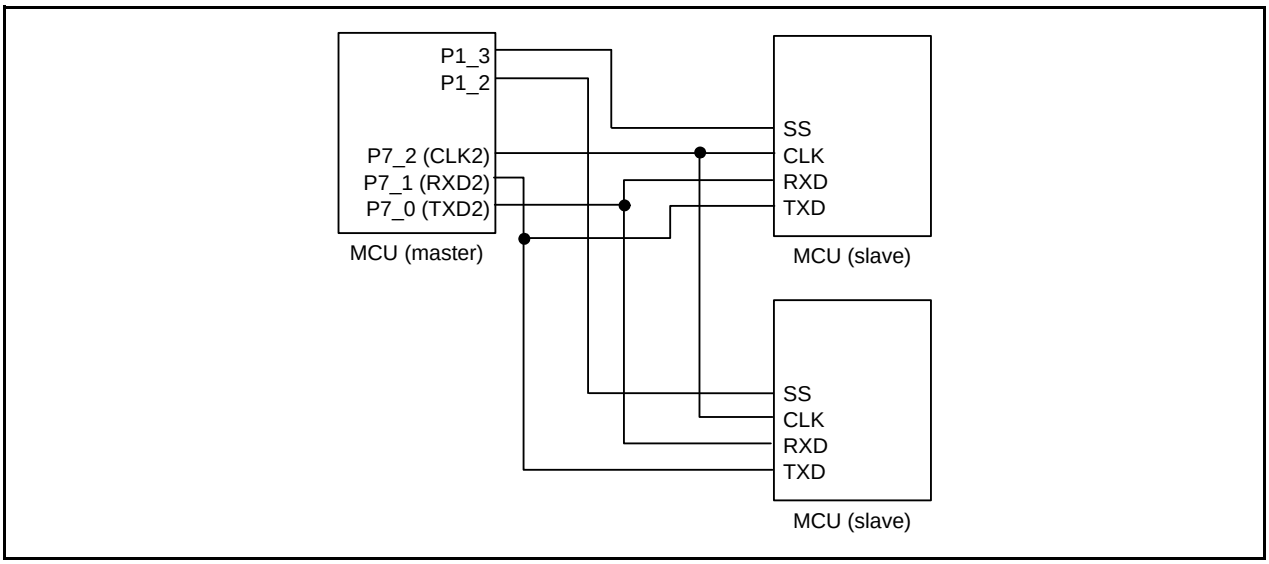


Figure 21.27 Serial Bus Communication Control Example in Special Mode 2

Table 21.19 I/O Pin Functions in Special Mode 2

Pin Name	I/O	Function	Method of Selection
CLK2	Output	Clock output	The CKDIR bit in the U2MR register = 0
TXD2	Output	Serial data output	(Dummy data is output when performing reception only.)
RXD2	Input	Serial data input	Set the port direction bits sharing pins to 0.
	Input	Input port	Set the port direction bits sharing pins to 0. (can be used as an input port only when transmitting)

Pins $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ are not used. (They can be used as I/O ports.)

Table 21.20 Registers Used and Settings in Special Mode 2 (1)

Register	Bits	Function
UCLKSEL0	OCOSEL0	Select clock prior to division for UART0 to UART2.
PCLKR	PCLK1	Select the count source for the U2BRG register.
U2TB	0 to 7	Set transmission data.
	8	- (does not need to be set) If necessary, set to 0.
U2RB	0 to 7	Reception data can be read.
	OER	Overrun error flag
	8, 11, 13 to 15	When read, the read value is undefined.
U2BRG	0 to 7	Set bit rate.
U2MR	SMD2 to SMD0	Set to 001b.
	CKDIR	Set to 0.
	4 to 6	Set to 0.
	IOPOL	Set to 0.
U2C0	CLK0, CLK1	Select the count source for the U2BRG register.
	CRS	Disabled because CRD is 1
	TXEPT	Transmit register empty flag
	CRD	Set to 1.
	NCH	Select TXD2 pin output format.
	CKPOL	Clock phases can be set in combination with the CKPH bit in the U2SMR3 register.
	UFORM	Select the LSB first or MSB first.
U2C1	TE	Set to 1 to enable transmission/reception.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	U2IRS	Select UART2 transmit interrupt source.
	U2RRM	Set to 1 to use continuous receive mode.
	U2LCH	Set to 1 to use inverted data logic.
	U2ERE	Set to 0.
U2SMR	0 to 7	Set to 0.
U2SMR2	0 to 7	Set to 0.
U2SMR3	CKPH	Clock phases can be set in combination with the CKPOL bit in the U2C0 register.
	NODC	Set to 0.
	0, 2, 4 to 7	Set to 0.
U2SMR4	0 to 7	Set to 0.

Notes:
1. This table does not describe a procedure.

21.3.4.1 Clock Phase Setting Function

One of four combinations of transmit/receive clock phases and polarities can be selected using the CKPH bit in the U2SMR3 register and the CKPOL bit in the U2C0 register.

Make sure the transmit/receive clock polarity and phase are the same for the master and slaves to be used for communication.

Figure 21.28 shows the Transmit and Receive Timing in Master Mode (Internal Clock).

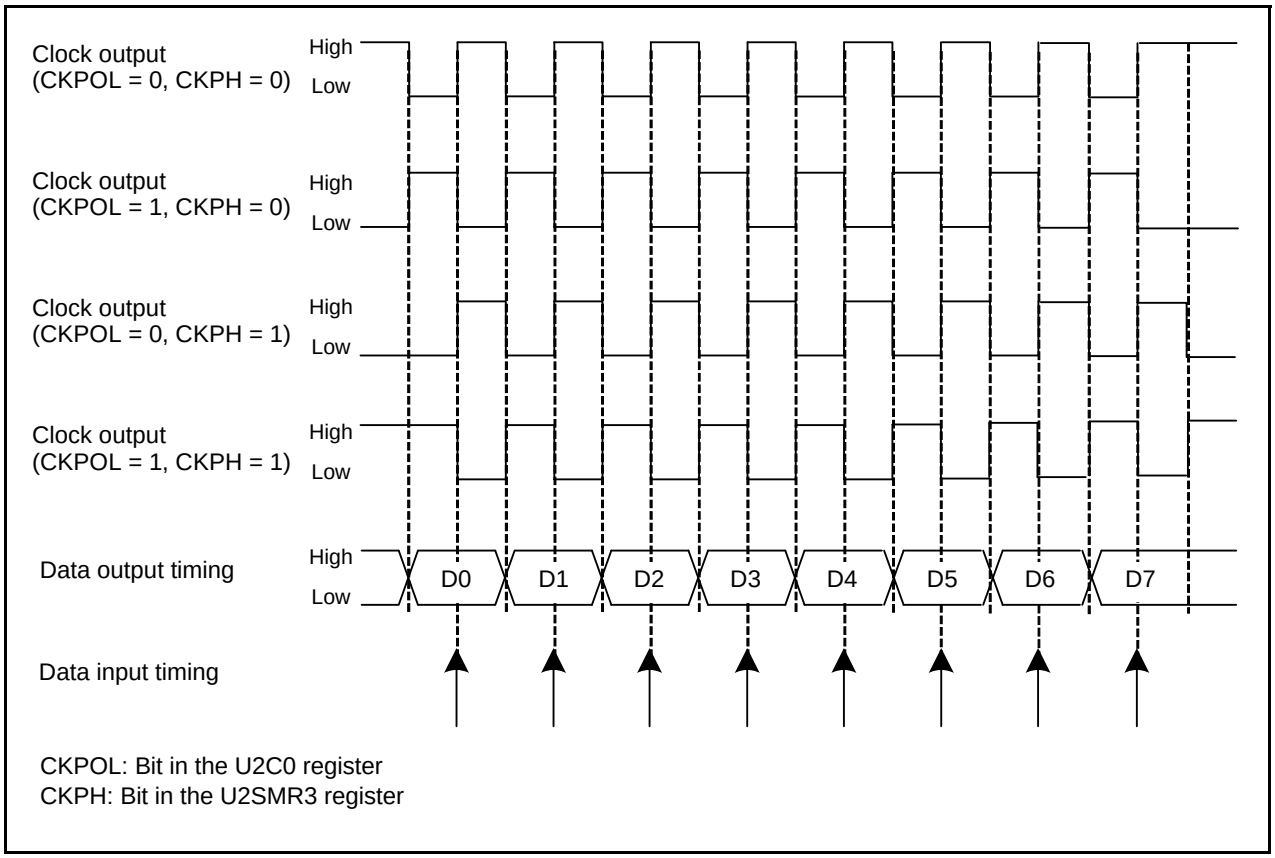


Figure 21.28 Transmit and Receive Timing in Master Mode (Internal Clock)

21.3.5 Special Mode 3 (IE Mode) (UART2)

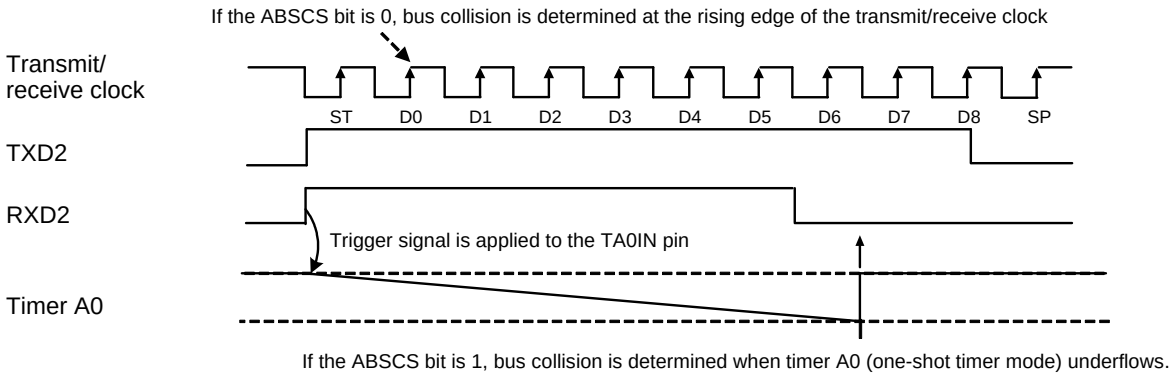
In this mode, 1 bit of IEBus is approximated by 1 byte of UART mode waveform.
Table 21.21 lists the Registers Used and Settings in IE Mode. Figure 21.29 shows the Bus Collision Detect Function-Related Bits.
If the TXD2 pin output level and RXD2 pin input level do not match, a UART2 bus collision detect interrupt request is generated.

Table 21.21 Registers Used and Settings in IE Mode (1)

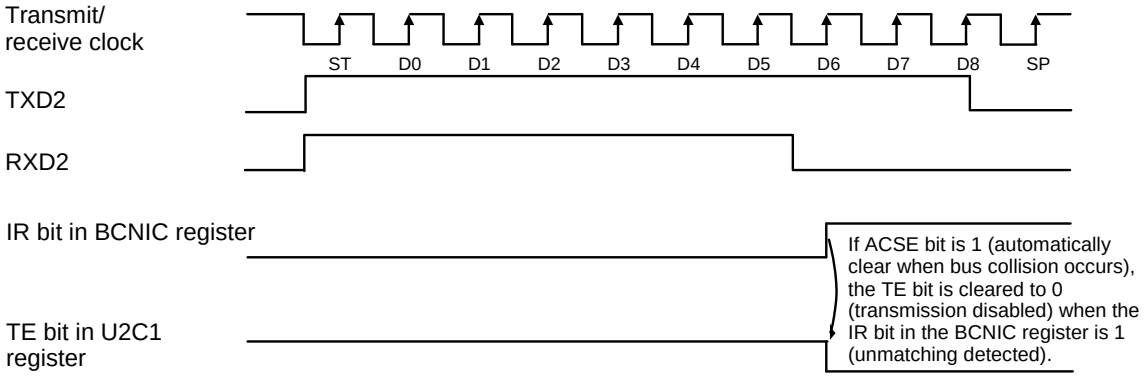
Register	Bits	Function
U2TB	0 to 8	Set transmission data.
U2RB (2)	0 to 8	Reception data can be read.
	OER, FER, PER, SUM	Error flag
U2BRG	0 to 7	Set bit rate.
U2MR	SMD2 to SMD0	Set to 110b.
	CKDIR	Select internal clock or external clock.
	STPS	Set to 0.
	PRY	Disabled because PRYE is 0
	PRYE	Set to 0.
	IOPOL	Select the TXD and RXD input/output polarity.
U2C0	CLK1, CLK0	Select the count source for the U2BRG register.
	CRS	Disabled because CRD is 1
	TXEPT	Transmit register empty flag
	CRD	Set to 1.
	NCH	Select TXD2 pin output format.
	CKPOL	Set to 0.
	UFORM	Set to 0.
U2C1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	U2IRS (2)	Select the source of UART transmit interrupt.
	U2RRM (2), U2LCH, U2ERE	Set to 0.
U2SMR	0 to 3, 7	Set to 0.
	ABSCS	Select the sampling timing to detect a bus collision.
	ACSE	Set to 1 to use the auto clear function of the transmit enable bit.
	SSS	Select the transmit start condition.
U2SMR2	0 to 7	Set to 0.
U2SMR3	0 to 7	Set to 0.
U2SMR4	0 to 7	Set to 0.

Notes:
1. This table does not describe a procedure.
2. Set the bits not listed above to 0 when writing to registers in IE mode.

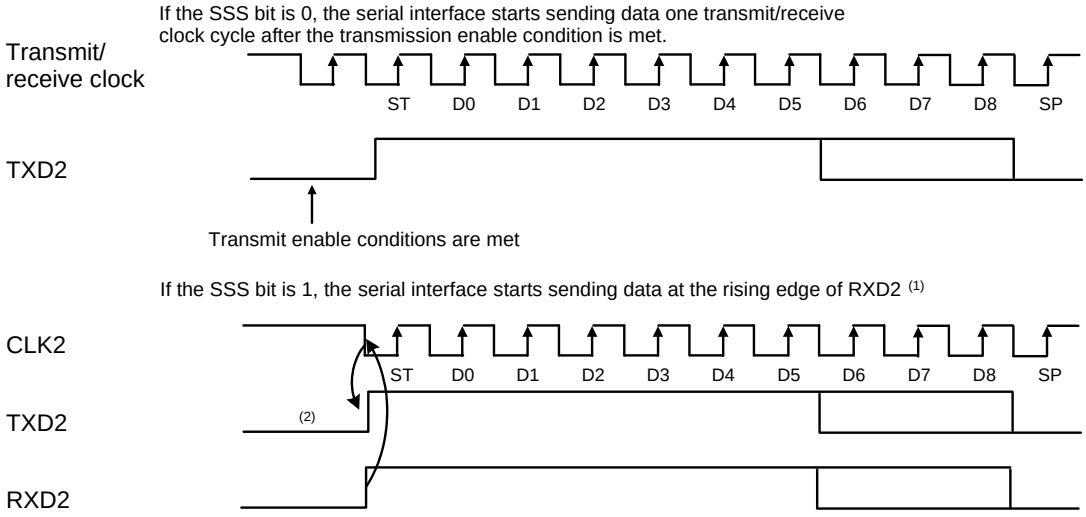
(1) The ABSCS Bit in the U2SMR Register (Bus collision detect sampling clock select)



(2) The ACSE Bit in the U2SMR Register (Auto clear of transmit enable bit)



(3) The SSS Bit in the U2SMR Register (Transmit start condition select)



Notes:
1. The falling edge of RXD2 when the IOPOL bit is 0; the rising edge of RXD2 when the IOPOL bit is1.
2. The transmit condition must be met before the falling edge of RXD2 (1).
   The above assumes the IOPOL bit is 1 (inverted).

Figure 21.29 Bus Collision Detect Function-Related Bits

21.3.6 Special Mode 4 (SIM Mode) (UART2)

In this mode, the serial interface module allows SIM interface devices to communicate in UART mode. Both direct and inverted formats are available. The TXD2 pin outputs a low-level signal when a parity error is detected.

Table 21.22 lists the specifications of SIM mode. Table 21.23 lists the related registers and their settings.

Table 21.22 SIM Mode Specifications

Item	Specification
Data formats	• Direct format • Inverted format
Transmit/receive clock	• The CKDIR bit in the U2MR register is 0 (internal clock): fi/(16(n + 1)) fi = f1SIO, f2SIO, f8SIO, f32SIO n = setting value of the U2BRG register 00h to FFh • The CKDIR bit is 1 (external clock): fEXT/(16(n + 1)) fEXT = input from the CLK2 pin n = setting value of the U2BRG register 00h to FFh
Transmission start conditions	To start transmission, satisfy the following requirements: • The TE bit in the U2C1 register is 1 (transmission enabled) • The TI bit in the U2C1 register is 0 (data present in the U2TB register)
Reception start conditions	To start reception, satisfy the following requirements: • The RE bit in the U2C1 register is 1 (reception enabled) • Start bit detection
Interrupt request generation timing (2)	• While transmitting When the serial interface completes transmitting data from the UART2 transmit register (the U2IRS bit is 1) • While receiving When transferring data from the UART2 receive register to the U2RB register (at completion of reception)
Error detection	• Overrun error (1) This error occurs if the serial interface starts receiving the next data before reading the U2RB register and receives the bit before the last stop bit of the next data. • Framing error (3) This error occurs when the number of stop bits set is not detected. • Parity error (3) During reception, if a parity error is detected, a parity error signal is output from the TXD2 pin. During transmission, a parity error is detected by the level of input to the RXD2 pin when a transmission interrupt occurs. • Error sum flag This flag becomes 1 when an overrun, framing, or parity errors occurs.

Notes:

1. If an overrun error occurs, the received data of the U2RB register will be undefined. The IR bit in the S2RIC register does not change.
2. After reset is deasserted, a transmit interrupt request is generated by setting bits U2IRS and U2ERE in the U2C1 register to 1 (transmission completed, error signal output), then setting the TE bit to 1 (transmission enabled) and the transmission data to the U2TB register. Therefore, when using SIM mode, make sure to set the IR bit to 0 (interrupt not requested) after setting these bits.
3. The timing at which the framing error flag and the parity error flag are set is detected when data is transferred from the UART2 receive register to the U2RB register.

Table 21.23 Registers Used and Settings in SIM Mode (1)

Register	Bit	Function
U2TB (2)	0 to 7	Set transmit data.
U2RB (2)	0 to 7	Received data can be read.
	OER, FER, PER, SUM	Error flag
U2BRG	0 to 7	Set a bit rate.
U2MR	SMD2 to SMD0	Set to 101b.
	CKDIR	Select the internal clock or external clock.
	STPS	Set to 0.
	PRY	Set to 1 in direct format or 0 in inverted format.
	PRYE	Set to 1.
	IOPOL	Set to 0.
U2C0	CLK0, CLK1	Select the count source for the U2BRG register.
	CRS	Disabled because CRD is 1.
	TXEPT	Transmit register empty flag
	CRD	Set to 1.
	NCH	Set to 1.
	CKPOL	Set to 0.
	UFORM	Set to 0 in direct format or 1 in inverted format.
U2C1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	U2IRS	Set to 1.
	U2RRM	Set to 0.
	U2LCH	Set to 0 in direct format or 1 in inverted format.
	U2ERE	Set to 1.
U2SMR (2)	0 to 3	Set to 0.
U2SMR2	0 to 7	Set to 0.
U2SMR3	0 to 7	Set to 0.
U2SMR4	0 to 7	Set to 0.

Notes:
1. This table does not describe a procedure.
2. Set bits not listed above to 0 when writing to the registers in SIM mode.

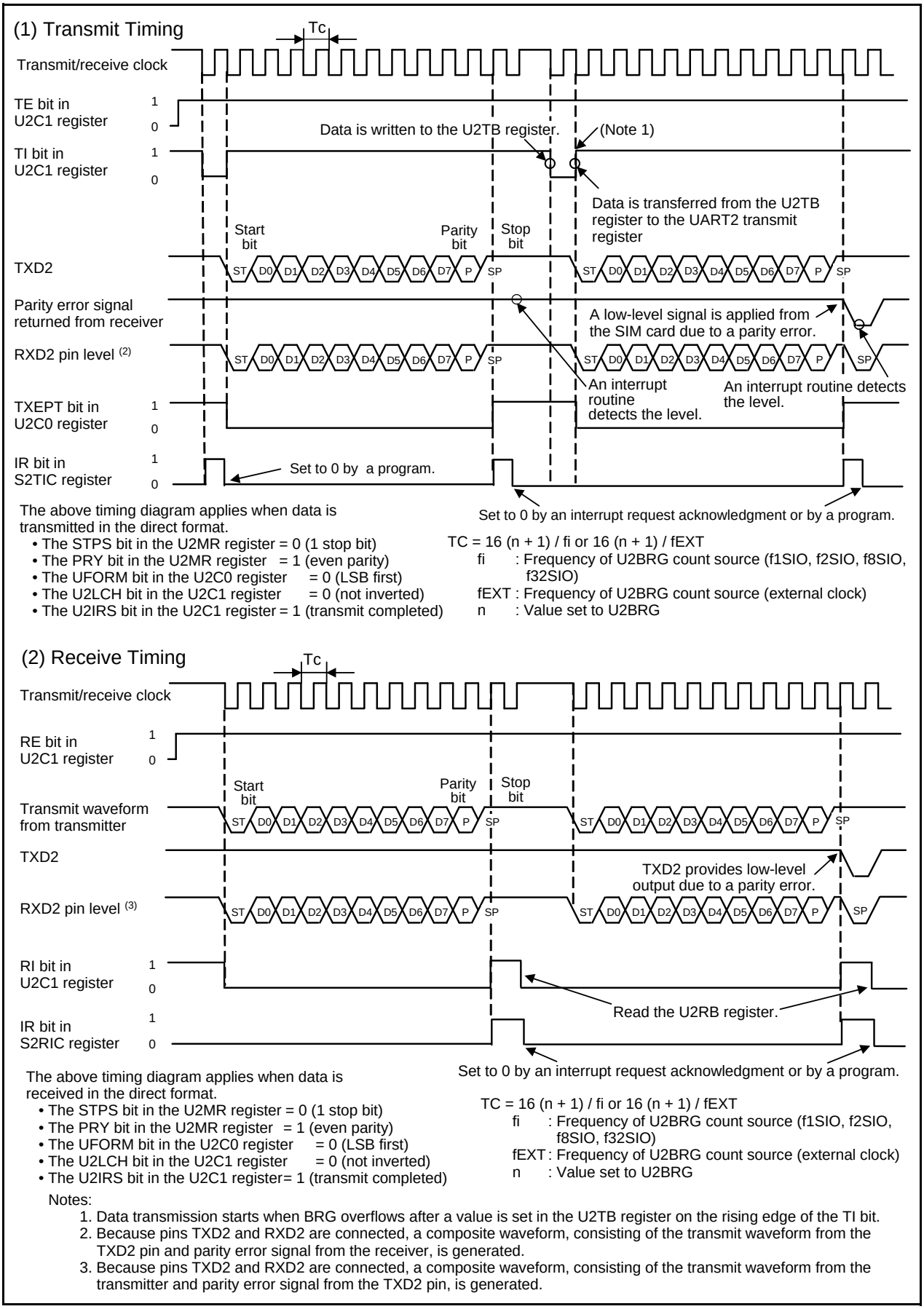


Figure 21.30 Transmit/Receive Timing in SIM Mode

Figure 21.31 shows the Example of SIM Interface Connection. Connect pins TXD2 and RXD2, and then place a pull-up resistance.

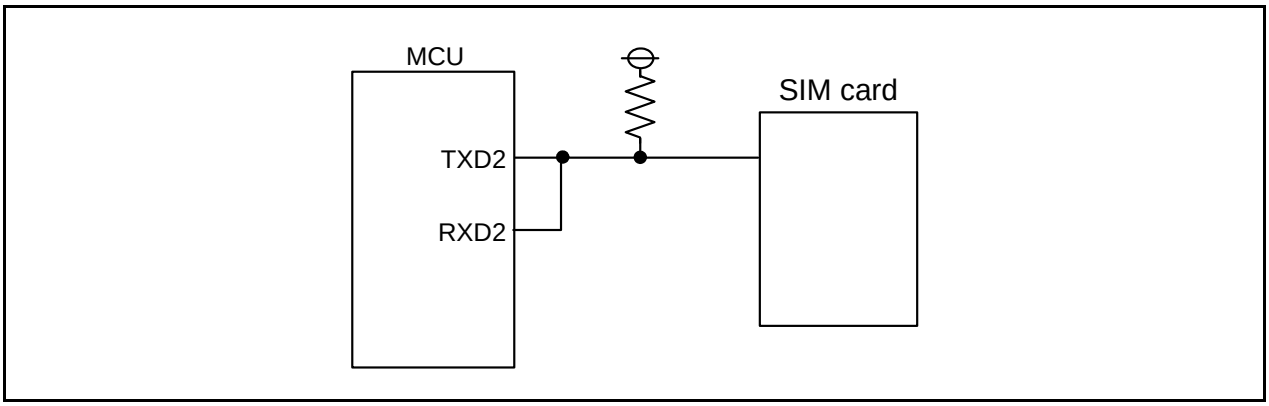


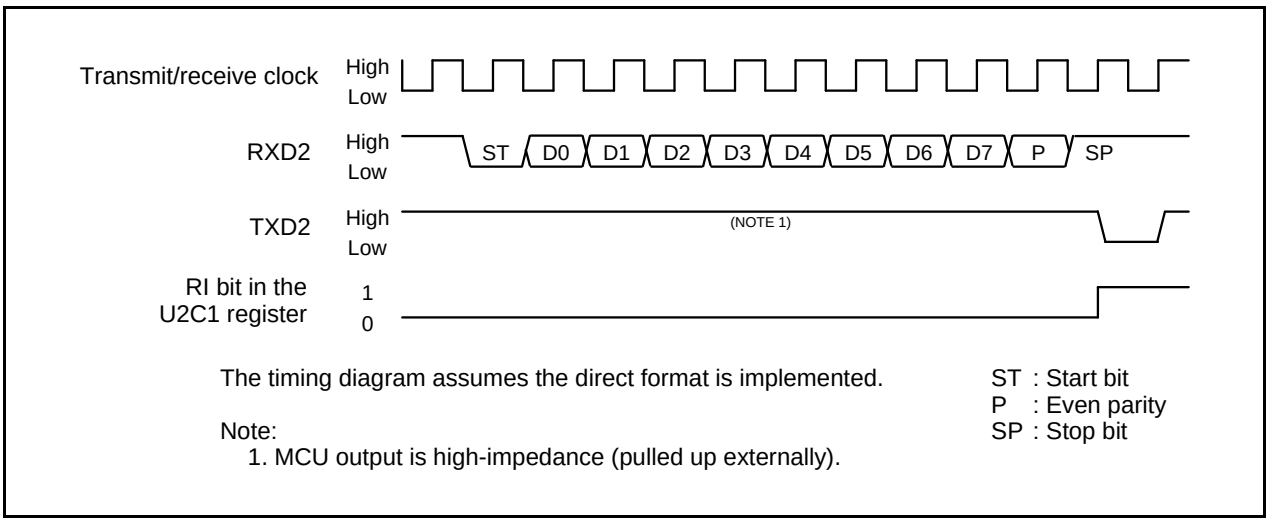
Figure 21.31 Example of SIM Interface Connection

21.3.6.1 Parity Error Signal Output

The parity error signal is enabled by setting the U2ERE bit in the U2C1 register to 1 (error signal output).

The parity error signal is output when a parity error is detected while receiving data. A low-level signal is output from the TXD2 pin in the timing shown in Figure 21.32. If the U2RB register is read while outputting a parity error signal, the PER bit is cleared to 0 (no parity error) and at the same time the TXD2 output again goes high.

When transmitting, a transmission complete interrupt request is generated at the falling edge of the transmit/receive clock pulse that immediately follows the stop bit. Therefore, whether a parity error signal has been returned can be determined by reading the port that shares the RXD2 pin in a transmission complete interrupt routine.



The timing diagram assumes the direct format is implemented.

ST : Start bit
P : Even parity
SP : Stop bit

Note:
1. MCU output is high-impedance (pulled up externally).

Figure 21.32 Parity Error Signal Output Timing

21.3.6.2 Formats

Two formats are available: direct format and inverse format.

For direct format, set the PRYE bit in the U2MR register to 1 (parity enabled), the PRY bit to 1 (even parity), the UFORM bit in the U2C0 register to 0 (LSB first), and the U2LCH bit in the U2C1 register to 0 (not inverted). When data is transmitted, data set in the U2TB register are transmitted with the even-numbered parity, starting from D0. When data is received, the received data is stored in the U2RB register, starting from D0. The even-numbered parity is used to determine whether a parity error occurs.

For inverted format, set the PRYE bit to 1, the PRY bit to 0 (odd parity), the UFORM bit to 1 (MSB first), and the U2LCH bit to 1 (inverted). When data is transmitted, values set in the U2TB register are logically inverted and are transmitted with the odd-numbered parity, starting from D7. When data is received, the received data is logically inverted to be stored in the U2RB register, starting from D7. The odd-numbered parity is used to determine whether a parity error occurs.

Figure 21.33 shows the SIM Interface Format.

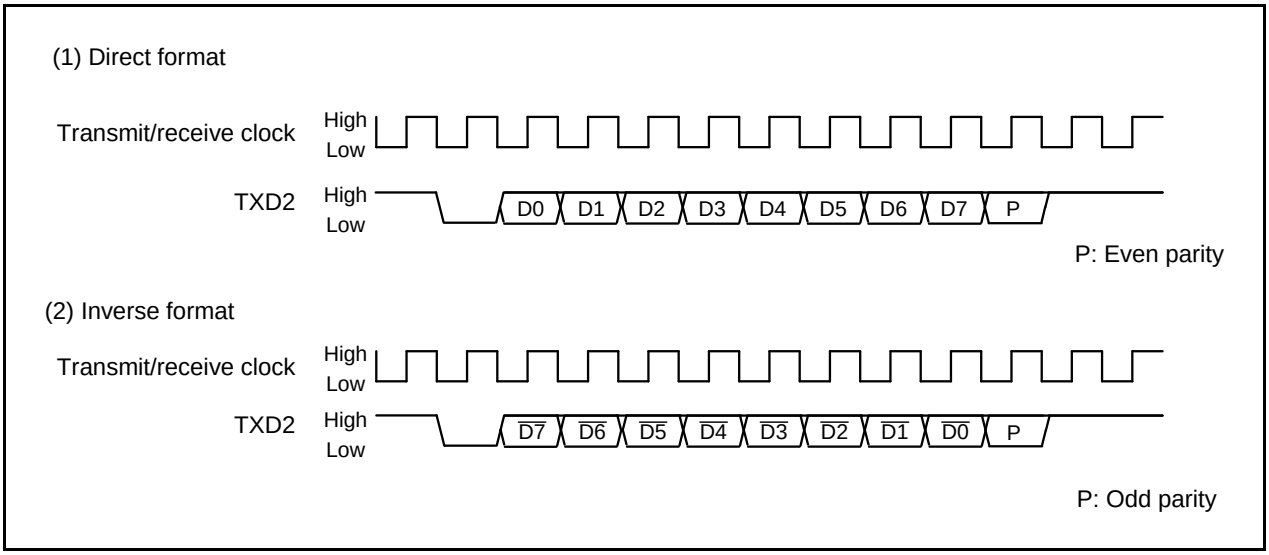


Figure 21.33 SIM Interface Format

21.4 Interrupts

UART0 to UART4 include interrupts by transmission, reception, ACK, NACK, start/stop condition detection, and bus collision detection.

21.4.1 Interrupt Related Registers

Refer to operation examples in each mode for interrupt sources and interrupt request generation timing. For details of interrupt control, refer to 12.7 “Interrupt Control”. Table 21.24 lists UART0 to UART4 Interrupt Related Registers.

Table 21.24 UART0 to UART4 Interrupt Related Registers

Address	Register	Symbol	Reset Value
004Ah	UART2 Bus Collision Detection Interrupt Control Register	BCNIC	XXXX X000b
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXX X000b
0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXX X000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXX X000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXX X000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXX X000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXX X000b
006Fh	UART4 Transmit Interrupt Control Register	S4TIC	XXXX X000b
0070h	UART4 Receive Interrupt Control Register	S4RIC	XXXX X000b
0072h	UART3 Transmit Interrupt Control Register	S3TIC	XXXX X000b
0073h	UART3 Receive Interrupt Control Register	S3RIC	XXXX X000b
0204h	Interrupt Source Select Register 4	IFSR4A	00h
0205h	Interrupt Source Select Register 3	IFSR3A	00h
0206h	Interrupt Source Select Register 2	IFSR2A	00h

Some interrupts of UART0 to UART4 share interrupt vectors and interrupt control registers with other peripheral functions. When using these interrupts, select them by interrupt source select registers. Table 21.25 lists Interrupt Selection in UART0 to UART4.

Table 21.25 Interrupt Selection in UART0 to UART4

Interrupt Source	Interrupt Source Select Register Settings		
	Register	Bit	Setting Value
UART2 start/stop condition detection, bus collision detection	IFSR2A	IFSR20	0
UART3 transmission	IFSR2A	IFSR25	0
UART3 reception	IFSR3A	IFSR32	0
UART4 transmission	IFSR3A	IFSR36	0
UART0 transmission	IFSR4A	IFSR43	0

In the following modes, an interrupt request can be generated by rewriting bit values.

- Special mode 1 (I^2C mode)
  Set the IR bit in the interrupt control register of UART2 to 0 (interrupt not requested), when the following bits are changed:
  Bits SMD2 to SMD0 in the U2MR register, the IICM bit in the U2SMR register, the IICM2 bit in the U2SMR2 register, the CKPH bit in the U2SMR3 register
- Special mode 4 (SIM mode)
  After reset, a transmit interrupt request is generated by setting bits U2IRS and U2ERE in the U2C1 register to 1 (transmission completed, error signal output), then setting the TE bit to 1 (transmission enabled) and the transmission data to the U2TB register. Therefore, when using SIM mode, make sure to set the IR bit to 0 (interrupt not requested) after setting these bits.

21.4.2 Reception Interrupt

- The case that bits SMD2 to SMD0 in the U2MR register are not set to 010b (I^2C mode)
  When the RI bit in the U2C1 register is changed from 0 (no data in the U2RB register) to 1 (data present in the U2RB register), the IR bit in the S2RIC register is automatically set to 1 (interrupt requested).
  If an overrun error occurs (when the RI bit is 1, the next data is received), the RI bit remains 1, and therefore, the IR bit in the S2RIC register remains unchanged.
- The case that bits SMD2 to SMD0 in the U2MR register are set to 010b (I^2C mode)
  When the RI bit in the U2C1 register is changed from 0 (no data in the U2RB register) to 1 (data present in the U2RB register), the IR bit in the S2RIC register is automatically set to 1 (interrupt requested).
  When an overrun error occurs, the IR bit in the S2RIC register also becomes 1.

21.5 Notes on Serial Interface UARTi (i = 0 to 4)

21.5.1 Common Notes on Multiple Modes

21.5.1.1 Influence of $\overline{SD}$

When a low-level signal is applied to the $\overline{SD}$ pin while the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on $\overline{SD}$ pin enabled), the following pins become high-impedance: P7_2/CLK2/TA1OUT/V/RXD1, P7_3/$\overline{CTS2}$/$\overline{RTS2}$/TA1IN/$\overline{V}$/TXD1, P7_4/TA2OUT/W/LIN0OUT, P7_5/TA2IN/$\overline{W}$/LIN0IN, P8_0/TA4OUT/U/TSUDA, P8_1/TA4IN/$\overline{U}$/TSUDB

21.5.1.2 Register Setting

Set the OCOSEL0 or OCOSEL1 bit in the UCLKSEL0 register before setting other registers associated with UART0 to UART4. After changing the OCOSEL0 or OCOSEL1 bit, set other registers associated with UART0 to UART4 again.

21.5.2 Clock Synchronous Serial I/O Mode

21.5.2.1 Transmission/Reception

When the $\overline{RTS}$ function is used with an external clock, the $\overline{RTSi}$ pin (i = 0 to 3) outputs a low-level signal, which informs the transmitting side that the MCU is ready for a receive operation. The $\overline{RTSi}$ pin outputs a high-level signal when a receive operation starts. Therefore, transmit timing and receive timing can be synchronized by connecting the $\overline{RTSi}$ pin to the $\overline{CTSi}$ pin on the transmitting side. The $\overline{RTS}$ function is disabled when an internal clock is selected.

21.5.2.2 Transmission

If the transmission is started while an external clock is selected and the TXEPT bit in the UiC0 register (i = 0 to 4) is 1 (no data present in transmit register), meet the last requirement at either of the following timings:

External clock level:

- The CKPOL bit in the UiC0 register is 0 (transmit data is output at the falling edge of transmit/receive clock and receive data is input at the rising edge) and the external clock is high.
- The CKPOL bit is 1 (transmit data is output at the rising edge of transmit/receive clock and receive data is input at the falling edge) and the external clock is low.

Requirements to start transmission (in no particular order):

- The TE bit in the UiC1 register is 1 (transmission enabled).
- The TI bit in the UiC1 register is 0 (data present in the UiTB register).
- When the $\overline{CTS}$ function is selected, input on the $\overline{CTSi}$ pin is low.

21.5.2.3 Reception

In clock synchronous serial I/O mode, a shift clock is generated by activating a transmitter. Set the UARTi-associated registers for a transmit operation even if the MCU is used for a receive operations only. Dummy data is output from the TXDi pin (i = 0 to 4) while receiving.

When an internal clock is selected, a shift clock is generated by setting the TE bit in the UiC1 register to 1 (transmission enabled) and placing dummy data in the UiTB register. When an external clock is selected, set the TE bit to 1 (transmission enabled), set dummy data in the UiTB register, and input an external clock to the CLKi pin to generate a shift clock.

If data is received consecutively, an overrun error occurs when the RI bit in the UiC1 register is 1 (data present in the UiRB register) and the next receive data is received in the UARTi receive register. Then, the OER bit in the UiRB register becomes 1 (overrun error occurred). At this time, the UiRB register is undefined. When an overrun error occurs, program the transmitting and receiving sides to retransmit the previous data. If an overrun error occurs again, the IR bit in the SiRIC register remains unchanged.

To receive data consecutively, set dummy data in the low-order byte in the UiTB register for each receive operation.

If the reception is started while an external clock is selected and the TXEPT bit in the UiC0 register is 1 (no data present in transmit register), meet the last requirement at either of the timings below.

External clock level:

- The CKPOL bit in the UiC0 register is 0 (transmit data is output at the falling edge of transmit/receive clock and receive data is input at the rising edge) and the external clock is high.
- The CKPOL bit is 1 (transmit data is output at the rising edge of transmit/receive clock and receive data is input at the falling edge) and the external clock is low.

Requirements to start reception (in no particular order):

- The RE bit in the UiC1 register is 1 (reception enabled).
- The TE bit in the UiC1 register is 1 (transmission enabled).
- The TI bit in the UiC1 register is 0 (data present in the UiTB register).

21.5.3 Special Mode 1 (I^2C Mode)

21.5.3.1 Generating Start and Stop Conditions

(Technical update number: TN-16C-130A/EA)

When generating start, stop, and restart conditions, set the STSPSEL bit in the U2SMR4 register to 0 and wait for more than a half cycle of the transmit/receive clock. Then set each condition generation bit (STAREQ, RSTAREQ, and STPREQ) from 0 to 1.

21.5.3.2 IR Bit

Set the following bits first, and then set the IR bit in each UART2 interrupt control register to 0 (interrupt not requested).

Bits SMD2 to SMD0 in the U2MR register, the IICM bit in the U2SMR register, the IICM2 bit in the U2SMR2 register, the CKPH bit in the U2SMR3 register

21.5.3.3 Setup and Hold Times When Generating a Start/Stop Condition

When generating a start condition, the hold time (t_{HD}:STA) is a half cycle of the SCL clock. When generating a stop condition, the setup time (t_{SU}:STO) is a half cycle of the SCL clock.

When the SDA digital delay function is enabled, take delay time into consideration (see 21.3.3.7 “SDA Digital Delay”).

The following shows a calculation example of hold and setup times when generating a start/stop condition.

Calculation example when setting 100 kbps

- U2BRG count source: f1 = 20 MHz
- U2BRG register setting value: n = 100 - 1
- SDA digital delay setting value: DL2 to DL0 are 101b (5 or 6 cycles of U2BRG count source)

f_{SCL} (theoretical value) = f1 / (2(n+1)) = 20 MHz / (2 × (99 + 1)) = 100 kbps

t_{DL} = delay cycle count / f1 = 6 / 20 MHz = 0.3 μs

$t_{HD:STA}$ (theoretical value) = 1 / (2f_{SCL} (theoretical value)) = 1 / (2 × 100 kbps) = 5 μs

$t_{SU:STO}$ (theoretical value) = 1 / (2f_{SCL} (theoretical value)) = 1 / (2 × 100 kbps) = 5 μs

$f_{HD:STA}$ (actual value) = $t_{HD:STA}$ (theoretical value) - t_{DL} = 5 μs - 0.3 μs = 4.7 μs

$f_{SU:STO}$ (actual value) = $t_{SU:STO}$ (theoretical value) + t_{DL} = 5 μs + 0.3 μs = 5.3 μs

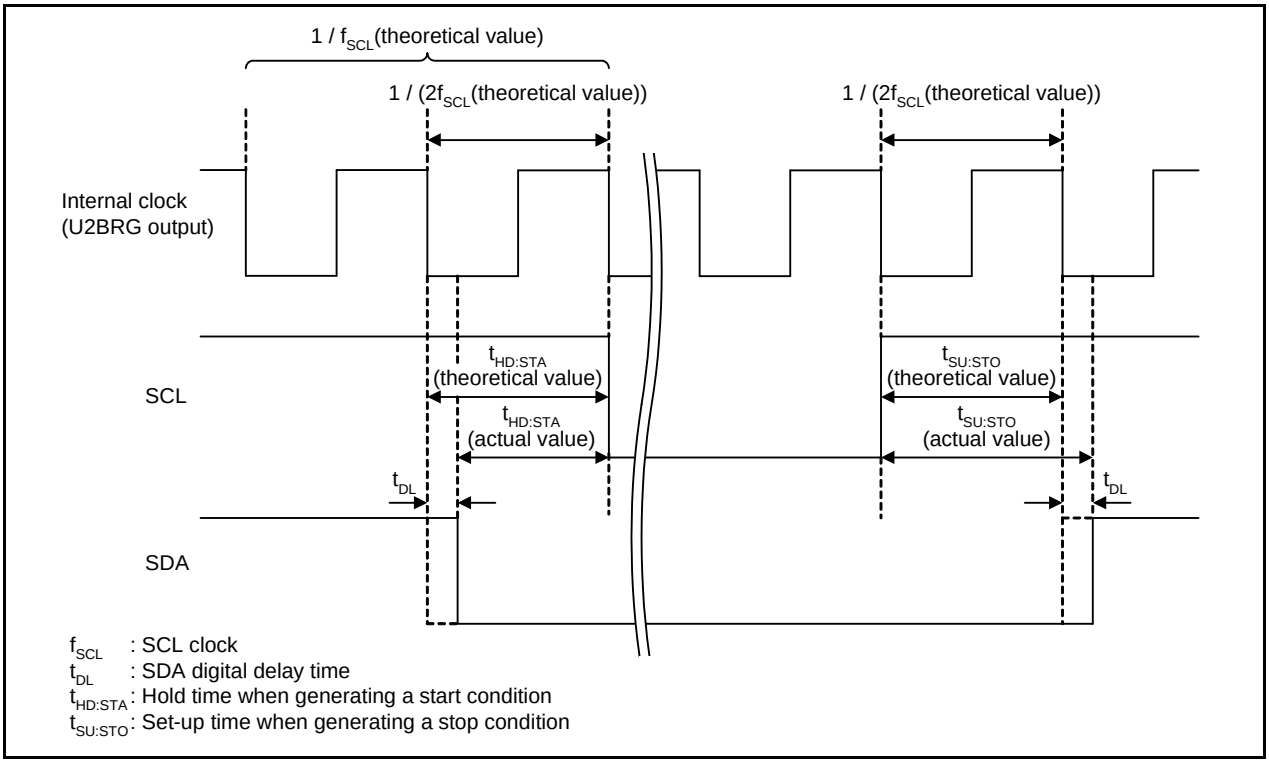


Figure 21.34 Setup and Hold Times When Generating Start and Stop Conditions

21.5.3.4 Restrictions on the Bit Rate When Using the U2BRG Count Source

In I^2C mode, set the U2BRG register to a value of 03h or greater.

A maximum of three U2BRG count source cycles are necessary until the internal circuit acknowledges the SCL clock level. The connectable I^2C-bus bit rate is one-third or less than the U2BRG count source speed. If a value between 00h to 02h is set to the U2BRG register, bit slippage may occur.

21.5.3.5 Restart Condition in Slave Mode

When a restart condition is detected in slave mode, the successive processes may not be executed correctly. In slave mode, do not use a restart condition.

21.5.3.6 Requirements to Start Transmission/Reception in Slave Mode

When transmission/reception is started in slave mode and the TXEPT bit in the UiC0 register is 1 (no data present in transmit register), meet the last requirement when the external clock is high.

Requirements to start transmission (in no particular order):

- The TE bit in the U2C1 register is 1 (transmission enabled).
- The TI bit in the U2C1 register is 0 (data present in the UiTB register).

Requirements to start reception (in no particular order):

- The RE bit in the U2C1 register is 1 (reception enabled).
- The TE bit in the U2C1 register is 1 (transmission enabled).
- The TI bit in the U2C1 register is 0 (data present in the UiTB register).

21.5.4 Special Mode 4 (SIM Mode)

(Technical update number: TN-M16C-101-0309)

After reset is deasserted, a transmit interrupt request is generated by setting bits U2IRS and U2ERE in the U2C1 register to 1 (transmission completed, error signal output), then setting the TE bit to 1 (transmission enabled) and the transmission data to the U2TB register. Therefore, when using SIM mode, make sure to set the IR bit to 0 (interrupt not requested) after setting these bits.

22. Multi-master I2C-bus Interface

22.1 Introduction

The multi-master I2C-bus interface (I2C interface) is a serial communication circuit based on the I2C-bus data transmit/receive format, and is equipped with arbitration lost detect and clock synchronous functions. Table 22.1 lists the Multi-master I2C-bus Interface Specifications, Table 22.2 lists the I2C Interface Detection Function, Figure 22.1 shows the Multi-master I2C-bus Interface Block Diagram, and Table 22.3 lists the I/O Ports.

Table 22.1 Multi-master I2C-bus Interface Specifications

Item	Function
Formats	Based on I2C-bus standard: 7-bit addressing format Fast-mode Standard clock mode
Communication modes	Based on I2C-bus standard: Master transmission Master reception Slave transmission Slave reception
Bit rate	16.1 kbps to 400 kbps (fVIIC = 4 MHz)
I/O pins	Serial data line SDAMM (SDA) Serial clock line SCLMM (SCL)
Interrupt request generating sources	• I2C-bus interrupt Completion of transmission Completion of reception Slave address match detection General call detection Stop condition detection Timeout detection • SDA/SCL interrupt Rising or falling edge of the signal of the SDAMM or SCLMM pin
Selectable functions	• I2C-bus interface pin input level select Selectable input level with I2C-bus input level or SMBus input level • Timeout detection A function that detects when the SCLMM pin is driven high over a certain period of time when the bus is busy. • Free data format select A function that generates an interrupt request when receiving the first byte of data, regardless of the slave address value.

fVIIC: I2C-bus system clock

Table 22.2 I2C Interface Detection Function

Item	Function
Slave address match detection	A function to detect a slave address match when in slave transmission/reception. If slave address match is detected, an ACK is returned. If the slave address match is not detected, a NACK is returned, and no further data is transmitted/received. Up to three slave addresses can be set.
General call detection	A function to detect a general call in slave reception.
Arbitration lost detection	A function to detect arbitration lost and stop the output from pins SDAMM and SCLMM.
Bus busy detection	A function to detect a bus busy state and set/reset the BB bit.

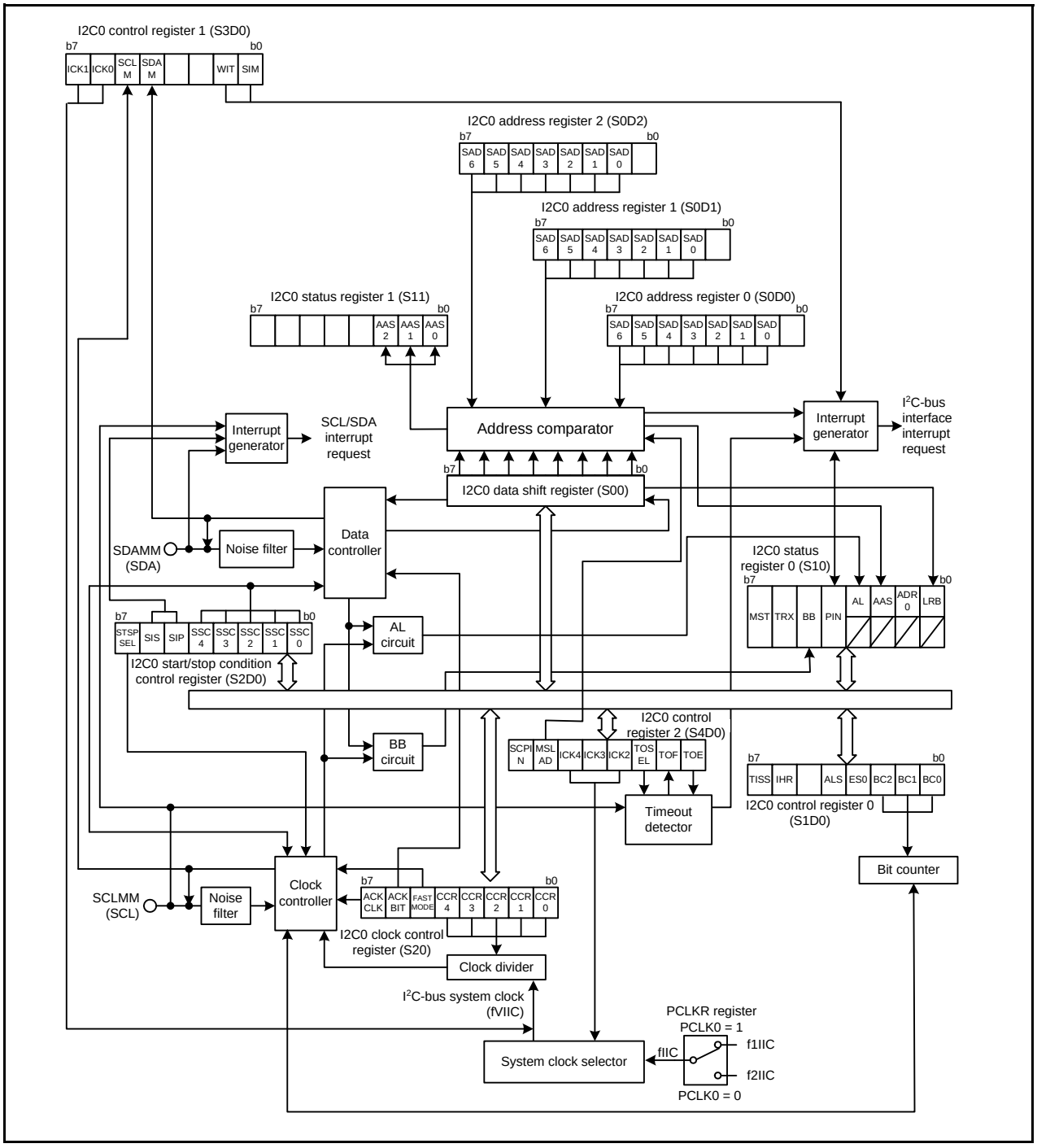


Figure 22.1 Multi-master I2C-bus Interface Block Diagram

Table 22.3 I/O Ports

Pin Name	I/O	Function
SDAMM	I/O	I/O pin for SDA (N-channel open drain output) (1)
SCLMM	I/O	I/O pin for SCL (N-channel open drain output) (1)

Note:
1. This function disables the P-channel transistor of CMOS output buffer for at all time. However, it does not make the SDAMM and SCLMM open drain output completely. Refer to electrical characteristics on input voltage range.

22.2 Registers Descriptions

Table 22.4 lists registers associated with multi-master I2C-bus interface. When the CM07 bit in the CM0 register is set to 1 (sub clock is CPU clock), registers listed in Table 22.4 should not be accessed. Set them after the CM07 bit is set to 0 (main clock, PLL clock, or on-chip oscillator clock).

Table 22.4 Registers

Address	Register	Symbol	Reset Value
02B0h	I2C0 Data Shift Register	S00	XXh
02B2h	I2C0 Address Register 0	S0D0	0000 000Xb
02B3h	I2C0 Control Register 0	S1D0	00h
02B4h	I2C0 Clock Control Register	S20	00h
02B5h	I2C0 Start/Stop Condition Control Register	S2D0	0001 1010b
02B6h	I2C0 Control Register 1	S3D0	0011 0000b
02B7h	I2C0 Control Register 2	S4D0	00h
02B8h	I2C0 Status Register 0	S10	0001 000Xb
02B9h	I2C0 Status Register 1	S11	XXXX X000b
02BAh	I2C0 Address Register 1	S0D1	0000 000Xb
02BBh	I2C0 Address Register 2	S0D2	0000 000Xb

22.2.1 I2C0 Data Shift Register (S00)

I2C0 Data Shift Register

b7 b0	Symbol	Address	Reset Value
	S00	02B0h	XXh

Function	RW
Transmit/receive data is stored.	RW

When the I2C interface is a transmitter, write transmit data to the S00 register. When the I2C interface is a receiver, received data can be read from the S00 register. In master mode, this register is also used to generate a start condition or stop condition on a bus. (Refer to 22.3.2 “Generating a Start Condition” and 22.3.3 “Generating a Stop Condition”.)

Write to the S00 register when the ES0 bit in the S1D0 register is 1 (I2C interface enabled).

Do not write to the S00 register when transmitting/receiving data.

When the I2C interface is a transmitter, the data in the S00 register is transmitted to other devices. The MSB (bit 7) is transmitted first, synchronizing with the SCLMM clock. Every time 1-bit data is output, the S00 register value is shifted 1 bit to the left.

When the I2C interface is a receiver, data is transferred to the S00 register from other devices. The LSB (bit 0) is input first, synchronizing with the SCLMM clock. Every time 1-bit data is output, the S00 register value is shifted 1 bit to the left. Figure 22.2 shows Timing to Store Received Data to the S00 Register.

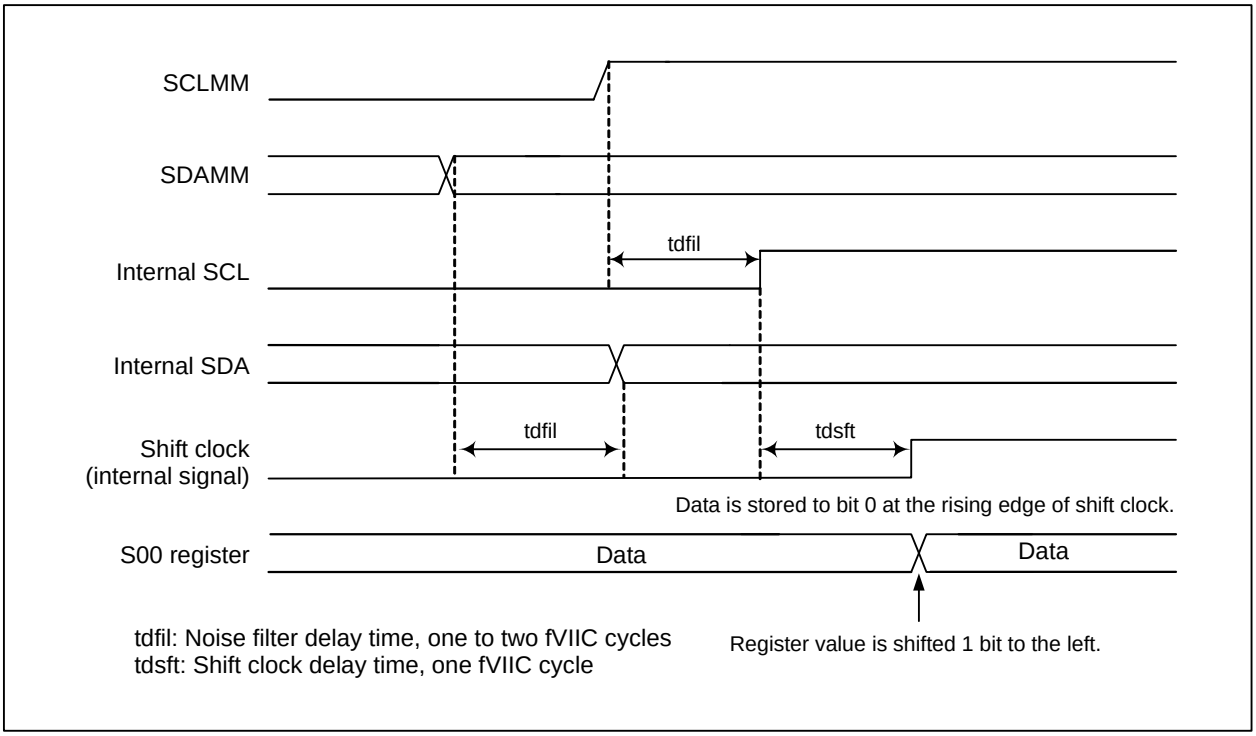
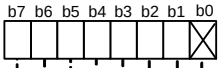


Figure 22.2 Timing to Store Received Data to the S00 Register

22.2.2 I2C0 Address Register i (S0Di) (i = 0 to 2)

I2C0 Address Register i (i = 0 to 2)



Symbol	Address	Reset Value
S0D0	02B2h	0000 000Xb
S0D1	02BAh	0000 000Xb
S0D2	02BBh	0000 000Xb

Bit Symbol	Bit Name	Function	RW
— (b0)	No register bit. If necessary, set to 0. The read value is undefined.		—
SAD0	Slave address	Set a slave address	RW
SAD1			RW
SAD2			RW
SAD3			RW
SAD4			RW
SAD5			RW
SAD6			RW

SAD6 to SAD0 (Slave address) (b7-b1)

Bits SAD6 to SAD0 indicate a slave address to be compared for a slave address match detection in slave mode. Up to three slave addresses can be set. Set the S0Di register to 00h when not setting the slave address.

However, when the MSLAD bit in the S4D0 register is 0, registers S0D1 and S0D2 are disabled. Only the slave address set to the S0D0 register is compared with address the data received.

22.2.3 I2C0 Control Register 0 (S1D0)

I2C0 Control Register 0

b7	b6	b5	b4	b3	b2	b1	b0
		0					

Symbol	Address	Reset Value
S1D0	02B3h	00h

Bit Symbol	Bit Name	Function	RW
BC0	Bit counter (number of transmitted/received bits)	b2 b1 b0 0 0 0: 8 0 0 1: 7 0 1 0: 6 0 1 1: 5 1 0 0: 4 1 0 1: 3 1 1 0: 2 1 1 1: 1	RW
BC1			RW
BC2			RW
ES0	I2C-bus interface enable bit	0: Disabled 1: Enabled	RW
ALS	Data format select bit	0: Addressing format 1: Free data format	RW
— (b5)	Reserved bit	Set to 0.	RW
IHR	I2C-bus interface reset bit	0: Reset is deasserted (automatically) 1: Reset	RW
TISS	I2C-bus interface pin input level select bit	0: I2C-bus input 1: SMBus input	RW

BC2 to BC0 (Bit counter) (b2-b0)

Bits BC2 to BC0 become 000b (8 bits) when a start condition is detected.
When the ACKCLK bit in the S20 register is 0 (no ACK clock), and data for the number of bits selected by bits BC2 to BC0 is transmitted or received, bits BC2 to BC0 become 000b again.
When the ACKCLK bit in the S20 register is 1 (ACK clock), and data for the number of bits selected and an ACK is transmitted or received, bits BC2 to BC0 become 000b again.

ES0 (I2C-bus interface enable bit) (b3)

The ES0 bit enables the I2C interface.
When the ES0 bit is set to 0, the I2C interface becomes as follows:

- Pins SDAMM and SCLMM: I/O ports or other peripheral pins
- The S00 register is write disabled.
- The I2C-bus system clock (hereinafter called fVIIC) stops.
- S10 register
  - ADR0 bit: 0 (general call not detected)
  - AAS bit: 0 (slave address not matched)
  - AL bit: 0 (arbitration lost not detected)
  - PIN bit: 1 (no I2C-bus interrupt request)
  - BB bit: 0 (bus free)
  - TRX bit: 0 (receive mode)
  - MST bit: 0 (slave mode)

- Bits AAS2 to AAS0 in the S11 register: 0 (slave address not matches)
- The TOF bit in the S4D0 register: 0 (timeout not detected)

ALS (Data format select bit) (b4)

The ALS bit is enabled in slave mode. When the ALS bit is 0 (addressing format), the slave address match detection is performed.
When a slave address stored to bits SAD6 to SAD0 in the S0Di register (i = 0 to 2) is compared and matched with the calling address by a master, or when a general call address is received, the IR bit in the IICIC register becomes 1 (interrupt requested).
When the ALS bit is 1 (free data format), the slave address match detection is not performed. Therefore, the IR bit in the IICIC register becomes 1 (interrupt requested), regardless of the calling address by a master.

IHR (I2C-bus interface reset bit) (b6)

The IHR bit resets the I2C interface if there is an anomaly during transmission/reception. When the ES0 bit in the S1D0 register is 1 (I2C interface enabled) and then the IHR bit is set to 1 (reset), the I2C interface becomes as follows:

- S10 register
  - ADR0 bit: 0 (general call not detected)
  - AAS bit: 0 (slave address not matched)
  - AL bit: 0 (arbitration lost not detected)
  - PIN bit: 1 (No I2C-bus interrupt request)
  - BB bit: 0 (bus free)
  - TRX bit: 0 (receive mode)
  - MST bit: 0 (slave mode)
- Bits AAS2 to AAS0 in the S11 register: 0 (slave address not matches)
- TOF bit in the S4D0 register: 0 (timeout not detected)

When the IHR bit is set to 1, the I2C interface is reset and the IHR bit becomes 0 automatically. It takes a maximum of 2.5 fVIIC cycles to complete the reset sequence.
Figure 22.3 shows the I2C Interface Reset Timing.

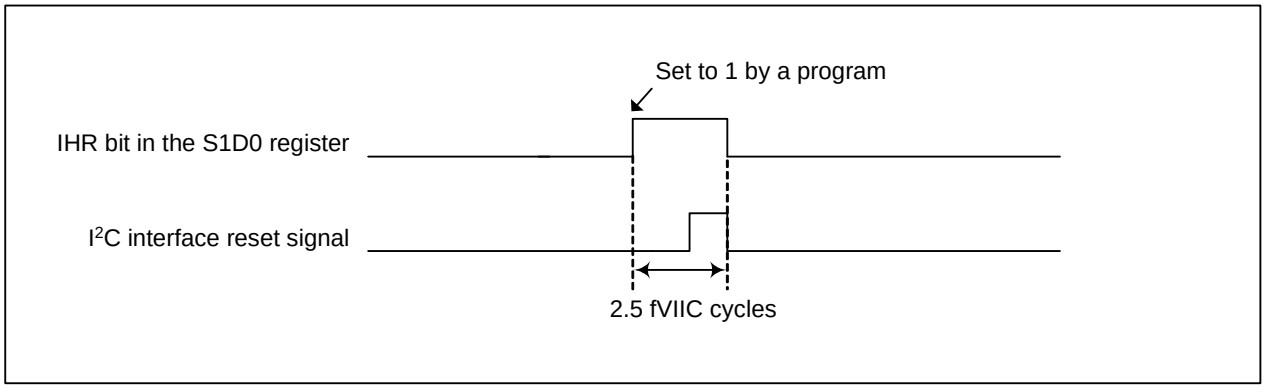


Figure 22.3 I2C Interface Reset Timing

TISS (I2C-bus interface pin input level select bit) (b7)

Set the TISS bit to select the input level of the SCLMM pin and SDAMM pin for the I2C interface.

22.2.4 I2C0 Clock Control Register (S20)

I2C0 Clock Control Register

b7 b6 b5 b4 b3 b2 b1 b0	Symbol	Address	Reset Value
	S20	02B4h	00h

Bit Symbol	Bit Name	Function	RW
CCR0	Bit rate control bit	Refer to bits CCR4 to CCR0 (Bit Rate Control Bit) (b4 to b0) in the next page.	RW
CCR1			RW
CCR2			RW
CCR3			RW
CCR4			RW
FASTMODE	SCL mode select bit	0: Standard-speed clock mode 1: Fast-mode	RW
ACKBIT	ACK bit	0: ACK is returned 1: ACK is not returned	RW
ACKCLK	ACK clock bit	0: No ACK clock present 1: ACK clock present	RW

CCR4 to CCR0 (Bit rate control bit) (b4-b0)

Assuming the CCR value (3 to 31) is the value set to bits CCR4 to CCR0, the bit rate can be calculated using the following equation:
Refer to 22.3.1.2 “Bit Rate and Duty Cycle” for more details.

In standard-speed clock mode,

$$\text{Bit rate} = \frac{\text{fVIIC}}{8 \times \text{CCR value}} \leq 100 \text{ kbps}$$

When the CCR value is other than 5 in fast-mode,

$$\text{Bit rate} = \frac{\text{fVIIC}}{4 \times \text{CCR value}} \leq 400 \text{ kbps}$$

When the CCR value is 5 in fast-mode, the bit rate is assumed to reach 400 kbps, the maximum bit rate in fast-mode.

$$\text{Bit rate} = \frac{\text{fVIIC}}{2 \times \text{CCR value}} = \frac{\text{fVIIC}}{10} \leq 400 \text{ kbps}$$

Do not set the CCR value from 0 to 2 regardless of the fVIIC frequency.
Rewrite bits CCR4 to CCR0 when the ES0 bit in the S1D0 register is 0 (disabled).

FASTMODE (SCL mode select bit) (b5)

When using the fast-mode I2C-bus standard (maximum 400 kbps), set the FASTMODE bit to 1 (fast-mode) and set fVIIC to 4 MHz or more.
Rewrite the FASTMODE bit when the ES0 bit in the S1D0 register is 0 (disabled).

ACKBIT (ACK bit) (b6)

The ACK bit is enabled in master reception, slave reception, or slave address reception. When receiving a slave address, the SDAMM pin level during the ACK clock pulse is determined by a combination of bits ALS and ACKBIT in the S1D0 register and the received slave address.
When receiving data, the SDAMM pin level during the ACK clock pulse is determined by the ACKBIT bit. Table 22.5 lists the SDAMM Pin Level during the ACK Clock Pulse.

Table 22.5 SDAMM Pin Level during the ACK Clock Pulse

Received Content	ALS Bit in the S1D0 Register	ACKBIT Bit in the S20 Register	Slave Address Content	SDAMM Pin Level at ACK Clock
Slave Address	0	0	When the MSLAD bit in the S4D0 register is 0: Matched with bits SAD6 to SAD0 in the S0D0 register. When the MSLAD bit is 1: Matched with bits SAD6 to SAD0 in any of registers S0D0 to S0D2.	Low (ACK)
			0000000b	Low (ACK)
			Others	High (NACK)
		1	—	High (NACK)
	1	0	—	Low (ACK)
		1	—	High (NACK)
Data	—	0	—	Low (ACK)
		1	—	High (NACK)

ACKCLK (ACK clock bit) (b7)

When the ACKCLK bit is 1 (ACK clock present), an ACK clock is generated immediately after 1-byte data is transmitted or received (8 clocks).
When the ACKCLK bit is 0 (no ACK clock), no ACK clock is generated after 1-byte data is transmitted or received (8 clocks). At the falling edge of data transmission/reception (the falling edge of the eighth clock), the IR bit in the IICIC register becomes 1 (interrupt requested).
Do not write to this bit when transmitting/receiving data.

22.2.5 I2C0 Start/Stop Condition Control Register (S2D0)

I2C0 Start/Stop Condition Control Register

b7 b6 b5 b4 b3 b2 b1 b0	Symbol	Address	Reset Value
	S2D0	02B5h	0001 1010b

Bit Symbol	Bit Name	Function	RW
SSC0	Start/stop condition setting bit	Refer to SSC4 to SSC0 (Start/Stop Condition Setting Bit) (b4 to b0) in the same page	RW
SSC1			RW
SSC2			RW
SSC3			RW
SSC4			RW
SIP	SCL/SDA interrupt pin polarity select bit	0: Falling edge 1: Rising edge	RW
SIS	SCL/SDA interrupt pin select bit	0: SDAMM 1: SCLMM	RW
STSPSEL	Start/stop condition generation select bit	0: Short setup/hold time mode 1: Long setup/hold time mode	RW

SSC4 to SSC0 (Start/stop condition setting bit) (b4-b0)

Set bits SSC4 to SSC0 to select the start/stop condition detect parameter (SCL open time, setup time, hold time) in standard-speed clock mode. Refer to 22.3.7 “Detecting Start/Stop Conditions”.
Do not set an odd value or 00000b to these bits.

SIP (SCL/SDA interrupt pin polarity select bit) (b5)
SIS (SCL/SDA interrupt pin select bit) (b6)

The IR bit in the SCLDAIC register becomes 1 (interrupt requested) when the I2C interface detects the edge selected by the SIP bit for the pin signal selected by the SIS bit. Refer to 22.4 “Interrupts”.

STSPSEL (Start/stop condition generation select bit) (b7)

See Table 22.12 “Setup/Hold Time for Generating a Start/Stop Condition”.
If the fVIIC frequency is more than 4 MHz, set the STSPSEL bit to 1 (long mode).

22.2.6 I2C0 Control Register 1 (S3D0)

I2C0 Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0
				0	0		

Symbol	Address	Reset Value
S3D0	02B6h	0011 0000b

Bit Symbol	Bit Name	Function	RW
SIM	Stop condition detect interrupt enable bit	0: I2C-bus interrupt by stop condition detection is disabled 1: I2C-bus interrupt by stop condition detection is enabled	RW
WIT	Data receive interrupt enable bit	When write, 0: I2C-bus interrupt at the 8th clock is disabled 1: I2C-bus interrupt at the 8th clock is enabled When read, internal WAIT bit monitor 0: I2C-bus interrupt by falling edge of ACK clock 1: I2C-bus interrupt at the 8th clock	RW
— (b3-b2)	Reserved bits	Set to 0	RW
SDAM	Internal SDA output monitor bit	0: Logic 0 output 1: Logic 1 output	RO
SCLM	Internal SCL output monitor bit	0: Logic 0 output 1: Logic 1 output	RO
ICK0	I2C-bus system clock select bit (Enabled when bits ICK4 to ICK2 in the S4D0 register are 000b)	b7 b6 0 0: fIIC divided by 2 0 1: fIIC divided by 4 1 0: fIIC divided by 8 1 1: Should not be set	RW
ICK1			RW

Do not use the bit managing instruction (read-modify-write instruction) to access the S3D0 register. Use the MOV instruction to write to the S3D0 register.

SIM (Stop condition detect interrupt enable bit) (b0)

When the SIM bit is 1 (I2C-bus interrupt by stop condition detection enabled) and a stop condition is detected, the SCPIN bit in the S4D0 register becomes 1 (stop condition detect interrupt requested) and the IR bit in the IICIC register becomes 1 (interrupt requested).

WIT (Data receive interrupt enable bit) (b1)

The WIT bit is enabled in master reception or slave reception.
The WIT bit has two functions:

- Selects the I2C-bus interrupt timing when data is received. (write)
- Monitors the state of the internal WAIT flag. (read)

The WIT bit can select whether to generate an I2C-bus interrupt request at eighth clock (before ACK clock) during the data reception.
When the ACKCLK bit in the S20 register is 1 (ACK clock presents) and the WIT bit is set to 1 (enable I2C-bus interrupt at 8th clock), an I2C-bus interrupt request is generated at the eighth clock (before the ACK clock). Then, the PIN bit in the S10 register becomes 0 (interrupt requested).
When the ACKCLK bit in the S20 register is 0 (no ACK clock presents), write 0 to the WIT bit to disable the I2C-bus interrupt by data reception.
When transmitting data and receiving a slave address, no interrupt requests are generated at the eighth clock (before the ACK clock) regardless of the value written to the WIT bit.
Reading the WIT bit returns the internal WAIT flag status.
An I2C-bus interrupt request is generated at the falling edge of the ninth clock (ACK clock) regardless of the value written to the WIT bit. Then, the PIN bit in the S10 register becomes 0 (interrupt requested). Therefore, read the internal WAIT flag status to determine whether the I2C-bus interrupt request is generated at the eighth clock (before the ACK clock) or at the falling edge of the ACK clock.
When the WIT bit is set to 1 (I2C-bus interrupt enabled by receiving data), the internal WAIT flag changes under the following conditions:
Condition to become 0:

- The S20 register (ACKBIT bit) is written.

Condition to become 1:

- The S00 register is written during data reception.

When transmitting data and receiving a slave address, the internal WAIT flag is 0 and the I2C-bus interrupt request will be generated only at the falling edge of the ninth clock (ACK clock), regardless of the value written to the WIT bit.
Table 22.6 lists interrupt request generation timing and the conditions to restart transmission/reception when receiving data. Figure 22.4 shows Interrupt Request Generation Timing in Receive Mode.

Table 22.6 Generating an Interrupt Request and Restarting Transmission/Reception When Receiving Data

I2C-bus Interrupt Request Generation Timing	Internal WAIT Flag Status	Conditions to Restart Transmission/Reception
At the falling edge of the eighth clock (before the ACK clock) (1)	1	Write to the ACKBIT bit in the S20 register (3)
At the falling edge of the ninth clock (ACK clock) (2)	0	Write to the S00 register

Notes:
1. See the timing of (1) on the IR bit in the IICIC register in Figure 22.4.
2. See the timing of (2) on the IR bit in the IICIC register in Figure 22.4.
3. When setting the ACKBIT bit, do not rewrite any other bits and do not set the S00 register.

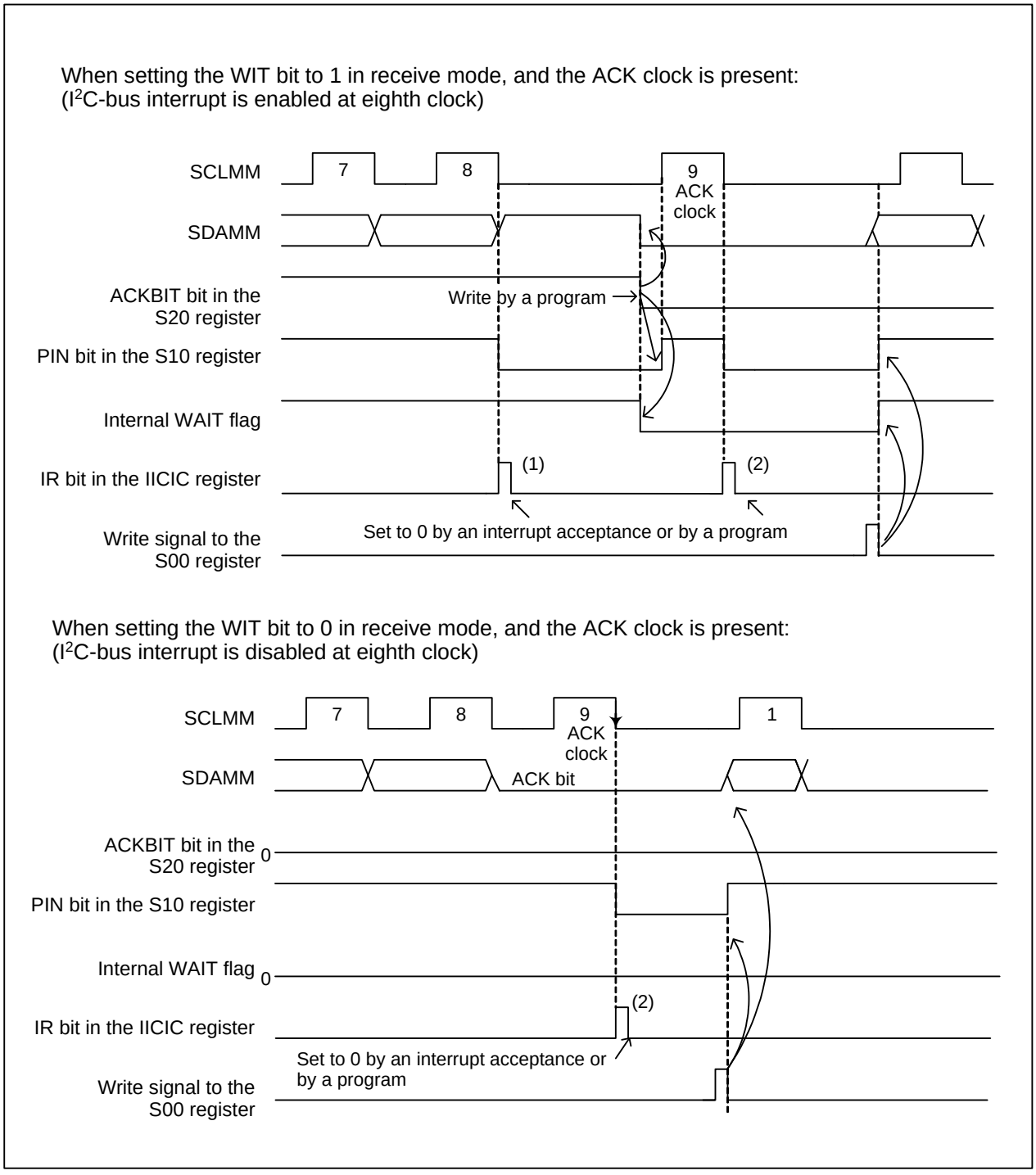


Figure 22.4 Interrupt Request Generation Timing in Receive Mode

SDAM (Internal SDA output monitor bit) (b4)
SCLM (Internal SCL output monitor bit) (b5)

The internal SDA and SCL output signal levels are the same as the output level of the I2C interface before it has any effect from the external device output. Bits SDAM and SCLM are read only bits. If necessary, set these bits to 0.

ICK1 and ICK0 (I2C-bus system clock select bit) (b7-b6)

Rewrite these bits when the ES0 bit in the S1D0 register is 0 (I2C interface disabled). fVIIC is selected by setting all the bits ICK1 to ICK0, bits ICK4 to ICK2 in the S4D0 register, and the PCLK0 bit in the PCLKR register. Refer to 22.3.1.2 “Bit Rate and Duty Cycle”.

Table 22.7 I2C-bus System Clock Select Bits

S4D0 Register			S3D0 Register		fVIIC
ICK4 Bit	ICK3 Bit	ICK2 Bit	ICK1 Bit	ICK0 Bit	
0	0	0	0	0	fIIC divided-by-2
0	0	0	0	1	fIIC divided-by-4
0	0	0	1	0	fIIC divided-by-8
0	0	1	–	–	fIIC divided-by-2.5
0	1	0	–	–	fIIC divided-by-3
0	1	1	–	–	fIIC divided-by-5
1	0	0	–	–	fIIC divided-by-6

–: 0 or 1
Only set the values listed above.

22.2.7 I2C0 Control Register 2 (S4D0)

I2C0 Control Register 2

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	Reset Value
								S4D0	02B7h	00b

Bit Symbol	Bit Name	Function	RW
TOE	Timeout detect function enable bit	0: Disabled 1: Enabled	RW
TOF	Timeout detect flag	0: Not detected 1: Detected	RO
TOSEL	Timeout detect time select bit	0: Long time 1: Short time	RW
ICK2	I2C-bus system clock select bit	b5 b4 b3 0 0 0: Bits ICK1 and ICK0 in the S3D0 register are enabled 0 0 1: fIIC divided by 2.5 0 1 0: fIIC divided by 3 0 1 1: fIIC divided by 5 1 0 0: fIIC divided by 6 Only set the values listed above.	RW
ICK3			RW
ICK4			RW
MSLAD	Slave address control bit	0: S0D0 register only 1: Registers S0D0 to S0D2	RW
SCPIN	Stop condition detect interrupt request bit	0: I2C-bus interrupt not requested 1: I2C-bus interrupt requested	RW

TOE (Timeout detect function enable bit) (b0)

The TOE bit enables the timeout detect function. Refer to 22.3.9 “Timeout Detection” for details.

TOF (Timeout detect flag) (b1)

The TOF bit is enabled when the TOE bit is set to 1. When the TOF bit becomes 1 (detected), the IR bit in the IICIC register becomes 1 (interrupt requested) at the same time.

Conditions to become 0:

- The ES0 bit in the S1D0 register is set to 0 (I2C interface disabled).
- The IHR bit in the S1D0 register is set to 1 (I2C interface reset).

Condition to become 1:

- The BB bit in the S10 register is set to 1 (bus busy) and the SCLMM high period is greater than the timeout detect period.

TOSEL (Timeout detect time select bit) (b2)

Set the TOSEL bit to select a timeout detection period. The TOSEL bit is enabled when the TOE bit is 1 (timeout detect function enabled).
When long time is selected, the internal counter increments fVIIC as a 16-bit counter. When short time is selected, the internal counter increments fVIIC as a 14-bit counter. Therefore, the timeout detect time is as follows:
When the TOSEL bit is set to 0 (long time)

$$65536 \times \frac{1}{fVIIC}$$

When the TOSEL bit is set to 1 (short time)

$$16384 \times \frac{1}{fVIIC}$$

Table 22.8 lists Timeout Detect Time.

Table 22.8 Timeout Detect Time

fVIIC	Timeout Detect	
	TOSEL bit: 0 (Long time)	TOSEL bit: 1 (Short time)
4 MHz	16.4 ms	4.1 ms
2 MHz	32.8 ms	8.2 ms
1 MHz	65.6 ms	16.4 ms

Rewrite this bit when the TOE bit is 0.

ICK4-ICK2 (I2C-bus system clock select bit) (b5-b3)

Rewrite bits ICK4 to ICK2 when the ES0 bit in the S1D0 register is 0 (I2C interface disabled).
fVIIC is selected by setting all the bits ICK4 to ICK2, bits ICK1 to ICK0 in the S3D0 register, and the PCLK0 bit in the PCLKR register. Refer to Table 22.7 “I2C-bus System Clock Select Bits” and 22.3.1.2 “Bit Rate and Duty Cycle”.

MSLAD (Slave address control bit) (b6)

The MSLAD bit is enabled when the ALS bit in the S1D0 register is set to 0 (addressing format). The MSLAD bit is used to select the S0Di register (i = 0 to 2) used for slave address match detection.

SCPIN (Stop condition detect interrupt request bit) (b7)

The SCPIN bit is enabled when the SIM bit in the S3D0 register is set to 1 (enable I2C-bus interrupt by stop condition detection).
Condition to become 0:

- Writing 0 by a program.

Condition to become 1:

- Stop condition is detected
  (This bit cannot be set to 1 by a program.)

22.2.8 I2C0 Status Register 0 (S10)

I2C0 Status Register 0

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	Reset Value
								S10	02B8h	0001 000Xb

Bit Symbol	Bit Name	Function	RW
LRB	Last receive bit	When read, 0: Last bit = 0 1: Last bit = 1 When write, see Table 22.9 “Functions Enabled by Writing to the S10 Register”	RW
ADR0	General call detect flag	When read, 0: Not detected 1: Detected When write, see Table 22.9 “Functions Enabled by Writing to the S10 Register”	RW
AAS	Slave address compare flag	When read, 0: Address not matched 1: Address matched When write, see Table 22.9 “Functions Enabled by Writing to the S10 Register”	RW
AL	Arbitration lost detect flag	When read, 0: Not detected 1: Detected When write, see Table 22.9 “Functions Enabled by Writing to the S10 Register”	RW
PIN	I2C-bus interface interrupt request bit	When read, 0: Interrupt requested 1: Interrupt not requested When write, see Table 22.9 “Functions Enabled by Writing to the S10 Register”	RW
BB	Bus busy flag	When read, 0: Bus free 1: Bus busy When write, see Table 22.9 “Functions Enabled by Writing to the S10 Register”	RW
TRX	Communication mode select bit 0	0: Receive mode 1: Transmit mode	RW
MST	Communication mode select bit 1	0: Slave mode 1: Master mode	RW

Do not use the bit managing instruction (read-modify-write instruction) to access the S10 register. Use the MOV instruction to write to the S10 register.

Bit 5 to bit 0 in the S10 register (6 lower bits) monitor the state of the I2C interface. The bit values cannot be changed by a program. However, writing to the S10 register, including the 6 lower bits, generates a start/stop condition.

Bits MST and TRX are read and write bits. To change bits MST or TRX without generating a start/stop condition, set 1111b to the 4 lower bits in the S10 register.

Table 22.9 lists Functions Enabled by Writing to the S10 Register. Only set the values listed in Table 22.9. If the values listed in Table 22.9 are written to the S10 register, the 6 lower bits in the S10 register will not be changed.

Table 22.9 Functions Enabled by Writing to the S10 Register

Bit Setting of the S10 Register								Function
MST	TRX	BB	PIN	AL	AAS	ADR0	LRB	
1	1	1	0	0	0	0	0	Sets the I2C interface to start condition standby state in master transmit/receive mode
1	1	0	0	0	0	0	0	Sets the I2C interface to stop condition standby state in master transmit/receive mode
0	0	–	0	1	1	1	1	Slave receive mode
0	1	–	0	1	1	1	1	Slave transmit mode
1	0	–	0	1	1	1	1	Master receive mode
1	1	–	0	1	1	1	1	Master transmit mode

–: 0 or 1

Refer to 22.3.2 “Generating a Start Condition” and 22.3.3 “Generating a Stop Condition” for start/stop conditions.

LRB (Last receive bit) (b0)

When read, the LRB bit functions as described below. See Table 22.9 “Functions Enabled by Writing to the S10 Register” for the bit function in write access.
The LRB bit stores the value of the last bit of the received data. It is used to check if ACK is received. The bit becomes 0 after writing to the S00 register.

ADR0 (General call detect flag) (b1)

The ADR0 bit function in read access is described below. See Table 22.9 “Functions Enabled by Writing to the S10 Register” for the bit function in write access.
Conditions to become 0:

- Stop condition is detected.
- Start condition is detected.
- The ES0 bit in the S1D0 register is set to 0 (I2C interface disabled).
- The IHR bit in the S1D0 register is set to 1 (I2C interface reset).

Condition to become 1:

- The ALS bit in the S1D0 register is set to 0 (addressing format) and the received slave address is 0000000b (general call) in slave mode.

AAS (Slave address compare flag) (b2)

The AAS bit function in read access is described below. See Table 22.9 “Functions Enabled by Writing to the S10 Register” for the bit function in write access.

Conditions to become 0:

- The S00 register is written.
- The ES0 bit in the S1D0 register is set to 0 (I2C interface disabled).
- The IHR bit in the S1D0 register is set to 1 (I2C interface reset).

Conditions to become 1:

- In slave receive mode, the MSLAD bit in the S4D0 register is 1 (registers S0D0 to S0D2), the ALS bit in the S1D0 register is 0 (addressing format), and the received slave address is matched with bits SAD6 to SAD0 in any registers from S0D0 to S0D2.
- In slave receive mode, the MSLAD bit is 0, the ALS bit in the S1D0 register is 0 (addressing format), and the received slave address is matched with bits SAD6 to SAD0 in the S0D0 register.
- In slave receive mode, the ALS bit in the S1D0 register is 0 (addressing format) and the received slave address is 0000000b (general call).

AL (Arbitration lost detect flag) (b3)

The AL bit function in read access is described below. See Table 22.9 “Functions Enabled by Writing to the S10 Register” for the bit function in write access.

Conditions to become 0:

- The S00 register is written.
- The ES0 bit in the S1D0 register is set to 0 (I2C interface disabled).
- The IHR bit in the S1D0 register is set to 1 (I2C interface reset).

Conditions to become 1:

- In master transmit mode or master receive mode, the SDAMM pin level changes to low by an external device, not by the ACK clock, when slave address is transmitted.
- The SDAMM pin level changes to low by an external device for other than the ACK clock when data is transmitted in master transmit mode.
- In master transmit mode or master receive mode, the SDAMM pin level changes to low by an external device when start condition is transmitted.
- In master transmit mode or master receive mode, the SDAMM pin level changes to low by an external device when stop condition is transmitted.
- The function to prevent start condition overlaps is activated.

PIN (I2C-bus interface interrupt request bit) (b4)

The PIN bit function in read access is described below. See Table 22.9 “Functions Enabled by Writing to the S10 Register” for the bit function in write access.

Conditions to become 0:

- Slave address transmission is completed in master mode (including a case of detecting arbitration lost).
- 1-byte data transmission is completed (including a case of detecting arbitration lost).
- 1-byte data reception is completed (the falling edge of eighth clock is detected when the ACKCLK bit in the S20 register is 0, or the falling edge of ACK clock when the ACKCLK bit is 1).
- The WIT bit in the S3D0 register is 1 (I2C-bus interrupt enabled at 8th clock) and 1-byte data reception is completed (before ACK clock).
- In slave receive mode, the MSLAD bit in the S4D0 register is 1, the ALS bit in the S1D0 register is 0 (addressing format), and any of the slave address stored in bits SAD6 to SAD0 in the S0Di register (i = 0 to 2) is matched with the received slave address (slave address match).
- In slave receive mode, the MSLAD bit is 0, the ALS bit is 0 (addressing format), and the slave address stored in bits SAD6 to SAD0 in the S0D0 register is matched with the received slave address (slave address match).
- In slave receive mode, the ALS bit in the S1D0 register is 0 (addressing format) and the received slaved address is 0000000b (general call).
- In slave receive mode, the ALS bit in the S1D0 register is 1 (free data format) and the slave address reception is completed.

Conditions to become 1:

- The S00 register is written.
- The S20 register is written (when the WIT bit is 1 and the internal WAIT flag is 1).
- The ES0 bit in the S1D0 register is set to 0 (I2C interface disabled).
- The IHR bit in the S1D0 register is set to 1 (I2C interface reset).

The IR bit in the IICIC register becomes 1 (interrupt requested) as soon as the PIN bit becomes 0 (I2C-bus interrupt requested). When the PIN bit is 0, the SCLMM pin output level is low.

However, when all of the following conditions are met, the SCLMM pin does not output a low level signal:

- In master mode, arbitration lost is detected by a slave address or data
- The ALS bit in the S1D0 register is 0 (addressing format)
- The slave address is not 0000000b (general call) and does not match any of the bits from SAD6 to SAD0 in registers S0D0 to S0D2.

BB (Bus busy flag) (b5)

The BB bit function in read access is described below. See Table 22.9 “Functions Enabled by Writing to the S10 Register” for the bit function in write access.

The BB bit indicates the state of the bus system, whether the bus is free or not. The BB bit changes depending on the SCLMM and SDAMM input signals, regardless of master mode or slave mode.

Conditions to become 0:

- Stop condition is detected.
- The ES0 bit in the S1D0 register is set to 0 (I2C interface disabled).
- The IHR bit in the S1D0 register is set to 1 (I2C interface reset).

Condition to become 1:

- Start condition is detected.

TRX (Communication mode select bit 0) (b6)

Set the TRX bit to select transmit mode or receive mode.
Conditions to become 0:

- The TRX bit is set to 0 by a program.
- Arbitration lost is detected.
- Stop condition is detected.
- Start condition overlap protect function is enabled.
- Start condition is detected when the MST bit in the S10 register is 0 (slave mode).
- No ACK is detected from a receiver when the MST bit in the S10 register is 0 (slave mode).
- The ES0 bit in the S1D0 register is set to 0 (I2C interface disabled).
- The IHR bit in the S1D0 register is set to 1 (I2C interface reset).

Conditions to become 1:

- The TRX bit is set to 1 by a program.
- In slave mode, the ALS bit in the S1D0 register is 0 (addressing format), the AAS bit in the S10 register becomes 1 (address matched) after receiving the slave address, and the received R/W bit is 1.

MST (Communication mode select bit 1) (b7)

Set the MST bit to select master mode or slave mode.
Conditions to become 0:

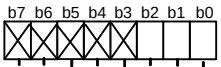
- The MST bit is set to 0 by a program.
- The 1-byte data that lost arbitration is completed transmitting/receiving when arbitration lost is detected.
- Stop condition is detected.
- Start condition overlap protect function is enabled.
- The ES0 bit in the S1D0 register is 0 (I2C interface disabled).
- The IHR bit in the S1D0 register is 1 (I2C interface reset).

Conditions to become 1:

- The MST bit is set to 1 by a program.

22.2.9 I2C0 Status Register 1 (S11)

I2C0 Status Register 1



Symbol	Address	Reset Value
S11	02B9h	XXXX X000b

Bit Symbol	Bit Name	Function	RW
AAS0	Slave address 0 compare flag	0: No address matched 1: Address matched	RO
AAS1	Slave address 1 compare flag	0: No address matched 1: Address matched	RO
AAS2	Slave address 2 compare flag	0: No address matched 1: Address matched	RO
— (b7-b3)	No register bits. If necessary, set to 0. The read value is undefined.		—

AAS0 (Slave address 0 compare flag) (b0)
AAS1 (Slave address 1 compare flag) (b1)
AAS2 (Slave address 2 compare flag) (b2)

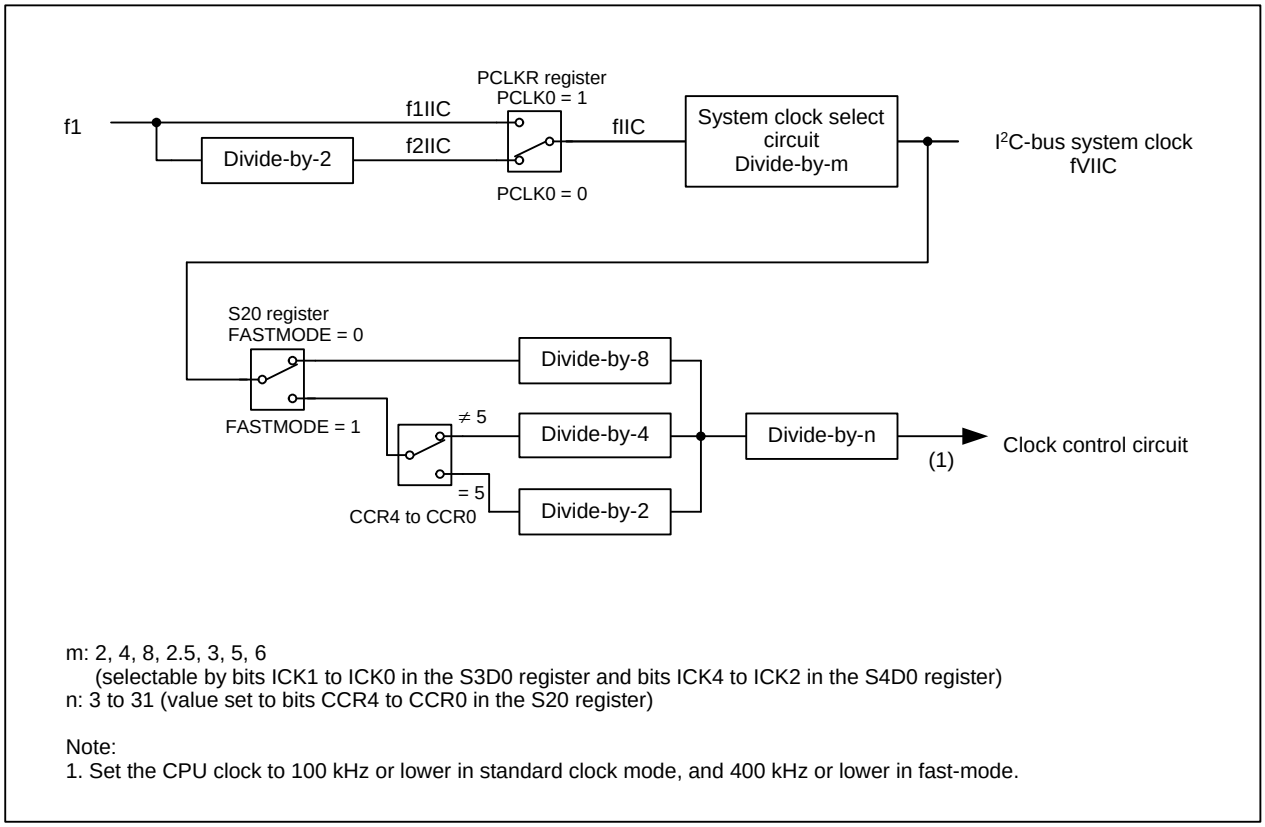
When the ALS bit in the S1D0 register is 0 (addressing format), any slave address stored in bits SAD6 to SAD0 in the S0Di register (i = 0 to 2) is compared with the received slave address. The compare result is shown in the AASi bit. The AASi bit becomes 1 when there is an address match or when a general call address is received.
The AAS0 bit is enabled when the MSLAD bit in the S4D0 register is 0 (S0D0 register only). Bits AAS2 to AAS0 are enabled when the MSLAD bit is 1 (registers S0D0 to S0D2).
Conditions to become 0:

- The ES0 bit in the S1D0 register is set to 0 (I2C interface disabled).
- The IHR bit in the S1D0 register is set to 1 (I2C interface reset).
- The S00 register is written.

22.3 Operations

22.3.1 Clock

Figure 22.5 shows the I2C-bus Interface Clock.



m: 2, 4, 8, 2.5, 3, 5, 6
(selectable by bits ICK1 to ICK0 in the S3D0 register and bits ICK4 to ICK2 in the S4D0 register)
n: 3 to 31 (value set to bits CCR4 to CCR0 in the S20 register)

Note:
1. Set the CPU clock to 100 kHz or lower in standard clock mode, and 400 kHz or lower in fast-mode.

Figure 22.5 I2C-bus Interface Clock

22.3.1.1 fVIIC

fVIIC is determined by setting a combination of the following:

- The frequency of peripheral clock f1
- The PCLK0 bit in the PCLKR register
- Bits ICK1 to ICK0 in the S3D0 register
- Bits ICK4 to ICK2 in the S4D0 register

fVIIC stops when the ES0 bit in the S1D0 register is 0 (I2C interface disabled).

See Table 22.7 “I2C-bus System Clock Select Bits” for details.

22.3.1.2 Bit Rate and Duty Cycle

Bit rate is determined by a combination of fVIIC, the FASTMODE bit in the S20 register, and bits CCR4 to CCR0 in the S20 register.

Table 22.10 lists the Bit Rate of Internal SCL Output and Duty Cycle. When the change in the internal SCL output high level is a negative value, although the low period increases the amount that the high periods decreases, the bit rate does not increase. The values described is the following table are the values of the internal SCL output before being effected by the SCL output of an external device.

Table 22.10 Bit Rate of Internal SCL Output and Duty Cycle

Item	Standard Clock Mode (FASTMODE = 0)	Fast-mode (FASTMODE = 1) (CCR value = other than 5)	Fast-mode (FASTMODE = 1) (CCR value = 5)
Bit rate (bps)	$\frac{fVIIC}{8 \times CCR\ value}$	$\frac{fVIIC}{4 \times CCR\ value}$	$\frac{fVIIC}{2 \times CCRvalue} = \frac{fVIIC}{10}$
Duty cycle	50% Fluctuation of high level: -4 to +2 fVIIC cycles	50% Fluctuation of high level: -2 to +2 fVIIC cycles	35 to 45%

CCR value: Value set to bits CCR4 to CCR0

When the CCR value (setting value of bits CCR4 to CCR0) is 5 (00101b) in fast-mode, the bit rate is assumed to reach 400 kbps, the maximum bit rate in fast-mode.

The bit rate and duty cycle are as follows.

- Bit rate:

$$\frac{fVIIC}{2 \times CCR\ value} = \frac{fVIIC}{10}$$

When fVIIC is 4 MHz, the bit rate is 400 kbps.

- Duty cycle is 35 to 45%

Even if the bit rate is 400 kbps, the 1.3 μs minimum low period of the SCLMM clock (I2C-bus standard) is allocated. Table 22.11 lists the Bit Setting for Bits CCR4 to CCR0 and Bit Rate (fVIIC = 4 MHz).

Table 22.11 Bit Setting for Bits CCR4 to CCR0 and Bit Rate (fVIIC = 4 MHz)

Bits CCR4 to CCR0 in the S20 Register					Bit Rate (kbps)	
CCR4	CCR3	CCR2	CCR1	CCR0	Standard Clock Mode	Fast-mode
0	0	0	0	0	Do not set (1)	Do not set (1)
0	0	0	0	1	Do not set (1)	Do not set (1)
0	0	0	1	0	Do not set (1)	Do not set (1)
0	0	0	1	1	Do not set (2)	333
0	0	1	0	0	Do not set (2)	250
0	0	1	0	1	100	400
0	0	1	1	0	83.3	166
:	:	:	:	:	:	:
1	1	1	0	1	17.2	34.5
1	1	1	1	0	16.6	33.3
1	1	1	1	1	16.1	32.3

Notes:

1. Do not set bits CCR4 to CCR0 to 0 to 2 regardless of the fVIIC frequency.
2. Do not exceed the maximum bit rates of 100 kbps in standard clock mode and 400 kbps in fast-mode.

22.3.1.3 Receiving a Slave Address in Wait Mode and Stop Mode

When the CM02 bit in the CM0 register is set to 0 (peripheral clock f1 does not stop in wait mode) and transition is made to wait mode, the I2C interface can receive the slave address even in wait mode.

When the CM02 bit in the CM0 register is set to 1 (peripheral clock f1 stops in wait mode) and transition is made to wait mode, the I2C interface stops operating because fVIIC supply is stopped in stop mode and low-power consumption mode.

The SCL/SDA interrupt can be used in either wait mode or stop mode.

22.3.2 Generating a Start Condition

Follow the procedure below when the ES0 bit in the S1D0 register is 1 (I2C interface enabled) and the BB bit in the S10 register is set to 0 (bus free). Figure 22.6 shows the Procedure to Generate a Start Condition.

(1) Write E0h to the S10 register.
The I2C interface enters the start condition standby state and the SDAMM pin is released.

(2) Write a slave address to the S00 register.
A start condition is generated. Then, the bit counter becomes 000b, the SCL clock signal is output for 1 byte, and the slave address is transmitted.

After a stop condition is generated and the BB bit becomes 0 (bus free), a write to the S10 register is disabled for 1.5 fVIIC cycles. Therefore, even if the S00 register is subsequently written to, a start condition is not generated. When generating a start condition shortly after changing the BB bit from 1 to 0, confirm that both bits TRX and MST are 1 after executing step (1), then execute step (2).

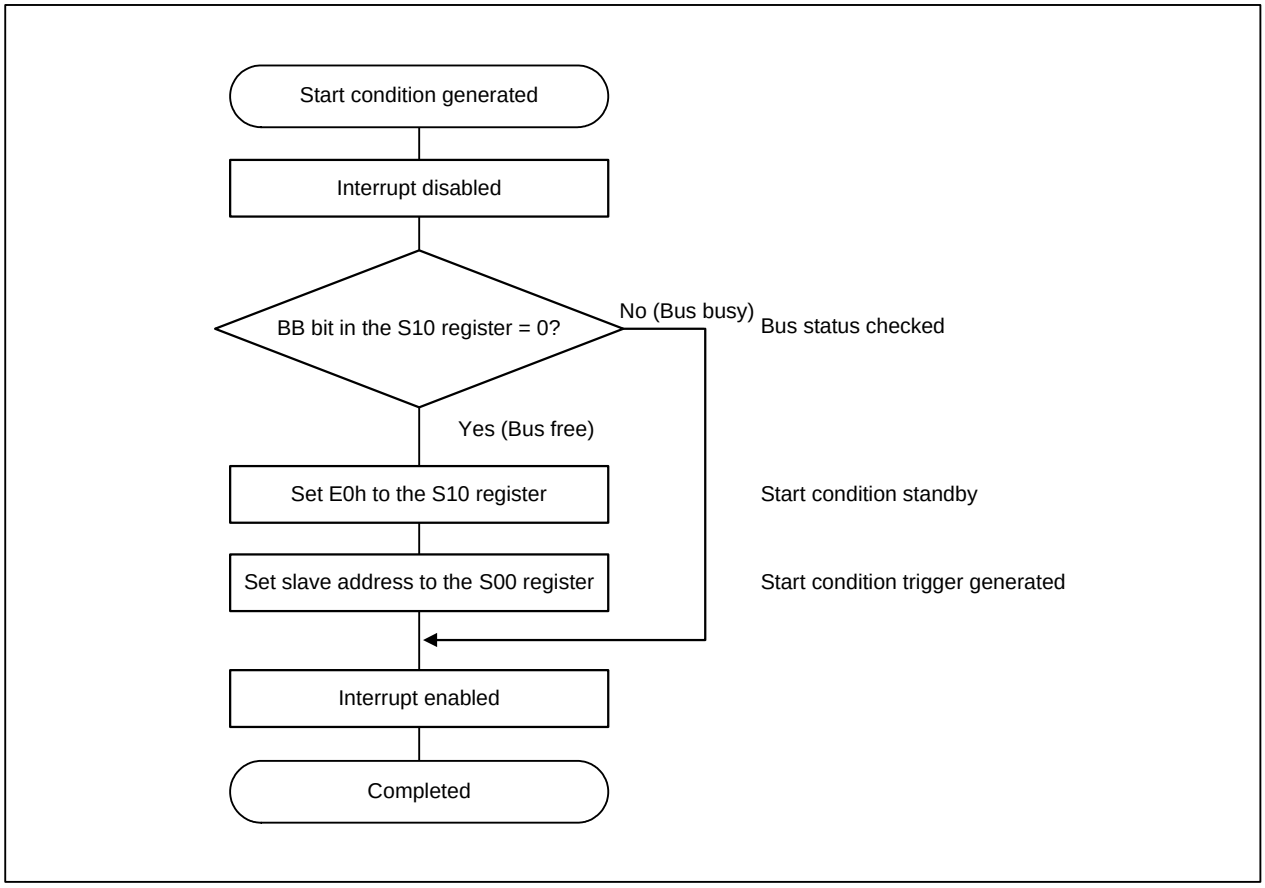


Figure 22.6 Procedure to Generate a Start Condition

The start condition generation timing depends on the modes - standard clock mode or fast-mode. Figure 22.7 shows the Start Condition Generation Timing.
Table 22.12 lists the Setup/Hold Time for Generating a Start/Stop Condition.

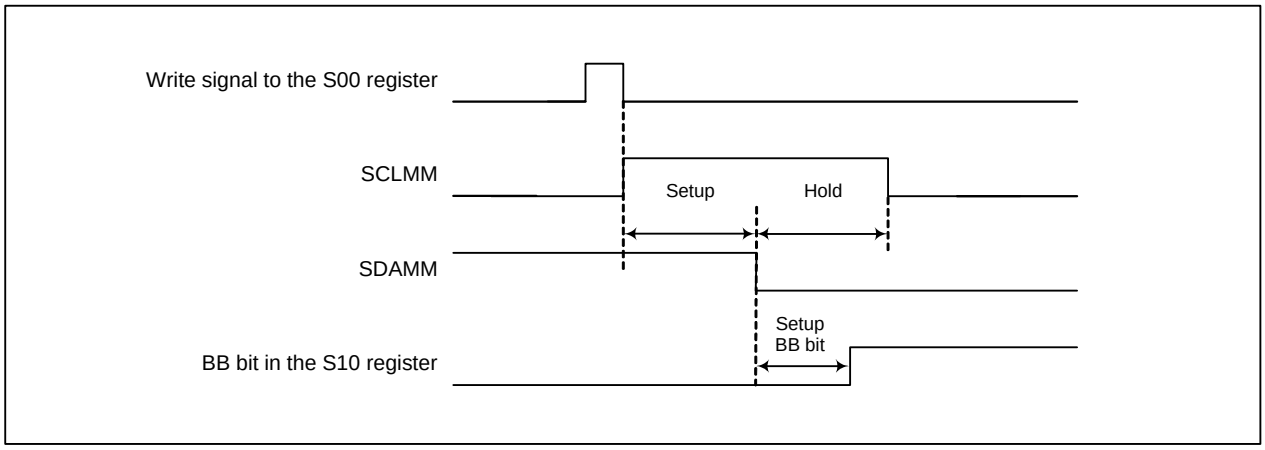


Figure 22.7 Start Condition Generation Timing

Table 22.12 Setup/Hold Time for Generating a Start/Stop Condition

Item	STSPSEL Bit	Standard Clock Mode		Fast-mode	
		fVIIC cycles	fVIIC = 4 MHz	fVIIC cycles	fVIIC = 4 MHz
Setup time	0 (short mode)	20	5.0 µs	10	2.5 µs
	1 (long mode)	52	13.0 µs	26	6.5 µs
Hold time	0 (short mode)	20	5.0 µs	10	2.5 µs
	1 (long mode)	52	13.0 µs	26	6.5 µs
BB bit set/reset time	-	$\frac{\text{SSC value} - 1}{2} + 2$	3.375 µs (1)	3.5	0.875 µs

-: 0 or 1
STSPSEL: Bit in the S2D0 register
SSC value: Value of bits SSC4 to SSC0 in the S2D0 register
Note:
1. Example value when bits SSC4 to SSC0 are 11000b.

22.3.3 Generating a Stop Condition

Use the following procedure when the ES0 bit in the S1D0 register is 1 (I2C interface enabled).

(1) Write C0h to the S10 register.
The I2C interface enters the stop condition standby state and the SDAMM pin is driven low.

(2) Write dummy data to the S00 register.
A stop condition is generated.

The stop condition generation timing depends on the modes - standard clock mode or fast-mode. Figure 22.8 shows the Stop Condition Generation Timing. See Table 22.12 “Setup/Hold Time for Generating a Start/Stop Condition” for setup/hold time.

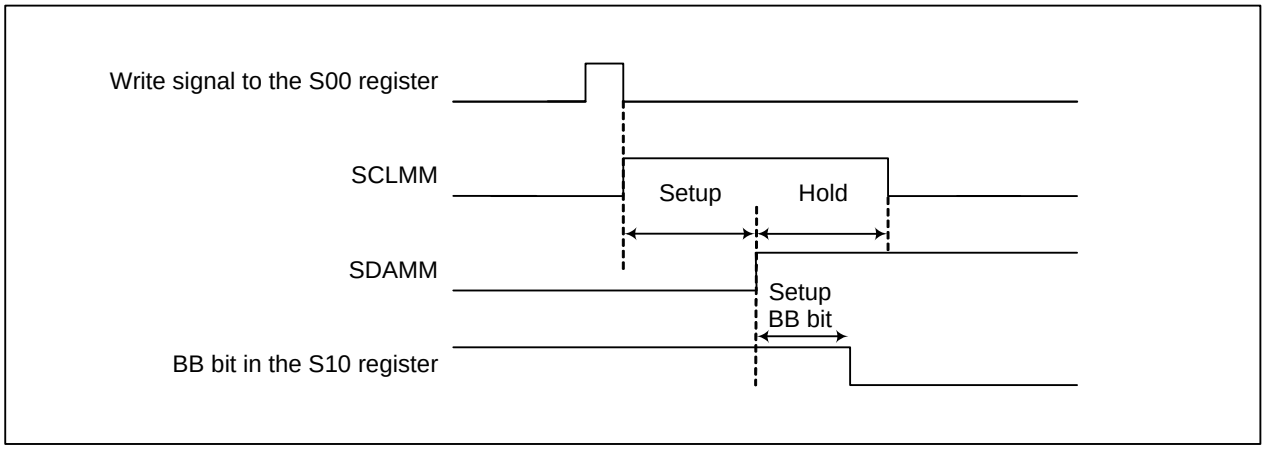


Figure 22.8 Stop Condition Generation Timing

Do not write to the S10 register or S00 register until the BB bit in the S10 register becomes 0 (bus free) after the instructions to generate a stop condition (refer to above (2)) are executed.

If the SCLMM pin input signal becomes low until the BB bit in the S10 register becomes 0 (bus free) from the instruction to generate a stop condition is executed and the SCLMM pin becomes high-level, the internal SCL output becomes low. In this case, perform one of the steps below to stop the low signal output from the SCLMM pin (release the SCLMM pin).

- Generate a stop condition (perform steps (1) and (2) above).
- Set the ES0 bit in the S1D0 register to 0 (I2C interface disabled).
- Write 1 to the IHR bit (I2C interface reset).

22.3.4 Generating a Restart Condition

Use the following procedure to generate a restart condition when 1-byte data is transmitted/received.

(1) Write E0h to the S10 register. (Start condition standby state. The SDAMM pin released.)
(2) Wait until the SDAMM pin level becomes high.
(3) Write a slave address to the S00 register (a start condition trigger is generated)

Figure 22.9 shows the Restart Condition Generation Timing.

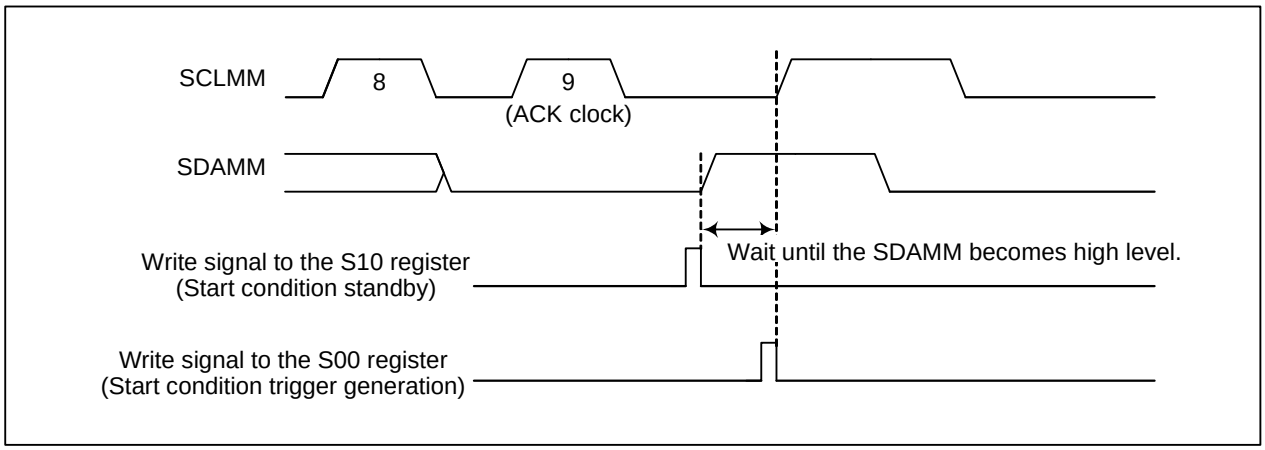


Figure 22.9 Restart Condition Generation Timing

22.3.5 Start Condition Overlap Protect

The I2C interface generates a start condition by setting registers S10 and S00 by a program. The bus system must be free before setting these registers. Check whether the bus is free with the BB bit in the S10 register by a program before setting the registers.

However, even after confirming that the bus is free, other master devices may generate a start condition before setting registers S10 and S00. In this case, when the I2C interface detects a start condition, the BB bit becomes 1 (bus busy) and the start condition overlap protect function is activated. The start condition overlap protect function operates as follows:

- The multi-master I2C-bus interface does not enter start condition standby state even if the S10 register is set to E0h.
- If the I2C interface is in a start condition standby state, exit the state.
- A start condition trigger is not generated even if a data is written to the S00 register by program.
- Bits MST and TRX in the S10 register become 0 (slave receive mode).
- The AL bit in the S10 register becomes 1 (arbitration lost detected).

Figure 22.10 shows the Start Condition Overlap Protect Operation.

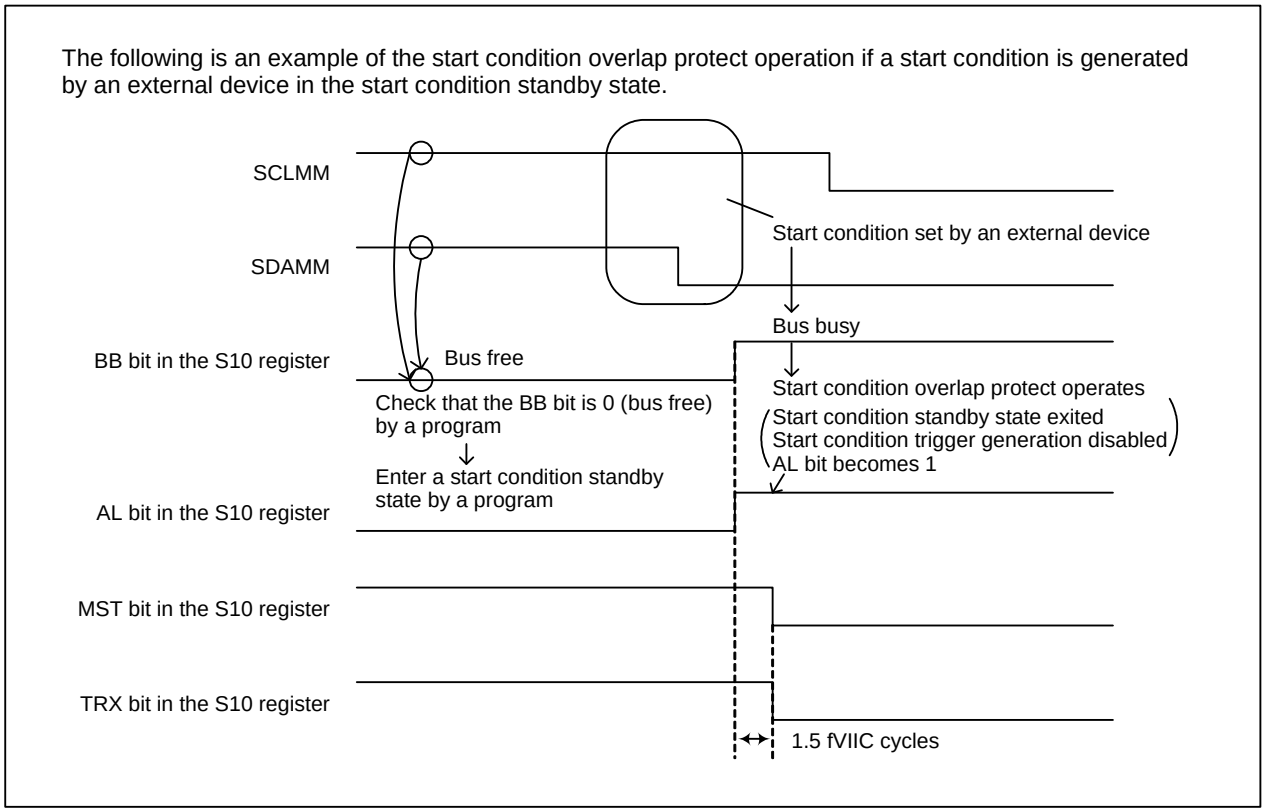


Figure 22.10 Start Condition Overlap Protect Operation

The start condition overlap protect is enabled from the falling edge of SDAMM (start condition) to the completion of the slave address receive. If data is written to registers S10 and S00 during that period, the above operation is performed. Figure 22.11 shows the Start Condition Overlap Protect Function Enable Period.

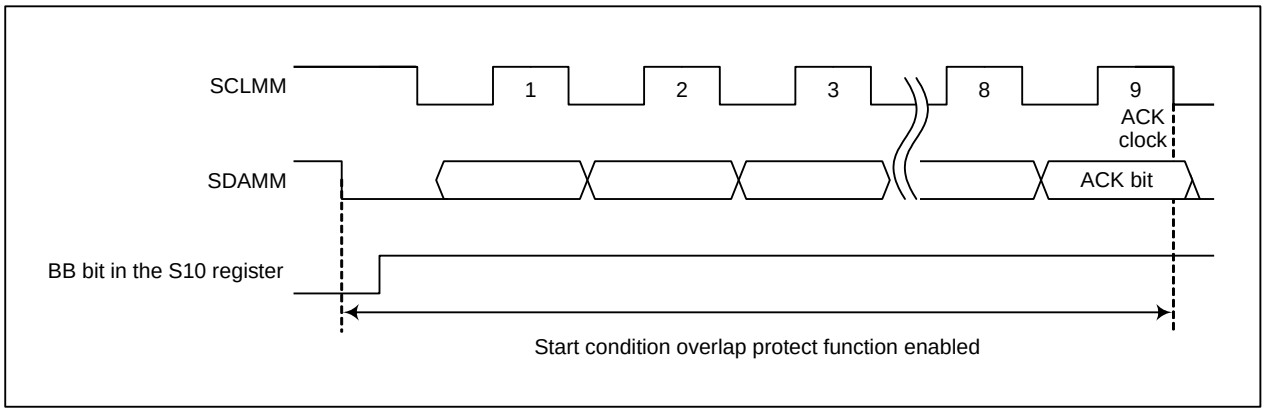


Figure 22.11 Start Condition Overlap Protect Function Enable Period

22.3.6 Arbitration Lost

When all of the conditions below are met, the SDAMM pin signal level becomes low by an external device and the I2C interface determines that it has lost arbitration.

(a) Transmit/receive (one of the following)
- Slave address transmit (not an ACK clock) in master transmit mode or master receive mode
- Data transmit (not an ACK clock) in master transmit mode
- Start condition generated in master transmit mode or master receive mode
- Stop condition generated in master transmit mode or master receive mode

(b) Internal SDA output: High

(c) SDAMM pin level: Low (sampling at the rising edge of the clock of SCLMM pin.)

Figure 22.12 shows Operation Example When Arbitration Lost is Detected.

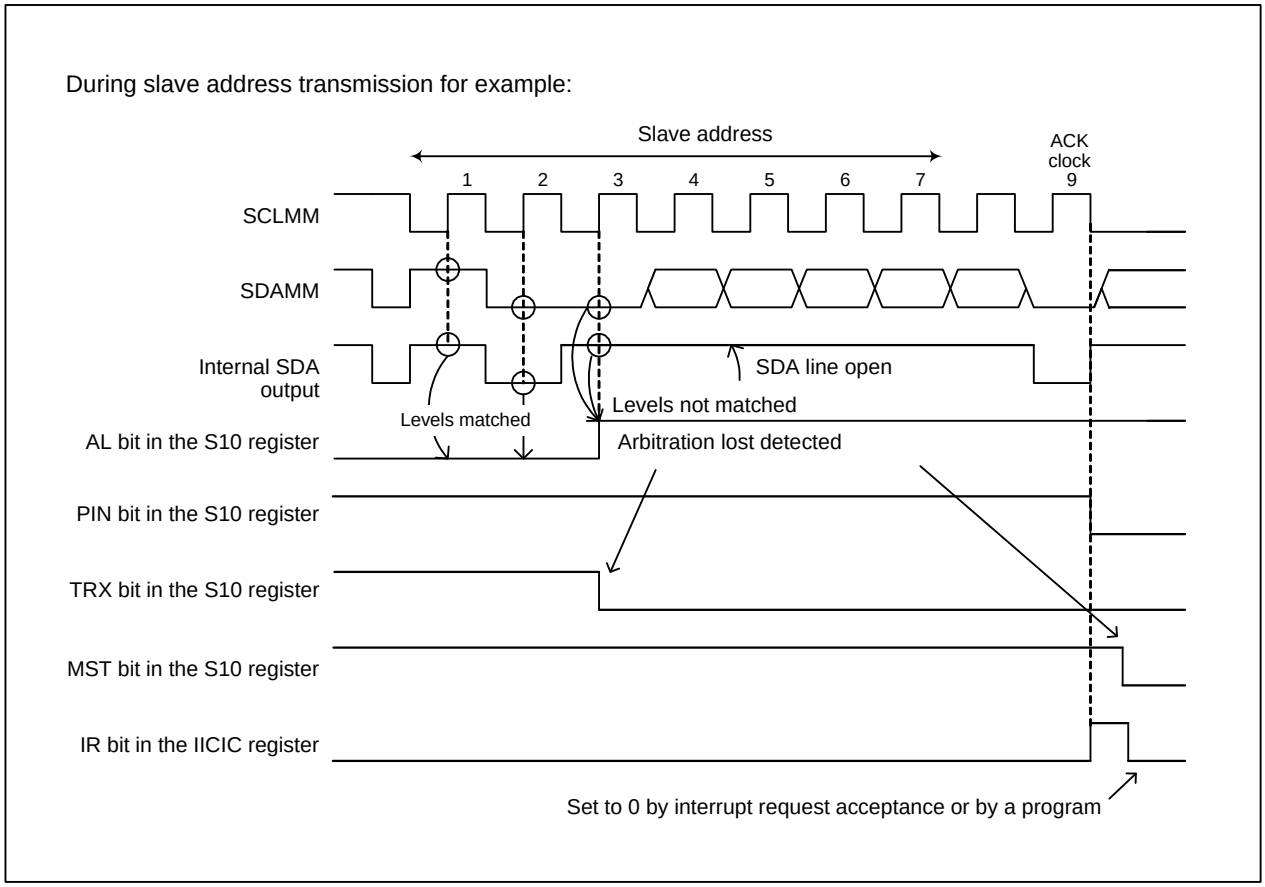


Figure 22.12 Operation Example When Arbitration Lost is Detected

When arbitration lost is detected:

- The AL bit in the S10 register becomes 1 (arbitration lost detected)
- Internal SDA output becomes high. (SDAMM released)
- The I2C interface enters the slave receive mode
  The TRX bit in the S10 register is 0 (receive mode).
  The MST bit in the S10 register is 0 (slave mode).

In order to set the AL bit to 0 again after arbitration lost is detected, set a value to the S00 register.

When arbitration lost is detected during slave address transmission, the I2C interface automatically enters slave receive mode and receives the slave address sent from another master. When the ALS bit in the S1D0 register is 0 (addressing format), the slave address comparison result is determined by reading bits ADR0 and AAS in the S10 register.

When arbitration lost is detected during data transmission, the I2C interface automatically enters slave receive mode.

Also, when arbitration lost is detected, the TRX bit becomes 0 (receive mode) even when the bit after the slave address is 1 (read). Therefore, read the S00 register after arbitration lost is detected. When bit 0 in the S00 register is 1, write 4Fh (slave transmit mode) to the S10 register and execute slave transmission.

22.3.7 Detecting Start/Stop Conditions

Figure 22.13 shows Start Condition Detection, Figure 22.14 shows Stop Condition Detection, and Table 22.13 lists Conditions to Detect Start/Stop Condition.

A start/stop condition can be detected only when the start/stop condition detect parameters are selected by setting bits SSC4 to SSC0 in the S2D0 register, and the signals input to pins SCLMM and SDAMM meet all three conditions (SCLMM release time, setup time, and hold time) listed in Table 22.13.

The BB bit in the S10 register becomes 1 when a start condition is detected, and becomes 0 when a stop condition is detected. The set timing and reset timing of the BB bit depends on whether the mode is standard mode or fast-mode. Refer to the BB bit set/reset times in Table 22.14.

Table 22.14 lists the Recommended Values of Bits SSC4 to SSC0 in Standard Clock Mode.

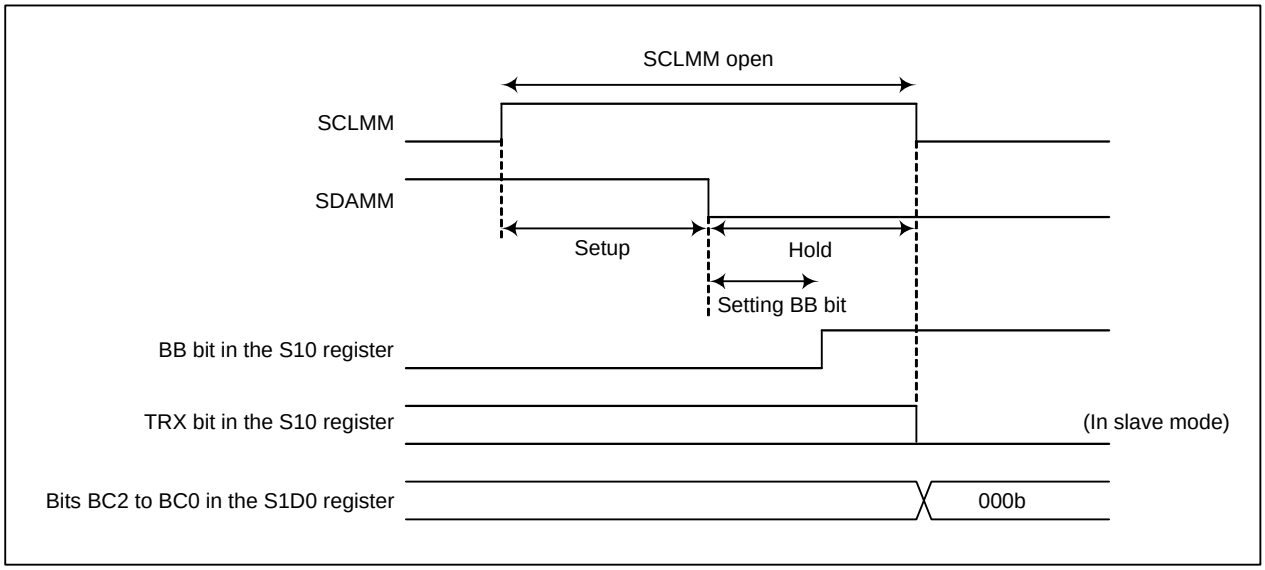


Figure 22.13 Start Condition Detection

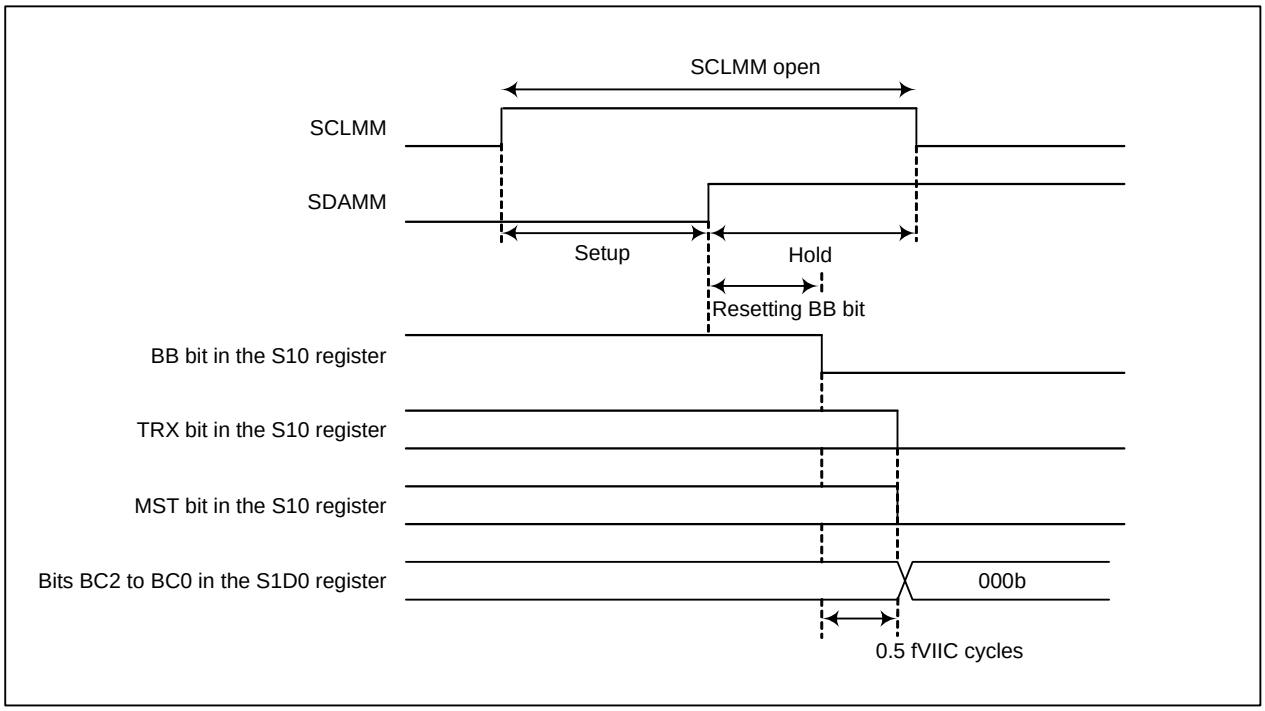


Figure 22.14 Stop Condition Detection

Table 22.13 Conditions to Detect Start/Stop Condition

	Standard Clock Mode	Fast-Mode
SCLMM open time	SSC value + 1 cycle	4 cycles
Setup time	$\frac{\text{SSC value}}{2}$ + 1 cycle	2 cycles
Hold time	$\frac{\text{SSC value}}{2}$ cycles	2 cycles
BB bit setting/resetting time	$\frac{\text{SSC value} - 1}{2}$ + 2 cycles	3.5 cycles

Unit: Number of fVIIC cycles
SSC value: Value of bits SSC4 to SSC0 in the S2D0 register

Table 22.14 Recommended Values of Bits SSC4 to SSC0 in Standard Clock Mode

fVIIC	SSC Value (recommended)	Start/Stop Condition Detect Parameter			BB Bit Setting/Resetting Time
		SCLMM open time	Setup time	Hold time	
5 MHz	11110b	6.2 µs (31)	3.2 µs (16)	3.0 µs (15)	3.3 µs (16.5)
4 MHz	11010b	6.75 µs (27)	3.5 µs (14)	3.25 µs (13)	3.625 µs (14.5)
	11000b	6.25 µs (25)	3.25 µs (13)	3.0 µs (12)	3.375 µs (13.5)
2 MHz	01100b	6.5 µs (13)	3.5 µs (7)	3.0 µs (6)	3.75 µs (7.5)
	01010b	5.5 µs (11)	3.0 µs (6)	2.5 µs (5)	3.25 µs (6.5)
1 MHz	00100b	5.0 µs (5)	3.0 µs (3)	2.0 µs (2)	3.5 µs (3.5)

SSC value: Value of bits SSC4 to SSC0 in the S2D0 register
( ): Number of fVIIC cycles

22.3.8 Operation after Transmitting/Receiving a Slave Address or Data

After a slave address or 1-byte data has been transmitted/received, the PIN bit in the S10 register becomes 0 (interrupt requested) at the falling edge of the ACK clock. The IR bit in the IICIC register becomes 1 (interrupt requested) at the same time. The value in the S10 register or other register changes depending on the state of the transmit/receive data, and the level of pins SCLMM and SDAMM. Figure 22.15 shows Operation When Transmitted/Received a Slave Address or Data.

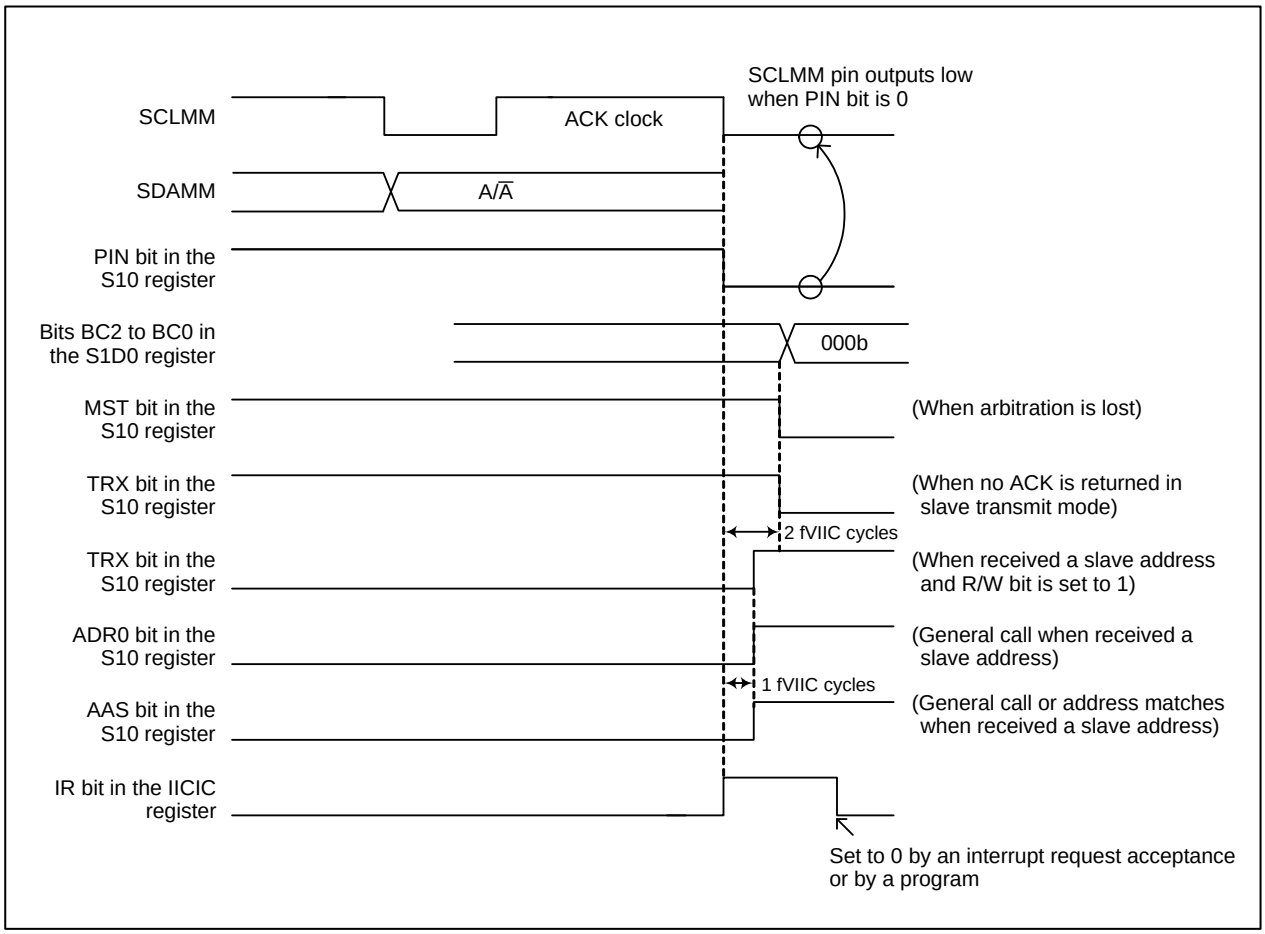


Figure 22.15 Operation When Transmitted/Received a Slave Address or Data

22.3.9 Timeout Detection

When the SCL clock is stopped during transmission/reception, each device stops operating, keeping the communication state. To avoid this, the I2C interface incorporates a function to detect timeouts and generate an I2C-bus interrupt request when the SCLMM pin is driven high for more than the selected timeout detection period during transmission/reception. Figure 22.16 shows the Timeout Detection Timing. Refer to “TOSEL (Timeout Detection Period Select Bit) (b2)” in 22.2.7 “I2C0 Control Register 2 (S4D0)” for the timeout detection period.

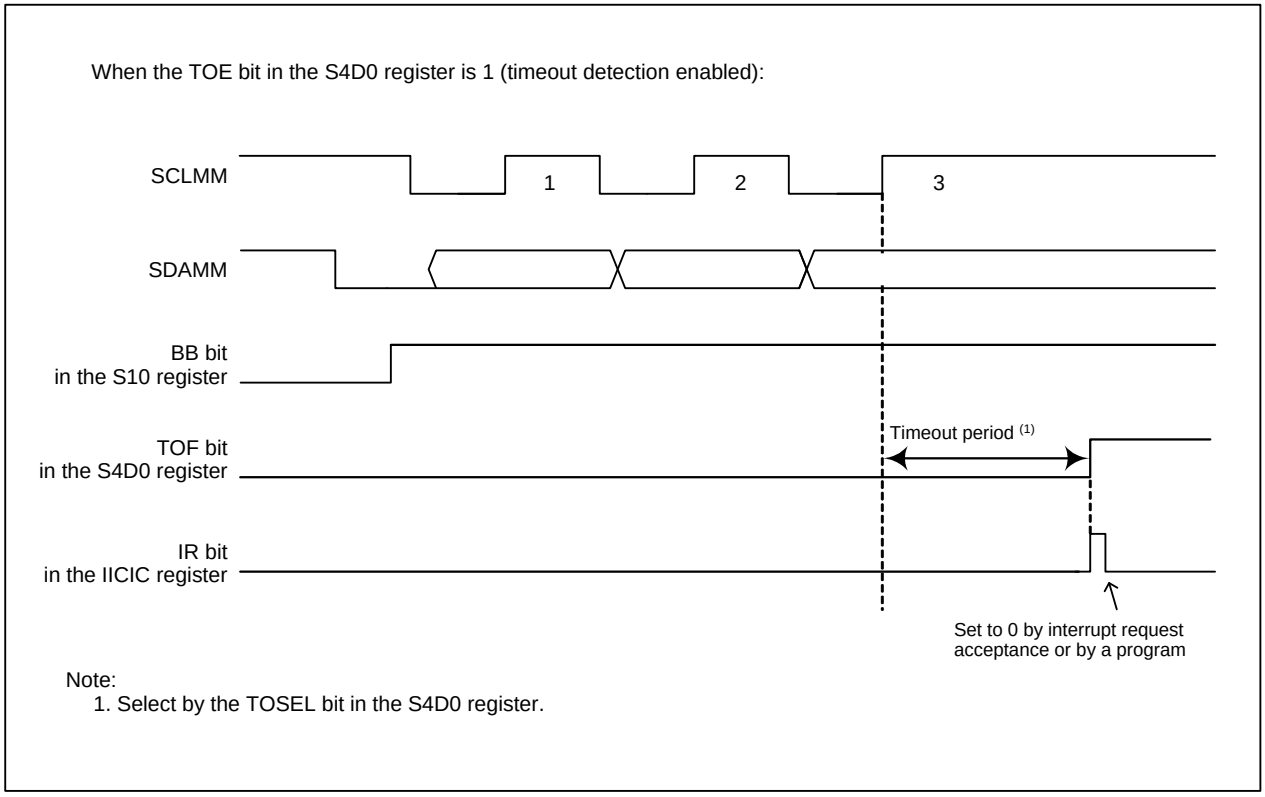


Figure 22.16 Timeout Detection Timing

A timeout is detected when the all of the following conditions are met:

- The TOE bit in the S4D0 register is 1 (timeout detection enabled)
- The BB bit in the S10 register is 1 (bus busy)
- The SCLMM pin is driven high for more than the timeout detect period

When a timeout is detected:

- The TOF bit in the S4D0 register becomes 1 (timeout detected)
- The IR bit in the IICIC register becomes 1 (I2C-bus interrupt requested)

When the timeout is detected, perform one of the following:

- Set the ES0 bit in the S1D0 register to 0 (disabled).
- Set the IHR bit in the S1D0 register to 1 (I2C interface reset).

22.3.10 Data Transmit/Receive Examples

The data transmit/receive examples are described in this section. The conditions for the examples are as follows:

- Slave address: 7 bits
- Data: 8 bits
- ACK clock
- Standard clock mode, bit rate: 100 kbps (fIIC: 20 MHz; fVIIC: 4 MHz)
  20 MHz (fIIC) divided-by-5 = 4 MHz (fVIIC),
  4 MHz (fVIIC) divided-by-8 and further divided-by-5 = 100 kbps (bit rate)
- In receive mode, an ACK is returned for received data other than the last data. NACK is returned after the last data is received.
- When receiving data, I2C-bus interrupt at the eighth clock (just before ACK clock): disabled
- Stop condition interrupt: enabled
- Timeout detect interrupt: disabled
- Set an own slave address to the S0D0 register (registers S0D1 or S0D2 should not be used)

When enabling an I2C-bus interrupt at the eighth clock (just before ACK clock) during data reception, a receiver can determine whether to generate ACK or NACK after checking the received data each byte.

22.3.10.1 Initial Settings

Follow the initial setting procedures below for 22.3.10.2 to 22.3.10.5.

(1) Write an own slave address to bits SAD6 to SAD0 in the S0D0 register.
(2) Write 85h to the S20 register. (CCR value: 5, standard clock mode, ACK clock presents)
(3) Write 18h to the S4D0 register. (fVIIC: fIIC divided-by-5, timeout interrupt disabled)
(4) Write 01h to the S3D0 register. (stop condition detect interrupt enabled and I2C-bus interrupt at eighth clock is disabled when receiving data)
(5) Write 0Fh to the S10 register. (slave receive mode)
(6) Write 98h to the S2D0 register (SSC value: 18h; start/stop condition generation timing: long mode)
(7) Write 08h to the S1D0 register (bit counter: 8, I2C interface enabled, addressing format, input level: I2C-bus input)

If the MCU uses a single-master system and it is a master, start the initial setting procedures from step (2).

22.3.10.2 Master Transmission

Master transmission is described in this section. The initial settings described in 22.3.10.1 “Initial Settings” are assumed to be completed. Figure 21.17 shows master transmission operation.
The following programs (A) to (C) are executed at (A) to (C) in Figure 22.17, respectively.

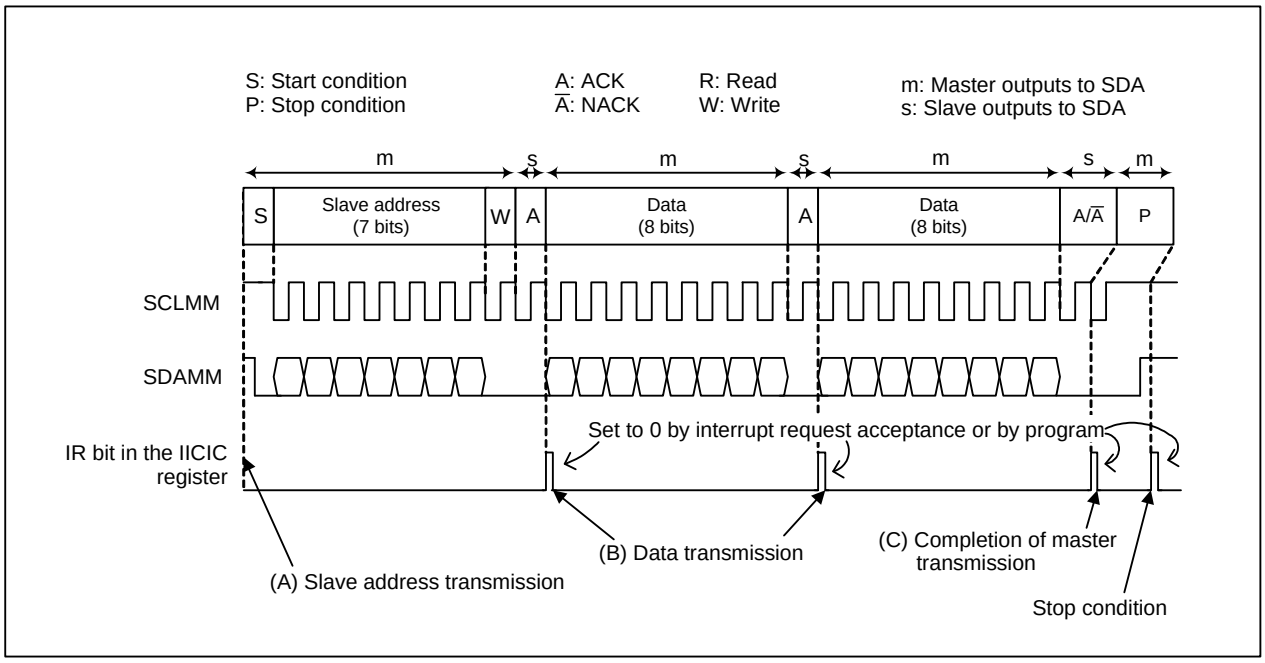


Figure 22.17 Example of Master Transmission

(A) Slave address transmission
(1) The BB bit in the S10 register must be 0 (bus free).
(2) Write E0h to the S10 register. (start condition standby)
(3) Write a slave address to the upper 7 bits and set the least significant bit (LSB) to 0. (start condition generated, then slave address transmitted)

(B) Data transmission
(in I2C-bus interrupt routine)
(1) Write transmit data to the S00 register. (data transmission)

(C) Completion of Master transmission
(in I2C-bus interrupt routine)
(1) Write C0h to the S10 register. (Stop condition standby state)
(2) Write dummy data to the S00 register. (stop condition generated)

When transmission is completed or ACK is not returned from a slave device (NACK returned), master transmission should be completed as shown in the example above.

22.3.10.3 Master Reception

Master reception is described in this section. The initial settings described in 22.3.10.1 “Initial Settings” are assumed to be completed. Figure 22.18 shows the operation example of master reception. The following programs (A) to (D) are executed at (A) to (D) in Figure 22.18, respectively.

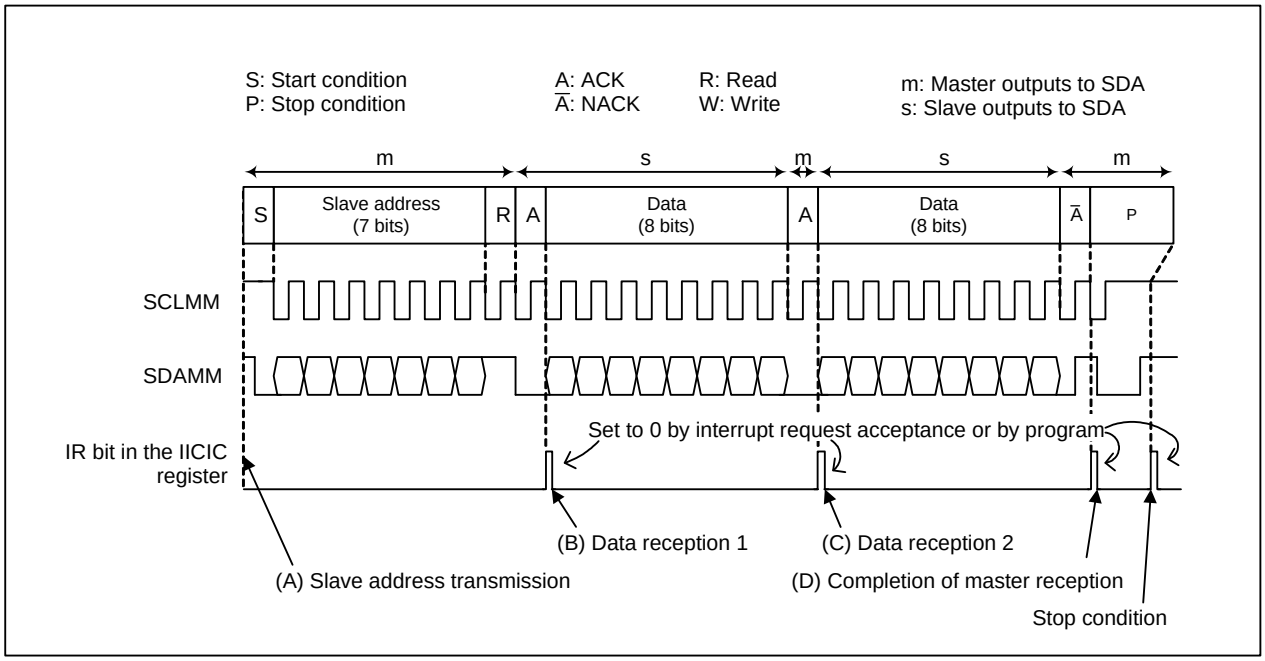


Figure 22.18 Example of Master Reception

(A) Slave address transmission
- (1) The BB bit in the S10 register must be 0 (bus free).
- (2) Write E0h to the S10 register. (Start condition standby)
- (3) Write a slave address to the upper 7 bits and a set the least significant bit (LSB) to 1. (Start condition generated, then slave address transmitted)

(B) Data reception 1 (after slave address transmission)

(In I2C-bus interrupt routine)
- (1) Write AFh to the S10 register. (Master receive mode)
- (2) Set the ACKBIT bit in the S20 register to 0 (ACK presents) because the data is not the last one.
- (3) Write dummy data to the S00 register

(C) Data reception 2 (data reception)

(In I2C-bus interrupt routine)
- (1) Read the received data from the S00 register
- (2) Set the ACKBIT bit in the S20 register to 1 (no ACK) because the data is the last one.
- (3) Write dummy data to the S00 register

(D) Completion of master reception

(In I2C-bus interrupt routine)
- (1) Read the received data from the S00 register
- (2) Write C0h to the S10 register. (Stop condition standby state)
- (3) Write dummy data to the S00 register (stop condition generated)

22.3.10.4 Slave Reception

The slave reception is described in this section. The initial settings described in 222.3.10.1 “Initial Settings” are assumed to be completed. Figure 22.19 shows the example of slave reception. The following programs (A) to (C) are executed at (A) to (C) in Figure 22.19, respectively.

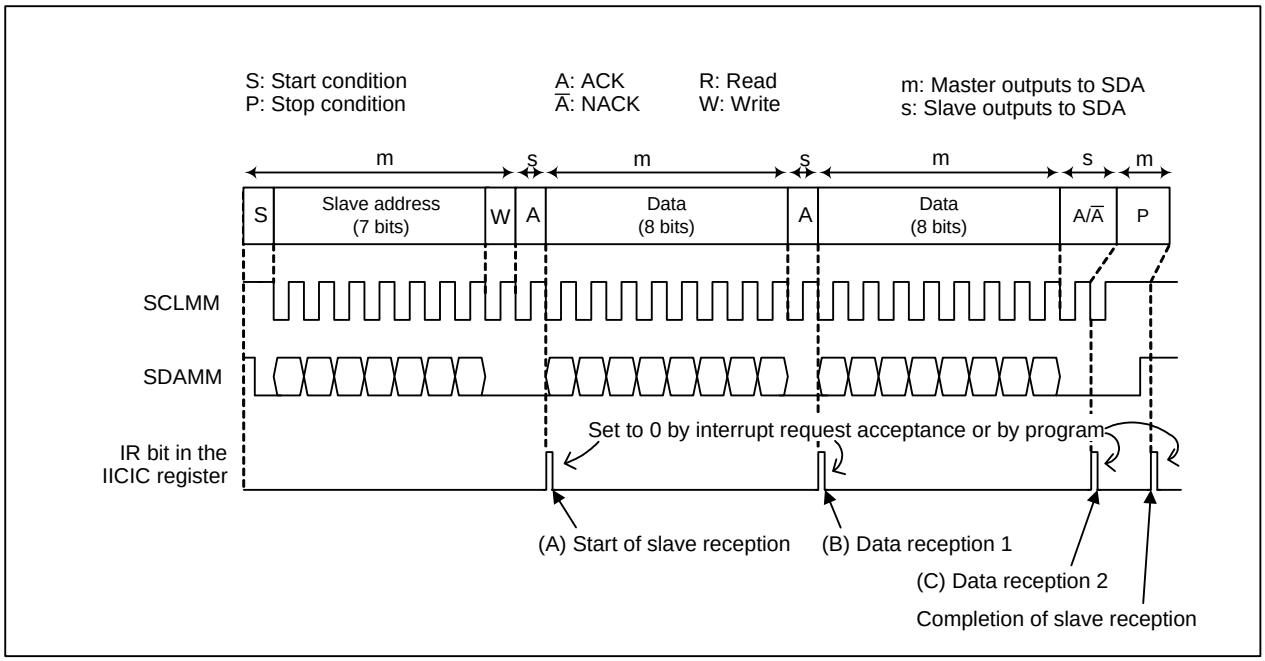


Figure 22.19 Example of Slave Reception

(A) Slave receive is started.
(In I2C-bus interrupt routine)
(1) Check the value of the S10 register. When the TRX bit is 0, the I2C interface is in slave receive mode.
(2) Write dummy data to the S00 register.

(B) Data reception 1
(In I2C-bus interrupt routine)
(1) Read the received data from the S00 register.
(2) Set the ACKBIT bit in the S20 register to 0 (ACK presents) because the data is not the last one.
(3) Write dummy data to the S00 register.

(C) Data reception 2
(In I2C-bus interrupt routine)
(1) Read the received data from the S00 register.
(2) Set the ACKBIT bit in the S20 register to 1 (no ACK presents) because the data is the last one.
(3) Write dummy data to the S00 register.

22.3.10.5 Slave Transmission

Slave transmission is described in this section. The initial settings described in 22.3.10.1 “Initial Settings” are assumed to be completed. Figure 22.20 shows the example of slave transmission. The following programs (A) to (B) are executed at (A) and (B) in Figure 22.20, respectively.
When arbitration lost is detected, the TRX bit becomes 0 (receive mode) even when the bit after the slave address is 1 (read). Therefore, after arbitration lost is detected, read the S00 register. When the bit 0 in the S00 register is 1, write 4Fh (slave transmit mode) to the S10 register and execute slave transmission.

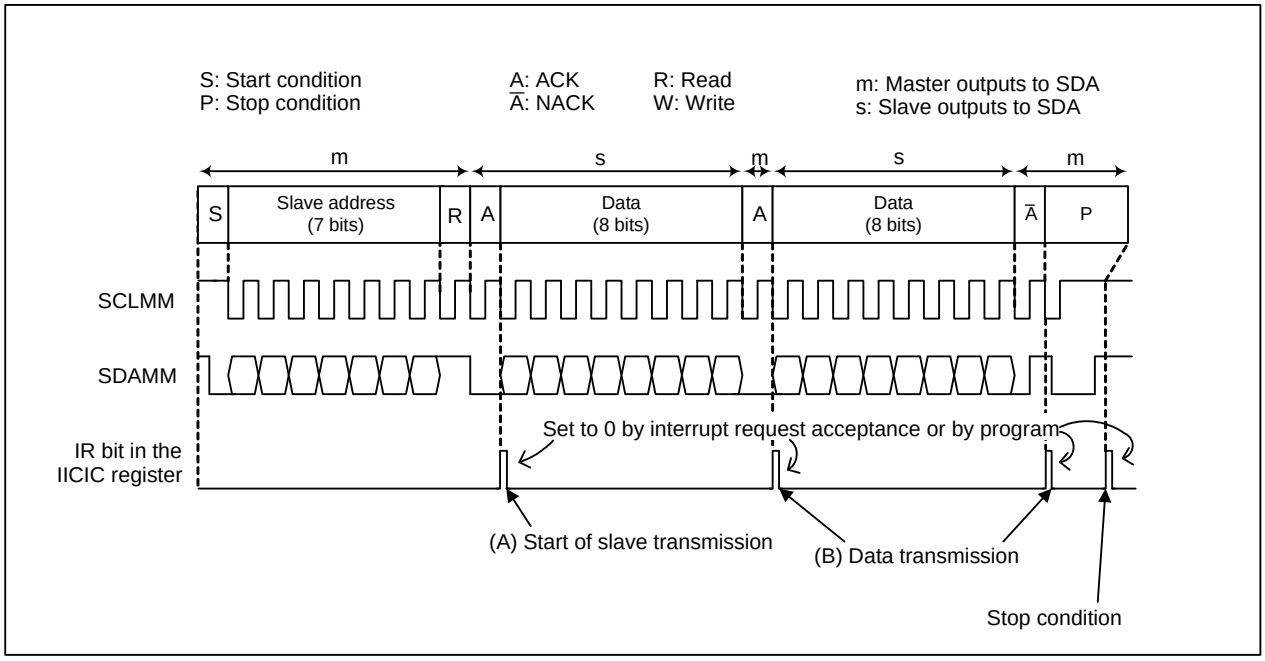


Figure 22.20 Example of Slave Transmission

(A) Start of slave transmission
(In I2C-bus interrupt routine)
(1) Check the value of the S10 register. When the TRX bit is 1, the I2C interface is in slave transmit mode.
(2) Write transmit data to the S00 register

(B) Data transmission
(In I2C-bus interrupt routine)
(1) Write transmit data to the S00 register

Write dummy data to the S00 register even if an interrupt occurs at an ACK clock of the last transmit data. After writing to the S00 register, the SCLMM pin is released.

22.4 Interrupts

The I2C interface generates interrupt requests. Figure 22.21 shows I2C Interface Interrupts, and Table 22.15 lists I2C-bus Interrupts.

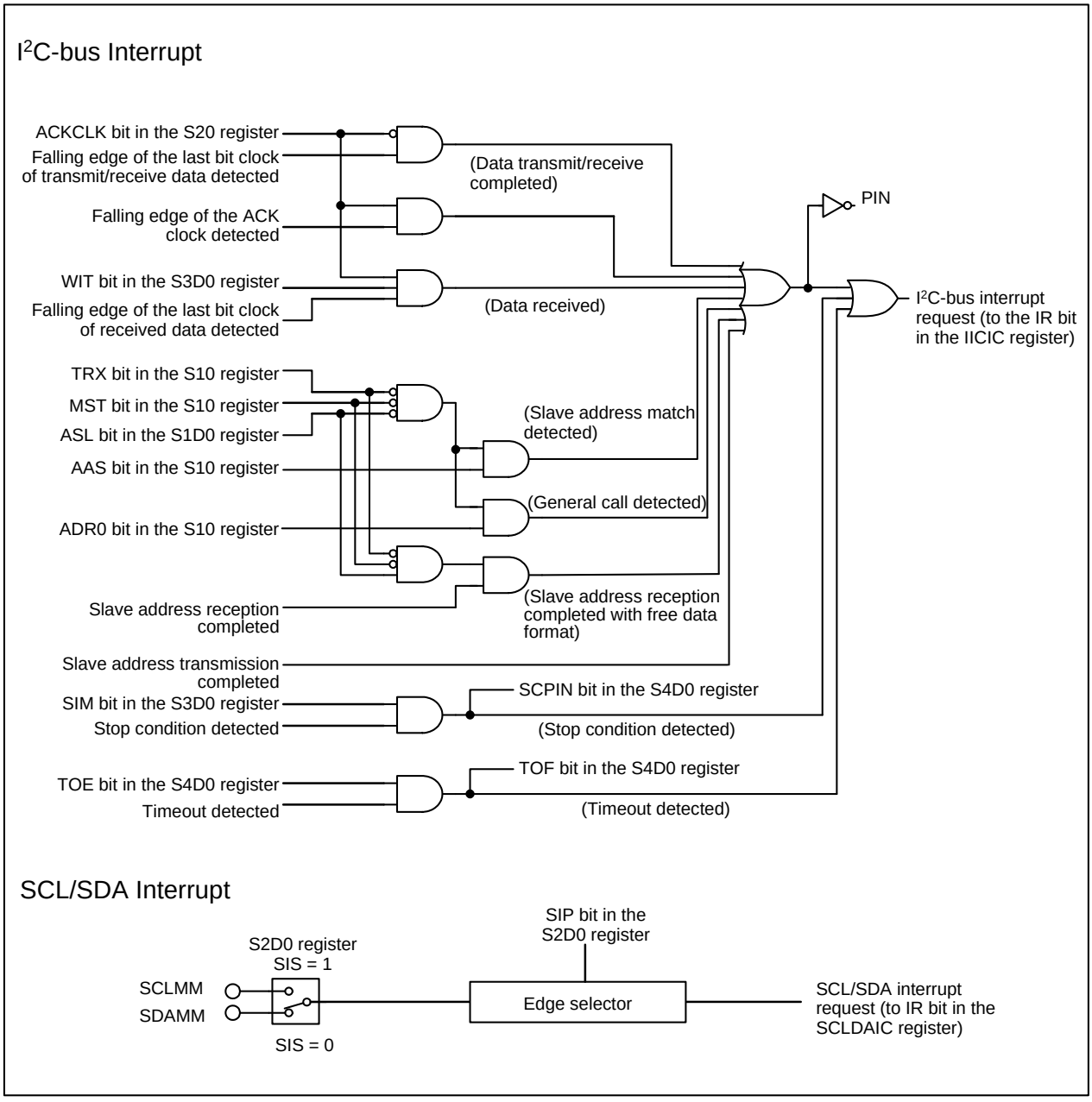


Figure 22.21 I2C Interface Interrupts

Table 22.15 I2C-bus Interrupts

Interrupt	Interrupt Source	Associated Bits (Register)		Interrupt Control Register
		Interrupt enabled	Interrupt request	
I2C-bus Interrupt	Completion of data transmit/receive When the ACKCLK bit in the S20 register is 0: Detection of the falling edge of the last clock of transmit/receive data through the SCLMM pin When the ACKCLK bit is 1: Detection of the falling edge of ACK clock through the SCLMM pin	—	PIN (S10)	IICIC
	Data reception (before ACK clock) Detection of the falling edge of the last clock of transmit/receive data through the SCLMM pin	WIT (S3D0)		
	Detection of slave address match Received slave address matches bits SAD6 to SAD0 in registers S0D0 to S0D2 in slave receive mode with addressing format (AAS bit in the S10 register = 1)	—		
	Detection of general call General call in slave receive mode with addressing format (ADR0 bit in the S10 register = 1)			
	Completion of receiving slave address in slave receive mode with free data format			
	Stop condition detected	SIM (S3D0)	SCPIN (S4D0)	
	Timeout detected	TOE (S4D0)	TOF (S4D0)	
SCL/SDA interrupt	Detection of the falling edge or rising edge of input/output signal for the SCLMM or SDAMM pin	—	—	SCLDAIC

Refer to 12.7 “Interrupt Control”. Table 22.16 lists Registers Associated with I2C Interface Interrupts.

Table 22.16 Registers Associated with I2C Interface Interrupts

Address	Register	Symbol	Reset Value
007Bh	I2C-bus Interface Interrupt Control Register	IICIC	XXXX X000b
007Ch	SCL/SDA Interrupt Control Register	SCLDAIC	XXXX X000b
0206h	Interrupt Source Select Register 2	IFSR2A	00h

When using the I2C-bus interface interrupt, set the IFSR22 bit in the IFSR2A register to 1 (I2C-bus interrupt). When using the SCL/SDA interrupt, set the IFSR23 bit in the IFSR2A register to 1 (SCL/SDA interrupt).

The SCL/SDA interrupt is enabled even in wait mode and stop mode.

The IR bit in the SCLDAIC register may become 1 (interrupt requested) when the ES0 bit in the S1D0 register, the SIP bit in the S2D0 register, or the SIS bit in the S2D0 register is changed. Therefore, follow the procedure below to change these bits. Refer to 12.13 “Notes on Interrupts”.

(1) Set bits ILVL2 to ILVL0 in the SCLDAIC register to 000b (interrupt disabled).
(2) Set the ES0 bit in the S1D0 register and bits SIP and SIS in the S2D0 register.
(3) Set the IR bit in the SCLDAIC register to 0 (no interrupt request).

22.5 Notes on Multi-master I2C-bus Interface

22.5.1 Limitation on CPU Clock

When the CM07 bit in the CM0 register is 1 (CPU clock is a sub clock), do not access the registers listed in Table 22.4 “Registers”. Set the CM07 bit to 0 (main clock, PLL clock, or on-chip oscillator clock) to access these registers.

22.5.2 Register Access

Refer to the notes below when accessing the I2C interface control registers. The period from the rising edge of the first clock of the slave address or 1-byte data transmission/reception to the falling edge of an ACK clock is considered to be the transmission/reception period. When the ACKCLK bit is 0 (no ACK clock), the transmission/reception period is from the rising edge of the first clock of the slave address or 1-byte data transmission/reception to the falling edge of the eighth clock.

22.5.2.1 S00 Register

Do not write to the S00 register during transmission/reception.

22.5.2.2 S1D0 Register

Do not change bits other than the IHR bit in the S1D0 register during transmission/reception.

22.5.2.3 S20 Register

Do not change bits other than the ACKBIT bit in the S20 register during transmission/reception.

22.5.2.4 S3D0 Register

- Do not use the bit managing instruction (read-modify-write instruction) to access the S3D0 register. Use the MOV instruction to write to this register.
- Rewrite bits ICK1 and ICK0 when the ES0 bit in the S1D0 register is 0 (I2C interface disabled).

22.5.2.5 S4D0 Register

Rewrite bits ICK4 to ICK2 when the ES0 bit in the S1D0 register is 0 (I2C interface disabled).

22.5.2.6 S10 Register

- Do not use the bit managing instruction (read-modify-write instruction) to access the S10 register. Use the MOV instruction to write to this register.
- Do not write to the S10 register when bits MST and TRX change their values.

Refer to operation examples in 22.3 “Operations” for bits MST and TRX change.

23. Serial Bus Interface

23.1 Overview

The serial bus interface has one independent channel (SBI0).
The SBI0 has the following modes:

- Synchronous serial communication mode
- 4-wire serial bus mode

To select a mode, use the SSUMS bit in the SS0MR2 register.

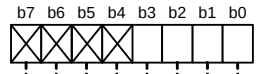
23.2 Registers

Table 23.1 Registers

Address	Register	Symbol	Reset Value
0353h	SS0 Bit Counter Register	SS0BR	1111 1000b
0354h	SS0 Transmit Data Register	SS0TDR	FFh
0355h			FFh
0356h	SS0 Receive Data Register	SS0RDR	FFh
0357h			FFh
0358h	SS0 Control Register H	SS0CRH	00h
0359h	SS0 Control Register L	SS0CRL	0111 1101b
035Ah	SS0 Mode Register	SS0MR	0001 0000b
035Bh	SS0 Enable Register	SS0ER	00h
035Ch	SS0 Status Register	SS0SR	00h
035Dh	SS0 Mode Register 2	SS0MR2	00h

23.2.1 SS0 Bit Counter Register (SS0BR)

SS0 Bit Counter Register



Symbol: SS0BR
Address: 0353h
Reset Value: 1111 1000b

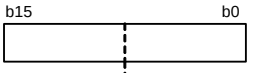
Bit Symbol	Bit Name	Function	RW
BS0	Serial Bus Interface Data Transfer Length Bit	b3 b2 b1 b0 0 0 0 0 : 16 bits 1 0 0 0 : 8 bits 1 0 0 1 : 9 bits 1 0 1 0 : 10 bits 1 0 1 1 : 11 bits 1 1 0 0 : 12 bits 1 1 0 1 : 13 bits 1 1 1 0 : 14 bits 1 1 1 1 : 15 bits Only set the values listed above.	RW
BS1			RW
BS2			RW
BS3			RW
— (b7-b4)	No register bits. If necessary, set to 0. The read value is 1.		—

BS0 to BS3 (Serial bus interface data transfer length bit) (b0 to b3)

Do not write to bits BS0 to BS3 during serial bus interface operation. Write to these bits when the RE bit in the SSER register is set to 0 (reception disabled) and the TE bit is set to 0 (transmission disabled).

23.2.2 SS0 Transmit Data Register (SS0TDR)

SS0 Transmit Data Register

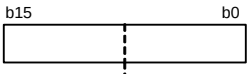


Symbol	Address	Reset Value
SS0TDR	0355h - 0354h	FFFFh

Function	RW
This register stores transmit data. Data should be written as LSB aligned. When the transmit/receive shift register is detected to be empty, the transmit data stored in this register is transferred to the transmit/receive shift register to start data transmission. If the next transmit data is set to this register while the current data is being transmitted from the transmit/receive shift register, data transmission continues. When the MLS bit in the SS0MR register is 1 (LSB first), the MSB-LSB reversed data is read from this register.	RW

23.2.3 SS0 Receive Data Register (SS0RDR)

SS0 Receive Data Register



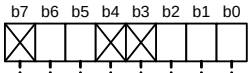
Symbol	Address	Reset Value
SS0RDR	0357h - 0356h	FFFFh

Function	RW
This register stores received data. Receive operation completes when one frame of data received by the transmit/receive shift register is transferred to this register. The next data reception is enabled simultaneously when one sequence of receive operation completes. Continuous data reception is supported by this double buffer structure of the transmit/receive shift register and the SS0RDR register.	RO

When the RDRF bit in the SS0SR register becomes 1 (received data is stored), the next received data is not stored in the SS0RDR register. When the OER bit in the SS0SR register becomes 1 (overrun error), the received data is nullified.

23.2.4 SS0 Control Register H (SS0CRH)

SS0 Control Register H



Symbol: SS0CRH
Address: 0358h
Reset Value: 00h

Bit Symbol	Bit Name	Function	RW
CKS0	Transmit/Receive Clock Rate Select Bit	b6 b5 b4 0 0 0 : f1 / 256 0 0 1 : f1 / 128 0 1 0 : f1 / 64 0 1 1 : f1 / 32 1 0 0 : f1 / 16 1 0 1 : f1 / 8 1 1 0 : f1 / 4 1 1 1 : Do not use this combination	RW
CKS1			RW
CKS2			RW
— (b4-b3)	No register bits. If necessary, set to 0. The read value is 0.		—
MSS	Master/Slave Mode Select Bit	0: Slave mode 1: Master mode	RW
RSSTP	Receive Single Stop bit	After receiving the current frame, 0: Continue receive operation (output the receive clock) 1: End receive operation (stop the receive clock)	RW
— (b7)	No register bit. If necessary, set to 0. The read value is 0.		—

CKS2 to CKS0 (Transmit/receive clock rate select bit) (b2 to b0)

The clock rate selection is applicable only when the MSS bit is set to 1 (master mode).

MSS (Master/slave mode select bit) (b5)

To output the transmit/receive clock at the SSCK0 pin, set this bit to 1. This bit becomes 0 when the CE bit in the SS0SR register becomes 1 (conflict error).

RSSTP (Receive single stop bit)

This bit is disabled when the MSS bit is 0 (slave mode).
When the RSSTP bit is 1 and the data in the SS0RDR register is not read while receiving, the receive clock is stopped after the current frame reception is completed. When the data in the SS0RDR register is read while receiving, the receive clock is output after the current frame reception is completed.
When the RSSTP bit is 0, while the RE bit in the SS0ER register is 1 (enable data reception), the receive clock is output after the current frame reception is completed even if the SS0RDR register is not read.

23.2.5 SS0 Control Register L (SS0CRL)

SS0L Control Register L

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	Reset Value
SS0CRL	0359h	0111 1101b

Bit Symbol	Bit Name	Function	RW
— (b0)	No register bit. If necessary, set to 0. The read value is 1.		—
SRES	Serial Bus Interface Controller Reset Bit	After setting this bit to 1, setting to 0, initializes the transmit/receive controller and the transmit/receive shift register. The internal register (1) value remains unchanged.	RW
— (b3-b2)	No register bits. If necessary, set to 0. The read value is undefined.		—
SOLP	SOL Write Protect Bit	0: Unlock the protection of the SOL bit (SOL bit setting is reflected to output pin) 1: Output pin level remains changed. This bit is read as 1	RW
SOL	Serial Data Output Setting Bit	When read: 0: Serial data output pin is low 1: Serial data output pin is high When write: 0: Drive serial data output pin low 1: Drive serial data output pin high	RW
— (b6)	No register bit. If necessary, set to 0. The read value is 1.		—
— (b7)	No register bit. If necessary, set to 0. The read value is 0.		—

Note:
1. Registers SS0BR, SS0CRH, SS0CRL, SS0ER, SS0SR, SS0MR2, SS0TDR and SS0RDR, and bits MLS, CPOS, and CPHS in the SS0MR register.

SRES (Serial bus interface controller reset bit) (b1)

Set the SRES bit when the TE bit in the SS0ER register is 0 (disable data transmission). When the SRES bit is set to 1, the transmit/receive controller and the transmit/receive shift register are reset. If the SRES bit is set to 0 after that, the reset is deasserted.

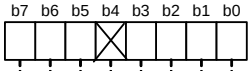
SOL (Serial data output setting bit) (b5)

To change the output pin level, set the SOL bit before or after transmitting data. Set the SOL bit to 0 or 1 and the SOLP bit to 0 simultaneously by the MOV instruction. When the serial bus interface controller is not reset at this timing, set the SRES bit to 0.
Do not write to this bit during data transmission.

23.2.6 SS0 Mode Register (SS0MR)

SS0 Mode Register

Symbol: SS0MR
Address: 035Ah
Reset Value: 0001 0000b



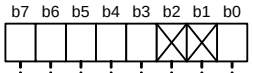
Bit Symbol	Bit Name	Function	RW
BC0	Bit Counter	Number of bits left for transmission/ reception b3 b2 b1 b0 0 0 0 0 : 16 bits left 0 0 0 1 : 1 bit left 0 0 1 0 : 2 bits left 0 0 1 1 : 3 bits left 0 1 0 0 : 4 bits left 0 1 0 1 : 5 bits left 0 1 1 0 : 6 bits left 0 1 1 1 : 7 bits left 1 0 0 0 : 8 bits left 1 0 0 1 : 9 bits left 1 0 1 0 : 10 bits left 1 0 1 1 : 11 bits left 1 1 0 0 : 12 bits left 1 1 0 1 : 13 bits left 1 1 1 0 : 14 bits left 1 1 1 1 : 15 bits left	RO
BC1			RO
BC2			RO
BC3			RO
— (b4)	No register bit. If necessary, set to 0. The read value is 1.		—
CPHS	SSCK0 Clock Phase Select Bit	0: Change data at odd edges (load data at even edges) 1: Change data at even edges (load data at odd edges)	RW
CPOS	SSCK0 Clock Polarity Select Bit	0: High when clock is stopped 1: Low when clock is stopped	RW
MLS	Bit Order Select Bit	0: MSB first 1: LSB first	RW

CPHS (SSCK0 clock phase select bit) (b5)

Set this bit to 0 in synchronous serial communication mode.

23.2.7 SS0 Enable Register (SS0ER)

SS0 Enable Register

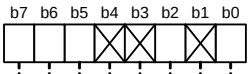


Symbol	Address	Reset Value
SS0ER	035Bh	00h

Bit Symbol	Bit Name	Function	RW
CEIE	Conflict Error Interrupt Enable Bit	0: Disable conflict error interrupt request 1: Enable conflict error interrupt request	RW
— (b2-b1)	No register bits. If necessary, set to 0. The read value is 0.		—
RE	Receive Enable Bit	0: Disable data reception 1: Enable data reception	RW
TE	Transmit Enable Bit	0: Disable data transmission 1: Enable data transmission	RW
RIE	Receive Interrupt Enable Bit	0: Disable receive data register full or overrun error interrupt request 1: Enable receive data register full or overrun error interrupt request	RW
TEIE	Transmit End Interrupt Enable Bit	0: Disable transmit end interrupt request 1: Enable transmit end interrupt request	RW
TIE	Transmit Interrupt Enable Bit	0: Disable transmit data register empty interrupt request 1: Enable transmit data register empty interrupt request	RW

23.2.8 SS0 Status Register (SS0SR)

SS0 Status Register



Symbol	Address	Reset Value
SS0SR	035Ch	00h

Bit Symbol	Bit Name	Function	RW
CE	Conflict Error Flag	0: No conflict error 1: Conflict error	RW
— (b1)	No register bits. If necessary, set to 0. The read value is undefined.		—
ORER	Overrun Error Flag	0: No overrun error 1: Overrun error	RW
— (b4-b3)	No register bit. If necessary, set to 0. The read value is undefined.		—
RDRF	Receive Data Register Full Flag	0: No data left in the SS0RDR register 1: Received data left in the SS0RDR register	RW
TEND	Transmit End Flag	0: Transmission continues 1: Transmission has completed	RW
TDRE	Transmit Data Register Empty Flag	0: Unsent data left in the SS0TDR register 1: No data left in the SS0TDR register	RW

Insert four or more NOP instructions when performing either of following operations continuously. And that is the operation (a) below is performed, four or more NOP instructions are inserted, then the operation (b) is performed.

- Access the SS0SR register (a), then access the SS0SR register (b).
- Write to the SS0TDR register (a), then read the SS0SR register (b).
- Read the SS0RDR register (a), then read the SS0SR register (b).

The state remains unchanged if 1 is written to bits in the SS0SR register. To set these bits to 0, first read the register, then use the MOV instruction to set the necessary bits to 0 and set the rest of bits to 1.

CE (Conflict error flag) (b0)

This bit becomes 1 under either of the following conditions:

- The $\overline{SCS0}$ pin as input is low when the SSUMS bit in the SS0MR2 register is 1 (4-wire serial bus mode), and the MSS bit in the SS0CRH register is 1 (master mode).
- The $\overline{SCS0}$ pin as input becomes high during frame transmission/reception when the SSUMS bit is 1 (4-wire serial bus mode), and the MSS bit is 0 (slave mode).

ORER (Overrun error flag) (b2)

This bit indicates the data reception ended unexpectedly because of an overrun error. This bit becomes 1 when the next serial data reception has completed while the RDRF bit is 1. Data transmission/reception is disabled while the ORER bit is 1 and the MSS bit is 1 (master mode).

RDRF (Receive data register full flag) (b5)

This bit becomes 0 when data is read from the SS0RDR register.

TEND (Transmit end flag) (b6)

This bit becomes 1 when no data to be transmitted is left in the SS0TDR register before the end of the transmission of the last bit of current data. This bit becomes 0 when data is written to the SS0TDR register.

TDRE (Transmit data register empty flag) (b7)

This bit becomes 1 when the TE bit in the SS0ER register is switched from 0 (data transmission disabled) to 1 (data transmission enabled). It also becomes 1 when data is transferred from the SS0TDR register to the transmit/receive shift register. This bit becomes 0 when data is written to the SS0TDR register.
When writing 0 to the TDRE bit, perform the operation while the TE bit in the SS0ER register is 0 (disable data transmission).

23.2.9 SS0 Mode Register 2 (SS0MR2)

SS0 Mode Register 2

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	Reset Value
SS0MR2	035Dh	00h

Bit Symbol	Bit Name	Function	RW
SSUMS	Mode Select Bit	0: Synchronous serial communication mode 1: 4-wire serial bus mode	RW
CSOS	$\overline{SCS0}$ Pin Open Drain Output Select Bit	0: CMOS output 1: N-channel open drain output	RW
SOOS	Serial Data Open Drain output Select Bit	0: CMOS output 1: N-channel open drain output	RW
SCKOS	SSCK0 Pin Open Drain Output Select Bit	0: CMOS output 1: N-channel open drain output	RW
CSS0	$\overline{SCS0}$ Pin Function Select Bit	b5 b4 0 0 : No function as chip select 0 1 : $\overline{SCS0}$ pin as input 1 0 : 1 1 : } $\overline{SCS0}$ pin as output	RW
CSS1			RW
SCKS	SSCK0 Pin Function Select Bit	0: No function as I/O pin for transmit/ receive clock 1: I/O pin for transmit/receive clock	RW
BIDE	Bidirectional mode Enable Bit	0: Standard mode (two individual pins for data I/O) 1: Bidirectional mode (one common pin for data I/O)	RW

SSUMS (Mode select bit) (b0)

Refer to 23.3.1.6 “Data I/O Pin and Transmit/Receive Shift Register” for information on combination of data I/O pins.

SOOS (Serial data open drain output select bit) (b2)

When the SOOS bit is set to 0 (CMOS output), set the direction register bits corresponding to pins SSI0 and SSO0 to 0 (input mode).

CSS1 and CSS0 ($\overline{SCS0}$ pin function select bit) (b5, b4)

Irrespective of the CSS1 and CSS0 bit setting, the $\overline{SCS0}$ pin function is not applicable when the SSUMS bit is 0 (synchronous serial communication mode).

BIDE (Bidirectional mode enable bit) (b7)

Refer to 23.3.1.6 “Data I/O Pin and Transmit/Receive Shift Register” for information on combination of data I/O pins.

When the SSUMS bit is 0 (synchronous serial communication mode), the BIDE bit setting is ignored and standard mode is always selected.

23.3 Operations

23.3.1 Common Operations

23.3.1.1 Transmit/Receive Clock

To use the serial bus interface in synchronous serial communication mode or 4-wire serial bus mode, configure the SSCK0 pin to be a transmit/receive clock pin by setting the SCKS bit in the SS0MR2 register to 1.

(1) To operate the serial bus interface in master mode

When the MSS bit in the SS0CRH register is 1 (master mode), select a transmit/receive clock from seven internal clocks (f1/256, f1/128, f1/64, f1/32, f1/16, f1/8 and f1/4).
Since the SSCK0 pin functions as clock output, the selected transmit/receive clock is output from the SSCK0 pin as soon as the data transmission/reception starts.

(2) To operate the serial bus interface in slave mode

When the MSS bit in the SS0CRH register is 0 (slave mode), the external clock is used.
Set the corresponding pin as input by the port direction register. The SSCK0 pin functions as clock input.

23.3.1.2 Association between Transmit/Receive Clock Polarity, Phase and Data

The relation between the transmit/receive clock polarity and phase for transmit/receive data varies with the setting combination of the SSUMS bit in the SS0MR2 register, bits CPHS and CPOS in the SS0MR register.

Figure 23.1 shows the relation between those parameters.

Also, the MSB first transfer or LSB first transfer can be selected by setting the MLS bit in the SS0MR register. When the MLS bit is set to 1, transfer is started from the LSB and proceeds to the MSB. When the MLS bit is set to 0, transfer is started from the MSB and proceeds to the LSB.

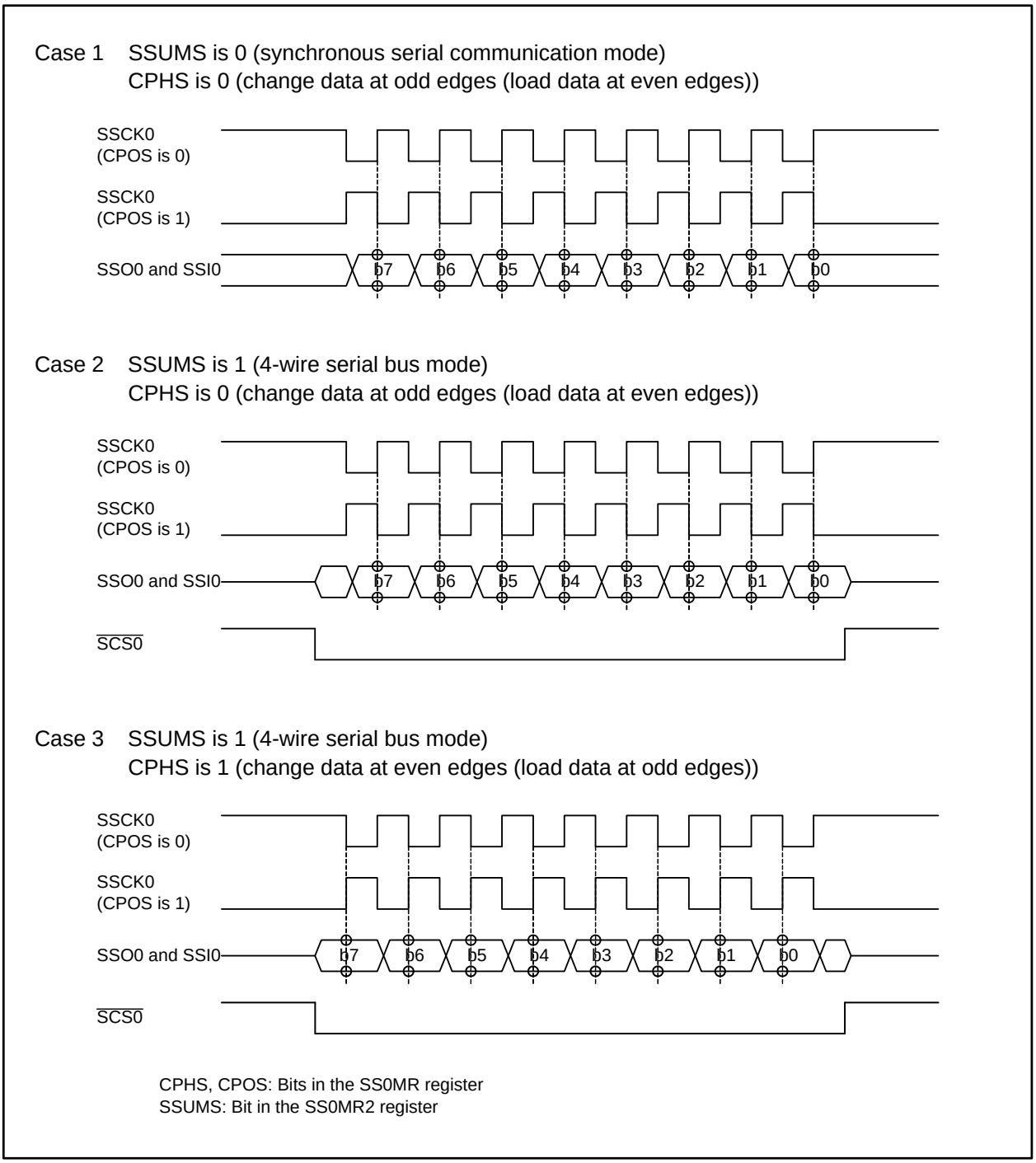


Figure 23.1 Transmit/Receive Clock Polarity and Phase of Transmit/Receive Data

23.3.1.3 Transmit/Receive Shift Register

The transmit/receive shift register transmits and receives serial data. Data transferred to the transmit/receive shift register is shifted-out with the MSB first. Received data is shifted-in with the LSB first.

Figure 23.2 shows the transmit/receive shift register operation.

23.3.1.4 Data transfer direction

The bit order to be transmitted/received can be selected by using the MLS bit in the SS0MR register. When the MLS bit is 1 (LSB first), transmission starts from the LSB and completes with the MSB. In receive operation, the first received bit is considered as the LSB. When the MLS bit is 0 (MSB first), the bit order to be transmitted is reversed and the first received bit is considered as the MSB.

(1) Transmit operation

When the MLS bit is 0 (MSB first), the written value is reflected in the SS0TDR register in the written order.

When the MLS bit is 1 (LSB first), the written value is reflected in the SS0TDR register in the reversed order, that is, the reversed written value is read from the SS0TDR register.

In both cases, however, data is transferred to the transmit/receive shift register in the transmitted order.

(2) Receive operation

When the MLS bit is 0 (MSB first), the received data is transferred from the transmit/receive shift register to the SS0RDR register in the received order.

When the MLS bit is 1 (LSB first), the received data is transferred from the transmit/receive shift register to the SS0RDR register in the reversed order.

23.3.1.5 Variable-Length Data Transmission/Reception

When the data length is less than 16 bits, the shift-in/shift-out position is changed to adjust the bit position.

This function allows transmit/receive data to be LSB aligned.

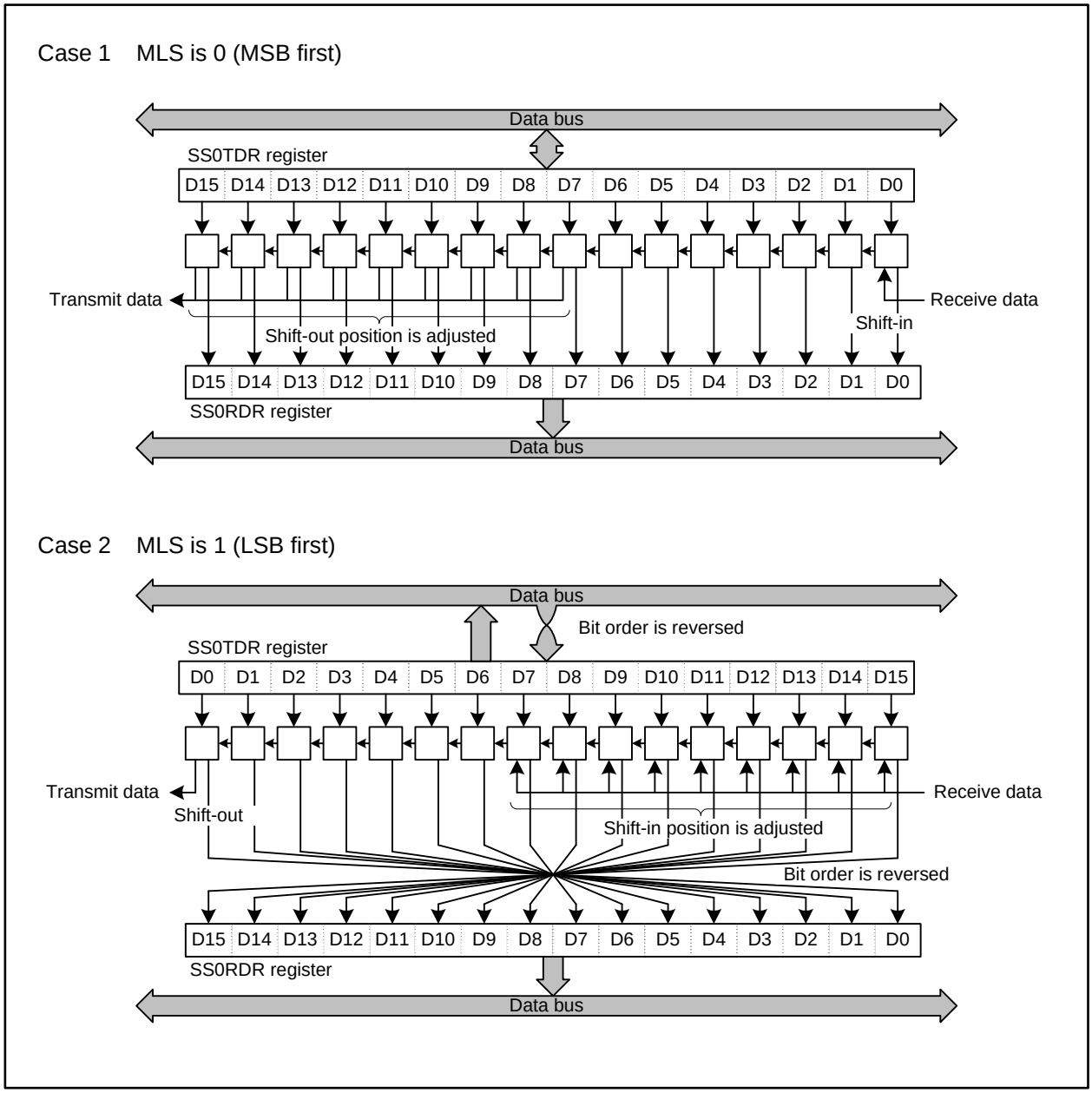


Figure 23.2 Transmit/Receive Shift Register Operation

23.3.1.6 Data I/O Pin and Transmit/Receive Shift Register

The connection pattern of the data I/O pins and the transmit/receive shift register varies with the setting combination of the MSS bit in the SS0CRH register, bits SSUMS and BIDE in the SS0MR2 register. Figure 23.3 shows the Data I/O Pins and Transmit/Receive Shift Register.

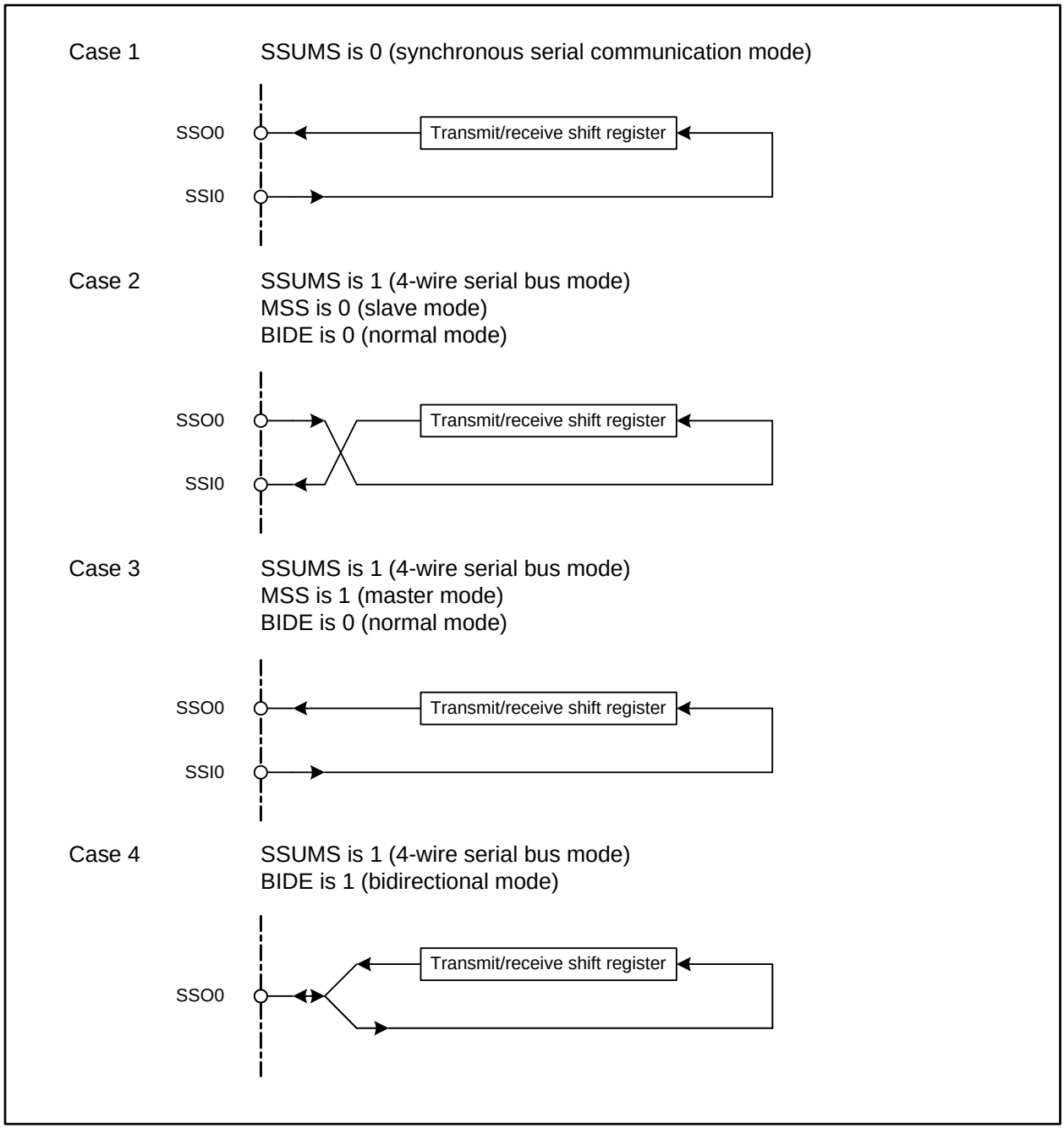


Figure 23.3 Data I/O Pins and Transmit/Receive Shift Register

23.3.1.7 Error Processing

When an error occurs, follow the procedure below to reset the settings. Refer to 23.5.1 “SS0SR register” for notes when writing to the SS0SR register.

When an overrun error occurs:

(1) Set the TE bit to 0 (disable data transmission) and the RE bit to 0 (disable data reception) in the SS0ER register.
(2) Set the SS0SR register to 00h (no error status).
(3) Dummy read the SS0RDR register.
(4) Set the RE bit to 1 (enable data reception). When performing a transmit operation, set the TE bit to 1 (enable data transmission).

When a conflict error occurs:

(1) Set the TE bit to 0 (disable data transmission), and set the RE bit to 0 (disable data reception) in the SS0ER register.
(2) Set the SS0SR register to 00h. (no error status)
(3) Set the SRES bit in the SS0CRL register to 1, then to 0 (initializes the transmit/receive controller and the transmit/receive shift register).
(4) When using as a master device, set the MSS bit in the SS0CRH register to 1 (master mode).
(5) When performing a receive operation, set the RE bit to 1 (enable data reception). For a transmit operation, set the TE bit to 1 (enable data transmission).

When other errors occur:

(1) Set the TE bit to 0 (disable data transmission), and the RE bit to 0 (disable data reception) in the SS0ER register.
(2) Set the SS0SR register to 00h. (no error status).
(3) Set the SRES bit in the SS0CRL register to 1, then to 0.
(4) When performing a receive operation, set the RE bit to 1 (enable data reception). For a transmit operation, set the TE bit to 1 (enable data transmission).

23.3.2 Synchronous Serial Communication Mode

Table 23.2 Synchronous Serial Communication Mode Specifications

Item	Specification
Data format	Character length: 8 to 16 bits (variable length)
Master/slave mode	Selectable
I/O pins	SSCK0 (I/O): Clock I/O pin SSI0 (input): Data input pin SSO0 (output): Data output pin
Transmit/receive clocks	• When the MSS bit in the SS0CRH register is 0 (slave mode): External clock (input at the SS0CK pin) • When the MSS bit in the SS0CRH register is 1 (master mode): Internal clock (output at the SSCK0 pin) Selectable from f1/256, f1/128, f1/64, f1/32, f1/16, f1/8, f1/4
Transmit starting conditions	• TE bit in the SS0ER register is 1 (transmission enabled) • TDRE bit in the SS0SR register is 0 (unsent data left in the SS0TDR register) • ORER bit in the SS0SR register is 0 (no overrun error) • Clock input at the SSCK0 pin (applicable only when the MSS bit in the SS0CRH register is 0 (slave mode))
Receive starting conditions	• RE bit in the SS0ER register is 1 (reception enabled) • ORER bit in the SS0SR register is 0 (no overrun error) • Read operation to the SS0RDR register (applicable only when the MSS bit in the SS0CRH register is 1 (master mode)) • Clock input at the SSCK0 pin (applicable only when the MSS bit in the SS0CRH register is 0 (slave mode))
Error detection	• Overrun error Overrun error occurs if, while the RDRF bit in the SS0SR register is 1 (received data left in the SS0RDR register), reception of next serial data has completed
Interrupt request sources	Four interrupt request sources (transmit end, transmit data register empty, receive data register full, and overrun error) (1)
Selectable functions	• Programmable bit order MSB first or LSB first, selectable with the MLS bit in the SS0MR register • SSCK0 clock polarity Low or high when clock is stopped, selectable with the CPOS bit in the SS0MR register

Note:
1. Each channel has its own interrupt vector table.

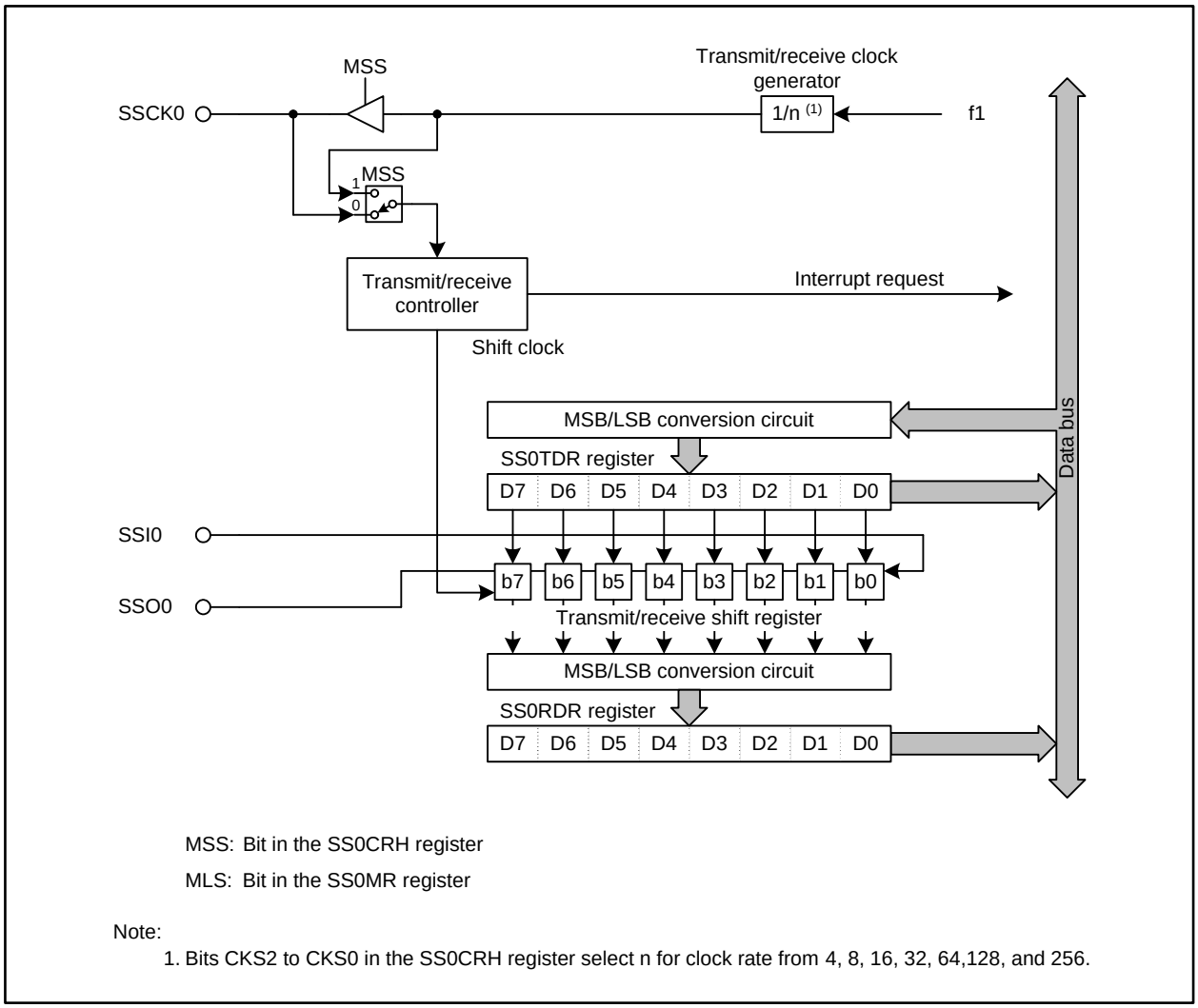


Figure 23.4 Block Diagram of Synchronous Serial Communication Mode

In synchronous serial communication mode, the function of the I/O pins varies with the setting combination of the MSS bit in the SS0CRH register, bits RE and TE in the SS0ER register. The SSCK0 pin functions as output in master mode. This pin is used for input when the slave mode is selected.

Table 23.3 Communication Modes and I/O Pins

Bit Setting					Pin State		
SSUMS	BIDE	MSS	TE	RE	SSI0	SSO0	SSCK0
0	Disabled	0 (slave)	0	1	Input	– (1)	Input
			1	0	– (1)	Output	
				1	Input	Output	
		1 (master)	0	1	Input	– (1)	Output
			1	0	– (1)	Output	
				1	Input	Output	

Note:
1. This pin can be used as a programmable I/O port.

SSUMS and BIDE: Bits in the SS0MR2 register
MSS: Bit in the SS0CRH register
TE and RE: Bits in the SS0ER register

23.3.2.1 Initialization of Synchronous Communication Mode

Figure 23.6 shows the initialization flow of synchronous serial communication mode. Initialize the TE bit in the SS0ER register to 0 (transmission disabled) and the RE bit in the SS0ER register to 0 (reception disabled) before data transmit/receive operation.
Refer to 23.5.1 “SS0SR register” for notes when writing to the SS0SR register.

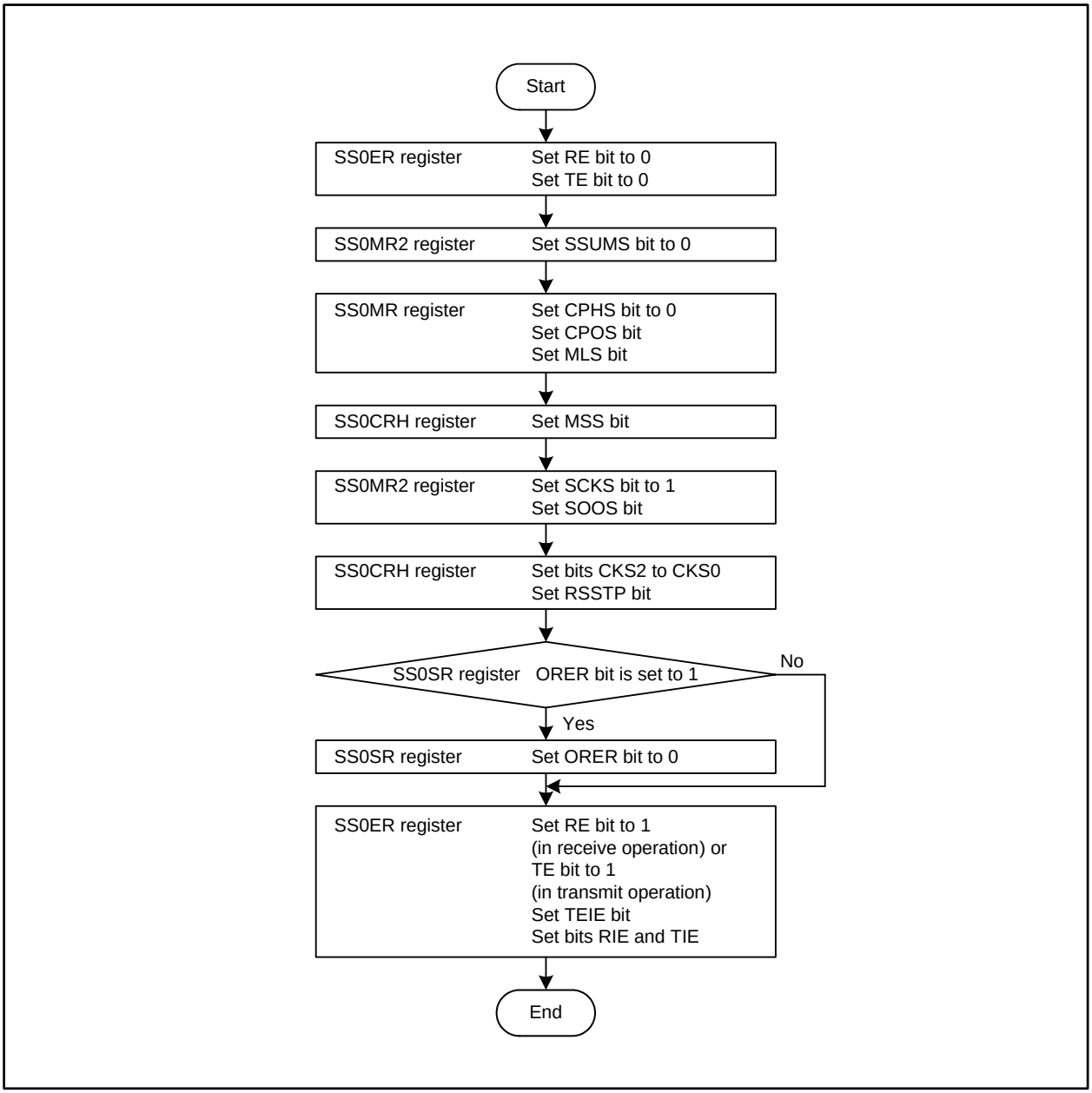


Figure 23.5 Initialization Flow in Synchronous Communication Mode

To change communication mode or the communication data format, set bits TE and RE to 0 in advance. Note that bits RDRF and ORER and the SS0RDR register are unaffected even if the RE bit is set to 0.

23.3.2.2 Data Transmission

Figure 23.6 shows an example of transmit operation in synchronous serial communication mode. During data transmission, the serial bus interface operates as described below.

When it operates in master mode, an internally generated clock as transmit/receive clock is output from the SSCK0 pin. When it is in slave mode, the transmit/receive clock is a clock input from the SSCK0 pin. In both cases, transmit data is output synchronized with the transmit/receive clock.

When the TE bit in the SS0ER register is set to 1 (transmission enabled), if the TIE bit in the SS0ER register is 1 (enable transmit data register empty interrupt request), and the TDRE bit in the SS0SR register is 1 (no data left in the SS0TDR register), a transmit data empty interrupt request (TXI) is generated. After that, if transmit data is written to the SS0TDR register, the TDRE bit automatically becomes 0 (unsent data left in the SS0TDR register), and data in the SS0TDR register is transferred to the transmit/receive shift register. Then the TDRE bit becomes 1 and data transmission starts. In addition, if the TIE bit in the SS0ER register is 1, a transmit data empty interrupt request (TXI) is generated.

When the TDRE bit is 0, after transmitting one frame of data, the data is transferred from the SS0TDR register to the transmit/receive shift register to start the next data transmission. When the TDRE bit is 1, after transmitting the eighth bit of data, the TEND bit in the SS0SR register becomes 1 (transmission has completed). In addition, if the TEIE bit in the SS0ER register is 1 (transmit end interrupt enabled), a transmit end interrupt request (TEI) is generated.

After data transmission is completed, the SSCK0 pin is fixed to the level specified by the CPOS bit in the SS0MR register.
Note that data cannot be transmitted while the ORER bit in the SS0SR register is 1 (overrun error).
Figure 23.7 shows an example of data transmission flow in synchronous serial communication mode.

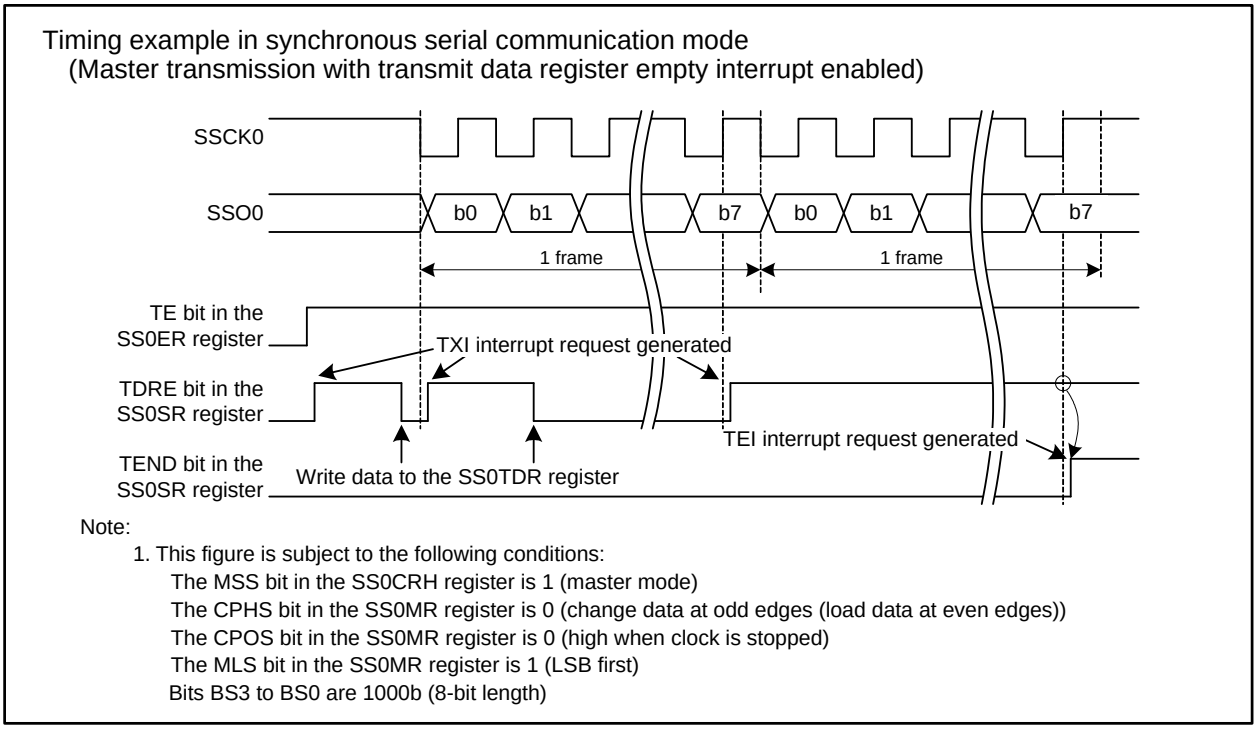


Figure 23.6 Transmit Operation Example in Synchronous Serial Communication Mode

Transmitting data using the transmit data empty interrupt

When using the transmit data empty interrupt, set the interrupt priority level of the SS0IC register, and set the TIE bit in the SS0ER register to 1 (enable transmit data register empty interrupt request). When the TE bit in the SS0ER register is 1 (enable data transmission), the serial bus interface 0 interrupt request is generated.

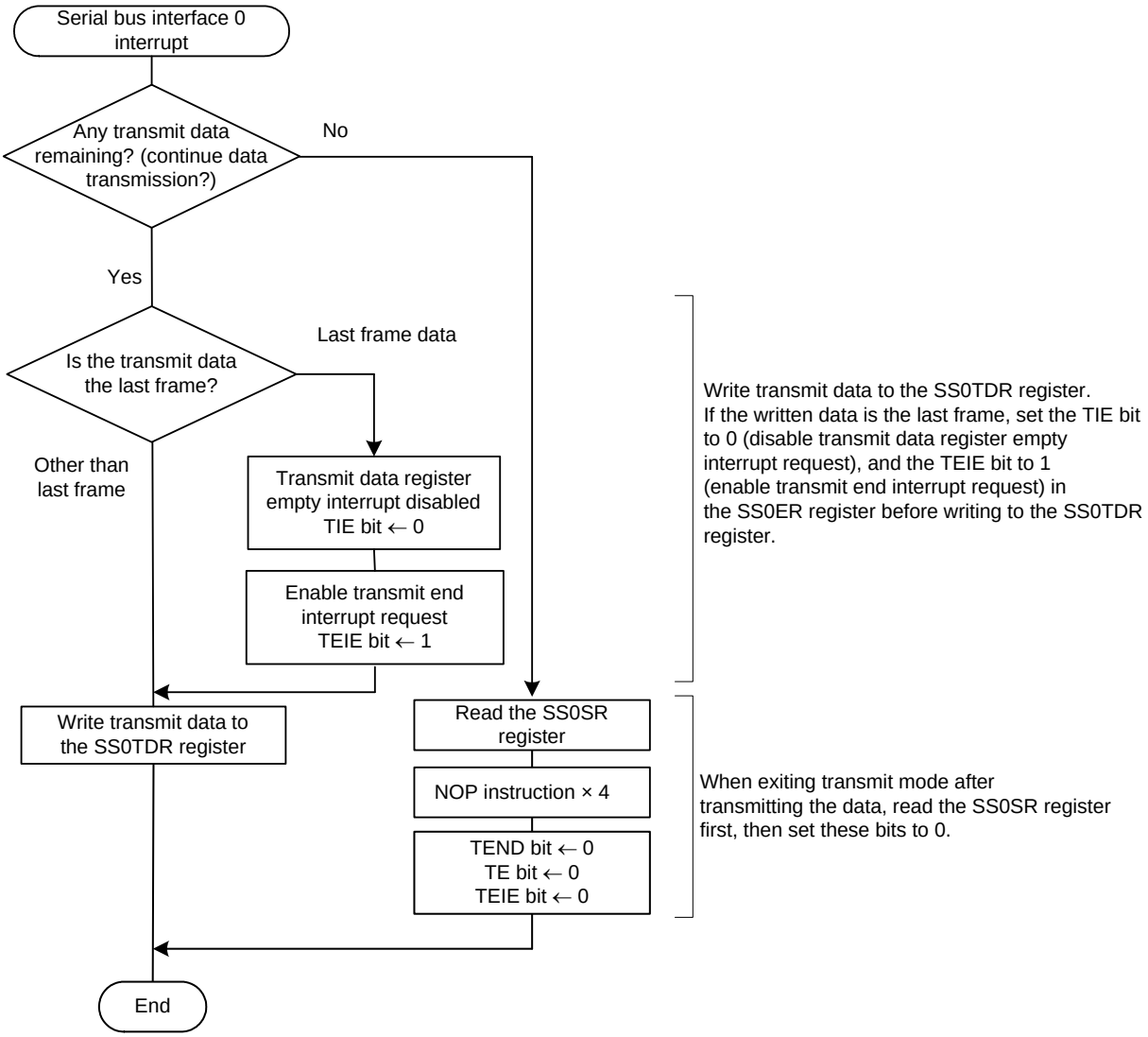


Figure 23.7 Example of Data Transmission Flow in Synchronous Serial Communication Mode

23.3.2.3 Data Reception

Figure 23.8 shows an example of receive operation in synchronous serial communication mode. During data reception, the serial bus interface operates as described below.

When it operates in master mode, an internally generated clock as transmit/receive clock is output from the SSCK0 pin. When it operates in slave mode, the transmit/receive clock is a clock input from the SSCK0 pin. In both cases, receive data is input synchronized with the transmit/receive clock.

In master mode, a dummy read to the SS0RDR register evokes the receive clock output to start data reception.

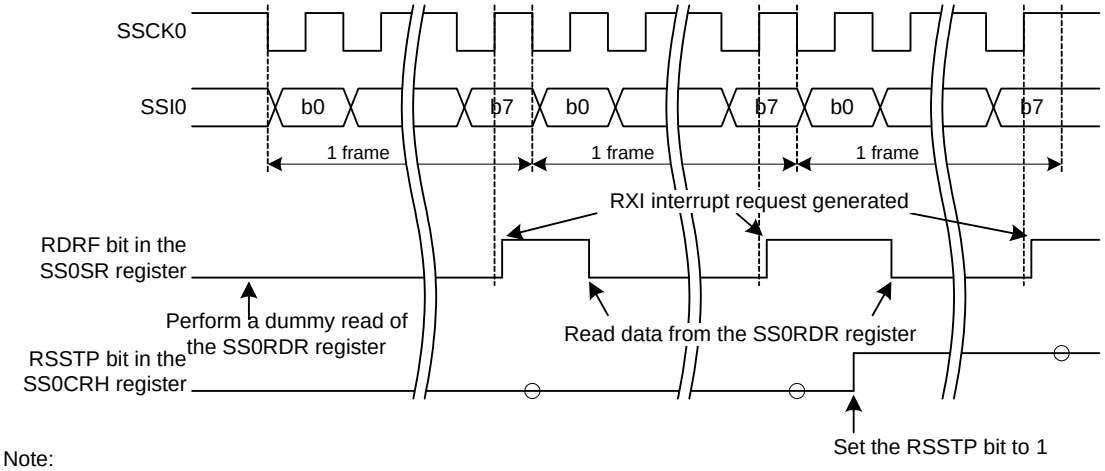
When the eighth bit of data is received, the RDRF bit in the SS0SR register becomes 1 (received data left in the SS0RDR register) and the received data is stored into the SS0RDR register. And, if the RIE bit in the SS0ER register is 1 (receive data register full interrupt/overrun error interrupt enabled), a receive data register full interrupt request (RXI) is generated. When the SS0RDR register is read, the RDRF bit automatically becomes 0 (no data left in the SS0RDR register).

To end the receive data operation in master mode, set the RSSTP bit in the SS0CRH register to 1 (receive operation ended after receiving the current frame) before completing reception of the last frame. Then the transmit/receive clock stops when the last frame reception has completed. When the clock stops, set the RE bit to 0 (reception disabled) and the RSSTP bit to 0 (receive operation continued after receiving the current frame) in the SS0ER register and read the data of the last frame. Note that if the SS0RDR register is read while the RE bit is 1, then the receive clock is output again.

If the eighth bit of the data is received when the RDRF bit is set to 1, the ORER bit in the SS0SR register becomes 1 (overrun error), and the receive operation stops. Note that data cannot be received while the ORER bit is 1. Set the ORER bit to 0 before resuming data reception.

Figure 23.9 shows an example of data reception flow in master mode in synchronous communication mode.

Receive operation example in synchronous serial communication mode



Note:
1. This figure is subject to the following conditions.
   The MSS bit in the SS0CRH register is 1 (master mode)
   The CPHS bit in the SS0MR register is 0 (change data at odd edges (load data at even edged))
   The CPOS bit in the SS0MR register is 0 (high when clock is stopped)
   The MLS bit in the SS0MR register is 1 (LSB first)
   Bits BS3 to BS0 are 1000b (8-bit length)

Figure 23.8 Receive Operation Example in Master Mode in Synchronous Serial Communication Mode

Receiving data using the receive data register full interrupt

When using the receive data register full interrupt, set the interrupt priority level of the SS0IC register, and set the RIE bit in the SS0ER register to 1 (enable receive data register full interrupt request). When the RE bit in the SS0ER register is set to 1 (enable data reception), and the SS0RDR register is dummy read, the receive operation starts. The serial bus interface 0 interrupt request is generated after 1 byte of data is received.

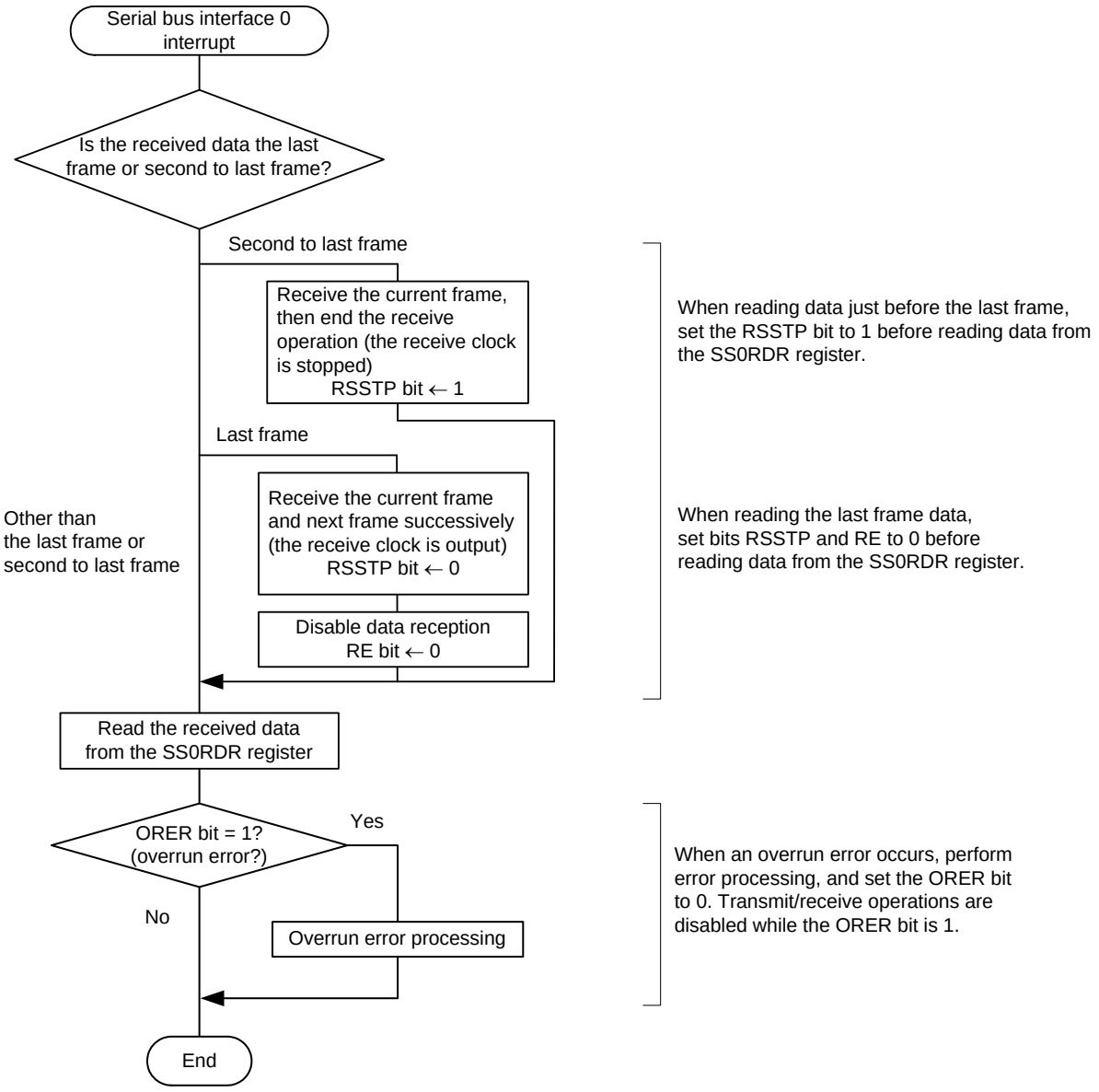


Figure 23.9 Example of Data Reception Flow While in Master Mode of the Synchronous Serial Communication Mode

23.3.2.4 Data Transmission/Reception

Data transmission/reception is a combined operation of data transmission and data reception described previously.

Data transmission/reception starts when data is written to the SS0TDR register, and ends when the eighth bit of data is transmitted while the TDRE bit is 1 (no data left in the SS0TDR register). The data transmit/receive operation stops when the ORER bit becomes 1 (overrun error) due to an error.

To switch the mode, from transmit mode (TE is 1 and RE is 0) or receive mode (TE is 0 and RE is 1) to transmit/receive mode (TE is 1 and RE is 1), set bits TE and RE to 0 first. Then make sure that the TEND bit is 0 (transmission continued), the RDRF bit is 0 (no data left in the SS0RDR register), and the ORER bit is 0 (no overrun error), and subsequently set bits TE and RE to 1 at the same time.

Figure 23.10 shows an example of data transmission/reception flow in synchronous serial communication mode.

Also, the SS0BR register can set the data transfer length between 8 to 16 bits.

Transmitting and receiving data using the receive data register full interrupt

Set the interrupt priority level of the SS0IC register, and set the RIE bit in the SS0ER register to 1 (enable receive data register full interrupt request).
When bits RE and TE in the SS0ER register are both set to 1 (enable data reception/transmission), and the first transmit data is set to the SS0TDR register, the serial bus interface 0 interrupt request is generated after 1 byte of data transmission/reception.

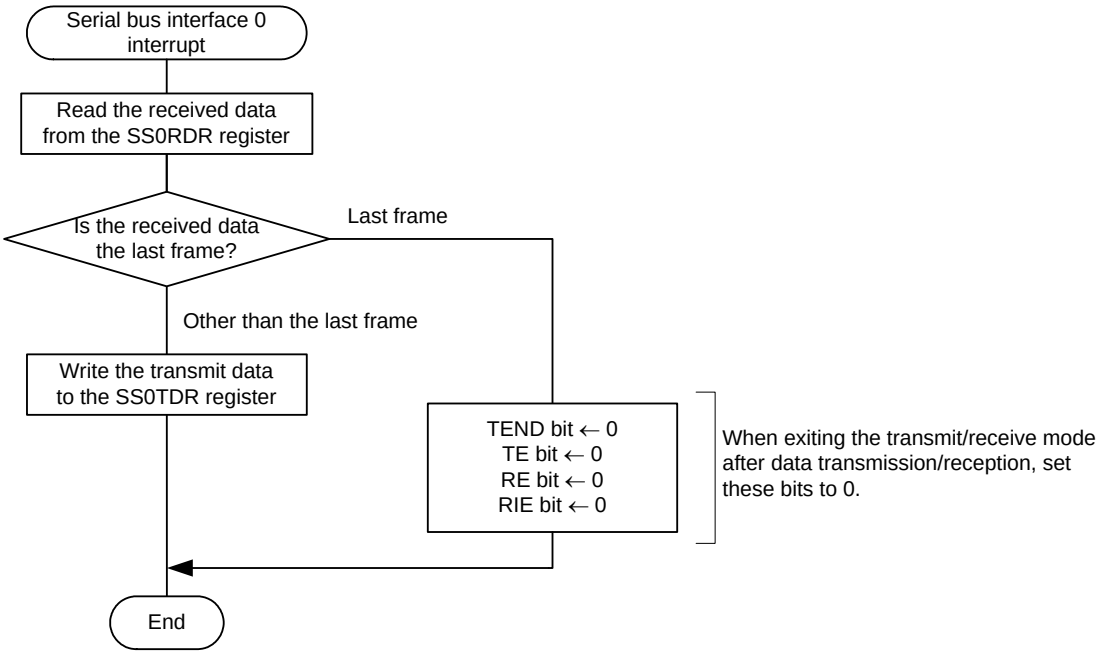


Figure 23.10 Example of Data Transmission/Reception Flow in Synchronous Communication Mode

23.3.3 4-Wire Serial Bus Mode

Table 23.4 4-Wire Serial Bus Mode Specifications

Item	Specification
Data format	Character length: 8 to 16 bits (variable length)
Master/slave mode	Selectable
I/O pins	SSCK0 (I/O): Clock I/O pin SSI0 (I): Data input pin SSO0 (O): Data output pin $\overline{SCS0}$ (I/O): Chip select I/O pin
Transmit/receive clocks	• When the MSS bit in the SS0CRH register is 0 (slave mode): External clock (input at SS0CK pin) • When the MSS bit in the SS0CRH register is 1 (master mode): Internal clock (output at SSCK0 pin) Selectable from f1/256, f1/128, f1/64, f1/32, f1/16, f1/8, f1/4
Transmit starting conditions	• TE bit in the SS0ER register is 1 (transmission enabled) • TDRE bit in the SS0SR register is 0 (unsent data left in the SS0RDR register) • ORER bit in the SS0SR register is 0 (no overrun error) • Clock input at the SSCK0 pin while the $\overline{SCS0}$ pin is low (applicable only when the MSS bit in the SS0CRH register is 0 (slave mode))
Receive starting conditions	• RE bit in the SS0ER register is 1 (reception enabled) • ORER bit in the SS0SR register is 0 (no overrun error) • Read operation to the SS0RDR register while TE bit in the SS0ER register is 0 (transmission disabled) (applicable only when the MSS bit in the SS0CRH register is 1 (master mode)) • Clock input at the SSCK0 pin (applicable only when the MSS bit in the SS0CRH register is 0 (slave mode))
Error detection	• Overrun error Overrun error occurs if, while the RDRF bit in the SS0SR register is 1 (received data left in the SS0RDR register), reception of next serial data has completed • Conflict error Conflict error occurs in either of the following two cases: • An attempt to start a serial communication while the $\overline{SCS0}$ pin is low (applicable when the MSS bit in the SS0CRH register is 1 (master mode)) • The $\overline{SCS0}$ pin becomes high during the data transfer (applicable when the MSS bit in the SS0CRH register is 0 (slave mode))
Interrupt request sources	Five interrupt request sources (transmit end, transmit data register empty, receive data register full, overrun error, and conflict error) (1)
Selectable functions	• Programmable bit order MSB first or LSB first, selectable with the MLS bit in the SS0MR register • SSCK0 clock polarity Low or high when clock is stopped, selectable with the CPOS bit in the SS0MR register • SSCK0 clock phase Combination of odd and even edges for changing and loading data, selectable with the CPHS bit in the SS0MR register

Note:
1. Each channel has its own interrupt vector table.

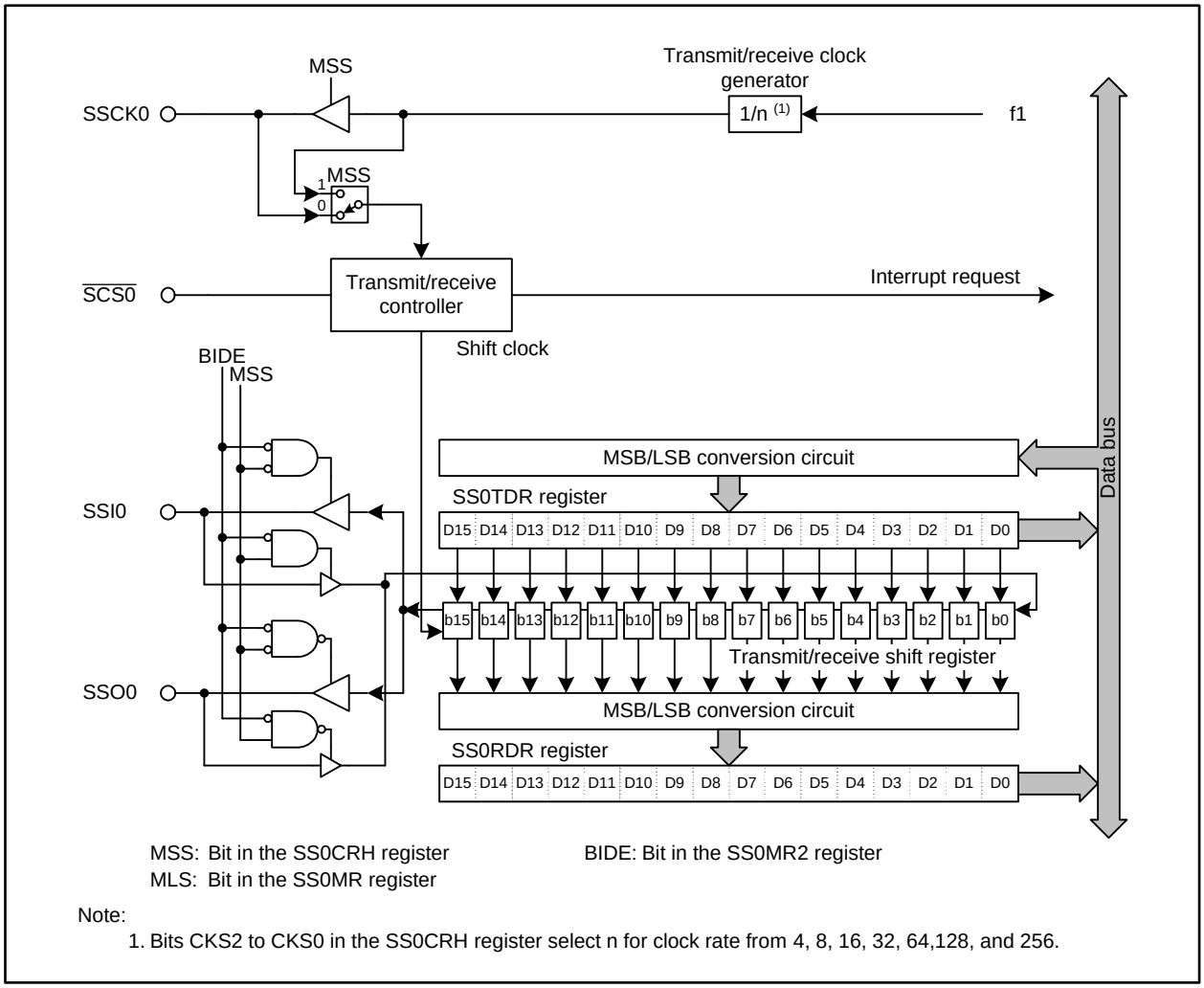


Figure 23.11 Block Diagram of 4-wire Serial Bus Mode

In 4-wire serial bus mode, the serial bus interface operates serial communication via four logic signal lines: clock line, data input line, data output line, and chip select line. This mode also contains a bidirectional mode, in which a single pin is used for the data input line and the data output line.

The data input line and data output line share the SSI0 pin and SSO0 pin. The combined setting of the MSS bit in the SS0CRH register and the BIDE bit in the SS0MR2 register determines which line (input or output) is assigned to which pin (the SSI0 pin or the SSO0 pin). Refer to 23.3.1.6 “Data I/O Pin and Transmit/Receive Shift Register” for more details. In this mode, the clock polarity and phase for transmit/receive data can be configured by setting bits CPOS and CPHS in the SS0MR register. Refer to 23.3.1.2 “Association between Transmit/Receive Clock Polarity, Phase and Data” for more details.

The chip select line functions as output pin in master mode and as input pin in slave mode. By setting bits CSS1 to CSS0 in the SS0MR2 register to 10b or 11b in master mode, the $\overline{\text{SCS0}}$ pin can be auto-controlled as an output pin, or a programmable I/O port can be assigned as the chip select pin. In slave mode, the $\overline{\text{SCS0}}$ pin is assigned as input pin by setting bits CSS1 and CSS0 in the SS0MR2 register to 01b.

In 4-wire serial bus mode, normally, serial communication is performed with the MSB first (the MSL bit in the SS0MR register is set to 0).

In 4-wire serial bus mode, the function of I/O pins varies with the setting combination of the MSS bit in the SS0CRH register, bits RE and TE in the SS0ER register. The SSCK0 pin functions as output in master mode. This pin is used for input when the slave mode is selected.

Table 23.5 Communication Modes and I/O Pins

Communication Mode	Bit Setting					Pin State		
	SSUMS	BIDE	MSS	TE	RE	SSI0	SSO0	SSCK0
4-wire serial bus mode (in standard mode)	1	0	0 (slave)	0	1	– (1)	Input	Input
				1	0	Output	– (1)	
					1	Output	Input	
			1 (master)	0	1	Input	– (1)	Output
				1	0	– (1)	Output	
					1	Input	Output	
4-wire bus communication mode (in bidirectional mode) (2)	1	1	0 (slave)	0	1	– (1)	Input	Input
				1	0	– (1)	Output	
			1 (master)	0	1	– (1)	Input	Output
				1	0	– (1)	Output	

Notes:
1. This pin can be used as a programmable I/O port.
2. Do not set bits TE and RE to 1 in 4-wire bus communication mode (in bidirectional mode) simultaneously.

SSUMS and BIDE: Bits in the SS0MR2 register
MSS: Bit in the SS0CRH register
TE and RE: Bits in the SS0ER register

23.3.3.1 Initialization of 4-wire Serial Bus Mode

Figure 23.12 shows the initialization flow of 4-wire serial bus mode. Initialize the TE bit in the SS0ER register to 0 (transmission disabled) and RE bit in the SS0ER register to 0 (reception disabled) before the data transmission/reception.

To change communication mode or the communication data format, set bits TE and RE to 0 in advance. Note that flags RDRF and ORER and the SS0RDR register are unaffected even if the RE bit is set to 0. Refer to 23.5.1 “SS0SR register” for notes when writing to the SS0SR register.

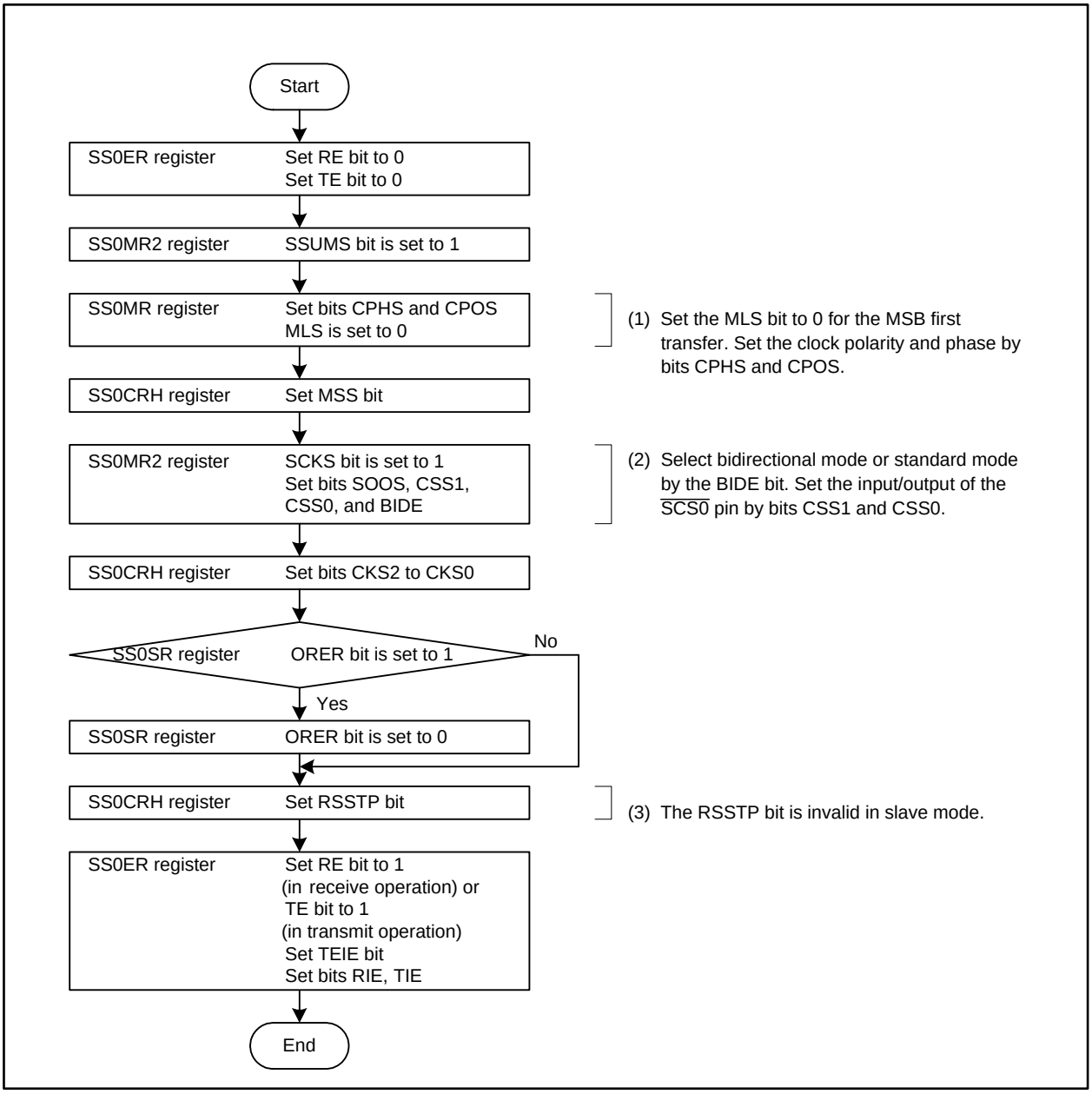


Figure 23.12 Initialization Flow in 4-wire Serial Bus Mode

23.3.3.2 Data Transmission

Figure 23.13 shows an example of transmit operation in 4-wire serial bus mode. During data transmission, the serial bus interface operates as described below.

When it operates in master mode, an internally generated clock as transmit/receive clock is output from the SSCK0 pin. When it is in slave mode, the transmit/receive clock is a clock input from the SSCK0 pin while the $\overline{SCS0}$ pin is low. In both cases, transmit data is output synchronized with the transmit/receive clock.

After setting the TE bit in the SS0ER register to 1 (transmission enabled), if transmit data is written to the SS0TDR register, the TDRE bit in the SS0SR register automatically becomes 0 (unsent data left in the SS0TDR register), and data in the SS0TDR register is transferred to the transmit/receive shift register. Then the TDRE bit becomes 1 (no data left in the SS0TDR register) and data transmission starts. And, if the TIE bit in the SS0ER register is 1 (transmit data register empty interrupt enabled), a transmit data empty interrupt request (TXI) is generated.

When the TDRE bit is 0, after transmitting one frame of data, the data is transferred from the SS0TDR register to the transmit/receive shift register to start the next data transmission. When the TDRE bit is 1, after transmitting the last bit of data, the TEND bit in the SS0SR register becomes 1 (transmission has completed). And, if the TEIE bit in the SS0ER register is 1 (transmit end interrupt enabled), a transmit end interrupt request (TEI) is generated.

After the data transmission has completed, both the SSCK0 pin and the $\overline{SCS0}$ pin become high. To continue the data transmission with the $\overline{SCS0}$ pin low, write the data to be transmitted next to the SS0TDR register before the last bit is transmitted.

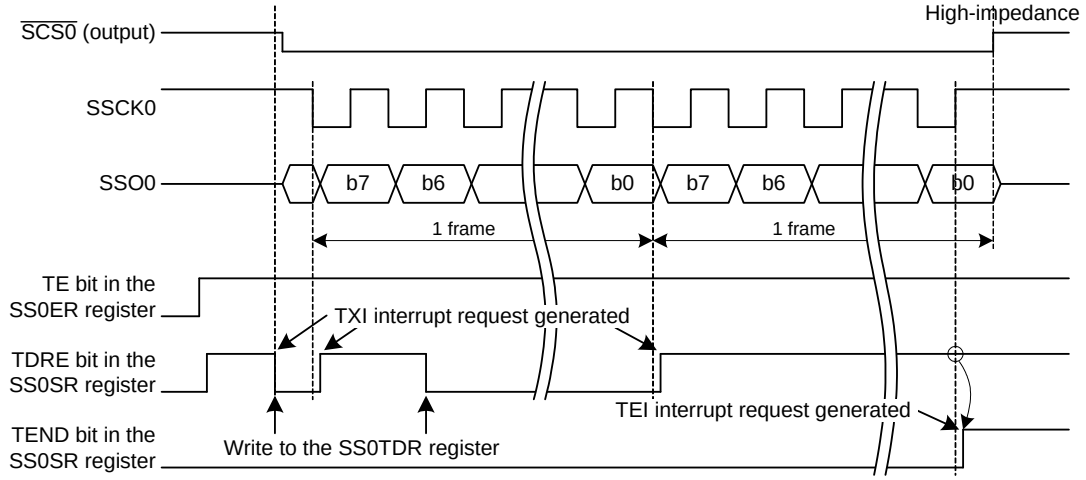
Note that data cannot be transmitted while the ORER bit in the SS0SR register is 1 (overrun error). Make sure that the ORER bit is set to 0 before data transmission.

In contrast to synchronous serial communication mode, the $\overline{SCS0}$ pin is used in 4-wire serial bus mode. With 4-wire serial bus mode, when in master mode, the SSO0 pin is high-impedance while the output level at the $\overline{SCS0}$ pin is high. In slave mode, the SSIi pin is high-impedance while the input level at the $\overline{SCS0}$ pin is high.

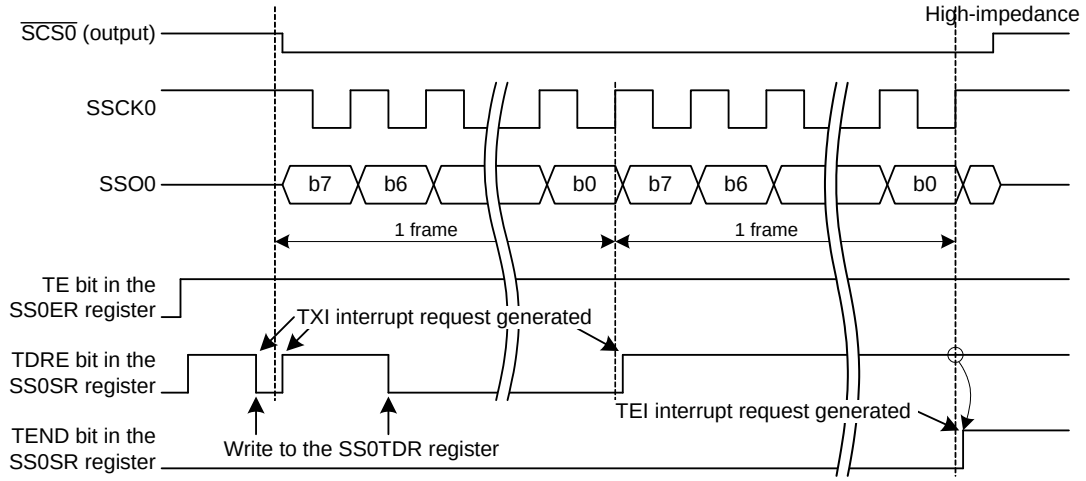
For sample flowchart of data transmission, refer to Figure 23.7.

Also, the SS0BR register can set the data transfer length between bits 8 to 16.

Case 1 CPHS is 0 (change data at odd edges and load data at even edges)



Case 2 CPHS is 1 (change data at even edges and load data at odd edges)



CPOS: Bit in the SS0MR register

Note:

1. The above assumes the following:
   The MSS bit in the SS0CRH register is 1 (master mode)
   The CPOS bit in the SS0MR register is 0 (high when clock is stopped)
   The MLS bit in the SS0MR register is 0 (MSB first)
   Bits BC3 to BC0 are 1000b (8-bit length)
   The CSOS bit in the SS0MR2 is 1 ($\overline{SCSi}$ pin is N-channel open drain output)

Figure 23.13 Transmit Operation Example in 4-wire Serial Bus Mode

23.3.3.3 Data Reception

Figure 23.14 shows an example of receive operation in 4-wire serial bus mode. During data reception, the serial bus interface operates as described below.

When it operates in master mode, an internally generated clock as transmit/receive clock is output from the SSCK0 pin. When it operates in slave mode, the transmit/receive clock is a clock input from the SSCKi pin while the $\overline{SCS0}$ pin is low. In both cases, receive data is input synchronized with the transmit/receive clock.

In master mode, a dummy read to the SS0RDR register, after setting the TE bit in the SS0ER register to 0 and exiting from transmit mode, evokes the receive clock output to start data reception.

When the data of preset bits is received, the RDRF bit in the SS0SR register becomes 1 (received data left in the SS0RDR register) and the received data is stored into the SS0RDR register. And, if the RIE bit in the SS0ER register is 1 (receive data register full interrupt/overrun error interrupt enabled), a receive data register full interrupt request (RXI) is generated. When the SS0RDR register is read, the RDRF bit automatically becomes 0 (no data left in the SS0RDR register).

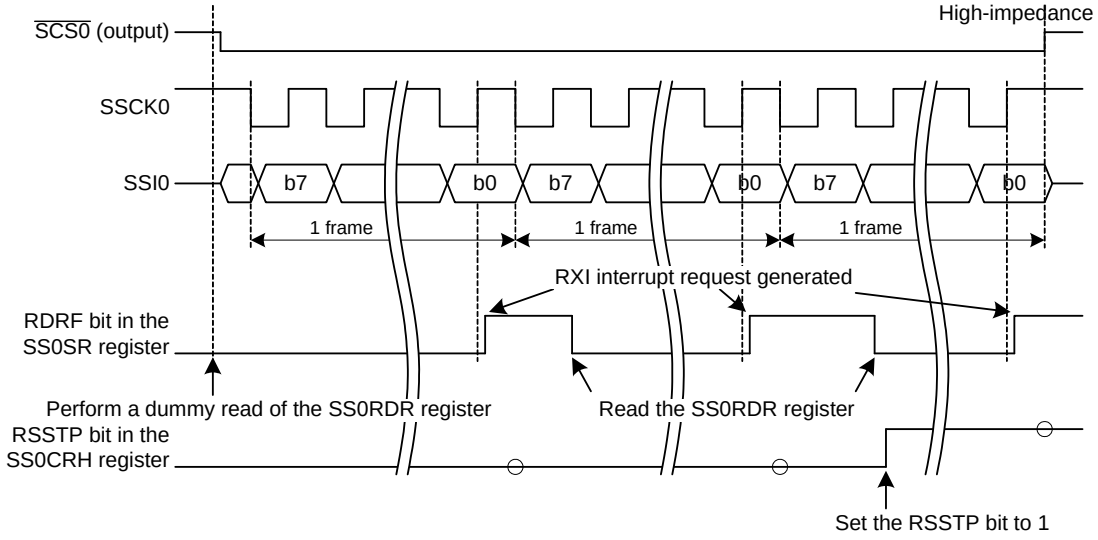
To end the receive data operation in master mode, set the RSSTP bit in the SS0CRH register to 1 (receive operation ended after receiving the current frame) before reading the data of the second last frame from the SS0RDR register. Then the transmit/receive clock stops when the last frame reception has completed. When the clock stops, set the RE bit in the SS0ER register to 0 (reception disabled) and the RSSTP bit to 0 (receive operation continued after receiving the current frame) and read the data of the last frame. Note that if the SS0RDR register is read while the RE bit is 1 (reception enabled), then the receive clock is output again.

If the last bit of the data is received with the RDRF bit set to 1, the ORER bit in the SS0SR register becomes 1 (overrun error), and the receive operation stops. Note that data cannot be received while the ORER bit is 1. Make sure that the ORER bit is set to 0 before resuming data reception.

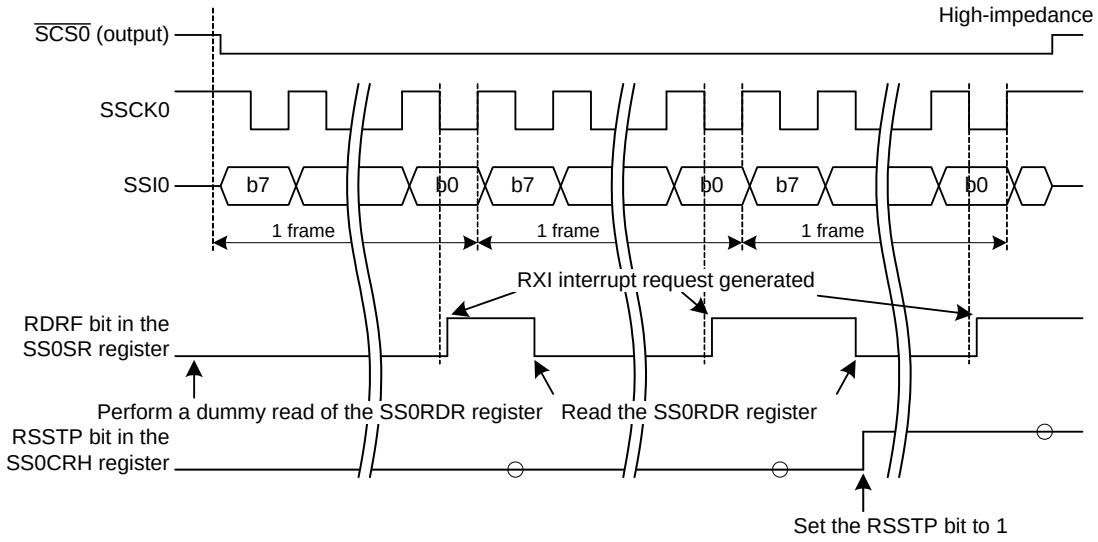
For sample flowchart of data reception, refer to Figure 23.9.

Also, the SS0BR register can set the data transfer length between bits 8 to 16.

Case 1 CPHS is 0 (change data at odd edges and load data at even edges)



Case 2 CPHS is 1 (change data at even edges and load data at odd edges)



CPOS: Bit in the SS0MR register

Note:

1. The above assumes the following:
   - The MSS bit in the SS0CRH register is 1 (master mode)
   - The CPOS bit in the SS0MR register is 0 (high when clock is stopped)
   - The MLS bit in the SS0MR register is 0 (MSB first)
   - Bits BC3 to BC0 in the SS0MR register is 1000b (8-bit length)
   - The CSOS bit in the SS0MR2 register is 1 ($\overline{SCS0}$ is N-channel open drain output)

Figure 23.14 Receive Operation Example in 4-wire Serial Bus Mode

23.3.3.4 $\overline{\text{SCS0}}$ Pin Control and Arbitration

In 4-wire serial bus mode, when bits CSS1 and CSS0 are set to 10b or 11b (functions as $\overline{\text{SCS0}}$ output pin), and the MSS bit in the SS0CRH register is 1 (master mode), then an arbitration is performed by monitoring the $\overline{\text{SCS0}}$ pin before starting serial data transmission. When the serial bus interface detects that the synchronized internal $\overline{\text{SCS0}}$ signal level drops to low before data transmission, the CE bit in the SS0SR register becomes 1 (conflict error) and the MSS bit automatically becomes 0 (slave mode). Figure 23.15 shows the arbitration timing.

Note that the serial bus interface can no longer continue transmit operation while the CE bit is 1. To start data transmission, confirm the CE bit is 1 and then set this bit to 0 (no conflict error).

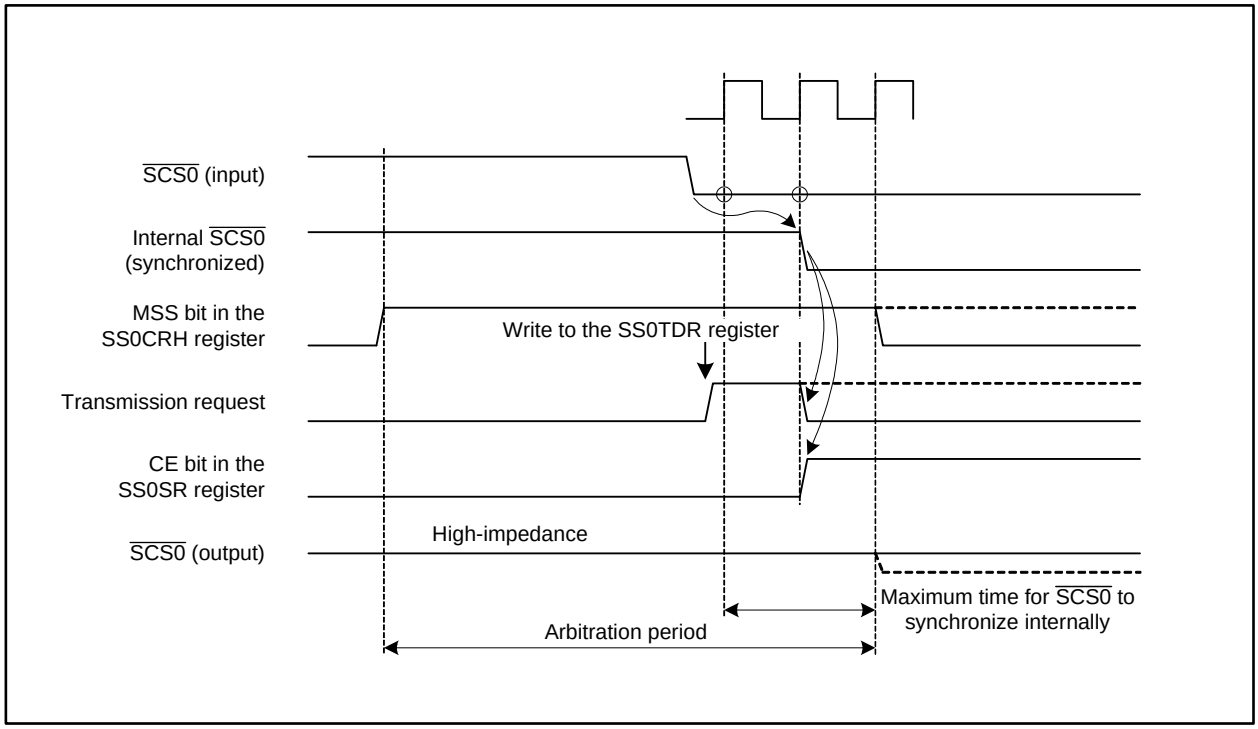


Figure 23.15 Arbitration Check Timing

23.4 Interrupts

In synchronous serial communication mode, there are four interrupt request sources: transmit data register empty, transmit end, receive data register full and overrun error. In 4-wire serial bus mode, there is one interrupt request source: conflict error. Since all these interrupt request sources are assigned to an interrupt vector table, they should be identified by flags in the interrupt handler.
Table 23.6 lists the serial bus interface interrupt request sources.

Table 23.6 Interrupt Request Sources in Synchronous Serial Communication Mode and 4-wire Serial Bus Mode

Interrupt Request Source		Generating Condition for Interrupt Requests
Transmit data register empty	TXI	TIE = 1 and TDRE = 1
Transmit end	TEI	TEIE = 1 and TEND = 1
Receive data register full	RXI	RIE = 1 and RDRF = 1
Overrun error	OEI	RIE = 1 and ORER = 1
Conflict error (1)	CEI	CEIE = 1 and CE = 1

Note:
1. The conflict error occurs only in 4-wire serial bus mode.
CEIE, RIE, TEIE, and TIE: Bits in the SS0ER register
CE, ORER, RDRF, TEND, and TDRE: Bits in the SS0SR register

When one or more generating conditions for interrupt requests in Table 23.6 is/are met, a serial bus interface 0 interrupt request is generated. Set the corresponding interrupt source(s) to 0 by the interrupt handler.
However, bits TDRE (transmit data register empty) and TEND (transmit end) automatically become 0 when the next transmit data is written to the SS0TDR register. The RDRF bit (receive data register full) automatically becomes 0 when the SS0RDR register is read.
Note that if no data is in transmission, the TDRE bit which became 0 as mentioned above is set back to 1 (no data left in the SS0TDR register) since the written data is immediately transferred to the transmit/receive shift register. And, if the TDRE bit is set to 0 (unsent data left in SS0TDR register) by a program, it may cause the transmission of an additional data frame.

Table 23.7 Serial Bus Interface Related Register

Address	Register Name	Register Symbol	Reset Value
0042h	Serial Bus Interface 0 Interrupt Control Register	SS0IC	XX00 X000b

The serial bus interface shares interrupt vectors and interrupt control registers with other peripheral functions. When using the serial bus interface 0 interrupt, set the IFSR44 bit in the IFSR4A register to 1 (serial bus interface 0).

The IR bit in the SS0IC register operates differently from other IR bits. Refer to 12.2.3 “Interrupt Control Register 2” for more details.

23.5 Notes on Serial Bus Interface

23.5.1 SS0SR register

To write to the SS0SR register, perform the following:

- Use the MOV instruction.
- Read the register once, insert four or more NOP instructions, then write to the register.
- Write 1 to bits which are not set to 0 (bits to which 1 is written will not be changed).

Example of setting the ORER bit (b2) in the SS0SR register to 0

```
MOV.B SS0SR, MEM          ;Read the SS0SR register
NOP                       ;Insert four or more NOP instructions
NOP
NOP
NOP
MOV.B #11100001b, SS0SR   ;Write 0 to b2.
                          ;Write 1 to b7, b6, b5 and b0 since they do not change.
                          ;b4, b3 and b1 are not register bits. Write 0 to these bits.
```

24. LIN Module

The M16C/5M Group implements a LIN (Local Interconnect Network) module, compliant with LIN Specification Package Revisions 1.3, 2.0, and 2.1, which transmits and receives frames, and judges errors automatically. The LIN module has a master controller with one channel.
Table 24.1 and Table 24.2 list the LIN module specifications. Figure 24.1 shows the LIN module block diagram.

Table 24.1 LIN Module Specifications (1/2)

Item	Specifications
Protocols	LIN Specification Package Revisions 1.3, 2.0, and 2.1
Channel	1 channel (LIN master)
Variable frame composition	Break: 13 to 28 Tbits Break delimiter: 1 to 4 Tbits Interbyte space (header): 0 to 7 Tbits (space between Sync field and ID field) (1) Response space: 0 to 7 Tbits (1) Interbyte space: 0 to 3 Tbits (space between bytes in response space) Wake-up: 1 to 16 Tbits
Checksum	Automatic calculation in both transmission and reception Classic checksum or enhanced checksum selectable (changeable at each frame)
Data byte(s) in response field	Variable from 0 to 8
Frame transmission mode	Non-frame separate mode or frame separate mode selectable • In non-frame separate mode, the header and response are both transmitted by a single transmission start command. • In frame separate mode, the header and response are transmitted separately by their respective transmission start commands.
Wake-up transmission/reception	Available in LIN wake-up mode • Wake-up transmission • Wake-up reception • Input signal Low time counting • Input signal Low detection
Operational status	• Frame/wake-up transmit completion • Header transmit completion • Frame/wake-up receive completion (2) • Data 1 receive completion • Error detection • Operational modes (LIN reset mode, LIN wake-up mode, LIN operation mode, and LIN self-test mode)
Error status	• Bit error • Checksum error • Frame timeout error • Physical bus error • Framing error
Baud rate	Selectable LIN-specified value generated by the baud rate generator

Notes:
1. The interbyte space (header) has the same value as the response space since the both spaces are set in the same register.
2. The input signal Low time counting is used on wake-up reception.

Table 24.2 LIN Module Specifications (2/2)

Item	Specifications
Test mode	Self-test mode for user evaluation
Interrupt function	• Frame/wake-up transmit completion • Frame/wake-up receive completion (1) • Error detection • LIN0 Low detection (input signal Low detection)

Note:
1. The input signal Low time counting is used on wake-up reception.

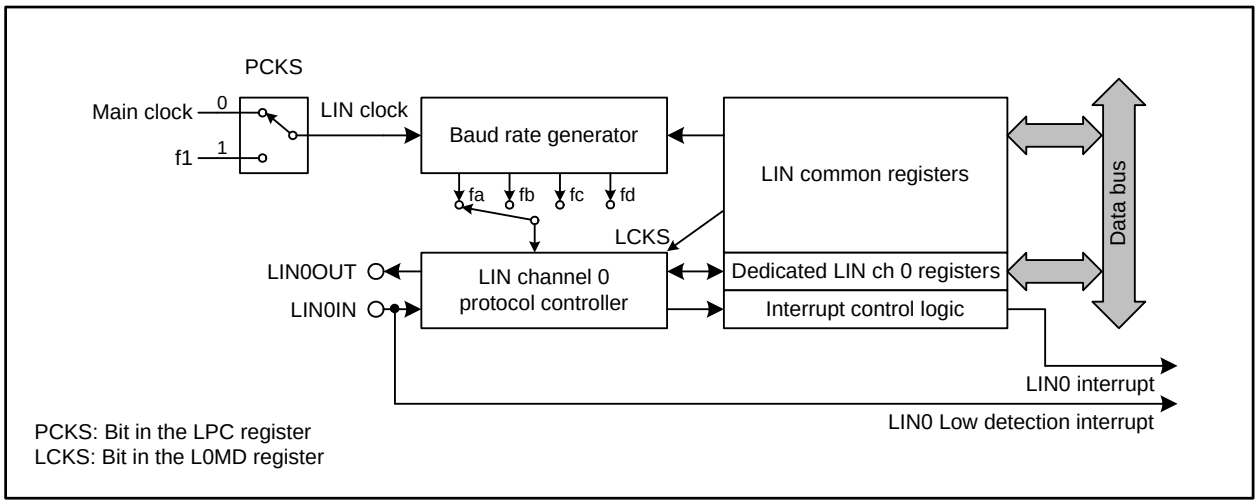


Figure 24.1 LIN Module Block Diagram

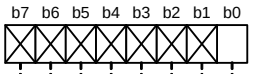
- LIN0OUT, LIN0IN: LIN I/O pins
- Baud rate generator: Generates a communication clock for LIN
- LIN common registers, dedicated LIN channel 0 registers: Registers for the LIN module
- Interrupt control logic: Controls the interrupt request (LIN0 interrupt) generated by the LIN module

24.1 LIN Module Associated Registers

Figure 24.2 to 24.21 show registers associated with the LIN module.

24.1.1 LIN Wake-up Baud Rate Select Register (LWBR)

LIN Wake-up Baud Rate Select Register



Symbol	Address	Reset Value
LWBR	0161h	00h

Bit Symbol	Bit Name	Function	RW
LWBR0	Wake-up Baud Rate Select Bit	0: When LIN 1.3 used 1: When LIN 2.0 and 2.1 used	RW
— (b7-b1)	No register bits. If necessary, set to 0. The read value is 0.		—

Figure 24.2 LWBR Register

Set this register in LIN reset mode.

24.1.1.1 LWBR0 Bit

When LIN Specification Package Revision 1.3 is used, set the LWBR0 bit in the LWBR register to 0. This setting allows the input signal Low time to be measured when it is 2.5 Tbits or more.
When LIN Specification Package Revisions 2.0 and 2.1 are used, set the LWBR0 bit to 1. By setting this bit to 1, fa is selected for the LIN system clock (fLIN) regardless of what is set to the LCKS bit in the L0MD register during LIN wake-up mode (the LCKS bit does not change). The input signal Low time can be measured when it is 2.5 Tbits or more.

24.1.2 LIN Baud Rate Prescaler 0 Register (LBRP0)

LIN Baud Rate Prescaler 0 Register

b7 b0

Symbol	Address	Reset Value
LBRP0	0162h	00h

Function	Setting Range	RW
The LIN clock source is divided by (N + 1) (N = setting value (0 to 255)) by the baud rate prescaler	00h to FFh	RW

Figure 24.3 LBRP0 Register

Set this register in LIN reset mode.

24.1.3 LIN Baud Rate Prescaler 1 Register (LBRP1)

LIN Baud Rate Prescaler 1 Register

b7 b0

Symbol	Address	Reset Value
LBRP1	0163h	00h

Function	Setting Range	RW
The LIN clock source is divided by (M + 1) (M = setting value (0 to 255)) by the baud rate prescaler	00h to FFh	RW

Figure 24.4 LBRP1 Register

Set this register in LIN reset mode.

24.1.4 LIN Self-test Control Register (LSTC)

LIN Self-test Control Register

b7 b0

Symbol	Address	Reset Value
LSTC	0164h	00h

Function	RW
When A7h, 58h, and 01h are consecutively written, the LIN module enters LIN self-test mode. When reading bits b7 to b1, the read values are 0. When reading b0, see the figure about the LSTM bit below.	RW

b7 b0

Bit Symbol	Bit Name	Function	RW
LSTM	Self-test Mode Bit	0: Mode other than LIN self-test mode 1: LIN self-test mode	RW

Figure 24.5 LSTC Register

Set this register in LIN reset mode.
This register is used to release the protection of LIN self-test mode.
When A7h, 58h, and 01h are consecutively written to this register, the LIN module enters LIN self-test mode.
If consecutive writing is successful and the LIN module enters LIN self-test mode, the LSTM bit becomes 1.
Do not perform another write operation while consecutive writing is in progress.
For details on transition to LIN self-test mode, refer to 24.11 “LIN Self-test Mode”.

24.1.4.1 LSTM Bit

This bit becomes 1 when the LIN module enters LIN self-test mode.
For details on exiting LIN self-test mode, refer to 24.11 “LIN Self-test Mode”.
Other than consecutively writing A7h, 58h, and 01h to the LSTC register, writing 1 does not change the value of this bit.

24.1.5 LIN Port Clock Control Register (LPC)

LIN Port Clock Control Register

b7	b6	b5	b4	b3	b2	b1	b0
						0	

Symbol	Address	Reset Value
LPC	0165h	00h

Bit Symbol	Bit Name	Function	RW
PCKS	LIN Clock Source Select Bit	0: Main clock 1: f1	RW
— (b1)	Reserved	Set to 0.	RW
LPE	LIN Port Enable Bit	0: Function as I/O port 1: Function as LIN I/O	RW
— (b7-b3)	No register bits. If necessary, set to 0. The read value is 0.		—

Figure 24.6 LPC Register

Set this register in LIN reset mode.

24.1.5.1 PCKS Bit

Set this bit to select the LIN clock source to be input to the baud rate generator.
When this bit is set to 0, the main clock is input to the baud rate generator.
When this bit is set to 1, f1 is input to the baud rate generator.
To set this bit to 1, set the CM21 bit to 0 (main clock or PLL clock).

24.1.5.2 LPE Bit

When the LPE bit is set to 1, the functions of the LIN I/O pins (LIN0OUT and LIN0IN) are enabled.
Set this bit to 1 to use the LIN module.
To set this bit to 1, set the port direction bit corresponding to the LIN0IN pin to 0 (input).
When the LPE bit is set to 0, the functions of the port I/O pins are enabled.

24.1.6 LIN0 Mode Register (L0MD)

LIN0 Mode Register

b7	b6	b5	b4	b3	b2	b1	b0
×	×	×	×			×	0

Symbol	Address	Reset Value
L0MD	0168h	00h

Bit Symbol	Bit Name	Function	RW
— (b0)	Reserved	Set to 0.	RW
— (b1)	No register bit. If necessary, set to 0. The read value is 0.		—
LCKS	LIN System Clock Select Bit	b3 b2 0 0 : fa 0 1 : fb 1 0 : fc 1 1 : fd	RW
— (b7-b4)	No register bits. If necessary, set to 0. The read value is 0.		—

Figure 24.7 L0MD Register

Set this register in LIN reset mode.

24.1.6.1 LCKS Bit

Set this bit to select the clock to be input to the protocol controller.
When this bit is set to 00b, fa (clock generated by baud prescaler 0) is input to the protocol controller.
When this bit is set to 01b, fb (clock generated by baud prescaler 0 divided by 2) is input to the protocol controller.
When this bit is set to 10b, fc (clock generated by baud prescaler 0 divided by 8) is input to the protocol controller.
When this bit is set to 11b, fd (clock generated by baud prescaler 1 divided by 2) is input to the protocol controller.
When the LWBR0 bit in the LWBR register is 1 (when LIN 2.0 and 2.1 used), and the L0MST register is 01h (LIN0 wake-up mode), fa is input to the protocol controller regardless of the setting in this bit (the LCKS bit does not change).

24.1.7 LIN0 Break Field Setting Register (L0BRK)

LIN0 Break Field Setting Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	Reset Value
L0BRK	0169h	00h

Bit Symbol	Bit Name	Function	RW
BLT	Break Transmission Setting Bit	b3 b2 b1 b0 0 0 0 0 : 13 Tbits 0 0 0 1 : 14 Tbits 0 0 1 0 : 15 Tbits : : 1 1 1 0 : 27 Tbits 1 1 1 1 : 28 Tbits	RW
BDT	Break Delimiter Transmission Setting Bit	b5 b4 0 0 : 1 Tbit 0 1 : 2 Tbits 1 0 : 3 Tbits 1 1 : 4 Tbits	RW
— (b7-b6)	No register bits. If necessary, set to 0. The read value is 0.		—

Figure 24.8 L0BRK Register

Set this register in LIN reset mode.
The length of one frame may exceed frame timeout time depending on the combination of setting values. Make sure to set appropriate values.

24.1.7.1 BLT Bit

This bit sets the (Low) time pulse width for break in the transmit frame header.
A value from 13 Tbits to 28 Tbits can be set.

24.1.7.2 BDT Bit

This bit sets the (High) time pulse width for break delimiter in the transmit frame header.
A value from 1 Tbit to 4 Tbits can be set.

24.1.8 LIN0 Space Width Setting Register (L0SPC)

LIN0 Space Setting Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	Reset Value
L0SPC	016Ah	00h

Bit Symbol	Bit Name	Function	RW
IBSH	Interbyte Space (Header)/ Response Space Setting Bit	b2 b1 b0 0 0 0 : 0 Tbits 0 0 1 : 1 Tbit 0 1 0 : 2 Tbits 0 1 1 : 3 Tbits 1 0 0 : 4 Tbits 1 0 1 : 5 Tbits 1 1 0 : 6 Tbits 1 1 1 : 7 Tbits	RW
— (b3)	No register bit. If necessary, set to 0. The read value is 0.		—
IBS	Interbyte Space Setting Bit	b5 b4 0 0 : 0 Tbits 0 1 : 1 Tbit 1 0 : 2 Tbits 1 1 : 3 Tbits	RW
— (b7-b6)	No register bits. If necessary, set to 0. The read value is 0.		—

Figure 24.9 L0SPC Register

Set this register in LIN reset mode.
This register is enabled only for transmission (header and response). In response reception, this register is disabled.
The length of one frame may exceed frame timeout time depending on the combination of setting values. Make sure to set appropriate values.

24.1.8.1 IBSH Bit

This bit sets the space width of the interbyte space (Header) and response space required for the transmit frame header.
A value from 0 Tbits to 7 Tbits can be set.
The values of the interbyte space (Header) and response space are the same.

24.1.8.2 IBS Bit

This bit sets the space width of the interbyte space required for the transmit frame response.
A value from 0 Tbits to 3 Tbits can be set.

24.1.9 LIN0 Wake-up Setting Register (L0WUP)

LIN0 Wake-up Setting Register

b7	b6	b5	b4	b3	b2	b1	b0
							0

Symbol	Address	Reset Value
L0WUP	016Bh	00h

Bit Symbol	Bit Name	Function	RW
— (b0)	Reserved	Set to 0.	RW
— (b3-b1)	No register bits. If necessary, set to 0. The read value is 0.		—
WUTL	Wake-up Transmission Low Time Pulse Width Setting Bit	b7 b6 b5 b4 0 0 0 0 : 1 Tbit 0 0 0 1 : 2 Tbits 0 0 1 0 : 3 Tbits 0 0 1 1 : 4 Tbits : : 1 1 0 0 : 13 Tbits 1 1 0 1 : 14 Tbits 1 1 1 0 : 15 Tbits 1 1 1 1 : 16 Tbits	RW

Figure 24.10 L0WUP Register

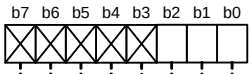
Set this register in LIN reset mode.

24.1.9.1 WUTL Bit

This bit sets the Low time pulse width of wake-up transmission.
A value from 1 Tbit to 16 Tbits can be set.
When the LWBR0 bit in the LWBR register is 1 (when LIN 2.0 and 2.1 used), fa is selected for LIN system clock (fLIN) regardless of what is set to the LCKS bit in the L0MD register (LCKS bit does not change).

24.1.10 LIN0 Interrupt Enable Register (L0IE)

LIN0 Interrupt Enable Register



Symbol	Address	Reset Value
L0IE	016Ch	00h

Bit Symbol	Bit Name	Function	RW
FTCIE	Frame/Wake-up Transmit Completion Interrupt Enable Bit	0: Frame/wake-up transmit completion interrupt disabled 1: Frame/wake-up transmit completion interrupt enabled	RW
FRCIE	Frame/Wake-up Receive Completion Interrupt Enable Bit	0: Frame/wake-up receive completion interrupt disabled 1: Frame/wake-up receive completion interrupt enabled	RW
ERRIE	Error Detection Interrupt Enable Bit	0: Error detection interrupt disabled 1: Error detection interrupt enabled	RW
— (b7-b3)	No register bits. If necessary, set to 0. The read value is 0.		—

Figure 24.11 L0IE Register

Set this register in LIN reset mode.

24.1.10.1 FTCIE Bit

This bit enables or disables an interrupt when a frame transmission or wake-up frame transmission is completed.
When this bit is set to 0, no LIN0 interrupt is generated when the FTC bit in the L0ST register becomes 1 (frame or wake-up transmission has been completed).
When this bit is set to 1, a LIN0 interrupt is generated when the FTC bit becomes 1.

24.1.10.2 FRCIE Bit

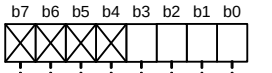
This bit enables or disables an interrupt when a frame reception or wake-up frame reception (input signal Low time counting) is completed.
When this bit is set to 0, no LIN0 interrupt is generated when the FRC bit in the L0ST register becomes 1 (frame or wake-up reception has been completed).
When this bit is set to 1, a LIN0 interrupt is generated when the FRC bit becomes 1.

24.1.10.3 ERRIE Bit

This bit enables or disables an interrupt when an error is detected.
When this bit is set to 0, no LIN0 interrupt is generated when the ERR bit in the L0ST register becomes 1 (error detected).
When this bit is set to 1, a LIN0 interrupt is generated when the ERR bit becomes 1.
The sources to generate the LIN0 interrupt are the following interrupts: bit error, physical bus error, frame timeout error, framing error, and checksum error.
The detection of the above errors except checksum error can be enabled or disabled by the L0EDE register.

24.1.11 LIN0 Error Detection Enable Register (L0EDE)

LIN0 Error Detection Enable Register



Symbol	Address	Reset Value
L0EDE	016Dh	00h

Bit Symbol	Bit Name	Function	RW
BERE	Bit Error Detection Enable Bit	0: Bit error detection disabled 1: Bit error detection enabled	RW
PBERE	Physical Bus Error Detection Enable Bit	0: Physical bus error detection disabled 1: Physical bus error detection enabled	RW
FTERE	Frame Timeout Error Detection Enable Bit	0: Frame timeout error detection disabled 1: Frame timeout error detection enabled	RW
FERE	Framing Error Detection Enable Bit	0: Framing error detection disabled 1: Framing error detection enabled	RW
— (b7-b4)	No register bits. If necessary, set to 0. The read value is 0.		—

Figure 24.12 L0EDE Register

Set this register in LIN reset mode.

24.1.11.1 BERE Bit

This bit enables or disables bit error detection.
When this bit is set to 0, no bit error is detected.
When this bit is set to 1, a bit error is detected.
The detection result when this bit is 1 is reflected in the BER bit in the L0EST register.
For details on bit error, refer to 24.9 “Error Status”.

24.1.11.2 PBERE Bit

This bit enables or disables physical bus error detection.
When this bit is set to 0, no physical bus error is detected.
When this bit is set to 1, a physical bus error is detected.
The detection result when this bit is 1 is reflected in the PBER bit in the L0EST register.
For details on physical bus error, refer to 24.9 “Error Status”.

24.1.11.3 FTERE Bit

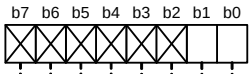
This bit enables or disables frame timeout error detection.
When this bit is set to 0, no frame timeout error is detected.
When this bit is set to 1, a frame timeout error is detected.
The detection result when this bit is 1 is reflected in the FTER bit in the L0EST register.
For details on frame timeout error, refer to 24.9 “Error Status”.

24.1.11.4 FERE Bit

This bit enables or disables framing error detection.
When this bit is set to 0, no framing error is detected.
When this bit is set to 1, a framing error is detected.
The detection result when this bit is 1 is reflected in the FER bit in the L0EST register.
For details on framing error, refer to 24.9 “Error Status”.

24.1.12 LIN0 Control Register (L0C)

LIN0 Control Register



Symbol	Address	Reset Value
L0C	016Eh	00h

Bit Symbol	Bit Name	Function	RW
OM0	LIN Reset Bit	0: LIN reset mode 1: Mode other than LIN reset mode	RW
OM1	LIN Mode Select Bit	0: LIN wake-up mode 1: LIN operation mode	RW
— (b7-b2)	No register bits. If necessary, set to 0. The read value is 0.		—

Figure 24.13 L0C Register

When entering LIN wake-up mode from LIN reset mode, write 01h to this register. When entering LIN operation mode from LIN reset mode, write 03h to this register.
In LIN self-test mode, write 03h to this register after the LIN module enters LIN self-test mode.

24.1.12.1 OM0 Bit

This bit selects whether the LIN module enters or exits in LIN reset mode.
When this bit is set to 0, the LIN module enters LIN reset mode.
When this bit is set to 1, the LIN module exits LIN reset mode.

24.1.12.2 OM1 Bit

This bit selects the operation mode (LIN wake-up mode or LIN operation mode) when the LIN module exits LIN reset mode.
When bits OM1 and OM0 are set to 01b, LIN wake-up mode is selected.
When bits OM1 and OM0 are set to 11b, LIN operation mode is selected.
This bit cannot be written while the FTS bit in the L0TC register is 1 (start frame transmission/wake-up transmission and reception).

24.1.13 LIN0 Transmit Control Register (L0TC)

LIN0 Transmission Control Register

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	X		

Symbol	Address	Reset Value
L0TC	0170h	00h

Bit Symbol	Bit Name	Function	RW
FTS	Frame Transmission/ Wake-up Transmission and Reception Start Bit	0: Stop frame transmission/wake-up transmission and reception 1: Start frame transmission/wake-up transmission and reception	RW
RTS	Response Transmission Start Bit	0: Stop response transmission in frame separate mode 1: Start response transmission in frame separate mode	RW
— (b7-b2)	No register bits. If necessary, set to 0. The read value is 0.		—

Figure 24.14 L0TC Register

24.1.13.1 FTS Bit

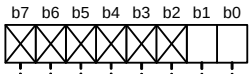
Set this bit to 1 when a frame/wake-up transmission starts.
Set this bit to 1 to perform a wake-up reception (input signal Low time counting).
The bit remains 1 during communication. It becomes 0 when there is no communication and when the LIN module enters LIN reset mode.
This bit can be set to 1 only. It cannot be set to 0. This bit automatically becomes 0 when transmission or reception is completed, or when an error is detected.

24.1.13.2 RTS Bit

Set this bit to 1 when a response transmission starts.
The bit remains 1 during communication. It becomes 0 when there is no communication, and when the LIN module enters LIN reset mode.
This bit can be set to 1 only. It cannot be set to 0. This bit automatically becomes 0 when the transmission is completed, or when an error is detected.
Set this bit when the FSM bit in the LMD0 register is 1 (frame separate mode) and the FTS bit is 1 (frame transmission/wake-up transmission and reception started).

24.1.14 LIN0 Mode Status Register(L0MST)

LIN0 Mode Status Register



Symbol	Address	Reset Value
L0MST	0171h	00h

Bit Symbol	Bit Name	Function	RW
OMM0	LIN Reset Status Monitor	0: LIN reset mode 1: Mode other than LIN reset mode	R
OMM1	LIN Mode Status Monitor	0: LIN wake-up mode 1: LIN operation mode	R
— (b7-b2)	No register bits. If necessary, set to 0. The read value is 0.		—

Figure 24.15 L0MST Register

24.1.14.1 Bits OMM0 and OMM1

These bits are used to check the current operational mode.

24.1.15 LIN0 Status Register (L0ST)

LIN0 Status Register

b7	b6	b5	b4	b3	b2	b1	b0
		X	X		X		

Symbol	Address	Reset Value
L0ST	0172h	00h

Bit Symbol	Bit Name	Function	RW
FTC	Frame/Wake-up Transmit Completion Flag	0: Transmission incompleted 1: Frame or wake-up transmission has been completed	RW
FRC	Frame/Wake-up Receive Completion Flag	0: Reception incompleted 1: Frame or wake-up reception has been completed	RW
— (b2)	No register bit. If necessary, set to 0. The read value is 0.		—
ERR	Error Detection Flag	0: Error not detected 1: Error detected	R
— (b5-b4)	No register bits. If necessary, set to 0. The read value is 0.		—
D1RC	Data 1 Receive Completion Flag	0: Reception incompleted 1: Data 1 reception completed	RW
HTRC	Header Transmit Completion Flag	0: Transmission incompleted 1: Header transmission completed	RW

Figure 24.16 L0ST Register

This register automatically becomes 00h when the LIN module enters LIN reset mode and when the next communication starts.
This register retains 00h during LIN reset mode.
Do not write to this register while the FTS bit in the L0TC register is 1 (frame transmission/wake-up transmission and reception started).

24.1.15.1 FTC Bit

This bit can be set to 0 only. Writing 1 to this bit has no effect.
This bit becomes 1 when a frame or wake-up transmission is completed. The LIN0 interrupt request is generated if the FTCIE bit in the L0IE register is set to 1 (interrupt enabled) at this time. To set this bit to 0 before the next communication starts, write 0 in LIN wake-up mode, or LIN operation mode.

24.1.15.2 FRC Bit

This bit can be set to 0 only. Writing 1 to this bit has no effect.
This bit becomes 1 when a frame reception or wake-up reception (input signal Low time counting) is completed. The LIN0 interrupt request is generated if the FRCIE bit in the L0IE register is set to 1 (interrupt enabled) at this time. To set this bit to 0 before the next communication starts, write 0 in LIN wake-up mode, or LIN operation mode.

24.1.15.3 ERR Bit

This bit becomes 1 when an error is detected. The LIN0 interrupt request is generated if the ERRIE bit in the L0IE register is set to 1 (interrupt enabled) at this time. To set this bit to 0 before the next communication starts, write 0 to bits BER, PBER, FTER, FER, and CSER in the L0EST register when in LIN wake-up mode or LIN operation mode. The ERR bit becomes 0.

24.1.15.4 D1RC Bit

This bit can be set to 0 only. Writing 1 to this bit has no effect.
This bit becomes 1 when a data 1 reception is completed, but an interrupt request is not generated.
To set this bit to 0 before the next communication starts, write 0 in LIN operation mode.

24.1.15.5 HTRC Bit

This bit can be set to 0 only. Writing 1 to this bit has no effect.
This bit becomes 1 when a header reception is completed, but an interrupt request is not generated.
To set this bit to 0 before the next communication starts, write 0 in LIN operation mode.

24.1.16 LIN0 Error Status Register (L0EST)

LIN0 Error Status Register

b7	b6	b5	b4	b3	b2	b1	b0
X	0		X				

Symbol	Address	Reset Value
L0EST	0173h	00h

Bit Symbol	Bit Name	Function	RW
BER	Bit Error Flag	0: Bit error not detected 1: Bit error detected	RW
PBER	Physical Bus Error Flag	0: Physical bus error not detected 1: Physical bus error detected	RW
FTER	Frame Timeout Error Flag	0: Frame timeout error not detected 1: Frame timeout error detected	RW
FER	Framing Error Flag	0: Framing error not detected 1: Framing error detected	RW
— (b4)	No register bit. If necessary, set to 0. The read value is 0.		—
CSER	Checksum Error Flag	0: Checksum error not detected 1: Checksum error detected	RW
— (b6)	Reserved	Set to 0.	RW
— (b7)	No register bit. If necessary, set to 0. The read value is 0.		—

Figure 24.17 L0EST Register

This register automatically becomes 00h when the LIN module enters LIN reset mode and when the next communication starts.
This register retains 00h during LIN reset mode.
Do not write to this register while the FTS bit in the L0TC register is 1 (frame transmission/wake-up transmission and reception started).

24.1.16.1 BER Bit

Only 0 can be written to this bit. Writing 1 to this bit has no effect.
This bit becomes 1 when a bit error is detected. To set this bit to 0 before the next communication starts, write 0 in LIN wake-up mode, or LIN operation mode.

24.1.16.2 PBER Bit

Only 0 can be written to this bit. Writing 1 to this bit has no effect.
This bit becomes 1 when a physical bus error is detected. To set this bit to 0 before the next communication starts, write 0 in LIN wake-up mode, or LIN operation mode.

24.1.16.3 FTER Bit

Only 0 can be written to this bit. Writing 1 to this bit has no effect.
This bit becomes 1 when a frame timeout error is detected. To set this bit to 0 before the next communication starts, write 0 in LIN operation mode.

24.1.16.4 FER Bit

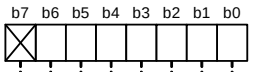
Only 0 can be written to this bit. Writing 1 to this bit has no effect.
This bit becomes 1 when a framing error is detected. To set this bit to 0 before the next communication starts, write 0 in LIN operation mode.

24.1.16.5 CSER Bit

Only 0 can be written to this bit. Writing 1 to this bit has no effect.
This bit becomes 1 when a checksum error is detected. To set this bit to 0 before the next communication starts, write 0 in LIN operation mode.

24.1.17 LIN0 Response Field Setting Register (L0RFC)

LIN0 Response Field Setting Register



Symbol	Address	Reset Value
L0RFC	0174h	00h

Bit Symbol	Bit Name	Function	RW
RFDL	Response Field Data Length Setting Bit	b3 b2 b1 b0 0 0 0 0 : 0 bytes + checksum 0 0 0 1 : 1 byte + checksum 0 0 1 0 : 2 bytes + checksum 0 0 1 1 : 3 bytes + checksum 0 1 0 0 : 4 bytes + checksum 0 1 0 1 : 5 bytes + checksum 0 1 1 0 : 6 bytes + checksum 0 1 1 1 : 7 bytes + checksum 1 0 0 0 : 8 bytes + checksum Only set the values listed above.	RW
RFT	Response Field Transmit/ Receive Direction Setting Bit	0: Reception 1: Transmission	RW
CSM	checksum Model Select Bit	0: Classic checksum 1: Enhanced checksum	RW
FSM	Frame Separate Mode Select Bit	0: Non-frame separate mode 1: Frame separate mode	RW
— (b7)	No register bit. If necessary, set to 0. The read value is 0.		—

Figure 24.18 L0RFC Register

Set this register when the FTS bit in the L0TC register is 0 (frame transmission/wake-up transmission and reception stopped).

24.1.17.1 RFDL Bit

This bit sets the data length of the response field.
The data length can be set to 0 bytes to 8 bytes, without including the size of checksum.

24.1.17.2 RFT Bit

When this bit is set to 0, reception is performed in the response field. In LIN wake-up mode, wake-up reception (input signal Low time counting) is performed.
When this bit is set to 1, transmission is performed in the response field. In LIN wake-up mode, wake-up transmission is performed.

24.1.17.3 CSM Bit

This bit sets the model of checksum.
When this bit is set to 0, the checksum model is classic.
When this bit is set to 1, the checksum model is enhanced.
When the FTERE bit in the L0EDE register is 1 (frame timeout error detection enabled), the frame timeout error value varies depending on the setting of the CSM bit. For details, refer to 24.9 “Error Status”.

24.1.17.4 FSM Bit

When this bit is set to 0, frame separate mode is not selected.
When this bit is set to 1, frame separate mode is selected.
In response reception (when the RFT bit is set to 0), the setting of the FSM bit has no effect.
To enter LIN self-test mode, set this bit to 0 before the LIN module enters LIN self-test mode.
For details on frame separate mode, refer to 24.6.1.1 “Frame Separate Mode”.

24.1.18 LIN0 ID Buffer Register (L0IDB)

LIN0 ID Buffer Register

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	Reset Value
L0IDB	0175h	XXh

Bit Symbol	Bit Name	Function	RW
ID	ID Setting Bit	Set an ID of 6 bits to be transmitted by the ID field	RW
IDP	Parity Setting Bit	Set the parity (P0, P1) bit to be transmitted by the ID field	RW

Figure 24.19 L0IDB Register

Set this register when the FTS bit in the L0TC register is 0 (frame transmission/wake-up transmission and reception stopped).

In LIN self-test mode, the specifications are as follows:

- When the RFT bit in the L0RFC register is 1 (transmission):
  The inverted value of the transmitted value can be read. The value to be transmitted can be written before communication.
- When the RFT bit is 0 (reception):
  The inverted value of the received value can be read. The value to be received can be written before communication.

24.1.18.1 ID Bit

This bit sets an ID of 6 bits to be transmitted by the ID field of the LIN frame.

24.1.18.2 IDP Bit

This bit sets the parity (P0, P1) bit to be transmitted by the ID field of the LIN frame.
Since the parity bit is not calculated, set an appropriate value. Even if an erroneous calculation result is set, transmit operation is still performed.

24.1.19 LIN0 Checksum Buffer Register (L0CB)

LIN0 Checksum Buffer Register

b7	b0	Symbol	Address	Reset Value
		L0CB	0176h	XXh

Function	RW
Store the checksum data to be transmitted and received	RW

Figure 24.20 L0CB Register

Set this register when the FTS bit in the L0TC register is 0 (frame transmission/wake-up transmission and reception stopped).

In LIN operation mode, the specifications are as follows.

- When the RFT bit in the L0RFC register is 1 (transmission):
  The transmitted value can be read. Writing is disabled.
- When the RFT bit is 0 (reception):
  The received value can be read. Writing is disabled.

In LIN self-test mode, the specifications are as follows:

- When the RFT bit is 1 (transmission):
  The inverted value of the transmitted value can be read.
- When the RFT bit is 0 (reception):
  The inverted value of the received value can be read. The value to be received can be written before communication.

Write operations are disabled when in LIN reset mode and LIN wake-up mode.

24.1.20 LIN0 Data n Buffer Register (L0DBn) (n = 1 to 8)

LIN0 Data n Buffer Register (n = 1 to 8)

b7 b0

Symbol	Address	Reset Value
L0DBn	0178h to 017Fh	XXh

Function	Setting Range	RW
Set the data to be transmitted or read the received data	00h to FFh	RW

Figure 24.21 Registers L0DB1 to L0DB8

Set registers with the states below.

In response transmission
- The RFT bit in the L0RFC register is 1 (transmission)
- The FSM bit in the L0RFC register is 0 (non-frame separate mode)
- The FTS bit in the L0TC register is 0 (frame transmission/wake-up transmission and reception stopped)

or
- The RFT bit in the L0RFC register is 1 (transmission)
- The FSM bit in the L0RFC register is 1 (frame separate mode)
- The RTS bit in the L0TC register is 0 (response transmission stopped)

In response reception
The received data is overwritten.
When an error is detected, data before the reception is aborted is stored.

In LIN self-test mode, the specifications are as follows:
- When the RFT bit in the L0RFC register is 1 (transmission):
  The inverted value of the transmitted value can be read. The value to be transmitted can be written before communication.
- When the RFT bit is 0 (reception):
  The inverted value of the received value can be read. The value to be received can be written before communication.

24.2 Operational Mode

The LIN module has the following four operational modes:

- LIN reset mode
- LIN operation mode
- LIN wake-up mode
- LIN self-test mode

When in LIN reset mode, power consumption can be reduced since the clock is not provided to the LIN module.
Figure 24.22 shows the transition processes between LIN operational mode, and Table 24.3 lists functions available in each mode.

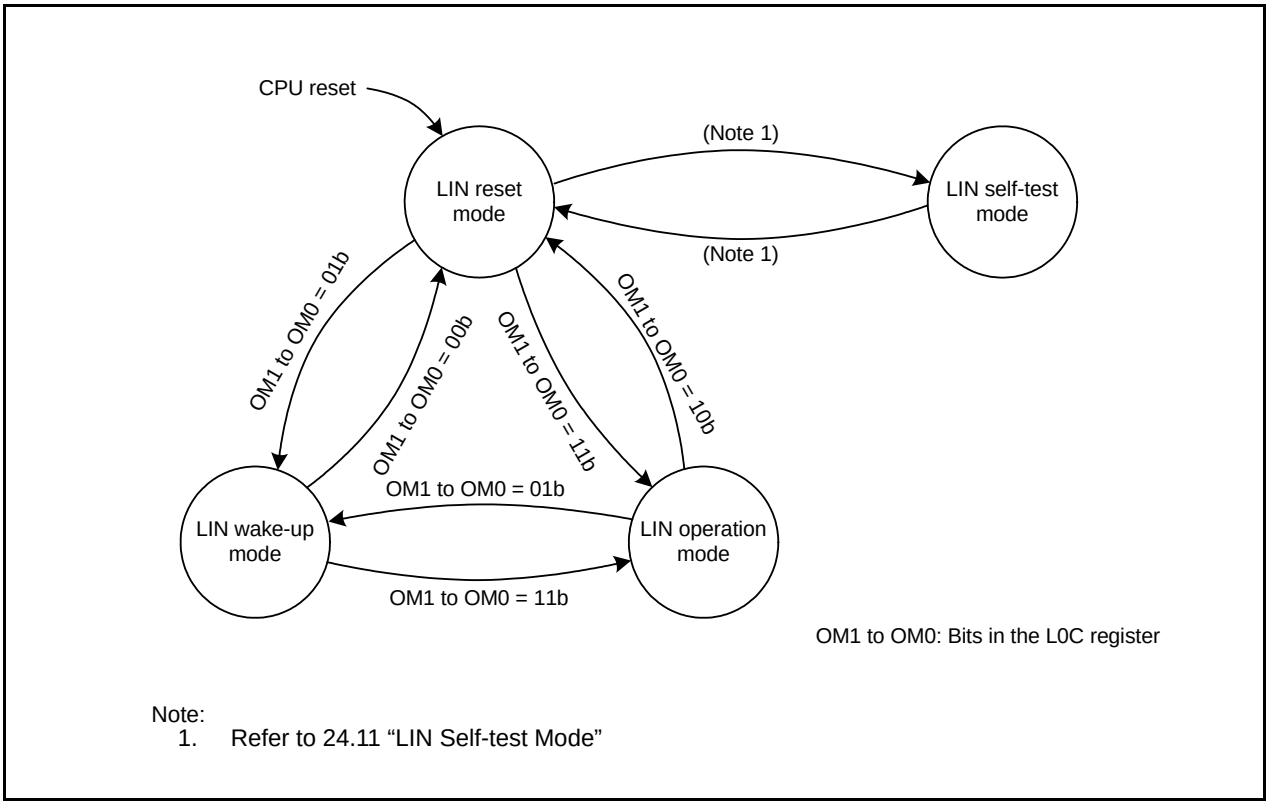


Figure 24.22 Operational Mode Transition

Table 24.3 Available Functions in Each Operational Mode

LIN Reset Mode	LIN Operation Mode	LIN Wake-up Mode	LIN Self-test Mode
LIN0 Low detection	Header transmission Response transmission Response reception Error detection LIN0 Low detection	Wake-up transmission Wake-up reception Error detection LIN0 Low detection	Self-test

The transition to LIN reset mode, LIN operation mode, and LIN wake-up mode can be checked by reading bits OMM1 to OMM0 in the L0MST register.
For details on LIN self-test mode, refer to 24.11 “LIN Self-test Mode”.

24.2.1 LIN Reset Mode

The LIN module enters LIN reset mode by setting the OM0 bit in the L0C register to 0. The transition to LIN reset mode can be confirmed by checking whether the read value of the OMM0 bit in the L0MST register is 0 (LIN reset mode). In this mode, all functions of LIN communication channels are stopped as well as LIN system clock (fLIN).
The LIN module can enter LIN operation mode, LIN wake-up mode, or LIN self-test mode from LIN reset mode.

The following registers are initialized to their reset values after the LIN module enters LIN reset mode. The registers retain their initial values during LIN reset mode.

- L0TC register
- L0ST register
- L0EST register

The following registers retain their previous values after the LIN module enters LIN reset mode.

- LWBR register
- LBRP0 register
- LBRP1 register
- LPC register
- L0MD register
- L0BRK register
- L0SPC register
- L0WUP register
- L0IE register
- L0EDE register
- L0RFC register
- L0IDB register
- L0CB register
- L0DBn register

24.2.2 LIN Operation Mode

LIN operation mode is activated by setting bits OM1 to OM0 in the L0C register to 11b, and bits OMM1 to OMM0 in the L0MST register become 11b.

24.2.3 LIN Wake-up Mode

LIN wake-up mode is activated by setting bits OM1 to OM0 in the L0C register to 01b, and bits OMM1 to OMM0 in the L0MST register become 01b.

24.2.4 LIN Self-test Mode

LIN self-test mode is activated by writing to the LSTC register. The transition to LIN self-test mode can be confirmed by checking whether the read value of the LSTM bit in the LSTC register is 1 (LIN self-test mode).

24.3 Operational Overview

24.3.1 Header Transmission

Figure 24.23 shows the operation in header transmission, and Table 24.4 lists the processing in header transmission.

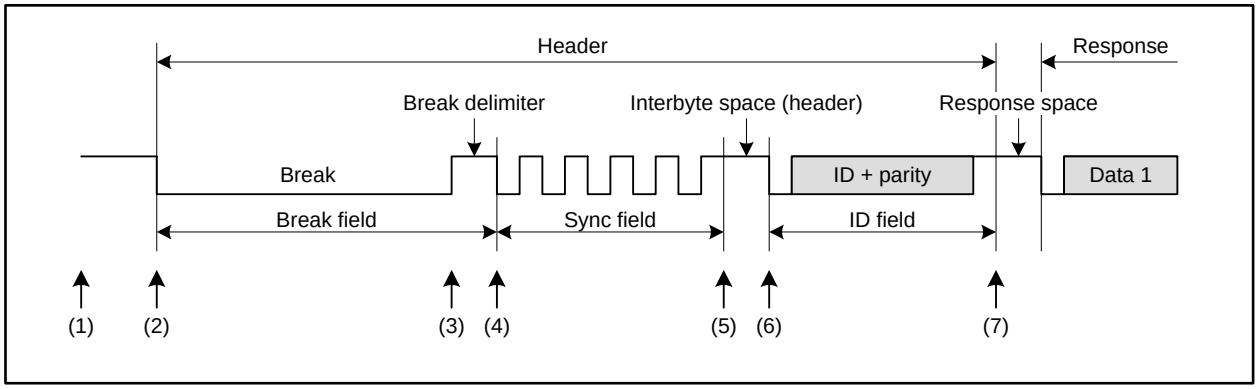


Figure 24.23 Operation in Header Transmission

Table 24.4 Processing in Header Transmission

	Software Processing	LIN Module Processing
(1)	• Set a baud rate (Refer to 24.4 “Baud Rate Generator”.) • Set the following bits in the L0IE register: FTCIE bit to 1 (frame/wake-up transmit completion interrupt enabled); FRCIE bit to 1 (frame/wake-up receive completion interrupt enabled); ERRIE bit to 1 (error detection interrupt enabled) • Set bits OM1 to OM0 in the L0C register for LIN mode operation • Set the following bits in the L0BRK register: BLT bits for break (13 to 28 Tbits); BDT bits for break delimiter (1 to 4 Tbits) • Set the following bits in the L0SPC register: IBSH bits for interbyte space (header)/response space (0 to 7 Tbits); IBS bits for interbyte space (0 to 3 Tbits) • Set the following bits in the L0IDB register: ID bit for ID value; IDP bit for parity value • Set the following bits in the L0RFC register: RFDL bits for data length; RFT bit for response transmit/receive direction; CSM bit for checksum model • Set the transmit data	Wait for frame/wake-up transmission start by software (idle)
(2)	• Set the FTS bit in the L0TC register to 1 (frame transmission/wake-up transmission and reception started)	Transmit break
(3)		Transmit break delimiter
(4)		Transmit sync field (55h)
(5)		Transmit interbyte space (header)
(6)		Transmit ID field
(7)		• Set header transmit completion flag or error flag • Transmit response space

24.3.2 Response Transmission

Figure 24.24 shows the operation in response transmission, and Table 24.5 lists the processing in response transmission.

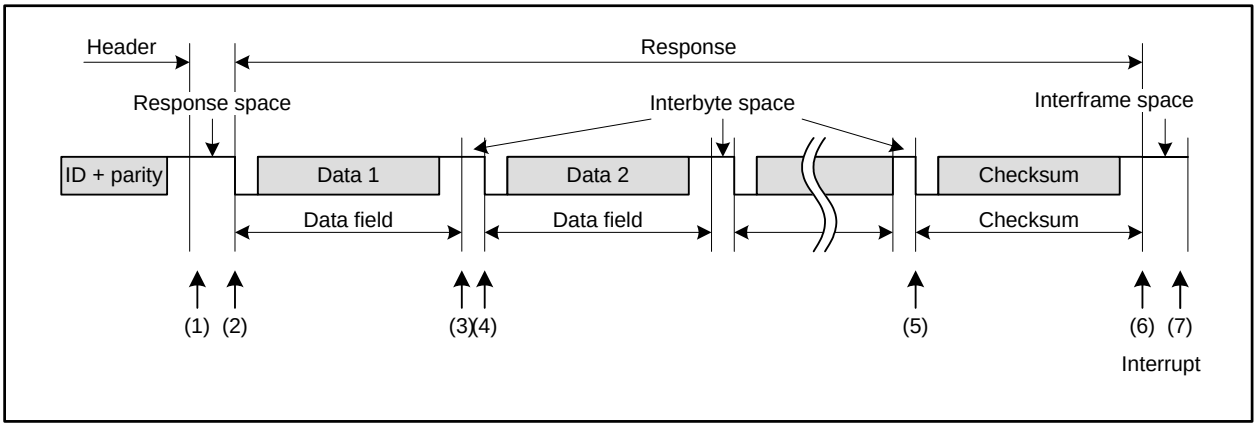


Figure 24.24 Operation in Response Transmission

Table 24.5 Processing in Response Transmission

	Software Processing	LIN Module Processing
(1)	• In frame separate mode Set the RTS bit in the L0TC register to 1 (response transmission started) • In non-frame separate mode Wait for generating an interrupt request	• In frame separate mode Transmit response space while waiting for response transmission enabled • In non-frame separate mode Go to (2) if the response space transmission has been completed
(2)	Wait for generating an interrupt request	Transmit Data 1
(3)		Transmit interbyte space
(4)		Transmit Data 2, then the next interbyte space Transmit Data 3, then the next interbyte space Repeat for the data length specified in the RFDL bit in the L0RFC register. If an error occurs, go to (6). : :
(5)		Transmit checksum
(6)		• Set frame/wake-up transmit completion flag or error flag • Set the following bits in the L0TC register: FTS bit = 0 (frame transmission/wake-up transmission and reception stopped); RTS bit = 0 (response transmission stopped)
(7)	Processing after communication Check the L0ST register and set flags to 0	Idle

24.3.3 Response Reception

Figure 24.25 shows the operation in response reception, and Table 24.6 lists the processing in response reception.

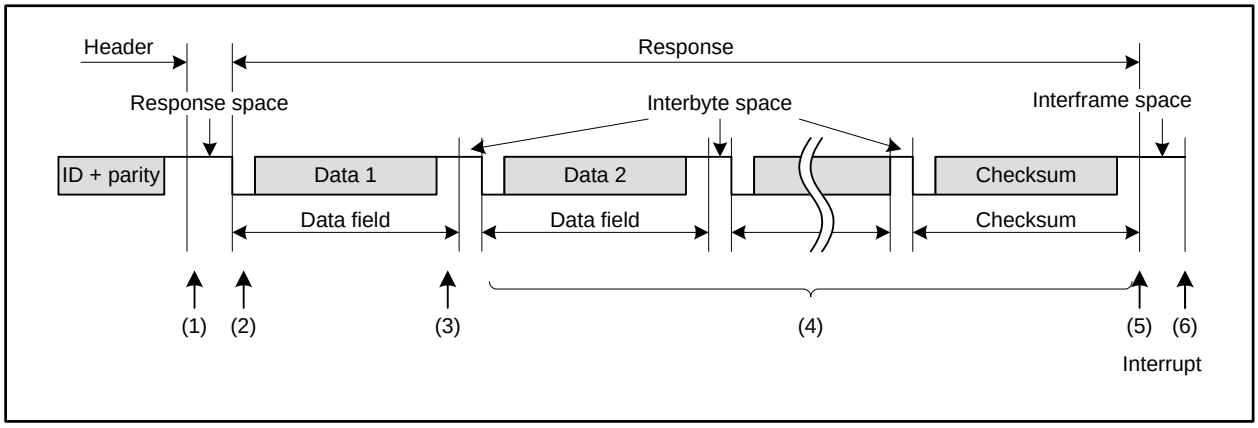


Figure 24.25 Operation in Response Reception

Table 24.6 Processing in Response Reception

	Software Processing	LIN Module Processing
(1)	Wait for generating an interrupt request (without processing)	Wait for detecting a start bit
(2)	Wait for generating an interrupt request	Receive Data 1 due to a start bit detected
(3)		• Set Data 1 receive completion flag
(4)		Receive Data 2 due to a start bit detected Receive Data 3 due to a start bit detected Repeat for the data length specified in the RFDL bit in the L0RFC register. If an error occurs, cancel the receive operation, and go to (5). In this case, checksum judgment in (5) is not executed. : : Receive checksum due to a start bit detected
(5)		• Judge the checksum • Set frame receive completion flag or error flag • Set the FTS bit in the L0TC register to 0 (frame transmission/wake-up transmission and reception stopped)
(6)	Processing after communication Read the received data Check the L0ST register and set flags to 0	Idle

24.4 Baud Rate Generator

The LIN system clock (fLIN) is generated by the LIN clock divided by the baud rate generator. This fLIN, divided by 16 is used as bit rate. The reciprocal of the bit rate is called bit time, expressed as “Tbit”.
The LBRP0 register should be set so that fa is 307200 Hz (19200 bps × 16). Therefore,
fa = 19200 bps × 16,
fb = 9600 bps × 16, and
fc = 2400 bps × 16.
Then they are divided by 16 in the bit timing generator, which results in 19200 bps, 9600 bps, and 2400 bps, respectively. The baud rate of 10417 bps can be generated by the bit setting of the LBRP1 register.

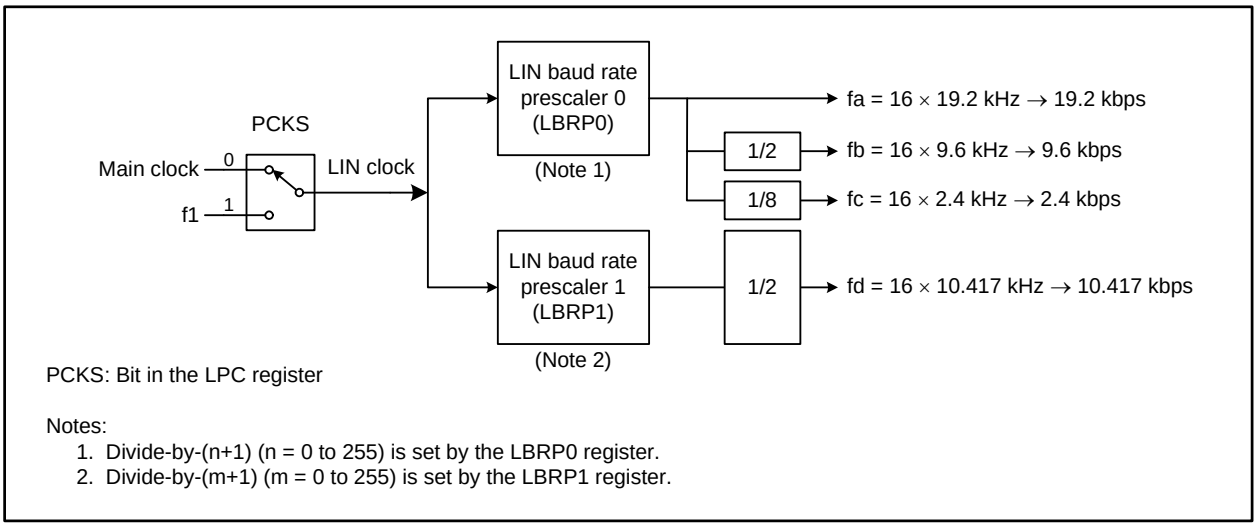


Figure 24.26 Baud Rate Generation Block Diagram

Table 24.7 and Table 24.8 list the baud rates (19200, 9600, 2400, and 10417 bps) generated by the LIN clock frequency, and their error.

Table 24.7 Baud Rate Generation Example for 19200 bps, 9600 bps, and 2400 bps

LIN Clock	Baud Rate Generator 0 Divide-by-(N + 1)	Baud Rate to be Generated			Error (unit: %)
		fa (unit: bps)	fb (unit: bps)	fc (unit: bps)	
32 MHz	104	19230.77 (19200)	9615.38 (9600)	2403.85 (2400)	+0.16
24 MHz	78	19230.77 (19200)	9615.38 (9600)	2403.85 (2400)	+0.16
20 MHz	65	19230.77 (19200)	9615.38 (9600)	2403.85 (2400)	+0.16
16 MHz	52	19230.77 (19200)	9615.38 (9600)	2403.85 (2400)	+0.16
12 MHz	39	19230.77 (19200)	9615.38 (9600)	2403.85 (2400)	+0.16
10 MHz	65	9615.38 (9600)	—	—	+0.16
8 MHz	26	19230.77 (19200)	9615.38 (9600)	2403.85 (2400)	+0.16
6 MHz	39	9615.38 (9600)	—	—	+0.16
	156	2403.85 (2400)			+0.16
5 MHz	130	2403.85 (2400)	—	—	+0.16
4 MHz	13	19230.77 (19200)	9615.38 (9600)	2403.85 (2400)	+0.16
2 MHz	13	9615.38 (9600)	—	—	+0.16
	52	2403.85 (2400)			+0.16

—: Corresponding baud rate cannot be generated

Table 24.8 Baud Rate Generation Example for 10417 bps

LIN Clock	Baud Rate Generator 1 Divide-by-(M + 1)	Baud Rate to be Generated	Error (unit: %)
		fd (unit: bps)	
32 MHz	96	10416.67	-0.003
24 MHz	72	10416.67	-0.003
20 MHz	60	10416.67	-0.003
16 MHz	48	10416.67	-0.003
12 MHz	36	10416.67	-0.003
10 MHz	30	10416.67	-0.003
8 MHz	24	10416.67	-0.003
6 MHz	18	10416.67	-0.003
5 MHz	15	10416.67	-0.003
4 MHz	12	10416.67	-0.003
2 MHz	6	10416.67	-0.003

24.5 Data Transmission and Reception

24.5.1 Data Transmission

The LIN transmits 1-bit data per Tbit.
The transmitted data returns to the input pin for data reception via the LIN transceiver. Then the received data is compared to the transmitted data bit by bit, and the result is stored in the BER bit in the L0EST register (refer to 24.9 “Error Status”). The sampling timing for the received data is at the 13th clock (position of 81.25%) where 1 Tbit is 16 fLIN.
Figure 24.27 shows the data transmission timing.

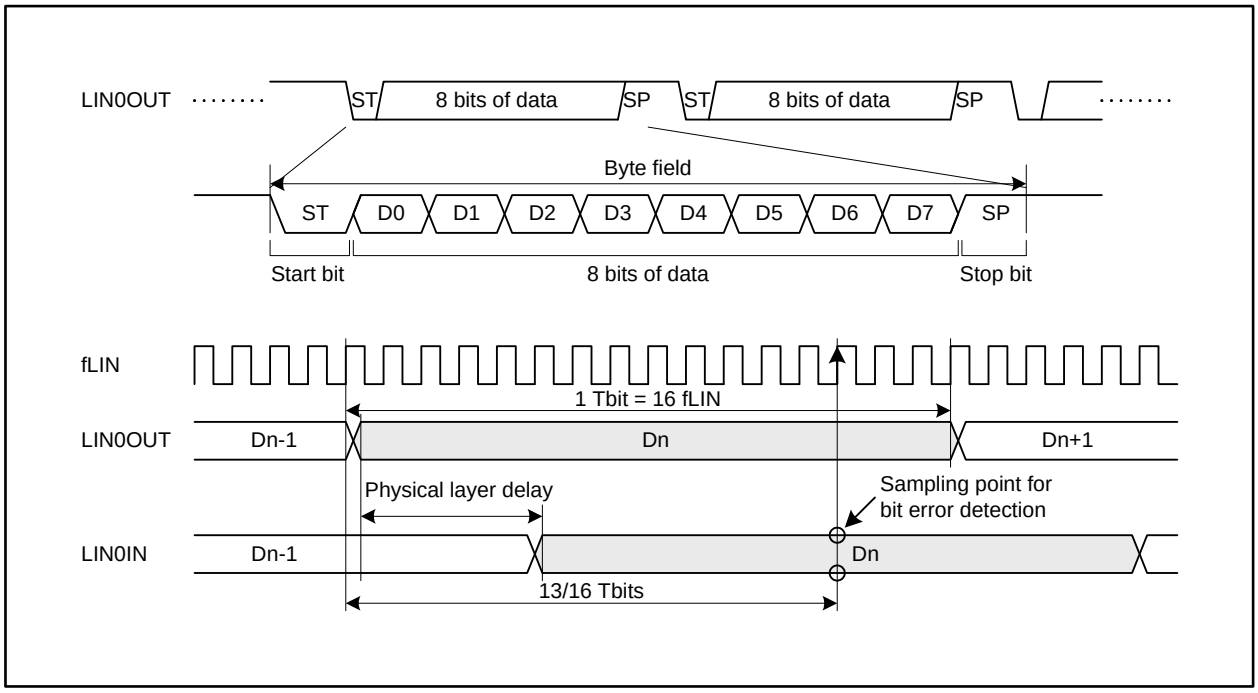


Figure 24.27 Data Transmission Timing

24.5.2 Data Reception

The data reception in the LIN requires an internal signal generated from the input signal at the LIN0IN pin by double-latch clocking scheme.
The byte field of this internal signal, called the synchronized LIN0IN, is synchronized with fLIN at the falling edge of the start bit. The start bit is verified if the synchronized LIN0IN signal is held low 0.5 Tbit after the falling edge is detected. Otherwise, that is, if the signal remains low after exiting reset mode or if it is held high on sampling, no start bit is found.
Once the start bit is detected, data bits are sampled every 1 Tbit.
Figure 24.28 shows the data reception timing.

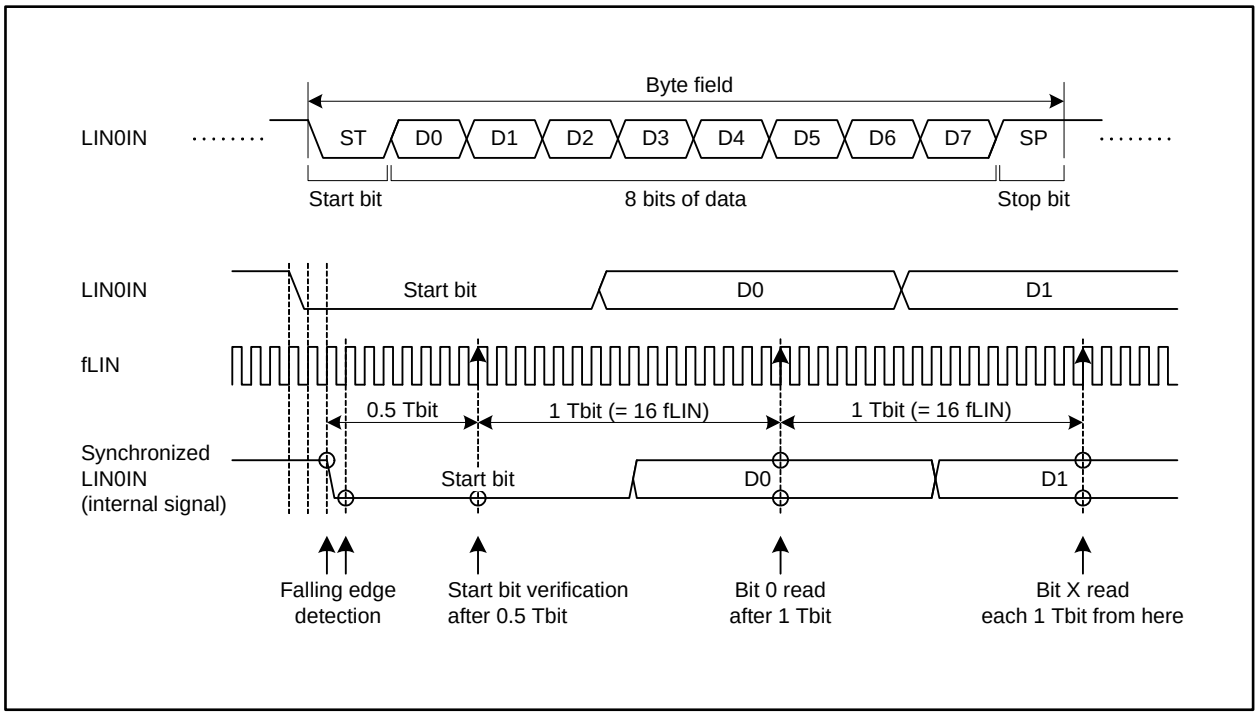


Figure 24.28 Data Reception Timing

24.6 Buffer Processing of Data to be Transmitted and Received Data

The buffer processing in consecutive data transmission and reception of the LIN module is described below.

24.6.1 Transmission of LIN Frame

In 8-byte transmission, the values stored in registers L0DB1 to L0DB8 are transmitted as data 1 to data 8 of the LIN frame, respectively.
In 4-byte transmission, the values stored in registers L0DB1 to L0DB4 are transmitted as data 1 to data 4 of the LIN frame, respectively, and the values stored in registers L0DB5 to L0DB8 are not transmitted.
The transmitted checksum data is stored in the L0CB register.
Figure 24.29 shows LIN transmission processing and buffers.

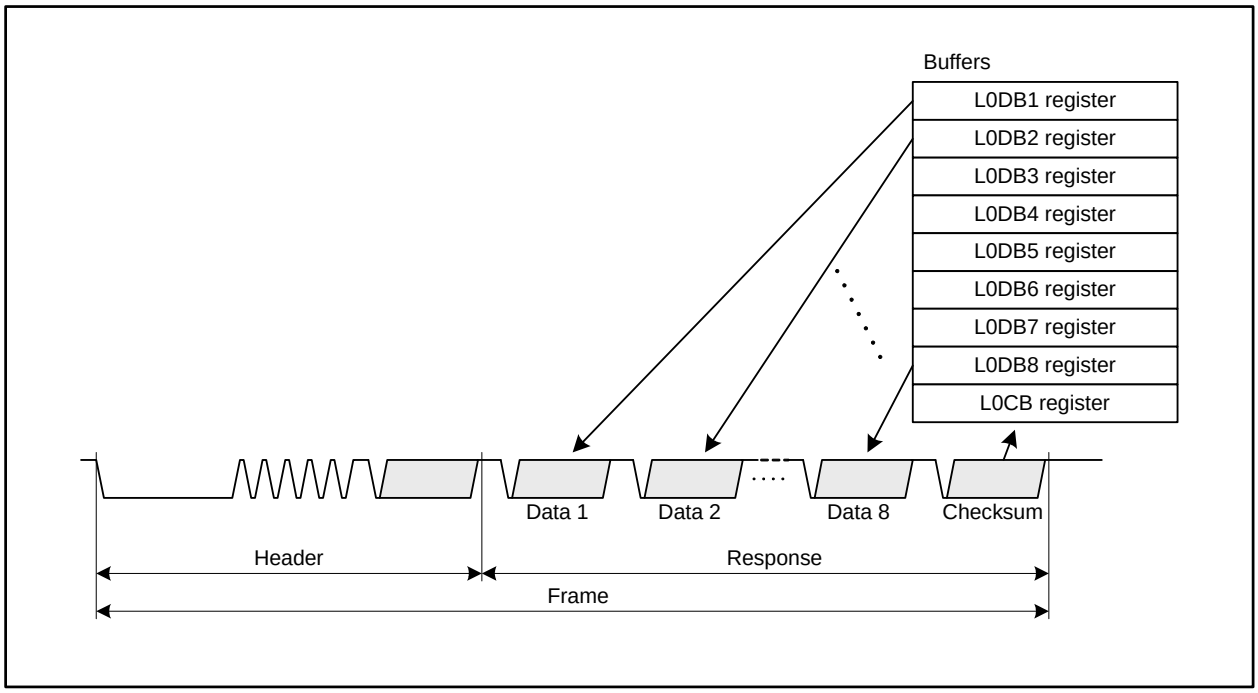


Figure 24.29 LIN Transmission Processing and Buffers

24.6.1.1 Frame Separate Mode

Frame separate mode is selected by setting the FSM bit in the L0RFC register to 1.
In frame separate mode, a header and response can be transmitted according to separate transmit start requests.
When the header transmission has been completed, the HTRC bit in the L0ST register becomes 1 (header transmission completed).

24.6.2 Reception of LIN Frame

In 8-byte reception, data 1 to data 8 of the LIN frame are stored in registers L0DB1 to L0DB8, respectively, every time a stop bit is received.
In 4-byte reception, data 1 to data 4 of the LIN frame are stored in registers L0DB1 to L0DB4, respectively, and no data is stored in registers L0DB5 to L0DB8.
The received checksum is stored in the L0CB register.
Figure 24.30 shows LIN reception processing and buffers.

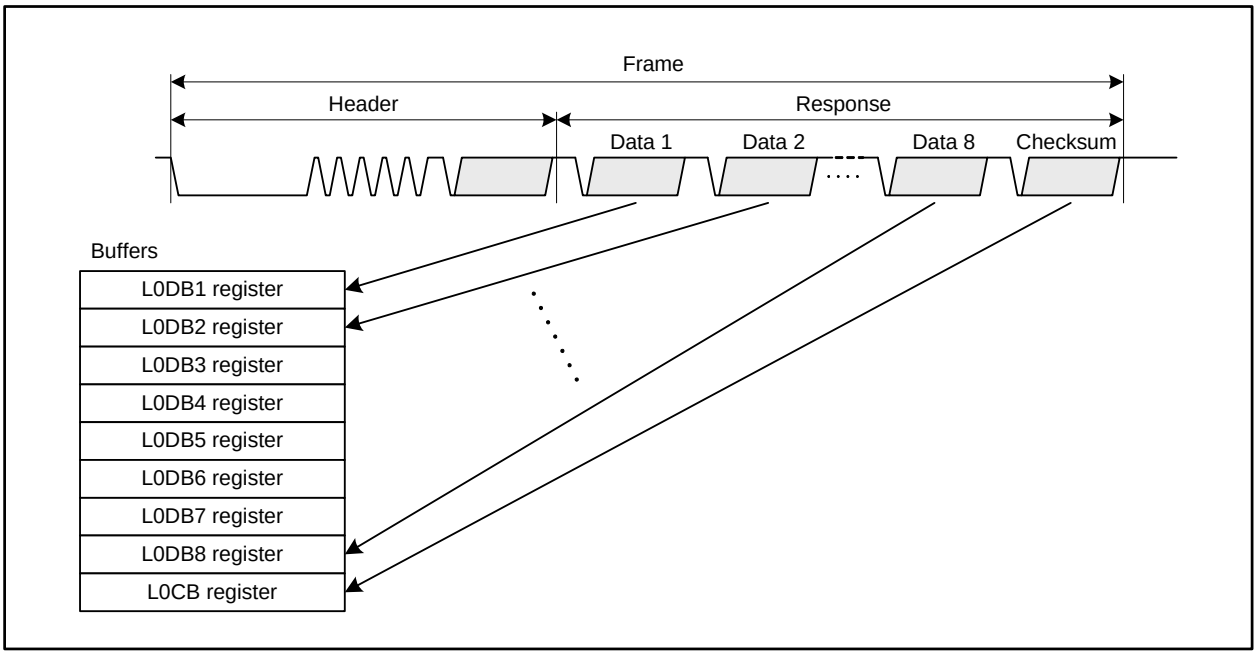


Figure 24.30 LIN Reception Processing and Buffers

24.6.2.1 Data 1 Reception

When the first byte of data reception is completed, the D1RC bit in the L0ST register becomes 1 (data 1 reception completed).

24.7 Wake-up Transmission and Reception

Wake-up transmission and reception is available in LIN wake-up mode.

24.7.1 Operation of Wake-up Transmission

In LIN wake-up mode, if the RFT bit in the L0RFC register is set to 1 (transmission) and the FTS bit in the L0TC register is set to 1 (frame transmission/wake-up transmission and reception started), the wake-up signal is output at the output pin. Low time of the wake-up signal is set by the WUTL bits in the L0WUP register.
When low of wake-up is output without any bit error detected, the FTC bit in the L0ST register becomes 1 (frame or wake-up transmission completed). If the FTCIE bit in the L0IE register is set to 1 (frame/wake-up transmit completion interrupt enabled), an interrupt request is generated.
When a bit error is detected, the operation is aborted and the BER bit in the L0EST register becomes 1 (bit error detected).
Figure 24.31 shows the wake-up transmission timing.

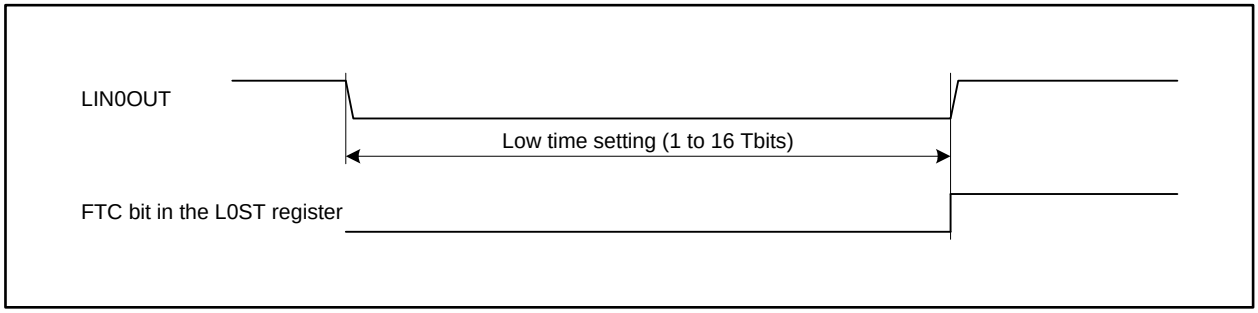


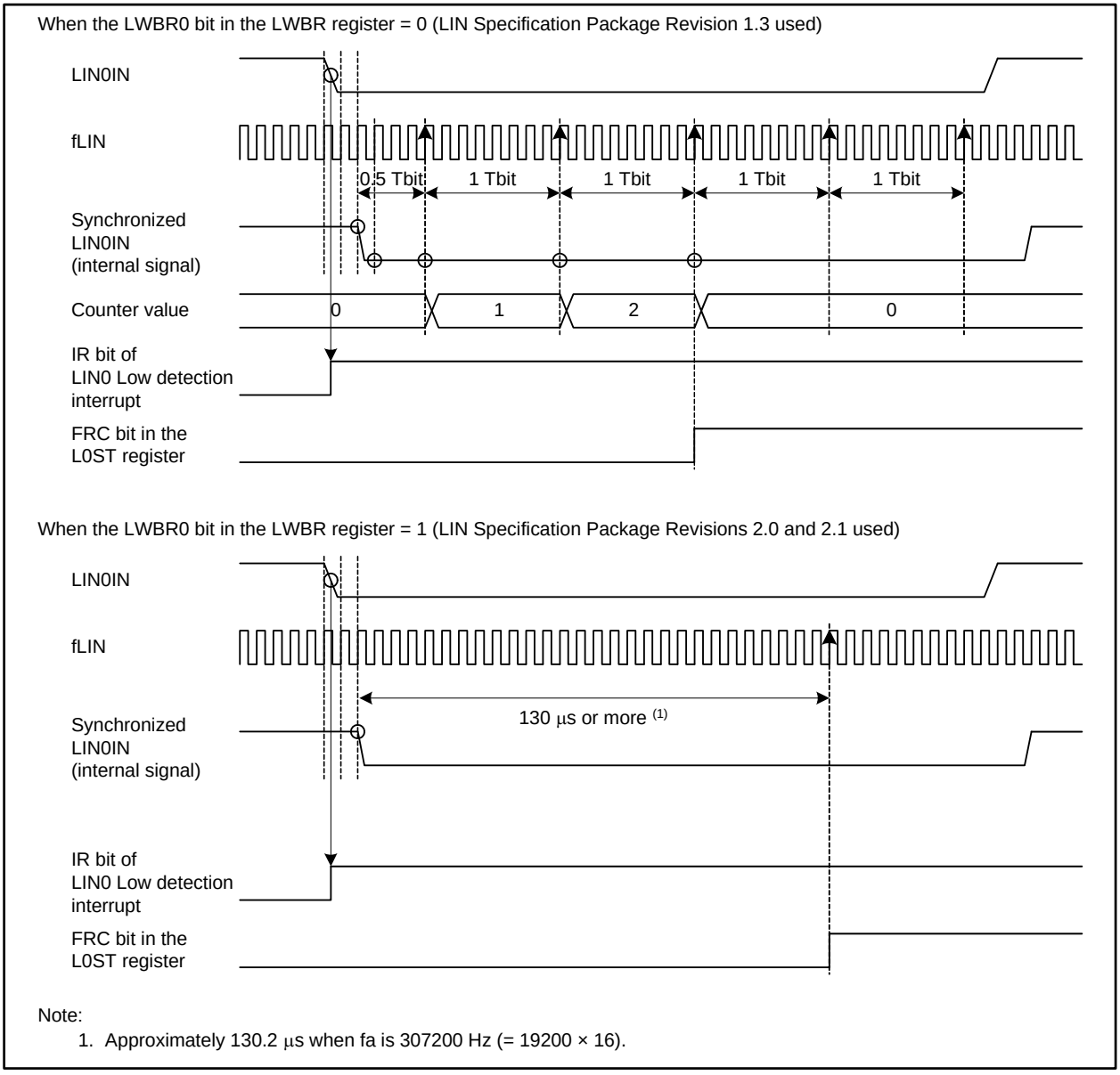
Figure 24.31 Wake-up Transmission Timing

24.7.2 Operation of Wake-up Reception

A wake-up is received by either of following two functions: LIN0 Low detection and input signal Low time counting.

The LIN0 Low detection is to asynchronously detect the falling edge of the input signal at the LIN0IN pin. When the rising edge of the input signal is detected, an interrupt request of LIN0 Low detection is generated.

The input signal Low time counting is to measure the low time of the input signal at the LIN0IN pin by counting at the same sampling timing as that of data reception. The input signal Low time can be measured when it is 2.5 Tbits or more. When LIN Specification Package Revision 1.3 is used, set the LWBR0 bit in the LWBR register to 0, and when LIN Specification Package Revisions 2.0 and 2.1 are used, set the LWBR0 bit to 1. When the LWBR0 is set to 1, fa is used for LIN system clock (fLIN) regardless of what is set to the LCKS bit in the L0MD register (the LCKS bit does not change).
To use this function, set the RFT bit in the L0RFC register to 0 (reception) and the FTS bit in the L0TC register to 1 (frame transmission/wake-up transmission and reception started).
When the Low time to be measured is reached, the FRC bit in the L0ST register becomes 1 (frame or wake-up reception completed). If the FRCIE bit in the L0IE register is set to 1 (frame/wake-up receive completion interrupt enabled), an interrupt request is generated.



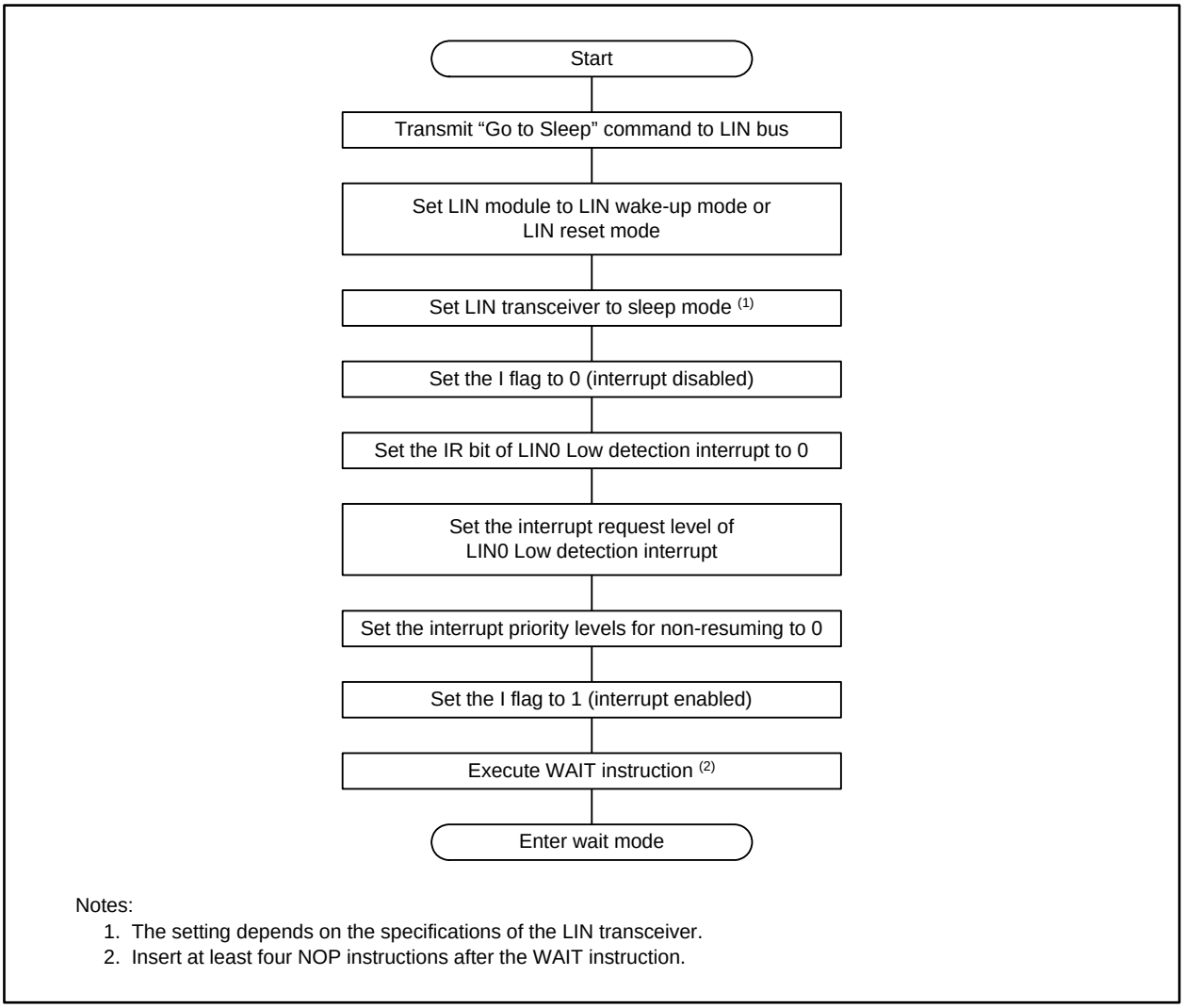
Note:
1. Approximately 130.2 µs when fa is 307200 Hz (= 19200 × 16).

Figure 24.32 Input Signal Low Time Counting

During wake-up transmission, the LIN0 Low detection is workable, but the input signal Low time counting is not workable.

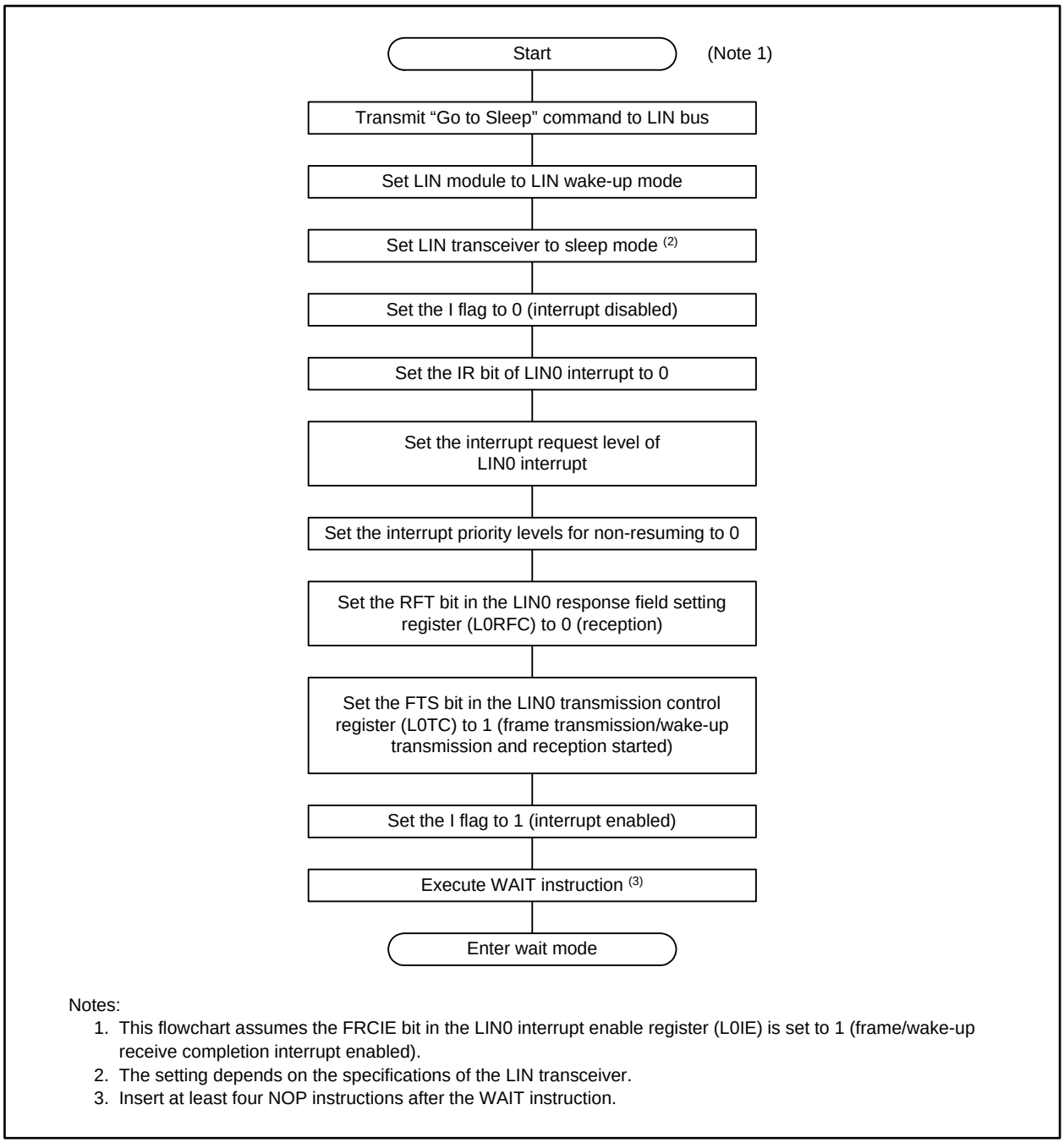
24.7.3 Low Power Mode Control Using Wake-up Reception

The LIN0 Low detection can be used for the interrupt to exit wait or stop mode. The input signal Low time counting can be used for the interrupt to exit wait mode.
Figure 24.33 shows the setting example before transition to wait mode when using LIN0 Low detection. Figure 24.34 shows the setting example before transition to wait mode when using input signal Low time counting. For details on transition to wait mode or stop mode, refer to 9. “Power Control”.



Notes:
1. The setting depends on the specifications of the LIN transceiver.
2. Insert at least four NOP instructions after the WAIT instruction.

Figure 24.33 Setting Example before Transition to Wait Mode when Using LIN0 Low Detection



Notes:
1. This flowchart assumes the FRCIE bit in the LIN0 interrupt enable register (L0IE) is set to 1 (frame/wake-up receive completion interrupt enabled).
2. The setting depends on the specifications of the LIN transceiver.
3. Insert at least four NOP instructions after the WAIT instruction.

Figure 24.34 Setting Example before Transition to Wait Mode when Using Input Signal Low Time Counting

24.7.4 Wake-up Collision

When the master and slave transmit wake-up signals simultaneously, a signal collision occurs on the LIN bus. However, no collision of wake-up signals is detected in the LIN module.

24.8 Operational Status

The LIN module detects seven types of operational status.
The status that can generate an interrupt request are: frame/wake-up transmit completion, frame/wake-up receive completion, and error detection.
Table 24.9 lists the types of operational status.

Table 24.9 Operational Status

Operational Status	Setting Condition	Clearing Condition	Detectable Operational Modes	Corresponding Bits
LIN mode	When LIN module has entered LIN operation mode after the setting of the OM1 bit in the L0C register for LIN operation mode	When LIN module has entered LIN wake-up mode after the setting of the OM1 bit in the L0C register for LIN wake-up mode	LIN operation mode LIN wake-up mode	OMM1 bit in the L0MST register
Reset	When LIN module has exited LIN reset mode after the setting of the OM0 bit in the L0C register for mode other than LIN reset mode	When LIN module has entered LIN reset mode after the setting of the OM0 bit in the L0C register for LIN reset mode	All modes	OMM0 bit in the L0MST register
Frame/wake-up transmit completion	When a response field or wake-up signal transmission has been successfully completed	When the next communication starts • Clearing by software • On transition to LIN reset mode	LIN operation mode LIN wake-up mode	FTC bit in the L0ST register
Frame/wake-up receive completion (1)	When a response field or wake-up signal reception has been successfully completed	When the next communication starts • Clearing by software • On transition to LIN reset mode	LIN operation mode LIN wake-up mode	FRC bit in the L0SRT register
Error detection	When any of bits BER, PBER, FTER, FER, CSER in the L0EST register becomes 1 (error detected)	When the next communication starts • Clearing by software • Note 2 • On transition to LIN reset mode	LIN operation mode LIN wake-up mode	ERR bit in the L0ST register
Data 1 receive completion	When the reception of the first byte of a response frame has been completed in the bit setting as follows: RFT bit in the L0RFC register = 0 (reception) (3)	When the next communication starts • Clearing by software • On transition to LIN reset mode	LIN operation mode	D1RC bit in the L0ST register
Header transmit completion	If a header field transmission has been successfully completed	When the next communication starts • Clearing by software • On transition to LIN reset mode	LIN operation mode	HTRC bit in the L0ST register

Notes:
1. The input signal Low counting is used on wake-up reception.
2. By writing 0 to bits BER, PEBER, FTER, FER, and CSER in the L0EST register when in LIN wake-up mode or LIN operation mode, the ERR bit is set to 0 (error not detected).
3. This status is not detected when the RFDL bits in the L0RFC register are set to 0000b (0 bytes + checksum).

24.9 Error Status

24.9.1 Error Status Types

The LIN module detects five types of error status. These error status can be checked by the bits in the LEST register.
Table 24.10 lists the types of error status.

Table 24.10 Error Status Types

Error Status	Error Detecting Condition (clearing to 0 by software)	Error Detectable Operational Modes	Communication Processing	Detection Enabled/ Disabled	Corresponding Bits
Bit error	When the transmitted data does not match with that on LIN bus monitored by the pin for reception (1)	LIN operation mode LIN wake-up mode	Abort	Selectable	BER bit in the L0EST register
Physical bus error	• If LIN bus detects high when the break field is transmitted • If LIN bus detects low when the break delimiter is transmitted • If LIN bus detects high when the wake-up is transmitted	LIN operation mode LIN wake-up mode	Abort	Selectable	PBER bit in the L0EST register
Frame timeout error	When the transmit/receive operation is not completed within a specified period of time (2)	LIN operation mode	Abort	Selectable	FTER bit in the L0EST register
Framing error	When the stop bit of each data byte is low in response frame reception processing	LIN operation mode	Abort	Selectable	FER bit in the L0EST register
Checksum error	When the checksum judgment of response frame reception processing results in an error	LIN operation mode	—	Unselectable	CSER bit in the L0EST register

Notes:
1. When a bit error is detected, the processing is aborted after the stop bit is transmitted. If it is detected in non-data space such as a break field or an interbyte space, or during wake-up, the transmission processing is aborted immediately after the error bit is transmitted.
2. The period of time (as timeout value) depends on the response field data length set by the RFDL bits in the L0RFC register and the checksum selected by the CSM bit in the L0RFC register as follows:

When classic checksum is selected (the CSM bit in the L0RFC register = 0)

$$\text{Timeout value} = 49 + (\text{data bytes} + 1) \times 14 \quad [\text{Tbit}]$$

When enhanced checksum is selected (the CSM bit in the L0RFC register = 1)

$$\text{Timeout value} = 48 + (\text{data bytes} + 1) \times 14 \quad [\text{Tbit}]$$

The above period of time will exceed the value of TFRAME_MAX shown in LIN Specification Package Revision 1.3 when classic checksum is selected, and the value of TFRAME_MAX shown in LIN Specification Package Revisions 2.0 and 2.1 when enhanced checksum is selected.

24.9.2 LIN Error Detection Targets

Figure 24.35 shows the time domain which the LIN module monitors for error detection.

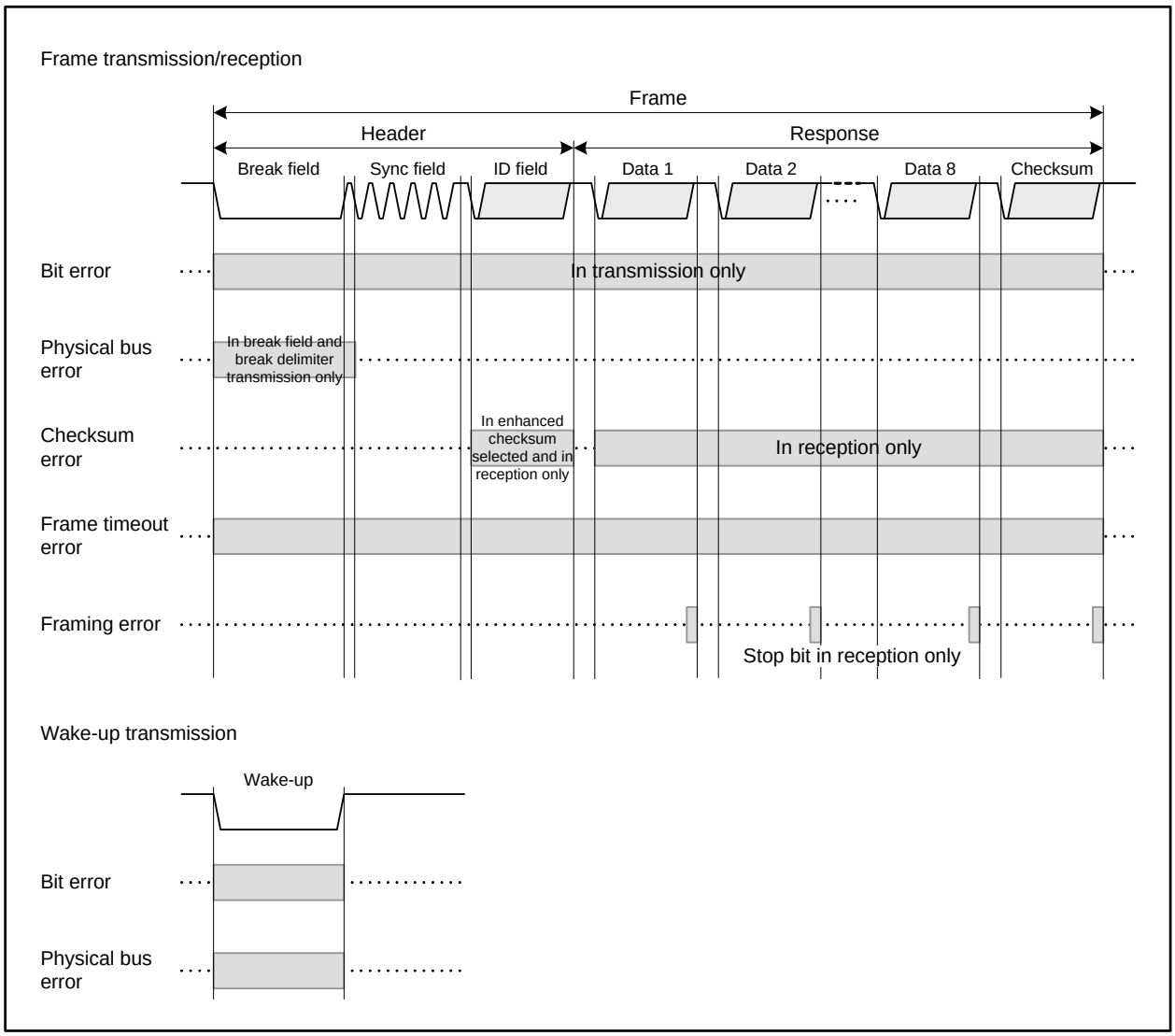


Figure 24.35 LIN Error Detection Targets

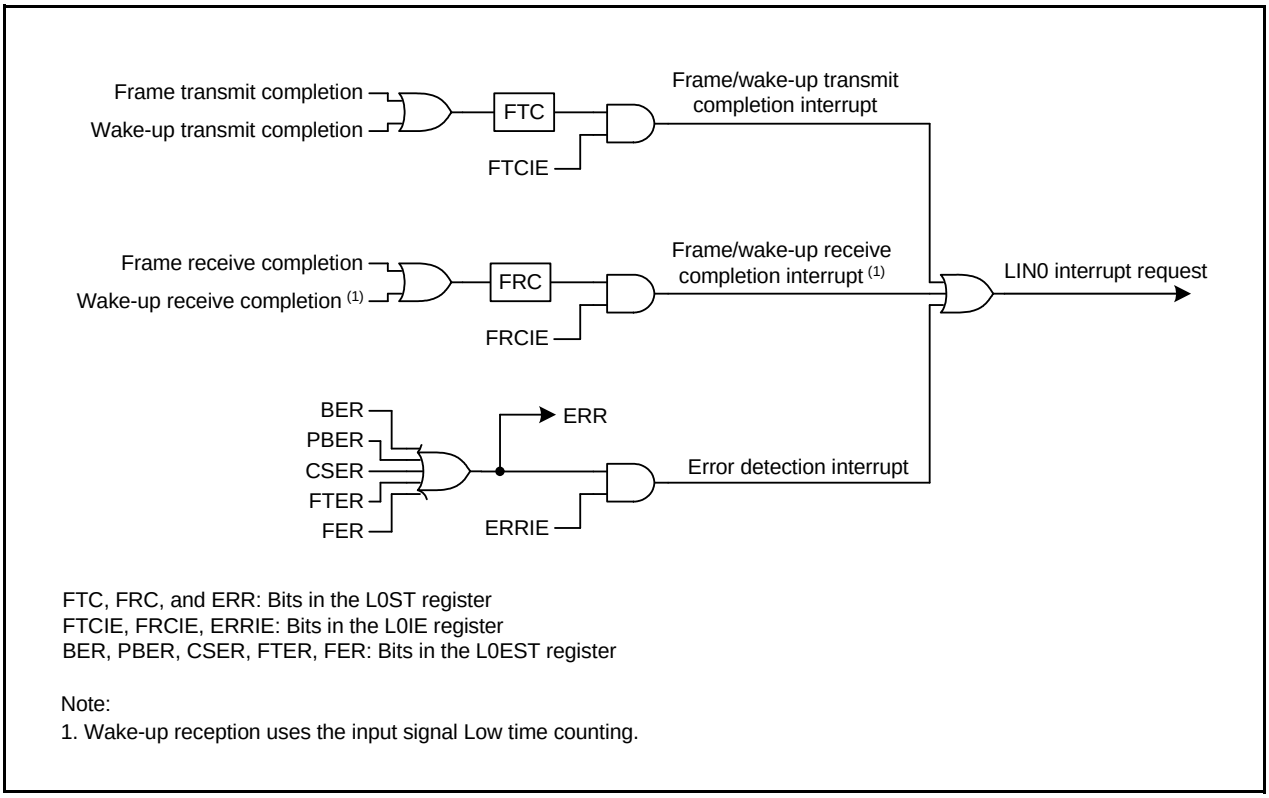
24.10 LIN Interrupt

The interrupts requests generated by the LIN module are LIN0 interrupt and LIN0 Low detection interrupt. The channel has four sources for these interrupts as follows: frame receive/wake-up receive (input signal Low time counting) completion, error detection, and LIN0 Low detection.

Among the four interrupt sources above, interrupt requests by the former three interrupt sources are aggregated by logical OR, and output LIN0 interrupt request. Each channel has an interrupt request generated by LIN0 Low detection.

The respective interrupt request is output when the corresponding flag in the L0ST register becomes 1 while the corresponding bit in the L0IE register is set to 1 (interrupt enabled).

Figure 24.36 shows the block diagram of the LIN0 interrupt. For details on the LIN0 Low detection interrupt, refer to 12. “Interrupts”.



FTC, FRC, and ERR: Bits in the L0ST register
FTCIE, FRCIE, ERRIE: Bits in the L0IE register
BER, PBER, CSER, FTER, FER: Bits in the L0EST register

Note:
1. Wake-up reception uses the input signal Low time counting.

Figure 24.36 LIN0 Interrupt Block Diagram

24.11 LIN Self-test Mode

The LIN module has LIN self-test mode. Once the LIN module enters LIN self-test mode, it is disconnected from the LIN bus, and the internal LIN0OUT is looped back to the internal LIN0IN (loop back).

LIN self-test mode operates in the following states.

- In LIN self-test mode
- Wake-up is not supported
- Frame separate mode is not supported
- The baud rate generator is set to the fastest settings (LBRP0 register is 00h, LBRP1 register is 00h, LCKS bit in the L0MD register is 00b (fa is selected as the LIN system clock.))

Do not enter LIN wake-up mode.

Before entering LIN self-test mode, set the FSM bit in the L0RFC register to 0 (non-frame separate mode).

In LIN self-test mode, operations are performed with the fastest speed setting of the baud rate generator.

Registers associated with the baud rate setting can be written, but the written value has no effect on the operation.

Registers L0ST and L0EST are functional, but bits BER, PBER, and FER in the L0EST register cannot be used.

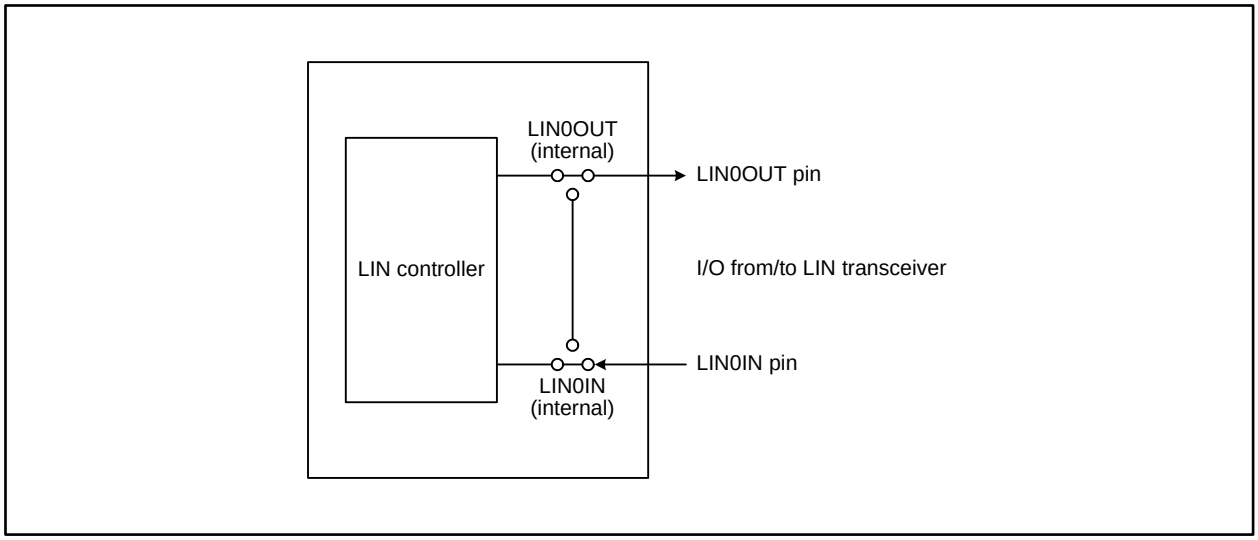


Figure 24.37 LIN Operation Mode Connection

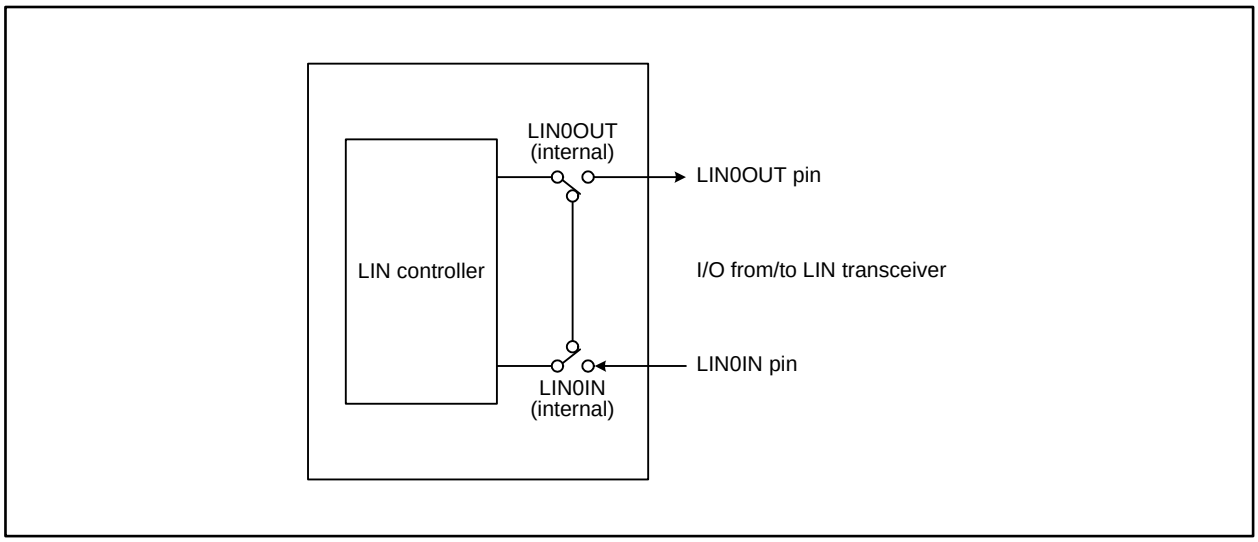


Figure 24.38 LIN Self-test Mode Connection

24.11.1 Entry into LIN Self-test Mode

To enter LIN self-test mode, a particular key sequence must be used. For this key sequence, write operation to the LSTC register has to be performed three times continuously.

(1) Transition to LIN reset mode
Set the OM0 bit in the L0C register to 0 (LIN reset mode).
Read the OMM0 bit in the L0MST register and check whether the value is 0 (LIN reset mode).
(2) Write A7h to the LSTC register (first written value).
(3) Write 58h to the LSTC register (second written value).
(4) Write 01h to the LSTC register (third written value).
(5) Confirm the transition to LIN self-test mode.
Read the LSTM bit in the LSTC register and confirm the value is 1 (LIN self-test mode).

If the first key (A7h) is written twice incorrectly, the transition to LIN self-test mode is canceled. Restart writing from the first key again. If the write operation is performed to the other LIN associated registers during this write operation (write operation to the LSTC register three times continuously), the transition is also canceled.

LIN self-test mode does not support frame separate mode. Two tests can be carried out.

- LIN self-test mode (transmission): Header transmission and response transmission
- LIN self-test mode (reception): Header transmission and response reception

24.11.2 Transmission in LIN Self-test Mode

To execute LIN self-test, perform the following:

(1) Write 11b to bits OM1 and OM0 in the L0C register (LIN operation mode).
(2) Read bits OMM1 and OMM0 in the L0MST register, and confirm the value is 11b (LIN operation mode).
(3) Set the RFT bit in the L0RFC register to 1 (transmission).
(4) Set the frame configuration for transmission.
(5) Set the FTS bit in the L0TC register to 1 (frame transmission/wake-up transmission and reception started).
The LIN module starts LIN self-test mode (transmission), and updates the interrupt request, status, and error status. The checksum is automatically calculated by the LIN module.
(6) Check the LIN module operation
When a transmission is completed, the inverted value of the loop back frame data is stored in registers L0IDB, L0CB, and L0DBn (inverted value is stored to compare the transmitted value and the loop back value). If a transmission is not completed due to an error, the corresponding error flag is updated.

24.11.3 Reception in LIN Self-test Mode

To execute LIN self-test, perform the following:

(1) Write 11b to bits OM1 and OM0 in the L0C register (LIN operation mode).
(2) Read bits OMM1 and OMM0 in the L0MST register, and confirm the value is 11b (LIN operation mode).
(3) Set the RFT bit in the L0RFC register to 0 (reception).
(4) Set the frame configuration for reception.
A checksum error can be tested by setting an unexpected checksum value in the L0CB register.
(5) Set the FTS bit in the L0TC register to 1 (frame transmission/wake-up transmission and reception started).
The LIN module starts LIN self-test mode (reception), and updates the interrupt request, status, and error status.
(6) Check the LIN module operation
When a reception is completed, the inverted value of the loop back frame data is stored in registers L0IDB, L0CB, and L0DBn. If a reception is not completed due to an error, the corresponding error flag is updated.

24.11.4 Exit from LIN Self-test Mode

To exit LIN self-test mode, perform the following:

(1) Write 0 to the OM0 bit in the L0C register (LIN reset mode).
When bits OMM1 to OMM0 in the L0MST register are not 11b (LIN operation mode), write 11b to bits OM1 to OM0 in the L0C register. Then confirm bits OMM1 to OMM0 are set to 11b before entering LIN reset mode.
(2) Confirm that LIN reset mode is released.
Read the LSTM bit in the LSTC register and confirm the value is 0 (Mode other than LIN self-test mode).
(3) Confirm the transition to LIN reset mode.
Read the OMM0 bit in the L0MST register and confirm the value is 0 (LIN reset mode).

24.12 Notes on LIN Module

24.12.1 Influence of $\overline{SD}$

When a low-level signal is applied to the $\overline{SD}$ pin while the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on $\overline{SD}$ pin enabled), the following pins become high-impedance: P7_2/CLK2/TA1OUT/V/RXD1, P7_3/$\overline{CTS2}$/$\overline{RTS2}$/TA1IN/$\overline{V}$/TXD1, P7_4/TA2OUT/W/LIN0OUT, P7_5/TA2IN/$\overline{W}$/LIN0IN, P8_0/TA4OUT/U/TSUDA, P8_1/TA4IN/$\overline{U}$/TSUDB

25. CAN Module

Note

Do not use CAN function in the M16C/57 Group.
In CAN module 1 channel version in the M16C/5M Group, use CAN0 not CAN1.

The M16C/5M Group implements up to two channels (referred to as CAN0 and CAN1) of the Controller Area Network (CAN) module that complies with the ISO11898-1 Specifications. The CAN module transmits and receives both formats of messages, namely the standard identifier (11 bits) (identifier hereafter referred to as ID) and extended ID (29 bits).
Tables 25.1 and 25.2 list the CAN module specifications, and Figure 25.1 shows the CAN module block diagram.
Connect the CAN bus transceiver externally.

Table 25.1 CAN Module Specifications (1)

Item	Specification
Protocol	ISO11898-1 compliant
Bit rate	Up to 1 Mbps
Message boxes	32 mailboxes: Two selectable mailbox modes: • Normal mailbox mode All 32 mailboxes can be configured for transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for transmission or reception. The remaining mailboxes can be configured as 4-stage FIFO for transmission and 4-stage FIFO for reception.
Reception	• Data frames and remote frames can be received. • Selectable receiving ID format (only standard ID, only extended ID, or both ID) • Programmable one-shot reception function • Selectable overwrite mode (message overwritten) or overrun mode (message discarded) • The reception complete interrupt can be individually enabled or disabled for each mailbox.
Acceptance filtering	8 acceptance masks: one mask every 4 mailboxes The mask can be individually enabled or disabled for each mailbox.
Transmission	• Data frame and remote frame can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID, or both ID). • Programmable one-shot transmission function • Selectable ID priority transmit mode or mailbox number priority transmit mode • Transmission request can be aborted. (The completion of abort can be confirmed with a flag.) • The transmission complete interrupt can be individually enabled or disabled for each mailbox.
Mode transition for bus-off recovery	Mode transition for the recovery from the bus-off state can be selected: • ISO11898-1 compliant • Automatic entry to CAN halt mode at bus-off entry • Automatic entry to CAN halt mode at bus-off end • Entry to CAN halt mode by a program • Transition to the error-active state by a program

Table 25.2 CAN Module Specifications (2)

Item	Specification
Error status monitoring	• CAN bus errors (stuff error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition to error states can be detected (error-warning, error-passive, bus-off entry, and bus-off recovery). • The error counters can be read.
Time stamp function	Time stamp function using a 16-bit counter The reference clock can be selected from either 1-, 2-, 4- or 8-bit time periods.
Interrupt sources	6 types: • Reception complete • Transmission complete • Receive FIFO • Transmit FIFO • Error • Wake-up
CAN sleep mode	Current consumption can be reduced by stopping the CAN clock.
Software support units	3 software support units: • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support
CAN clock source	Selectable BCLK or main clock
Test mode	3 test modes available for user evaluation: • Listen-only mode • Self-test mode 0 (external loop back) • Self-test mode 1 (internal loop back)

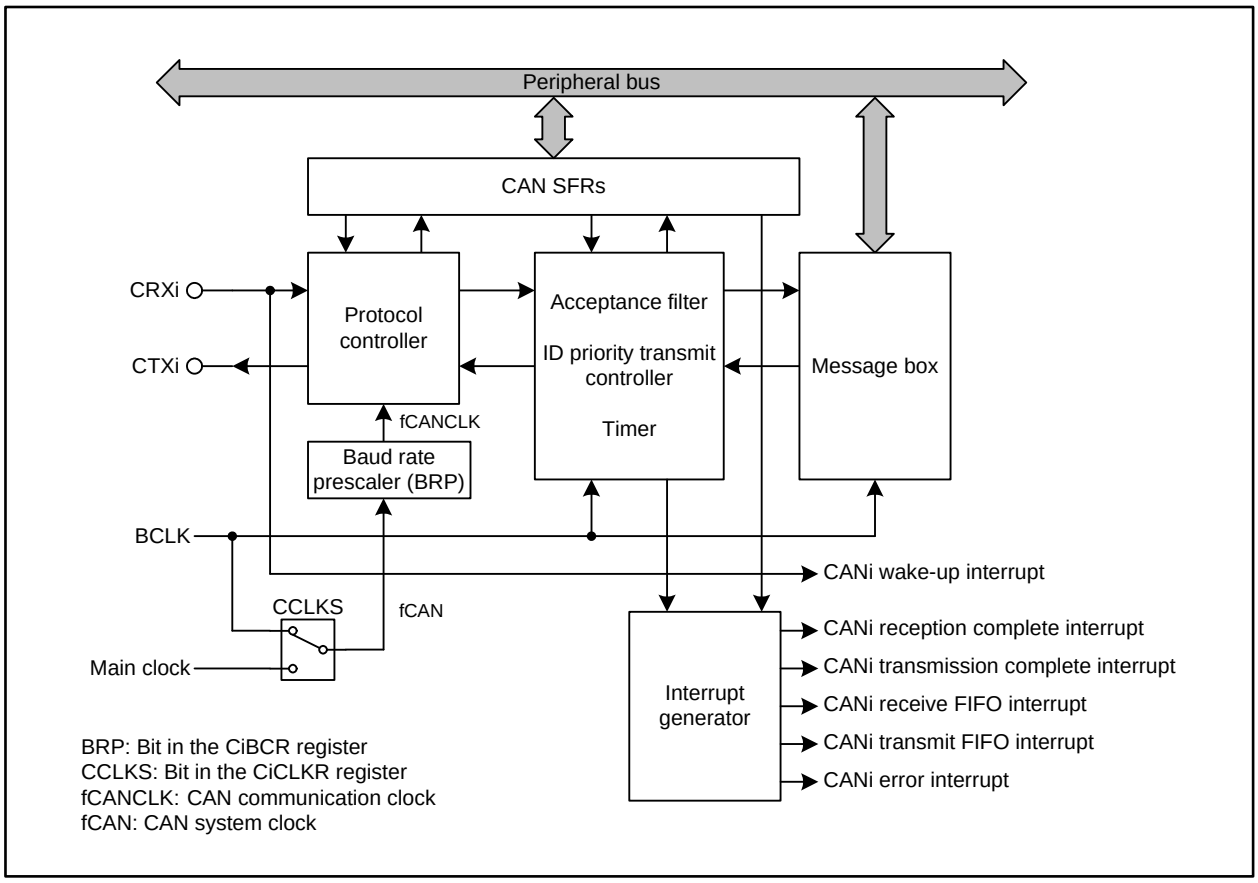


Figure 25.1 CAN Module Block Diagram (i = 0, 1)

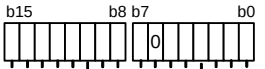
- CRXi/CTXi (i = 0, 1): CAN input/output pins
- Protocol controller: Handles CAN protocol processing such as bus arbitration, bit timing at transmission and reception, stuffing, and error handling, etc.
- Message box: Consists of 32 mailboxes which can be configured as either transmit or receive mailboxes. Each mailbox has an individual ID, data length code, a data field (8 bytes), and a time stamp.
- Acceptance filter: Performs filtering of received messages. Registers CiMKR0 to CiMKR7 are used for the filtering process.
- Timer: Used for the time stamp function. The timer value when storing a message into the mailbox is written as the time stamp value.
- Wake-up function: Generates a CANi wake-up interrupt request when a message is detected on the CAN bus.
- Interrupt generator: Generates the following five types of interrupts:
  - CANi reception complete interrupt
  - CANi transmission complete interrupt
  - CANi receive FIFO interrupt
  - CANi transmit FIFO interrupt
  - CANi error interrupt
- CAN SFRs: CAN-associated registers. Refer to 25.1 “CAN SFRs” for details.

25.1 CAN SFRs

The CAN-associated registers are shown in Figures 25.2 to 25.11, 25.13, 25.14, 25.16 to 25.20, 25.22, and 25.24 to 25.30.

25.1.1 CANi Control Register (CiCTLR) (i = 0, 1)

CANi Control Register (i = 0, 1)



Symbol	Address	Reset Value
C0CTLR	D7C1h-D7C0h	0000 0000 0000 0101b
C1CTLR	D4C1h-D4C0h	0000 0000 0000 0101b

Bit Symbol	Bit Name	Function	RW
CANM	CAN Operating Mode Select Bit (1)	b1 b0 0 0 : CAN operation mode 0 1 : CAN reset mode 1 0 : CAN halt mode 1 1 : Do not use this combination	RW
SLPM	CAN Sleep Mode Bit (1, 2)	0: Other than CAN sleep mode 1: CAN sleep mode	RW
BOM	Bus-Off Recovery Mode Select Bit (3)	b4 b3 0 0 : Normal mode (ISO11898-1 compliant) 0 1: Entry to CAN halt mode automatically at bus-off entry 1 0 : Entry to CAN halt mode automatically at bus-off end 1 1 : Entry to CAN halt mode (during bus-off recovery period) by a program request	RW
RBOC	Forcible Return From Bus-Off Bit (4)	0: Nothing occurred 1: Forcible return from bus-off (5)	RW
— (b6)	Reserved	Set to 0.	RW
CPE	CAN Port Enable Bit (3)	0: Function as I/O ports 1: Function as CAN I/O	RW
MBM	CAN Mailbox Mode Select Bit (3)	0: Normal mailbox mode 1: FIFO mailbox mode	RW
IDFM	ID Format Mode Select Bit (3)	b10b9 0 0 : Standard ID mode 0 1 : Extended ID mode 1 0 : Mixed ID mode 1 1 : Do not use this combination	RW
MLM	Message Lost Mode Select Bit (3)	0: Overwrite mode 1: Overrun mode	RW
TPM	Transmit Priority Mode Select Bit (3)	0: ID priority transmit mode 1: Mailbox number priority transmit mode	RW
TSRC	Time Stamp Counter Reset Bit (6)	0: Nothing occurred 1: Reset (5)	RW
TSPS	Time Stamp Prescaler Select Bit (3)	b15b14 0 0 : Every bit time 0 1 : Every 2-bit time 1 0 : Every 4-bit time 1 1 : Every 8-bit time	RW

Notes:
1. When bits CANM and SLPM are changed, check the CiSTR register to ensure that the mode has been switched. Do not change bits CANM and SLPM until the mode has been switched. Change the frequency of the CPU clock or BCLK in any mode other than CAN operation mode.
2. Write to the SLPM bit in CAN sleep mode, CAN reset mode, or CAN halt mode. When rewriting the SLPM bit, set only this bit to 0 or 1.
3. Write to bits BOM, CPE, MBM, IDFM, MLM, TPM, and TSPS in CAN reset mode.
4. Set the RBOC bit to 1 in bus-off state.
5. Bits RBOC and TSRC are automatically set back to 0 after being set to 1. It should be read as 0.
6. Set the TSRC bit to 1 in CAN operation mode.

Figure 25.2 Registers C0CTLR to C1CTLR

25.1.1.1 CANM Bit

The CANM bit selects one of the following modes for the CAN module: CAN operation mode, CAN reset mode, or CAN halt mode. Refer to 25.2 “Operating Mode” for details.
CAN sleep mode is set by the SLPM bit.
Do not set the CANM bit to 11b.
When the CAN module enters CAN halt mode according to the setting of the BOM bit, the CANM bit is automatically set to 10b.

25.1.1.2 SLPM Bit

When the SLPM bit is set to 1, the CAN module enters CAN sleep mode.
When this bit is set to 0, the CAN module exits CAN sleep mode.
Refer to 25.2 “Operating Mode” for details.

25.1.1.3 BOM Bit

The BOM bit is used to select bus-off recovery mode.

When the BOM bit is 00b, the recovery from bus-off is compliant with ISO11898-1, i.e. the CAN module reenters CAN communication (error-active state) after detecting 11 consecutive recessive bits 128 times. A bus-off recovery interrupt request is generated when recovering from bus-off.

When the BOM bit is 01b, as soon as the CAN module reaches the bus-off state, the CANM bit in the CiCTLR register (i = 0, 1) is set to 10b (CAN halt mode) and the CAN module enters CAN halt mode. No bus-off recovery interrupt request is generated when recovering from bus-off and registers CiTECR and CiRECR are set to 00h.

When the BOM bit is 10b, the CANM bit is set to 10b as soon as the CAN module reaches the bus-off state. The CAN module enters CAN halt mode after the recovery from the bus-off state, i.e. after detecting 11 consecutive recessive bits 128 times. A bus-off recovery interrupt request is generated when recovering from bus-off and registers CiTECR and CiRECR are set to 00h.

When the BOM bit is 11b, the CAN module enters CAN halt mode by setting the CANM bit to 10b while the CAN module is still in bus-off state. No bus-off recovery interrupt request is generated when recovering from bus-off and registers CiTECR and CiRECR are set to 00h. However, if the CAN module recovers from bus-off after detecting 11 consecutive recessive bits 128 times before the CANM bit is set to10b, a bus-off recovery interrupt request is generated.

If the CPU requests an entry to CAN reset mode at the same time as the CAN module attempts to enter CAN halt mode (at bus-off entry when the BOM bit is 01b, or at bus-off end when the BOM bit is 10b), then the CPU request to enter CAN reset mode has higher priority.

25.1.1.4 RBOC Bit

When the RBOC bit is set to 1 (force return from bus-off) in bus-off state, the CAN module forcibly returns from the bus-off state. This bit is automatically set to 0. The error state changes from bus-off to error-active.

When the RBOC bit is set to 1, registers CiRECR and CiTECR are set to 00h and the BOST bit in the CiSTR register is set to 0 (the CAN module is not in bus-off state). The other registers remain unchanged. No bus-off recovery interrupt request is generated by this recovery from the bus-off state.
Use the RBOC bit only when the BOM bit is 00b (normal mode).

25.1.1.5 CPE Bit

When the CPE bit is set to 1, the function of the CAN I/O pins (CRXi and CTRi (i = 0, 1)) is enabled. To use the CAN module, set this bit to 1.
To set the CPE bit to 1, set the port direction bit corresponding to the CRXi pin to 0.
When the CPE bit is set to 0, the function of the port I/O pins is enabled.
Write to the CPE bit only in CAN reset mode.
To use a CAN wake-up interrupt, set the CPE bit to 1.

25.1.1.6 MBM Bit

When the MBM bit is 0 (normal mailbox mode), mailboxes [0] to [31] are configured as transmit or receive mailboxes.
When this bit is 1 (FIFO mailbox mode), mailboxes [0] to [23] are configured as transmit or receive mailboxes. Mailboxes [24] to [27] are configured as a transmit FIFO and mailboxes [28] to [31] as a receive FIFO.
Transmit data is written into mailbox [24] (mailbox [24] is a window mailbox for the transmit FIFO).
Receive data is read from mailbox [28] (mailbox [28] is a window mailbox for the receive FIFO).
Table 25.3 lists the mailbox configuration.

Table 25.3 Mailbox Configuration

Mailbox	MBM = 0 (Normal Mailbox Mode)	MBM = 1 (1) (FIFO Mailbox Mode)
Mailboxes [0] to [23]	Normal mailbox	Normal mailbox
Mailboxes [24] to [27]		Transmit FIFO
Mailboxes [28] to [31]		Receive FIFO

Note:
1. When the MBM bit is set to 1, note the following:
   - Transmit FIFO is controlled by the CiTFCR register.
     The CiMCTLj register (j = 0 to 31) for mailboxes [24] to [27] is disabled.
     Registers CiMCTL24 to CiMCTL27 cannot be used.
   - Receive FIFO is controlled by the CiRFCR register.
     The CiMCTLj register for mailboxes [28] to [31] is disabled.
     Registers CiMCTL28 to CiMCTL31 cannot be used.
   - Refer to the CiMIER register about the FIFO interrupts.
   - The corresponding bits in the CiMKIVLR register for mailboxes [24] to [31] are disabled. Set 0 to these bits.
   - Transmit/receive FIFOs can be used for both data frames and remote frames.

25.1.1.7 IDFM Bit

The IDFM bit specifies the ID format.
When this bit is 00b, all mailboxes (including FIFO mailboxes) handle only standard IDs.
When this bit is 01b, all mailboxes (including FIFO mailboxes) handle only extended IDs.
When this bit is 10b, all mailboxes (including FIFO mailboxes) handle both standard IDs and extended IDs. Standard IDs or extended IDs are specified by using the IDE bit in the corresponding mailbox in normal mailbox mode. In FIFO mailbox mode, the IDE bit in the corresponding mailbox is used for mailboxes [0] to [23], the IDE bit in registers CiFIDCR0 and CiFIDCR1 is used for the receive FIFO, and the IDE bit in mailbox [24] is used for the transmit FIFO.
Do not set 11b to the IDFM bit.

25.1.1.8 MLM Bit

The MLM bit specifies the operation when a new message is captured in the unread mailbox.
Overwrite mode or overrun mode can be selected. All mailboxes (including the receive FIFO) are set to either overwrite mode or overrun mode.

When the MLM bit is 0, all mailboxes are set to overwrite mode and the new message is overwriting the old message.
When this bit is 1, all mailboxes are set to overrun mode and the new message is discarded.

25.1.1.9 TPM Bit

The TPM bit specifies the priority of modes when transmitting messages.
ID priority transmit mode or mailbox number transmit mode can be selected.
All mailboxes are set for either ID priority transmission or mailbox number priority transmission.

When the TPM bit is 0, ID priority transmit mode is selected and transmission priority complies with the CAN bus arbitration rule, as defined in the ISO 11898-1 Specifications. In ID priority transmit mode, mailboxes [0] to [31] (in normal mailbox mode), and mailboxes [0] to [23] (in FIFO mailbox mode), and the transmit FIFO are compared for the IDs of mailboxes configured for transmission. If two or more mailbox IDs are the same, the mailbox with the smaller number has higher priority.

Only the next message to be transmitted from the transmit FIFO is included in the transmission arbitration. If a transmit FIFO message is being transmitted, the next pending message within the transmit FIFO is included in the transmission arbitration.

When the TPM bit is 1, mailbox number transmit mode is selected and the transmit mailbox with the smallest mailbox number has the highest priority. In FIFO mailbox mode, the transmit FIFO has lower priority than normal mailboxes (mailboxes [0] to [23]).

25.1.1.10 TSRC Bit

The TSRC bit is used to reset the time stamp counter.
When this bit is set to 1, the CiTSR register (i = 0, 1) is set to 0000h. It is automatically set to 0.

25.1.1.11 TSPS Bit

The TSPS bit selects the prescaler for the time stamp.
The reference clock for the time stamp can be selected from 1-, 2-, 4- or 8-bit time periods.

25.1.2 CANi Clock Select Register (CiCLKR) (i = 0, 1)

CANi Clock Select Register (i = 0, 1)

b7	b6	b5	b4	b3	b2	b1	b0
0	X	X	0	0	X	0	

Symbol	Address	Reset Value
C0CLKR	D7C7h	00h
C1CLKR	D4C7h	00h

Bit Symbol	Bit Name	Function	RW
CCLKS	CAN Clock Source Select Bit (1)	0: BCLK 1: Main clock (2)	RW
— (b1)	Reserved	Set to 0.	RW
— (b2)	No register bit. If necessary, set to 0. The read value is 0.		—
— (b3)	Reserved	Set to 0.	RW
— (b4)	Reserved	Set to 0. The read value is undefined.	RW
— (b6-b5)	No register bits. If necessary, set to 0. The read value is 0.		—
— (b7)	Reserved	Set to 0.	RW

Notes:
1. Write to the CCLKS bit in CAN reset mode.
2. To set the CCLKS bit to 1, the frequency of the BCLK should be equal to or higher than the frequency of the main clock.

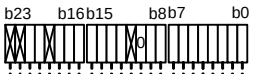
Figure 25.3 Registers C0CLKR to C1CLKR

25.1.2.1 CCLKS Bit

When the CCLKS bit is set to 0, the CAN clock source (fCAN) originates from the PLL.
When this bit is set to 1, fCAN originates directly from the external XIN pin bypassing the PLL.

25.1.3 CANi Bit Configuration Register (CiBCR) (i = 0, 1)

CANi Bit Configuration Register (i = 0, 1) (1, 2)



Symbol	Address	Reset Value
C0BCR	D7C6h-D7C4h	00 0000h
C1BCR	D4C6h-D4C4h	00 0000h

Bit Symbol	Bit Name	Function	RW
BRP	Prescaler Division Ratio Set Bit (10 bits)	If the setting value is P (0 to 1023), the baud rate prescaler divides fCAN by P + 1	RW
— (b10)	Reserved	Set to 0.	RW
— (b11)	No register bit. If necessary, set to 0. The read value is 0.		—
TSEG1	Time Segment 1 Control Bit	b15b14b13b12 0 0 0 0 : Do not use this combination 0 0 0 1 : Do not use this combination 0 0 1 0 : Do not use this combination 0 0 1 1 : 4 Tq 0 1 0 0 : 5 Tq 0 1 0 1 : 6 Tq 0 1 1 0 : 7 Tq 0 1 1 1 : 8 Tq 1 0 0 0 : 9 Tq 1 0 0 1 : 10 Tq 1 0 1 0 : 11 Tq 1 0 1 1 : 12 Tq 1 1 0 0 : 13 Tq 1 1 0 1 : 14 Tq 1 1 1 0 : 15 Tq 1 1 1 1 : 16 Tq	RW
TSEG2	Time Segment 2 Control Bit	b18b17b16 0 0 0 : Do not use this combination 0 0 1 : 2 Tq 0 1 0 : 3 Tq 0 1 1 : 4 Tq 1 0 0 : 5 Tq 1 0 1 : 6 Tq 1 1 0 : 7 Tq 1 1 1 : 8 Tq	RW
— (b19)	No register bit. If necessary, set to 0. The read value is 0.		—
SJW	Resynchronization Jump Width Control Bit	b21b20 0 0 : 1 Tq 0 1 : 2 Tq 1 0 : 3 Tq 1 1 : 4 Tq	RW
— (b23-22)	No register bits. If necessary, set to 0. The read value is 0.		—

Notes:
1. Set the CiBCR register before entering CAN halt mode from CAN reset mode or CAN operation mode from CAN reset mode. After the setting is made once, this register can be written to in CAN reset mode or CAN halt mode.
2. The CiBCR register consists of 24 bits. A 32-bit read/write access should be performed carefully not to rewrite the CiCLKR register.

Figure 25.4 Registers C0BCR to C1BCR

Refer to 25.3 “CAN Communication Speed Configuration” about the bit timing configuration.

25.1.3.1 BRP Bit

The BRP bit is used to set the frequency of the CAN communication clock (fCANCLK).
The cycle of fCANCLK is set to be 1 Time Quantum (Tq).

25.1.3.2 TSEG1 Bit

The TSEG1 bit is used to specify the total length of the propagation time segment (PROP_SEG) and phase buffer segment 1 (PHASE_SEG1) with the value of Tq.
A value from 4 to 16 time quanta can be set.

25.1.3.3 TSEG2 Bit

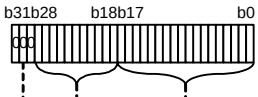
The TSEG2 bit is used to specify the length of phase buffer segment TSEG2 (PHASE_SEG2) with the value of Tq.
A value from 2 to 8 time quanta can be set.
Set the value smaller than that of the TSEG1 bit.

25.1.3.4 SJW Bit

The SJW bit is used to specify the resynchronization jump width with the value of Tq.
A value from 1 to 4 time quanta can be set.
Set the value smaller than or equal to that of the TSEG2 bit.

25.1.4 CANi Mask Register k (CiMKRk) (i = 0, 1; k = 0 to 7)

CANi Mask Register k (i = 0, 1; k = 0 to 7) (1)



Symbol	Address	Reset Value
C0MKR0, C0MKR1	D703h-D700h, D707h-D704h	Undefined
C0MKR2, C0MKR3	D70Bh-D708h, D70Fh-D70Ch	Undefined
C0MKR4, C0MKR5	D713h-D710h, D717h-D714h	Undefined
C0MKR6, C0MKR7	D71Bh-D718h, D71Fh-D71Ch	Undefined
C1MKR0, C1MKR1	D403h-D400h, D407h-D404h	Undefined
C1MKR2, C1MKR3	D40Bh-D408h, D40Fh-D40Ch	Undefined
C1MKR4, C1MKR5	D413h-D410h, D417h-D414h	Undefined
C1MKR6, C1MKR7	D41Bh-D418h, D41Fh-D41Ch	Undefined

Bit Symbol	Bit Name	Function	RW
EID	Extended ID Bit	0: Corresponding EID bit is not compared 1: Corresponding EID bit is compared	RW
SID	Standard ID Bit	0: Corresponding SID bit is not compared 1: Corresponding SID bit is compared	RW
— (b31-b29)	Reserved	Set to 0.	RW

Note:
1. Write to registers CiMKR0 to CiMKR7 in CAN reset mode or CAN halt mode.

Figure 25.5 Registers C0MKR0 to C1MKR7

Refer to 25.5 “Acceptance Filtering and Masking Function” about the masking function in FIFO mailbox mode.

25.1.4.1 EID Bit

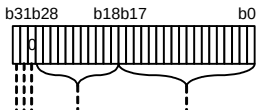
The EID bit is the filter mask bit corresponding to the CAN extended ID bit. This bit is used to receive extended ID messages.
When the EID bit is 0, the corresponding EID bit is not compared for the received ID and the mailbox ID.
When this bit is 1, the corresponding EID bit is compared for the received ID and the mailbox ID.

25.1.4.2 SID Bit

The SID bit is the filter mask bit corresponding to the CAN standard ID bit. This bit is used to receive both standard ID and extended ID messages.
When the SID bit is 0, the corresponding SID bit is not compared for the received ID and the mailbox ID.
When this bit is 1, the corresponding SID bit is compared for the received ID and the mailbox ID.

25.1.5 CANi FIFO Received ID Compare Register n (CiFIDCR0 to CiFIDCR1) (i = 0, 1; n = 0, 1)

CANi FIFO Received ID Compare Register n (i = 0, 1; n = 0, 1) (1)



Symbol	Address	Reset Value
C0FIDCR0	D723h-D720h	Undefined
C0FIDCR1	D727h-D724h	Undefined
C1FIDCR0	D423h-D420h	Undefined
C1FIDCR1	D427h-D424h	Undefined

Bit Symbol	Bit Name	Function	RW
EID	Extended ID Bit	0: Corresponding EID bit is 0 1: Corresponding EID bit is 1	RW
SID	Standard ID Bit	0: Corresponding SID bit is 0 1: Corresponding SID bit is 1	RW
— (b29)	Reserved	Set to 0.	RW
RTR	Remote Frame Request Bit	0: Data frame 1: Remote frame	RW
IDE	ID Extension Bit (2)	0: Standard ID 1: Extended ID	RW

Notes:
1. Write to registers CiFIDCR0 and CiFIDCR1 in CAN reset mode or CAN halt mode.
2. The IDE bit is enabled when the IDFM bit in the CiCTLR register is 10b (mixed ID mode). When the IDFM bit is not 10b, set the IDE bit to 0.

Figure 25.6 Registers C0FIDCR0 to C1FIDCR1

Registers CiFIDCR0 and CiFIDCR1 are enabled when the MBM bit in the CiCTLR register is set to 1 (FIFO mailbox mode). Bits EID, SID, RTR, and IDE in registers CiMB28 to CiMB31 are disabled. Refer to 25.5 “Acceptance Filtering and Masking Function” about the usage of these registers.

25.1.5.1 EID Bit

The EID bit sets the extended ID of data frames and remote frames. This bit is used to receive extended ID messages.

25.1.5.2 SID Bit

The SID bit sets the standard ID of data frames and remote frames. This bit is used to receive both standard ID and extended ID messages.

25.1.5.3 RTR Bit

The RTR bit sets the specified frame format of data frames or remote frames.
This bit specifies the following operation:

- When both RTR bits in registers CiFIDCR0 and CiFIDCR1 (i = 0, 1) are set to 0, only data frames can be received.
- When both RTR bits in registers CiFIDCR0 and CiFIDCR1 are set to 1, only remote frames can be received.
- When the RTR bits in registers CiFIDCR0 and CiFIDCR1 are set to 0 or 1 individually, both data frames and remote frames can be received.

25.1.5.4 IDE bit

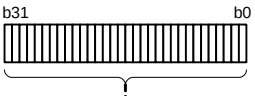
The IDE bit sets the ID format of standard ID or extended ID.
This bit is enabled when the IDFM bit in the CiCTLR register is 10b (mixed ID mode).
When the IDFM bit is 10b, the IDE bit specifies the following operation:

- When both IDE bits in registers CiFIDCR0 and CiFIDCR1 are set to 0, only standard ID frames can be received.
- When both IDE bits in registers CiFIDCR0 and CiFIDCR1 are set to 1, only extended ID frames can be received.
- When the IDE bits in registers CiFIDCR0 and CiFIDCR1 are set to 0 or 1 individually, both standard ID and extended ID frames can be received.

25.1.6 CANi Mask Invalid Register (CiMKIVLR) (i = 0, 1)

CANi Mask Invalid Register (i = 0, 1) (1)

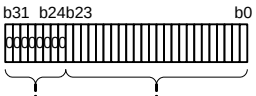
Normal mailbox mode



Symbol	Address	Reset Value
C0MKIVLR	D72Bh-D728h	Undefined
C1MKIVLR	D42Bh-D428h	Undefined

Bit Symbol	Bit Name	Function	RW
— (b31-b0)	Mask Invalid Bit	0: Mask valid 1: Mask invalid	RW

FIFO mailbox mode



Bit Symbol	Bit Name	Function	RW
— (b23-b0)	Mask Invalid Bit	0: Mask valid 1: Mask invalid	RW
— (b31-b24)	Reserved	Set to 0.	RW

Note:
1. Write to the CiMKIVLR register in CAN reset mode or CAN halt mode.

Figure 25.7 Registers C0MKIVLR to C1MKIVLR

Each bit corresponds to the mailbox with the same number. When each bit is 1, the acceptance mask for the mailbox corresponding to the bit number is disabled. In this case, a receiving message is stored into the mailbox only if its ID matches bits SID and EID in the CiMBj register (j = 0 to 31).

25.1.7 CANi Mailbox Register j (CiMBj) (i = 0, 1; j = 0 to 31)

Table 25.4 lists the CANi mailbox memory mapping, and Table 25.5 lists the CAN data frame structure. The value after reset of CANi mailbox is undefined.

Table 25.4 CANi Mailbox Memory Mapping (i = 0, 1)

Address		Message Content
CAN0	CAN1	Memory Mapping
D500h + j * 16 + 0	D200h + j * 16 + 0	EID7 to EID0
D500h + j * 16 + 1	D200h + j * 16 + 1	EID15 to EID8
D500h + j * 16 + 2	D200h + j * 16 + 2	SID5 to SID0, EID17, EID16
D500h + j * 16 + 3	D200h + j * 16 + 3	IDE, RTR, SID10 to SID6
D500h + j * 16 + 4	D200h + j * 16 + 4	—
D500h + j * 16 + 5	D200h + j * 16 + 5	Data length code (DLC)
D500h + j * 16 + 6	D200h + j * 16 + 6	Data byte 0
D500h + j * 16 + 7 : : : D500h + j * 16 + 13	D200h + j * 16 + 7 : : : D200h + j * 16 + 13	Data byte 1 : : : Data byte 7
D500h + j * 16 + 14	D200h + j * 16 + 14	Time stamp lower byte
D500h + j * 16 + 15	D200h + j * 16 + 15	Time stamp upper byte

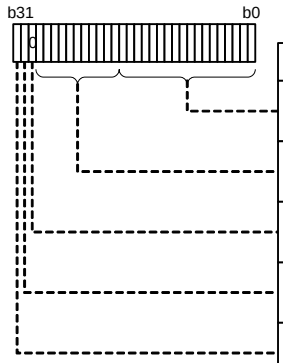
j: Mailbox number (j = 0 to 31)

Table 25.5 CAN Data Frame Structure

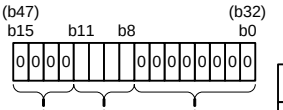
SID10 to SID6	SID5 to SID0	EID17 to EID16	EID15 to EID8	EID7 to EID0	DLC3 to DLC0	DATA0	DATA1	.....	DATA7

CANi Mailbox Register j (i = 0, 1; j = 0 to 31) (1)

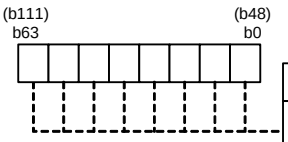
Symbol	Address (2)	Reset Value
C0MB0 to C0MB31	D500h to D6FFh	Undefined
C1MB0 to C1MB31	D200h to D3FFh	Undefined



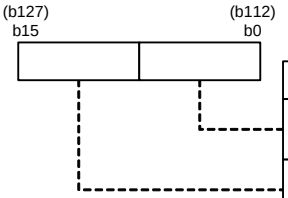
Bit Symbol	Bit Name	Function	RW
EID	Extended ID (3)	0: Corresponding EID bit is 0 1: Corresponding EID bit is 1	RW
SID	Standard ID	0: Corresponding SID bit is 0 1: Corresponding SID bit is 1	RW
— (b29)	Reserved	Set to 0.	RW
RTR	Remote Frame Request Bit	0: Data frame 1: Remote frame	RW
IDE	ID Extension Bit (4)	0: Standard ID 1: Extended ID	RW



Bit Symbol	Bit Name	Setting Value	RW
— (b7-b0)	Reserved	Set to 0.	RW
DLC	Data Length Code (5)	0h to Fh	RW
— (b15-b12)	Reserved	Set to 0.	RW



Symbol	Name	Setting Value	RW
DATA0 to DATA7	Data Bytes 0 to 7 (5, 6)	00 to FFh	RW



Symbol	Name	Setting Value	RW
TSL	Time Stamp Lower Byte	00 to FFh	RW
TSH	Time Stamp Higher Byte	00 to FFh	RW

Notes:
1. Write to the CiMBj register only when the associated CiMCTLj register is 00h and the corresponding mailbox is not processing an abort request.
2. Refer to Table 25.4 “CANi Mailbox Memory Mapping” for detailed addresses.
3. If the mailbox has received a standard ID message, the EID bit in the mailbox is undefined.
4. The IDE bit is enabled when the IDFM bit in the CiCTLR register is 10b (mixed ID mode). When the IDFM bit is not 10b, set to 0.
5. If the mailbox has received a message with n bytes less than 8 bytes, the values of DATAn to DATA7 in the mailbox are undefined.
6. If the mailbox has received a remote frame, the previous values of DATA0 to DATA7 in the mailbox are retained.

Figure 25.8 Registers C0MBj to C1MBj

The previous value of each mailbox is retained unless a new message is received.

25.1.7.1 EID Bit

The EID bit sets the extended ID of data frames and remote frames. This bit is used to transmit or receive extended ID messages.

25.1.7.2 SID Bit

The SID bit sets the standard ID of data frames and remote frames. This bit is used to transmit or receive both standard ID and extended ID messages.

25.1.7.3 RTR Bit

The RTR bit sets the frame format of data frames or remote frames.
This bit specifies the following operation:

- Receive mailbox receives only frames with the format specified by the RTR bit.
- Transmit mailbox transmits according to the frame format specified by the RTR bit.
- Receive FIFO mailbox receives the data frame, remote frame, or both frames specified by the RTR bit in registers CiFIDCR0 and CiFIDCR1 (i = 0, 1).
- Transmit FIFO mailbox transmits the data frame or remote frame specified by the RTR bit in the relevant transmitting message.

25.1.7.4 IDE Bit

The IDE bit sets the ID format of standard IDs or extended IDs.
This bit is enabled when the IDFM bit in the CiCTLR register is 10b (mixed ID mode).
When the IDFM bit is 10b, the IDE bit specifies the following operation:

- Receive mailbox receives only the ID format specified by the IDE bit.
- Transmit mailbox transmits according to the ID format specified by the IDE bit.
- Receive FIFO mailbox receives messages with the standard ID, extended ID, or both IDs specified by the IDE bit in registers CiFIDCR0 and CiFIDCR1.
- Transmit FIFO mailbox transmits messages with the standard ID or extended ID specified by the IDE bit in the relevant transmitting message.

25.1.7.5 DLC (Data Length Code)

The DLC is used to set the number of data bytes to be transmitted in a data frame. When data is requested using a remote frame, the number of data bytes to be requested is set.
When a data frame is received, the number of received data bytes is stored. When a remote frame is received, the number of requested data bytes is stored.
Table 25.6 lists the data length corresponding DLC.

Table 25.6 Data Length Corresponding DLC

DLC[3]	DLC[2]	DLC[1]	DLC[0]	Data Length
0	0	0	0	0 byte
0	0	0	1	1 byte
0	0	1	0	2 bytes
0	0	1	1	3 bytes
0	1	0	0	4 bytes
0	1	0	1	5 bytes
0	1	1	0	6 bytes
0	1	1	1	7 bytes
1	-	-	-	8 bytes

-: Any value

25.1.7.6 DATA0 to DATA7

DATA0 to DATA7 store the transmitted or received CAN message data. Transmission or reception starts from DATA0. The bit order on the CAN bus is MSB first, and transmission or reception starts from bit 7.

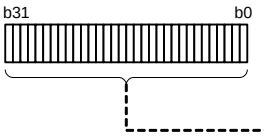
25.1.7.7 TSL and TSH

TSL and TSH store the counter value of the time stamp when received messages are stored in the mailbox.

25.1.8 CANi Mailbox Interrupt Enable Register (CiMIER) (i = 0, 1)

CANi Mailbox Interrupt Enable Register (i = 0, 1) (1, 2)

Normal mailbox mode



Symbol	Address	Reset Value
C0MIER	D72Fh-D72Ch	Undefined
C1MIER	D42Fh-D42Ch	Undefined

Bit Symbol	Bit Name	Function	RW
— (b31-b0)	Interrupt Enable Bit	0: Interrupt disabled 1: Interrupt enabled	RW

FIFO mailbox mode

Bit Symbol	Bit Name	Function	RW
— (b23-b0)	Interrupt Enable Bit	0: Interrupt disabled 1: Interrupt enabled	RW
— (b24)	Transmit FIFO Interrupt Enable Bit	0: Interrupt disabled 1: Interrupt enabled	RW
— (b25)	Transmit FIFO Interrupt Generation Timing Control Bit	Transmit FIFO interrupt request is generated 0: Every time transmission is completed 1: When transmit FIFO becomes empty due to completion of transmission	RW
— (b27-b26)	Reserved	Set to 0.	RW
— (b28)	Receive FIFO Interrupt Enable Bit	0: Interrupt disabled 1: Interrupt enabled	RW
— (b29)	Receive FIFO Interrupt Generation Timing Control Bit	Receive FIFO interrupt request is generated 0: Every time reception is completed 1: When receive FIFO becomes buffer warning by completion of reception (3)	RW
— (b31-b30)	Reserved	Set to 0.	RW

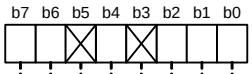
Notes:
1. Write to the CiMIER register only when the associated CiMCTLj register (j = 0 to 31) is 00h and the corresponding mailbox is not processing a transmission or reception abort request.
2. In FIFO mailbox mode, change the bits in the CiMIER register for the associated FIFO only when:
   - The TFE bit in the CiTFCR register is 0 and the TFEST bit is 1, and
   - The RFE bit in the CiRFCR register is 0 and the RFEST bit is 1.
3. No interrupt request is generated when the receive FIFO becomes buffer warning from full.

Figure 25.9 Registers C0MIER to C1MIER

Interrupts can enabled individually for each mailbox.
In normal mailbox mode (bits 0 to 31) and in FIFO mailbox mode (bits 0 to 23), each bit corresponds to the mailbox with the same number. These bits enable or disable transmission/reception complete interrupts for the corresponding mailboxes.
In FIFO mailbox mode, bits 24, 25, 28, and 29 specify whether transmit/receive FIFO interrupts are enabled/disabled and timing when interrupt requests are generated.
“Buffer warning” indicates a state in which the third unread message is stored in the receive FIFO.

25.1.9 CANi Message Control Register (CiMCTLj) (i = 0, 1; j = 0 to 31)

CANi Message Control Register j (i = 0,1; j = 0 to 31) (1, 2)



Symbol	Address	Reset Value
C0MCTL0 to C0MCTL31	D7A0h to D7BFh	00h
C1MCTL0 to C1MCTL31	D4A0h to D4BFh	00h

Bit Symbol	Bit Name	Function	RW
When the TRMREQ bit is 0 and the RECREQ bit is 1			
NEWDATA	Reception Complete Flag (3, 4)	0: No data has been received or 0 is written to the NEWDATA bit 1: A new message is being stored or has been stored to the mailbox	RW
INVALDATA	Reception-in-Progress Status Flag	0: Message valid 1: Message being updated	RO
MSGLOST	Message Lost Flag (3, 4)	0: Message is not overwritten or overrun 1: Message is overwritten or overrun	RW
When the TRMREQ bit is 1 and the RECREQ bit is 0			
SENTDATA	Transmission Complete Flag (3, 4)	0: Transmission is not completed (pending) 1: Transmission is completed (success)	RW
TRMACTIVE	Transmission-in-Progress Status Flag	0: Transmission is pending or transmission is not requested 1: From acceptance of transmission request to completion of transmission, or error/arbitration lost	RO
TRMABT	Transmission Abort Complete Flag (3, 4)	0: Transmission has started, transmission abort failed because transmission is completed, or transmission abort is not requested 1: Transmission abort is completed	RW
— (b3)	No register bit. If necessary, set to 0. The read value is 0.		—
ONESHOT	One-shot Enable Bit (5)	0: One-shot reception or one-shot transmission disabled 1: One-shot reception or one-shot transmission enabled	RW
— (b5)	No register bit. If necessary, set to 0. The read value is 0.		—
RECREQ	Receive Mailbox Set Bit (4, 6, 7)	0: Not configured for reception 1: Configured for reception	RW
TRMREQ	Transmit Mailbox Set Bit (4, 6)	0: Not configured for transmission 1: Configured for transmission	RW

Notes:
1. Write to the CiMCTLj register in CAN operation mode or CAN halt mode.
2. Do not use registers CiMCTL24 to CiMCTL31 in FIFO mailbox mode.
3. Write 0 only. Writing 1 has no effect.
4. When writing 0 to bits NEWDATA, SENTDATA, MSGLOST, TRMABT, RECREQ, and TRMREQ by a program, use the MOV instruction to ensure that only the specified bit is set to 0 and the other bits are set to 1.
5. To enter one-shot receive mode, write 1 to the ONESHOT bit at the same time as setting the RECREQ bit to 1. To exit one-shot receive mode, write 0 to the ONESHOT bit after writing 0 to the the RECREQ bit and confirming it has been set to 0.
   To enter one-shot transmit mode, write 1 to the ONESHOT bit at the same time as setting the TRMREQ bit to 1. To exit one-shot transmit mode, write 0 to the ONESHOT bit after the message has been transmitted or aborted.
6. Do not set both the RECREQ and TRMREQ bits to 1.
7. When setting the RECREQ bit to 0, set bits MSGLOST, NEWDATA, RECREQ to 0 simultaneously.

Figure 25.10 Registers C0MCTLj to C1MCTLj

25.1.9.1 NEWDATA Bit

The NEWDATA bit is set to 1 when a new message is being stored or has been stored to the mailbox.
The timing for setting this bit to 1 is simultaneous with the INVALDATA bit.
The NEWDATA bit is set to 0 by writing 0 by a program.
This bit cannot be set to 0 by writing 0 by a program while the related INVALDATA bit is 1.

25.1.9.2 SENTDATA Bit

The SENTDATA bit is set to 1 when data transmission from the corresponding mailbox is completed.
This bit is set to 0 by writing 0 by a program.
To set the SENTDATA bit to 0, first set the TRMREQ bit to 0.
Bits SENTDATA and TRMREQ cannot be set to 0 simultaneously.
To transmit a new message from the corresponding mailbox, set the SENTDATA bit to 0.

25.1.9.3 INVALDATA Bit

After the completion of a message reception, the INVALDATA bit is set to 1 while the received message is being updated into the corresponding mailbox.
This bit is set to 0 immediately after the message has been stored. If the mailbox is read while this bit is 1, the data is undefined.

25.1.9.4 TRMACTIVE Bit

The TRMACTIVE bit is set to 1 when the corresponding mailbox of the CAN module begins transmitting a message.
This bit is set to 0 when the CAN module has lost CAN bus arbitration, a CAN bus error occurs, or data transmission is completed.

25.1.9.5 MSGLOST Bit

The MSGLOST bit is set to 1 when the mailbox is overwritten or overrun by a new received message while the NEWDATA bit is 1. The MSGLOST bit is set to 1 at the end of the sixth bit of EOF.
This bit is set to 0 by writing 0 by a program.
In both overwrite and overrun modes, this bit cannot be set to 0 by writing 0 by a program during five cycles of fCAN (CAN system clock) following the sixth bit of EOF.

25.1.9.6 TRMABT Bit

The TRMABT bit is set to 1 in the following cases:

- Following a transmission abort request, when the transmission abort is completed before starting transmission.
- Following a transmission abort request, when the CAN module detects CAN bus arbitration lost or a CAN bus error.
- In one-shot transmission mode (RECREQ bit = 0, TRMREQ bit = 1, and ONESHOT bit = 1), when the CAN module detects CAN bus arbitration lost or a CAN bus error.

The TRMABT bit is not set to 1 when data transmission is completed. In this case, the SENTDATA bit is set to 1.
The TRMABT bit is set to 0 by writing 0 by a program.

25.1.9.7 ONESHOT Bit

The ONESHOT bit can be used in the following two ways, receive mode and transmit mode:

(1) One-Shot Receive Mode

When the ONESHOT bit is set to 1 in receive mode (RECREQ bit = 1 and TRMREQ bit = 0), the mailbox receives a message only one time. The mailbox does not behave as a receive mailbox after having received a message one time. The behavior of bits NEWDATA and INVALDATA is the same as in normal reception mode. In one-shot receive mode, the MSGLOST bit is not set to 1.
To set the ONESHOT bit to 0, first write 0 to the RECREQ bit and ensure that it has been set to 0.

(2) One-Shot Transmit Mode

When the ONESHOT bit is set to 1 in transmit mode (RECREQ bit = 0 and TRMREQ bit = 1), the CAN module transmits a message only one time. The CAN module does not transmit the message again if a CAN bus error or CAN bus arbitration lost occurs. When transmission is completed, the SENTDATA bit is set to 1. If transmission is not completed due to a CAN bus error or CAN bus arbitration lost, the TRMABT bit is set to 1.
Set the ONESHOT bit to 0 after the SENTDATA or TRMABT bit is set to 1.

25.1.9.8 RECREQ Bit

The RECREQ bit selects receive modes shown in Table 25.11.
When the RECREQ bit is set to 1, the corresponding mailbox is configured for reception of a data frame or a remote frame.
When this bit is set to 0, the corresponding mailbox is not configured for reception of a data frame or a remote frame.
Due to hardware protection, the RECREQ bit cannot be set to 0 by writing 0 by a program during the following period:
Hardware protection is started
- From the acceptance filter procedure (the beginning of the CRC field)

Hardware protection is released
- For the mailbox that is specified to receive the incoming message, after the received data is stored into the mailbox or a CAN bus error occurs (i.e. a maximum period of hardware protection is from the beginning of the CRC field to the end of the seventh bit of EOF).
- For the other mailboxes, after the acceptance filter procedure.
- If no mailbox is specified to receive the message, after the acceptance filter procedure.

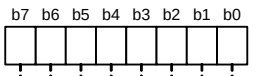
When setting the RECREQ bit to 1, do not set 1 to the TRMREQ bit.
To change the configuration of a mailbox from transmission to reception, first abort the transmission and then set bits SENTDATA and TRMABT to 0 before changing to reception.

25.1.9.9 TRMREQ Bit

The TRMREQ bit selects transmit modes shown in Table 25.11.
When this bit is set to 1, the corresponding mailbox is configured for transmission of a data frame or a remote frame.
When this bit is set to 0, the corresponding mailbox is not configured for transmission of a data frame or a remote frame.
If the TRMREQ bit is changed from 1 to 0 to cancel the corresponding transmission request, either the TRMABT or SENTDATA bit is set to 1.
When setting the TRMREQ bit to 1, do not set the RECREQ bit to 1.
To change the configuration of a mailbox from reception to transmission, first abort the reception and then set bits NEWDATA and MSGLOST to 0 before changing to transmission.

25.1.10 CANi Receive FIFO Control Register (CiRFCR) (i = 0, 1)

CANi Receive FIFO Control Register (i = 0, 1) (1)



Symbol	Address	Reset Value
C0RFCR	D7C8h	1000 0000b
C1RFCR	D4C8h	1000 0000b

Bit Symbol	Bit Name	Function	RW
RFE	Receive FIFO Enable Bit (2)	0: Receive FIFO disabled 1: Receive FIFO enabled	RW
RFUST	Receive FIFO Unread Message Number Status Bit	b3 b2 b1 0 0 0 : No unread message 0 0 1 : 1 unread message 0 1 0 : 2 unread messages 0 1 1 : 3 unread messages 1 0 0 : 4 unread messages 1 0 1 : Reserved 1 1 0 : Reserved 1 1 1 : Reserved	RO
RFMLF	Receive FIFO Message Lost Flag (3)	0: No receive FIFO message lost has occurred 1: Receive FIFO message lost has occurred	RW
RFFST	Receive FIFO Full Status Bit	0: Receive FIFO is not full 1: Receive FIFO is full (4 unread messages)	RO
RFWST	Receive FIFO Buffer Warning Status Bit	0: Receive FIFO is not buffer warning 1: Receive FIFO is buffer warning (3 unread messages)	RO
RFEST	Receive FIFO Empty Status Bit	0: Unread message in receive FIFO 1: No unread message in receive FIFO	RO

Notes:
1. Write to the CiRFCR register in CAN operation mode or CAN halt mode.
2. Write 0 to the RFE bit simultaneously with the RFMLF bit.
3. Write 0 only. Writing 1 has no effect.

Figure 25.11 Registers C0RFCR to C1RFCR

25.1.10.1 RFE Bit

When the RFE bit is set to 1, the receive FIFO is enabled.
When this bit is set to 0, the receive FIFO is disabled for reception and becomes empty (RFEST bit = 1).
Do not set this bit to 1 in normal mailbox mode (MBM bit in the CiCTLR register (i = 0, 1) = 0).
Due to hardware protection, the RFE bit is not set to 0 by writing 0 by a program during the following period:
Hardware protection is started

- From the acceptance filter procedure (the beginning of the CRC field)

Hardware protection is released

- If the receive FIFO is specified to receive the incoming message, after the received data is stored into the receive FIFO or a CAN bus error occurs. (i.e. a maximum period of hardware protection is from the beginning of the CRC field to the end of the seventh bit of EOF.)
- If the receive FIFO is not specified to receive the message, after the acceptance filter procedure.

25.1.10.2 RFUST Bit

The RFUST bit indicates the number of unread messages in the receive FIFO.
The value of this bit is initialized to 000b when the RFE bit is set to 0.

25.1.10.3 RFMLF Bit

The RFMLF bit is set to 1 (receive FIFO message lost has occurred) when the receive FIFO receives a new message and the receive FIFO is full. The timing for setting this bit to 1 is at the end of the sixth bit of EOF.
The RFMLF bit is set to 0 by writing 0 by a program.
In both overwrite and overrun modes, this bit cannot be set to 0 (receive FIFO message lost has not occurred) by writing 0 by a program due to hardware protection during the five cycles of fCAN following the sixth bit of EOF, if the receive FIFO is full and determined to receive the message.

25.1.10.4 RFFST Bit

The RFFST bit is set to 1 (receive FIFO is full) when the number of unread messages in the receive FIFO is 4. This bit is set to 0 (receive FIFO is not full) when the number of unread messages in the receive FIFO is less than 4. This bit is set to 0 when the RFE bit is 0.

25.1.10.5 RFWST Bit

The RFWST bit is set to 1 (receive FIFO is buffer warning) when the number of unread messages in the receive FIFO is 3. This bit is set to 0 (receive FIFO is not buffer warning) when the number of unread messages in the receive FIFO is less than 3 or equal to 4. This bit is set to 0 when the RFE bit is 0.

25.1.10.6 RFEST Bit

The RFEST bit is 1 (no unread message in receive FIFO) when the number of unread messages in the receive FIFO is 0. This bit is set to 1 when the RFE bit is set to 0. The RFEST bit is set to 0 (unread message in receive FIFO) when the number of unread messages in the receive FIFO is one or more.

Figure 25.12 shows the receive FIFO mailbox operation.

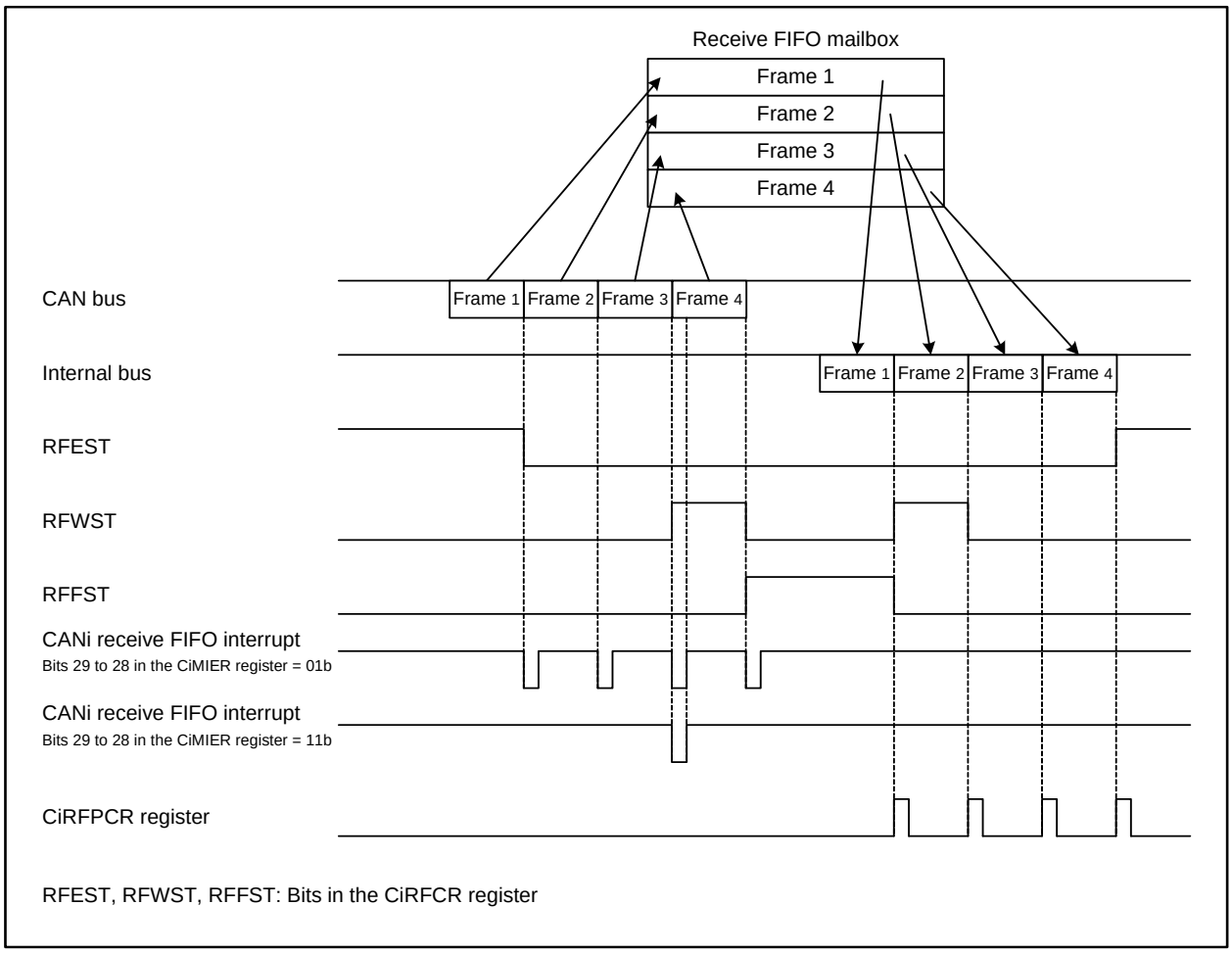


Figure 25.12 Receive FIFO Mailbox Operation (Bits 29 and 28 in CiMIER Register = 01b and 11b) (i = 0, 1)

25.1.11 CANi Receive FIFO Pointer Control Register (CiRFPCR) (i = 0, 1)

CANi Receive FIFO Pointer Control Register (i = 0, 1)

b7 b0

Symbol	Address	Reset Value
C0RFPCR	D7C9h	Undefined
C1RFPCR	D4C9h	Undefined

Function	Setting Value	RW
The CPU-side pointer for the receive FIFO is incremented by writing FFh	FFh	WO

Figure 25.13 Registers C0RFPCR to C1RFPCR

When the receive FIFO is not empty, write FFh to the CiRFPCR register by a program to increment the CPU-side pointer for the receive FIFO to the next mailbox location.
Do not write to the CiRFPCR register when the RFE bit in the CiRFCR register is 0 (receive FIFO disabled).
Both the CAN-side pointer and the CPU-side pointer are incremented when a new message is received and the RFFST bit is 1 (receive FIFO is full) in overwrite mode. When the RFMLF bit is 1 in this condition, the CPU-side pointer cannot be incremented by writing to the CiRFPCR register by a program.

25.1.12 CANi Transmit FIFO Control Register (CiTFCR) (i = 0, 1)

CANi Transmit FIFO Control Register (i = 0, 1) (1)

b7	b6	b5	b4	b3	b2	b1	b0
		0	X				

Symbol	Address	Reset Value
C0TFCR	D7CAh	1000 0000b
C1TFCR	D4CAh	1000 0000b

Bit Symbol	Bit Name	Function	RW
TFE	Transmit FIFO Enable Bit	0: Transmit FIFO disabled 1: Transmit FIFO enabled	RW
TFUST	Transmit FIFO Unsent Message Number Status Bit	b3 b2 b1 0 0 0 : No unsent message 0 0 1 : 1 unsent message 0 1 0 : 2 unsent messages 0 1 1 : 3 unsent messages 1 0 0 : 4 unsent messages 1 0 1 : Reserved 1 1 0 : Reserved 1 1 1 : Reserved	RO
— (b4)	No register bit. If necessary, set to 0. The read value is 0.		—
— (b5)	Reserved	If necessary, set to 0. The read value is undefined.	RO
TFFST	Transmit FIFO Full Status Bit	0: Transmit FIFO is not full 1: Transmit FIFO is full (4 unsent messages)	RO
TFEST	Transmit FIFO Empty Status Bit	0: Unsent message in transmit FIFO 1: No unsent message in transmit FIFO	RO

Note:
1. Write to the CiTFCR register in CAN operation mode or CAN halt mode.

Figure 25.14 Registers C0TFCR to C1TFCR

25.1.12.1 TFE Bit

When the TFE bit is set to 1, the transmit FIFO is enabled.
When this bit is set to 0, the transmit FIFO becomes empty (TFEST bit = 1) and then unsent messages from the transmit FIFO are lost as described below:

- If a message from the transmit FIFO is not scheduled for the next transmission or during transmission.
- Following the completion of transmission, a CAN bus error, CAN bus arbitration lost, or entry to CAN halt mode if a message from the transmit FIFO is scheduled for the next transmission or already during transmission.

Before setting the TFE bit to set to 1 again, ensure that the TFEST bit has been set to 1.
After setting the TFE bit to 1, write transmit data into the CiMB24 register.
Do not set this bit to 1 in normal mailbox mode (MBM bit in the CiCTLR register = 0).

25.1.12.2 TFUST Bit

The TFUST bit indicates the number of unsent messages in the transmit FIFO.
After the TFE bit is set to 0, the value of the TFUST bit is initialized to 000b when transmission abort or transmission is completed.

25.1.12.3 TFFST Bit

The TFFST bit is set to 1 (transmit FIFO is full) when the number of unsent messages in the transmit FIFO is 4. This bit is set to 0 (transmit FIFO is not full) when the number of unsent messages in the transmit FIFO is less than 4. This bit is set to 0 when transmission from the transmit FIFO has been aborted.

25.1.12.4 TFEST Bit

The TFEST bit is set to 1 (no message in transmit FIFO) when the number of unsent messages in the transmit FIFO is 0. This bit is set to 1 when transmission from the transmit FIFO has been aborted.
The TFEST bit is set to 0 (message in transmit FIFO) when the number of unsent messages in the transmit FIFO is not 0.

Figure 25.15 shows the transmit FIFO mailbox operation.

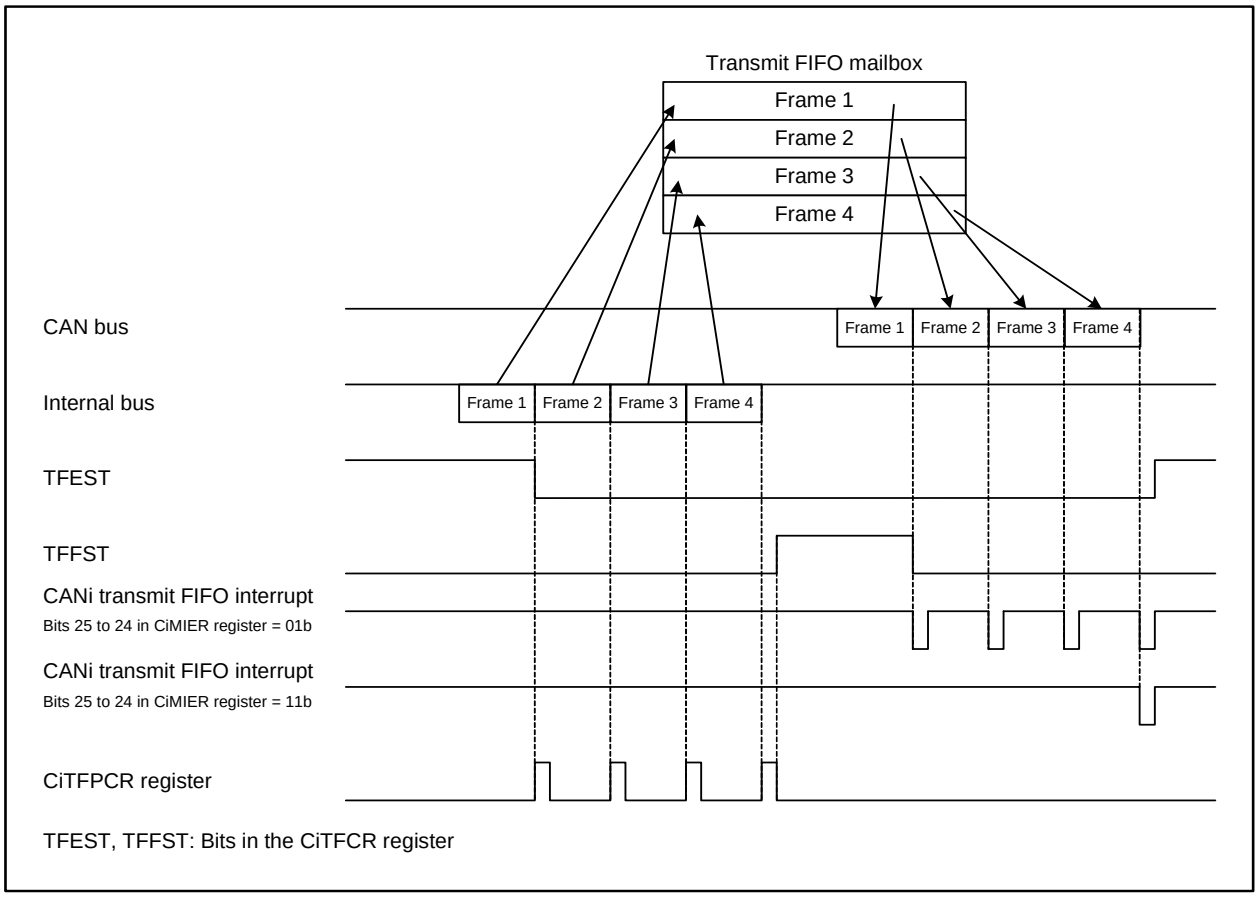


Figure 25.15 Transmit FIFO Mailbox Operation (Bits 25 and 24 in CiMIER Register = 01b and 11b) (i = 0, 1)

25.1.13 CANi Transmit FIFO Pointer Control Register (CiTFPCR) (i = 0, 1)

CANi Transmit FIFO Pointer Control Register (i = 0, 1)

b7 b0

Symbol	Address	Reset Value
C0TFPCR	D7CBh	Undefined
C1TFPCR	D4CBh	Undefined

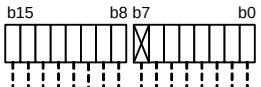
Function	Setting Value	RW
The CPU-side pointer for the transmit FIFO is incremented by writing FFh	FFh	WO

Figure 25.16 Registers C0TFPCR to C1TFPCR

When the transmit FIFO is not full, write FFh to the CiTFPCR register by a program to increment the CPU-side pointer for the transmit FIFO to the next mailbox location.
Do not write to the CiTFPCR register when the TFE bit in the CiTFPCR register is 0 (transmit FIFO disabled).

25.1.14 CANi Status Register (CiSTR) (i = 0, 1)

CANi Status Register (i = 0, 1)



Symbol	Address	Reset Value
C0STR	D7C3h-D7C2h	0000 0000 0000 0101b
C1STR	D4C3h-D4C2h	0000 0000 0000 0101b

Bit Symbol	Bit Name	Function	RW
RSTST	CAN Reset Status Flag	0: Not in CAN reset mode 1: In CAN reset mode	RO
HLTST	CAN Halt Status Flag	0: Not in CAN halt mode 1: In CAN halt mode	RO
SLPST	CAN Sleep Status Flag	0: Not in CAN sleep mode 1: In CAN sleep mode	RO
EPST	Error-Passive Status Flag	0: Not in error-passive state 1: In error-passive state	RO
BOST	Bus-Off Status Flag	0: Not in bus-off state 1: In bus-off state	RO
TRMST	Transmit Status Flag (transmitter)	0: Bus idle or reception in progress 1: Transmission in progress or in bus-off state	RO
RECST	Receive Status Flag (receiver)	0: Bus idle or transmission in progress 1: Reception in progress	RO
— (b7)	No register bit. The read value is 0.		—
NDST	NEWDATA Status Flag	0: No mailbox with NEWDATA bit = 1 1: Mailbox(es) with NEWDATA bit = 1	RO
SDST	SENTDATA Status Flag	0: No mailbox with SENTDATA bit = 1 1: Mailbox(es) with SENTDATA bit = 1	RO
RFST	Receive FIFO Status Flag	0: No message in receive FIFO 1: Message in receive FIFO	RO
TFST	Transmit FIFO Status Flag	0: Transmit FIFO is full 1: Transmit FIFO is not full	RO
NMLST	Normal Mailbox Message Lost Status Flag	0: No mailbox with MSGLOST bit = 1 1: Mailbox(es) with MSGLOST bit = 1	RO
FMLST	FIFO Mailbox Message Lost Status Flag	0: RFMLF bit = 0 1: RFMLF bit = 1	RO
TABST	Transmission Abort Status Flag	0: No mailbox with TRMABT bit = 1 1: Mailbox(es) with TRMABT bit = 1	RO
EST	Error Status Flag	0: No error occurred 1: Error occurred	RO

Figure 25.17 Registers C0STR to C1STR

25.1.14.1 RSTST Bit

The RSTST bit is set to 1 when the CAN module is in CAN reset mode.
This bit is set to 0 when the CAN module is not in CAN reset mode.
Even when the state is changed from CAN reset mode to CAN sleep mode, the RSTST bit remains 1.

25.1.14.2 HLTST Bit

The HLTST bit is set to 1 when the CAN module is in CAN halt mode.
This bit is set to 0 when the CAN module is not in CAN halt mode.
Even when the state is changed from CAN halt mode to CAN sleep mode, the HLTST bit remains 1.

25.1.14.3 SLPST Bit

The SLPST bit is set to 1 when the CAN module is in CAN sleep mode.
This bit is set to 0 when the CAN module is not in CAN sleep mode.

25.1.14.4 EPST Bit

The EPST bit is set to 1 when the value of the CiTECR or CiRECR register (i = 0, 1) exceeds 127 and the CAN module is in error-passive state ($128 \leq TEC < 256$ or $128 \leq REC < 256$). This bit is set to 0 when the CAN module is not in error-passive state.
TEC indicates the value of the transmit error counter (CiTECR register) and REC indicates the value of the receive error counter (CiRECR register).

25.1.14.5 BOST Bit

The BOST bit is set to 1 when the value of the CiTECR register exceeds 255 and the CAN module is in bus-off state ($TEC \geq 256$). This bit is set to 0 when the CAN module is not in bus-off state.

25.1.14.6 TRMST Bit

The TRMST bit is set to 1 when the CAN module performs as a transmitter node or is in bus-off state.
This bit is set to 0 when the CAN module performs as a receiver node or is in bus-idle state.

25.1.14.7 RECST Bit

The RECST bit is set to 1 when the CAN module performs as a receiver node.
This bit is set to 0 when the CAN module performs as a transmitter node or is in bus-idle state.

25.1.14.8 NDST Bit

The NDST bit is set to 1 when at least one NEWDATA bit in the CiMCTLj register (j = 0 to 31) is 1 regardless of the value of the CiMIER register.
The NDST bit is set to 0 when all NEWDATA bits are 0.

25.1.14.9 SDST Bit

The SDST bit is set to 1 when at least one SENTDATA bit in the CiMCTLj register (i = 0, 1; j = 0 to 31) is 1 regardless of the value of the CiMIER register.
The SDST bit is set to 0 when all SENTDATA bits are 0.

25.1.14.10 RFST Bit

The RFST bit is set to 1 when the receive FIFO is not empty.
This bit is set to 0 when the receive FIFO is empty.
This bit is set to 0 when normal mailbox mode is selected.

25.1.14.11 TFST Bit

The TFST bit is set to 1 when the transmit FIFO is not full.
This bit is set to 0 when the transmit FIFO is full.
This bit is set to 0 when normal mailbox mode is selected.

25.1.14.12 NMLST Bit

The NMLST bit is set to 1 when at least one MSGLOST bit in the CiMCTLj register is 1 regardless of the value of the CiMIER register.
The NMLST bit is set to 0 when all MSGLOST bits are 0.

25.1.14.13 FMLST Bit

The FMLST bit is set to 1 when the RFMLF bit in the CiRFCR register is 1 regardless of the value of the CiMIER register.
The FMLST bit is set to 0 when the RFMLF bit is 0.

25.1.14.14 TABST Bit

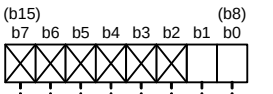
The TABST bit is set to 1 when at least one TRMABT bit in the CiMCTLj register is 1 regardless of the value of the CiMIER register.
The TABST bit is set to 0 when all TRMABT bits are 0.

25.1.14.15 EST Bit

The EST bit is 1 when at least one error is detected by the CiEIFR register regardless of the value of the CiEIER register.
This bit is set to 0 when no error is detected by the CiEIFR register.

25.1.15 CANi Mailbox Search Mode Register (CiMSMR) (i = 0, 1)

CANi Mailbox Search Mode Register (i = 0, 1) (1)



Symbol	Address	Reset Value
C0MSMR	D7D3h	0000 0000b
C1MSMR	D4D3h	0000 0000b

Bit Symbol	Bit Name	Function	RW
MBSM	Mailbox Search Mode Select Bit	b1 b0 0 0 : Receive mailbox search mode 0 1 : Transmit mailbox search mode 1 0 : Message lost search mode 1 1 : Channel search mode	RW
— (b7-b2)	No register bits. If necessary, set to 0. The read value is 0.		—

Note:
1. Write to the CiMSMR register in CAN operation mode or CAN halt mode.

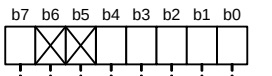
Figure 25.18 Registers C0MSMR to C1MSMR

25.1.15.1 MBSM Bit

The MBSM bit selects the search mode for the mailbox search function.
When this bit is 00b, receive mailbox search mode is selected. In this mode, the search targets are the NEWDATA bit in the CiMCTLj register (j = 0 to 31) for the normal mailbox and the RFEST bit in the CiRFCR register.
When the MBSM bit is 01b, transmit mailbox search mode is selected. In this mode, the search target is the SENTDATA bit in the CiMCTLj register.
When the MBSM bit is 10b, message lost search mode is selected. In this mode, the search targets are the MSGLOST bit in the CiMCTLj register for the normal mailbox and the RFMLF bit in the CiRFCR register.
When the MBSM bit is 11b, channel search mode is selected. In this mode, the search target is the CiCSSR register. Refer to 25.1.17 “CANi Channel Search Support Register (CiCSSR) (i = 0, 1)”.

25.1.16 CANi Mailbox Search Status Register (CiMSSR) (i = 0, 1)

CANi Mailbox Search Status Register (i = 0, 1)



Symbol	Address	Reset Value
C0MSSR	D7D2h	1000 0000b
C1MSSR	D4D2h	1000 0000b

Bit Symbol	Bit Name	Function	RW
MBNST	Search Result Mailbox Number Status Bit	Output of search result in each search mode Output number: 0 to 31	RO
— (b6-b5)	No register bits. If necessary, set to 0. The read value is 0.		—
SEST	Search Result Status Bit	0: Search result found 1: No search result	RO

Figure 25.19 Registers C0MSSR to C1MSSR

25.1.16.1 MBNST Bit

The MBNST bit outputs the smallest mailbox number that is searched in each mode of the CiMSMR register (i = 0, 1).
In receive mailbox, transmit mailbox, and message lost search modes, the value of the mailbox i.e.,the search result to be output, is updated as described below:

- When the NEWDATA, SENTDATA, or MSGLOST bit for the output mailbox is set to 0.
- When the NEWDATA, SENTDATA, or MSGLOST bit for a higher-priority mailbox is set to 1.

In receive mailbox search and message lost search modes, the receive FIFO (mailbox [28]) is output when the receive FIFO is not empty and there are no unread received messages or no lost messages in any of the normal mailboxes (mailboxes [0] to [23]).
In transmit mailbox search mode, the transmit FIFO (mailbox [24]) is not output.
Table 25.7 lists the behavior of MBNST bit in FIFO mailbox mode.

Table 25.7 Behavior of MBNST Bit in FIFO Mailbox Mode

MBSM Bit	Mailbox [24] (Transmit FIFO)	Mailbox [28] (Receive FIFO)
00b	Mailbox [24] is not output.	Mailbox [28] is output when no NEWDATA bit for the normal mailbox is set to 1 and the receive FIFO is not empty.
01b		Mailbox [28] is not output.
10b		Mailbox [28] is output when no MSGLOST bit for the normal mailbox is set to 1 and the RFMLF bit is set to 1 in the receive FIFO.
11b		Mailbox [28] is not output.

In channel search mode, the MBNST bit outputs the corresponding channel number. After the CiMSSR register is read by a program, the next target channel number is output.

25.1.16.2 SEST Bit

The SEST bit is set to 1 when no corresponding mailbox is found after searching all mailboxes.
For example, in transmit mailbox search mode, the SEST bit is set to 1 when no SENTDATA bit for mailboxes is 1. The SEST bit is set to 0 when at lease one SENTDATA bit is 1.
When the SEST bit is 1, the value of the MBNST bit is undefined.

25.1.17 CANi Channel Search Support Register (CiCSSR) (i = 0, 1)

CANi Channel Search Support Register (i = 0, 1) (1, 2)

b7 b0

Symbol	Address	Reset Value
C0CSSR	D7D1h	Undefined
C1CSSR	D4D1h	Undefined

Function	Setting Value	RW
When the value of the channel search is input, the channel number is output to the CiMSSR register	Channel value	RW

Notes:
1. Write to the CiCSSR register only when the MBSM bit in the CiMSMR register is 11b (channel search mode).
2. Write to the CiCSSR register in CAN operation mode or CAN halt mode.

Figure 25.20 Registers C0CSSR to C1CSSR

The bits in the CiCSSR register, which are set to 1, are encoded by an 8/3 encoder (the lower bit position, the higer priority) and output to the MBNST bits in the CiMSSR register.
The CiMSSR register outputs the updated value whenever the CiMSSR register is read by a program.
Figure 25.21 shows the write and read of registers CiCSSR and CiMSSR.

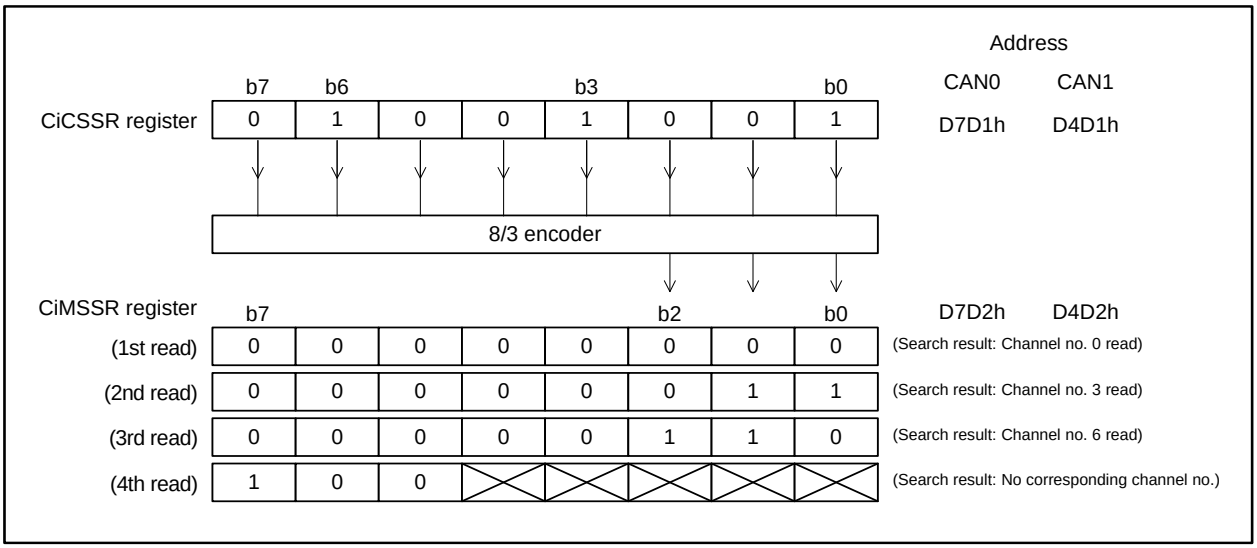
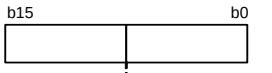


Figure 25.21 Write and Read of Registers CiCSSR and CiMSSR (i = 0, 1)

The value of the CiCSSR register is also updated whenever the CiMSSR register is read. When the CiCSSR register is read, the value before the 8/3 encoder conversion is read.

25.1.18 CANi Acceptance Filter Support Register (CiAFSR) (i = 0, 1)

CANi Acceptance Filter Support Register (i = 0, 1) (1)



Symbol	Address	Reset Value
C0AFSR	D7D7h-D7D6h	Undefined
C1AFSR	D4D7h-D4D6h	Undefined

Function	Setting Value	RW
After the standard ID of a received message is written, the value converted for data table search can be read	Standard ID/ converted value	RW

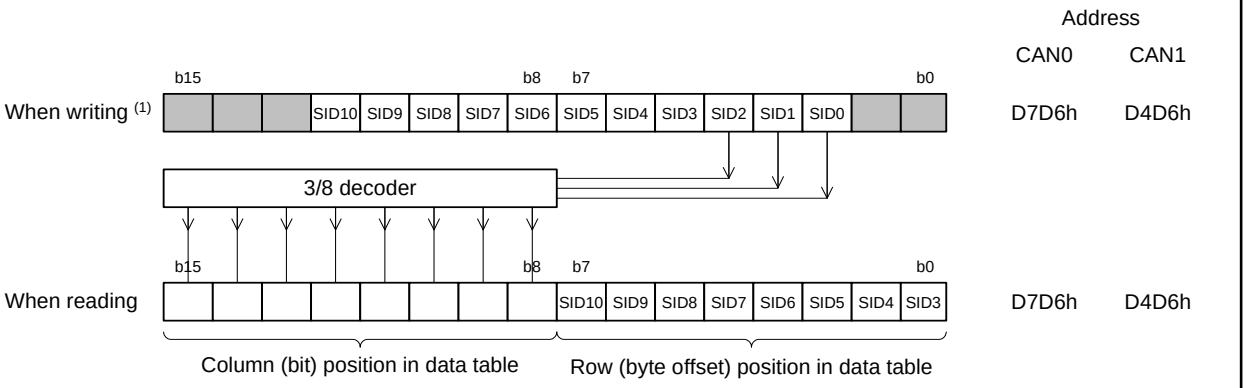
Note:
1. Write to the CiAFSR register in CAN operation mode or CAN halt mode.

Figure 25.22 Registers C0AFSR to C1AFSR

The acceptance filter support unit (ASU) can be used for data table (8 bits × 256) search. In the data table, all standard IDs created by the user are set to be valid/invalid in bit units. When the CAFSR register is written with the 16-bit unit data including the SID bit in the CiMBj register (j = 0 to 31), in which a received ID is stored, a decoded row (byte offset) position and column (bit) position for data table search can be read. The ASU can be used for standard (11-bit) IDs only.
The ASU is enabled in the following cases:

- When the ID to receive cannot be masked by the acceptance filter.
  Example) IDs to receive: 078h, 087h, 111h
- When there are too many IDs to receive and software filtering time is expected to be shortened.

Figure 25.23 shows the write and read of CiAFSR register.

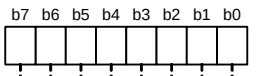


Note:
1. Write the same value as the 16-bit unit data including the SID bit in the CiMBj (j = 0 to 31) register.

Figure 25.23 Write and Read of CiAFSR Register (i = 0, 1)

25.1.19 CANi Error Interrupt Enable Register (CiEIER) (i = 0, 1)

CANi Error Interrupt Enable Register (i = 0, 1) (1)



Symbol	Address	Reset Value
C0EIER	D7CCh	00h
C1EIER	D4CCh	00h

Bit Symbol	Bit Name	Function	RW
BEIE	Bus Error Interrupt Enable Bit	0: Bus error interrupt disabled 1: Bus error interrupt enabled	RW
EWIE	Error Warning Interrupt Enable Bit	0: Error warning interrupt disabled 1: Error warning interrupt enabled	RW
EPIE	Error Passive Interrupt Enable Bit	0: Error passive interrupt disabled 1: Error passive interrupt enabled	RW
BOEIE	Bus-Off Entry Interrupt Enable Bit	0: Bus-off entry interrupt disabled 1: Bus-off entry interrupt enabled	RW
BORIE	Bus-Off Recovery Interrupt Enable Bit	0: Bus-off recovery interrupt disabled 1: Bus-off recovery interrupt enabled	RW
ORIE	Receive Overrun Interrupt Enable Bit	0: Receive overrun interrupt disabled 1: Receive overrun interrupt enabled	RW
OLIE	Overload Frame Transmit Interrupt Enable Bit	0: Overload frame transmit interrupt disabled 1: Overload frame transmit interrupt enabled	RW
BLIE	Bus Lock Interrupt Enable Bit	0: Bus lock interrupt disabled 1: Bus lock interrupt enabled	RW

Note:
1. Write to the CiEIER register in CAN reset mode.

Figure 25.24 Registers C0EIER to C1EIER

The CiEIER register is used to set the error interrupt enabled/disabled individually for each error interrupt source in the CiEIFR register.

25.1.19.1 BEIE Bit

When the BEIE bit is 0, no error interrupt request is generated even if the BEIF bit in the CiEIFR register (i = 0, 1) is set to 1.
When the BEIE bit is 1, an error interrupt request is generated if the BEIF bit is set to 1.

25.1.19.2 EWIE Bit

When the EWIE bit is 0, no error interrupt request is generated even if the EWIF bit in the CiEIFR register is set to 1.
When the EWIE bit is 1, an error interrupt request is generated if the EWIF bit is set to 1.

25.1.19.3 EPIE Bit

When the EPIE bit is 0, no error interrupt request is generated even if the EPIF bit in the CiEIFR register is set to 1.
When the EPIE bit is 1, an error interrupt request is generated if the EPIF bit is set to 1.

25.1.19.4 BOEIE Bit

When the BOEIE bit is 0, no error interrupt request is generated even if the BOEIF bit in the CiEIFR register is set to 1.
When the BOEIE bit is 1, an error interrupt request is generated if the BOEIF bit is set to 1.

25.1.19.5 BORIE Bit

When the BORIE bit is 0, an error interrupt request is not generated even if the BORIF bit in the CiEIFR register is set to 1.
When the BORIE bit is 1, an error interrupt request is generated if the BORIF bit is set to 1.

25.1.19.6 ORIE Bit

When the ORIE bit is 0, no error interrupt request is generated even if the ORIF bit in the CiEIFR register is set to 1.
When the ORIE bit is 1, an error interrupt request is generated if the ORIF bit is set to 1.

25.1.19.7 OLIE Bit

When the OLIE bit is 0, no error interrupt request is generated even if the OLIF bit in the CiEIFR register is set to 1.
When the OLIE bit is 1, an error interrupt request is generated if the OLIF bit is set to 1.

25.1.19.8 BLIE Bit

When the BLIE bit is 0, no error interrupt request is generated even if the BLIF bit in the CiEIFR register is set to 1.
When the BLIE bit is 1, an error interrupt request is generated if the BLIF bit is set to 1.

25.1.20 CANi Error Interrupt Factor Judge Register (CiEIFR) (i = 0, 1)

CANi Error Interrupt Factor Judge Register (i = 0, 1) (1)

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	Reset Value
C0EIFR	D7CDh	00h
C1EIFR	D4CDh	00h

Bit Symbol	Bit Name	Function	RW
BEIF	Bus Error Detect Flag	0: No bus error detected 1: Bus error detected	RW
EWIF	Error Warning Detect Flag	0: No error warning detected 1: Error warning detected	RW
EPIF	Error Passive Detect Flag	0: No error passive detected 1: Error passive detected	RW
BOEIF	Bus-Off Entry Detect Flag	0: No bus-off entry detected 1: Bus-off entry detected	RW
BORIF	Bus-Off Recovery Detect Flag	0: No bus-off recovery detected 1: Bus-off recovery detected	RW
ORIF	Receive Overrun Detect Flag	0: No receive overrun detected 1: Receive overrun detected	RW
OLIF	Overload Frame Transmission Detect Flag	0: No overload frame transmission detected 1: Overload frame transmission detected	RW
BLIF	Bus Lock Detect Flag	0: No bus lock detected 1: Bus lock detected	RW

Note:
1. When writing 0 to these bits by a program, use the MOV instruction to ensure that only the specified bit is set to 0 and the other bits are set to 1. Writing 1 has no effect to these bit values.

Figure 25.25 Registers C0EIFR to C1EIFR

If an event corresponding to each bit occurs, the corresponding bit in the CiEIFR register is set to 1 regardless of the setting of the CiEIER register.
To set each bit to 0, write 0 by a program. If the set timing occurs simultaneously with the clear timing by the program, the bit becomes 1.

25.1.20.1 BEIF Bit

The BEIF bit is set to 1 when a bus error is detected.

25.1.20.2 EWIF Bit

The EWIF bit is set to 1 when the value of the receive error counter (REC) or transmit error counter (TEC) exceeds 95.
This bit is set to 1 only when the REC or TEC initially exceeds 95. Thus, if 0 is written to the EWIF bit by a program while the REC or TEC remains greater than 95, this bit is not set to 1 until the REC and the TEC go below 95 and then exceed 95 again.

25.1.20.3 EPIF Bit

The EPIF bit is set to 1 when the CAN error state becomes error-passive (the REC or TEC value exceeds 127).
This bit is set to 1 only when the REC or TEC initially exceeds 127. Thus, if 0 is written by a program while the REC or TEC remains greater than 127, this bit is not set to 1 until the REC and the TEC go below 127 and then exceed 127 again.

25.1.20.4 BOEIF Bit

The BOEIF bit is set to 1 when the CAN error state becomes bus-off (the TEC value exceeds 255).
This bit is also set to 1 when the BOM bit in the CiCTLR register (i = 0, 1) is 01b (entry to CAN halt mode automatically at bus-off entry) and the CAN module becomes the bus-off state.

25.1.20.5 BORIF Bit

The BORIF bit is set to 1 when the CAN module recovers from the bus-off state normally by detecting 11 consecutive bits 128 times in the following conditions:
(1) When the BOM bit in the CiCTLR register is 00b.
(2) When the BOM bit is 10b.
(3) When the BOM bit is 11b.

The BORIF bit is not set to 1 if the CAN module recovers from the bus-off state in the following conditions:
(1) When the CANM bit in the CiCTLR register is set to 01b (CAN reset mode).
(2) When the RBOC bit in the CiCTLR register is set to 1 (forcible return from bus-off).
(3) When the BOM bit is 01b.
(4) When the BOM bit is 11b and the CANM bit is set to 10b (CAN halt mode) before normal recovery occurs.

Table 25.8 lists the behavior of bits BOEIF and BORIF according to BOM bit setting value.

Table 25.8 Behavior of Bits BOEIF and BORIF according to BOM Bit Setting Value

BOM Bit	BOEIF Bit	BORIF Bit
00b	Set to 1 on entry to the bus-off state.	Set to 1 on exit from the bus-off state.
01b		Do not set to 1.
10b		Set to 1 on exit from the bus-off state.
11b		Set to 1 if normal bus-off recovery occurs before the CANM bit is set to 10b (CAN halt mode).

25.1.20.6 ORIF Bit

The ORIF bit is set to 1 when a receive overrun occurs.
This bit is not to set to 1 in overwrite mode. In overwrite mode, a reception complete interrupt request is generated if an overwrite condition occurs and this bit is not set to 1.
In normal mailbox mode, if an overrun occurs in any of mailboxes [0] to [31] in overrun mode, this bit is set to 1.
In FIFO mailbox mode, if an overrun occurs in any of mailboxes [0] to [23] or the receive FIFO in overrun mode, this bit is set to 1.

25.1.20.7 OLIF Bit

The OLIF bit is set to 1 if the transmitting condition of an overload frame is detected when the CAN module performs transmission or reception.

25.1.20.8 BLIF Bit

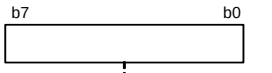
The BLIF bit is set to 1 if 32 consecutive dominant bits are detected on the CAN bus while the CAN module is in CAN operation mode.

After the BLIF bit is set to 1, 32 consecutive dominant bits are detected again under either of the following conditions:

- After this bit is set to 0 from 1, recessive bits are detected.
- After this bit is set to 0 from 1, the CAN module enters CAN reset mode or CAN halt mode and then enters CAN operation mode again.

25.1.21 CANi Receive Error Count Register (CiRECR) (i = 0, 1)

CANi Receive Error Count Register (i = 0, 1)



Symbol	Address	Reset Value
C0RECR	D7CEh	00h
C1RECR	D4CEh	00h

Function	Counter Value	RW
Receive error count function The CiRECR register increments or decrements the counter value according to the error status of the CAN module during reception	00h to FFh (1)	RO

Note:
1. The value in bus-off state is undefined.

Figure 25.26 Registers C0RECR to C1RECR

The CiRECR register indicates the value of the receive error counter.
Refer to the CAN Specifications (ISO11898-1) about the increment/decrement conditions of the receive error counter.

25.1.22 CANi Transmit Error Count Register (CiTECR) (i = 0, 1)

CANi Transmit Error Count Register (i = 0, 1)

b7 b0

Symbol	Address	Reset Value
C0TECR	D7CFh	00h
C1TECR	D4CFh	00h

Function	Counter Value	RW
Transmit error count function The CiTECR register increments or decrements the counter value according to the error status of the CAN module during transmission	00h to FFh (1)	RO

Note:
1. The value in bus-off state is undefined.

Figure 25.27 Registers C0TECR to C1TECR

The CiTECR register indicates the value of the TEC error counter.
Refer to the CAN Specifications (ISO11898-1) about the increment/decrement conditions of the transmit error counter.

25.1.23 CANi Error Code Store Register (CiECSR) (i = 0, 1)

CANi Error Code Store Register (i = 0, 1)

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	Reset Value
C0ECSR	D7D0h	00h
C1ECSR	D4D0h	00h

Bit Symbol	Bit Name	Function	RW
SEF	Stuff Error Flag (1, 2)	0: No stuff error detected 1: Stuff error detected	RW
FEF	Form Error Flag (1, 2)	0: No form error detected 1: Form error detected	RW
AEF	ACK Error Flag (1, 2)	0: No ACK error detected 1: ACK error detected	RW
CEF	CRC Error Flag (1, 2)	0: No CRC error detected 1: CRC error detected	RW
BE1F	Bit Error (recessive) Flag (1, 2)	0: No bit error detected 1: Bit error (recessive) detected	RW
BE0F	Bit Error (dominant) Flag (1, 2)	0: No bit error detected 1: Bit error (dominant) detected	RW
ADEF	ACK Delimiter Error Bit (1, 2)	0: No ACK delimiter error detected 1: ACK delimiter error detected	RW
EDPM	Error Display Mode Select Bit (3, 4)	0: Output of first detected error code 1: Output of accumulated error code	RW

Notes:
1. Writing 1 has no effect to these bit values.
2. When writing 0 to bits SEF, FEF, AEF, CEF, BE1F, BE0F, and ADEF by a program, use the MOV instruction to ensure that only the specified bit is set to 0 and the other bits are set to 1.
3. Write to the EDPM bit in CAN reset mode or CAN halt mode.
4. If more than one error condition is detected simultaneously, all related bits are set to 1.

Figure 25.28 Registers C0ECSR to C1ECSR

The CiECSR register can be used to monitor whether an error has occurred on the CAN bus. Refer to the CAN Specifications (ISO11898-1) to check the generation conditions of each error.
To set each bit except the EDPM bit to 0, write 0 by a program. If the timing at which each bit is set to 1 and the timing at which is written by a program are the same, the relevant bit is set to 1.

25.1.23.1 SEF Bit

The SEF bit is set to 1 when a stuff error is detected.

25.1.23.2 FEF Bit

The FEF bit is set to 1 when a form error is detected.

25.1.23.3 AEF Bit

The AEF bit is set to 1 when an ACK error is detected.

25.1.23.4 CEF Bit

The CEF bit is set to 1 when a CRC error is detected.

25.1.23.5 BE1F Bit

The BE1F bit is set to 1 when a recessive bit error is detected.

25.1.23.6 BE0F Bit

The BE0F bit is set to 1 when a dominant bit error is detected.

25.1.23.7 ADEF Bit

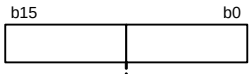
The ADEF bit is set to 1 when a form error is detected with the ACK delimiter during transmission.

25.1.23.8 EDPM Bit

The EDPM bit selects the output mode of the CiECSR register (i = 0, 1).
When this bit is set to 0, the CiECSR register outputs the first error code.
When this bit is set to 1, the CiECSR register outputs the accumulated error code.

25.1.24 CANi Time Stamp Register (CiTSR) (i = 0, 1)

CANi Time Stamp Register (i = 0, 1) (1)



Symbol	Address	Reset Value
C0TSR	D7D5h-D7D4h	0000h
C1TSR	D4D5h-D4D4h	0000h

Function	Counter Value	RW
Free-running counter value for the time stamp function	0000h to FFFFh	RO

Note:
1. Read the CiTSR register in 16-bit units.

Figure 25.29 Registers C0TSR to C1TSR

When the CiTSR register is read, the value of the time stamp counter (16-bit free-running counter) at that moment is read.
The value of the time stamp counter reference clock is a multiple of 1 bit time, as configured by the TSPS bit in the CiCTLR register.
The time stamp counter stops in CAN sleep mode and CAN halt mode, and is initialized in CAN reset mode.
The time stamp counter value is stored to TSL and TSH in the CiMBj register (j = 0 to 31) when a received message is stored in a receive mailbox.

25.1.25 CANi Test Control Register (CiTCR) (i = 0, 1)

CANi Test Control Register (i = 0, 1) (1)

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0			

Symbol	Address	Reset Value
C0TCR	D7D8h	00h
C1TCR	D4D8h	00h

Bit Symbol	Bit Name	Function	RW
TSTE	CAN Test Mode Enable Bit	0: CAN test mode disabled 1: CAN test mode enabled	RW
TSTM	CAN Test Mode Select Bit	b2 b1 0 0 : Other than CAN test mode 0 1 : Listen-only mode 1 0 : Self-test mode 0 (external loop back) 1 1 : Self-test mode 1 (internal loop back)	RW
— (b7-b3)	Reserved	Set to 0.	RW

Note:
1. Write to the CiTCR register only in CAN halt mode.

Figure 25.30 Registers C0TCR to C1TCR

25.1.25.1 TSTE Bit

When the TSTE bit is set to 0, CAN test mode is disabled.
When this bit is set to 1, CAN test mode is enabled.

25.1.25.2 TSTM Bit

The TSTM bit selects the CAN test mode.
The details of each CAN test mode is described below.

25.1.25.3 Listen-Only Mode

The ISO 11898-1 recommends an optional bus monitoring mode. In listen-only mode, the CAN node is able to receive valid data frames and valid remote frames. It sends only recessive bits on the CAN bus and the protocol controller is not required to send the ACK bit, overload flag, or active error flag.
Listen-only mode can be used for baud rate detection.
Do not request transmission from any mailboxes in this mode.
Figure 25.31 shows the connection when listen-only mode is selected.

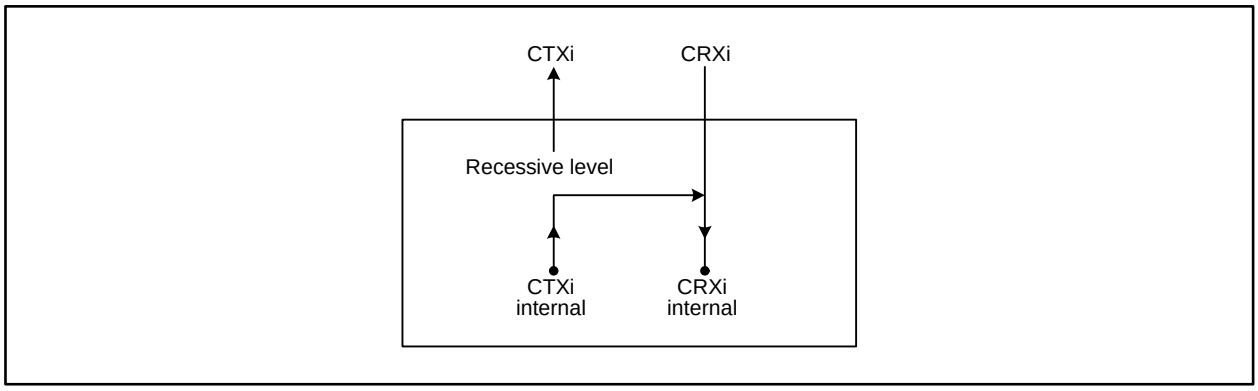


Figure 25.31 Connection when Listen-Only Mode is Selected (i = 0, 1)

25.1.25.4 Self-Test Mode 0 (External Loop Back)

Self-test mode 0 is provided for CAN transceiver tests.
In this mode, the protocol controller treats its own transmitted messages as messages received via the CAN transceiver and stores them into the receive mailbox. To be independent from external stimulation, the protocol controller generates the ACK bit.
Connect the CTXi/CRXi pins (i = 0, 1) to the transceiver.
Figure 25.32 shows the connection when self-test mode 0 is selected.

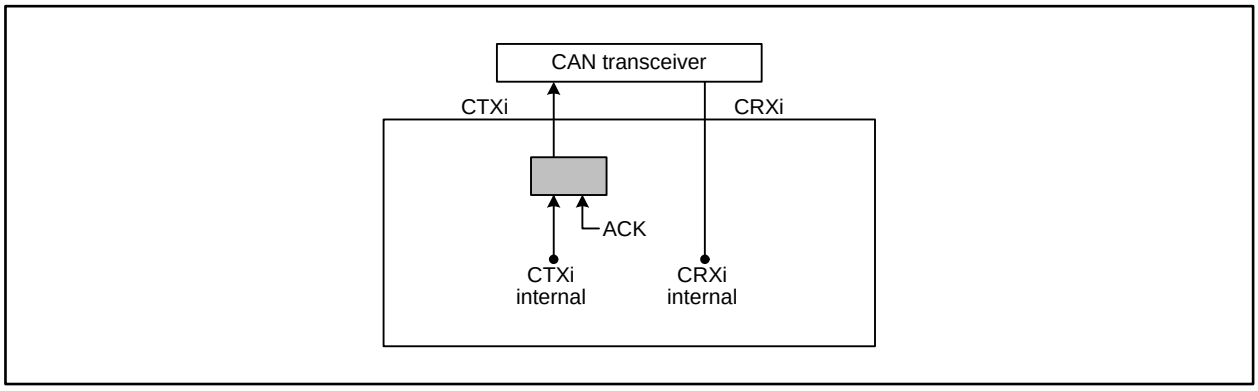


Figure 25.32 Connection when Self-Test Mode 0 is Selected (i = 0, 1)

25.1.25.5 Self-Test Mode 1 (Internal Loop Back)

Self-test mode 1 is provided for self-test functions.

In this mode, the protocol controller treats its transmitted messages as received messages and stores them into the receive mailbox. To be independent from external stimulation, the protocol controller generates the ACK bit.

In self-test mode 1, the protocol controller performs an internal feedback from the internal CTXi pin (i = 0, 1) to the internal CRXi pin. The input value of the external CRXi pin is ignored. The external CTXi pin outputs only recessive bits. The CTXi/CRXi pins do not need to be connected to the CAN bus or any external device.

Figure 25.33 shows the connection when self-test mode 1 is selected.

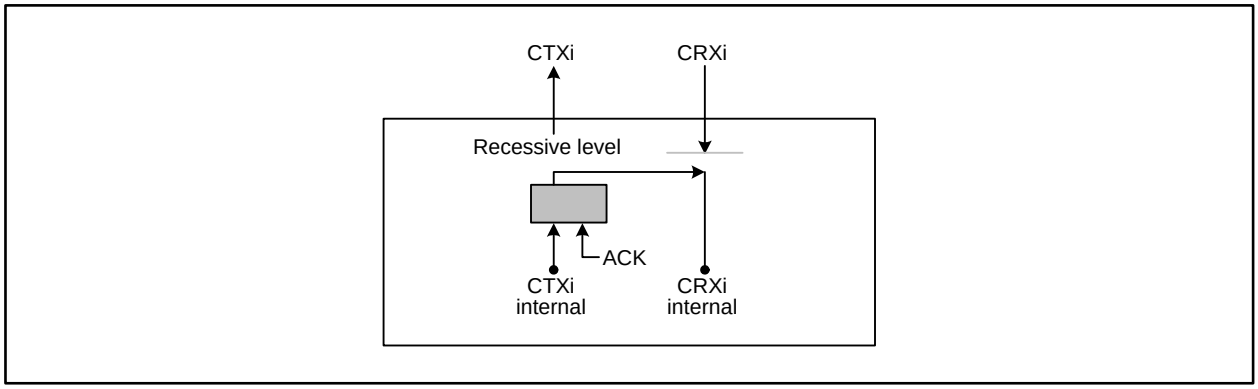


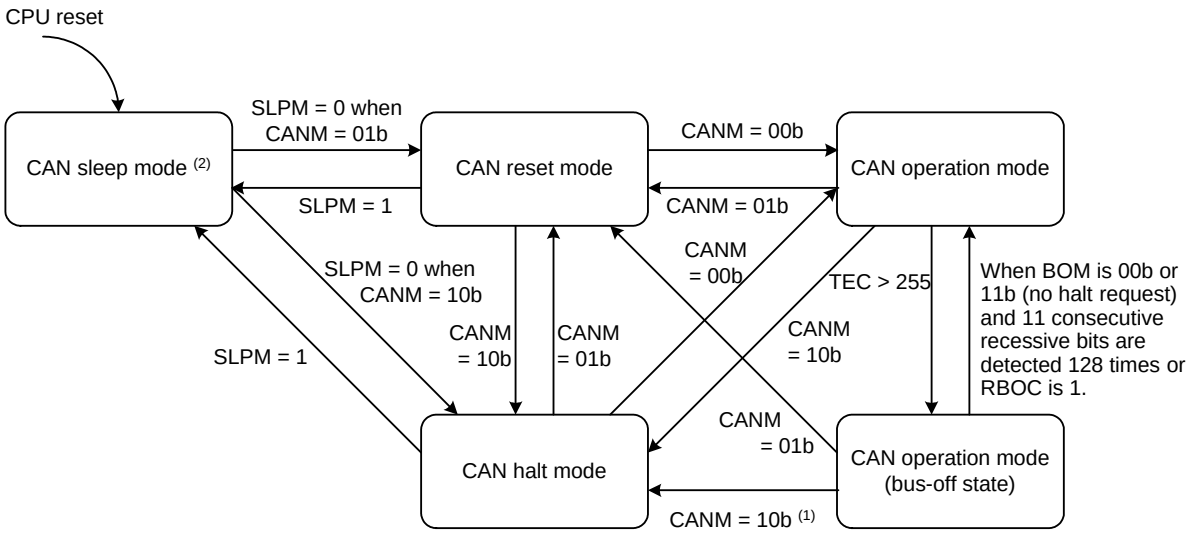
Figure 25.33 Connection when Self-Test Mode 1 is Selected (i = 0, 1)

25.2 Operating Mode

The CAN module has the following four operating modes:

- CAN reset mode
- CAN halt mode
- CAN operation mode
- CAN sleep mode

Figure 25.34 shows the transition between CAN operating modes.



CANM, SLPM, BOM, RBOC: Bits in the CiCTLR register

Notes:

1. The transition timing from the bus-off state to CAN halt mode depends on the setting of the BOM bit.
   - When the BOM bit is 01b, the state transition timing is immediately after entering the bus-off state.
   - When the BOM bit is 10b, the state transition timing is at the end of the bus-off state.
   - When the BOM bit is 11b, the state transition timing is at the setting of the CANM bit to 10b (CAN halt mode).
2. Write only to the SLPM bit to exit/set CAN sleep mode.

Figure 25.34 Transition between CAN Operating Modes (i = 0, 1)

25.2.1 CAN Reset Mode

CAN reset mode is provided for CAN communication configuration.
When the CANM bit in the CiCTLR register (i = 0, 1) is set to 01b, the CAN module enters CAN reset. Then the RSTST bit in the CiSTR register is set to 1. Do not change the CANM bit until the RSTST bit is set to 1.
Configure the CiBCR register before exiting CAN reset mode to any other modes.

The following registers are initialized to their reset values after entering CAN reset mode and their initialized values are retained during CAN reset mode:

- CiMCTLj register (j = 0 to 31)
- CiSTR register (except bits SLPST and TFST)
- CiEIFR register
- CiRECR register
- CiTECR register
- CiTSR register
- CiMSSR register
- CiMSMR register
- CiRFCR register
- CiTFCR register
- CiTCR register
- CiECSR register (except EDPM bit)

The previous values of the following registers are retained after entering CAN reset mode.

- CiCLKR register
- CiCTLR register
- CiSTR register (bits SLPST and TFST)
- CiMIER register
- CiEIER register
- CiBCR register
- CiCSSR register
- CiECSR register (EDPM bit only)
- CiMBj register
- Registers CiMKR0 to CiMKR7
- Registers CiFIDCR0 and CiFIDCR1
- CiMKIVLR register
- CiAFSR register
- CiRFPCR register
- CiTFPCR register

25.2.2 CAN Halt Mode

CAN halt mode is used for mailbox configuration and test mode setting.
When the CANM bit in the CiCTLR register (i = 0, 1) is set to 10b, CAN halt mode is selected. Then the HLTST bit in the CiSTR register is set to 1. Do not change the CANM bit until the HLTST bit is set to 1. Refer to Table 25.9 Operation in CAN Reset Mode and CAN Halt Mode regarding the state transition conditions when transmitting or receiving.

All registers except bits RSTST, HLTST, and SLPST in the CiSTR register remain unchanged when the CAN module enters CAN halt mode.
Do not change registers CiCLKR, CiCTLR (except bits CANM and SLPM,) and CiEIER in CAN halt mode. The CiBCR register can be changed in CAN halt mode only when listen-only mode is selected to use for automatic bit rate detection.

Table 25.9 Operation in CAN Reset Mode and CAN Halt Mode

Mode	Receiver	Transmitter	Bus-Off
CAN reset mode	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode after waiting for the end of message transmission. (1, 4)	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN halt mode	CAN module enters CAN halt mode after waiting for the end of message reception. (2, 3)	CAN module enters CAN halt mode after waiting for the end of message transmission. (1, 4)	[When the BOM bit is 00b] A halt request from a program will be acknowledged only after bus-off recovery. [When the BOM bit is 01b] CAN module enters automatically to CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM bit is 10b] CAN module enters automatically to CAN halt mode after waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM bit is 11b] CAN module enters CAN halt mode (without waiting for the end of bus-off recovery) if a halt is requested by a program during bus-off.

BOM bit: Bit in the CiCTLR register (i = 0, 1)
Notes:
1. If several messages are requested to be transmitted, mode transition occurs after the completion of the first transmission. In a case that the CAN reset mode is being requested during suspend transmission, mode transition occurs when the bus is idle, the next transmission ends, or the CAN module becomes a receiver.
2. If the CAN bus is locked at the dominant level, the program can detect this state by monitoring the BLIF bit in the CiEIFR register.
3. If a CAN bus error occurs during reception after CAN halt mode is requested, the CAN mode transits to CAN halt mode.
4. If a CAN bus error or arbitration lost occurs during transmission after CAN reset mode or CAN halt mode is requested, the CAN mode transits to the requested CAN mode.

25.2.3 CAN Sleep Mode

CAN sleep mode is used for reducing current consumption by stopping the clock supply to the CAN module. After MCU hardware reset or software reset, the CAN module starts from CAN sleep mode.

When the SLPM bit in the CiCTLR register (i = 0, 1) is set to 1, the CAN module enters CAN sleep mode. Then the SLPST bit in the CiSTR register is set to 1. Do not change the value of the SLPM bit until the bit is set to 1. The other registers remain unchanged when the MCU enters CAN sleep mode.

Write to the SLPM bit in CAN reset mode and CAN halt mode. Do not change any other registers (except the SLPM bit) during CAN sleep mode. Read operation is still allowed.
When the SLPM bit is set to 0, the CAN module is released from CAN sleep mode. When the CAN module exits CAN sleep mode, the other registers remain unchanged.

25.2.4 CAN Operation Mode (Excluding Bus-Off State)

CAN operation mode is used for CAN communication.
When the CANM bit in the CiCTLR register (i = 0, 1) is set to 00b, the CAN module enters CAN operation mode.
Then bits RSTST and HLTST in the CiSTR register are set to 0. Do not change the value of the CANM bit until these bits are set to 0.

If 11 consecutive recessive bits are detected after entering CAN operation mode, the CAN module is in the following states:

- The CAN module becomes an active node on the network that enables transmission and reception of CAN messages.
- Error monitoring of the CAN bus, such as receive and transmit error counters, is performed.

During CAN operation mode, the CAN module may be in one of the following three submodes, depending on the status of the CAN bus:

- Idle mode: Transmission or reception is not being performed.
- Receive mode: A CAN message sent by another node is being received.
- Transmit mode: A CAN message is being transmitted. The CAN module may receive its own message simultaneously when self-test mode 0 (TSTM bit in the CiSTR register = 10b) or self-test mode 1 (TSTM bit = 11b) is selected.

Figure 25.35 shows the submode in CAN operation mode.

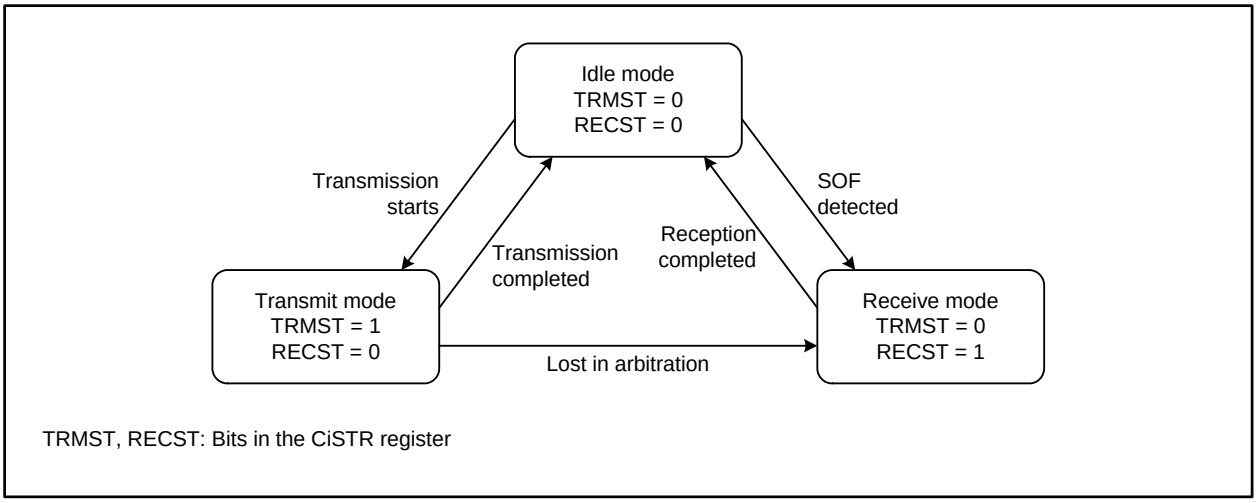


Figure 25.35 Submode in CAN Operation Mode (i = 0, 1)

25.2.5 CAN Operation Mode (Bus-Off State)

The CAN module enters the bus-off state according to the increment/decrement rules for the transmit/error counters in the CAN Specifications.
The following cases apply when recovering from the bus-off state. When the CAN module is in bus-off state, the values of the associated registers, except registers CiSTR, CiEIFR, CiRECR, CiTECR and CiTSR (i = 0, 1), remain unchanged.

(1) When the BOM bit in the CiCTLR register is 00b (normal mode)

The CAN module enters the error-active state after it has completed the recovery from the bus-off state and CAN communication is enabled. The BORIF bit in the CiEIFR register is set to 1 (bus-off recovery detected) at this time.

(2) When the RBOC bit in the CiCTLR register is set to 1 (forcible return from bus-off)

The CAN module enters the error-active state when it is in bus-off state and the RBOC bit is set to 1. CAN communication is enabled again after 11 consecutive recessive bits are detected. The BORIF bit is not set to 1 at this time.

(3) When the BOM bit is 01b (entry to CAN halt mode automatically at bus-off entry)

The CAN module enters CAN halt mode when it reaches the bus-off state. The BORIF bit is not set to 1 at this time.

(4) When the BOM bit is 10b (entry to CAN halt mode automatically at bus-off end)

The CAN module enters CAN halt mode when it has completed the recovery from bus-off. The BORIF bit is set to 1 at this time.

(5) When the BOM bit is 11b (entry to CAN halt mode by a program) and the CANM bit in the CiCTLR register is set to 10b (CAN halt mode) during the bus-off state

The CAN module enters CAN halt mode when it is in bus-off state and the CANM bit is set to 10b (CAN halt mode). The BORIF bit is not set to 1 at this time.
If the CANM bit is not set to 10b during bus-off, the same behavior as (1) applies.

25.3 CAN Communication Speed Configuration

The following description explains about the CAN communication speed configuration.

25.3.1 CAN Clock Configuration

This group has a CAN clock selector.
The CAN clock can be configured by setting the CCLKS bit in the CiCLKR register (i = 0, 1) and the BRP bit in the CiBCR register.
Figure 25.36 shows the block diagram of CAN clock generator.

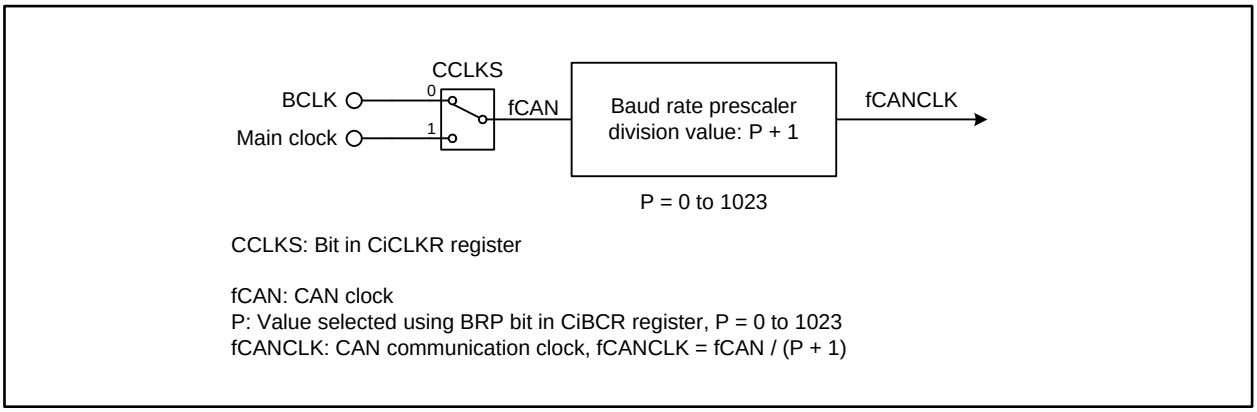


Figure 25.36 Block Diagram of CAN Clock Generator (i = 0, 1)

25.3.2 Bit Timing Configuration

The bit time is a single bit time for transmitting/receiving a message and consists of the following three segments.
Figure 25.37 shows the bit timing.

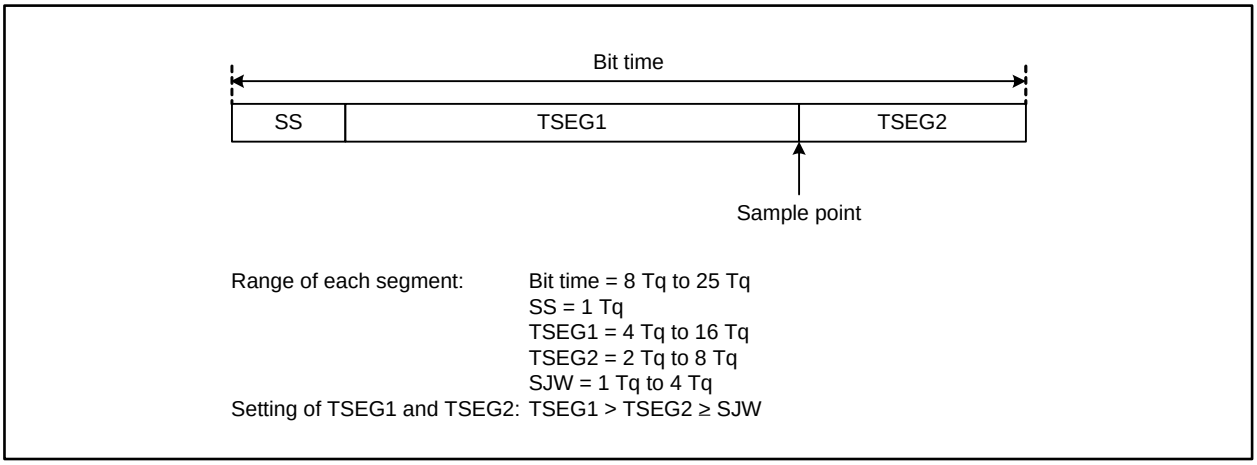


Figure 25.37 Bit Timing

25.3.3 Bit rate

The bit rate depends on the CAN clock (fCAN), the division value of the baud rate prescaler, and the number of Tq of 1-bit time.

$$\text{Bit rate[bps]} = \frac{fCAN}{\text{Baud rate prescaler division value}\ (1) \times \text{number of Tq of 1 bit time}} = \frac{fCANCLK}{\text{Number of Tq of 1-bit time}}$$

Note:

1. Division value of the baud rate prescaler = P + 1 (P = 0 to 1023)
   P: Setting value of the BRP bit in the CiBCR register (i = 0, 1)

Table 25.10 lists bit rate examples.

Table 25.10 Bit Rate Examples

fCAN	32 MHz		24 MHz		20 MHz		16 MHz		8 MHz	
Bit Rate	No. of Tq	P+1	No. of Tq	P+1	No. of Tq	P+1	No. of Tq	P+1	No. of Tq	P+1
1 Mbps	8 Tq	4	8 Tq	3	10 Tq	2	8 Tq	2	8 Tq	1
	16 Tq	2			20 Tq	1	16 Tq	1		
500 kbps	8 Tq	8	8 Tq	6	10 Tq	4	8 Tq	4	8 Tq	2
	16 Tq	4	16 Tq	3	20 Tq	2	16 Tq	2	16 Tq	1
250 kbps	8 Tq	16	8 Tq	12	10 Tq	8	8 Tq	8	8 Tq	4
	16 Tq	8	16 Tq	6	20 Tq	4	16 Tq	4	16 Tq	2
83.3 kbps	8 Tq	48	8 Tq	36	8 Tq	30	8 Tq	24	8 Tq	12
	16 Tq	24	16 Tq	18	10 Tq	24	16 Tq	12	16 Tq	6
					16 Tq	15				
					20 Tq	12				
33.3 kbps	8 Tq	120	8 Tq	90	8 Tq	75	8 Tq	60	8 Tq	30
	10 Tq	96	10 Tq	72	10 Tq	60	10 Tq	48	10 Tq	24
	16 Tq	60	16 Tq	45	20 Tq	30	16 Tq	30	16 Tq	15
	20 Tq	48	20 Tq	36			20 Tq	24	20 Tq	12

25.4 Mailbox and Mask Register Structure

There are 32 mailboxes with the same structure.
Figure 25.38 shows the structure of registers C0MBj to C1MBj (j = 0 to 31).

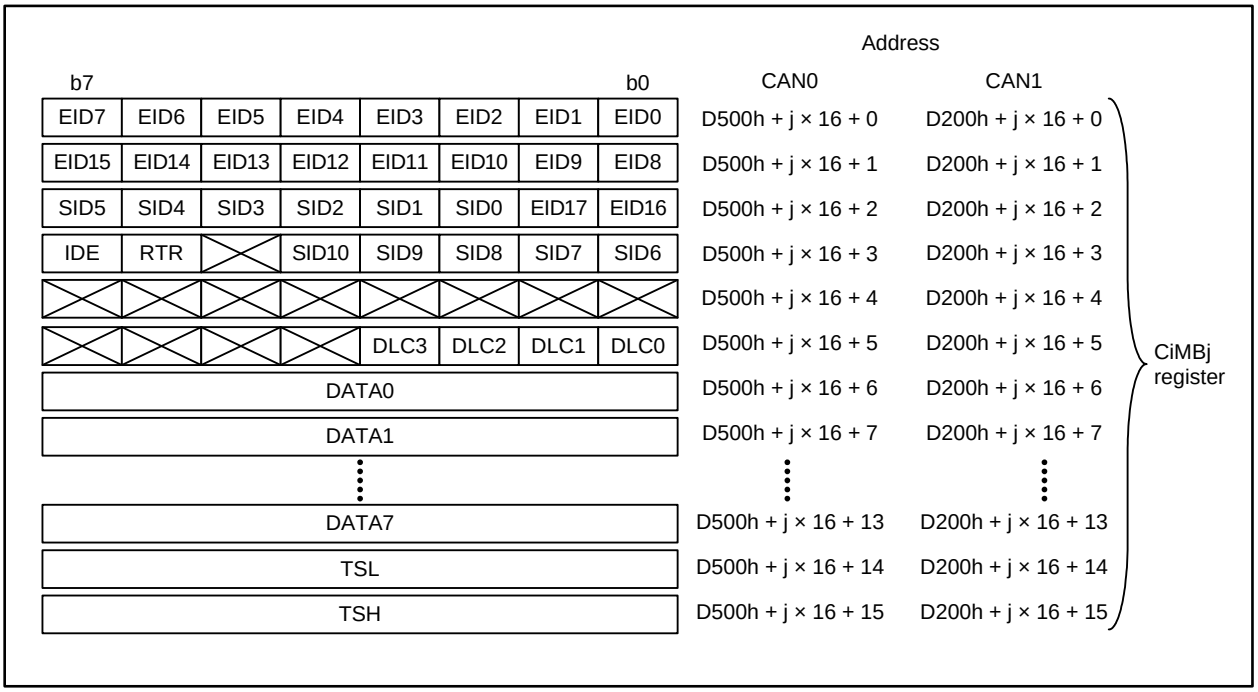


Figure 25.38 Structure of Registers C0MBj to C1MBj (i = 0, 1; j = 0 to 31)

There are 8 mask registers with the same structure.
Figure 25.39 shows the structure of registers C0MKRk to C1MKRk (k = 0 to 7).

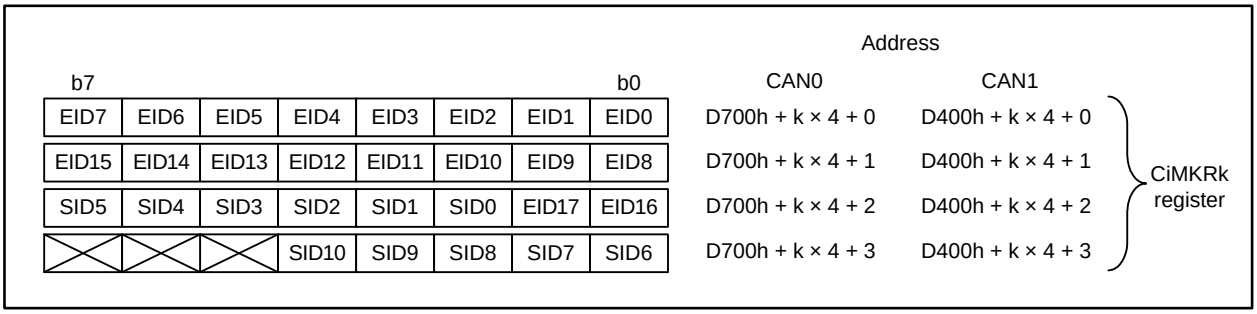


Figure 25.39 Structure of Registers C0MKRk to C1MKRk (i = 0, 1; k = 0 to 7)

There are 2 FIFO received ID compare registers with the same structure.
Figure 25.40 shows the structure of registers C0FIDCRn to C1FIDCRn (n = 0, 1).

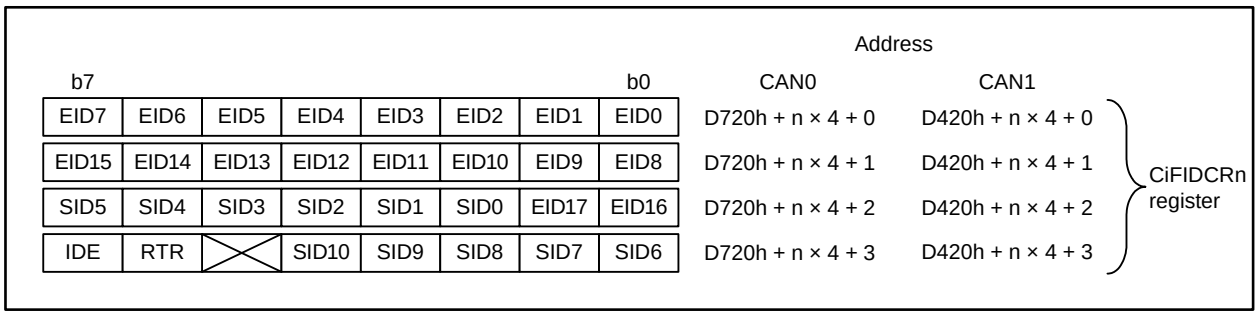


Figure 25.40 Structure of Registers C0FIDCRn to C1FIDCRn (i = 0, 1; n = 0, 1)

25.5 Acceptance Filtering and Masking Function

Acceptance filtering allows the user to receive messages with a specified range of multiple IDs for mailboxes.
Registers CiMKR0 to CiMKR7 (i = 0, 1) can perform masking of the standard ID and the extended ID of 29 bits.

- The CiMKR0 register corresponds to mailboxes [0] to [3].
- The CiMKR1 register corresponds to mailboxes [4] to [7].
- The CiMKR2 register corresponds to mailboxes [8] to [11].
- The CiMKR3 register corresponds to mailboxes [12] to [15].
- The CiMKR4 register corresponds to mailboxes [16] to [19].
- The CiMKR5 register corresponds to mailboxes [20] to [23].
- The CiMKR6 register corresponds to mailboxes [24] to [27] in normal mailbox mode, and receive FIFO mailboxes [28] to [31] in FIFO mailbox mode.
- The CiMKR7 register corresponds to mailboxes [28] to [31] in normal mailbox mode, and receive FIFO mailboxes [28] to [31] in FIFO mailbox mode.

The CiMKIVLR register disables acceptance filtering individually for each mailbox.

The IDE bit in the CiMBj register (j = 0 to 31) is enabled when the IDFM bit in the CiCTLR register is 10b (mixed ID mode).
The RTR bit in the CiMBj register selects a data frame or a remote frame.

In FIFO mailbox mode, normal mailboxes (mailboxes [0] to [23]) use the single corresponding register among registers CiMKR0 to CiMKR5 for acceptance filtering. Receive FIFO mailboxes (mailboxes [28] to [31]) use two registers CiMKR6 and CiMKR7 for the acceptance filtering.
Also, the receive FIFO uses two registers CiFIDCR0 and CiFIDCR1 for ID comparison. Bits EID, SID, RTR, and IDE in registers CiMB28 to CiMB31 for the receive FIFO are disabled. As acceptance filtering depends on the result of two ID-mask sets, two ranges of IDs can be received into the receive FIFO.
The CiMKIVLR register is disabled for the receive FIFO.

If both setting of standard ID and extended ID are set in the IDE bits in registers CiFIDCR0 and CiFIDCR1 individually, both ID formats are received.
If both setting of data frame and remote frame are set in the RTR bits in registers CiFIDCR0 and CiFIDCR1 individually, both data and remote frames are received.
When combination with two ranges of IDs is not necessary, set the same mask value and the same ID into both of the FIFO ID/mask register sets.

Figure 25.41 shows the correspondence of mask registers to mailboxes, and Figure 25.42 shows acceptance filtering.

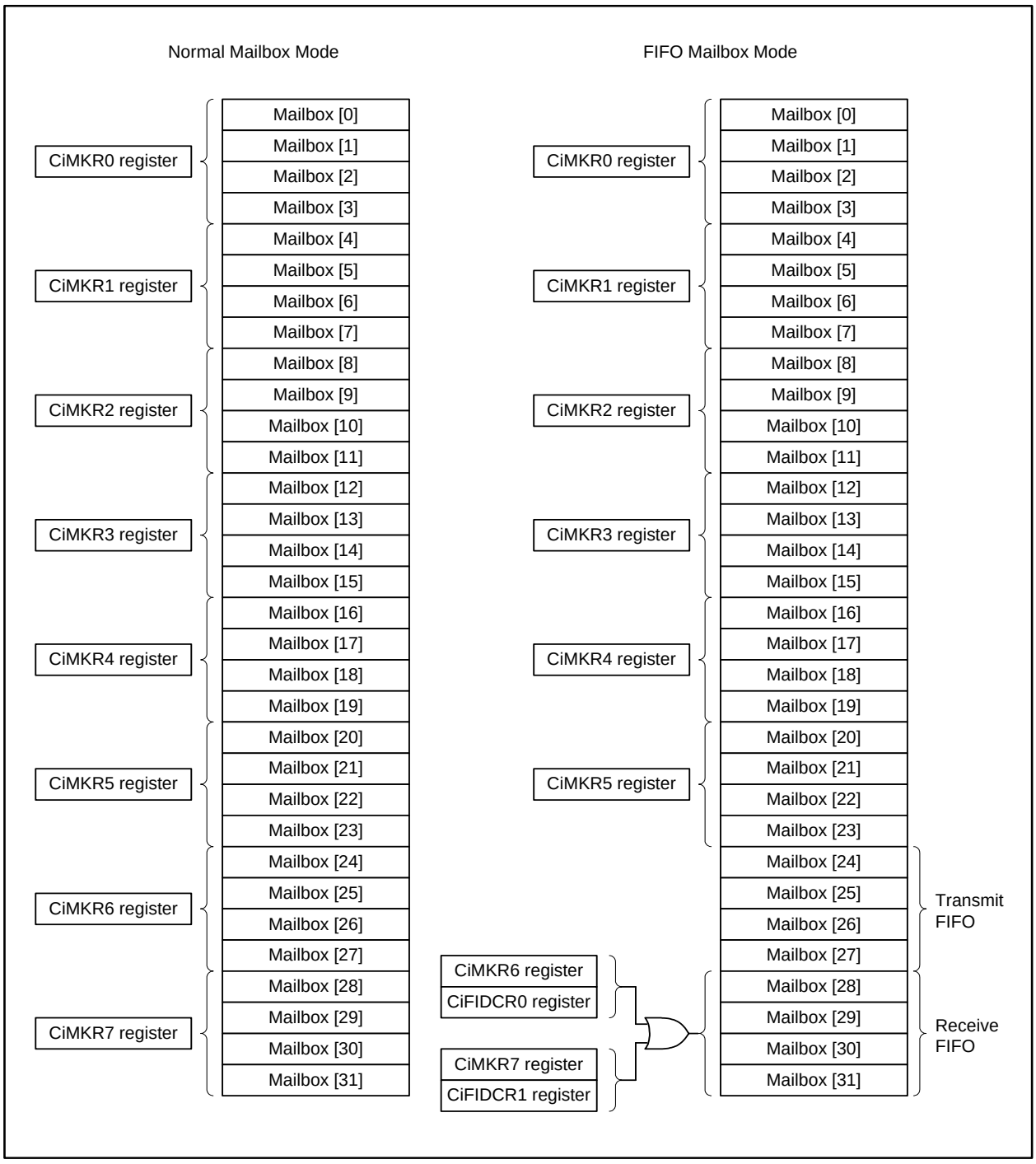


Figure 25.41 Correspondence of Mask Registers to Mailboxes (i = 0, 1)

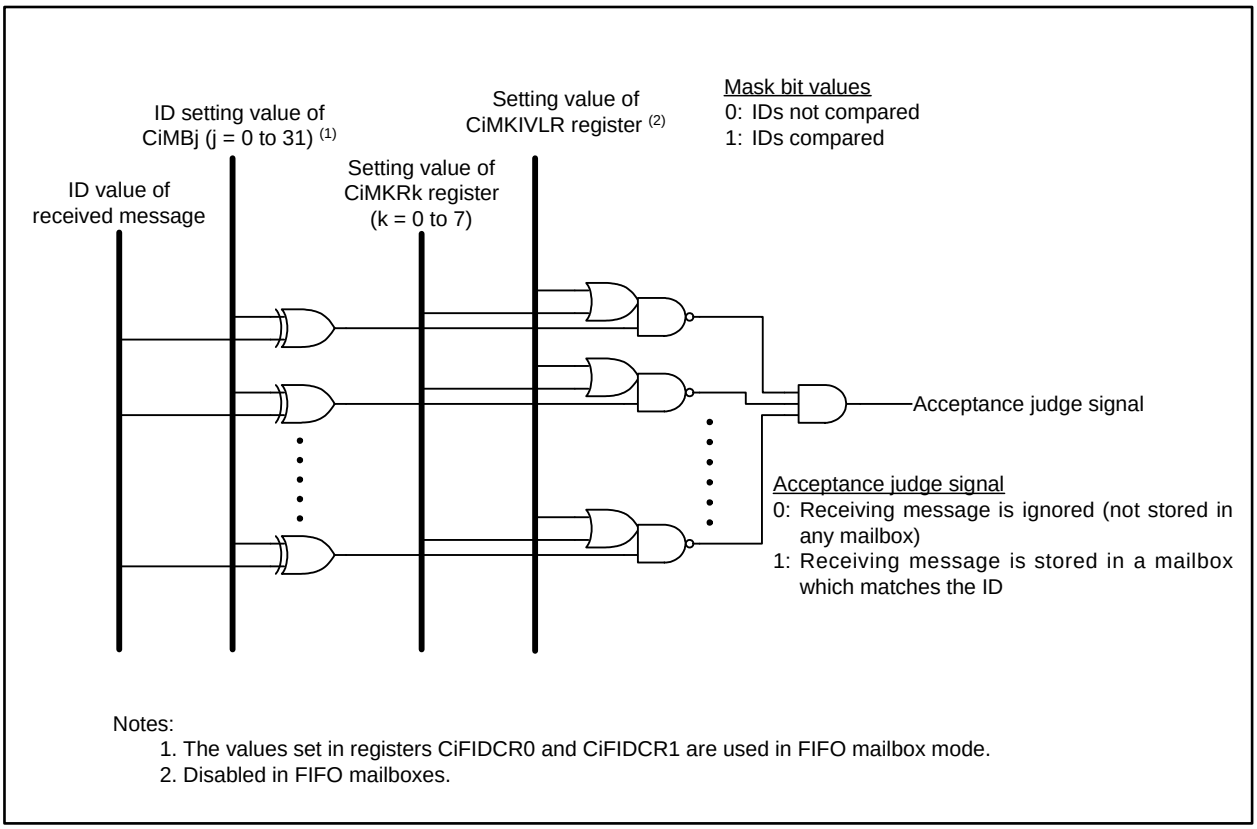


Figure 25.42 Acceptance Filtering (i = 0, 1)

25.6 Reception and Transmission

Table 25.11 list the CAN communication mode configuration.

Table 25.11 Configuration for CAN Reception Mode and Transmission Mode

TRMREQ	RECREQ	ONESHOT	Communication Mode of Mailbox
0	0	0	Mailbox disabled or transmission being aborted.
0	0	1	Configurable only when transmission or reception from a mailbox (programmed in one-shot mode) is aborted.
0	1	0	Configured as a receive mailbox for a data frame or a remote frame.
0	1	1	Configured as a one-shot receive mailbox for a data frame or a remote frame.
1	0	0	Configured as a transmit mailbox for a data frame or a remote frame.
1	0	1	Configured as a one-shot transmit mailbox for a data frame or a remote frame.
1	1	0	Do not set.
1	1	1	Do not set.

TRMREQ, RECREQ, ONESHOT: Bits in the CiMCTLj register (i = 0, 1; j = 0 to 31)

When a mailbox is configured as a receive mailbox or a one-shot receive mailbox, note the following:

(1) Before a mailbox is configured as a receive mailbox or a one-shot receive mailbox, set the CiMCTLj register (i = 0, 1; j = 0 to 31) to 00h.

(2) A received message is stored into the first mailbox that matches the condition according to the result of receive mode configuration and acceptance filtering. Upon deciding a mailbox which stores the received message, the mailbox with the smaller number has higher priority.

(3) In CAN operation mode, when a CAN module transmits a message whose ID matches with the ID/mask set of a mailbox configured to receive messages, the CAN module never receives the transmitted data. In self-test mode, however, the CAN module may receive its transmitted data. In this case, the CAN module sends an ACK.

When configuring a mailbox as a transmit mailbox or a one-shot transmit mailbox, note the following:

(1) Before a mailbox is configured as a transmit mailbox or one-shot transmit mailbox, ensure that the CiMCTLj register is 00h and that there is no pending abort process.

25.6.1 Reception

Figure 25.43 shows an operation example of data frame reception in overwrite mode.
This example shows the operation of overwriting the first message when the CAN module receives two consecutive CAN messages that matches the receiving conditions of the CiMCTL0 register (i = 0, 1).

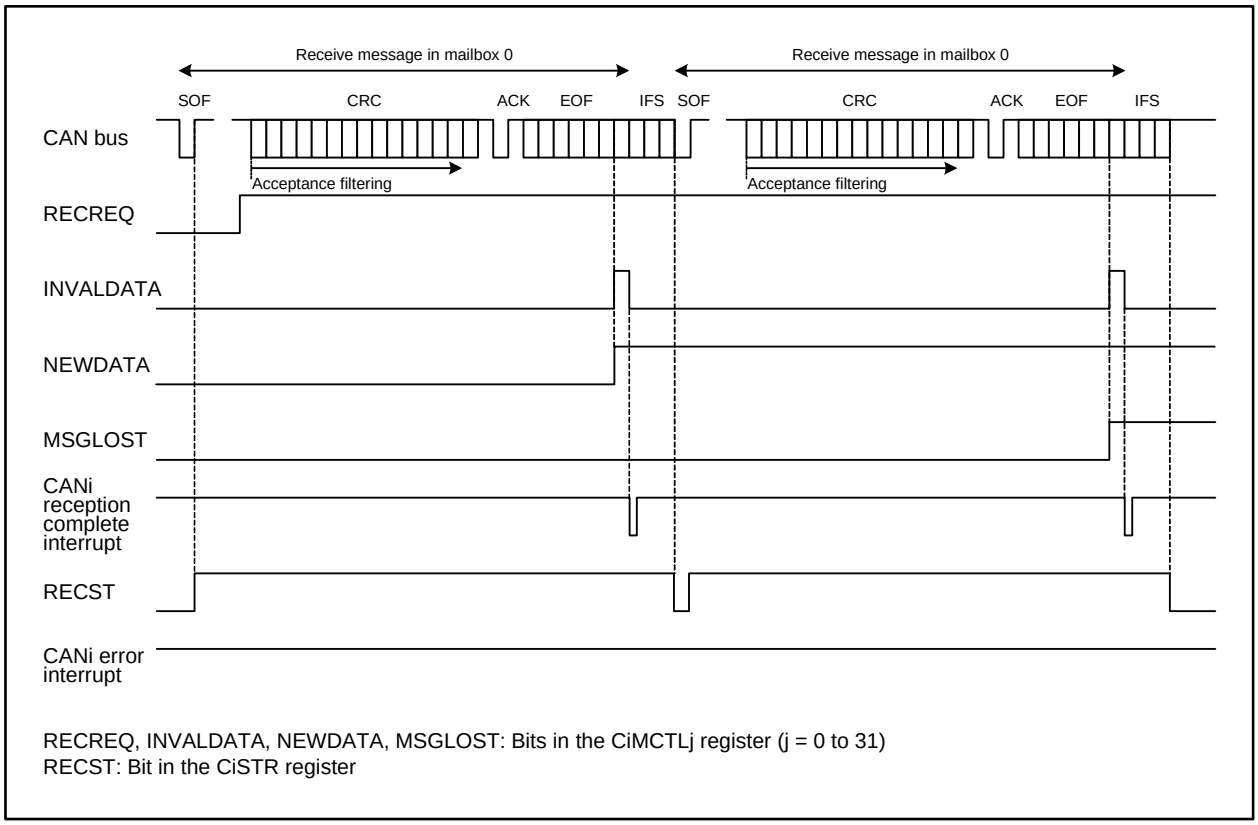


Figure 25.43 Operation Example of Data Frame Reception in Overwrite Mode (i = 0, 1)

(1) When a SOF is detected on the CAN bus, the RECST bit in the CiSTR register is set to 1 (reception in progress) if the CAN module has no message ready to start transmission.
(2) The acceptance filter procedure starts at the beginning of the CRC field to select the receive mailbox.
(3) After a message has been received, the NEWDATA bit in the CiMCTLj register (j = 0 to 31) for the receive mailbox is set to 1 (new data being updated/stored in the mailbox). The INVALDATA bit in the CiMCTLj register is set to 1 (message is being updated) at the same time, and then the INVALDATA bit is set to 0 (message valid) again after the complete message is transferred to the mailbox.
(4) When the interrupt enable bit in the CiMIER register for the receive mailbox is 1 (interrupt enabled), the CANi reception complete interrupt request is generated. This interrupt is generated when the INVALDATA bit is set to 0.
(5) After reading the message from the mailbox, the NEWDATA bit needs to be set to 0 by a program.
(6) In overwrite mode, if the next CAN message has been received into a mailbox whose NEWDATA bit is still set to 1, the MSGLOST bit in the CiMCTLj register is set to 1 (message has been overwritten). The new received message is transferred to the mailbox. The CANi reception complete interrupt request is generated the same as in (4).

Figure 25.44 shows the operational example of data frame reception in overrun mode.
This example shows the operation of overrunning the second message when the CAN module receives two consecutive CAN messages that matches the receiving conditions of the CiMCTL0 register (i = 0, 1).

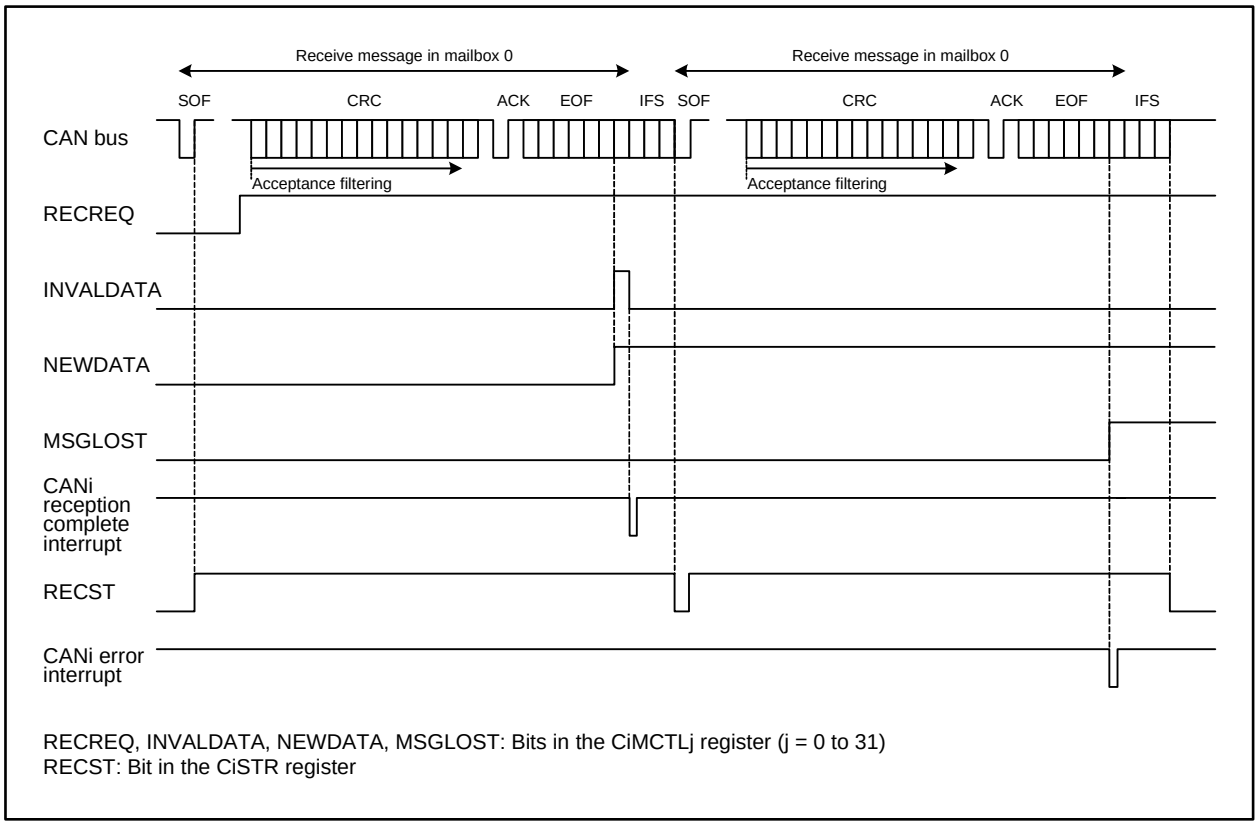


Figure 25.44 Operation Example of Data Frame Reception in Overrun Mode (i = 0, 1)

(1) to (5) are the same as overwrite mode.

(6) In overrun mode, if the next message has been received before the NEWDATA bit is set to 0, the MSGLOST bit in the CiMCTLj register (j = 0 to 31) is set to 1 (message has been overrun). The new received message is discarded and a CANi error interrupt request is generated if the corresponding interrupt enable bit in the CiEIER register is set to 1 (interrupt enabled).

25.6.2 Transmission

Figure 25.45 shows an operation example of data frame transmission. This example shows the operation of transmitting messages that has been set in registers CiMCTL0 and CiMCTL1 (i = 0, 1).

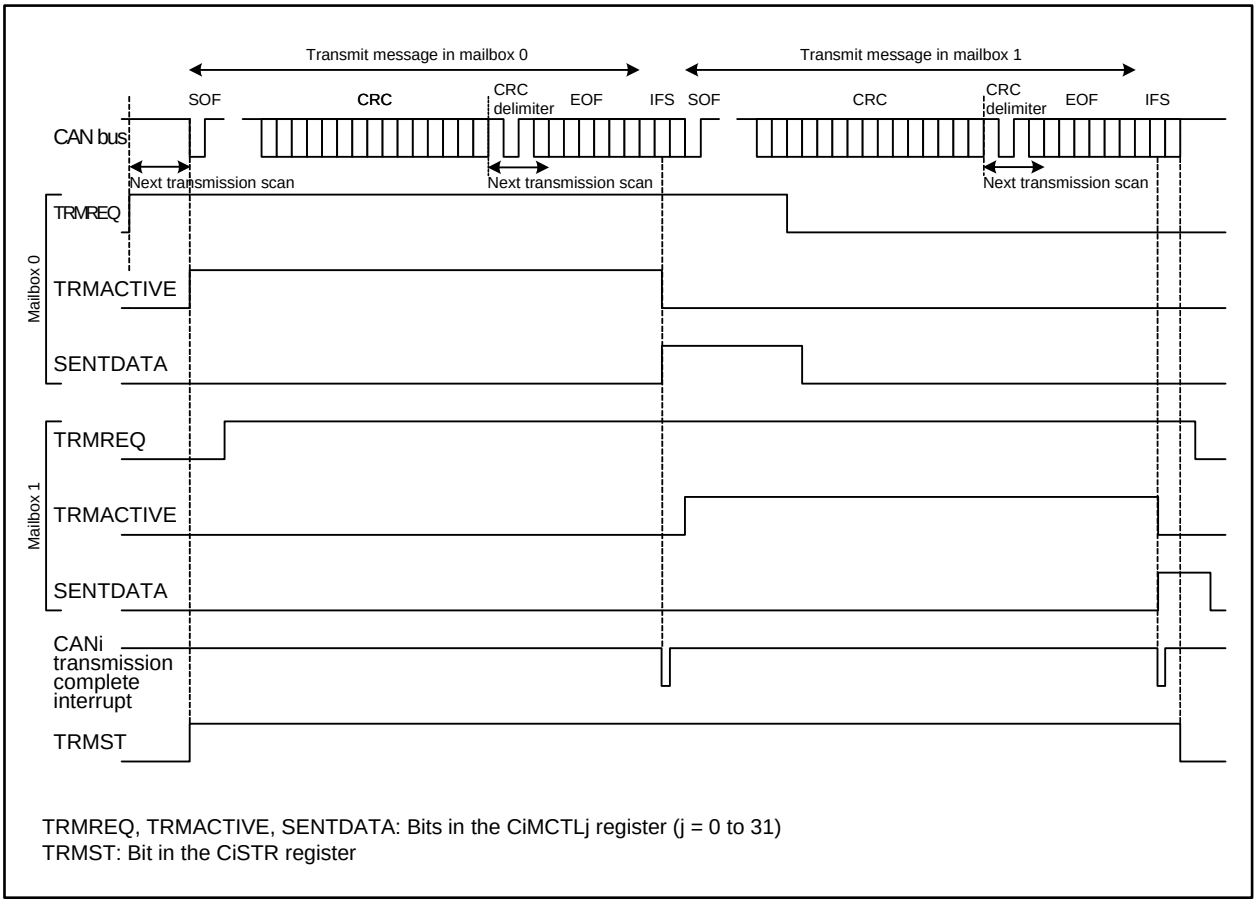


Figure 25.45 Operation Example of Data Frame Transmission (i = 0, 1)

(1) When a TRMREQ bit in the CiMCTLj register (j = 0 to 31) is set to 1 (transmit mailbox) in bus-idle state, the mailbox scan procedure starts to decide the highest-priority mailbox for transmission. Once the transmit mailbox is decided, the TRMACTIVE bit in the CiMCTLj register is set to 1 (from when a transmission request is received until transmission is completed, or an error/arbitration lost has occurred), the TRMST bit in the CiSTR register is set to 1 (transmission in progress), and the CAN module starts transmission. (1)

(2) If other TRMREQ bits are set, the transmission scan procedure starts with the CRC delimiter for the next transmission.

(3) If transmission is completed without losing arbitration, the SENTDATA bit in the CiMCTLj register is set to 1 (transmission completed) and the TRMACTIVE bit is set to 0 (transmission is pending, or no transmission request). If the interrupt enable bit in the CiMIER register is 1 (interrupt enabled), the CANi transmission complete interrupt request is generated.

(4) When requesting the next transmission from the same mailbox, set bits SENTDATA and TRMREQ to 0, then set the TRMREQ bit to 1 after checking that bits SENTDATA and TRMREQ have been set to 0.

Note:

1. If arbitration is lost after the CAN module starts transmission, the TRMACTIVE bit is set to 0. The transmission scan procedure is performed again to search for the highest-priority transmit mailbox from the beginning of the CRC delimiter. If an error occurs either during transmission or following the loss of arbitration, the transmission scan procedure is performed again from the start of the error delimiter to search for the highest-priority transmit mailbox.

25.7 CAN Interrupt

The CAN module provides the following CAN interrupts:

- CANi reception complete interrupt
- CANi transmission complete interrupt
- CANi receive FIFO interrupt
- CANi transmit FIFO interrupt
- CANi error interrupt

  There are eight types of interrupt sources for the CANi error interrupts. These sources can be determined by checking the CiEIFR register.
  - Bus error
  - Error-warning
  - Error-passive
  - Bus-off entry
  - Bus-off recovery
  - Receive overrun
  - Overload frame transmission
  - Bus lock
- CANi wake-up interrupt

i = 0, 1

26. A/D Converter

Note

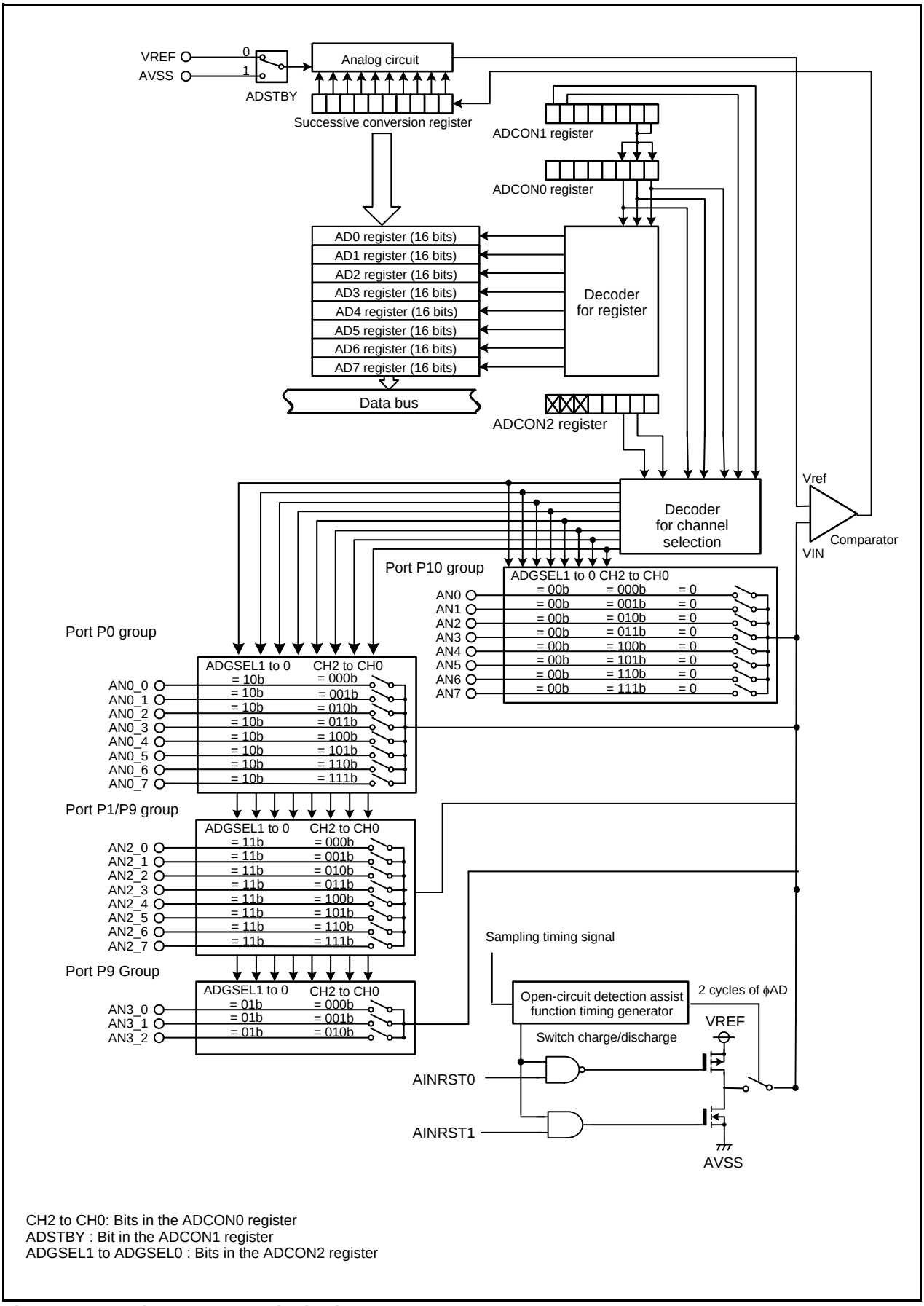
The 100-pin package has no AN2_4. The 64-pin package has no AN0_4 to AN0_7, AN2_0 to AN2_3, AN2_5 to AN2_7.
Do not use these pins as analog pins.

26.1 Introduction

The A/D converter consists of one 10-bit successive approximation A/D converter.
Table 26.1 lists the A/D Converter Specifications and Figure 26.1 shows an A/D Converter Block Diagram.

Table 26.1 A/D Converter Specifications

Item	Specification
A/D conversion method	Successive approximation
Analog input voltage	0 V to AVCC (VCC)
Operating clock ϕAD	f1, f1 divided by 2, f1 divided by 3, f1 divided by 4, f1 divided by 6, f1 divided by 12, fOCO40M divided by 2, fOCO40M divided by 3, fOCO40M divided by 4, fOCO40M divided by 6, or fOCO40M divided by 12
Resolution	10 bits
Integral nonlinearity error	AVCC = VREF = 5 V ±3 LSB AVCC = VREF = 3.3 V ±5 LSB
Operation modes	One-shot mode, repeat mode, single sweep mode, repeat sweep mode 0
Analog input pins	8 pins (AN0 to AN7) + 8 pins (AN0_0 to AN0_7)+ 7 pins (AN2_0 to AN2_3, AN2_5 to AN2_7) + 3 pins (AN3_0 to AN3_2) (100-pin package) 8 pins (AN0 to AN7) + 8 pins (AN0_0 to AN0_7)+ 8 pins (AN2_0 to AN2_7) + 3 pins (AN3_0 to AN3_2)(80-pin package) 8 pins (AN0 to AN7) + 4 pins (AN0_0 to AN0_3)+ 1 pin (AN2_4) + 3 pins (AN3_0 to AN3_2)(64-pin package)
A/D conversion start conditions	• Software trigger The ADST bit in the ADCON0 register is set to 1 (A/D conversion start). • External trigger (retrigger is enabled) Input to the $\overline{\text{ADTRG}}$ pin changes from high to low after the ADST bit is set to 1 (A/D conversion start).
Conversion rate per pin	Minimum 43 ϕAD cycles



CH2 to CH0: Bits in the ADCON0 register
ADSTBY : Bit in the ADCON1 register
ADGSEL1 to ADGSEL0 : Bits in the ADCON2 register

Figure 26.1 A/D Converter Block Diagram

Table 26.2 I/O Ports

Pin Name	I/O	Function
AN0 to AN7	Input	Analog input
AN0_0 to AN0_7	Input	Analog input
AN2_0 to AN2_7	Input	Analog input
AN3_0 to AN3_2	Input	Analog input
$\overline{\text{ADTRG}}$	Input	Trigger input

Note:
1. Set the direction bit of the ports sharing a port to 0 (input mode).

26.2 Registers

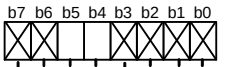
Table 26.3 lists registers associated with A/D converter. Set the CKS3 bit in the ADCON2 register before setting other registers associated with A/D converter. However, bits in the ADCON2 register and the CKS3 bit can be set simultaneously. After changing the CKS3 bit, set the registers in the same way again.

Table 26.3 Registers

Address	Register	Symbol	Reset Value
03A2h	Open-Circuit Detection Assist Function Register	AINRST	XX00 XXXXb
03C0h	A/D Register 0	AD0	XXXX XXXXb
03C1h			0000 00XXb
03C2h	A/D Register 1	AD1	XXXX XXXXb
03C3h			0000 00XXb
03C4h	A/D Register 2	AD2	XXXX XXXXb
03C5h			0000 00XXb
03C6h	A/D Register 3	AD3	XXXX XXXXb
03C7h			0000 00XXb
03C8h	A/D Register 4	AD4	XXXX XXXXb
03C9h			0000 00XXb
03CAh	A/D Register 5	AD5	XXXX XXXXb
03CBh			0000 00XXb
03CCh	A/D Register 6	AD6	XXXX XXXXb
03CDh			0000 00XXb
03CEh	A/D Register 7	AD7	XXXX XXXXb
03CFh			0000 00XXb
03D4h	A/D Control Register 2	ADCON2	0000 X00Xb
03D6h	A/D Control Register 0	ADCON0	0000 0XXXb
03D7h	A/D Control Register 1	ADCON1	0000 X000b

26.2.1 Open-Circuit Detection Assist Function Register (AINRST)

Open-Circuit Detection Assist Function Register



Symbol	Address	Reset Value
AINRST	03A2h	XX00 XXXXb

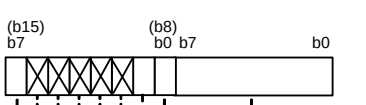
Bit Symbol	Bit Name	Function	RW
— (b3-b0)	No register bits. If necessary, set to 0. The read value is undefined.		—
AINRST0	Open-circuit detection assist function enable bit	b5 b4 0 0 : Open-circuit detection disabled 0 1 : Charge before conversion 1 0 : Discharge before conversion 1 1 : Do not set	RW
AINRST1			RW
— (b7-b6)	No register bits. If necessary, set to 0. The read value is undefined.		—

AINRST1-AINRST0 (Open-circuit detection assist function enable bit) (b5-b4)

To enable the A/D open-circuit detection assist function, set the AINRST0 bit or AINRST1 bit to 1, and then set the ADST bit in the ADCON0 register to 1 (A/D conversion) after waiting for one cycle of ϕAD.

26.2.2 A/D Register i (ADi) (i = 0 to 7)

A/D Register i (i = 0 to 7)



Symbol	Address	Reset Value
AD0	03C1h to 03C0h	0000 00XX XXXX XXXXb
AD1	03C3h to 03C2h	0000 00XX XXXX XXXXb
AD2	03C5h to 03C4h	0000 00XX XXXX XXXXb
AD3	03C7h to 03C6h	0000 00XX XXXX XXXXb
AD4	03C9h to 03C8h	0000 00XX XXXX XXXXb
AD5	03CBh to 03CAh	0000 00XX XXXX XXXXb
AD6	03CDh to 03CCh	0000 00XX XXXX XXXXb
AD7	03CFh to 03CEh	0000 00XX XXXX XXXXb

Function		RW
8 lower bits of A/D conversion result		RO
2 upper bits of A/D conversion result		RO
No register bits. If necessary, set to 0. The read value is 0.		—
Reserved bit	The read value is 0.	RO

The A/D conversion result is stored in the ADi register corresponding to pins ANi, AN0_i, AN2_i, and AN3_0 to AN3_2. Read the ADi register in 16-bit units. Table 26.4 lists Analog Pin and A/D Conversion Result Storing Register.

Table 26.4 Analog Pin and A/D Conversion Result Storing Register

Analog Pin				A/D Conversion Result Storing Register
AN0	AN0_0	AN2_0	AN3_0	AD0 register
AN1	AN0_1	AN2_1	AN3_1	AD1 register
AN2	AN0_2	AN2_2	AN3_2	AD2 register
AN3	AN0_3	AN2_3	—	AD3 register
AN4	AN0_4	AN2_4	—	AD4 register
AN5	AN0_5	AN2_5	—	AD5 register
AN6	AN0_6	AN2_6	—	AD6 register
AN7	AN0_7	AN2_7	—	AD7 register

26.2.3 A/D Control Register 2 (ADCON2)

A/D Control Register 2

b7	b6	b5	b4	b3	b2	b1	b0
	0	0		X			X

Symbol	Address	Reset Value
ADCON2	03D4h	0000 X00Xb

Bit Symbol	Bit Name	Function	RW
— (b0)	No register bit. If necessary, set to 0. The read value is undefined.		—
ADGSEL0	A/D input group select bit	b2 b1 0 0 : AN0 to AN7 0 1 : AN3_0 to AN3_2 1 0 : AN0_0 to AN0_7 1 1 : AN2_0 to AN2_7	RW
ADGSEL1			RW
— (b3)	No register bit. If necessary, set to 0. The read value is undefined.		—
CKS2	Frequency select bit 2	Refer to the CKS0 bit in the ADCON0 register.	RW
— (b6-b5)	Reserved bits	Set to 0	RW
CKS3	fAD select bit	0: f1 1: fOCO40M	RW

If the ADCON2 register is rewritten during A/D conversion, the conversion result is undefined.

CKS3 (fAD select bit) (b7)

Set the CKS3 bit while A/D conversion is stopped.

Set the CKS3 bit, and then set other A/D converter related registers. Also, after changing the CKS3 bit, set the A/D converter related registers again. Note that bits in the ADCON2 register and the CKS3 bit can be set simultaneously.

26.2.4 A/D Control Register 0 (ADCON0)

A/D Control Register 0

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	Reset Value
ADCON0	03D6h	0000 0XXXb

Bit Symbol	Bit Name	Function	RW
CH0	Analog input pin select bit	In one-shot mode or repeat mode b2 b1 b0 0 0 0 : AN0 0 0 1 : AN1 0 1 0 : AN2 0 1 1 : AN3 1 0 0 : AN4 1 0 1 : AN5 1 1 0 : AN6 1 1 1 : AN7	RW
CH1			RW
CH2			RW
MD0	A/D operation mode select bit 0	b4 b3 0 0 : One-shot mode 0 1 : Repeat mode 1 0 : Single sweep mode 1 1 : Repeat sweep mode 0	RW
MD1			RW
TRG	Trigger select bit	0 : Software trigger 1 : ADTRG trigger	RW
ADST	A/D conversion start flag	0 : A/D conversion stop 1 : A/D conversion start	RW
CKS0	Frequency select bit 0	Refer to the description of the CKS0 bit.	RW

If the ADCON0 register is rewritten during A/D conversion, the conversion result is undefined.

CKS0 (Frequency select bit 0) (b7)

ϕAD frequency is selected by a combination of the CKS0 bit in the ADCON0 register, the CKS1 bit in the ADCON1 register, and bits CKS3 and CKS2 in the ADCON2 register. Select bits CKS2 to CKS0 after setting the CKS3 bit in the ADCON2 register. Note that bits CKS3 and CKS2 can be set simultaneously. Table 26.5 lists ϕAD Frequency.

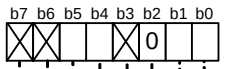
Table 26.5 ϕAD Frequency

CKS3	CKS2	CKS1	CKS0	ϕAD
0	0	0	0	fAD(f1) divided by 4
	0	0	1	fAD(f1) divided by 2
	0	1	0	fAD(f1)
	0	1	1	
	1	0	0	fAD(f1) divided by 12
	1	0	1	fAD(f1) divided by 6
	1	1	0	fAD(f1) divided by 3
	1	1	1	
1	0	0	0	fAD(fOCO40M) divided by 4
	0	0	1	fAD(fOCO40M) divided by 2
	1	0	0	fAD(fOCO40M) divided by 12
	1	0	1	fAD(fOCO40M) divided by 6
	1	1	0	fAD(fOCO40M) divided by 3
	1	1	1	

Only set the values listed above.

26.2.5 A/D Control Register 1 (ADCON1)

A/D Control Register 1



Symbol	Address	Reset Value
ADCON1	03D7h	0000 X000b

Bit Symbol	Bit Name	Function	RW
SCAN0	A/D sweep pin select bit	b1 b0 0 0: AN0 to AN1 (2 pins) 0 1: AN0 to AN3 (4 pins) 1 0: AN0 to AN5 (6 pins) 1 1: AN0 to AN7 (8 pins)	RW
SCAN1			RW
— (b2)	Reserved bit	Set to 0	RW
— (b3)	No register bit. If necessary, set to 0. The read value is undefined		—
CKS1	Frequency select bit 1	Refer to the CKS0 bit in the registers, ADCON0 and AD1CON0	RW
ADSTBY	A/D standby bit	0 : A/D operation stopped (standby) 1 : A/ operation enabled	RW
— (b7-b6)	Reserved bit	Set to 0	RW

If the ADCON1 register is rewritten during A/D conversion, the conversion result is undefined.

ADSTBY (A/D standby bit) (b5)

If the ADSTBY bit is changed from 0 (A/D operation stopped) to 1 (A/D operation enabled), wait for one ϕAD cycle or more before starting A/D conversion.

When the A/D converter is not used, no current flows in the A/D converter by setting the ADSTBY bit to 0 (A/D operation stopped: standby). This helps reduce power consumption.

26.3 Operations

26.3.1 A/D Conversion Cycle

A/D conversion cycle is based on fAD and ϕAD. Divide fAD so ϕAD conforms the standard frequency. Figure 26.2 shows fAD and ϕAD.

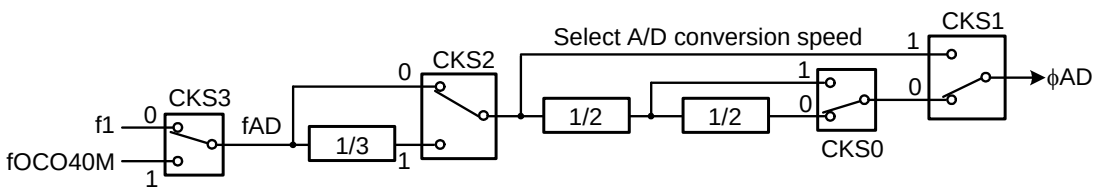


Figure 26.2 fAD and ϕAD

Figure 26.3 shows A/D Conversion Timing.

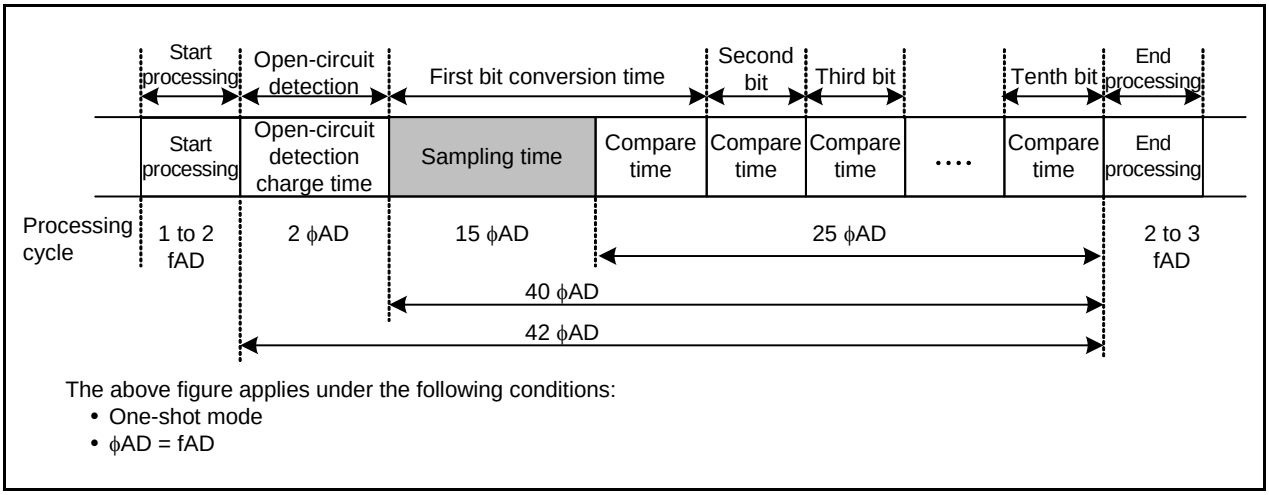


Figure 26.3 A/D Conversion Timing

Table 26.6 lists Cycles of A/D Conversion Item. A/D conversion time is described below.
Start processing time depends on which ϕAD is selected.
A/D conversion starts after the start processing time elapses by setting the ADST bit in the ADCON0 register to 1 (A/D conversion start). When reading the ADST bit before starting A/D conversion, 0 (A/D conversion stop) is read.
When selecting multiple pins, or in a mode which performs A/D conversion multiple times, inter-execution processing time is inserted between A/D conversions.
In one-shot mode and single sweep mode, the ADST bit becomes 0 at the end processing time and the last A/D conversion result is stored in the ADi register.

One-shot mode:
Start processing time + A/D conversion execution time + end processing time
Two pins are selected in single sweep mode:
Start processing time + (A/D conversion execution time + inter-execution processing time + A/D conversion execution time) + end processing time

Table 26.6 Cycles of A/D Conversion Item

A/D Conversion Item		Number of Cycles
Start processing time	ϕAD = fAD	1 to 2 cycles of fAD
	ϕAD = fAD divided by 2	2 to 3 cycles of fAD
	ϕAD = fAD divided by 3	3 to 4 cycles of fAD
	ϕAD = fAD divided by 4	3 to 4 cycles of fAD
	ϕAD = fAD divided by 6	4 to 5 cycles of fAD
	ϕAD = fAD divided by 12	7 to 8 cycles of fAD
A/D conversion execution time	Open-circuit detection disabled	40 cycles of ϕAD
	Open-circuit detection enabled	42 cycles of ϕAD
Inter-execution processing time		1 cycle of ϕAD
End processing time		2 to 3 cycles of fAD

26.3.2 A/D Conversion Start Conditions

An A/D conversion start trigger has a software trigger and an external trigger. Figure 26.4 shows A/D Conversion Start Trigger.

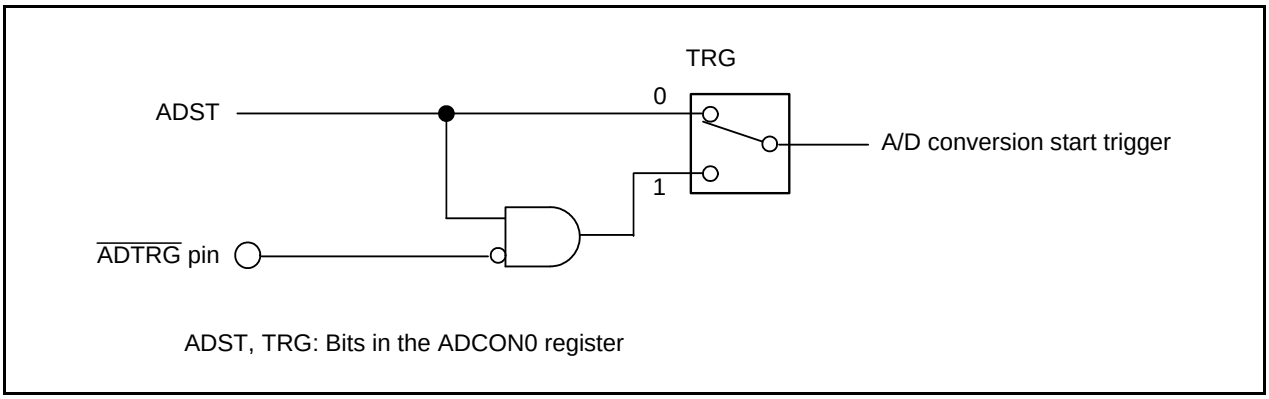


Figure 26.4 A/D Conversion Start Trigger

26.3.2.1 Software Trigger

The software trigger is enabled when the TRG bit in the ADCON0 register is 0 (software trigger). A/D conversion starts by setting the ADST bit in the ADCON0 register to 1 (A/D conversion start).

26.3.2.2 External Trigger

The external trigger is enabled when the TRG bit in the ADCON0 register is 1 ($\overline{\text{ADTRG}}$ trigger). To use this trigger, set the following:

- The direction bit of the port which shares a pin with $\overline{\text{ADTRG}}$ is 0 (input mode).
- The TRG bit in the ADCON0 register is 1 ($\overline{\text{ADTRG}}$ trigger).
- The ADST bit in the ADCON0 register is 1 (A/D conversion start).

Under the above conditions, when input to the $\overline{\text{ADTRG}}$ pin is changed from high to low, A/D conversion starts.

Set the high- and low-level durations of the pulse input to the $\overline{\text{ADTRG}}$ pin to two or more cycles of fAD.

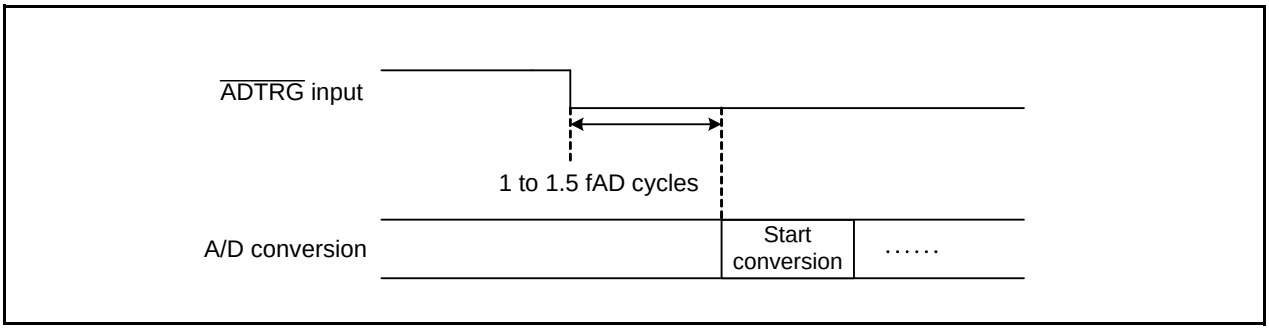


Figure 26.5 A/D Conversion Start Timing When External Trigger Input

26.3.3 A/D Conversion Result

When reading the ADi register before A/D conversion is completed, the undefined value is read. Read the ADi register after completing A/D conversion. Use the following procedure to detect the completion of A/D conversion.

- In one-shot mode and single sweep mode:
  The IR bit in the ADIC register becomes 1 (interrupt requested) at a completion of A/D conversion. Ensure that the IR bit becomes 1 to read the ADi register.
  When not using an A/D interrupt, set the IR bit to 0 (interrupt not requested) by a program after reading the ADi register.

- In repeat mode, repeat sweep mode 0:
  The IR bit remains unchanged (no interrupt request is generated). At first, read the ADi register after one A/D conversion time elapses (refer to 26.3.1 “A/D Conversion Cycle”). After that, whenever the ADi register is read, the conversion result which has been obtained before reading is read.
  The ADi register is overwritten after every A/D conversion. Read the value before the ADi register is overwritten.

26.3.4 Current Consumption Reduce Function

When the A/D converter is not in use, power consumption can be reduced by setting the ADSTBY bit in the ADCON1 register to 0 (A/D operation stopped: standby) to shut off any analog circuit current flow.
To use the A/D converter, set the ADSTBY bit to 1 (A/D operation enabled) and wait for one ϕAD cycle or more before setting the ADST bit in the ADCON0 register to 1 (A/D conversion start). Do not set bits ADST and ADSTBY to 1 at the same time.
Also, do not set the ADSTBY bit to 0 (A/D operation stopped: standby) during A/D conversion.

26.3.5 Open-Circuit Detection Assist Function

The A/D converter has a function to set the charge of the sampling capacitor to a predefined state (AVCC or AVSS) before A/D conversion starts. This helps prevent the influence of analog input voltage from the previous conversion and more reliably detect an open-circuit of a trace connected to an analog input pin.
Figure 26.6 shows A/D Open-Circuit Detection Example on AVCC (Preconversion Charge) and Figure 26.7 shows A/D Open-Circuit Detection Example on AVSS (Preconversion discharge).
The conversion result in open-circuit depends on the external circuit. Use this function only after careful evaluation of the system.

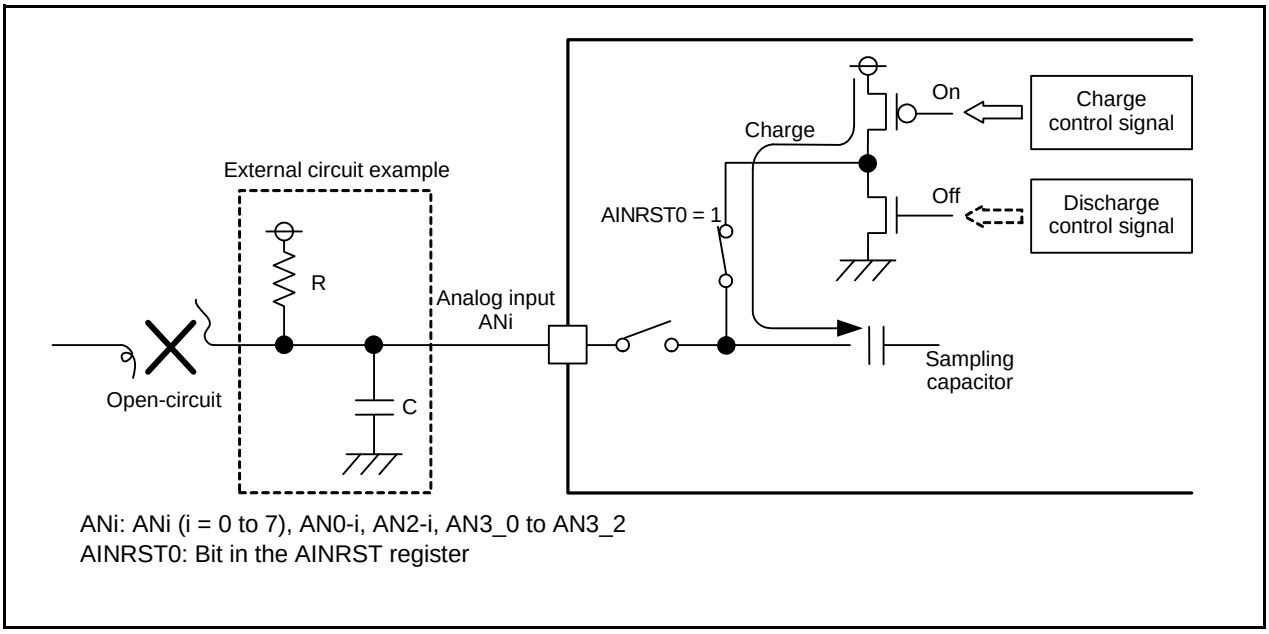


Figure 26.6 A/D Open-Circuit Detection Example on AVCC (Preconversion Charge)

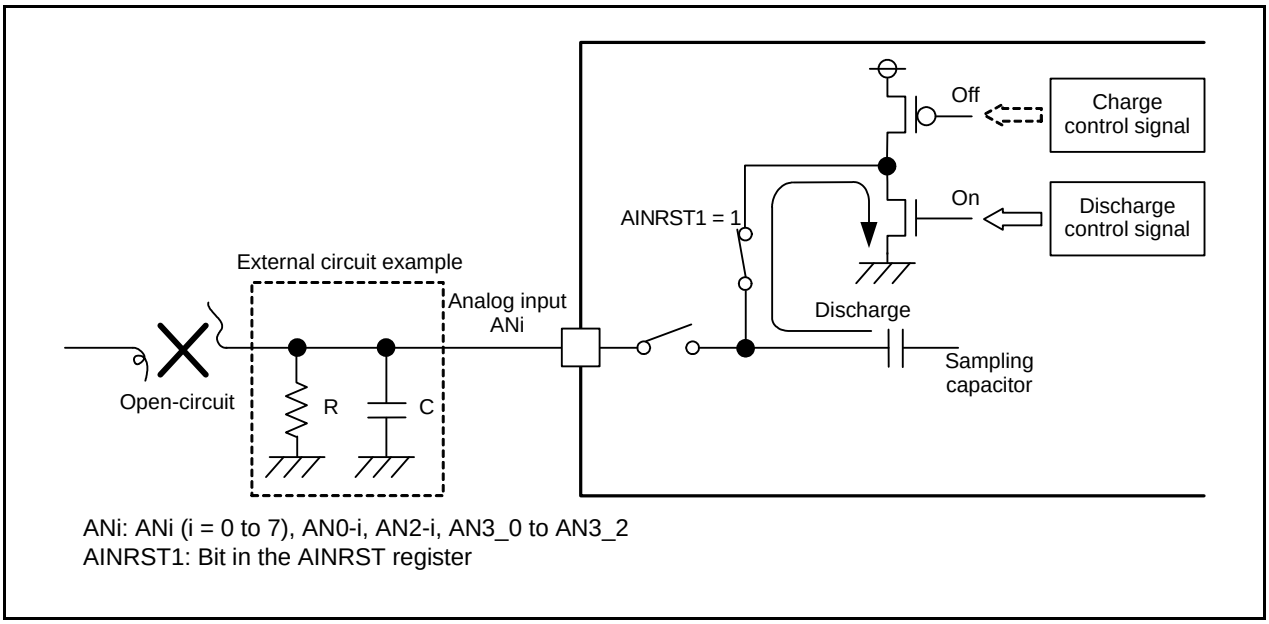


Figure 26.7 A/D Open-Circuit Detection Example on AVSS (Preconversion discharge)

26.4 Operational Modes

26.4.1 One-Shot Mode

In one-shot mode, the analog voltage applied to a selected pin is converted to a digital code once. Table 26.7 lists One-Shot Mode Specifications.

Table 26.7 One-Shot Mode Specifications

Item	Specification
Function	Bits CH2 to CH0 in the ADCON0 register and bits ADGSEL1 to ADGSEL0 in the ADCON2 register are used to select a pin. The analog voltage applied to the pin is converted to a digital code once.
A/D conversion start conditions	• When the TRG bit in the ADCON0 register is 0 (software trigger) the ADST bit in the ADCON0 register is set to 1 (A/D conversion starts). • When the TRG bit is 1 ($\overline{\text{ADTRG}}$ trigger) the input level at the $\overline{\text{ADTRG}}$ pin changes from high to low after the ADST bit is set to 1 (A/D conversion start).
A/D conversion stop conditions	• Completion of A/D conversion (if a software trigger is selected, the ADST bit becomes 0 (A/D conversion stop)). • Set the ADST bit to 0.
Interrupt request generation timing	Completion of A/D conversion.
Analog input pin	Select one pin from AN0 to AN7, AN0_0 to AN0_7, AN2_0 to AN2_7, or AN3_0 to AN3_2.
Reading of A/D conversion result	Read the register among AD0 to AD7 that corresponds to the selected pin.

Table 26.8 Registers and Settings in One-Shot Mode (1)

Register	Bit	Setting
AINRST	AINRST1, AINRST0	Select whether open-circuit detection assist function is used or not.
AD0 to AD7	b9 to b0	A/D conversion result can be read.
ADCON2	ADGSEL1, ADGSEL0	Select analog input pin group.
	CKS2	Select ϕAD frequency.
ADCON0	CH2 to CH0	Select analog input pin.
	MD1 to MD0	Set to 00b.
	TRG	Select a trigger.
	ADST	Set to 1 to start A/D conversion and set to 0 to stop it.
	CKS0	Select ϕAD frequency.
ADCON1	SCAN1, SCAN0	Disabled
	CKS1	Select ϕAD frequency.
	ADSTBY	Set to 1 when performing A/D conversion.

Note:
1. This table does not describe a procedure.

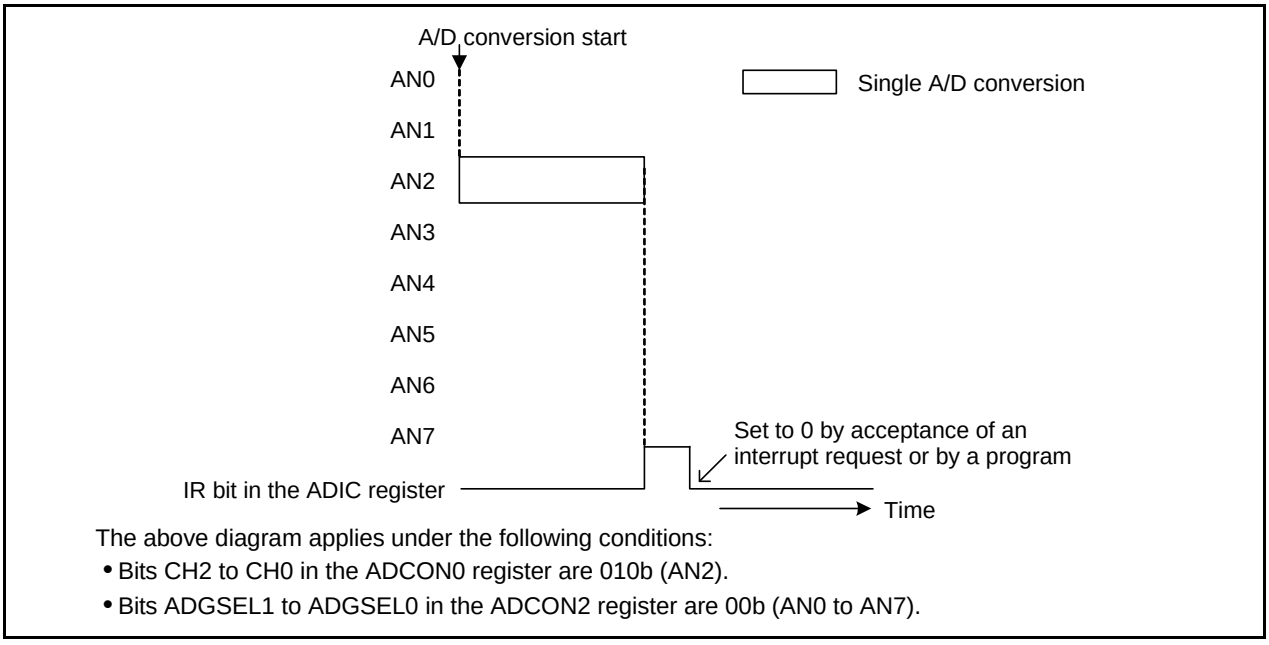


Figure 26.8 Operation Example in One-Shot Mode

26.4.2 Repeat Mode

In repeat mode, the analog voltage applied to a selected pin is repeatedly converted to a digital code. Table 26.9 lists Repeat Mode Specifications.

Table 26.9 Repeat Mode Specifications

Item	Specification
Function	Bits CH2 to CH0 in the ADCON0 register and bits ADGSEL1 to ADGSEL0 in the ADCON2 register are used to select a pin. The analog voltage applied to the pin is repeatedly converted to a digital code.
A/D conversion start conditions	• When the TRG bit in the ADCON0 register is 0 (software trigger) the ADST bit in the ADCON0 register is set to 1 (A/D conversion start). • When the TRG bit is 1 ($\overline{\text{ADTRG}}$ trigger) the input level at the $\overline{\text{ADTRG}}$ pin changes from high to low after the ADST bit is set to 1 (A/D conversion start).
A/D conversion stop condition	Set the ADST bit to 0 (A/D conversion stop).
Interrupt request generation timing	No interrupt requests generated
Analog input pin	Select one pin from among AN0 to AN7, AN0_0 to AN0_7, AN2_0 to AN2_7, or AN3_0 to AN3_2.
Reading of A/D conversion result	Read the register among AD0 to AD7 that corresponds to the selected pin.

Table 26.10 Registers and Settings in Repeat Mode (1)

Register	Bit	Setting
AINRST	AINRST1, AINRST0	Select whether open-circuit detection assist function is used or not.
AD0 to AD7	b9 to b0	A/D conversion result can be read.
ADCON2	ADGSEL1, ADGSEL0	Select analog input pin group.
	CKS2	Select ϕAD frequency.
ADCON0	CH2 to CH0	Select analog input pin.
	MD1 to MD0	Set to 01b.
	TRG	Select a trigger.
	ADST	Set to 1 to start A/D conversion and set to 0 to stop it.
	CKS0	Select ϕAD frequency.
ADCON1	SCAN1, SCAN0	Disabled
	CKS1	Select ϕAD frequency.
	ADSTBY	Set to 1 when performing A/D conversion.

Note:
1. This table does not describe a procedure.

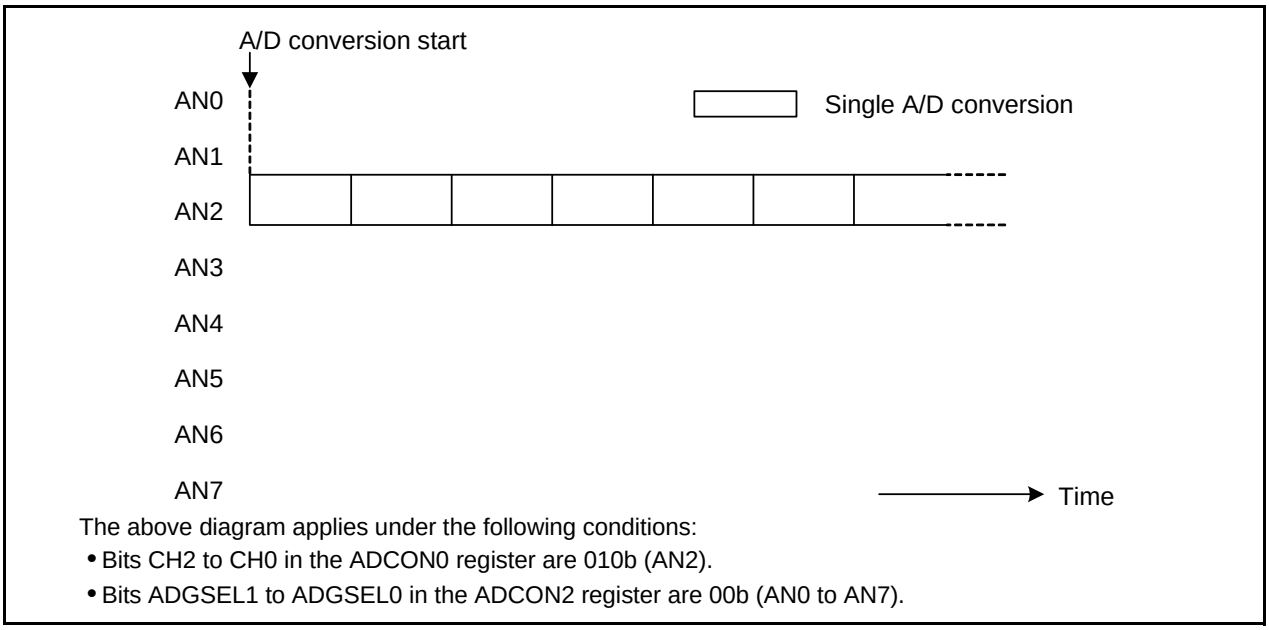


Figure 26.9 Operation Example in Repeat Mode

26.4.3 Single Sweep Mode

In single sweep mode, the analog voltage applied to selected pins is converted one-by-one to a digital code. Table 26.11 lists the Single Sweep Mode Specifications.

Table 26.11 Single Sweep Mode Specifications

Item	Specification
Function	Bits SCAN1 to SCAN0 in the ADCON1 register and bits ADGSEL1 to ADGSEL0 in the ADCON2 register are used to select pins. The analog voltage applied to the pins is converted one-by-one to a digital code.
A/D conversion start conditions	• When the TRG bit in the ADCON0 register is 0 (software trigger) the ADST bit in the ADCON0 register is set to 1 (A/D conversion start). • When the TRG bit is 1 ($\overline{\text{ADTRG}}$ trigger) the input level at the $\overline{\text{ADTRG}}$ pin changes from high to low after the ADST bit is set to 1 (A/D conversion start).
A/D conversion stop conditions	• Completion of A/D conversion (if a software trigger is selected, the ADST bit is set to 0 (A/D conversion stop)). • Set the ADST bit to 0.
Interrupt request generation timing	Completion of A/D conversion
Analog input pin	Select one of the following groupings from AN0 to AN7: 2 pins: AN0 and AN1 4 pins: AN0 to AN3 6 pins: AN0 to AN5 8 pins: AN0 to AN7 AN0_0 to AN0_7, AN2_0 to AN2_7, and AN3_0 to AN3_2 can also be selected in the same way.
Reading of A/D conversion result	Read the registers among AD0 to AD7 that corresponds to the selected pin.

Table 26.12 Registers and Settings in Single Sweep Mode (1)

Register	Bit	Setting
AINRST	AINRST1, AINRST0	Select whether open-circuit detection assist function is used or not.
AD0 to AD7	b9 to b0	A/D conversion result can be read.
ADCON2	ADGSEL1, ADGSEL0	Select analog input pin group.
	CKS2	Select ϕAD frequency.
ADCON0	CH2 to CH0	Disabled
	MD1 to MD0	Set to 10b.
	TRG	Select a trigger.
	ADST	Set to 1 to start A/D conversion and set to 0 to stop it.
	CKS0	Select ϕAD frequency.
ADCON1	SCAN1, SCAN0	Select analog input pin.
	CKS1	Select ϕAD frequency.
	ADSTBY	Set to 1 when performing A/D conversion.

Note:
1. This table does not describe a procedure.

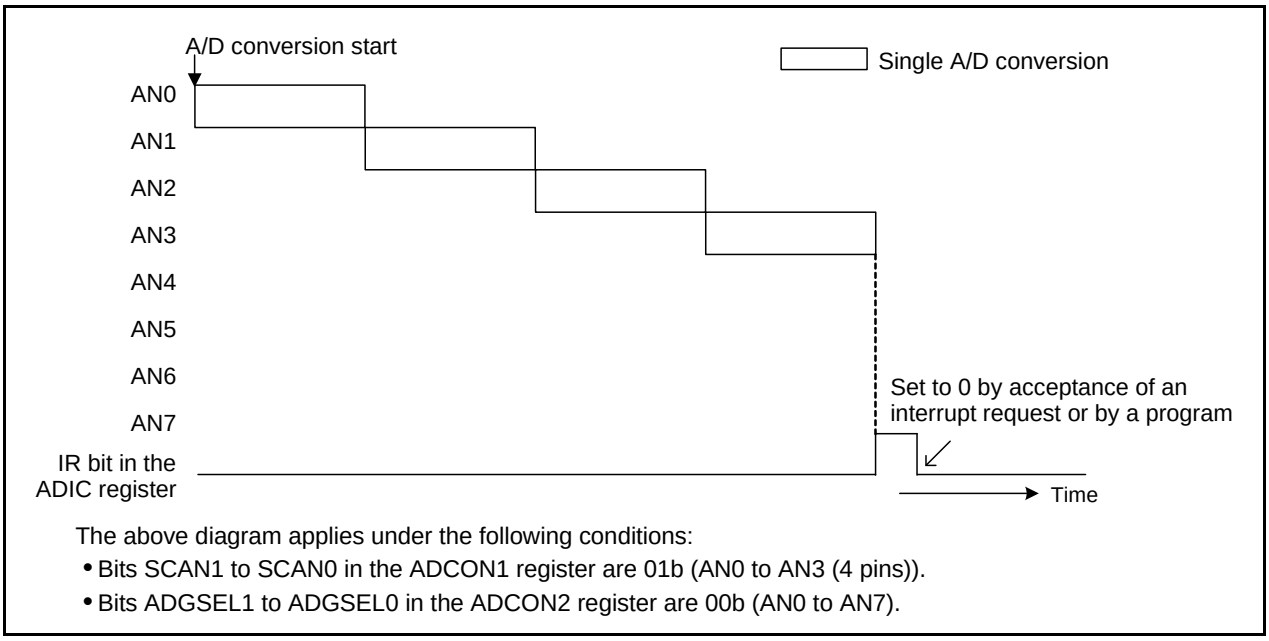


Figure 26.10 Operation Example in Single Sweep Mode

26.4.4 Repeat Sweep Mode 0

In repeat sweep mode 0, the analog voltage applied to selected pins is repeatedly converted to a digital code. Table 26.13 lists the Repeat Sweep Mode 0 Specifications.

Table 26.13 Repeat Sweep Mode 0 Specifications

Item	Specification
Function	Bits SCAN1 to SCAN0 in the ADCON1 register and bits ADGSEL1 to ADGSEL0 in the ADCON2 register are used to select pins. Analog voltage applied to the pins is repeatedly converted to a digital code.
A/D conversion start conditions	• When the TRG bit in the ADCON0 register is 0 (software trigger) the ADST bit in the ADCON0 register is set to 1 (A/D conversion start). • When the TRG bit is 1 ($\overline{\text{ADTRG}}$ trigger) the input level at the $\overline{\text{ADTRG}}$ pin changes from high to low after the ADST bit is set to 1 (A/D conversion start).
A/D conversion stop condition	Set the ADST bit to 0 (A/D conversion stop).
Interrupt request generation timing	No interrupt requests generated
Analog input pin	Select one of the following groupings from AN0 to AN7: 2 pins: AN0 and AN1 4 pins: AN0 to AN3 6 pins: AN0 to AN5 8 pins: AN0 to AN7 AN0_0 to AN0_7, AN2_0 to AN2_7, and AN3_0 to AN3_2 can also be selected in the same way.
Reading of A/D conversion result	Read the registers among AD0 to AD7 that correspond to the selected pins.

Table 26.14 Registers and Settings in Repeat Sweep Mode 0 (1)

Register	Bit	Setting
AINRST	AINRST1, AINRST0	Select whether open-circuit detection assist function is used or not.
AD0 to AD7	b9 to b0	A/D conversion result can be read.
ADCON2	ADGSEL1, ADGSEL0	Select analog input pin group.
	CKS2	Select ϕAD frequency.
ADCON0	CH2 to CH0	Disabled
	MD1 to MD0	Set to 11b.
	TRG	Select a trigger.
	ADST	Set to 1 to start A/D conversion and set to 0 to stop it.
	CKS0	Select ϕAD frequency.
ADCON1	SCAN1, SCAN0	Select analog input pin.
	CKS1	Select ϕAD frequency.
	ADSTBY	Set to 1 when performing A/D conversion.

Note:
1. This table does not describe a procedure.

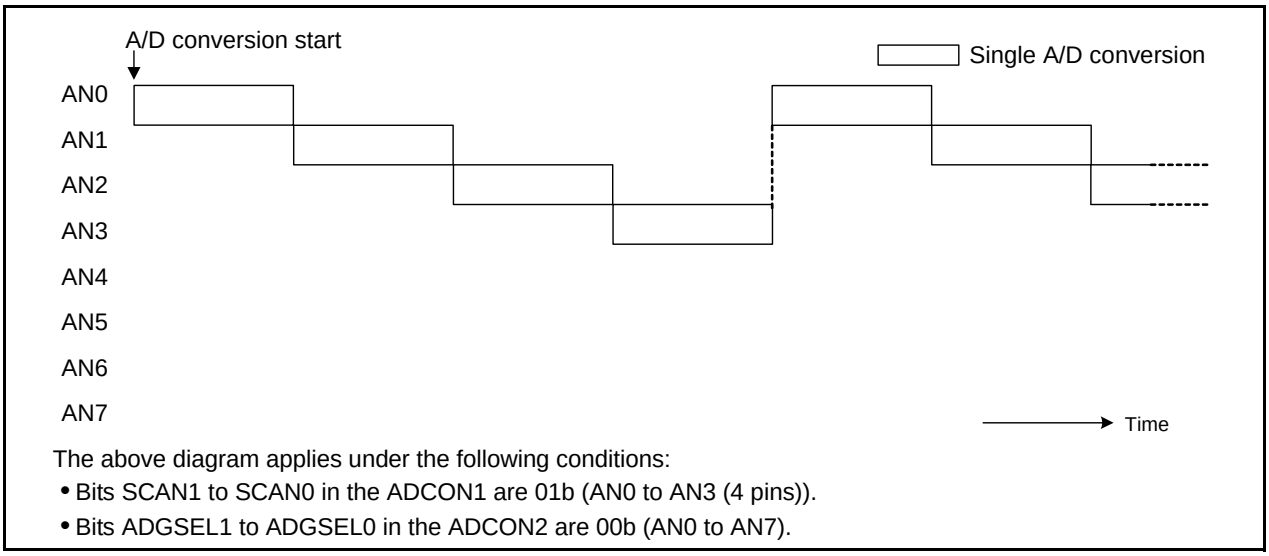


Figure 26.11 Operation Example in Repeat Sweep Mode 0

26.5 External Sensor

To perform A/D conversion accurately, charging the internal capacitor C shown in Figure 26.12 must be completed within a specified period of time.

T: Specified period of time (sampling time)
R0: Output impedance of sensor equivalent circuit
R: Internal resistance of the MCU
X: Precision (error) of the A/D converter
Y: Resolution of the A/D converter be Y (Y is 1024)

Generally, $VC = VIN\left\{1 - e^{-\frac{1}{C(R0+R)}t}\right\}$

When t = T, $VC = VIN - \frac{X}{Y}VIN = VIN\left(1 - \frac{X}{Y}\right)$

$$e^{-\frac{1}{C(R0+R)}T} = \frac{X}{Y}$$

$$-\frac{1}{C(R0+R)}T = \ln\frac{X}{Y}$$

Therefore, $R0 = -\frac{T}{C \bullet \ln\frac{X}{Y}} - R$

Figure 26.12 shows Analog Input Pin and External Sensor Equivalent Circuit. Impedance R0 by which voltage VC between pins of the capacitor C changes from 0 to VIN - (0.1/1024)VIN in time T when the difference between VIN and VC is 0.1LSB is obtained. (0.1/1024) means that A/D precision drop due to insufficient capacitor charge is kept to 0.1LSB in A/D conversion. However, the actual error is the value of absolute accuracy added to 0.1LSB.
When ϕAD is 20 MHz, T is 0.75 μs. Output impedance R0 for charging capacitor C sufficiently within time T is obtained as follows.

T = 0.75 μs, R = 10 kΩ, C = 6.0 pF, X = 0.1, and Y = 1024. Therefore,

$$R0 = -\frac{0.75 \times 10^{-6}}{6.0 \times 10^{-12} \bullet \ln\frac{0.1}{1024}} - 10 \times 10^{3} \approx 3.5 \times 10^{3}$$

Thus, the output impedance R0 of the sensor equivalent circuit, making the A/D converter precision (error) 0.1LSB or less, is up to 3.5 kΩ.

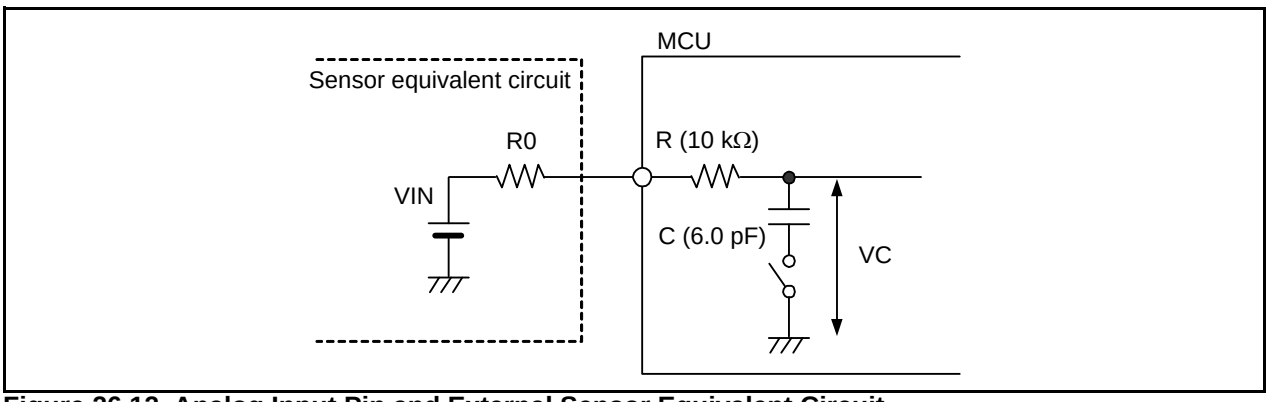


Figure 26.12 Analog Input Pin and External Sensor Equivalent Circuit

26.6 Interrupt

Refer to the operation examples for timing of generating interrupt requests.
Also, refer to 12.7 “Interrupt Control” for details. Table 26.15 lists Registers Associated with A/D Converter Interrupt.

Table 26.15 Registers Associated with A/D Converter Interrupt

Address	Register	Symbol	Reset Value
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXX X000b

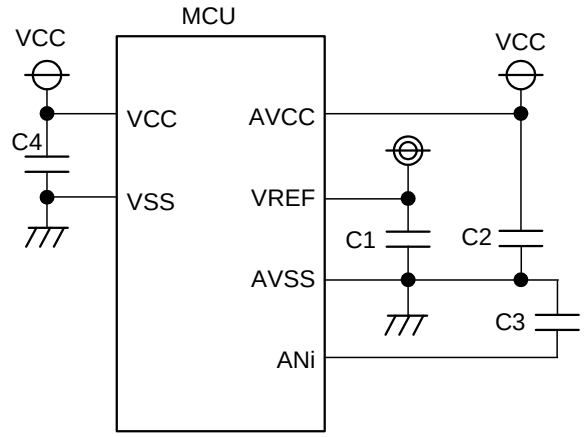
26.7 Notes on A/D Converter

26.7.1 Analog Input Pin

Do not use any pin from AN4 to AN7 as analog input pin if any pin from $\overline{KI0}$ to $\overline{KI3}$ is used as a key input interrupt.

26.7.2 Pin Configuration

To prevent operation errors due to noise or latchup, and to reduce conversion errors, place capacitors between the AVSS pin and the AVCC pin, the VREF pin, and analog inputs (ANi (i = 0 to 7), AN0_i, AN2_i, and AN3_0 to AN3_2). Also, place a capacitor between the VCC pin and VSS pin.



ANi: ANi (i = 0 to 7), AN0_i, AN2_i, and AN3_0 to AN3_2

Notes:
1. Reference values: C1 ≥ 0.47 μF, C2 ≥ 0.47 μF, C3 ≥ 100 pF, C4 ≥ 0.1 μF
2. The traces for the capacitor and MCU should be as short and as wide as much as physically possible.

Figure 26.13 Example of Pin Configuration

26.7.3 Register Access

Set registers associated with A/D converter after setting the CKS3 bit in the ADCON2 register. However the other bits in the ADCON2 register and the CKS3 bit can be set at the same time. After changing the CKS3 bit, set the others in the same way.

Write registers ADCON0 (excluding the ADST bit), ADCON1, and ADCON2 when A/D conversion stops (before a trigger is generated).

After A/D conversion stops, set the ADSTBY bit in the ADCON1 register from 1 to 0.

26.7.4 A/D Conversion Start

When rewriting the ADSTBY bit in the ADCON1 register from 0 (A/D operation stopped) to 1 (A/D operation enabled), wait for one ϕAD cycle or more before starting A/D conversion.

26.7.5 A/D Operation Mode Change

When the A/D operation mode has been changed, reselect analog input pins by using bits CH2 to CH0 in the ADCON0 register or bits SCAN1 to SCAN0 in the ADCON1 register.

26.7.6 State When Forcibly Terminated

If A/D conversion in progress is halted by setting the ADST bit in the ADCON0 register to 0 (A/D conversion stopped), the conversion result is undefined. In addition, the unconverted ADi register (i = 0 to 7) may also become undefined. Do not use any value in ADi registers when setting the ADST bit to 0 by a program during A/D conversion.

26.7.7 A/D Open-Circuit Detection Assist Function

The conversion result in open-circuit depends on the external circuit. Use this function only after careful evaluation of the system.

When A/D conversion starts after changing the AINRST register, follow these steps:

(1) Change bits AINRST1 to AINRST0 in the AINRST register.
(2) Wait for one cycle of ϕAD.
(3) Set the ADST bit in the ADCON0 register to 1 (A/D conversion started).

26.7.8 Detecting Completion of A/D Conversion

In one-shot mode and single sweep mode, use the IR bit in the ADIC register to detect completion of A/D conversion. When not using an interrupt, set the IR bit to 0 by a program after detection.

When 1 is written to the ADST bit in the ADCON0 register, the ADST bit becomes 1 (A/D conversion start) after start processing time elapses (see Table 26.6 “Cycles of A/D Conversion Item”). Therefore when reading the ADST bit immediately after writing 1, 0 (A/D conversion stop) may be read.

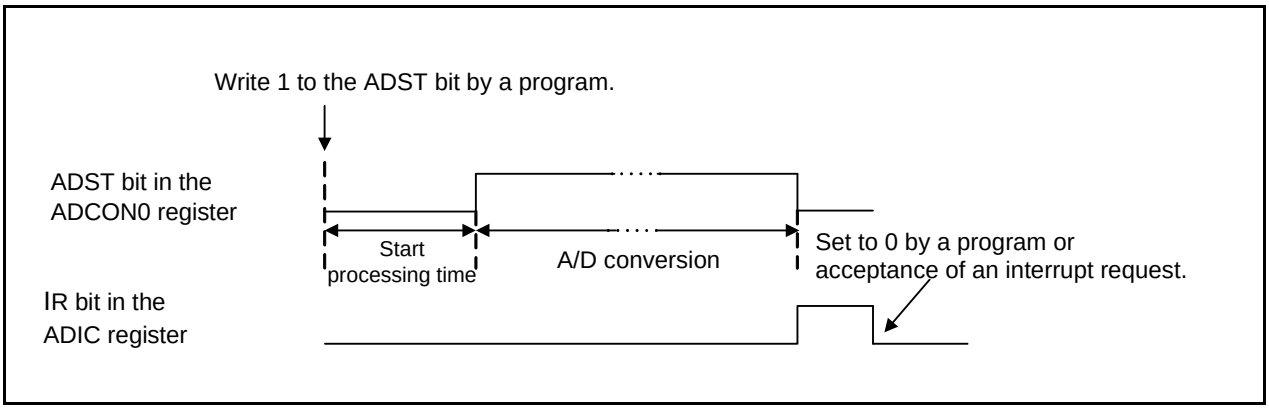


Figure 26.14 ADST Bit Operation

26.7.9 ϕAD

Divide fAD so ϕAD conforms to the standard frequency.

In particular, consider the maximum and minimum values of fOCO40M when the CKS3 bit in the ADCON2 register is 1 (fOCO40M is fAD).

27. D/A Converter

27.1 Introduction

The D/A converter is an 8-bit, R-2R type converter. Table 27.1 lists the D/A Converter Specifications and Figure 27.1 shows the D/A Converter Block Diagram.

Table 27.1 D/A Converter Specifications

Item	Specification
D/A conversion method	R-2R
Resolution	8 bits

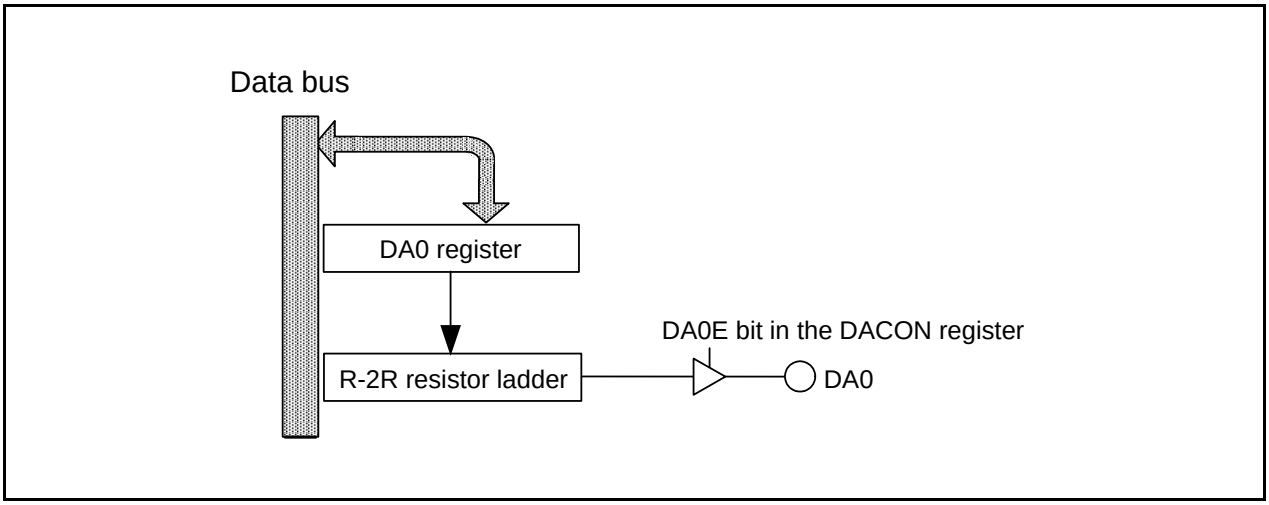


Figure 27.1 D/A Converter Block Diagram

Table 27.2 I/O Ports

Pin Name	I/O	Function
DA0	Output (1)	D/A comparator output

Note:
1. Set the direction bit of the ports sharing a pin to 0 (input mode). When the DA0E bit in the DACON register is set to 1 (output enabled), the corresponding port cannot be pulled up.

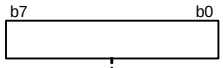
27.2 Registers

Table 27.3 Registers

Address	Register	Symbol	Reset Value
03D8h	D/A0 Register	DA0	00h
03DCh	D/A Control Register	DACON	00h

27.2.1 D/A0 Register (DA0)

D/A0 Register

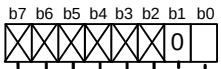


Symbol	Address	Reset Value
DA0	03D8h	00h

Function	Setting Range	RW
Output value of D/A conversion	00h to FFh	RW

27.2.2 D/A Control Register (DACON)

D/A Control Register



Symbol	Address	Reset Value
DACON	03DCh	00h

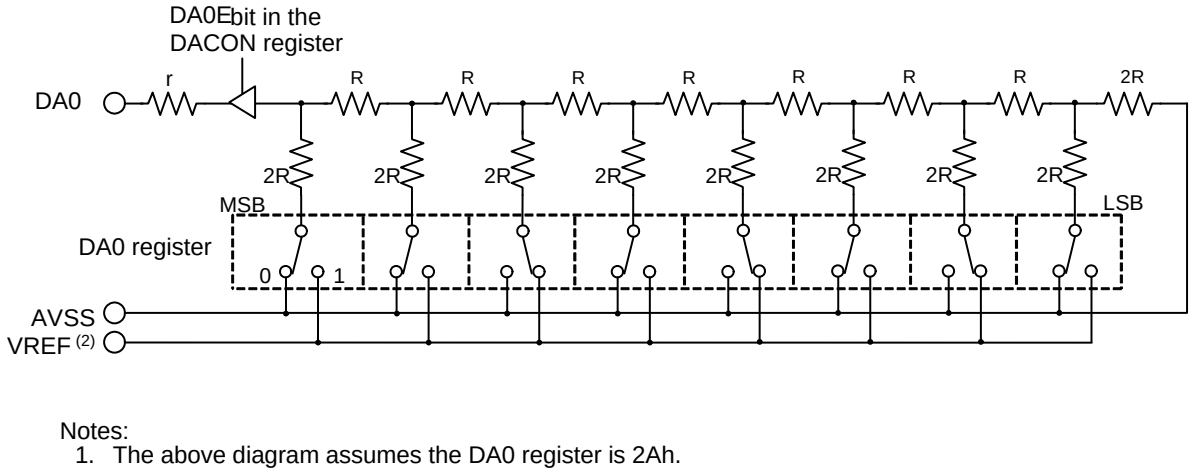
Bit Symbol	Bit Name	Function	RW
DA0E	D/A 0 output enable bit	0 : Output disabled 1 : Output enabled	RW
— (b1)	Reserved bit	Set to 0	RW
— (b7-b2)	No register bits. If necessary, set to 0. The read value is 0.		—

27.3 Operations

D/A conversion is performed by writing a value to the DA0 register.
Output analog voltage (V) is determined by the value n (n = decimal) set in the DA0 register.

$V = VREF \times \frac{n}{256}$ (n = 0 to 255)

VREF: Reference voltage
Figure 27.2 shows the D/A Converter Equivalent Circuit.



Notes:
1. The above diagram assumes the DA0 register is 2Ah.
2. VREF is not related to the ADSTBY bit in the ADCON1 register.

Figure 27.2 D/A Converter Equivalent Circuit

27.4 Notes on D/A Converter

27.4.1 When Not Using the D/A Converter

When not using the D/A converter, set the DA0E bit in the DACON register to 0 (output disabled) and the DA0 register to 00h in order to minimize unnecessary current consumption and prevent current flow to the R-2R resistor.

28. CRC Calculator

28.1 Introduction

The cyclic redundancy check (CRC) calculator detects errors in data blocks. This CRC calculator is enhanced by an additional feature, the CRC snoop, in order to monitor reads from and writes to a certain SFR address, and perform CRC calculations automatically on the data read from and data written to the aforementioned SFR address.

Table 28.1 CRC Calculator Specifications

Item	Specification
Generator polynomial	CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) or CRC-16 ($X^{16} + X^{15} + X^2 + 1$)
Selectable functions	• MSB/LSB selectable • CRC snoop

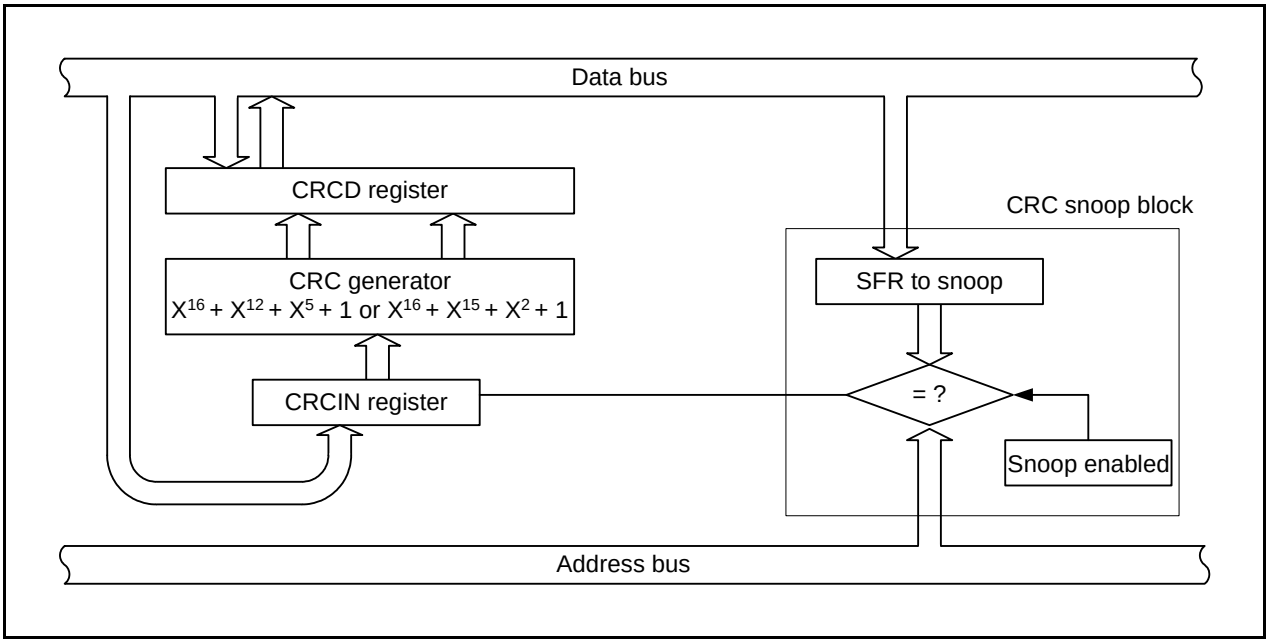


Figure 28.1 CRC Calculator Block Diagram

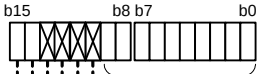
28.2 Registers

Table 28.2 Registers

Address	Register	Symbol	Reset Value
03B4h	SFR Snoop Address Register	CRCSAR	XXXX XXXXb
03B5h			00XX XXXXb
03B6h	CRC Mode Register	CRCMR	0XXX XXX0b
03BCh	CRC Data Register	CRCD	XXh
03BDh			XXh
03BEh	CRC Input Register	CRCIN	XXh

28.2.1 SFR Snoop Address Register (CRCSAR)

SFR Snoop Address Register



Symbol: CRCSAR
Address: 03B5h to 03B4h
Reset Value: 00XX XXXX XXXX XXXXb

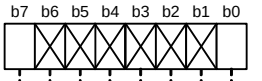
Bit Symbol	Bit Name	Function	RW
CRCSAR9 to CRCSAR0	SFR snoop address bit	Set the SFR address to snoop	RW
— (b13-b10)	No register bits. If necessary, set to 0. The read value is undefined.		—
CRCSR	Snoop-on-read enable bit	0: Disabled 1: Enabled	RW
CRCSW	Snoop-on-write enable bit	0: Disabled 1: Enabled	RW

CRCSR (Snoop-on-read enable bit) (b14)
CRCSW (Snoop-on-write enable bit) (b15)

Do not set bits CRCSR and CRCSW to 1 at the same time. Set the CRCSR bit to 0 when the CRCSW bit is 1. Set the CRCSW bit to 0 when the CRCSR bit is 1.

28.2.2 CRC Mode Register (CRCMR)

CRC Mode Register

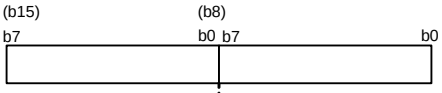


Symbol	Address	Reset Value
CRCMR	03B6h	0XXX XXX0b

Bit Symbol	Bit Name	Function	RW
CRCPS	CRC polynomial select bit	0: $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT) 1: $X^{16} + X^{15} + X^2 + 1$ (CRC-16)	RW
— (b6-b1)	No register bits. If necessary, set to 0. The read value is undefined.		—
CRCMS	CRC mode select bit	0: LSB first 1: MSB first	RW

28.2.3 CRC Data Register (CRCD)

CRC Data Register

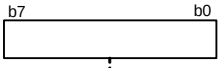


Symbol	Address	Reset Value
CRCD	03BDh to 03BCh	Undefined

Function	Setting Range	RW
When data is written to the CRCIN register after setting the initial value in the CRCD register, the CRC code can be read from this register.	0000h to FFFFh	RW

28.2.4 CRC Input Register (CRCIN)

CRC Input Register



Symbol	Address	Reset Value
CRCIN	03BEh	Undefined

Function	Setting Range	RW
Data input	00h to FFh	RW

28.3 Operations

28.3.1 Basic Operation

The CRC (Cyclic Redundancy Check) calculator detects errors in data blocks. The MCU uses two generator polynomials to generate CRC: CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) and CRC-16 ($X^{16} + X^{15} + X^2 + 1$).

The CRC code is 16-bit code generated for a given length of a data block in 8-bit units. After setting the default value in the CRCD register, the CRC code is stored in the CRCD register every time 1-byte of data is written to the CRCIN register. CRC code generation for 1-byte data is completed in two CPU clock cycles.

28.3.2 CRC Snoop

The CRC snoop monitors reads from and writes to a certain SFR address and performs CRC calculation on the data read from and written to the aforementioned SFR address automatically. Because the CRC snoop recognizes writes to and reads from a certain SFR address as a trigger to automatically perform CRC calculation, there is no need to write data to the CRCIN register. All SFR addresses from 0020h to 03FFh are subject to the CRC snoop. The CRC snoop is useful in monitoring writes to the UART transmit buffer, and reads from the UART receive buffer.

To use this function, write a target SFR address to bits CRCSAR9 to CRCSAR0 in the CRCSAR register. Then, set the CRCSW bit in the CRCSAR register to 1 to enable snooping on writes to the target, or set the CRCSR bit in the CRCSAR register to 1 to enable snooping on reads from the target.

When setting the CRCSW bit to 1 and writing data to a target SFR address by CPU or DMA, the CRC calculator stores the data in the CRCIN register and performs CRC calculation. Similarly, when setting the CRCSR bit to 1 and reading data in a target SFR address by CPU or DMA, the CRC calculator stores the data in the CRCIN register and performs CRC calculation.

CRC calculation is performed 1-byte at a time. When the target SFR address is accessed in words (16 bits), CRC code is generated on the lower byte (1 byte) of data.

CRC calculation and setting procedure to generate CRC, 80C4h, with CRC-CCITT (LSB first selected)

- CRC calculator specification

CRC: remainder of a division, $\frac{\text{inverted value of the CRCIN register}}{\text{generator polynomial}}$

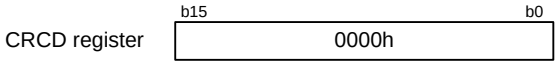
Generator polynomial: $X^{16} + X^{12} + X^5 + 1$ (1 0001 0000 0010 0001b)

- Setting procedures

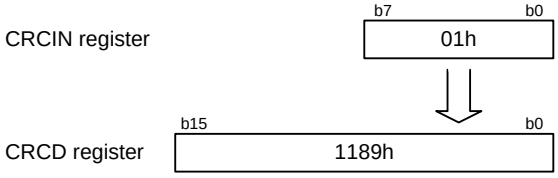
(1) Invert the bit position of the value 80C4h by a program in 1-byte units.

80h → 01h, C4h→23h

(2) Write 0000h (initial value) to the CRCD register.

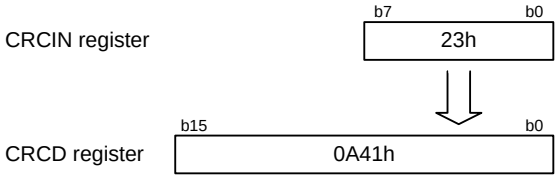


(3) Write 01h (inverted value of 80h) to the CRCIN register.



After two cycles, 1189h, which is a bit-position-inverse value of 9188h (CRC for 80h) is stored in the CRCD register.

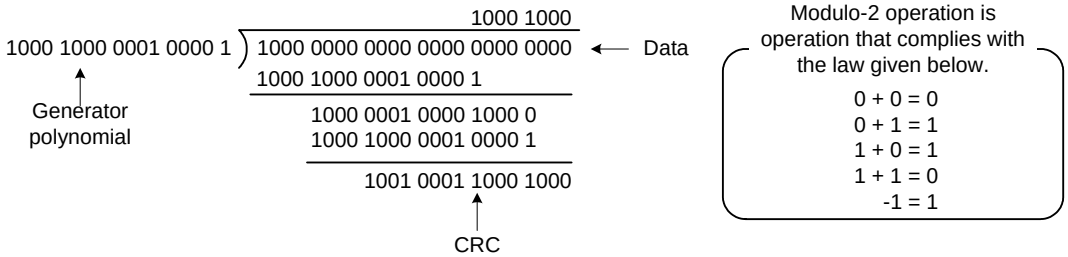
(4) Write 23h (inverted value of C4h) to the CRCIN register.



After two cycles, 0A41h, which is a bit-position-inverse value of 8250h (CRC for 80C4h) is stored in the CRCD register.

- Details on CRC calculation

As shown in (3) above, bit position of 01h (0000 0001b) written to the CRCIN register is reversed and becomes 80h (1000 0000b). Add 1000 0000 0000 0000 0000 0000b, as 1000 0000b plus 16 digits, to 0000 0000 0000 0000 0000 0000b, as 0000 0000 0000 0000b plus 8 digits as the default value of the CRCD register to perform the modulo-2 division.



0001 0001 1000 1001b (1189h), the remainder 1001 0001 1000 1000b (9188h) with inversed bit position, can be read from the CRCD register.

When going on to (4) above, 23h (0010 0011b) written in the CRCIN register is inversed and becomes C4h (1100 0100b). Add 1100 0100 0000 0000 0000 0000b, as 1100 0100b plus 16 digits, to 1001 0001 1000 1000 0000 0000b, as 1001 0001 1000 1000b plus 8 digits as a remainder of (3) left in the CRCD register to perform the modulo-2 division. 0000 1010 0100 0001b (0A41h), the remainder 1000 0010 0101 0000b (8250h) with inversed bit position, can be read from the CRCD register.

Figure 28.2 CRC Calculation When Using CRC-CCITT

CRC calculation and setting procedure to generate CRC, 80C4h with CRC-16 (MSB first selected)

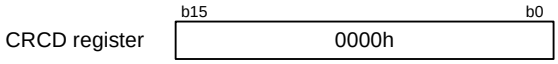
- CRC operation specification

CRC: remainder of a division, $\frac{\text{the CRCIN register}}{\text{generator polynomial}}$

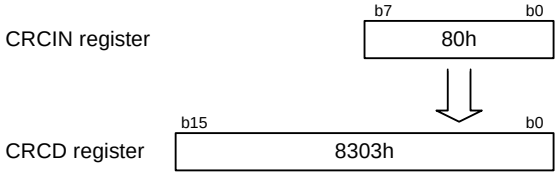
Generator polynomial: $X^{16} + X^{15} + X^2 + 1$ (1 1000 0000 0000 0101b)

- Setting procedures

(1) Write 0000h (initial value) to the CRCD register.

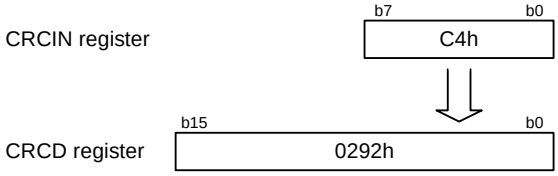


(2) Write 80h to the CRCIN register.



After two cycles, 8303h (CRC for 80h) is stored in the CRCD register.

(3) Write C4h to the CRCIN register.



After two cycles, 0292h (CRC for 80C4h) is stored in the CRCD register.

- Details on CRC calculation

As shown in (2) above, add 1000 0000 0000 0000 0000 0000b, as 80h (1000 0000b) written in the CRCIN register plus 16 digits, to 0000 0000 0000 0000 0000 0000b, as 0000 0000 0000 0000b plus 8 digits as the default value of the CRCD register. Perform the modulo-2 division on the result. The remainder, 1000 0011 0000 0011b (8303h) can be read from the CRCD register.

When going on to (3) above, add 1100 0100 0000 0000 0000 0000b, as C4h (1100 0100b) written in the CRCIN register plus 16 digits, to 1000 0011 0000 0011 0000 0000b, as 8303h (1000 0011 0000 0011b) plus 8 digits as a remainder of (2) left in the CRCD register to perform the modulo-2 division.
The remainder, 0000 0010 1001 0010b (0292h) can be read from the CRCD register.

Figure 28.3 CRC Calculation When Using CRC-16

29. Flash Memory

Note

Pins P4_0 to P4_7, P5_0 to P5_7, P9_4 cannot be used in the 80-pin package.
Pins P0_4 to P0_7, P1_0 to P1_7, P3_4 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P9_4 to P9_7 cannot be used in the 64-pin package. For the 80-pin package and 64-pin package, do not use these pins for the entry of user boot function.

29.1 Introduction

This product uses flash memory as ROM. In this chapter, flash memory refers to the flash memory inside the MCU.
In this product, the flash memory can perform in three rewrite modes: CPU rewrite mode, standard serial I/O mode, and parallel I/O mode.
Table 29.1 lists Flash Memory Specifications (see Table 1.1 to Table 1.6 “Specifications” for the items not listed in Table 29.1).

Table 29.1 Flash Memory Specifications

Item		Specification
Flash memory rewrite modes		3 modes (CPU rewrite, standard serial I/O, and parallel I/O)
Erase block	Program ROM 1	See Figure 29.1 “Flash Memory Block Diagram”.
	Program ROM 2	1 block (16 KB)
	Data flash	2 blocks (4 KB each)
Program method		In 2-word (4-byte) units
Erase method		Block erase
Program and erase control method		Program and erase controlled by software commands
Suspend function		Program suspend and erase suspend
Protect method		A lock bit protects each block.
Number of commands		8
Program and erase cycles	Program ROM 1 and program ROM 2	1,000 times (1)
	Data flash	10,000 times (1)
Data retention		20 years
Flash memory rewrite disable function		Parallel I/O mode ROM code protect function Standard serial I/O mode ID code check function, forced erase function, and standard serial I/O mode disable function
User boot function		User boot mode

Note:
1. Definition of program and erase cycles:
The program and erase cycles is the number of erase operations performed on a per-block basis. For example, assume that a 4 KB block is programmed in 1,024 operations, writing 2 words at a time, and erased thereafter. In this case, the block is considered to have been programmed and erased once.
If the program and erase cycles are 1,000 times, each block can be erased up to 1,000 times.

Table 29.2 Flash Memory Rewrite Modes Overview

Flash Memory Rewrite Mode	CPU Rewrite Mode	Standard Serial I/O Mode	Parallel I/O Mode
Function	The flash memory is rewritten when the CPU executes software commands. EW0 mode: Rewritable in RAM EW1 mode: Rewritable in the flash memory	The flash memory is rewritten using a dedicated serial programmer. Standard serial I/O mode 1: Clock synchronous serial I/O Standard serial I/O mode 2: 2-wire clock asynchronous serial I/O	The flash memory is rewritten using a dedicated parallel programmer.
Areas which can be rewritten	Program ROM 1, program ROM 2, and data flash	Program ROM 1, program ROM 2, and data flash	Program ROM 1, program ROM 2, and data flash
CPU operating mode	Single-chip mode	Boot mode	Pararell I/O mode
ROM programmer	None	Serial programmer	Parallel programmer
On-board rewrite	Available	Available	Unavailable

29.2 Memory Map

The flash memory is used as ROM in this product. The flash memory is comprised of program ROM 1, program ROM 2, and data flash. Figure 29.1 shows the Flash Memory Block Diagram.
The flash memory is divided into several blocks, each of which can be protected (locked) from being programmed or erased. The flash memory can be rewritten in CPU rewrite, standard serial I/O, and parallel I/O modes.
Program ROM 2 can be used when the PRG2C0 bit in the PRG2C register is 0 (program ROM 2 enabled).
Data flash can be used when the PM10 bit in the PM1 register is set to 1 (0E000h to 0FFFFh: data flash).
Data flash is divided into block A and block B.
Table 29.3 lists the differences among program ROM 1, program ROM 2, and data flash.
In single-chip mode, program can be allocated in either program ROM 1, program ROM 2, or data flash.

Table 29.3 Program ROM 1, Program ROM 2, and Data Flash

Item	Flash Memory		
	Program ROM 1	Program ROM 2	Data flash
Program and erase cycles	1,000 times		10,000 times
Forced erase function	Enabled		Disabled
Frequency limit when reading	No		Yes
User boot program	Do not allocate	Allocatable	Do not allocate

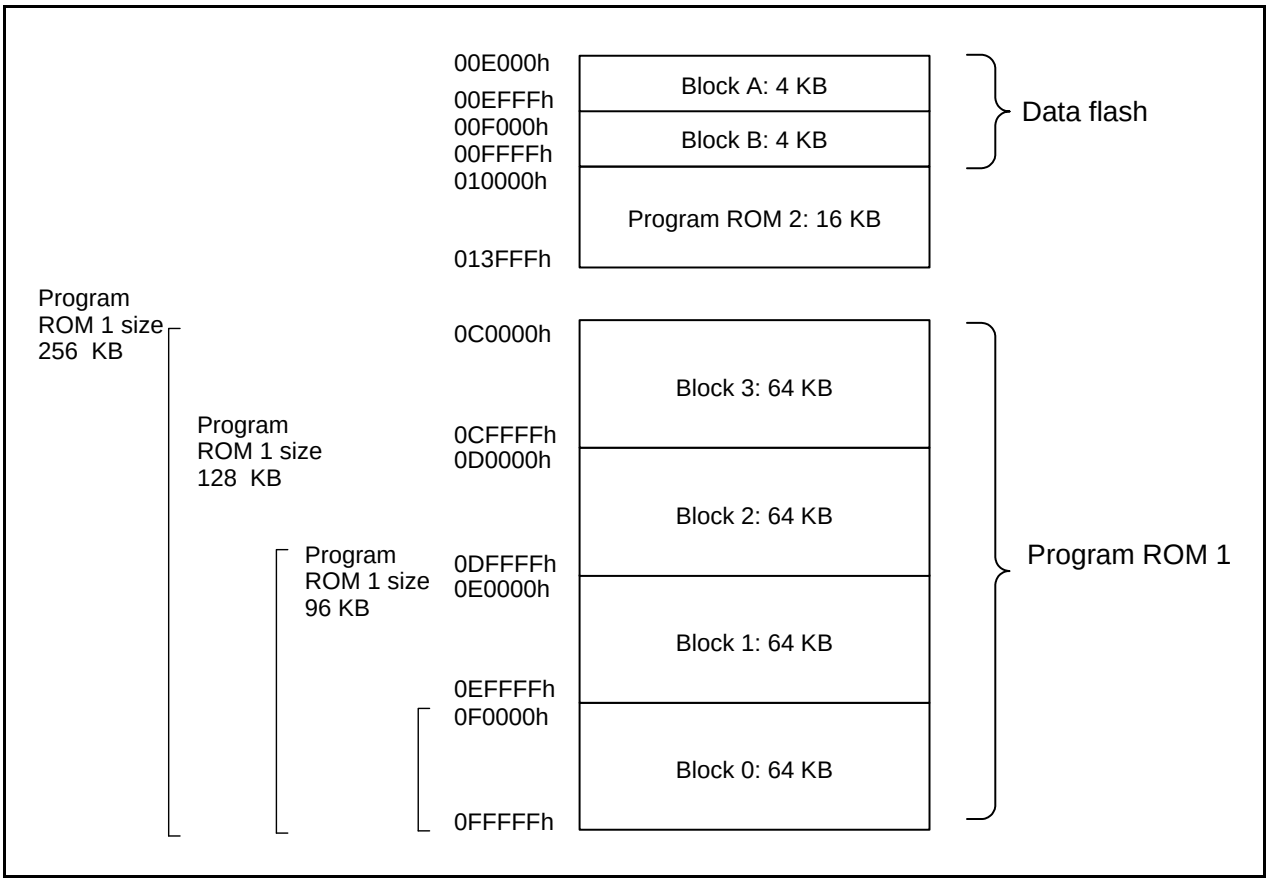


Figure 29.1 Flash Memory Block Diagram

29.3 Registers

Table 29.4 Registers

Address	Register	Symbol	Reset Value
0220h	Flash Memory Control Register 0	FMR0	0000 0001b (Other than user boot mode) 0010 0001b (User boot mode)
0221h	Flash Memory Control Register 1	FMR1	00X0 XX0Xb
0222h	Flash Memory Control Register 2	FMR2	XXXX 0000b
0223h	Flash Memory Control Register 3	FMR3	XXXX 0000b
0230h	Flash Memory Control Register 6	FMR6	XX0X XX00b

29.3.1 Flash Memory Control Register 0 (FMR0)

Flash Memory Control Register 0

b7	b6	b5	b4	b3	b2	b1	b0
			0				

Symbol: FMR0 — Address: 0220h — Reset Value: 0000 0001b (other than user boot mode), 0010 0001b (user boot mode)

Bit Symbol	Bit Name	Function	RW
FMR00	RY/$\overline{BY}$ status flag	0 : Busy (being written or erased) 1 : Ready	RO
FMR01	CPU rewrite mode select bit	0 : CPU rewrite mode disabled 1 : CPU rewrite mode enabled	RW
FMR02	Lock bit disable select bit	0 : Lock bit enabled 1 : Lock bit disabled	RW
FMSTP	Flash memory stop bit	0 : Flash memory operation enabled 1 : Flash memory operation stopped (low power-mode, flash memory initialized)	RW
— (b4)	Reserved bit	Set to 0	RW
— (b5)	Reserved bit	Set to 0 in other than user boot mode Set to 1 in user boot mode	RW
FMR06	Program status flag	0 : Completed as expected 1 : Completed in error	RO
FMR07	Erase status flag	0 : Completed as expected 1 : Completed in error	RO

FMR00 (RY/$\overline{BY}$ status flag) (b0)

This bit indicates the flash memory operating state.

Conditions to become 0:

- When executing the following commands:
  Program, block erase, lock bit program, read lock bit status, and block blank check
- When the flash memory stops (the FMSTP bit is 1)
- During the wake up operation when the FMSTP bit is changed from 1 to 0

Condition to become 1:

- Other than those above.

FMR01 (CPU rewrite mode select bit) (b1)

Commands can be accepted by setting the FMR01 bit to 1 (CPU rewrite mode enabled).
To set the FMR01 bit to 1, write 0 and then 1 in succession. Do not generate any interrupts or DMA transfers between setting 0 and 1.
Change the FMR01 bit when the PM24 bit in the PM2 register is 0 ($\overline{\text{NMI}}$ interrupt disabled) or high is input to the $\overline{\text{NMI}}$ pin.
While in EW0 mode, write to this bit from a program in RAM.
Enter read array mode, and then set this bit to 0.

FMR02 (Lock bit disable select bit) (b2)

The lock bit is disabled by setting the FMR02 bit to 1 (lock bit disabled) (Refer to 29.8.4 “Data Protect Function”).
The FMR02 bit does not change the lock bit data, but disables the lock bit function. If an erase command is executed when the FMR02 bit is set to 1, the lock bit data status changes from 0 (locked) to 1 (unlocked) after command execution is completed.
To set the FMR02 bit to 1, write 0 and then 1 to the FMR02 bit in succession when the FMR01 bit is 1. Make sure no interrupts or DMA transfers will occur before writing 1 after writing 0.
Do not change the FMR02 bit while programming, erasing or suspending.

FMSTP (Flash memory stop bit) (b3)

The FMSTP bit resets the flash memory control circuits and minimizes current consumption in the flash memory. Access to the internal flash memory is disabled when the FMSTP bit is set to 1 (flash memory operation stopped). Set the FMSTP bit by a program located in RAM.
Set the FMSTP bit to 1 under the following condition:

- A flash memory access error occurs while erasing or programming in EW0 mode (the FMR00 bit does not revert to 1 (ready)).

Use the following steps to rewrite the FMSTP bit.
To stop the flash memory:
(1) Set the FMSTP bit to 1.
(2) Wait the wait time to stabilize the flash memory circuit (tps).
To restart the flash memory:
(1) Set the FMSTP bit to 0.
(2) Wait the wait time to stabilize the flash memory circuit (tps).

The FMSTP bit is enabled when the FMR01 bit is 1 (CPU rewrite mode). When the FMR01 bit is 0, although the FMSTP bit can be set to 1 by writing 1, the flash memory is neither placed in low-power mode nor initialized.
When the FMR22 bit is 1 (slow read mode enabled) or the FMR23 bit is 1 (low-current consumption read mode enabled), do not set the FMSTP bit in the FMR0 register to 1 (flash memory operation stopped). Also, when the FMSTP bit is 1, do not set the FMR22 or FMR23 bit to 1.

FMR06 (Program status flag) (b6)

This bit indicates the auto-program operation state.
Condition to become 0:
- Execute the clear status command.

Condition to become 1:
- Refer to 29.8.7.1 “Full Status Check”.

Do not execute the following commands when the FMR06 bit is 1:
Program, block erase, lock bit program, and block blank check.

FMR07 (Erase status flag) (b7)

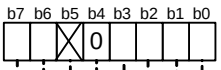
This bit indicates the auto-erase operation state.
Condition to become 0:
- Execute the clear status command

Condition to become 1:
- Refer to 29.8.7.1 “Full Status Check”.

Do not execute the following commands when the FMR07 bit is 1:
Program, block erase, lock bit program, and block blank check.

29.3.2 Flash Memory Control Register 1 (FMR1)

Flash Memory Control Register 1



Symbol	Address	Reset Value
FMR1	0221h	00X0 XX0Xb

Bit Symbol	Bit Name	Function	RW
— (b0)	Reserved bit	The read value is undefined.	RO
FMR11	Write to FMR6 register enable bit	0 : Disabled 1 : Enabled	RW
— (b3-b2)	Reserved bits	The read value is undefined.	RO
— (b4)	Reserved bit	Set to 0	RW
— (b5)	No register bit. If necessary, set to 0. The read value is undefined.		—
FMR16	Lock bit status flag	0 : Lock 1 : Unlock	RO
FMR17	Data flash wait bit	0 : 1 wait 1 : Follow the setting of the PM17 bit in the PM1 register	RW

FMR11 (Write to FMR6 register enable bit) (b1)

Change FMR11 bit when the PM24 bit in the PM2 register is 0 ($\overline{\text{NMI}}$ interrupt disabled) or high is input to the $\overline{\text{NMI}}$ pin.

FMR16 (Lock bit status flag) (b6)

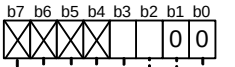
This bit indicates the execution result of the read lock bit status command.

FMR17 (Data flash wait bit) (b7)

This bit is used to select the number of waits for data flash.
When setting this bit to 0, one wait is inserted to the read cycle of the data flash. The write cycle is not affected.

29.3.3 Flash Memory Control Register 2 (FMR2)

Flash Memory Control Register 2



Symbol: FMR2 | Address: 0222h | Reset Value: XXXX 0000b

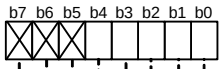
Bit Symbol	Bit Name	Function	RW
— (b1-b0)	Reserved bits	Set to 0	RW
FMR22	Slow read mode enable bit	0 : Disabled 1 : Enabled	RW
FMR23	Low current consumption read mode enable bit	0 : Disabled 1 : Enabled	RW
— (b7-b4)	No register bits. If necessary, set to 0. The read value is undefined.		—

FMR22 (Slow read mode enable bit) (b2)
FMR23 (Low-current consumption read mode enable bit) (b3)

Refer to 9.4 “Power Control in Flash Memory”.

29.3.4 Flash Memory Control Register 3 (FMR3)

Flash Memory Control Register 3



Symbol	Address	Reset Value
FMR3	0223h	XXXX 0000b

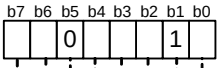
Bit Symbol	Bit Name	Function	RW
FMR30	Suspend function enable bit	0 : Disabled 1 : Enabled	RW
FMR31	Suspend request bit	0 : Command restart 1 : Suspend request	RW
FMR32	Erase suspend status flag	0 : Erase suspend not accepted 1 : Erase suspend accepted	RO
FMR33	Program suspend status flag	0 : Program suspend not accepted 1 : Program suspend accepted	RO
— (b4)	Reserved bit	The read value is undefined.	RO
— (b7-b5)	No register bits. If necessary, set to 0. The read value is undefined.		—

FMR30 (Suspend function enable bit) (b0)

To set the FMR30 bit to 1, write 0 and then 1 in succession. Make sure no interrupts or DMA transfers will occur before writing 1 after writing 0.

29.3.5 Flash Memory Control Register 6 (FMR6)

Flash Memory Control Register 6



Symbol	Address	Reset Value
FMR6	0230h	XX0X XX00b

Bit Symbol	Bit Name	Function	RW
FMR60	EW1 mode select bit	0 : EW0 mode 1 : EW1 mode	RW
FMR61	Reserved bit	Set to 1	RW
— (b4-b2)	Reserved bits	The read value is undefined.	RO
— (b5)	Reserved bit	Set to 0	RW
— (b7-b6)	Reserved bits	The read value is undefined.	RO

When accessing the FMR6 register, select a CPU clock frequency of 16 MHz or less by setting the CM06 bit in the CM0 register and bits CM17 and CM16 in the CM1 register. Also, set the PM17 bit in the PM1 register to 1 (wait state).

FMR60 (EW1 mode select bit) (b0)

To set the FMR60 bit to 1, write 1 when both FMR01 bit in the FMR0 register and FMR11 bit in the FMR1 register are 1.
Change the FMR60 bit when the PM24 bit in the PM2 register is 0 ($\overline{\text{NMI}}$ interrupt disabled) or high is input to the $\overline{\text{NMI}}$ pin. Also, change this bit when the FMR00 bit in the FMR0 register is 1 (ready).

FMR61 (b1)

Set the FMR61 bit to 1 when using CPU rewrite mode.

29.4 Optional Function Select Area

In an option function select area, the MCU state after reset and the function to prevent rewrite in parallel I/O mode are selected.

The option function select area is not an SFR, and therefore cannot be rewritten by a program. Set an appropriate value when writing a program to the flash memory. The entire option function select area becomes FFh when the block including the option function select area is erased.

In blank products, the OFS1 and OFS2 address values are FFh when shipped. After a value is written by the user, this address takes on the written value. In programmed products, the OFS1 and OFS2 addresses are the value set in the user program prior to shipping.

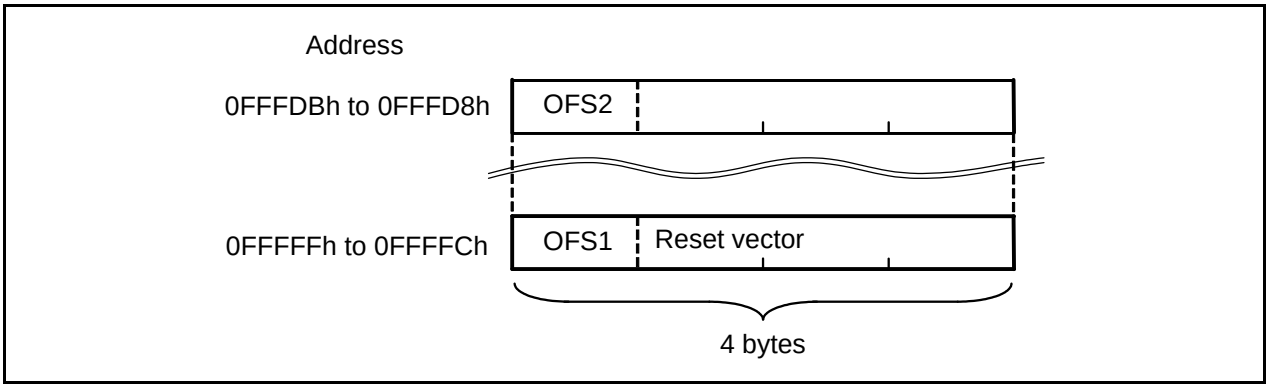
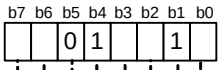


Figure 29.2 Option Function Select Area

29.4.1 Optional Function Select Address 1 (OFS1)

Optional Function Select Address 1



Symbol: OFS1

Address: FFFFFh

Bit Symbol	Bit Name	Function
WDTON	Watchdog timer start select bit	0 : Watchdog timer starts automatically after reset. 1 : Watchdog timer is in a stopped state after reset.
— (b1)	Reserved bit	Set to 1.
ROMCR	ROM code protect cancel bit	0 : ROM code protection cancelled. 1 : ROMCP1 bit enabled.
ROMCP1	ROM code protect bit	0 : ROM code protection enabled. 1 : ROM code protection cancelled.
— (b4)	Reserved bit	Set to 1.
— (b5)	Reserved bit	Set to 0.
LVDAS	Voltage detector 0 start bit	0 : Voltage monitor 0 reset enabled after hardware reset. 1 : Voltage monitor 0 reset disabled after hardware reset.
CSPROINI	After-reset count source protection mode select bit	0 : Count source protection mode enabled after reset. 1 : Count source protection mode disabled after reset.

ROMCR (ROM code protect disable bit) (b2)
ROMCP1 (ROM code protect bit) (b3)

These bits are used to disable the flash memory from being read or rewritten in parallel I/O mode.

Table 29.5 ROM Code Protect

Bit Setting		ROM Code Protect
ROMCR bit	ROMCP1 bit	
0	0	Disabled
0	1	
1	0	Enabled
1	1	Disabled

29.4.2 Optional Function Select Address 2 (OFS2)

Optional Function Select Address 2

b7	b6	b5	b4	b3	b2	b1	b0
1	1	1	1				

Symbol: OFS2

Address: FFFDBh

Bit Symbol	Bit Name	Function
WDTUFS0	Watchdog timer initial setting bit	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh
WDTUFS1		
WDTRCS0	Watchdog timer refresh duty cycle setting bit	Refresh period is the last n% of watchdog timer period: b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%
WDTRCS1		
— (b7-b4)	Reserved bits	Set to 1.

29.5 Flash Memory Rewrite Disable Function

This function disables the flash memory from being read, written, and erased. The following are details for each mode:

Parallel I/O mode

ROM code protect function

Standard serial I/O mode

ID code check function, forced erase function, and standard serial I/O mode disable function

29.6 Boot Mode

A hardware reset occurs while a high-level signal is applied to pins CNVSS. After reset, the MCU enters boot mode. In boot mode, user boot mode or standard serial I/O mode is selected in accordance with the content of the user boot code area. Refer to 29.9 “Standard Serial I/O Mode” for details.

The MCU does not enter boot mode in power-on reset and voltage monitor 0 reset.

29.7 User Boot Mode

This mode is used for starting the flash memory rewrite program programmed by a user.

Allocate the flash memory rewrite program to program ROM 2. In user boot mode, the program is executed from address 10000h (starting address of program ROM 2). After starting the program, the flash memory is rewritten according to the program in EW0 or EW1 mode.

29.7.1 User Boot Function

User boot mode can be selected by the status of a port when the MCU starts in boot mode. Table 29.6 lists the User Boot Function Specifications.

Table 29.6 User Boot Function Specifications

Item	Specification
Entry pin	None or select a port from P0 to P10
User boot start level	Select high or low
User boot start address	Address 10000h (program ROM 2 start address)

Set “UserBoot” in ASCII code to addresses 13FF0h to 13FF7h in the user boot code area, select a port for entry from addresses 13FF8h to 13FF9h and 13FFAh, and select the start level with address 13FFBh. After starting boot mode, user boot mode or standard serial I/O mode is selected in accordance with the input level of the selected port.

In addition, if addresses 13FF0h to 13FF7h are set to “UserBoot” in ASCII code and addresses 13FF8h to 13FFBh are set to 00h, user boot mode is selected.

In user boot mode, the program of address 10000h (program ROM 2 start address) is executed.

Figure 29.3 shows the User Boot Code Area, Table 29.7 lists Start Mode (When Port Pi_j is Selected for Entry), Table 29.8 lists “UserBoot” in ASCII Code, and Table 29.9 lists Addresses of Selectable Ports for Entry.

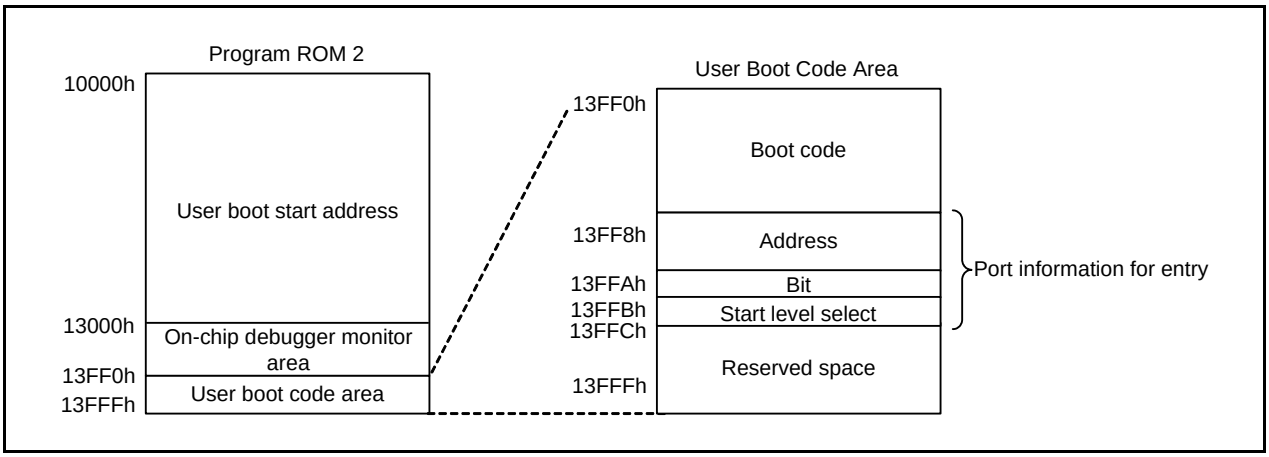


Figure 29.3 User Boot Code Area

Table 29.7 Start Mode (When Port Pi_j is Selected for Entry) (1)

Boot Code (13FF0h to 13FF7h)	Port Information for Entry			Port Pi_j Input Level	Start Mode
	Address (13FF8h to 13FF9h)	Bit (13FFAh)	Start level select (13FFBh)		
"UserBoot" in ASCII code (2)	0000h	00h	00h	–	User boot mode
	Pi register address (3)	00h to 07h (value of j)	00h	High	Standard serial I/O mode
				Low	User boot mode
	Pi register address (3)	00h to 07h (value of j)	01h	High	User boot mode
				Low	Standard serial I/O mode
Other than "UserBoot" in ASCII code	–	–	–	–	Standard serial I/O mode

i = 0 to 10; j = 0 to 7

Notes:
1. Only use the values listed in Table 29.7.
2. See Table 29.8 "UserBoot" in ASCII Code.
3. See Table 29.9 "Addresses of Selectable Ports for Entry".

Table 29.8 "UserBoot" in ASCII Code

Address	ASCII Code
13FF0h	55h (upper-case U)
13FF1h	73h (lower-case s)
13FF2h	65h (lower-case e)
13FF3h	72h (lower-case r)
13FF4h	42h (upper-case B)
13FF5h	6Fh (lower-case o)
13FF6h	6Fh (lower-case o)
13FF7h	74h (lower-case t)

Table 29.9 Addresses of Selectable Ports for Entry

Port	Address	
	13FF9h	13FF8h
P0	03h	E0h
P1	03h	E1h
P2	03h	E4h
P3	03h	E5h
P4	03h	E8h
P5	03h	E9h
P6	03h	ECh
P7	03h	EDh
P8	03h	F0h
P9	03h	F1h
P10	03h	F4h

Table 29.10 Example Settings of User Boot Code Area

When starting up in user boot mode while input level of the port P1_5 is low:

Address	Setting Value	Meaning
13FF0h	55h	Upper-case U
13FF1h	73h	Lower-case s
13FF2h	65h	Lower-case e
13FF3h	72h	Lower-case r
13FF4h	42h	Upper-case B
13FF5h	6Fh	Lower-case o
13FF6h	6Fh	Lower-case o
13FF7h	74h	Lower-case t
13FF8h	E1h	Port P1_5
13FF9h	03h	
13FFAh	05h	
13FFBh	00h	Low level

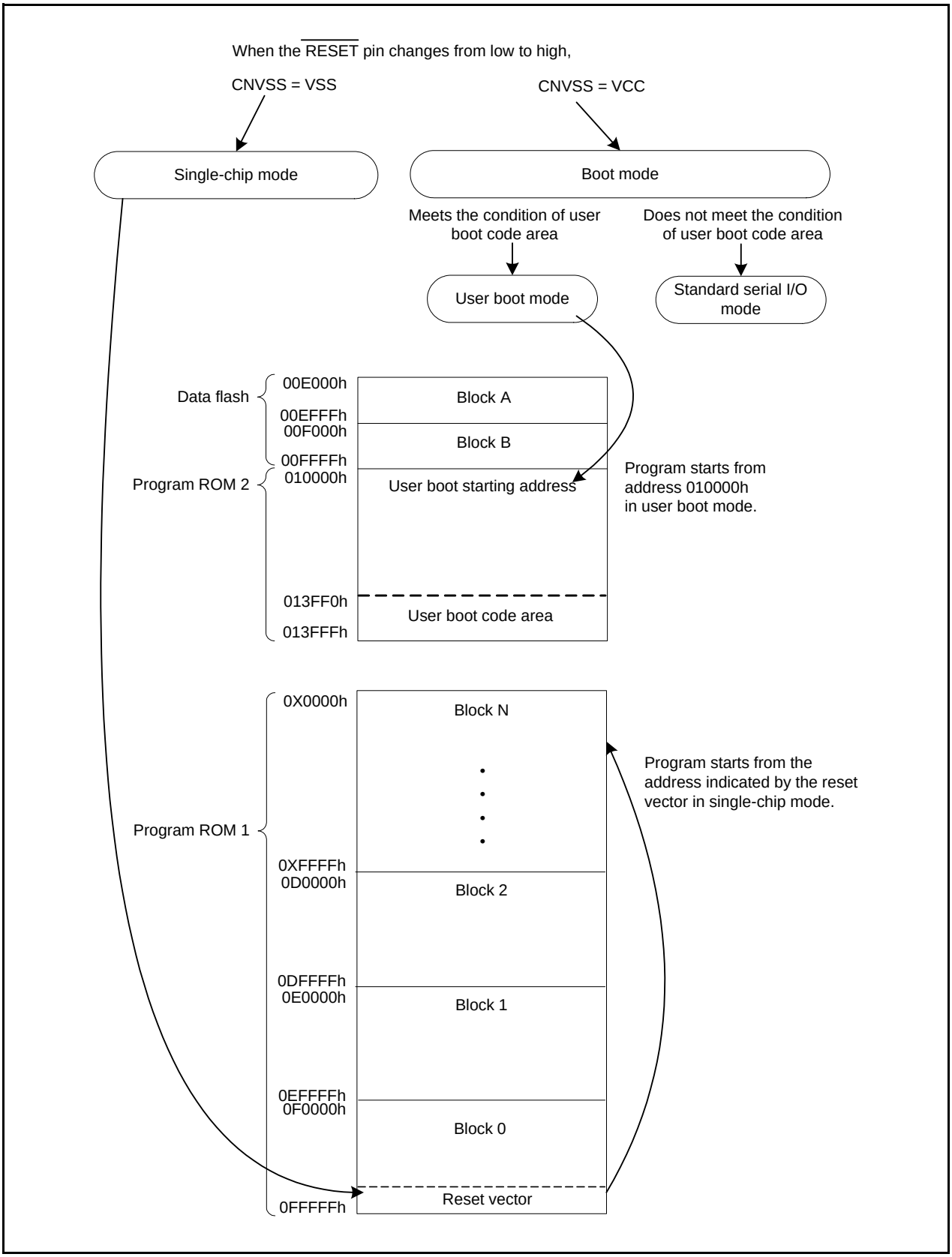


Figure 29.4 Program Starting Address in User Boot Mode

29.8 CPU Rewrite Mode

In CPU rewrite mode, the flash memory can be rewritten when the CPU executes software commands. Program ROM 1, program ROM 2, and data flash can be rewritten with the MCU mounted on the board and without using a ROM programmer.

The program and block erase commands are executed only in individual block areas of program ROM 1, program ROM 2, and data flash.

The flash memory has a suspend function to temporarily suspend operation when erasing or programming in CPU rewrite mode. Refer to 29.8.5 “Suspend Function” for details of the suspend function.

EW0 mode and EW1 mode are available in CPU rewrite mode. Table 29.11 lists the differences between EW0 mode and EW1 mode.

Refer to 29.8.1 “EW0 Mode” and 29.8.2 “EW1 Mode” for details.

Table 29.11 EW0 Mode and EW1 Mode

Item	EW0 Mode	EW1 Mode
Operating mode	• Single-chip mode	Single-chip mode
Rewrite control program allocatable area	• Program ROM 1 • Program ROM 2	• Program ROM 1 • Program ROM 2
Rewrite control program executable area	The rewrite control program must be transferred to RAM before being executed.	The rewrite control program can be executed in program ROM 1 and program ROM 2.
Rewritable area	• Program ROM 1 • Program ROM 2 • Data flash	• Program ROM 1 • Program ROM 2 • Data flash Excluding blocks with the rewrite control program
Software command restriction	None	• Do not execute program and block erase commands in a block with the rewrite control program. • Read status register command Do not execute.
Mode after program/erase, or during program/erase suspend	Read status register mode	Read array mode
State during auto write and auto erase	Bus is not in a hold state.	Bus is in a hold state. (1)
Flash memory status detection	• Read bits FMR00, FMR06, and FMR07 in the FMR0 register, and bits FMR32 and FMR33 in the FMR3 register by a program. • Execute the read status register command, and then read bits SR7, SR5 and SR4 in the status register.	Read bits FMR00, FMR06, and FMR07 in the FMR0 register, and bits FMR32 and FMR33 in the FMR3 register by a program.

Note:

1. Refer to 10.4 “Bus Hold” for detail about the bus hold.

29.8.1 EW0 Mode

The MCU enters CPU rewrite mode when the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled) and is ready to accept commands. EW0 mode is selected by setting the FMR60 bit in the FMR6 register to 0. Figure 29.5 shows Setting and Resetting of EW0 Mode

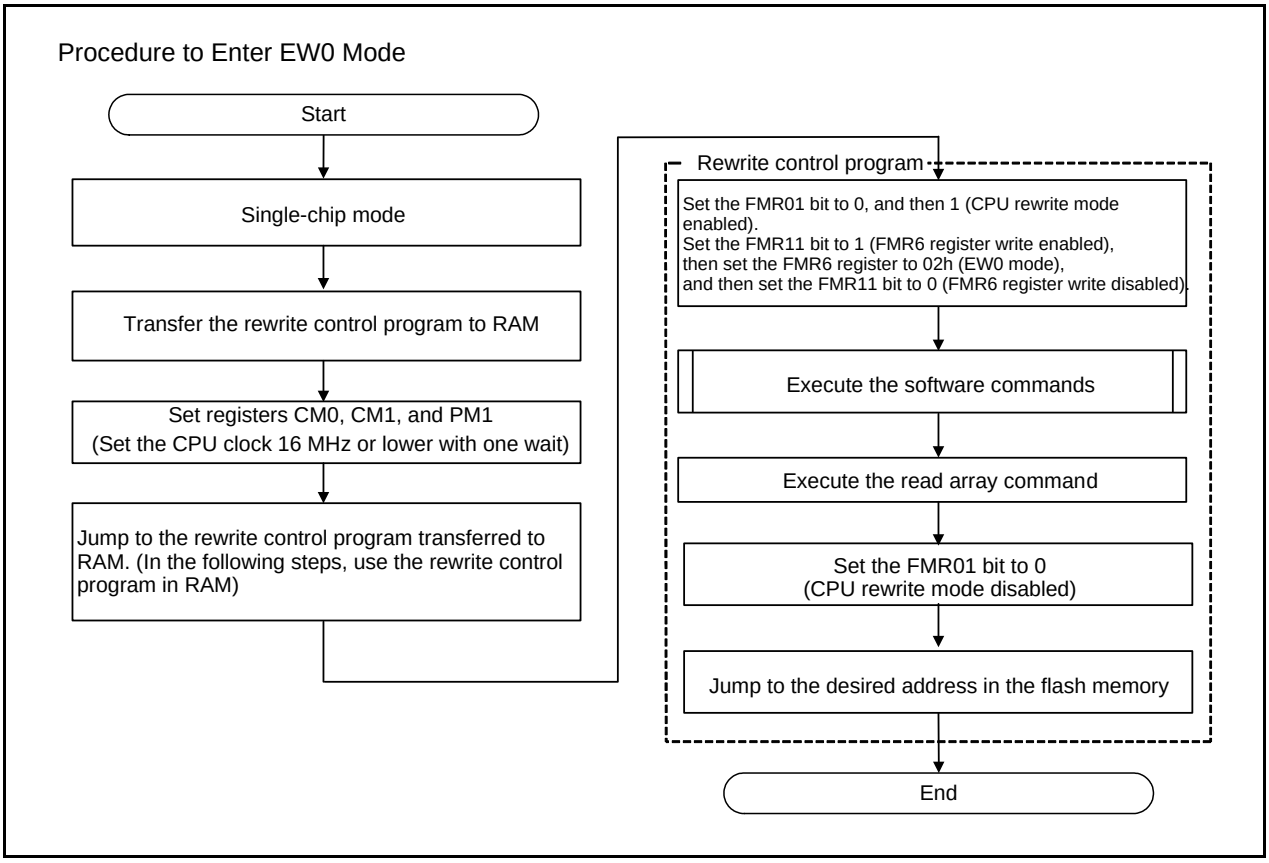


Figure 29.5 Setting and Resetting of EW0 Mode

Do not execute the following instructions in EW0 mode:
UND instruction, INTO instruction, JMPS instruction, JSRS instruction, and BRK instruction.

The following are interrupts which can be used in EW0 mode and operations when the interrupts occur during auto-erase operation or auto-program operation:

- Maskable interrupt (suspend disabled)
  To use the interrupt, allocate a variable vector table on RAM.
- Maskable interrupt (suspend enabled)
  To use the interrupt, allocate a variable vector table on RAM.
  When the FMR00 bit in the FMR0 register is checked in the interrupt routine and the result is 0 (being written or erased), auto-erase operation or auto-program operation suspends after td(SR-SUS) elapses by setting the FMR31 bit in the FMR3 register to 1 (suspend request). Auto-erase operation or auto-program operation restarts by setting the FMR31 bit to 0 (command restart) at the completion of the interrupt.
- $\overline{\text{NMI}}$, watchdog timer, oscillator stop/restart detect, and voltage detect 2 interrupts
  Auto-erase operation or auto-program operation is forcibly stopped as soon as the interrupt occurs, and then the interrupt process starts.
  After the flash memory restart, execute auto-erase operation again and confirm that it is completed as expected in order to read the correct value.

The watchdog timer operates even in auto erasing or auto programming operation. Refresh the watchdog timer regularly.

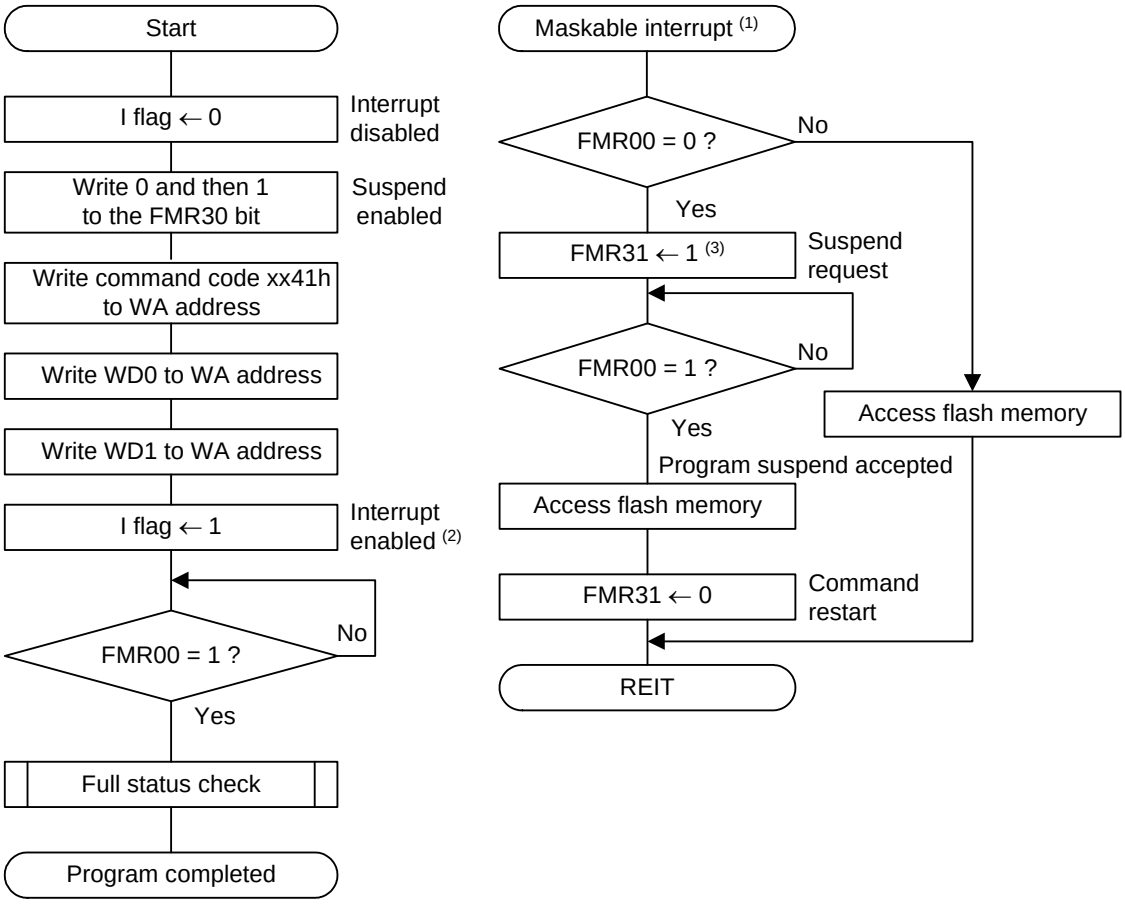
Table 29.12 Modes after Executing Commands (in EW0 Mode)

Command	Mode after Executing Command
Read array	Read array mode
Clear status register	Read array mode
Program	Read status register mode (1)
Block erase	
Lock bit program	
Read lock bit status	Read lock bit status mode (1)
Block blank check	Read status register mode (1)

Note:
1. Flash memory can be read only in read array mode.

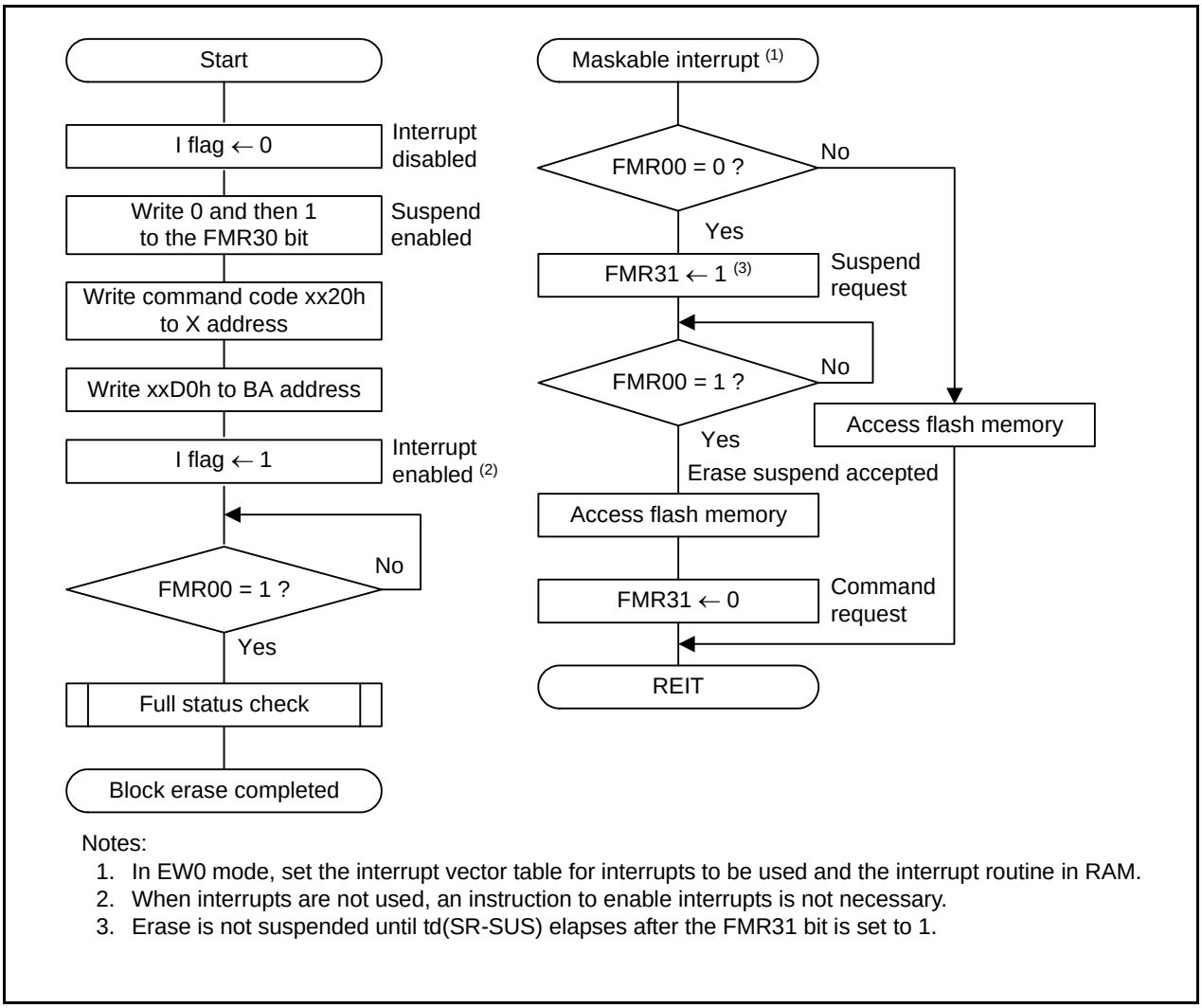
29.8.1.1 Suspend Function (EW0 Mode)

When using suspend function in EW0 mode, check the status of the flash memory in the interrupt routine and enter suspend mode. Program suspend or erase suspend is not accepted until td(SR-SUS) elapses after the FMR31 bit is set to 1. Access to the flash memory after confirming the acceptance of program suspend or erase suspend by the FMR33 or FMR32 bit. Set the FMR31 bit to 0 (command restart) to restart auto-program and auto-erase operations at the completion of the access to the flash memory. Figure 29.6 to Figure 29.8 show a flowchart in EW0 mode when the suspend function is enabled, and Figure 29.9 shows Suspend Operation Example in EW0 Mode.



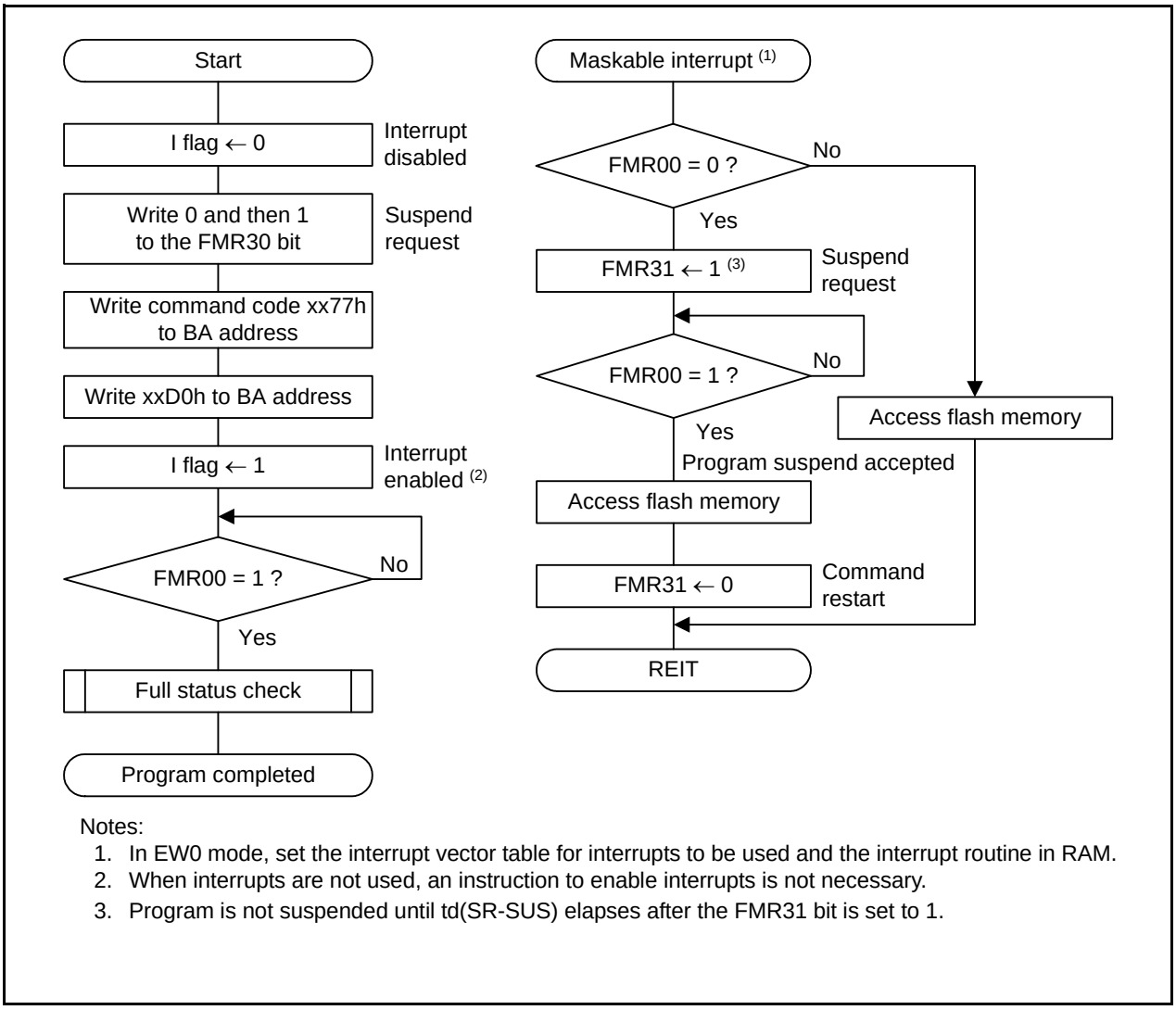
Notes:
1. In EW0 mode, set the interrupt vector table for interrupts to be used and the interrupt routine in RAM.
2. When interrupts are not used, an instruction to enable interrupts is not necessary.
3. Program is not suspended until td(SR-SUS) elapses after the FMR31 bit is set to 1.

Figure 29.6 Program Flowchart in EW0 Mode (Suspend Function Enabled)



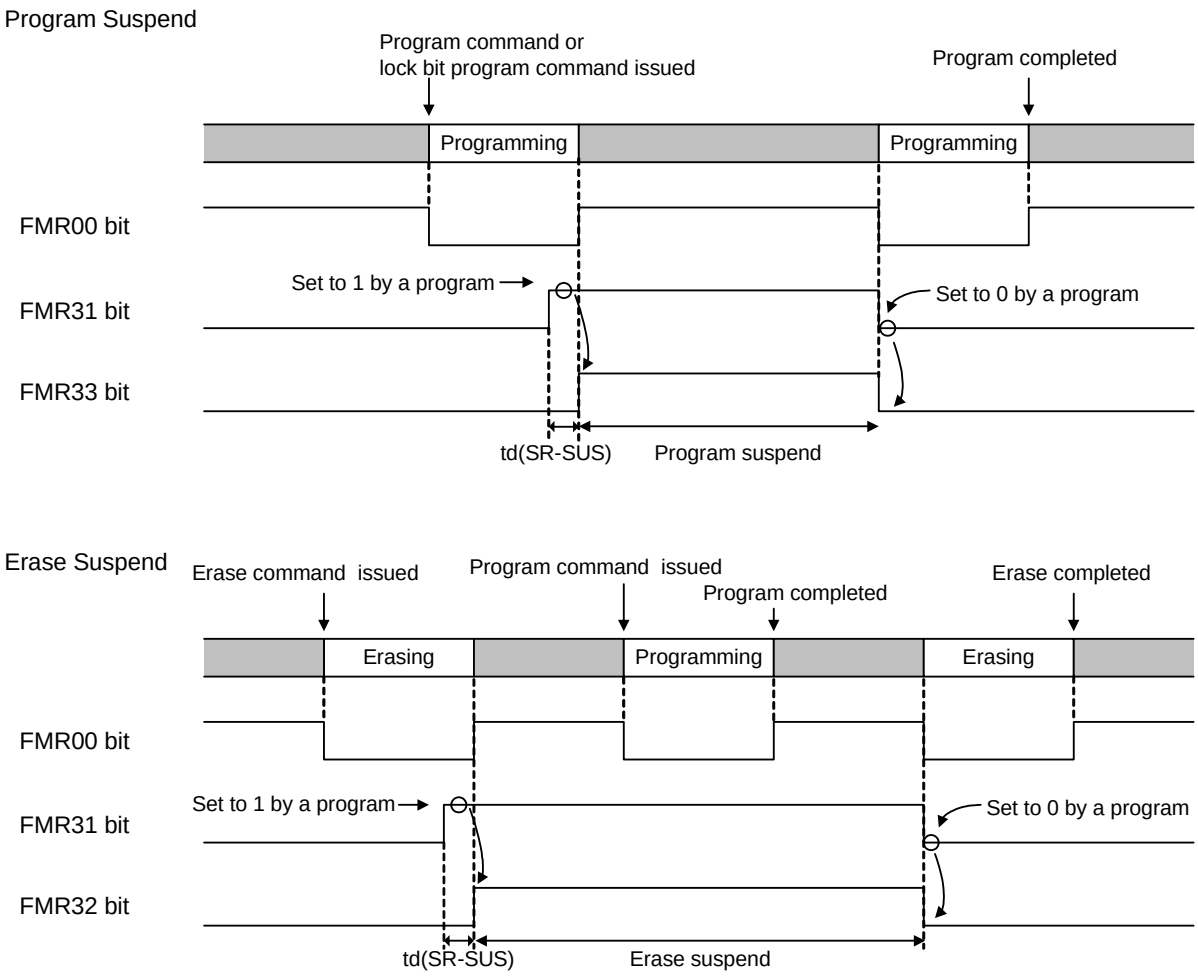
Notes:
1. In EW0 mode, set the interrupt vector table for interrupts to be used and the interrupt routine in RAM.
2. When interrupts are not used, an instruction to enable interrupts is not necessary.
3. Erase is not suspended until td(SR-SUS) elapses after the FMR31 bit is set to 1.

Figure 29.7 Block Erase Flowchart in EW0 Mode (Suspend Function Enabled)



Notes:
1. In EW0 mode, set the interrupt vector table for interrupts to be used and the interrupt routine in RAM.
2. When interrupts are not used, an instruction to enable interrupts is not necessary.
3. Program is not suspended until td(SR-SUS) elapses after the FMR31 bit is set to 1.

Figure 29.8 Lock Bit Program Flowchart in EW0 Mode (Suspend Function Enabled)



FMR00: Bit in the FMR0 register
FMR33, FMR32, FMR31: Bits in the FMR3 register

The above assumes the following:

- The FMR30 bit in the FMR3 register is 1 (suspend enabled).

Figure 29.9 Suspend Operation Example in EW0 Mode

29.8.2 EW1 Mode

EW1 mode is selected by setting the FMR60 bit in the FMR6 register to 1 after setting the FMR01 bit in the FMR0 register to 1. Figure 29.10 shows Setting and Resetting of EW1 Mode.
When a program or erase operation is initiated, the CPU halts all program execution until the operation is completed.

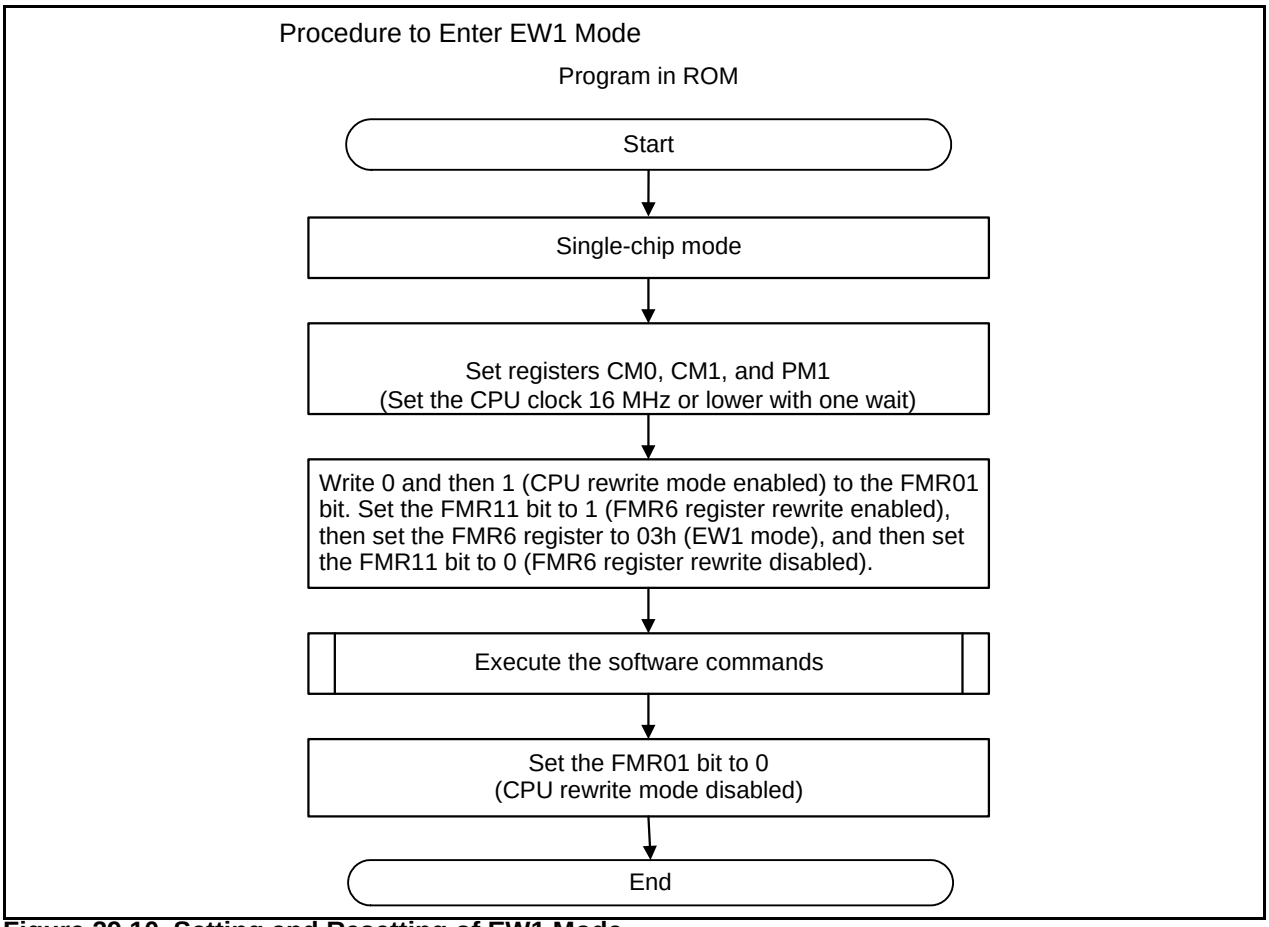


Figure 29.10 Setting and Resetting of EW1 Mode

The following are interrupts which can be used in EW1 mode and operations when the interrupts occur during auto-erase operation or auto-program operation:

- Maskable interrupt (suspend function enabled)
  Auto-erase operation or auto-program operation suspends after td(SR-SUS) elapses and the interrupt process is executed. Auto-erase operation or auto-program operation restarts by setting the FMR31 bit in the FMR3 register to 0 (command restart) after the interrupt process is completed.
- Maskable interrupt (suspend function disabled)
  Auto-erase operation or auto-program operation has a higher priority level and the interrupt request has to wait. The interrupt process is executed after auto-erase operation or auto-program operation is completed.
- $\overline{\text{NMI}}$, watchdog timer, oscillator stop/restart detect, and voltage detect 2 interrupts
  Auto-erase operation or auto-program operation forcibly stops as soon as the interrupt occurs, and then the interrupt process starts.
  After the flash memory restart, execute auto-erase operation again and confirm that it is completed as expected in order to read the correct value.

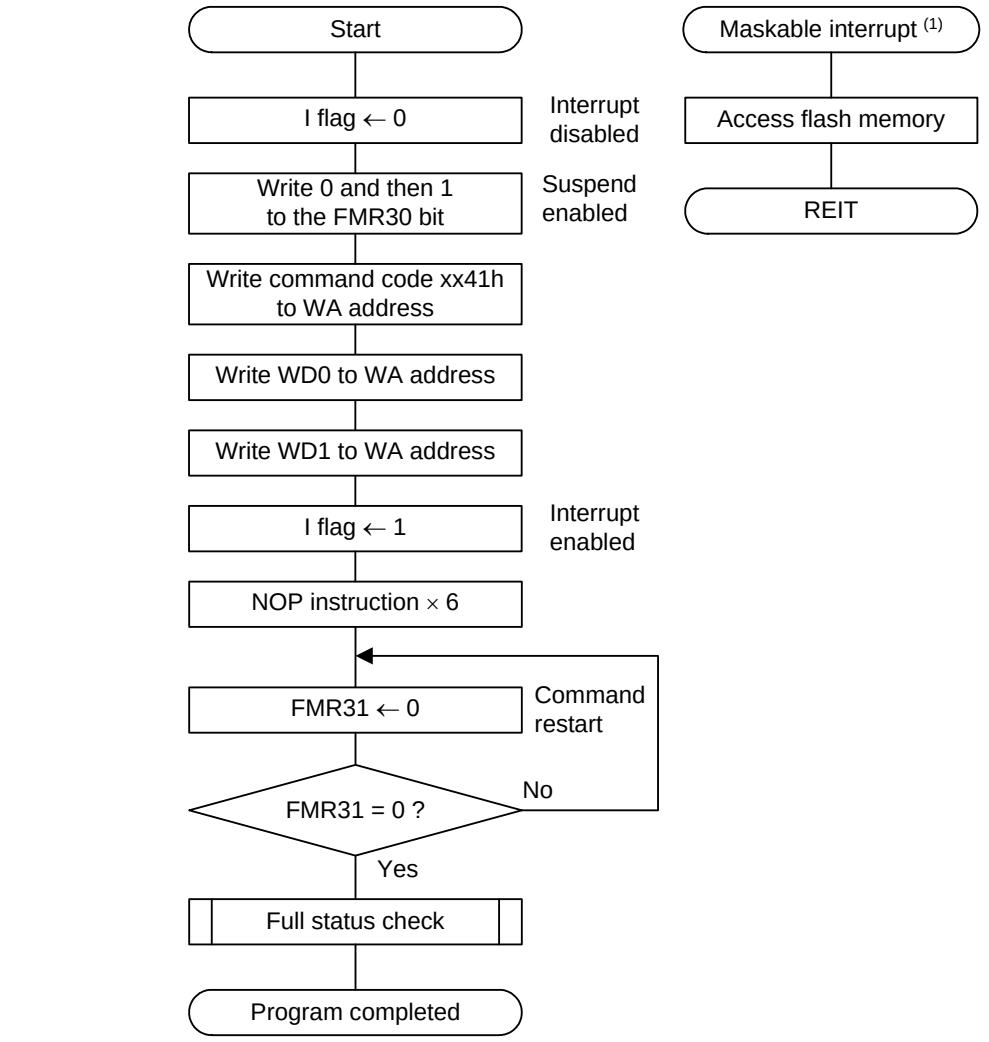
The watchdog timer stops its counting during auto-erase or auto-programming. Do not use EW1 mode while the CSPRO bit in the CSPR register is 1 (count source protection mode enabled). Use EW0 mode. However, counts does not stop during erase suspend or program suspend. As the interrupt request may be generated, initialize the watchdog timer regularly using the suspend function.

Table 29.13 Modes after Executing Commands (in EW1 Mode)

Command	Mode after Executing Command
Read array	Read array mode
Clear status register	
Program	
Block erase	
Lock bit program	
Read lock bit status	
Block blank check	

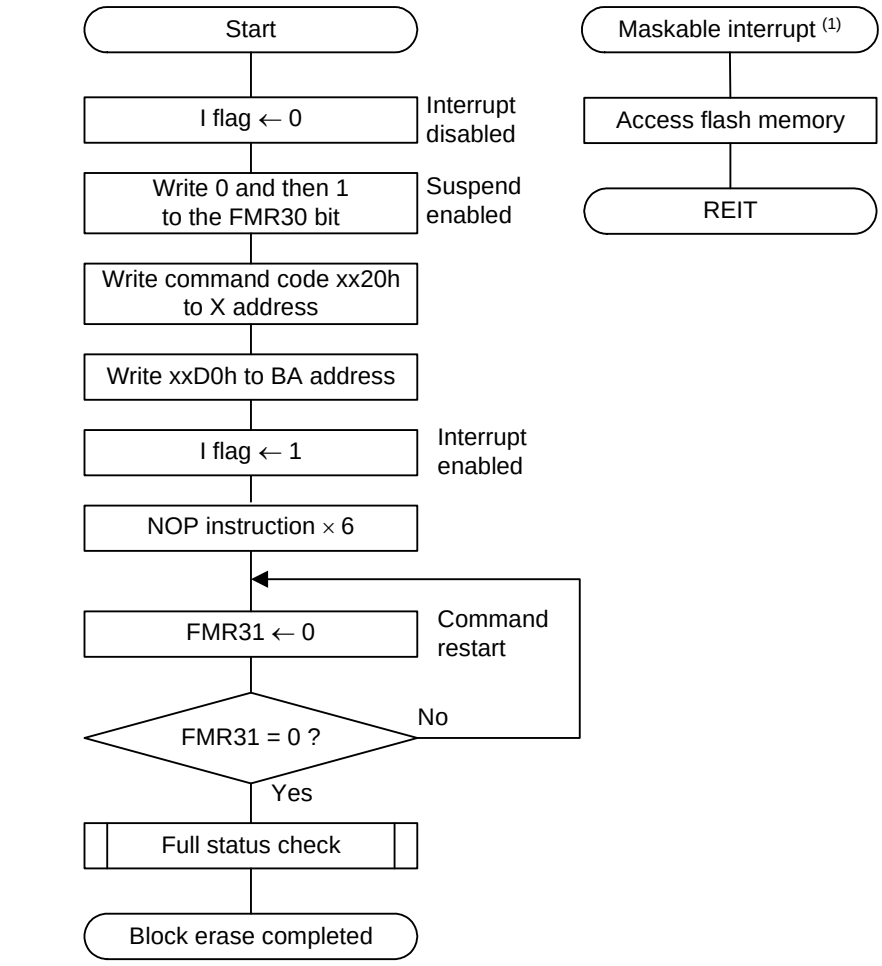
29.8.2.1 Suspend Function (EW1 Mode)

When using suspend function in EW1 mode, an interrupt request is not accepted until td(SR-SUS) elapses after the interrupt request is generated. When the interrupt request is accepted, the flash memory enters erase suspend or program suspend. Set the FMR31 bit to 0 (command restart) to restart automatic program and erase operations at the completion of the interrupt. Figure 29.11 to Figure 29.13 show a flowchart in EW1 mode when the suspend function is enabled, and Figure 29.14 shows Suspend Operation Example in EW1 Mode.



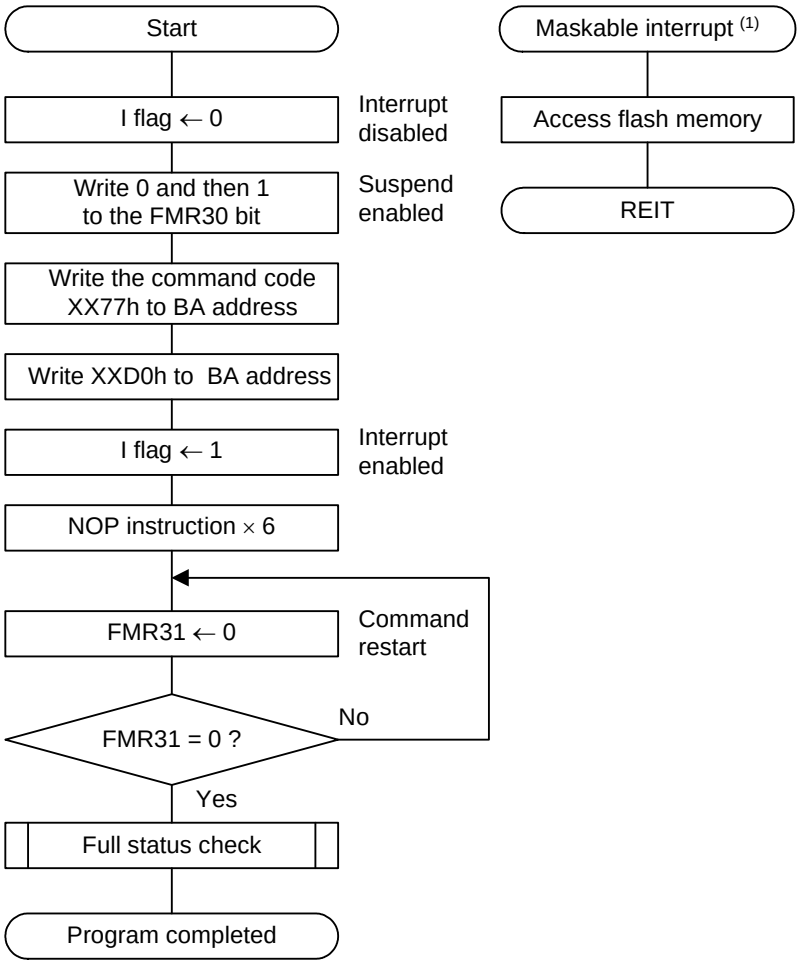
Note:
1. An interrupt request is not accepted until td(SR-SUS) elapses after the interrupt request is generated. Enable interrupts used to enter suspend mode beforehand.

Figure 29.11 Program Flowchart in EW1 Mode (Suspend Function Enabled)



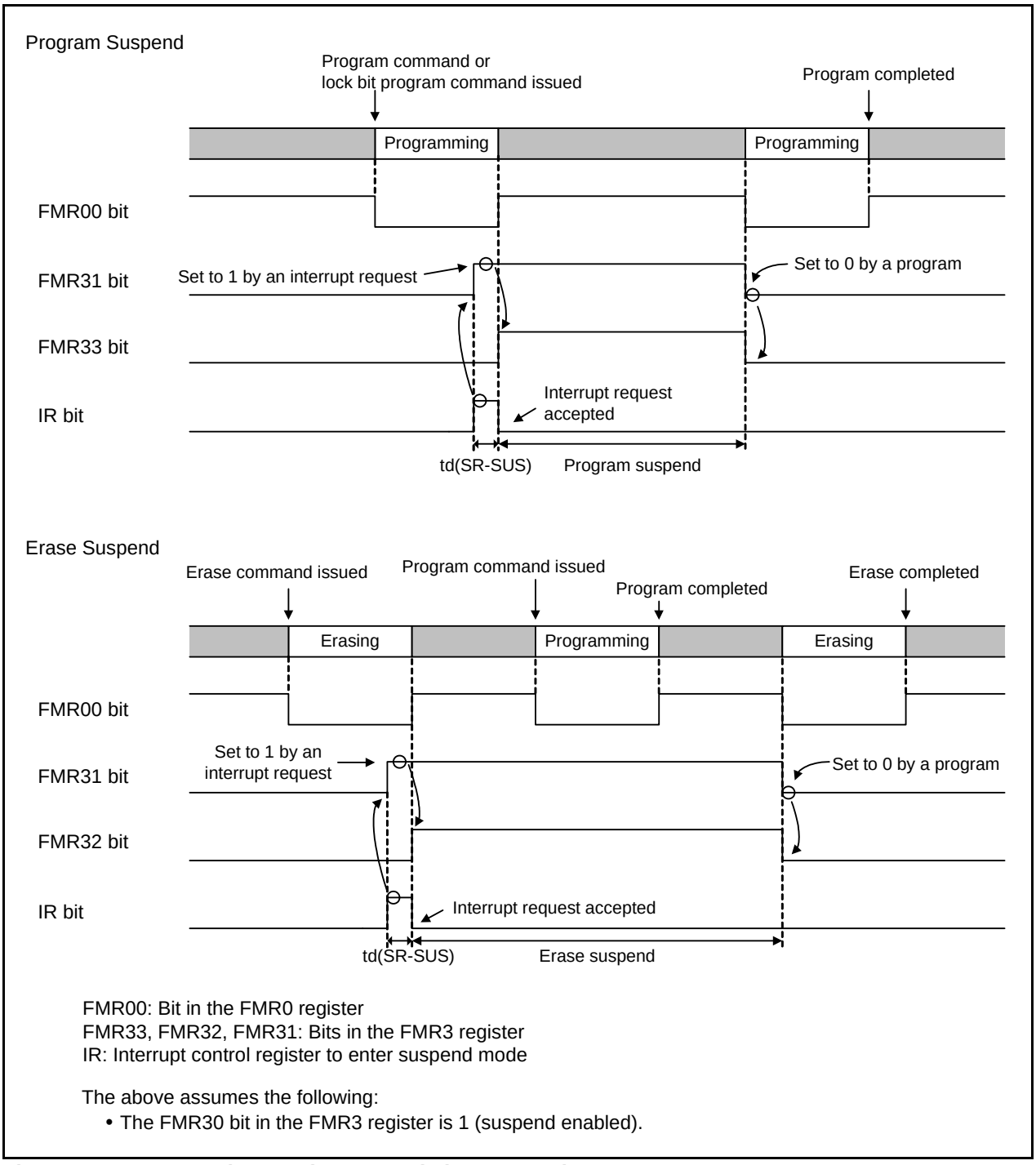
Note:
1. An interrupt request is not accepted until td(SR-SUS) elapses after the interrupt request is generated. Enable interrupts used to enter suspend mode beforehand.

Figure 29.12 Block Erase Flowchart in EW1 Mode (Suspend Function Enabled)



Note:
1. An interrupt request is not accepted until td(SR-SUS) elapses after the interrupt request is generated. Enable interrupts used to enter suspend mode beforehand.

Figure 29.13 Lock Bit Program Flowchart in EW1 Mode (Suspend Function Enabled)



FMR00: Bit in the FMR0 register
FMR33, FMR32, FMR31: Bits in the FMR3 register
IR: Interrupt control register to enter suspend mode

The above assumes the following:

- The FMR30 bit in the FMR3 register is 1 (suspend enabled).

Figure 29.14 Suspend Operation Example in EW1 Mode

29.8.3 Operating Speed

Select a CPU clock frequency of 16 MHz or less by setting the CM06 bit in the CM0 register and bits CM17 and CM16 in the CM1 register before entering CPU rewrite mode (EW0 or EW1 mode). Also, set the PM17 bit in the PM1 register to 1 (wait state).

29.8.4 Data Protect Function

Each block in the flash memory has a nonvolatile lock bit. The lock bit is enabled by setting the FMR02 bit to 0 (lock bit enabled). The lock bit allows blocks to be individually protected (locked) against being programmed and erased. This prevents data from being inadvertently written to or erased from the flash memory. Table 29.14 lists Lock Bit and Block State.

Table 29.14 Lock Bit and Block State

FMR02 Bit in the FMR0 Register	Lock Bit	Block State
0 (enabled)	0 (locked)	Protected against being programmed and erased
	1 (unlocked)	Can be programmed or erased
1 (disabled)	0 (locked)	Can be programmed or erased
	1 (unlocked)	

Condition to become 0:
- Execute the lock bit program command

Condition to become 1:
- Execute the block erase command while the FMR02 bit in the FMR0 register is set to 1 (lock bit disabled).

If the block erase command is executed while the FMR02 bit is set to 1, the target block is erased regardless of lock bit status. The lock bit data can be read by the read lock bit status command.
Refer to 29.8.6 “Software Commands”, for details on each command.

29.8.5 Suspend Function

The suspend function suspends automatic programming and erasure. It can be used for an interrupt operation because program ROM 1, program ROM 2, and data flash can be read while automatic programming or erasure is suspended. Enable the interrupts used to enter suspend mode beforehand.
The program command, erase command, and lock bit program command are subjects for suspend. Suspend operation is the same for the program command and lock bit program command, so both commands are described together as program suspend.
Do not suspend again in suspend mode. Table 29.15 lists Operation after Command is Issued during Suspend.

Table 29.15 Operation after Command is Issued during Suspend

Suspend	Command	Operation	
		Blocks erased or programmed before suspend	Other blocks
Erase suspend (Suspend while executing erase command)	Block erase	The command is not executed. A command sequence error occurs.	
	Program	The command is not executed. A command sequence error occurs.	The command can be executed. Program suspend does not start or an error does not occur even when setting the FMR31 bit to 1 (suspend request).
	Lock bit program	The command is not executed. A command sequence error occurs.	The command can be executed.
	Read array	The command can be executed.	
	Read status register		
	Clear status register		
	Read lock bit status	The command is not executed. A command sequence error occurs.	The command can be executed.
	Block blank check	Do not execute the command.	
Program suspend (Suspend while executing program or lock bit program command)	Block erase	The command is not executed. A command sequence error occurs. (1)	
	Program		
	Lock bit program		
	Read array	The command can be executed.	
	Read status register		
	Clear status register	Do not execute the command. (1)	
	Read lock bit status	Do not execute the command.	
	Block blank check		

Note:
1. If the command sequence error occurs after executing block erase, program, or lock bit program commands mistakenly during program suspend. execute the clear status register command, then restart suspend.

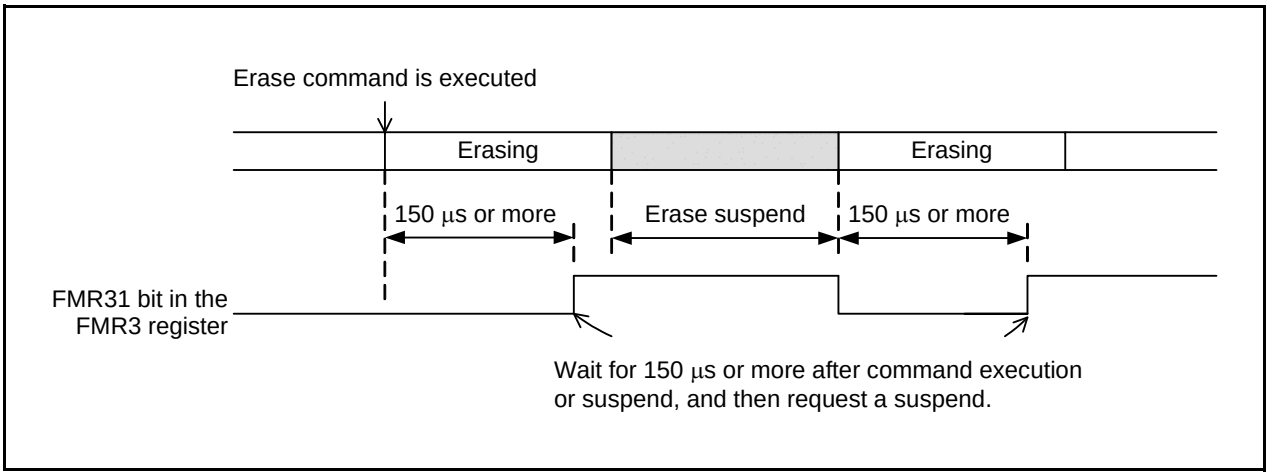


Figure 29.15 Suspend Request

29.8.6 Software Commands

Table 29.16 list Software Commands. Read or write commands and data in 16-bit units. When command code is written, the upper 8 bits (D15 to D8) are ignored.

Table 29.16 Software Commands

Command	First Bus Cycle			Second Bus Cycle			Third Bus Cycle		
	Mode	Address	Data (D15 to D0)	Mode	Address	Data (D15 to D0)	Mode	Address	Data (D15 to D0)
Read array	Write	x	xxFFh	–	–	–	–	–	–
Read status register	Write	x	xx70h	Read	x	SRD	–	–	–
Clear status register	Write	x	xx50h	–	–	–	–	–	–
Program	Write	WA	xx41h	Write	WA	WD0	Write	WA	WD1
Block erase	Write	x	xx20h	Write	BA	xxD0h	–	–	–
Lock bit program	Write	BA	xx77h	Write	BA	xxD0h	–	–	–
Read lock bit status	Write	x	xx71h	Write	BA	xxD0h	–	–	–
Block blank check (1)	Write	x	xx25h	Write	BA	xxD0h	–	–	–

SRD : Data in the status register (D7 to D0)
WA : Write address (set the end of the address to 0h, 4h, 8h, or Ch)
WD0 : Write data lower word (16 bits)
WD1 : Write data upper word (16 bits)
BA : Highest block address (even address)
x : Any even address in program ROM 1, program ROM 2, or data flash
xx : 8 upper bits of command code (ignored)
Note:
1. Block blank check command is designed for programmer manufacturer. Not for customers in general.

Software commands are described below.
For symbols shown in the flowcharts, refer to those in Table 29.16.
Refer to 29.8.5 “Suspend Function” for program, block erase, and lock bit program commands when using suspend function.

29.8.6.1 Read Array Command

The read array command is used to read the flash memory.
By writing the command code xxFFh in the first bus cycle, the flash memory enters read array mode. The value of the specified address can be read in 16-bit units by entering the address to be read after the next bus cycle.
The flash memory remains in read array mode until another command is written. Therefore, the values of multiple addresses can be read consecutively.

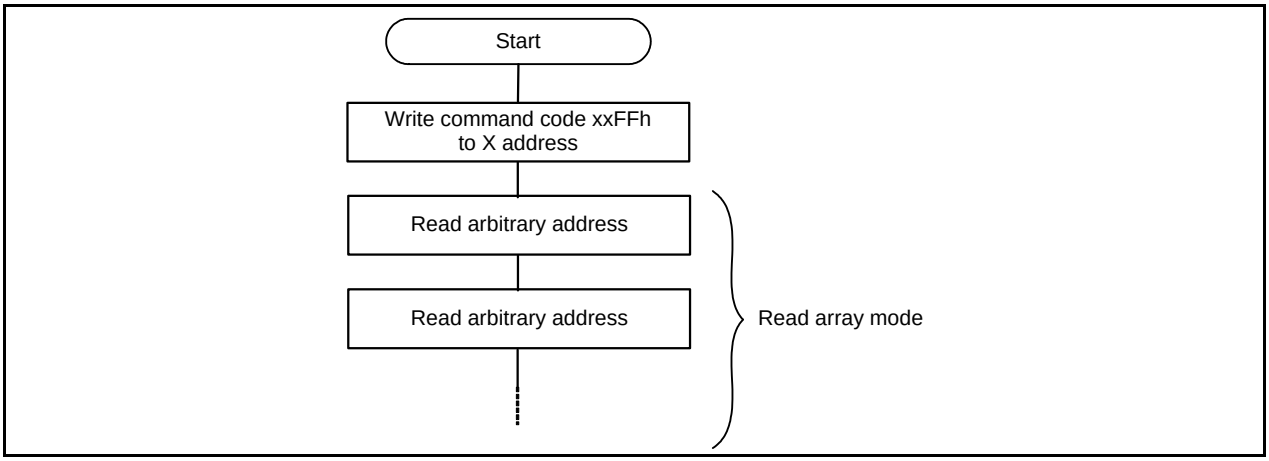


Figure 29.16 Read Array Command

29.8.6.2 Read Status Register Command

The read status register command is used to read the status register.
By writing the command code xx70h in the first bus cycle, the status register can be read in the second bus cycle. (Refer to 29.8.7 “Status Register”). To read the status register, read an even address in program ROM 1, program ROM 2, or the data flash.
Do not execute this command in EW1 mode.

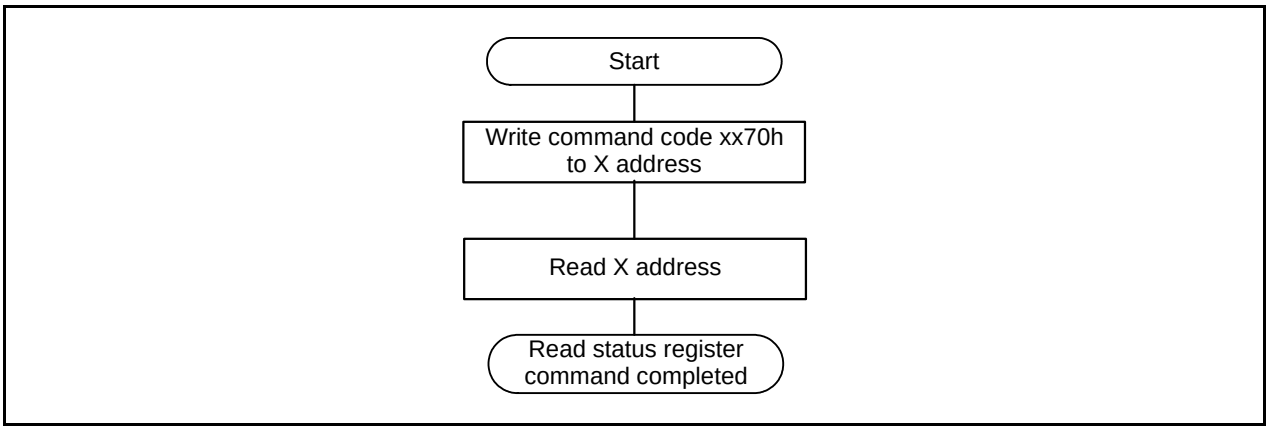


Figure 29.17 Read Status Register Command

29.8.6.3 Clear Status Register Command

The clear status register command is used to clear the status register.
By writing the command code xx50h, bits FMR07 and FMR06 in the FMR0 register (SR5 and SR4 in the status register) become 00b.

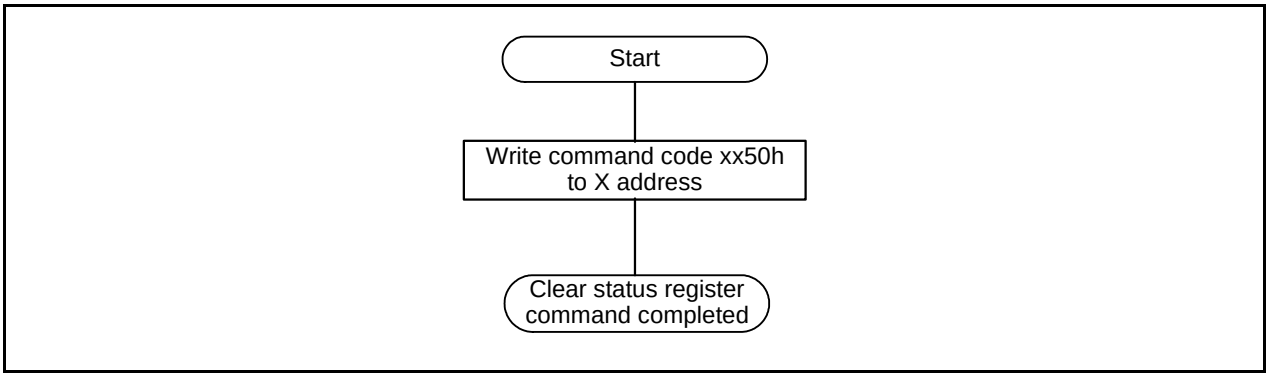


Figure 29.18 Clear Status Register Command

29.8.6.4 Program Command

The program command is used to write 2 words (4 bytes) of data to the flash memory.
By writing xx41h in the first bus cycle and data to the write address in the second and third bus cycles, an auto-program operation (data program and verify) is started. Set the end of the write address to 0h, 4h, 8h, or Ch.
The FMR00 bit in the FMR0 register indicates whether the auto-program operation has been completed. The FMR00 bit is 0 (busy) during the auto-program operation, and becomes 1 (ready) after the auto-program operation is completed. Do not execute other commands while the FMR00 bit is 0.
After the auto-program operation is completed, the FMR06 bit in the FMR0 register indicates whether or not the auto-program operation has been completed as expected. (Refer to 29.8.7.1 “Full Status Check”).
Do not rewrite the addresses already programmed. Figure 29.19 shows a flowchart of the Program Command (Suspend Function Disabled).
The lock bit protects individual blocks from being programmed inadvertently. (Refer to 29.8.4 “Data Protect Function”.)

In EW1 mode, do not execute this command on a block to which the rewrite control program is allocated.

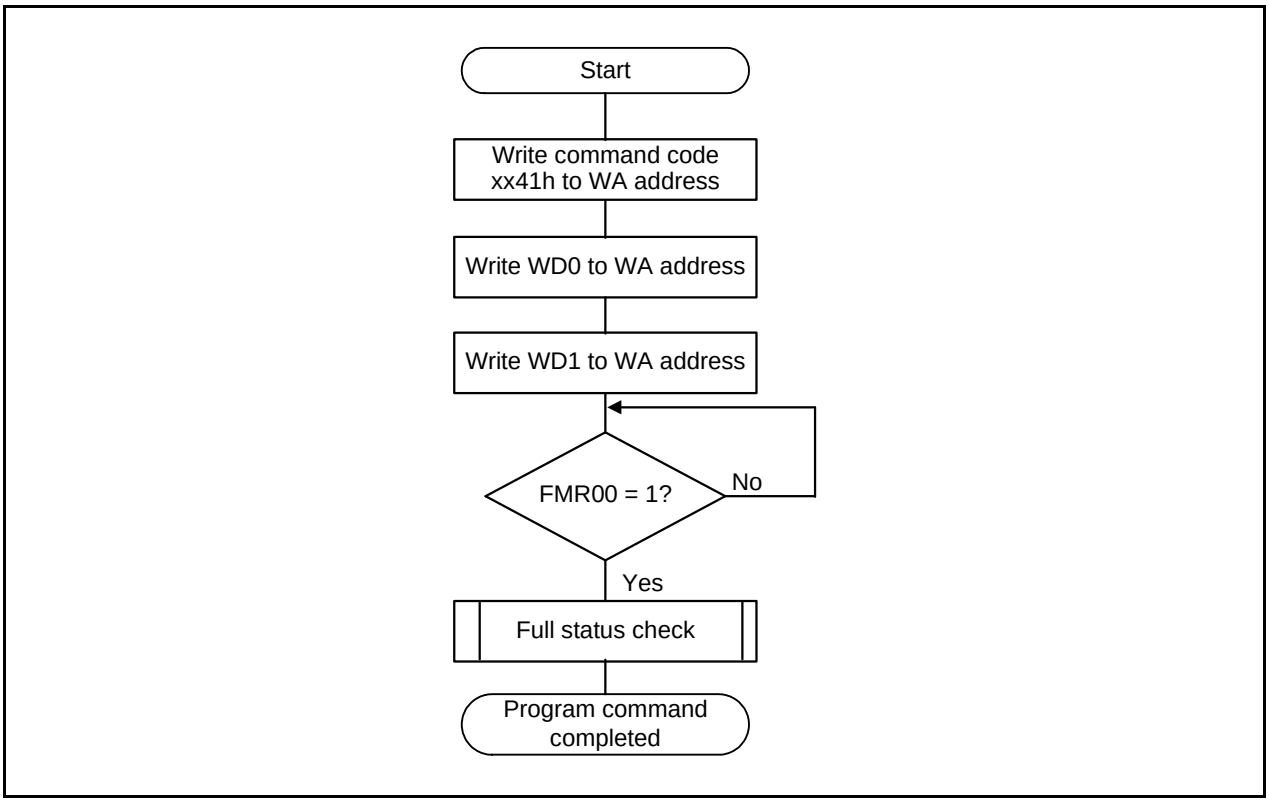


Figure 29.19 Program Command (Suspend Function Disabled)

29.8.6.5 Block Erase Command

By writing xx20h in the first bus cycle and xxD0h to the highest even address of a block in the second bus cycle, an auto-erase operation (erase and verify) is started on the specified block.
The FMR00 bit in the FMR0 register indicates whether the auto-erase operation has been completed. The FMR00 bit is 0 (busy) during the auto-erase operation, and becomes 1 (ready) when the auto-erase operation is completed. Do not execute other commands while the FMR00 bit is 0.
After the auto erase operation is completed, the FMR07 bit in the FMR0 register indicates whether or not the auto erase operation has been completed as expected. (Refer to 29.8.7.1 “Full Status Check”).
Figure 29.20 shows a flowchart of the Block Erase Command (Suspend Function Disabled).
The lock bit protects individual blocks from being erased inadvertently. (Refer to 29.8.4 “Data Protect Function”.)
In EW1 mode, do not execute this command on the block to which the rewrite control program is allocated.

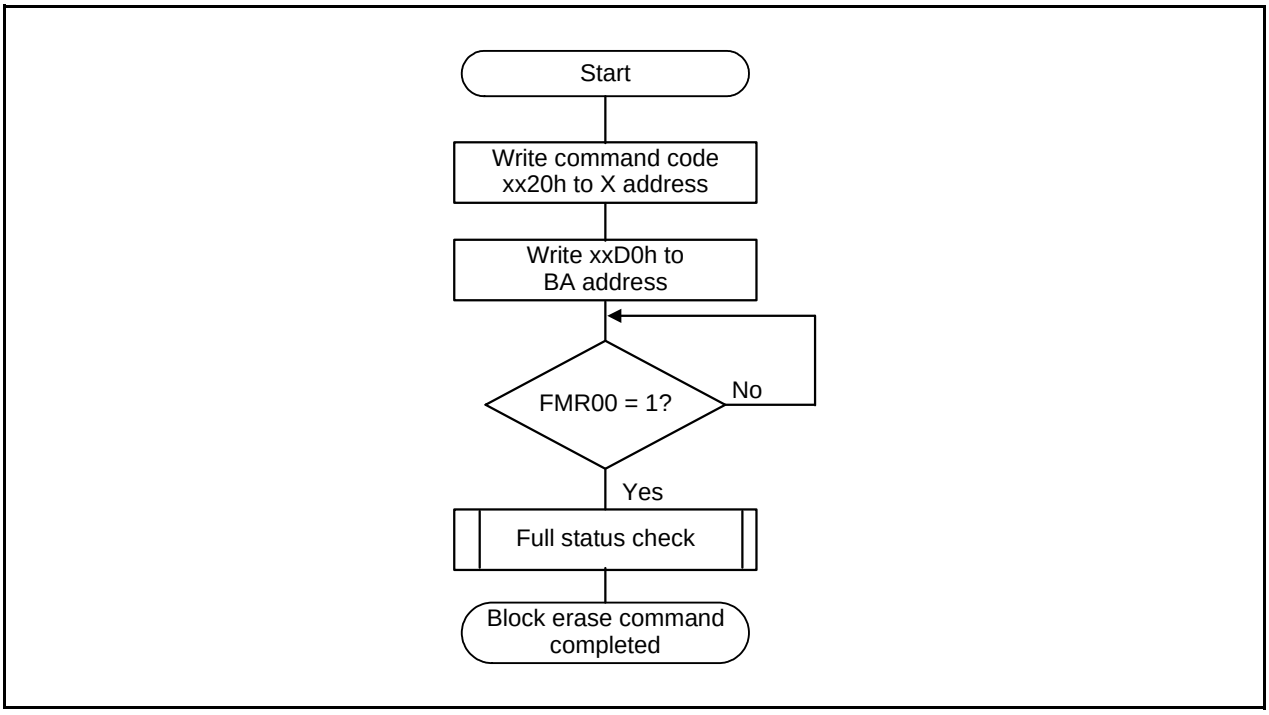


Figure 29.20 Block Erase Command (Suspend Function Disabled)

29.8.6.6 Lock Bit Program Command

The lock bit program command is used to set the lock bit for a specified block to 0 (locked).
By writing xx77h in the first bus cycle and xxD0h to the highest even address of a block in the second bus cycle, the lock bit for the specified block is set to 0. The address value specified in the first bus cycle must be the same highest address of a block specified in the second bus cycle.
Figure 29.21 shows a flowchart of the Lock Bit Program Command (Suspend Function Disabled).
Execute the read lock bit status command to read the lock bit state (lock bit data).
The FMR00 bit in the FMR0 register indicates whether a lock bit program operation has been completed. Do not execute other commands while the FMR00 bit is 0.
Refer to 29.8.4 “Data Protect Function”, for details on lock bit functions and how to set it to 1 (unlocked).

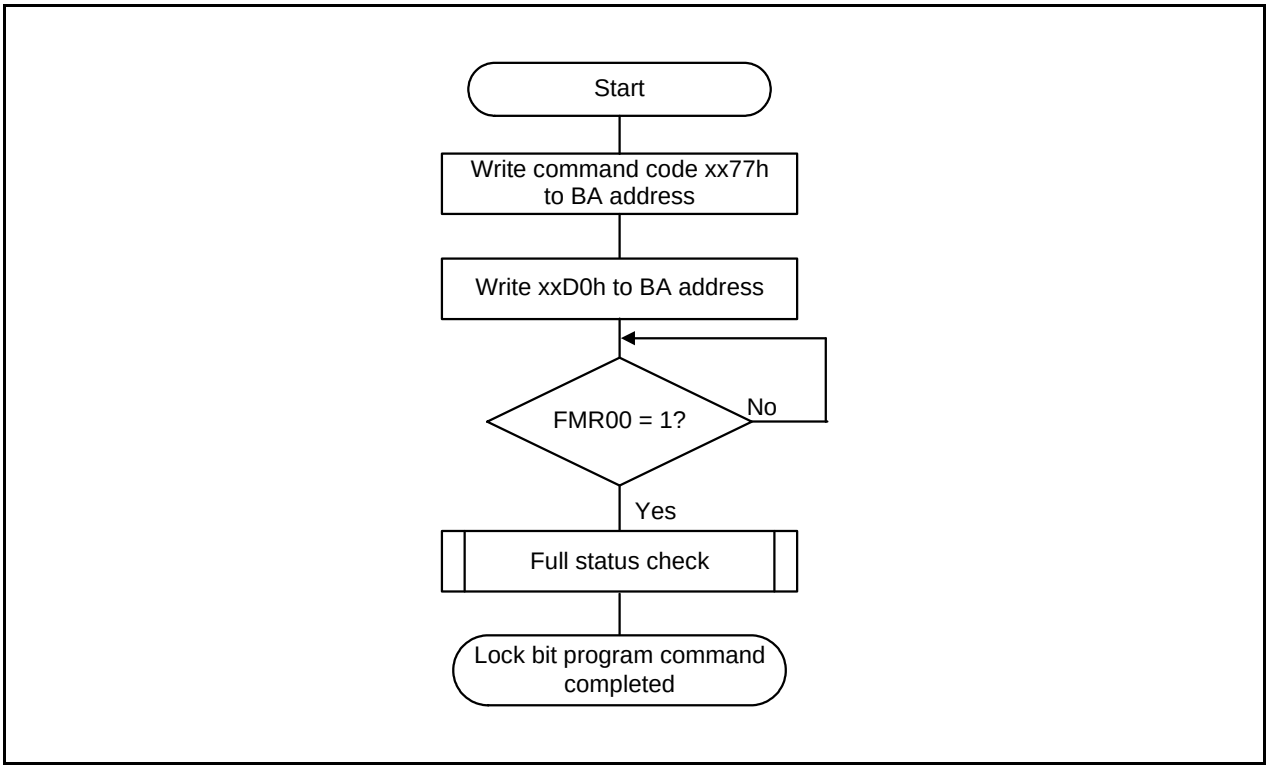


Figure 29.21 Lock Bit Program Command (Suspend Function Disabled)

29.8.6.7 Read Lock Bit Status

The read lock bit status command is used to read the lock bit state of a specified block.
By writing xx71h in the first bus cycle and xxD0h to the highest even address of a block in the second bus cycle, the FMR16 bit in the FMR1 register stores information on the lock bit status of a specified block. Read the FMR16 bit after the FMR00 bit in the FMR0 register becomes 1 (ready). Do not execute other commands while the FMR00 bit is 0.
Figure 29.22 shows a flowchart of the Read Lock Bit Status Command.

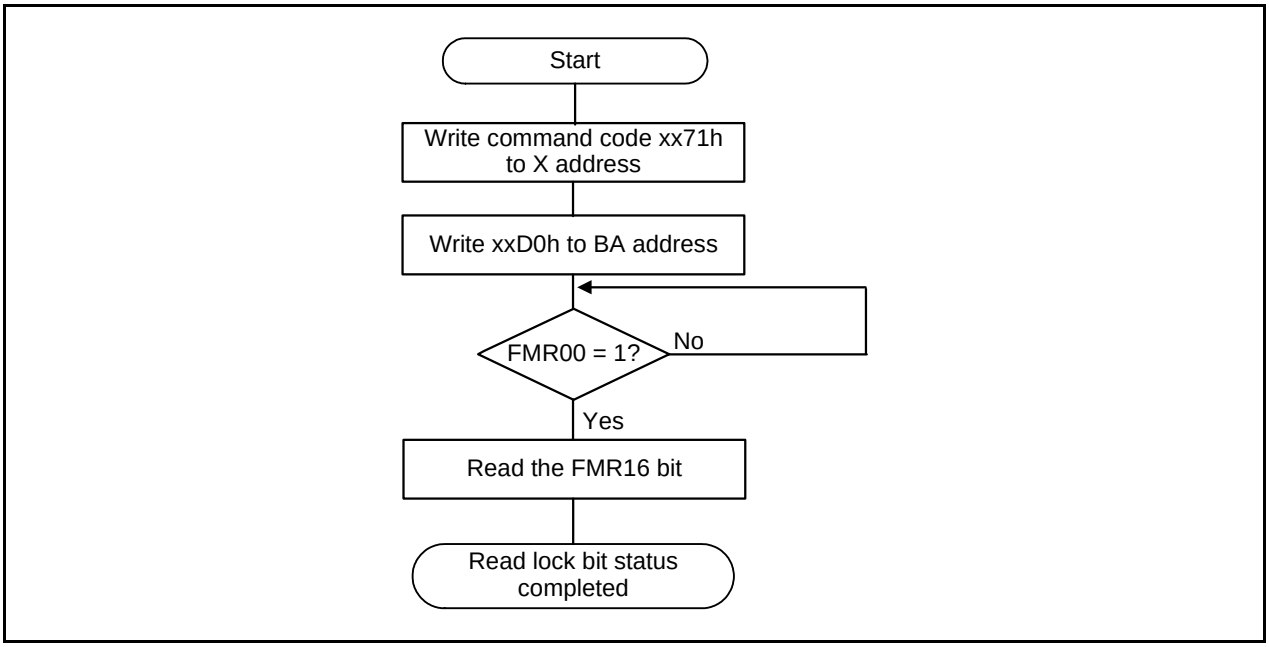


Figure 29.22 Read Lock Bit Status Command

29.8.6.8 Block Blank Check Command

The block blank check command is used to check whether or not a specified block is blank (state after erase).
By writing xx25h in the first bus cycle and xxD0h in the second bus cycle to the highest even address of a block, the check result is stored in the FMR07 bit in the FMR0 register. Read the FMR07 bit after the FMR00 bit in the FMR0 register is set to 1 (ready). Do not execute other commands while the FMR00 bit is 0.
The block blank check command is valid for unlocked blocks.
If the block blank check command is executed on a block whose lock bit is 0 (locked), the FMR07 bit (SR5) is set to 1 (not blank) regardless of the FMR02 bit state.
Figure 29.23 shows a flowchart of the Block Blank Check Command.

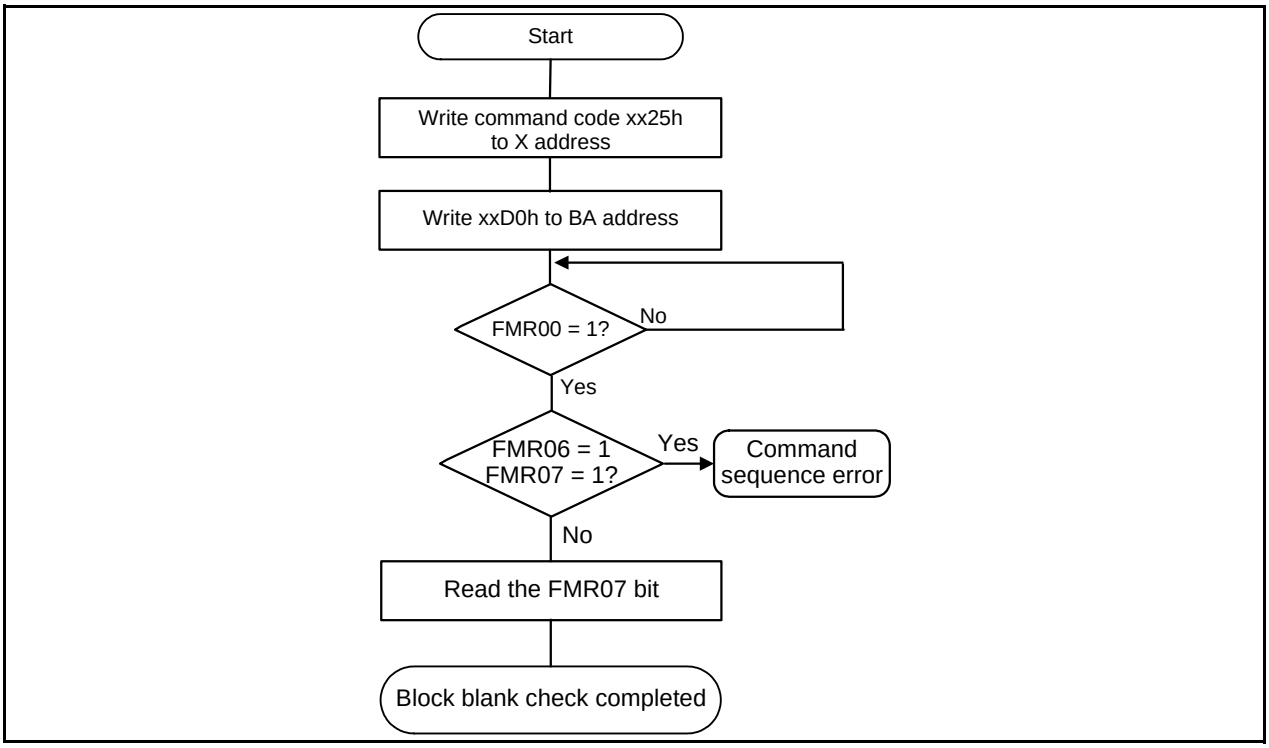


Figure 29.23 Block Blank Check Command

As a result of block blank check, when the block is not blank, execute the clear status register command before executing other software commands.

The block blank check command is designated for use with a programmer. Use this command where instantaneous power failures do not occur. When an instantaneous power failure occurs while the block erase command is executed, execute the block erase command again. The block blank check command cannot be used to check whether the erase operation is successfully completed or not.
Do not execute the block blank check command during suspend.

29.8.7 Status Register

The status register indicates flash memory operating state and whether or not an erase or program operation has been completed as expected.
Bits FMR00, FMR06, and FMR07 in the FMR0 register indicate status register states. Refer to 29.3.1 “Flash Memory Control Register 0 (FMR0)” for a description of each bit.

Table 29.17 Difference in Reading of Status Register

Item	FMR0 register	Command
Condition	No limit	
Reading procedure	Read bits FMR00, FMR06, and FMR07 in the FMR0 register	• Read any even address in program ROM 1, program ROM 2, or data flash after writing the read status register command. • Read any even address in program ROM 1, program ROM 2, or data flash after executing the program command, block erase command, lock bit program command, or block blank check command before executing the read array command.

Table 29.18 Status Register

Bits in Status Register	Bit in FMR0 Register	Status	Status		Reset Value
			0	1	
SR0 (D0)	-	Reserved	-	-	-
SR1 (D1)	-	Reserved	-	-	-
SR2 (D2)	-	Reserved	-	-	-
SR3 (D3)	-	Reserved	-	-	-
SR4 (D4)	FMR06	Program status	Completed as expected	Completed in error	0
SR5 (D5)	FMR07	Erase status	Completed as expected	Completed in error	0
SR6 (D6)	-	Reserved	-	-	-
SR7 (D7)	FMR00	Sequencer status	Busy	Ready	1

D0 to D7: The data buses read when the read status register command is executed.

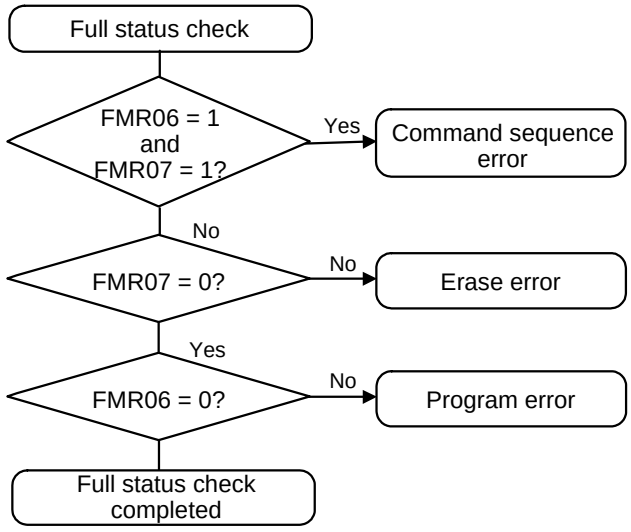
29.8.7.1 Full Status Check

If an error occurs, bits FMR06 and FMR07 in the FMR0 register become 1, indicating the occurrence of an error. Therefore, the execution results can be confirmed by checking these status bits (full status check).

Table 29.19 Errors and FMR0 Register States

FMR00 Register		Error	Error Occurrence Conditions
FMR07 bit	FMR06 bit		
1	1	Command sequence error	• Command is written incorrectly. • Data other than xxD0h and xxFFh is written in the second bus cycle of the lock bit program, block erase, block blank check, or read lock bit status command. (1)
1	0	Erase error	• The block erase command is executed on a locked block. (2) • The block erase command is executed on an unlocked block, but the auto-erase operation is not completed as expected. • The block blank check command is executed, and the check result is not blank.
0	1	Program error	• The program command is executed on a locked block. (2) • The program command is executed on an unlocked block, but the auto-program operation is not completed as expected. • The lock bit program command is executed, but the lock bit is not written as expected.

Notes:
1. When writing xxFFh in the second bus cycle of the command, the flash memory becomes the state before executing the command, and the command code written in the first bus cycle is cancelled.
2. When the FMR02 bit is 1 (lock bit disabled), no error occurs even under the conditions above.



FMR07, FMR06: Bits in the FMR0 register

Figure 29.24 Full Status Check

29.8.7.2 Handling Procedure for Errors

When errors occur, follow the procedures below.
Do not execute the program, block erase, lock bit program, and block blank check commands when either FMR06 or FMR07 bit is 1 (completed in error). Execute each command after executing the clear status register command.

Command sequence error

(1) Execute the clear status register command and set bits FMR06 and FMR07 to 0 (completed as expected).
(2) Check if the command is written correctly and execute the correct command.

Erase error

(1) Execute the clear status register command and set the FMR07 bit to 0 (completed as expected).
(2) Execute the read lock bit status command. Set the FMR02 bit in the FMR register to 1 (lock bit disabled) if the lock bit in the block where the error occurred is set to 0 (locked).
(3) Execute the block erase command again.
(4) Repeat (1) to (3) until an erase error is not generated.

If an error still occurs even after repeating three times, do not use that block.
When handling an erase error of the block blank check command and erasing is not necessary, execute (1) only.

Program error

[When a program operation is executed]

(1) Execute the clear status register command and set the FMR06 bit to 0 (completed as expected).
(2) Execute the read lock bit status command. Set the FMR02 bit in the FMR0 register to 1 if the lock bit in the block where the error occurred is set to 0.
(3) Execute the program command again.

If the lock bit is set to 1 (unlocked), do not use the address in which error has occurred as it is. Execute the block erase command to erase the block, in which the error has occurred, before executing the program command to write to the same address again.
If an error still occurs, do not use that block.

[When a lock bit program operation is executed]

(1) Execute the clear status register command and set the FMR06 bit to 0.
(2) Set the FMR02 bit in the FMR0 register to 1.
(3) Execute the block erase command to erase the block where the error occurred.
(4) Execute the lock bit program command again after writing the data as needed.

If an error still occurs, do not use that block.

29.9 Standard Serial I/O Mode

In standard serial I/O mode, a serial programmer supporting the M16C/5M Group, M16C/57 Group can be used to rewrite program ROM 1, program ROM 2, and data flash while the MCU is mounted on a board. Standard serial I/O mode has following modes:

- Standard serial I/O mode 1: The MCU is connected to the serial programmer by using clock synchronous serial I/O
- Standard serial I/O mode 2: The MCU is connected to the serial programmer by using 2-wire clock asynchronous serial I/O

For more information about the serial programmer, contact the serial programmer manufacturer. Refer to the user's manual included with your serial programmer for instructions.

29.9.1 ID Code Check Function

Use the ID code check function in standard serial I/O mode. This function determines whether the ID codes sent from the serial programmer match those written in the flash memory. If the ID codes do not match, commands sent from the serial programmer are not accepted. However, if the 4 bytes of the reset vector are FFFFFFFFh, ID codes are not compared, allowing all commands to be accepted.
The ID codes are 7-byte data stored consecutively, starting with the first byte, at addresses 0FFFDFh, 0FFFE3h, 0FFFEBh, 0FFFEFh, 0FFFF3h, 0FFFF7h, and 0FFFFBh. The flash memory must have a program with the ID codes set in these addresses. Figure 29.25 shows ID Code Storage Addresses.
The ID code of “ALeRASE” in ASCII code is used for forced erase function. The ID code “Protect” in ASCII code is used for standard serial I/O mode disable function. Table 29.20 lists Reserved Word of ID Code. All ID code storage addresses and data must match the combinations listed in Table 29.20. When the forced erase function or standard serial I/O mode disable function is not used, use another combination of ID codes.

Table 29.20 Reserved Word of ID Code

ID Code Storage Address		Reserved Word of ID Code (ASCII)	
		ALeRASE	Protect
FFFDFh	ID1	41h (upper-case A)	50h (upper-case P)
FFFE3h	ID2	4Ch (upper-case L)	72h (lower-case r)
FFFEBh	ID3	65h (lower-case e)	6Fh (lower-case o)
FFFEFh	ID4	52h (upper-case R)	74h (lower-case t)
FFFF3h	ID5	41h (upper-case A)	65h (lower-case e)
FFFF7h	ID6	53h (upper-case S)	63h (lower-case c)
FFFFBh	ID7	45h (upper-case E)	74h (lower-case t)

All ID code storage addresses and data must match the combinations listed in Table 29.20.

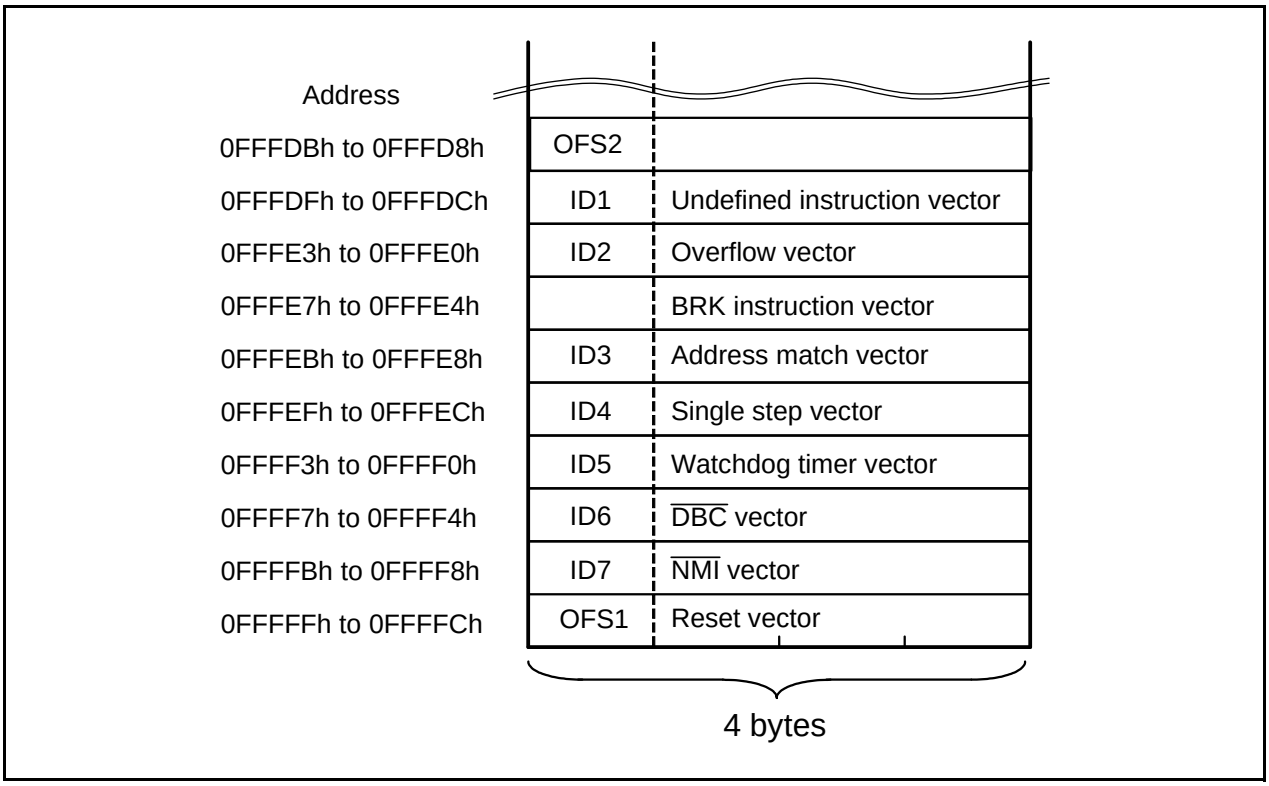


Figure 29.25 ID Code Storage Addresses

29.9.2 Forced Erase Function

Use the forced erase function in standard serial I/O mode. When the reserved word, “ALeRASE” in ASCII code, is sent from the serial programmer as an ID code, the contents of program ROM 1 and program ROM 2 will all be erased. However, if the ID codes stored in the ID code storage addresses are set to a reserved word other than “ALeRASE” (other than the combination table listed in Table 29.20), the ROMCR bit in the OFS1 address is 1 (ROMCP1 bit enabled), and the ROMCP1 bit in the OFS1 address is 0 (ROM code protect enabled), the forced erase function is ignored and ID code check is executed by the ID code check function. Table 29.21 lists conditions and functions for forced erase function.

When both the ID codes sent from the serial programmer and the ID codes stored in the ID code storage addresses correspond to the reserved word “ALeRASE”, program ROM 1 and program ROM 2 will be erased. However, when the serial programmer sends other than “ALeRASE”, even if the ID codes stored in the ID code storage addresses are “ALeRASE”, there is no ID match and no command is accepted. The flash memory cannot be operated.

Table 29.21 Forced Erase Function

Condition			Function
ID code from serial programmer	Code in ID code storage address	ROMCP1 bit in the OFS1 address	
ALeRASE	ALeRASE	–	Program ROM 1 and program ROM 2 all erase (forced erase function)
	Other than ALeRASE (1)	1 (ROM code protect disabled)	
		0 (ROM code protect enabled)	ID code check (ID code check function. No ID match)
Other than ALeRASE	ALeRASE	–	ID code check (ID code check function. No ID match)
	Other than ALeRASE (1)	–	ID code check (ID code check function)

Note:
1. When the combination of the stored addresses is “Protect”, refer to 29.9.3 “Standard Serial I/O Mode Disable Function”.

29.9.3 Standard Serial I/O Mode Disable Function

Use the standard serial I/O mode disable function in standard serial I/O mode. When the ID codes in the ID code stored addresses are set to “Protect” in ASCII code (see Table 29.20 “Reserved Word of ID Code”), the MCU does not communicate with the serial programmer. Therefore, the flash memory cannot be read, written or erased by the serial programmer. User boot mode can be selected even when the ID codes are set to “Protect”.

When the ID codes are set to “Protect”, the ROMCR bit in the OFS1 address is 1 (ROMCP1 bit enabled), and the ROMCP1 bit in the OFS1 address is set to 0 (ROM code protect enabled), ROM code protection cannot be disabled by the serial programmer. Therefore, the flash memory cannot be read, written, or erased by the serial or parallel programmer.

29.9.4 Standard Serial I/O Mode 1

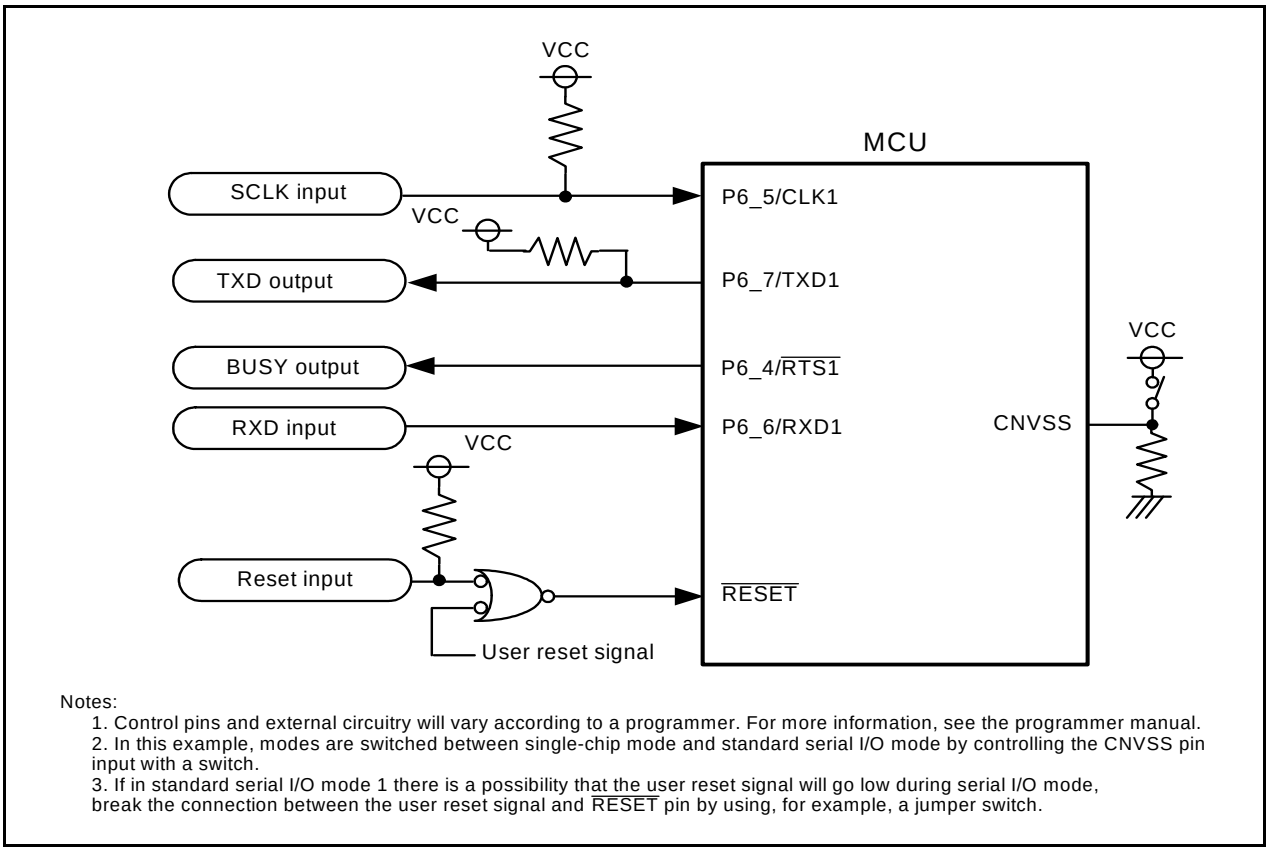
In standard serial I/O mode 1, a serial programmer is connected to the MCU using clock synchronous serial I/O.

Table 29.22 Pin Functions (Flash Memory Standard Serial I/O Mode 1)

Pin	Name	I/O	Description
VCC, VSS	Power input		Apply the flash memory program and erase voltage to the VCC pin. Apply 0 V to the VSS pin.
CNVSS	CNVSS	Input	Connect to the VCC pin.
$\overline{\text{RESET}}$	Reset input	Input	Reset input pin.
XIN	Clock input	Input	Input a high-level signal to the XIN pin and open the XOUT pin when a main clock is not used. Connect a ceramic resonator or crystal between pins XIN and XOUT when the main clock is used. To input an externally generated clock, input it to the XIN pin and open the XOUT pin.
XOUT	Clock output	Output	
AVCC, AVSS	Analog power supply input		Connect the AVCC pin to VCC and the AVSS pin to VSS, respectively.
VREF	Reference voltage input	Input	Reference voltage input pin for A/D converter. When using standard serial I/O mode 1, and power supply to VREF is not supplied, connect with VSS.
P0_0 to P0_7	Input port P0	Input	Input a high- or low-level signal or leave open.
P1_0 to P1_7	Input port P1	Input	Input a high- or low-level signal or leave open.
P2_0 to P2_7	Input port P2	Input	Input a high- or low-level signal or leave open.
P3_0 to P3_7	Input port P3	Input	Input a high- or low-level signal or leave open.
P4_0 to P4_7	Input port P4	Input	Input a high- or low-level signal or leave open.
P5_0 to P5_7	Input port P5	Input	Input a high- or low-level signal or leave open.
P6_0 to P6_3	Input port P6	Input	Input a high- or low-level signal or leave open.
P6_4 / $\overline{\text{RTS1}}$	BUSY output	Output	BUSY signal output pin
P6_5/CLK1	SCLK input	Input	Serial clock input pin
P6_6 / RXD1	RXD input	Input	Serial data input pin.
P6_7 / TXD1	TXD output	Output	Serial data output pin.
P7_0 to P7_7	Input port P7	Input	Input a high- or low-level signal or leave open.
P8_0 to P8_7	Input port P8	Input	Input a high- or low-level signal or leave open.
P9_0 to P9_7	Input port P9	Input	Input a high- or low-level signal or leave open.
P10_0 to P10_7	Input port P10	Input	Input a high- or low-level signal or leave open.

Table 29.23 Setting of Standard Serial I/O Mode 1

Signal	Input Level
CNVSS	VCC
$\overline{\text{RESET}}$	VSS → VCC
SCLK	VCC



Notes:
1. Control pins and external circuitry will vary according to a programmer. For more information, see the programmer manual.
2. In this example, modes are switched between single-chip mode and standard serial I/O mode by controlling the CNVSS pin input with a switch.
3. If in standard serial I/O mode 1 there is a possibility that the user reset signal will go low during serial I/O mode, break the connection between the user reset signal and $\overline{\text{RESET}}$ pin by using, for example, a jumper switch.

Figure 29.26 Circuit Application in Standard Serial I/O Mode 1

29.9.5 Standard Serial I/O Mode 2

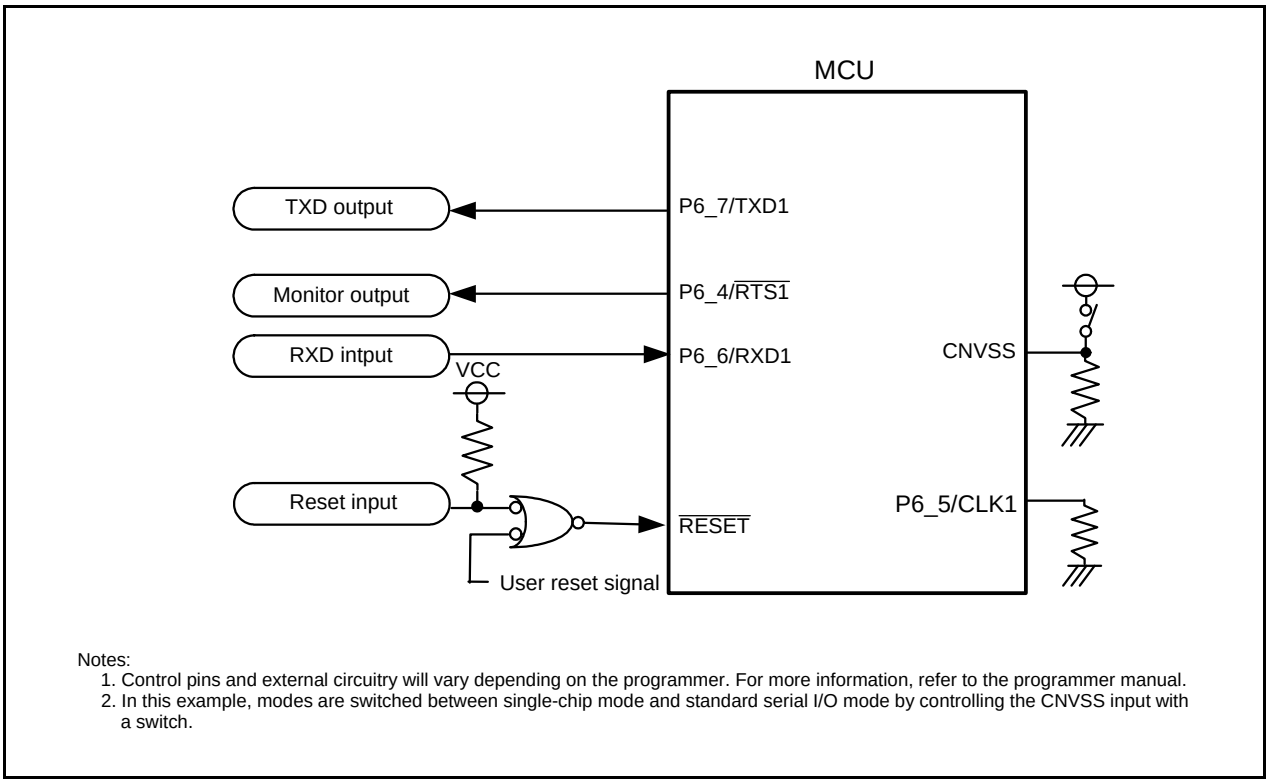
In standard serial I/O mode 2, a serial programmer is connected to the MCU by using 2-wire clock asynchronous serial I/O. The main clock is used.

Table 29.24 Pin Functions (Flash Memory Standard Serial I/O Mode 2)

Pin	Name	I/O	Description
VCC, VSS	Power input		Apply the flash memory program and erase voltage to the VCC pin. Apply 0 V to the VSS pin.
CNVSS	CNVSS	I	Connect to the VCC pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin.
XIN	Clock input	I	Connect a ceramic resonator or crystal between pins XIN and XOUT. To input an externally generated clock, input it to the XIN pin and open the XOUT pin.
XOUT	Clock output	O	
AVCC, AVSS	Analog power supply input		Connect the AVCC pin to VCC and the AVSS pin to VSS, respectively.
VREF	Reference voltage input	I	Reference voltage input pin for A/D converter. When using standard serial I/O mode 2, and power supply to VREF is not supplied, connect with VSS.
P0_0 to P0_7	Input port P0	I	Input a high- or low-level signal or leave open.
P1_0 to P1_7	Input port P1	I	Input a high- or low-level signal or leave open.
P2_0 to P2_7	Input port P2	I	Input a high- or low-level signal or leave open.
P3_0 to P3_7	Input port P3	I	Input a high- or low-level signal or leave open.
P4_0 to P4_7	Input port P4	I	Input a high- or low-level signal or leave open.
P5_0 to P5_7	Input port P5	I	Input a high- or low-level signal or leave open.
P6_0 to P6_3	Input port P6	I	Input a high- or low-level signal or leave open.
P6_4 / $\overline{\text{RTS1}}$	BUSY output	O	Monitor signal output pin for checking the boot program operation.
P6_5/CLK1	SCLK input	I	Input a low-level signal
P6_6 / RXD1	RXD input	I	Serial data input pin.
P6_7 / TXD1	TXD output	O	Serial data output pin.
P7_0 to P7_7	Input port P7	I	Input a high- or low-level signal or leave open.
P8_0 to P8_7	Input port P8	I	Input a high- or low-level signal or leave open.
P9_0 to P9_7	Input port P9	I	Input a high- or low-level signal or leave open.
P10_0 to P10_7	Input port P10	I	Input a high- or low-level signal or leave open.

Table 29.25 Setting of Standard Serial I/O Mode 2

Signal	Input Level
CNVSS	VCC
$\overline{\text{RESET}}$	VSS → VCC
P6_5/CLK1	VSS



Notes:
1. Control pins and external circuitry will vary depending on the programmer. For more information, refer to the programmer manual.
2. In this example, modes are switched between single-chip mode and standard serial I/O mode by controlling the CNVSS input with a switch.

Figure 29.27 Circuit Application in Standard Serial I/O Mode 2

29.10 Parallel I/O Mode

In parallel I/O mode, program ROM 1, program ROM 2, and data flash can be rewritten using a parallel programmer supporting the M16C/5M Group, M16C/57 Group. Contact the parallel programmer manufacturer for more information. Refer to the user's manual included with your parallel programmer for instructions.

29.10.1 ROM Code Protect Function

The ROM code protect function disables the flash memory from being read or rewritten during parallel I/O mode. Refer to 29.4.1 "Optional Function Select Address 1 (OFS1)". The OFS1 address is located in block 0 of program ROM 1.

When the ROMCR bit in the OFS1 address is 1 (ROMCP1 bit enabled) and the ROMCP1 bit is set to 0, the ROM code protect function is enabled.

To cancel ROM code protect, erase block 0 including the OFS1 address using standard serial I/O mode or CPU rewrite mode.

29.11 Notes on Flash Memory

29.11.1 OFS1 Address, OFS2 Address, and ID Code Storage Address

The OFS1 address, OFS2 address, and ID code storage address are part of flash memory. When writing a program to flash memory, write an appropriate value to those addresses simultaneously.

In the OFS1 address, the MCU state after reset and the function to prevent rewrite in parallel I/O mode are selected. The OFS1 address is 0FFFFFh. This is the most significant address of block 0 in program ROM 1 and upper address of reset vector. Also, OFS2 address and the ID code storage address is in block 0 and upper address of the interrupt vector.

The ID code check function cannot be disabled. Even if the protect using the ID code check function is unnecessary, input the appropriate ID code when using a serial programmer or debugger. Without the appropriate ID code, the serial programmer or debugger cannot be used.

ex) Set FEh to the OFS1 address, and set FFh to the OFS2 address

When using an address control instruction and logical addition:

```
.org 0FFDBH
.byte 0FFh
.org 0FFFFCh
RESET:
.lword start | 0FE000000h
```

When using an address control instruction:

```
.org 0FFDBH
.byte 0FFh
.org 0FFFFCh
RESET:
.addr start
.byte 0FEh
```

(Program format varies depending on the compiler. Refer to the compiler manual.)

29.11.2 Reading Data Flash

When 3.0 V < VCC ≤ 5.5 V and f(BCLK) ≥ 20 MHz, one wait must be inserted to execute the program on the data flash and read the data. Set the PM17 in the PM1 register or FMR17 bit in the FMR1 register to insert one wait.

29.11.3 CPU Rewrite Mode

29.11.3.1 Operating Speed

Select a CPU clock frequency of 16 MHz or less by setting the CM06 bit in the CM0 register and bits CM17 and CM16 in the CM1 register before entering CPU rewrite mode (EW0 or EW1 mode). Also, set the PM17 bit in the PM1 register to 1 (wait state).

29.11.3.2 CPU Rewrite Mode Select

Change FMR01 bit in the FMR0 register, FMR11 bit in the FMR1 register, and FMR60 bit in the FMR6 register while in the following state:

- The PM24 bit in the PM2 register is 0 ($\overline{\text{NMI}}$ interrupt disabled).
- High is input to the $\overline{\text{NMI}}$ pin.

Change the FMR60 bit while the FMR00 bit in the FMR0 register is 1 (ready).

29.11.3.3 Prohibited Instructions

Do not use the following instructions in EW0 mode:
UND instruction, INTO instruction, JMPS instruction, JSRS instruction, and BRK instruction.

29.11.3.4 Interrupts (EW0 Mode and EW1 Mode)

- Do not use an address match interrupt during command execution because the address match interrupt vector is located in ROM.
- Do not use a non-maskable interrupt during block 0 erase because fixed vector is located in block 0.

29.11.3.5 Rewrite (EW0 Mode)

If the power supply voltage drops while rewriting the block where the rewrite control program is stored, the rewrite control program is not correctly rewritten. This may prevent the flash memory from being rewritten. If this error occurs, use standard serial I/O mode or parallel I/O mode for rewriting.

29.11.3.6 Rewrite (EW1 Mode)

Do not rewrite any blocks in which the rewrite control program is stored.

29.11.3.7 DMA transfer

In EW0 mode, do not use flash memory as a source of the DMA transfer.
In EW1 mode, do not generate a DMA transfer while the FMR00 bit in the FMR0 register is 0 (auto programming or auto erasing).

29.11.3.8 Wait Mode

To enter wait mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before executing the WAIT instruction.

29.11.3.9 Stop Mode

To enter stop mode, set the FMR01 bit to 0 (CPU rewrite mode disabled), and then disable DMA transfer before setting the CM10 bit in the CM 1 register to 1 (stop mode).

29.11.3.10 Software Command

Observe the notes below when using the following commands.

- Program
- Block erase
- Lock bit program
- Read lock bit status
- Block blank check

(a) The FMR00 bit in the FMR0 register indicates the status while executing these commands. Do not execute other commands while the FMR00 bit is 0 (busy).

(b) Use these commands in 40 MHz on-chip oscillator mode, high-speed mode, medium-speed mode, and PLL operating mode. Do not change clock modes while the FMR00 bit in the FMR0 register is 0 (busy).

(c) After executing the program, block erase, or lock bit program command, perform a full status check per command (Do not execute multiple commands or same command more than once before performing a full status check).

(d) Do not execute the program, block erase, lock bit program, or block blank check command when either or both bits FMR06 and FMR07 in the FMR0 register are 1 (error).

(e) Do not use these commands in slow read mode (when the FMR22 bit is 1) or low current consumption read mode (when both bits FMR22 and FMR23 are 1).

29.11.3.11 Program and Erase Cycles and Execution Time

Execution time of the program, block erase, and lock bit program commands becomes longer as the number of programming and erasing increases.

29.11.3.12 Suspending the Auto-Erase and Auto-Program Operations

When the program, block erase, and lock bit program commands are suspended, the blocks for those commands must be erased. Execute the program and lock bit program commands again after erasing.

Those commands are suspended by the following reset or interrupts:

- Hardware, power-on, voltage monitor 0, voltage monitor 2, oscillator stop detect, watchdog timer, software resets.
- $\overline{\text{NMI}}$, watchdog timer, oscillator stop/restart detect, and voltage monitor 2 interrupts.

29.11.4 User Boot

29.11.4.1 User Boot Mode Program

Note the following when using user boot mode:

- When using user boot mode, make sure to allocate the program to be executed to program ROM 2.
- The LVDAS bit in the OFS1 address and bits WDTRCS1 and WDTRCS0 in the OFS2 address are disabled in boot mode.
- When restarting the MCU in user boot mode after starting it in user boot mode, RAM becomes undefined.
- If addresses 13FF8h to 13FFBh are all 00h, the MCU does not enter standard serial I/O mode. Therefore, the programmer or on-chip debugger cannot be connected.
- As the reset sequence differs, the time necessary for starting the program is longer than in single-chip mode.
- Functions in user boot mode cannot be debugged by the on-chip debugging emulator or full spec emulator.
- While using user boot mode, do not change the input level of the pin used for user boot entry. However, if there is a possibility that the input level may change, perform the necessary processes in user boot mode, then restart the MCU in single-chip mode before the input level changes.
- To use user boot mode after standard serial I/O mode, turn off the power when exiting standard serial I/O mode, and then turn on the power again (cold start). The MCU enters user boot mode under the right conditions.

30. E2PROM Emulation Data Flash

30.1 Overview

The E2PROM emulation data flash (hereafter referred to as E2dataFlash) is a data flash that utilizes the strengths of serial E2PROMs. The units erased are considerably smaller than that of the data flash, and the E2dataFlash can program or erase without stopping the CPU.

Table 30.1 and Figure 30.1 show specifications and the block diagram of the E2dataFlash, respectively.

Table 30.1 E2dataFlash Specifications

Item	Specification	
	ECC disabled	ECC enabled
Memory size	4 KB	2 KB
Block size	32 bytes	16 bytes
Number of blocks	128	
Unit to be programmed	2 bytes	1 byte
Unit to be erased	1 block (after erase, the memory value is 1.)	
How to control program and erase	By software commands	
Software commands	4	
Error correction	None	Corrects 1-bit error per byte

ECC: Error Check and Correct

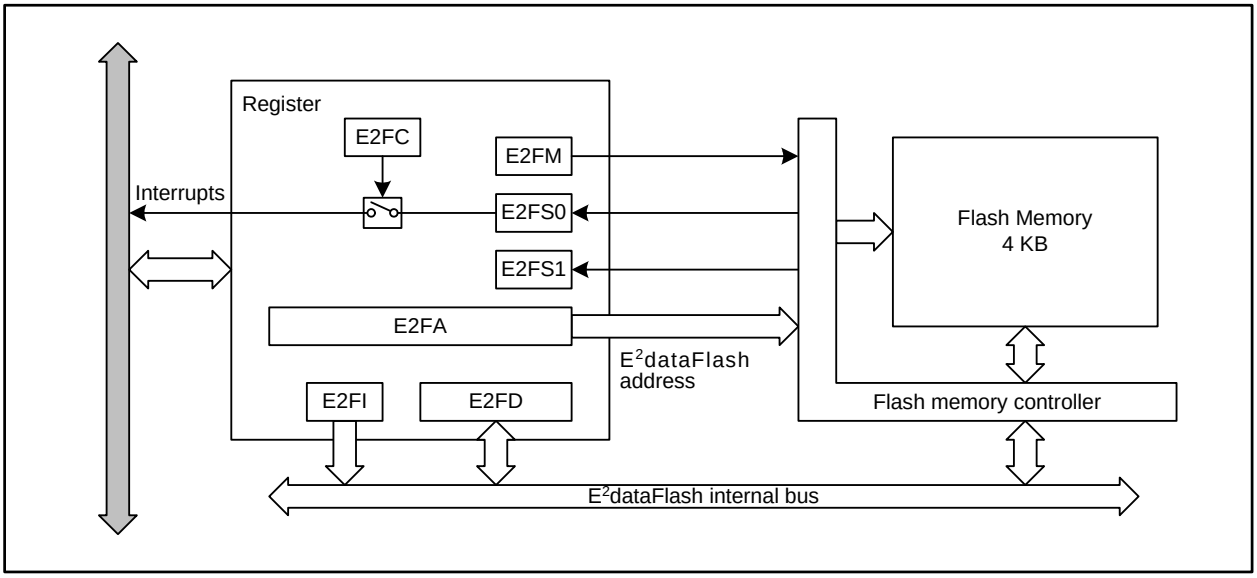


Figure 30.1 E2dataFlash Block Diagram

The CPU indirectly accesses the E2dataFlash via registers E2FA, E2FI, and E2FD that are set for SFR space.

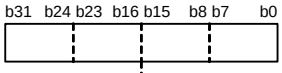
30.2 Registers

Table 30.2 Registers

Address	Register	Symbol	Reset Value
0080h	E2dataFlash Address Register	E2FA	00h
0081h			00h
0082h			XXh
0083h			XXh
0088h	E2dataFlash Command Register	E2FI	00h
0089h			XXh
008Ch	E2dataFlash Data Register	E2FD	XXh
008Dh			XXh
0090h	E2dataFlash Mode Register	E2FM	00h
0092h	E2dataFlash Control Register	E2FC	XXXX XXX0b
0094h	E2dataFlash Status Register 1	E2FS1	XXXX XXX0b
00A1h	E2dataFlash Status Register 0	E2FS0	0X00 XXXXb

30.2.1 E2dataFlash Address Register (E2FA)

E2dataFlash Address Register



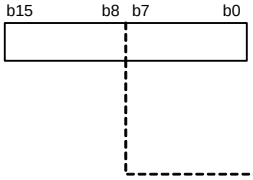
Symbol	Address	Reset Value
E2FA	0083h-0080h	XXXX 0000h

Function	Setting Range	RW
Set an address to be accessed. The 2 upper bytes are read as an undefined value.	14000h to 14FFEh (for ECC disabled) 14000h to 147FFh (for ECC enabled)	RW

The memory space of the E2dataFlash is not the same as that of the MCU. The E2dataFlash memory address is the E2FA register value.
When the ECC bit in the E2FM register is 0 (ECC disabled), set the E2FA register to an even address (LSB is 0) to write or read to the E2dataFlash. When erasing, set the highest-order even address of the corresponding block.

30.2.2 E2dataFlash Command Register (E2FI)

E2dataFlash Command Register



Symbol	Address	Reset Value
E2FI	0089h, 0088h	XX00h

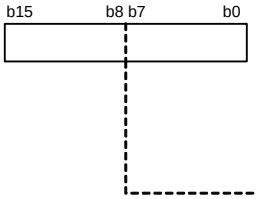
Function	Setting Range	RW
Set a command for the flash memory. The upper byte is read as an undefined value.	0020h, 0040h, 0050h, 00D0h, 00F3h	RW

Read and Write to the E2FI register in 16-bit units.
Refer to the table below for details on the setting values. Two values need to be written for block erase.
When writing to the E2FI register, check that the RDY bit in the E2FS0 register is 1.

Command	Setting Value
Read	00F3h
Program	0040h
Block Erase	0020h, 00D0h
Clear status register	0050h

30.2.3 E2dataFlash Data Register (E2FD)

E2dataFlash Data Register



Symbol	Address	Reset Value
E2FD	008Dh-008Ch	Undefined

Function	Setting Range	RW
After a read command, the data of the address written to the E2FA register is read. After a program command, the data set to this register is written to the address set to the E2FA register.	0000h to FFFFh (for ECC disabled) 0000h to 00FFh (for ECC enabled)	RW

Read and Write to the E2FD register in 16-bit units.
When programming, write the data to this register after writing 0040h to the E2FI register.

30.2.4 E2dataFlash Mode Register (E2FM)

E2dataFlash Mode Register

b7	b6	b5	b4	b3	b2	b1	b0
	0	0	0	0			

Symbol: E2FM
Address: 0090h
Reset Value: 00h

Bit Symbol	Bit Name	Function	RW
OM	Operating mode select bit	0: E2dataFlash stopped 1: E2dataFlash operating	RW
RST	E2dataFlash reset bit	0: Normal operating 1: E2dataFlash Reset	RW
EWM	EW mode setting bit	0: Erase/program disable mode 1: Erase/program enable mode	RW
— (b6-b3)	Reserved	Set to 0.	RW
ECC	ECC control bit	0: ECC disabled 1: ECC enabled	RW

Rewrite the E2FM register after setting the PRC7 bit in the PRCR register to 1 (write enabled).
When activating the E2dataFlash from sleep mode, set bits OM, EWM, and ECC, and check that the RDY bit in the E2FS0 register is 1 before rewriting or reading the E2dataFlash.

RST (E2dataFlash reset bit) (b1)

When the RST bit is 1 (E2dataFlash reset), an operation selected by the E2FI register is stopped. After stopping the operation, check that the RDY bit is 1 before setting it to 0.
When the RST bit is 1, both bits WERR and EERR in the E2FS0 register are 0 (no error).

EWM (EW mode setting bit) (b2)

When the EWM bit is 0 (erase/write disable mode), any write access results in setting 00F3h (read command) to the E2FI register.

ECC (ECC control bit) (b7)

After setting the ECC bit and programming the E2dataFlash memory, do not change the ECC bit from 0 (ECC disabled) to 1 (ECC enabled), or from 1 to 0.

30.2.5 E2dataFlash Control Register (E2FC)

E2dataFlash Control Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	Reset Value
E2FC	0092h	XXXX XXX0b

Bit Symbol	Bit Name	Function	RW
RIE	Ready interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	RW
— (b7-b1)	No register bits. If necessary, set to 0. The read value is undefined.		—

RIE (Ready interrupt enable bit) (b0)

When the RDY bit in the E2FS0 register becomes 1 while the RIE bit is 1, an E2dataFlash interrupt request is generated.

30.2.6 E2dataFlash Status Register 1 (E2FS1)

E2dataFlash Status Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	Reset Value
E2FS1	0094h	XXXX XXX0b

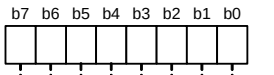
Bit Symbol	Bit Name	Function	RW
OMM	Operating mode monitor flag	0: E2dataFlash stopped 1: E2dataFlash operating	RO
— (b7-b1)	No register bits. If necessary, set to 0. The read value is undefined.		—

OMM (Operating mode monitor flag) (b0)

After setting the OM bit in the E2FM register to 1, the E2dataFlash transition to operating state can be confirmed.

30.2.7 E2dataFlash Status Register 0 (E2FS0)

E2dataFlash Status Register 0



Symbol	Address	Reset Value
E2FS0	00A1h	0X00 XXXXb

Bit Symbol	Bit Name	Function	RW
— (b3-b0)	Reserved	The read value is undefined.	RO
WERR	Program error flag	0: No write error 1: Write error occurred	RO
EERR	Erase error flag	0: No erase error 1: Erase error occurred	RO
— (b6)	Reserved	The read value is undefined.	RO
RDY	Ready flag	0: Busy 1: Ready	RO

When reading the E2FS0 register after writing the E2FD or E2FI register, insert at least four NOP instructions before reading the E2FS0 register.

WERR (Program error flag) (b4)
EERR (Erase error flag) (b5)

Conditions to become 0:

- Execute the clear status command.
- Set the RST bit in the E2FM register to 1 (E2dataFlash reset).

Condition to become 1:

- Refer to 30.5 “Full Status Check” for details.

Do not execute the program and block erase commands when the WERR or EERR bit is 1.

RDY (Ready flag) (b7)

The RDY bit becomes 0 under either of the following conditions:

- The period between setting the OM bit in the E2FM register to 1 (E2dataFlash operating) and the OMM bit in the E2FS1 register becoming 1 (E2dataFlash operating)
- During processing by the E2F1 register

The RDY bit becomes 1 when the E2dataFlash mode can be changed or when a command can be accepted.

30.3 Block Configuration

The E2dataFlash consists of 32 bytes x 128 blocks of flash memory in the ECC disabled setting, and 16 bytes x 128 blocks in the ECC enabled setting. Refer to Figure 30.2 for details.

Set the E2FA register to set the E2dataFlash memory address. The memory space of the E2dataFlash is not the same as that of the MCU.

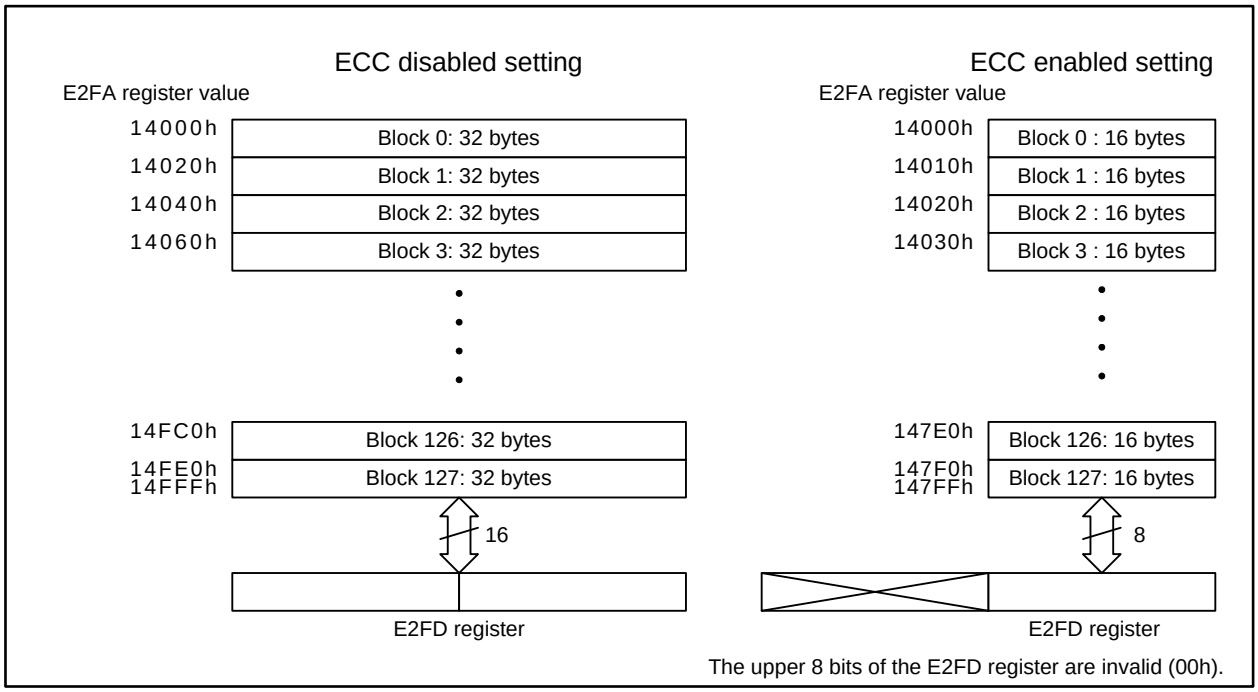
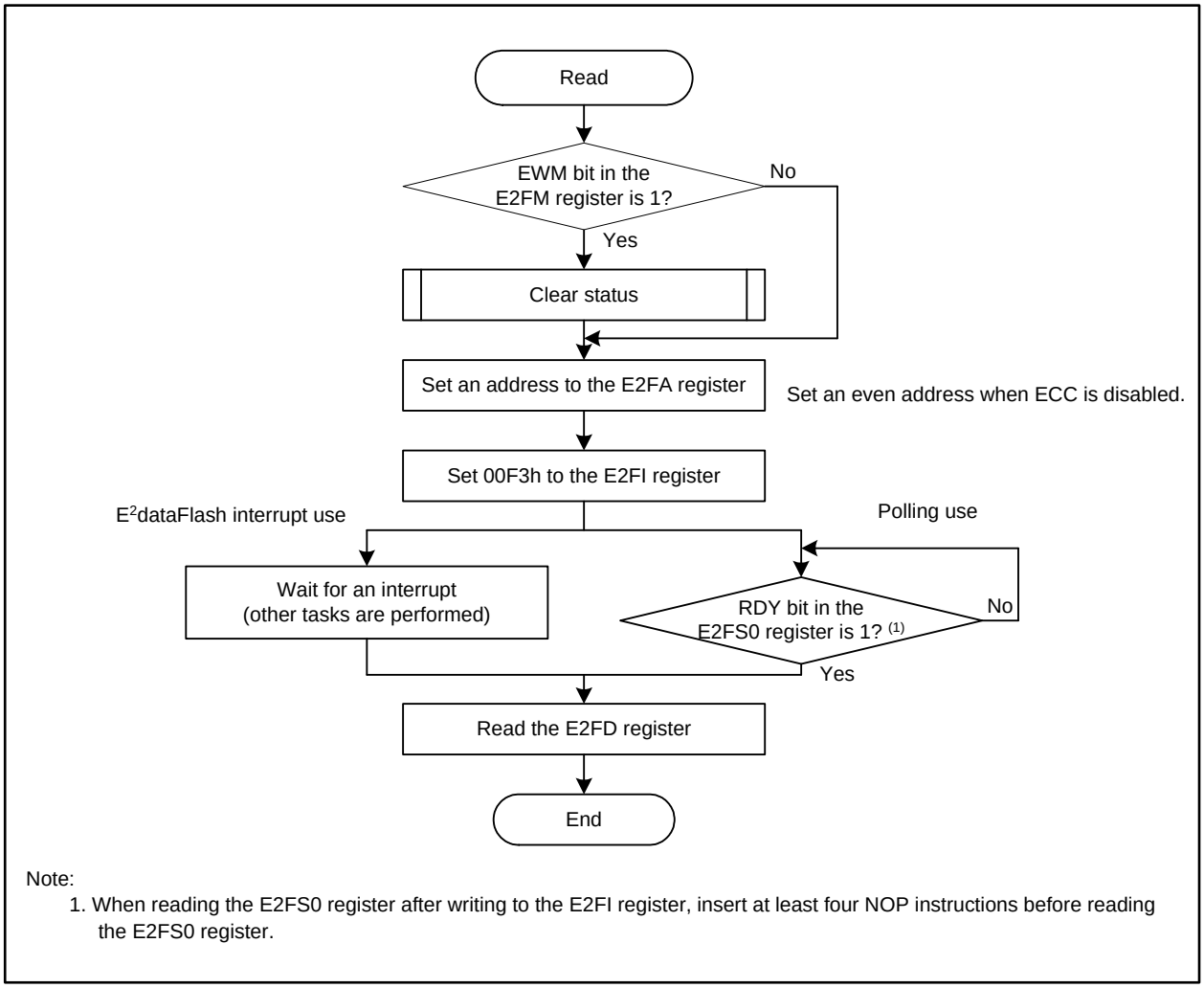


Figure 30.2 E2dataFlash Memory Configuration

30.4 Operational Procedures

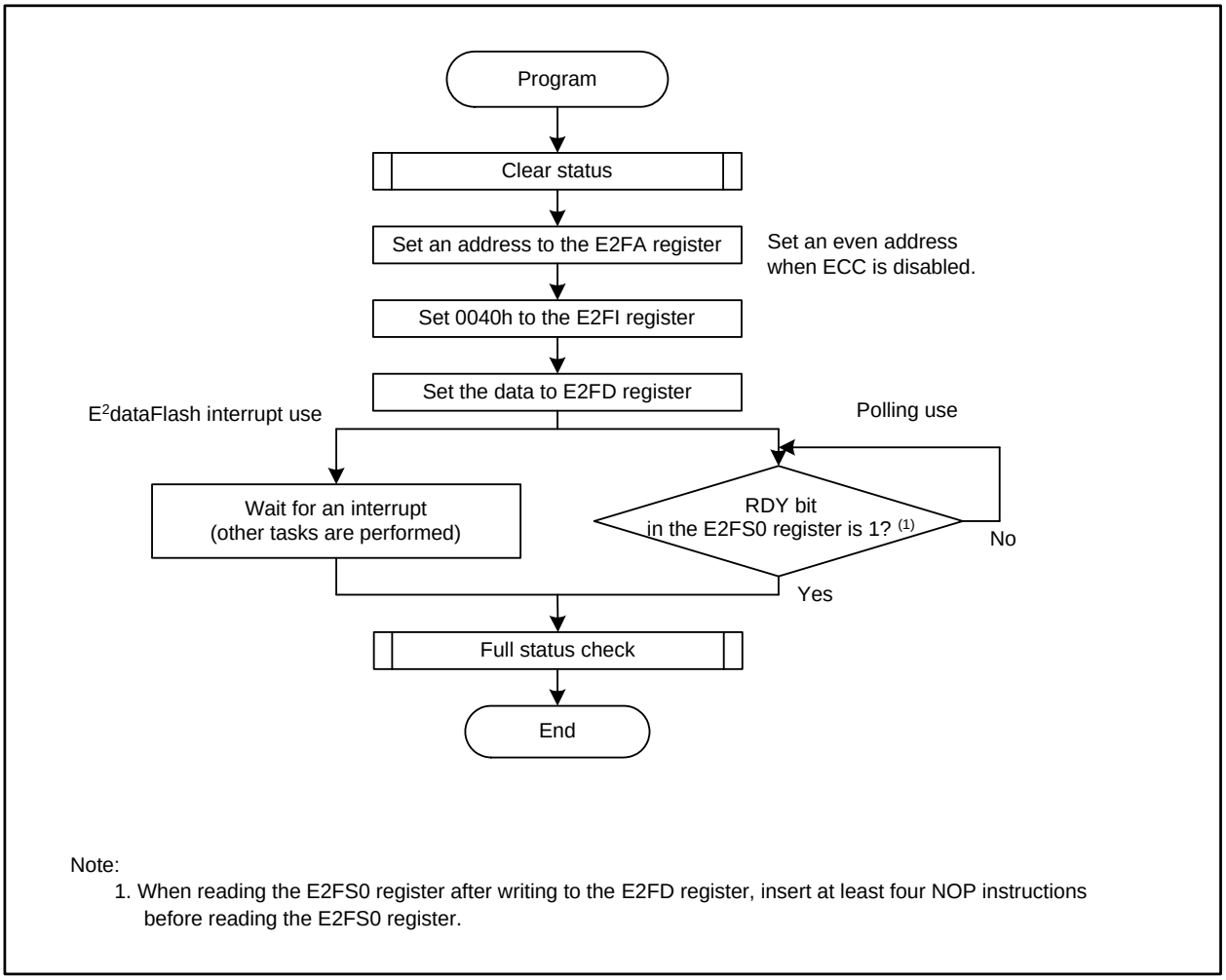
When operating the E2dataFlash, confirm that the RDY bit in the E2FS0 register is 1 (ready), and then execute the read, program, block erase, and clear status operations following the procedures shown in Figure 30.3 to Figure 30.6.

Do not program or erase the E2dataFlash during programming or erasing program ROM 1, program ROM 2, or the data flash. Do not overwrite data to an address that has already been written.



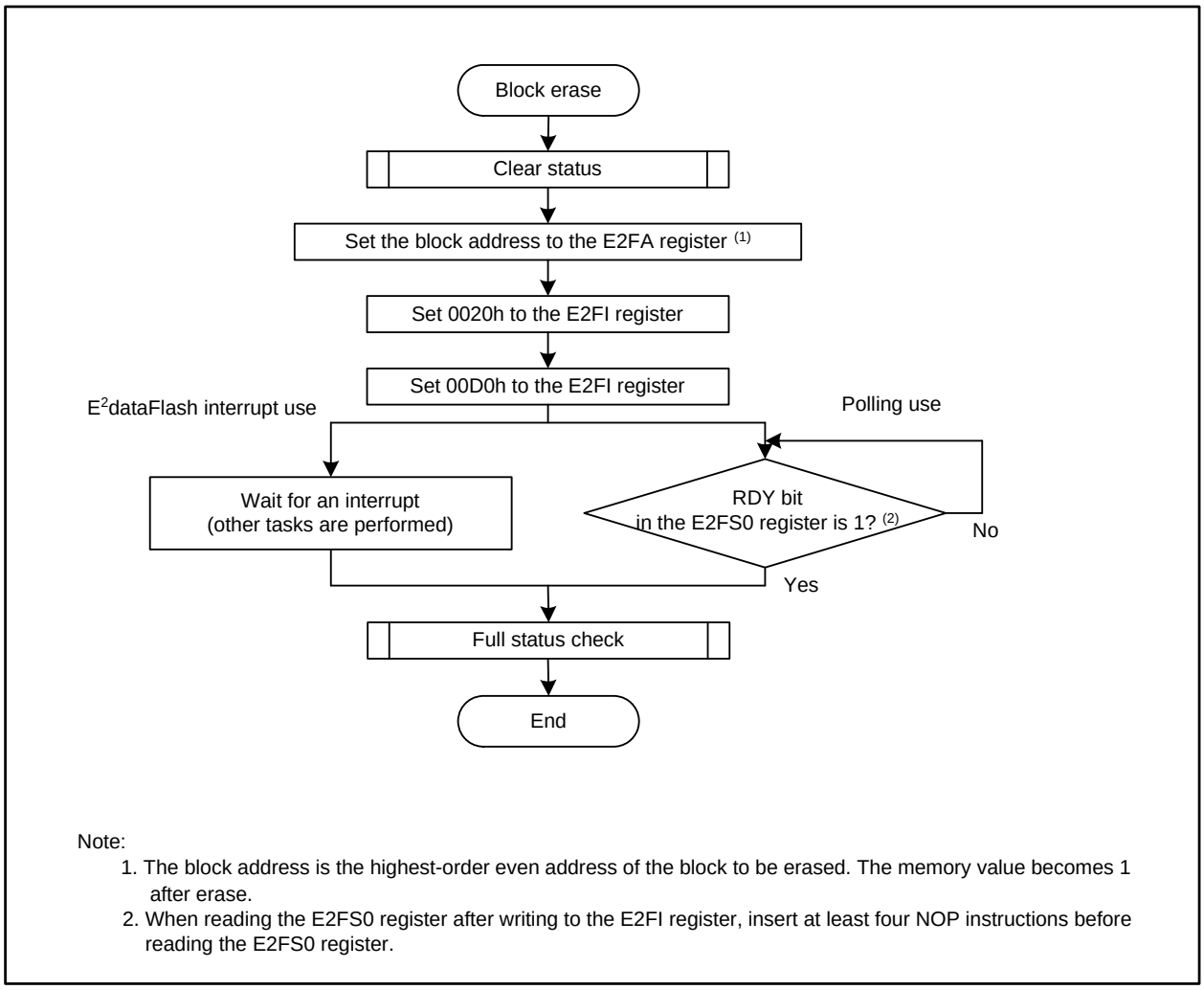
Note:
1. When reading the E2FS0 register after writing to the E2FI register, insert at least four NOP instructions before reading the E2FS0 register.

Figure 30.3 Read Operation Example



Note:
1. When reading the E2FS0 register after writing to the E2FD register, insert at least four NOP instructions before reading the E2FS0 register.

Figure 30.4 Program Operation Example



Note:
1. The block address is the highest-order even address of the block to be erased. The memory value becomes 1 after erase.
2. When reading the E2FS0 register after writing to the E2FI register, insert at least four NOP instructions before reading the E2FS0 register.

Figure 30.5 Block Erase Operation Example

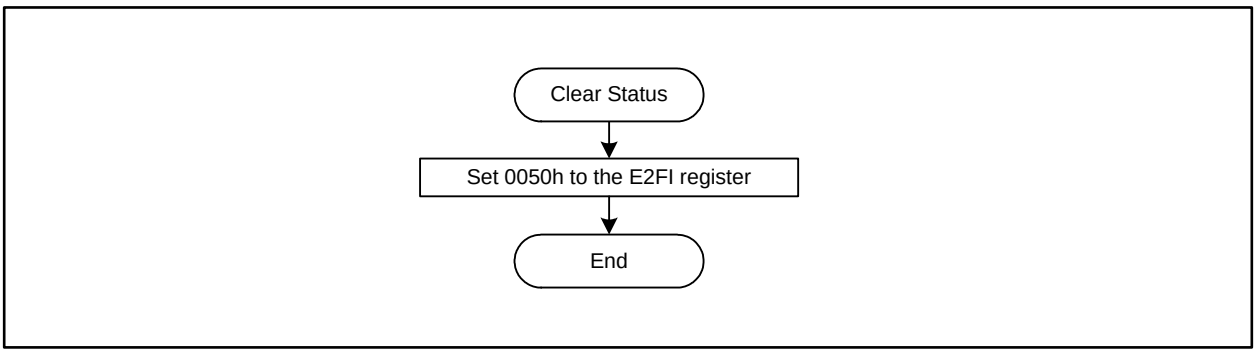


Figure 30.6 Clear Status Operation Example

30.5 Full Status Check

If an error occurs, the WERR or EERR bit in the E2FS0 register becomes 1, indicating the occurrence of an error. Therefore, the execution results can be confirmed by checking the status of these bits (full status check).

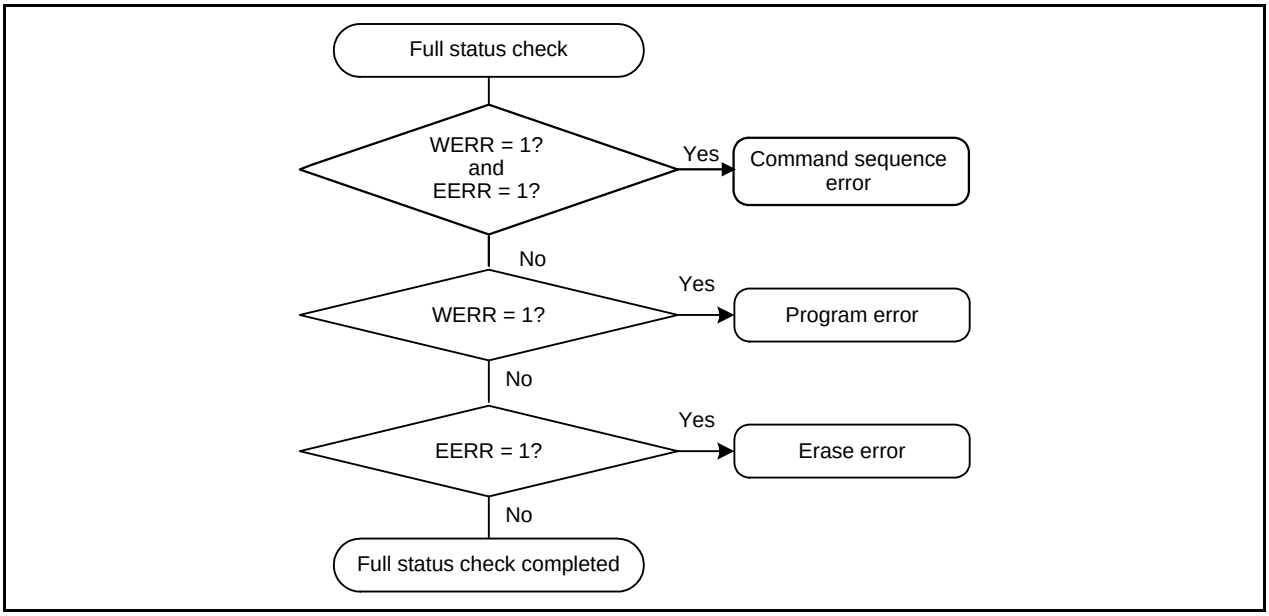


Figure 30.7 Full Status Check

30.5.1 Error Processing Procedures

When errors occur, follow the procedures below.
Do not execute the program command or block erase command when the WERR or EERR bit is 1 (completed in error). Execute each command after executing the clear status register command.

Command sequence error
(1) Execute the clear status register command and set the WERR or EERR bit to 0 (no error).
(2) Check to see that the command is written correctly and execute the command again.

A command sequence error occurs when writing data other than xxD0h and xxFFh in the second bus cycle of the block erase command. When writing xxFFh in the second bus cycle of the block erase command, the E2dataFlash becomes the state before executing the command, and the command code written in the first bus cycle is cancelled.

Erase error
(1) Execute the clear status register command and set the EERR bit to 0 (no erase error).
(2) Execute the block erase command again.
Execute (1) and (2) until an erase error does not occur.
If an error still occurs after executing (1) and (2) three times, do not use that block.

Program error
(1) Execute the clear status register command and set the WERR bit to 0 (no write error).
(2) Execute the block erase command.
(3) Execute the program command.
If an error still occurs, do not use that address.

30.6 Interrupt

An interrupt request is generated when the RDY bit in the E2FS0 register becomes 1 while the RIE bit in the E2FC register is 1 (ready interrupt enabled). Refer to 12.7 “Interrupt Control” for more details on interrupt control.

Table 30.3 E2dataFlash Interrupt Related Register

Address	Register Name	Register Symbol	Reset Value
0041h	E2dataFlash Interrupt Control Register	E2FIC	XXXX X000b

30.7 Notes on E2PROM Emulation Data Flash

30.7.1 Relation with CPU Rewrite Mode

When the FMR01 bit in the FMR0 register is 1 (CPU rewrite mode enabled), do not set the EWM bit in the E2FM register to 1 (erase/program enabled).

30.7.2 CPU Clock When Rewriting

Rewrite the E2dataFlash in high speed mode, medium speed mode, or PLL operating mode, 40 MHz on-chip oscillator mode.

30.7.3 Clock Transition

To change the mode after rewriting the E2dataFlash, follow the steps below.

(a) Transition to wait mode, stop mode, 125 kHz on-chip oscillator low power mode, or low power mode
  (1) Wait until the RDY bit in the E2FS0 register becomes 1 (ready).
  (2) Set the OM bit in the E2FM register to 0 (E2dataFlash stopped).
  (3) Change modes.

(b) Transition to a mode not listed in (a)
  (1) Wait until the RDY bit in the E2FS0 register becomes 1 (ready).
  (2) Change modes.

31. Electrical Characteristics

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31.1 Electrical Characteristics (J-Version, Common to 3 V and 5 V)

31.1.1 Absolute Maximum Rating

Table 31.1 Absolute Maximum Ratings

Symbol	Characteristic		Condition	Rated Value	Unit
V_{CC}	Supply voltage		$V_{CC} = AV_{CC}$	-0.3 to 6.5	V
AV_{CC}	Analog supply voltage		$V_{CC} = AV_{CC}$	-0.3 to 6.5	V
V_{REF}	Analog reference voltage			–0.3 to V_{CC} + 0.1 (1)	V
V_I	Input voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 toP9_7, P10_0 to P10_7 XIN, $\overline{\text{RESET}}$, CNVSS		-0.3 to V_{CC} + 0.3	V
V_O	Output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XOUT		-0.3 to V_{CC} + 0.3	V
P_d	Power consumption		-40°C ≤ T_{opr} ≤ 85°C	300	mW
T_{opr}	Operating temperature range	While CPU operation		-40 to 85	°C
		While flash memory program and erase operation	Programming area	0 to 60	
			Data area	-40 to 85	
T_{stg}	Storage temperature range			-65 to 150	°C

Note:
1. Maximum value is 6.5 V.

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31.1.2 Recommended Operating Conditions

Table 31.2 Operating Conditions (1)

V_{CC} = 3.0 V to 5.5 V, T_{opr} = -40°C to 85°C unless otherwise specified.

Symbol	Characteristic			Standard			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply voltage			3.0		5.5	V
AV_{CC}	Analog supply voltage				V_{CC}		V
V_{SS}	Ground voltage				0		V
AV_{SS}	Analog ground voltage				0		V
V_{IH}	High level input voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7	Input level 0.50 V_{CC}	0.7 V_{CC}		V_{CC}	V
			Input level 0.70 V_{CC}	0.85V_{CC}		V_{CC}	V
		XIN, $\overline{RESET}$, CNVSS		0.8 V_{CC}		V_{CC}	
		SDAMM, SCLMM	When I^2C-bus input level selected	0.7 V_{CC}		V_{CC}	V
			When SMBUS input level selected	2.1		V_{CC}	V
V_{IL}	Low level input voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7	Input level 0.50 V_{CC}	0		0.3 V_{CC}	V
			Input level 0.70 V_{CC}	0		0.45V_{CC}	V
		XIN, $\overline{RESET}$, CNVSS		0		0.2 V_{CC}	V
		SDAMM, SCLMM	When I^2C-bus input level selected	0		0.3 V_{CC}	V
			When SMBUS input level selected	0		0.8	V
$I_{OH(sum)}$	High peak output current	Sum of $I_{OH(peak)}$ at P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6 to P8_7, P9_0 to P9_7, P10_0 to P10_7				-80.0	mA
$I_{OH(peak)}$	High level peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6 to P8_7, P9_0 to P9_7, P10_0 to P10_7				-10.0	mA
$I_{OH(avg)}$	High level average output current (1)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6 to P8_7, P9_0 to P9_7, P10_0 to P10_7				-5.0	mA
$I_{OL(sum)}$	Low peak output current	Sum of $I_{OL(peak)}$ at P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7				80.0	mA
$I_{OL(peak)}$	Low level peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7				10.0	mA
$I_{OL(avg)}$	Low level average output current (1)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7				5.0	mA
$f_{(XIN)}$	Main clock input oscillation frequency (2)			0		20	MHz
$f_{(XCIN)}$	Sub clock oscillation frequency				32.768	50	kHz
$f_{(PLL)}$	PLL clock oscillation frequency (2)			10		32	MHz
$f_{(BCLK)}$	CPU operation frequency			0		32	MHz
$t_{su(PLL)}$	Wait time to stabilize PLL frequency synthesizer					1	ms

Notes:
1. The mean output current is the mean value within 100 ms.
2. Refer to Figure 31.1 “Main clock input oscillation frequency, PLL clock oscillation frequency” for the relationship between main clock oscillation frequency/PLL clock oscillation frequency and supply voltage.

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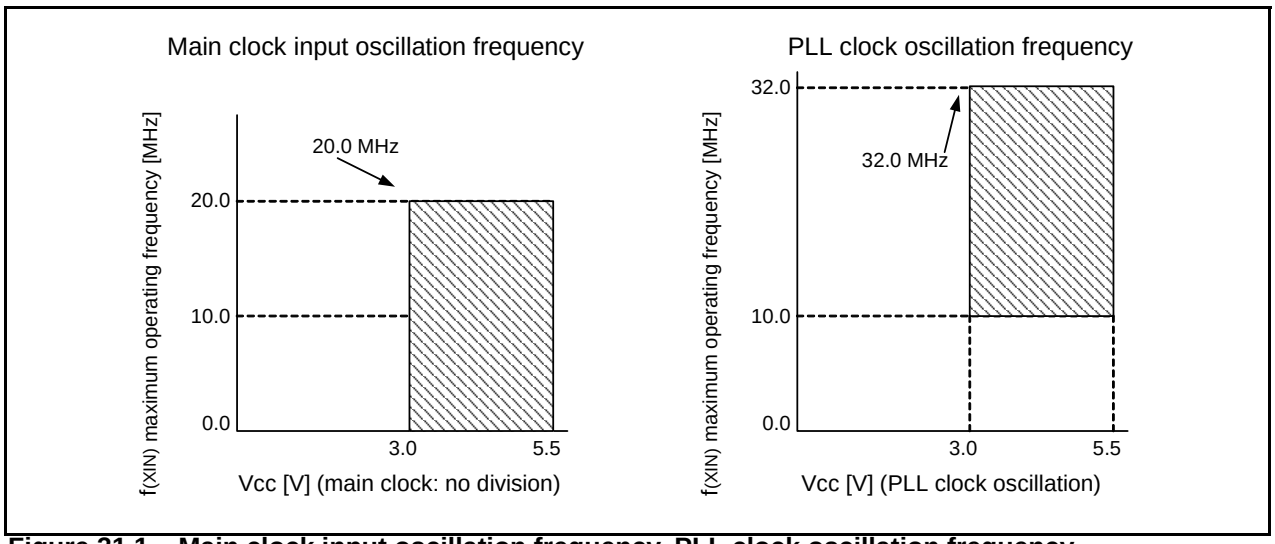

Figure 31.1 Main clock input oscillation frequency, PLL clock oscillation frequency

Table 31.3 Recommended Operating Conditions (2/2) (1)

V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_{opr} = -40°C to 85°C unless otherwise specified.
The ripple voltage must not exceed $V_{r(VCC)}$ and/or $dV_{r(VCC)}/dt$.

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$V_{r(VCC)}$	Allowable ripple voltage	V_{CC} = 5.0 V			0.5	Vp-p
		V_{CC} = 3.0 V			0.3	Vp-p
$dV_{r(VCC)}/dt$	Ripple voltage falling gradient	V_{CC} = 5.0 V			0.3	V/ms
		V_{CC} = 3.0 V			0.3	V/ms

Note:
1. The device is operationally guaranteed under these operating conditions.

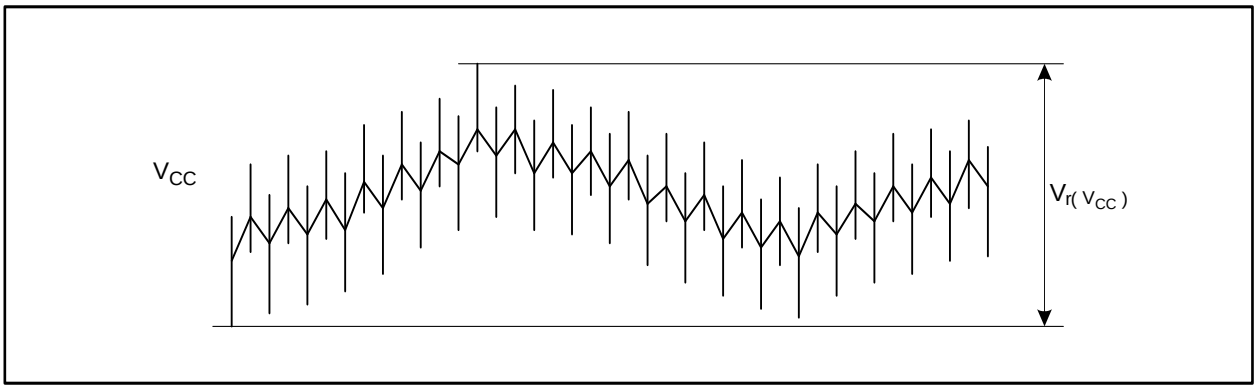

Figure 31.2 Ripple Waveform

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31.1.3 A/D Conversion Characteristics

Table 31.4 A/D Conversion Characteristics (1)

$V_{CC} = AV_{CC} = V_{REF} = 3.0$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V at $T_{opr} = -40°C$ to 85°C unless otherwise specified.

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Resolution	$V_{REF} = V_{CC}$			10	Bits
I_{NL}	Integral non-linearity error	$V_{REF} = V_{CC} = 5.0$ V (2)			±3	LSB
		$V_{REF} = V_{CC} = 3.3$ V (2)			±5	LSB
—	Absolute accuracy	$V_{REF} = V_{CC} = 5.0$ V (2)			±3	LSB
		$V_{REF} = V_{CC} = 3.3$ V (2)			±5	LSB
ϕAD	A/D operating clock frequency	4.0 V ≤ V_{CC} ≤ 5.5 V	2		25	MHz
		3.2 V ≤ V_{CC} ≤ 4.0 V	2		16	MHz
		3.0 V ≤ V_{CC} ≤ 3.2 V	2		10	MHz
—	Tolerance level impedance			3		kΩ
D_{NL}	Differential non-linearity error	See note 2			±1	LSB
—	Offset error	See note 2			±3	LSB
—	Gain error	See note 2			±3	LSB
t_{CONV}	10-bit conversion time	$V_{REF} = V_{CC} = 5$V, ϕAD = 25 MHz	1.60			µs
t_{SAMP}	Sampling time		0.6			µs
V_{REF}	Reference voltage		3.0		V_{CC}	V
V_{IA}	Analog input voltage (3)		0		V_{REF}	V

Notes:
1. Use when $AV_{CC} = V_{CC}$
2. Flash memory rewrite disabled. Except for the analog input pin, set the pins to be measured as input ports and connect them to V_{SS}. See Figure 31.3 “A/D Accuracy Measure Circuit”.
3. When analog input voltage is over reference voltage, the result of A/D conversion is 3FFh.

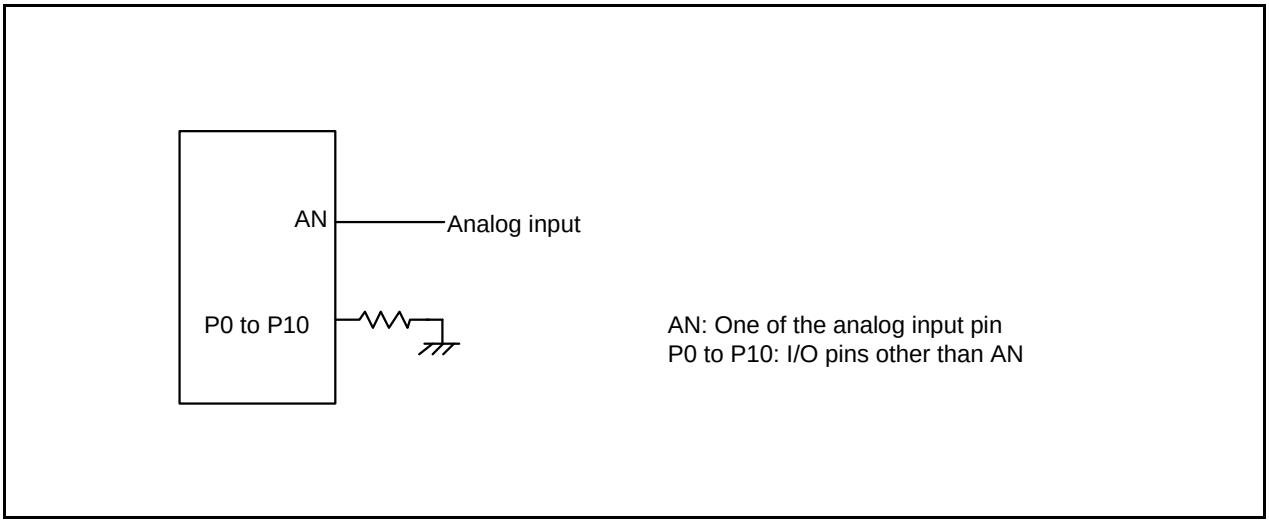

Figure 31.3 A/D Accuracy Measure Circuit

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31.1.4 D/A Conversion Characteristics

Table 31.5 D/A Conversion Characteristics

$V_{CC} = AV_{CC} = V_{REF} = 3.0$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V at $T_{opr} = -40°C$ to 85°C unless otherwise specified.

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute accuracy				2.5	LSB
t_{SU}	Setup time				3	µs
R_O	Output resistance		5	6	8.2	kΩ
I_{VREF}	Reference power supply input current	See Notes 1 and 2			1.5	mA

Notes:
1. This applies when using one D/A converter, with the D/A register for the unused D/A converter set to 00h.
2. The current consumption of the A/D converter is not included. Also, the I_{VREF} of the D/A converter will flow even if the ADSTBY bit in the ADCON1 register is 0 (A/D operation stopped (standby)).

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31.1.5 Flash Memory Electrical Characteristics

Table 31.6 CPU Clock When Operating Flash Memory ($f_{(BCLK)}$)

V_{CC} = 3.0 to 5.5 V at T_{opr} = -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	CPU rewrite mode				16 (1)	MHz
$f_{(SLOW\_R)}$	Slow read mode				5 (3)	MHz
-	Low current consumption read mode			fC	35	kHz
	Data flash read				20 (2)	MHz

Notes:
1. Set the PM17 bit in the PM1 register to 1 (one wait).
2. When the frequency is over this value, set the FMR17 bit in the FMR1 register to 0 (one wait) or the PM17 bit in the PM1 register to 1 (one wait)
3. Set the PM17 bit in the PM1 register to 1 (one wait). When using the 125 kHz on-chip oscillator clock or sub clock as the CPU clock source, a wait is not necessary.

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Table 31.7 Flash Memory (Program ROM 1, 2) Electrical Characteristics

V_{CC} = 3.0 to 5.5 V at T_{opr} = 0°C to 60°C, unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	Program/erase cycles (1, 3, 4)	V_{CC} = 3.3 V, T_{opr} = 25°C	1,000 (2)			times
-	2 words program time	V_{CC} = 3.3 V, T_{opr} = 25°C		150	4000	µs
	Lock bit program time	V_{CC} = 3.3 V, T_{opr} = 25°C		70	3000	µs
-	Block erase time	V_{CC} = 3.3 V, T_{opr} = 25°C		0.2	3.0	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend				$5 + \frac{3}{f(BCLK)}$	ms
-	Interval from erase start/restart until following suspend request		0			µs
-	Suspend interval necessary for auto-erasure to complete (7)		20			ms
-	Time from suspend until erase restart				$30 + \frac{1}{f(BCLK)}$	µs
-	Program, erase voltage		3.0		5.5	V
-	Read voltage	Topr = -40°C to 85°C	3.0		5.5	V
-	Program, erase temperature		0		60	°C
t_{PS}	Flash memory circuit stabilization wait time				50	µs
-	Data hold time (6)	Ambient temperature = 55°C	20			year

Notes:
1. Definition of program and erase cycles:
   The program and erase cycles refer to the number of per-block erasures. If the program and erase cycles are n (n = 1,000), each block can be erased n times. For example, if a 64 KB block is erased after writing 2 word data 16,384 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
2. Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. It is advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact a Renesas Electronics sales office.
6. The data hold time includes time that the power supply is off or the clock is not supplied.
7. After an erase start or erase restart, if an interval of at least 20 ms is not set before the next suspend request, the erase sequence cannot be completed.

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Table 31.8 Flash Memory (Data Flash) Electrical Characteristics

V_{CC} = 3.0 to 5.5 V at T_{opr} = -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	Program/erase cycles (1, 3, 4)	V_{CC} = 3.3 V, T_{opr} = 25°C	10,000 (2)			times
-	2 words program time	V_{CC} = 3.3 V, T_{opr} = 25°C		300	4000	µs
-	Lock bit program time	V_{CC} = 3.3 V, T_{opr} = 25°C		140	3000	µs
-	Block erase time	V_{CC} = 3.3 V, T_{opr} = 25°C		0.2	3.0	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend				$5 + \frac{3}{f(BCLK)}$	ms
-	Interval from erase start/restart until following suspend request		0			µs
-	Suspend interval necessary for auto-erasure to complete (7)		20			ms
-	Time from suspend until erase restart				$30 + \frac{1}{f(BCLK)}$	µs
-	Program, erase voltage		3.0		5.5	V
-	Read voltage		3.0		5.5	V
-	Program, erase temperature		–40		85	°C
t_{PS}	Flash memory circuit stabilization wait time				50	µs
-	Data hold time (6)	Ambient temperature = 55°C	20			year

1. Definition of program and erase cycles
   The program and erase cycles refer to the number of per-block erasures.
   If the program and erase cycles are n (n = 10,000), each block can be erased n times.
   For example, if a 4 KB block is erased after writing 2 word data 1,024 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
2. Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 256 groups before erasing them all in one operation. In addition, averaging the erasure cycles between blocks A and B can further reduce the actual erasure cycles. It is also advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact a Renesas Electronics sales office.
6. The data hold time includes time that the power supply is off or the clock is not supplied.
7. After an erase start or erase restart, if an interval of at least 20 ms is not set before the next suspend request, the erase sequence cannot be completed.

J-Version

31.1.6 E²PROM Emulation Data Flash

Table 31.9 E²PROM Emulation Data Flash Electrical Characteristics

VCC = 3.0 to 5.5 V, VSS = 0 V, and T_{opr} = -40°C to 85°C unless otherwise specified.

Symbol	Characteristic		Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase cycles (1)		100000			times
—	Word program time (2-byte program)			100	2000	µs
—	Read time (2-byte read)				1	µs
—	Block erase time (32-byte block)			15	200	ms
t_{PS}	Flash memory circuit stabilization wait time (sleep mode to normal mode)				50	µs
—	Data hold time (2)	Ambient temperature = 55°C (3, 4)	20			years

Notes:

1. Definition of program/erase cycles definition
   This value represents the number of erasure per block.
   If the flash memory is programmed/erased n times, each block can be erased n times.
   i.e. If a word write is performed in different 16 addresses in a block and then the block is erased, it is considered the programming/erasure is performed just once. However a write in the same address more than once for one erasure is disabled. (overwrite disabled).
2. The data hold time includes the periods when the supply voltage is not applied and no clock is provided.
3. This data hold time includes (7000) hours in Ambient temperature = 85°C.
4. Please contact a Renesas Electronics sales office regarding data retention time other than the above.

J-Version

31.1.7 Voltage Detector and Power Supply Circuit Electrical Characteristics

Table 31.10 Voltage Detector 0 Electrical Characteristics

The measurement condition is V_{CC} = 3.0 to 5.5 V, T_{opr} = -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level V_{det0}	When V_{CC} is falling.	2.70	2.85	3.00	V
$t_{d(E-A)}$	Waiting time until voltage detector operation starts (1)	V_{CC} = 3.0 to 5.0 V			100	µs

Note:
1. Necessary time until the voltage detector operates when setting to 1 again after setting the VC25 bit in the VCR2 register to 0.

Table 31.11 Voltage Detector 2 Electrical Characteristics

The measurement condition is V_{CC} = 3.0 to 5.5 V, T_{opr} = -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet2_0	Voltage detection level Vdet2_0	When V_{CC} is falling		3.21		V
Vdet2_1	Voltage detection level Vdet2_1			3.36		V
Vdet2_2	Voltage detection level Vdet2_2			3.51		V
Vdet2_3	Voltage detection level Vdet2_3			3.66		V
Vdet2_4	Voltage detection level Vdet2_4		3.51	3.81	4.11	V
Vdet2_5	Voltage detection level Vdet2_5			3.96		V
Vdet2_6	Voltage detection level Vdet2_6			4.10		V
Vdet2_7	Voltage detection level Vdet2_7			4.25		V
-	Hysteresis width at the rising of V_{CC} in voltage detector 2			0.15		V
$t_{d(E-A)}$	Waiting time until voltage detector operation starts (1)	V_{CC} = 3.0 to 5.0 V			100	µs

Note:
1. Necessary time until the voltage detector operates after setting to 1 again after setting the VC27 bit in the VCR2 register to 0.

J-Version

Table 31.12 Power-On Reset Circuit

The measurement condition is T_{opr} = -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient		2.0		50000	mV/ms
t_{fth}	External power V_{CC} fall gradient				50000	mV/ms
V_{por}	Voltage at which power-on reset enabled (1)				0.1	V
$t_{w(por)}$	Hold time at which power-on reset enabled		1.0			ms

Note:
1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS1 address to 0.

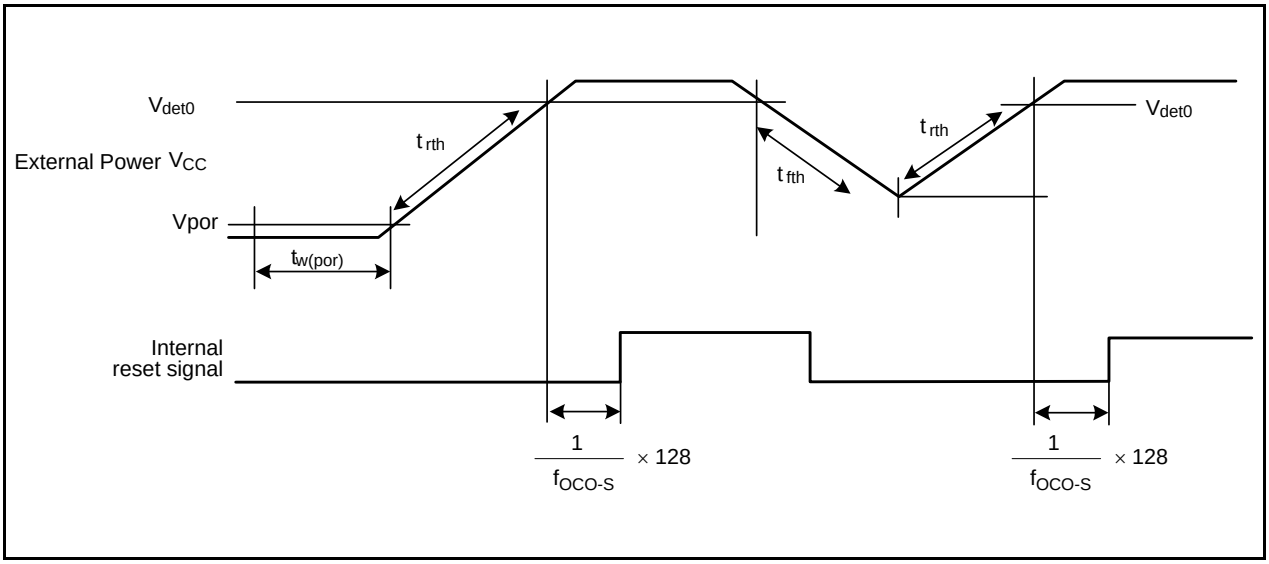


Figure 31.4 Power-On Reset Circuit Electrical Characteristics

Table 31.13 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during powering-on	VCC = 3.0 V to 5.5V			5	ms
$t_{d(R-S)}$	STOP release time				300	µs
$t_{d(W-S)}$	Low power mode wait mode release time				300	µs

Note:
1. When V_{CC} = 5 V.

J-Version

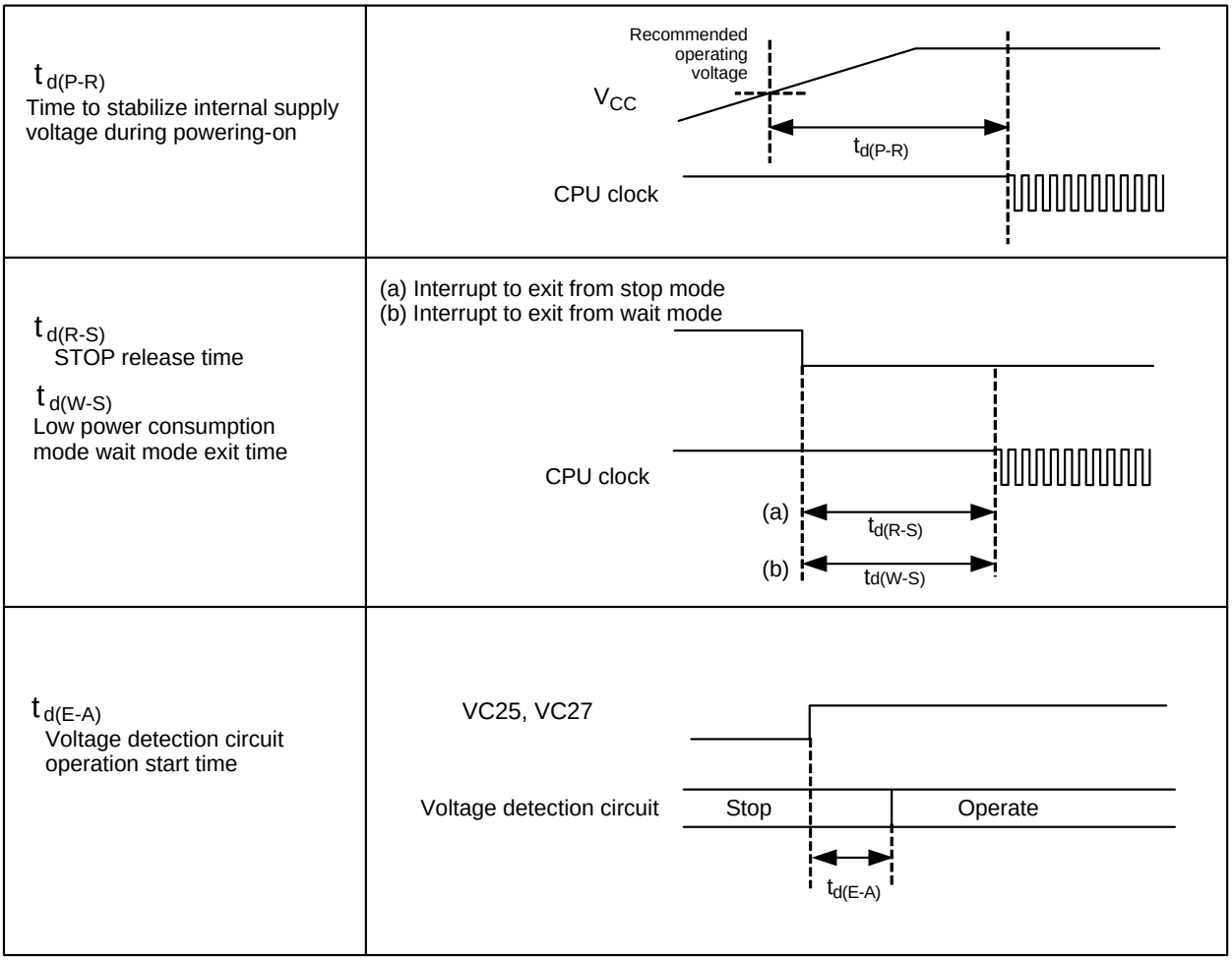


Figure 31.5 Power Supply Circuit Timing Diagram

31.1.8 Oscillator Electrical Characteristics

Table 31.14 On-Chip Oscillator Electrical Characteristics

V_{CC} = 3.0 to 5.5 V, T_{opr} = –40°C to 85°C, unless otherwise specified

Symbol	Characteristic	Standard			Unit
		Min.	Typ.	Max.	
f_{OCO-S}	125 kHz on-chip oscillator oscillation frequency	100	125	150	kHz
f_{OCO40M}	40 MHz on-chip oscillator oscillation frequency	32	40	48	MHz
f_{WDT}	Dedicated 125 kHz on-chip oscillator for the watchdog timer oscillation frequency	100	125	150	kHz

31.2 Electrical Characteristics (J-Version, V_{CC} = 5 V)

31.2.1 Electrical Characteristics

J-Version, V_{CC} = 5 V

Table 31.15 Electrical Characteristics (1)

V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V at T_{opr} = -40°C to 85°C, $f_{(BCLK)}$ = 32 MHz unless otherwise specified.

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	HIGH output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6 to P8_7, P9_0 to P9_7, P10_0 to P10_7	I_{OH}=–5 mA	V_{CC}–2.0		V_{CC}	V
V_{OH}	HIGH output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6 to P8_7,P9_0 to P9_7, P10_0 to P10_7	I_{OH} = –200 µA	V_{CC}–0.3		V_{CC}	V
V_{OH}	HIGH output voltage XOUT	HIGH POWER	I_{OH} = –1 mA	V_{CC}–2.0		V_{CC}	V
		LOW POWER	I_{OH} = –0.5 mA	V_{CC}–2.0		V_{CC}	
	HIGH output voltage XCOUT	HIGH POWER	With no load applied		2.5		V
		LOW POWER	With no load applied		1.6		
V_{OL}	LOW output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7	I_{OL} = 5 mA			2.0	V
V_{OL}	LOW output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7	I_{OL} = 200 µA			0.45	V
V_{OL}	LOW output voltage XOUT	HIGH POWER	I_{OL} = 1 mA			2.0	V
		LOW POWER	I_{OL} = 0.5 mA			2.0	
	LOW output voltage XCOUT	HIGH POWER	With no load applied		0		V
		LOW POWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	TA0IN to TA4IN, TB0IN to TB5IN, $\overline{INT0}$ to $\overline{INT7}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS3}$, SCL2, SDA2, CLK0 to CLK4, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD4, ZP, IDU, IDW, IDV, SD, INPC1_0 to INPC1_7, SSI0, SSCK0, $\overline{SCS0}$, LIN0IN, CRX0, CRX1		0.2		0.4V_{CC}	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$		0.2		2.5	V
V_{T+}-V_{T-}	Hysteresis	XIN		0.2		0.8	V
I_{IH}	HIGH input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$, CNVSS	V_I = 5 V			5.0	µA
I_{IL}	LOW input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$, CNVSS	V_I = 0 V			–5.0	µA
R_{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6 to P8_7, P9_0 to P9_7, P10_0 to P10_7	V_I = 0 V	30	50	170	kΩ
R_{fXIN}	Feedback resistance XIN				1.5		MΩ
R_{fXCIN}	Feedback resistance XCIN				15		MΩ
V_{RAM}	RAM retention voltage		At stop mode	2.0			V

J-Version, V_{CC} = 5 V

Table 31.16 Electrical Characteristics (2)

T_{opr} = –40°C to 85°C unless otherwise specified.

Symbol	Parameter	Measuring Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC} = 4.2V to 5.5 V) In single-chip mode, the output pins are open and other pins are V_{SS}	High speed mode	$f_{(BCLK)}$ = 32 MHz, XIN = 8 MHz (square wave), PLL multiply-by-8 125 kHz on-chip oscillator operating		25	45	mA
			$f_{(BCLK)}$ = 20 MHz, XIN = 20 MHz (square wave), 125 kHz on-chip oscillator operating		21	39	mA
			$f_{(BCLK)}$ = 16 MHz, XIN = 16 MHz (square wave), 125 kHz on-chip oscillator operating		17		mA
		40 MHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator operating 125 kHz on-chip oscillator operating No division		21	39	mA
			Main clock stopped 40 MHz on-chip oscillator operating 125 kHz on-chip oscillator operating Divide-by-8		6		mA
		125 kHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Divide-by-8 FMR22 = FMR23 = 1 (Low-current consumption read mode)		190	580	µA
		Low power mode	$f_{(BCLK)}$ = 32 kHz On Flash memory (2) FMR22 = FMR23 = 1 (Low-current consumption read mode)		200		µA
		Wait mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Peripheral clock operating T_{opr} = 25°C		25		µA
			Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Peripheral clock operating T_{opr} = 85°C		55		µA
		Stop mode	T_{opr} = 25°C		3	15	µA
			T_{opr} = 85°C		30		µA
		During flash memory program	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC} = 5.0 V		20.0		mA
		During flash memory erase	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC} = 5.0 V		30.0		mA
I_{det2}	Low voltage detection dissipation current				3		µA
I_{det0}	Reset area detection dissipation current				6		µA

Note:

1. This indicates the memory in which the program to be executed exists.

J-Version, V_{CC} = 5 V

31.2.2 Timing Requirements (Peripheral Functions and Others)

(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = -40°C to 85°C unless otherwise specified)

31.2.2.1 Reset Input ($\overline{\text{RESET}}$ Input)

Table 31.17 Reset Input ($\overline{\text{RESET}}$ Input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(RSTL)}$	$\overline{\text{RESET}}$ input low pulse width	10		µs

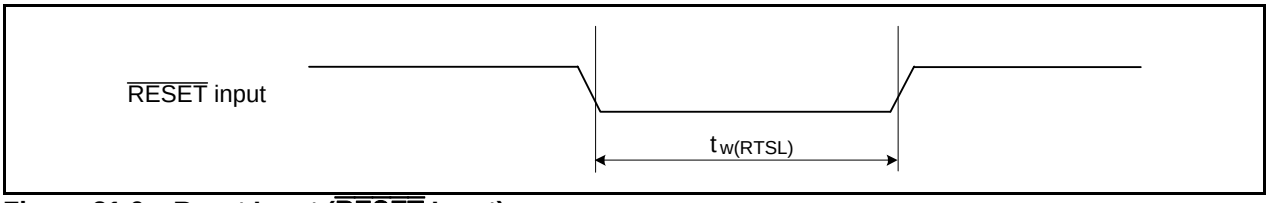


Figure 31.6 Reset Input ($\overline{\text{RESET}}$ Input)

31.2.2.2 External Clock Input

Table 31.18 External Clock Input (XIN Input) (1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	50		ns
$t_{w(H)}$	External clock input high pulse width	20		ns
$t_{w(L)}$	External clock input low pulse width	20		ns
t_r	External clock rise time		9	ns
t_f	External clock fall time		9	ns

Note:
1. The condition is V_{CC} = 5.0V.

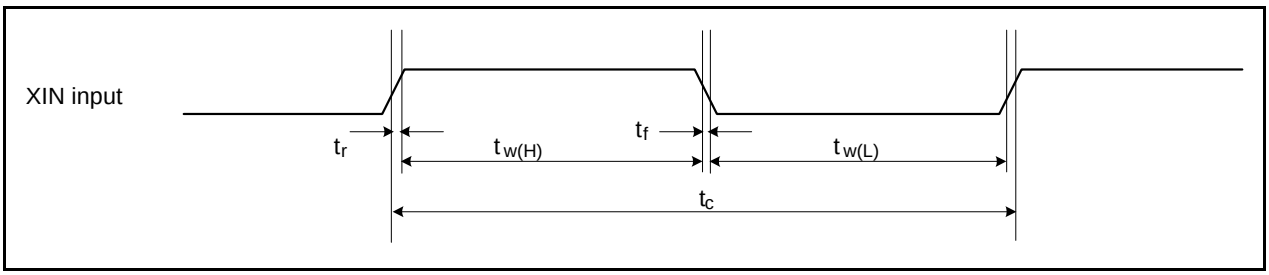


Figure 31.7 External Clock Input (XIN Input)

J-Version, V_{CC} = 5 V

Timing Requirements
(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

31.2.2.3 Timer A Input

Table 31.19 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	100		ns
$t_{w(TAH)}$	TAiIN input high pulse width	40		ns
$t_{w(TAL)}$	TAiIN input low pulse width	40		ns

Table 31.20 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	400		ns
$t_{w(TAH)}$	TAiIN input high pulse width	200		ns
$t_{w(TAL)}$	TAiIN input low pulse width	200		ns

Table 31.21 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	200		ns
$t_{w(TAH)}$	TAiIN input high pulse width	100		ns
$t_{w(TAL)}$	TAiIN input low pulse width	100		ns

Table 31.22 Timer A Input (External Trigger Input in PWM Mode, Programmable Output Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high pulse width	100		ns
$t_{w(TAL)}$	TAiIN input low pulse width	100		ns

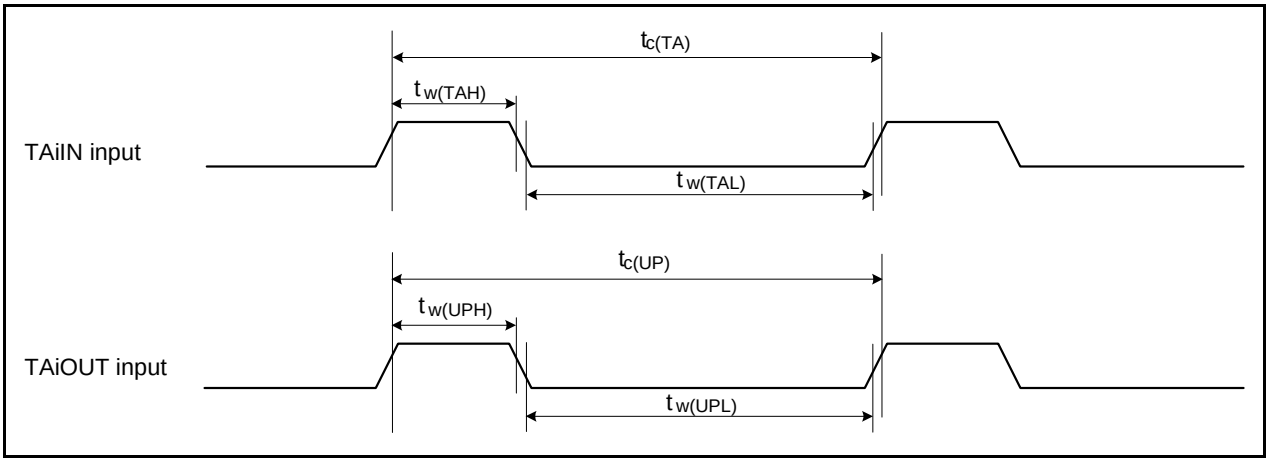


Figure 31.8 Timer A Input

J-Version, V_{CC} = 5 V

Timing Requirements
(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = −40°C to 85°C unless otherwise specified)

Table 31.23 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	800		ns
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	200		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	200		ns

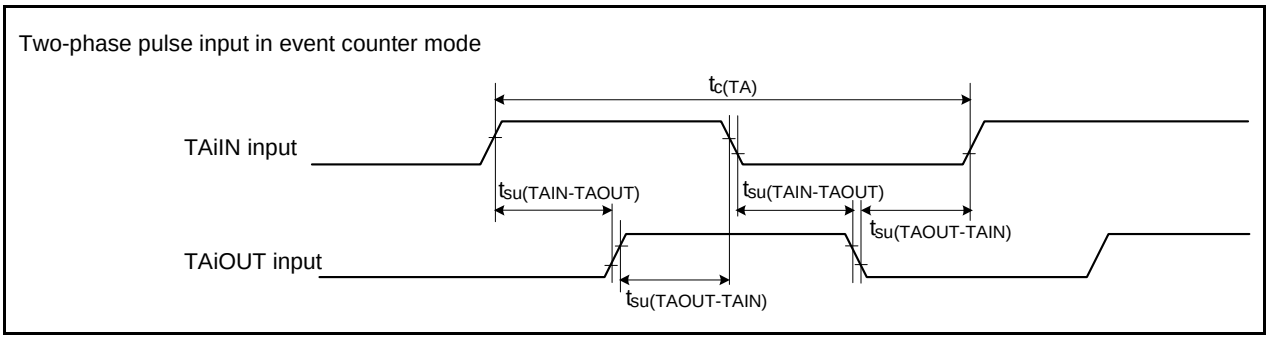


Figure 31.9 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

J-Version, V_{CC} = 5 V

Timing Requirements
(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

31.2.2.4 Timer B Input

Table 31.24 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input low pulse width (counted on both edges)	80		ns

Table 31.25 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high pulse width	200		ns
$t_{w(TBL)}$	TBiIN input low pulse width	200		ns

Table 31.26 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high pulse width	200		ns
$t_{w(TBL)}$	TBiIN input low pulse width	200		ns

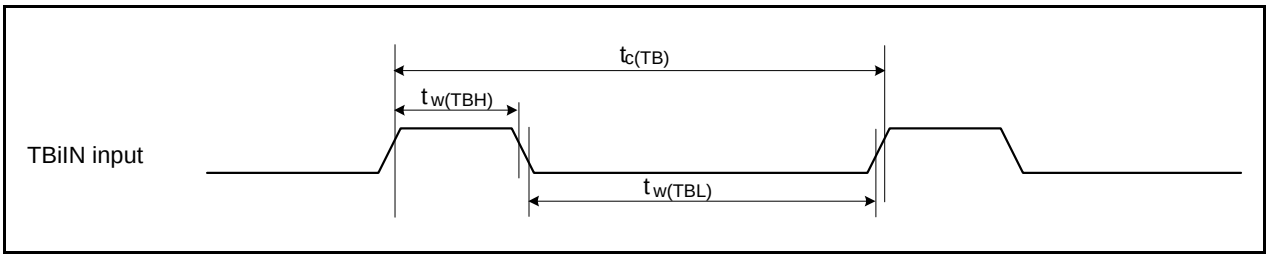


Figure 31.10 Timer B Input

J-Version, V_{CC} = 5 V

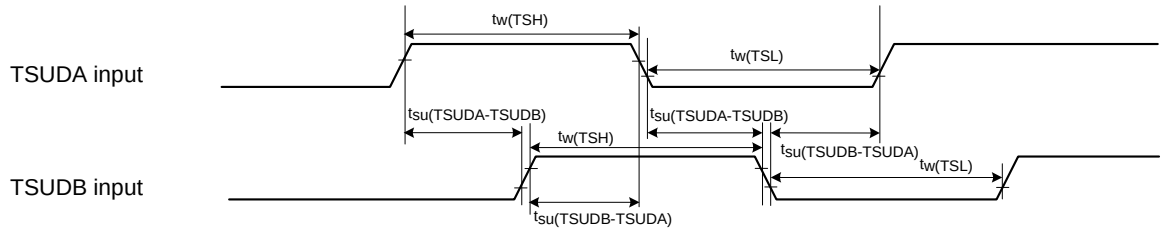
Timing Requirements
(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

31.2.2.5 Timer S Input

Table 31.27 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TSH)}$	TSUDA, TSUDB input high pulse width	2		µs
$t_{w(TSL)}$	TSUDA, TSUDB input low pulse width	2		µs
$t_{su(TSUDA-TSUDB)}$	TSUDB input setup time	1		µs
$t_{su(TSUDB-TSUDA)}$	TSUDA input setup time	1		µs

Two-phase pulse input in two-phase pulse signal processing mode



Note:
1. When the TSUDA and TSUDB phases are interchanged, $t_{su(TSUDA-TSUDB)}$ and $t_{su(TSUDB-TSUDA)}$ are also interchanged.

Figure 31.11 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)

J-Version, V_{CC} = 5 V

Timing Requirements
(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

31.2.2.6 Serial Interface

Table 31.28 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200		ns
$t_{w(CKH)}$	CLKi input high pulse width	100		ns
$t_{w(CKL)}$	CLKi input low pulse width	100		ns
$t_{d(C-Q)}$	TXDi output delay time		80	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	70		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

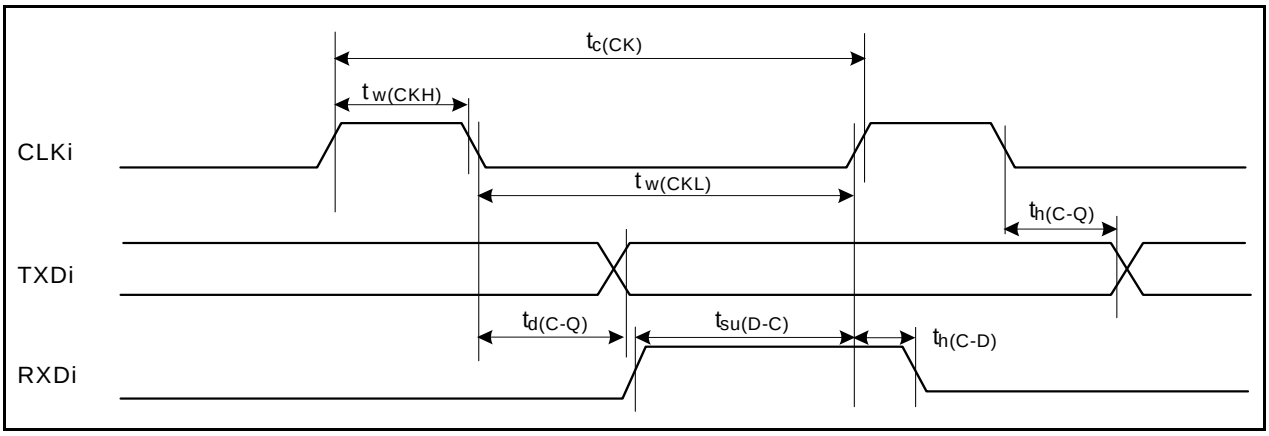


Figure 31.12 Serial Interface

31.2.2.7 External Interrupt $\overline{INTi}$ Input

Table 31.29 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input high pulse width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ input low pulse width	250		ns

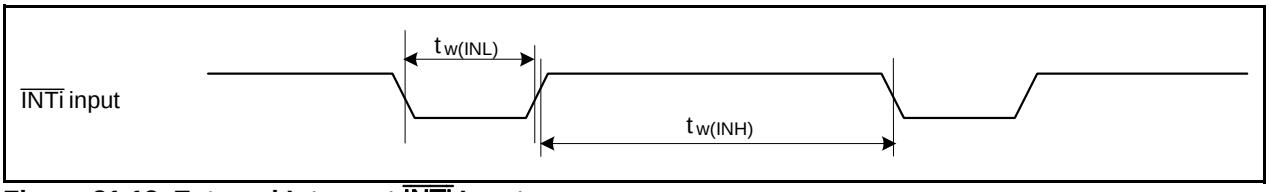


Figure 31.13 External Interrupt $\overline{INTi}$ Input

J-Version, V_{CC} = 5 V

Timing Requirements
(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = −40°C to 85°C unless otherwise specified)

31.2.2.8 Multi-master I²C-bus

Table 31.30 Multi-master I²C-bus

Symbol	Parameter	Standard Clock Mode		Fast-mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		µs
$t_{HD;STA}$	Hold time in start condition	4.0		0.6		µs
t_{LOW}	Hold time in SCL clock 0 status	4.7		1.3		µs
t_R	SCL, SDA signals' rising time		1000	20 + 0.1 Cb	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	µs
t_{HIGH}	Hold time in SCL clock 1 status	4.0		0.6		µs
t_F	SCL, SDA signals' falling time		300	20 + 0.1 Cb	300	ns
$t_{su;DAT}$	Data setup time	250		100		ns
$t_{su;STA}$	Setup time in restart condition	4.7		0.6		µs
$t_{su;STO}$	Stop condition setup time	4.0		0.6		µs

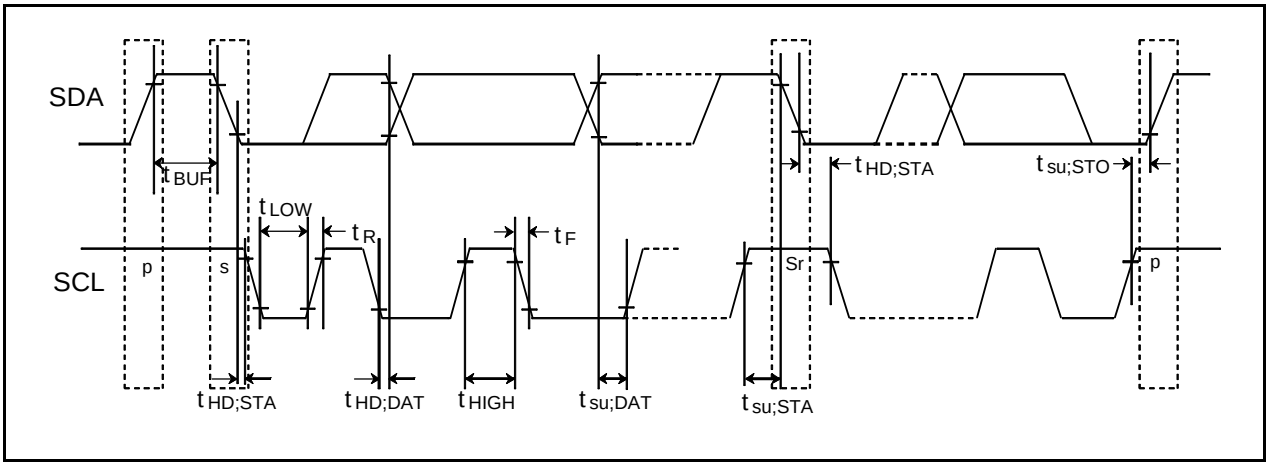


Figure 31.14 Multi-master I²C-bus

J-Version, V_{CC} = 5 V

Timing Requirements
(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = −40°C to 85°C unless otherwise specified)

31.2.2.9 Serial bus interface

Table 31.31 Serial Bus Interface

Symbol	Characteristic		Measurement condition	Standard			Unit
				Min.	Typ.	Max.	
$t_{c(SSCK)}$	SSCK clock cycle time			250			ns
$t_{w(SSCKH)}$	SSCK clock high pulse width			0.4		0.6	$t_{c(SSCK)}$
$t_{w(SSCKL)}$	SSCK clock low pulse width			0.4		0.6	$t_{c(SSCK)}$
$t_{r(SSCK)}$	SSCK clock rising time	Master				1	t_{CYC} (1)
		Slave				1	µs
$t_{f(SSCK)}$	SSCK clock falling time	Master				1	t_{CYC} (1)
		Slave				1	µs
$t_{su(SSIO-SSCK)}$	SSO, SSI data input setup time			100			ns
$t_{h(SSCK-SSIO)}$	SSO, SSI data input hold time			1			t_{CYC} (1)
$t_{su(SCS-SSCK)}$	$\overline{SCS}$ setup time	Slave		1 t_{CYC} + 50 (1)			ns
$t_{h(SSCK-SCS)}$	$\overline{SCS}$ hold time	Slave		1 t_{CYC} + 50 (1)			ns
$t_{d(SSCK-SSIO)}$	SSO, SSI data output delay time	Master				1	t_{CYC} (1)
		Slave				80	ns
$t_{en(SCS-SSI)}$	SSI output enable time		3.0 V ≤ V_{CC} ≤ 5.5 V			1.5 t_{CYC} + 100 (1)	ns
$t_{dis(SCS-SSI)}$	SSI output disable time		3.0 V ≤ V_{CC} ≤ 5.5 V			1.5 t_{CYC} + 100 (1)	ns

Note:
1. 1 t_{CYC} is 1/f1 (s).

J-Version, V_{CC} = 5 V

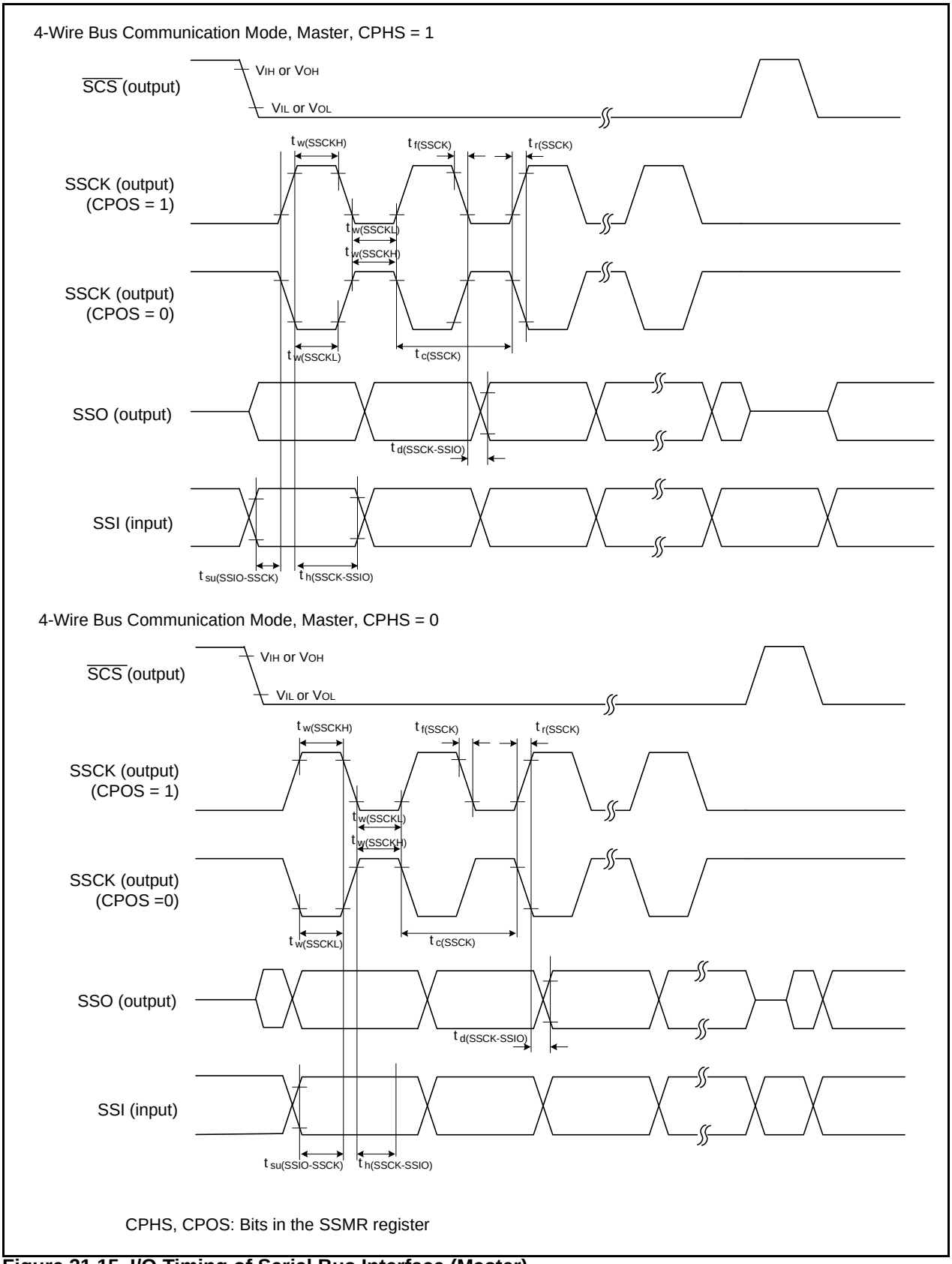


Figure 31.15 I/O Timing of Serial Bus Interface (Master)

J-Version, V_{CC} = 5 V

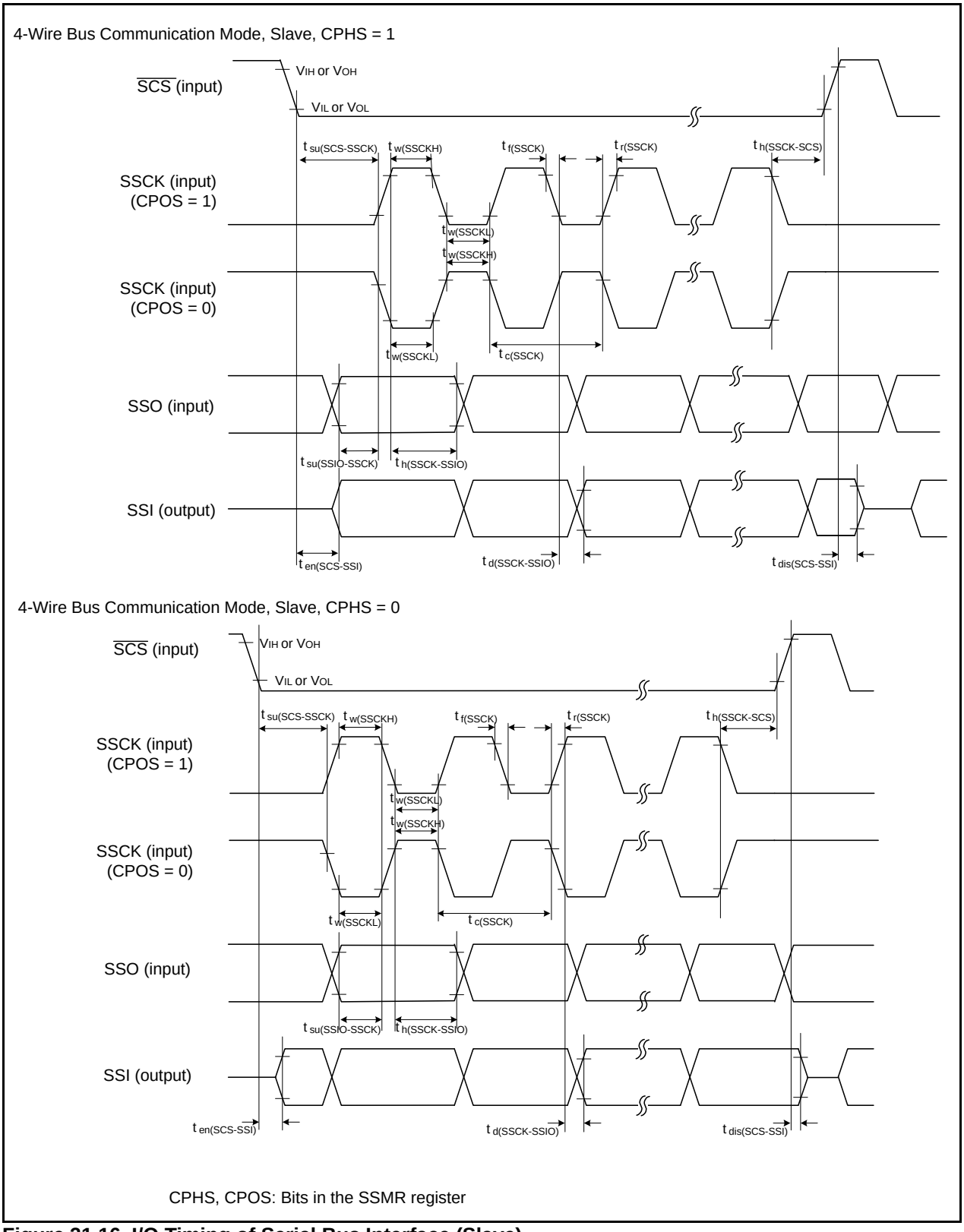


Figure 31.16 I/O Timing of Serial Bus Interface (Slave)

J-Version, V_{CC} = 5 V

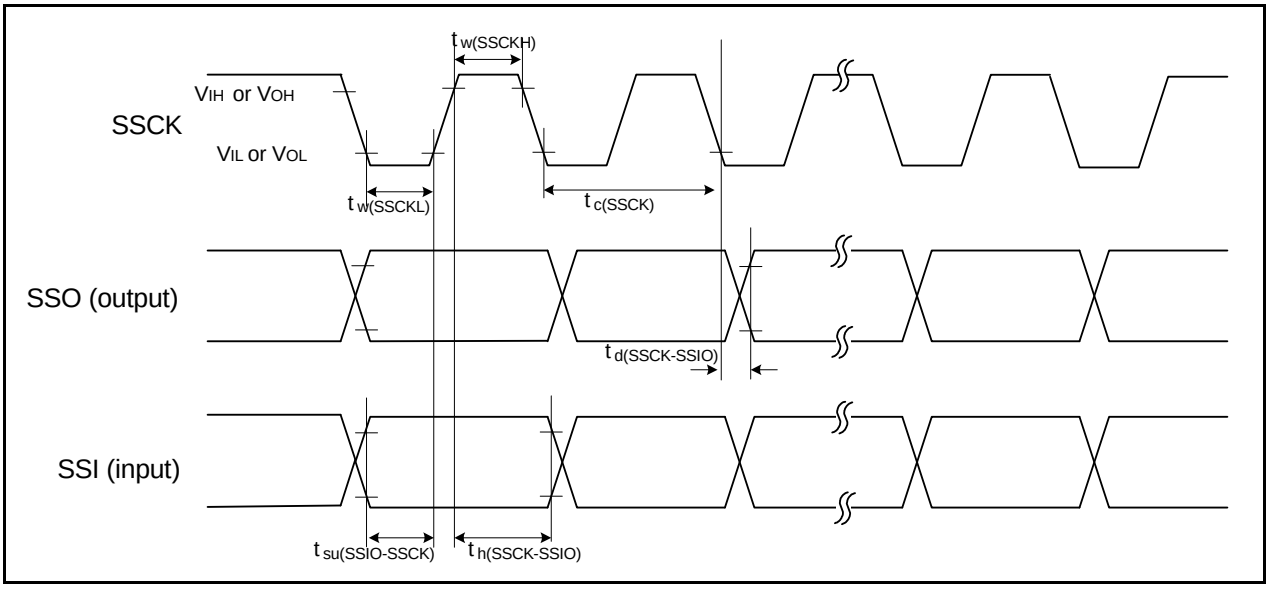


Figure 31.17 I/O Timing of Serial Bus Interface (Synchronous Communication Mode)

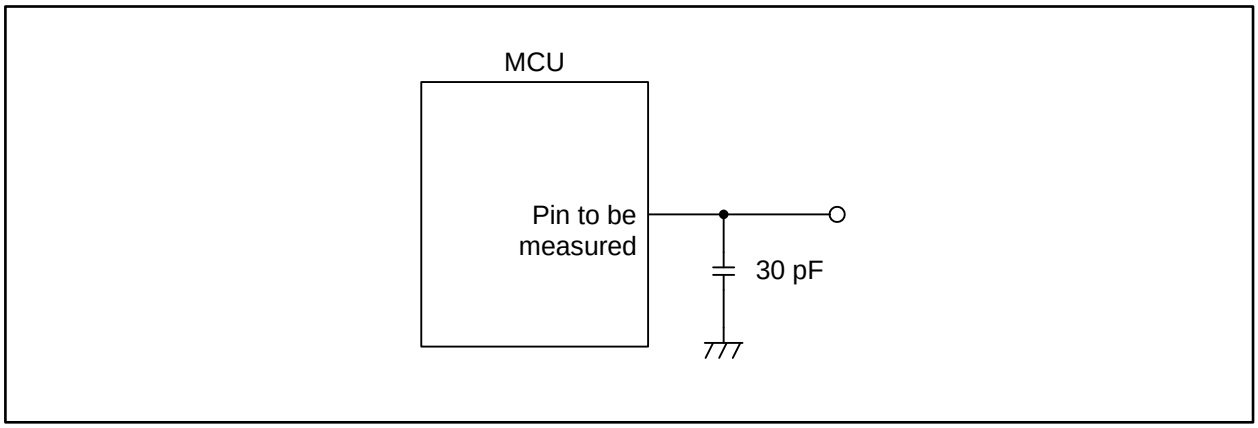


Figure 31.18 Switching Characteristic Measurement Circuit

31.3 Electrical Characteristics (J-Version, V_{CC} = 3 V)

31.3.1 Electrical Characteristics

J-Version, V_{CC} = 3 V

Table 31.32 Electrical Characteristics (1)

V_{CC} = 3.0 to 3.6 V, V_{SS} = 0 V at T_{opr} = −40°C to 85°C, $f_{(BCLK)}$= 32 MHz unless otherwise specified.

Symbol	Parameter			Measuring Condition	Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	HIGH output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6 to P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OH} = −1 mA	V_{CC}−0.5		V_{CC}	V
V_{OH}	HIGH output voltage XOUT		HIGH POWER	I_{OH} = −0.1 mA	V_{CC}−0.5		V_{CC}	V
			LOW POWER	I_{OH} = −50 µA	V_{CC}−0.5		V_{CC}	
	HIGH output voltage XCOUT		HIGH POWER	With no load applied		2.5		V
			LOW POWER	With no load applied		1.6		
V_{OL}	LOW output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OL} = 1mA			0.5	V
V_{OL}	LOW output voltage XOUT		HIGH POWER	I_{OL} = 0.1mA			0.5	V
			LOW POWER	I_{OL} = 50µA			0.5	
	LOW output voltage XCOUT		HIGH POWER	With no load applied		0		V
			LOW POWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	TA0IN to TA4IN, TB0IN to TB5IN, $\overline{INT0}$ to $\overline{INT7}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS3}$, SCL2, SDA2, CLK0 to CLK4, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD4, ZP, IDU, IDW, IDV, SD, INPC1_0 to INPC1_7, SSI0, SSCK0, $\overline{SCS0}$, LIN0IN, CRX0, CRX1					0.4V_{CC}	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$					1.8	V
V_{T+}-V_{T-}	Hysteresis	XIN					0.8	V
I_{IH}	HIGH input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$, CNVSS		V_I = 3V			4.0	µA
I_{IL}	LOW input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$, CNVSS		V_I = 0V			−4.0	µA
R_{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6 to P8_7, P9_0 to P9_7, P10_0 to P10_7		V_I = 0V	50	100	500	kΩ
R_{fXIN}	Feedback resistance XIN					3.0		MΩ
R_{fXCIN}	Feedback resistance XCIN					25		MΩ
V_{RAM}	RAM retention voltage			At stop mode	2.0			V

J-Version, V_{CC} = 3 V

Table 31.33 Electrical Characteristics (2)

Topr = –40°C to 85°C unless otherwise specified.

Symbol	Parameter	Measuring Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC} = 3.0 V to 3.6 V) In single-chip mode, the output pins are open and other pins are VSS	High speed mode	$f_{(BCLK)}$ = 32 MHz, XIN = 8 MHz (square wave), PLL multiply-by-8 125 kHz on-chip oscillator operating		23	43	mA
			$f_{(BCLK)}$ = 20 MHz, XIN = 20 MHz (square wave), 125 kHz on-chip oscillator operating		20	38	mA
			$f_{(BCLK)}$ = 16 MHz, XIN = 16 MHz (square wave), 125 kHz on-chip oscillator operating		16		mA
		40 MHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator operating 125 kHz on-chip oscillator operating No division		20	38	mA
			Main clock stopped 40 MHz on-chip oscillator operating 125 kHz on-chip oscillator operating Divide-by-8		6		mA
		125 kHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Divide-by-8 FMR22 = FMR23 = 1 (Low-current consumption read mode)		190	580	µA
		Low power mode	$f_{(BCLK)}$ = 32 kHz On Flash memory (1) FMR22 = FMR23 = 1 (Low-current consumption read mode)		200		µA
		Wait mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Peripheral clock operating Topr = 25°C		25		µA
			Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Peripheral clock operating T_{opr} = 85°C		55		µA
		Stop mode	T_{opr} = 25°C		2	12	µA
			T_{opr} = 85°C		30		µA
		During flash memory program	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC} = 3.0 V		20.0		mA
		During flash memory erase	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC} = 3.0 V		30.0		mA
I_{det2}	Low voltage detection dissipation current				3		µA
I_{det0}	Reset area detection dissipation current				6		µA

Note:

1. This indicates the memory in which the program to be executed exists.

J-Version, V_{CC} = 3 V

31.3.2 Timing Requirements (Peripheral Functions and Others)

(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = −40°C to 85°C unless otherwise specified)

31.3.2.1 Reset Input ($\overline{\text{RESET}}$ Input)

Table 31.34 Reset Input ($\overline{\text{RESET}}$ Input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(RSTL)}$	$\overline{\text{RESET}}$ input low pulse width	10		µs

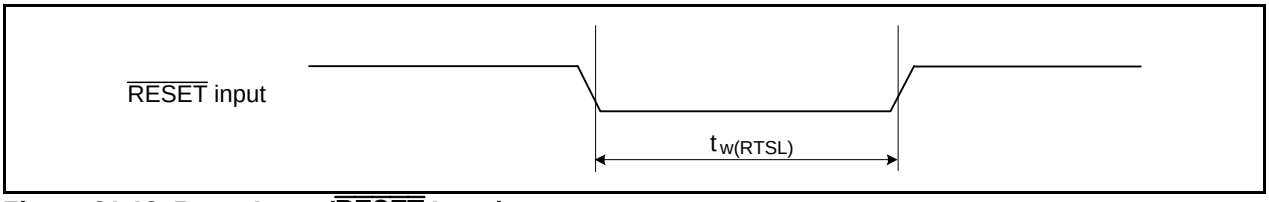


Figure 31.19 Reset Input ($\overline{\text{RESET}}$ Input)

31.3.2.2 External Clock Input

Table 31.35 External Clock Input (XIN input) (1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	50		ns
$t_{w(H)}$	External clock input high pulse width	20		ns
$t_{w(L)}$	External clock input low pulse width	20		ns
t_r	External clock rise time		9	ns
t_f	External clock fall time		9	ns

Note:
1. The condition is V_{CC} = 3.0V.

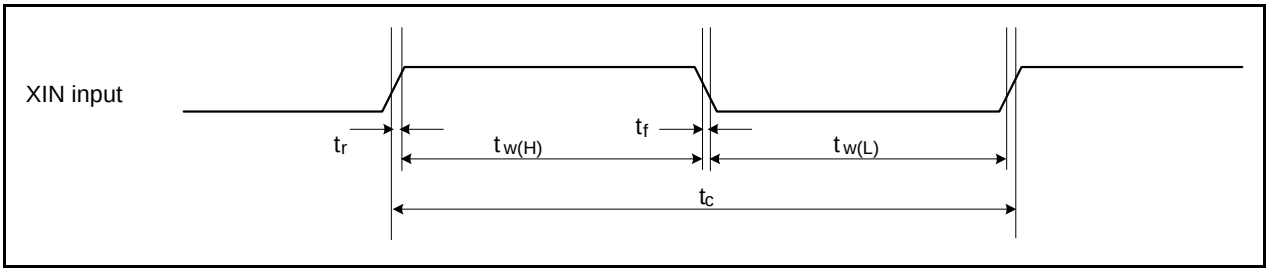


Figure 31.20 External Clock Input (XIN Input)

J-Version, V_{CC} = 3 V

Timing Requirements
(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

31.3.2.3 Timer A Input

Table 31.36 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	150		ns
$t_{w(TAH)}$	TAiIN input high pulse width	60		ns
$t_{w(TAL)}$	TAiIN input low pulse width	60		ns

Table 31.37 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	600		ns
$t_{w(TAH)}$	TAiIN input high pulse width	300		ns
$t_{w(TAL)}$	TAiIN input low pulse width	300		ns

Table 31.38 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	300		ns
$t_{w(TAH)}$	TAiIN input high pulse width	150		ns
$t_{w(TAL)}$	TAiIN input low pulse width	150		ns

Table 31.39 Timer A Input (External Trigger Input in PWM Mode, Programmable Output Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high pulse width	150		ns
$t_{w(TAL)}$	TAiIN input low pulse width	150		ns

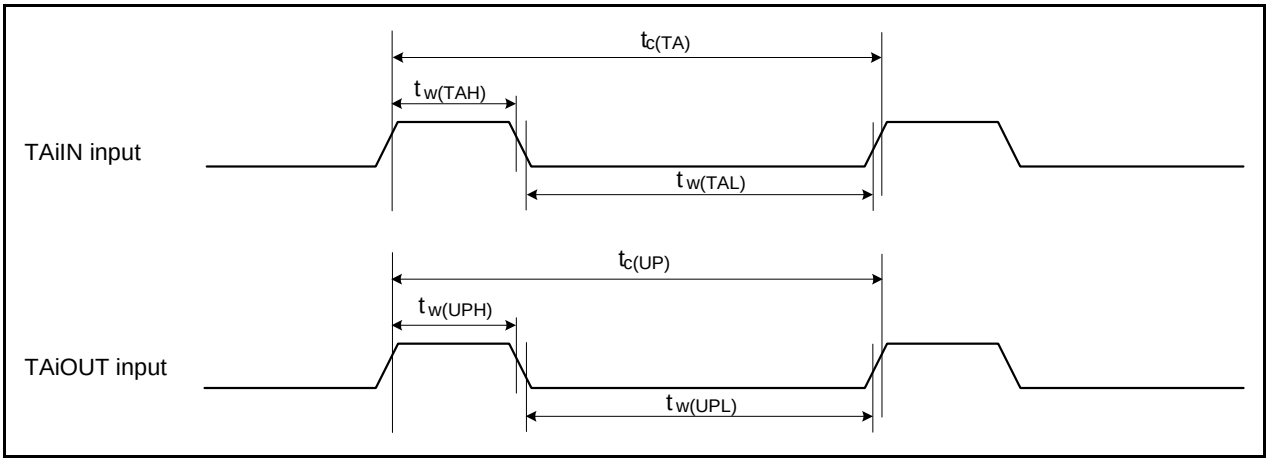


Figure 31.21 Timer A Input

J-Version, V_{CC} = 3 V

Timing Requirements
(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

Table 31.40 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	2		µs
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	500		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	500		ns

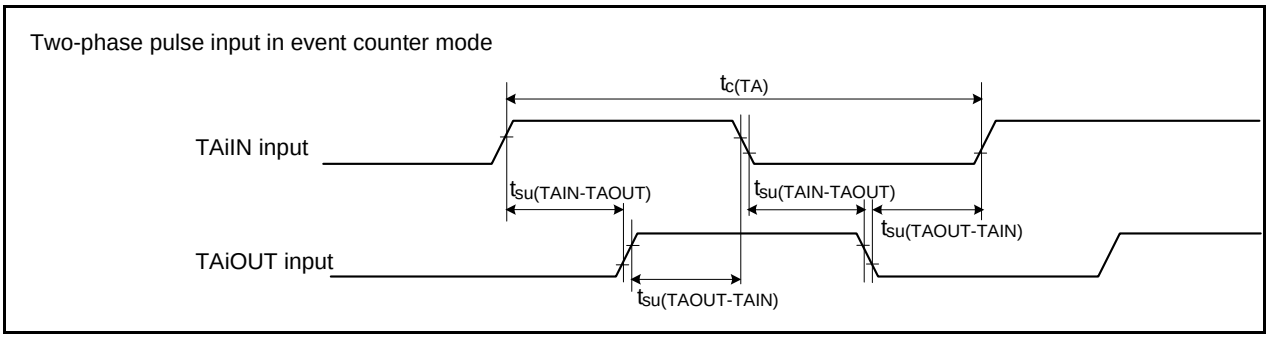


Figure 31.22 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

J-Version, V_{CC} = 3 V

Timing Requirements
(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

31.3.2.4 Timer B Input

Table 31.41 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on one edge)	60		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on both edges)	120		ns
$t_{w(TBL)}$	TBiIN Input low pulse width (counted on both edges)	120		ns

Table 31.42 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input high pulse width	300		ns
$t_{w(TBL)}$	TBiIN input low pulse width	300		ns

Table 31.43 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input high pulse width	300		ns
$t_{w(TBL)}$	TBiIN input low pulse width	300		ns

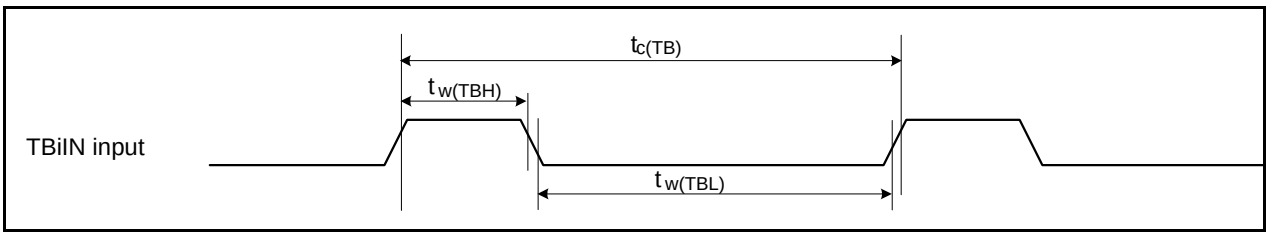


Figure 31.23 Timer B Input

J-Version, V_{CC} = 3 V

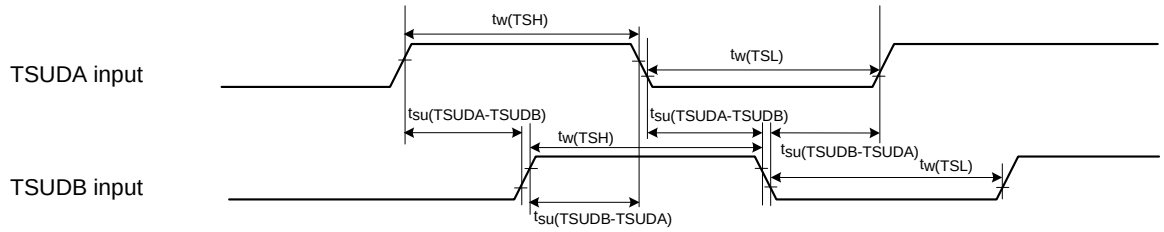
Timing Requirements
(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

31.3.2.5 Timer S Input

Table 31.44 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TSH)}$	TSUDA, TSUDB input high pulse width	2		µs
$t_{w(TSL)}$	TSUDA, TSUDB input low pulse width	2		µs
$t_{su(TSUDA-TSUDB)}$	TSUDB input setup time	1		µs
$t_{su(TSUDB-TSUDA)}$	TSUDA input setup time	1		µs

Two-phase pulse input in two-phase pulse signal processing mode



Note:
1. When the TSUDA and TSUDB phases are interchanged, $t_{su(TSUDA-TSUDB)}$ and $t_{su(TSUDB-TSUDA)}$ are also interchanged.

Figure 31.24 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)

J-Version, V_{CC} = 3 V

Timing Requirements
(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

31.3.2.6 Serial Interface

Table 31.45 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300		ns
$t_{w(CKH)}$	CLKi input high pulse width	150		ns
$t_{w(CKL)}$	CLKi input low pulse width	150		ns
$t_{d(C-Q)}$	TXDi output delay time		160	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	100		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

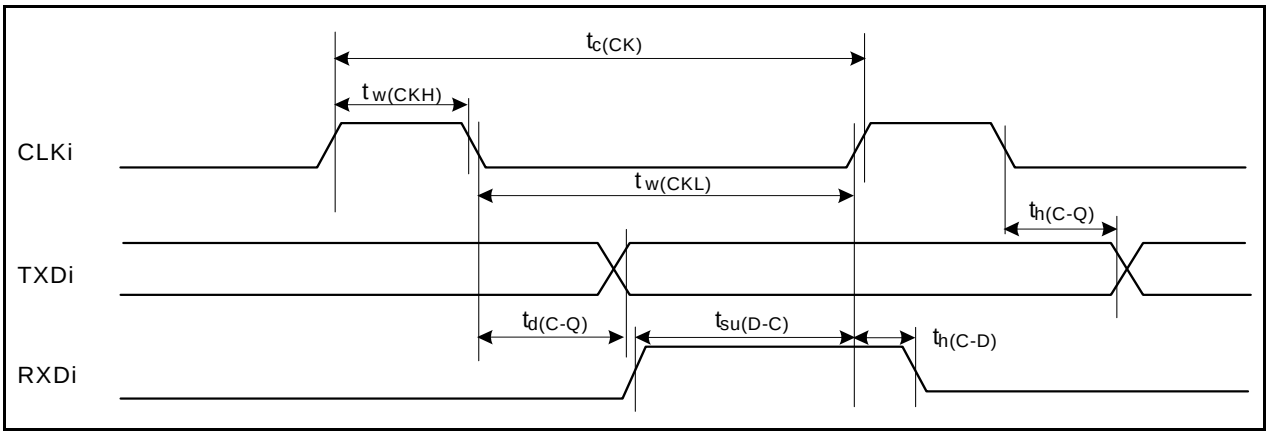


Figure 31.25 Serial Interface

31.3.2.7 External Interrupt $\overline{INTi}$ Input

Table 31.46 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input HIGH Pulse Width	380		ns
$t_{w(INL)}$	$\overline{INTi}$ Input LOW Pulse Width	380		ns

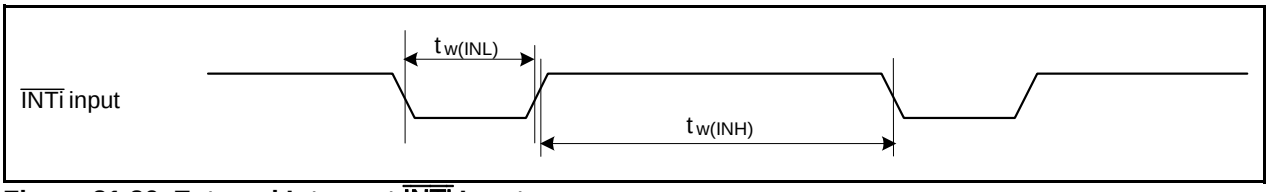


Figure 31.26 External Interrupt $\overline{INTi}$ Input

J-Version, V_{CC} = 3 V

Timing Requirements
(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

31.3.2.8 Multi-master I²C-bus

Table 31.47 Multi-master I²C-bus

Symbol	Parameter	Standard Clock Mode		Fast-mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		µs
$t_{HD;STA}$	Hold time in start condition	4.0		0.6		µs
t_{LOW}	Hold time in SCL clock 0 status	4.7		1.3		µs
t_R	SCL, SDA signals' rising time		1000	20 + 0.1 Cb	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	µs
t_{HIGH}	Hold time in SCL clock 1 status	4.0		0.6		µs
t_F	SCL, SDA signals' falling time		300	20 + 0.1 Cb	300	ns
$t_{su;DAT}$	Data setup time	250		100		ns
$t_{su;STA}$	Setup time in restart condition	4.7		0.6		µs
$t_{su;STO}$	Stop condition setup time	4.0		0.6		µs

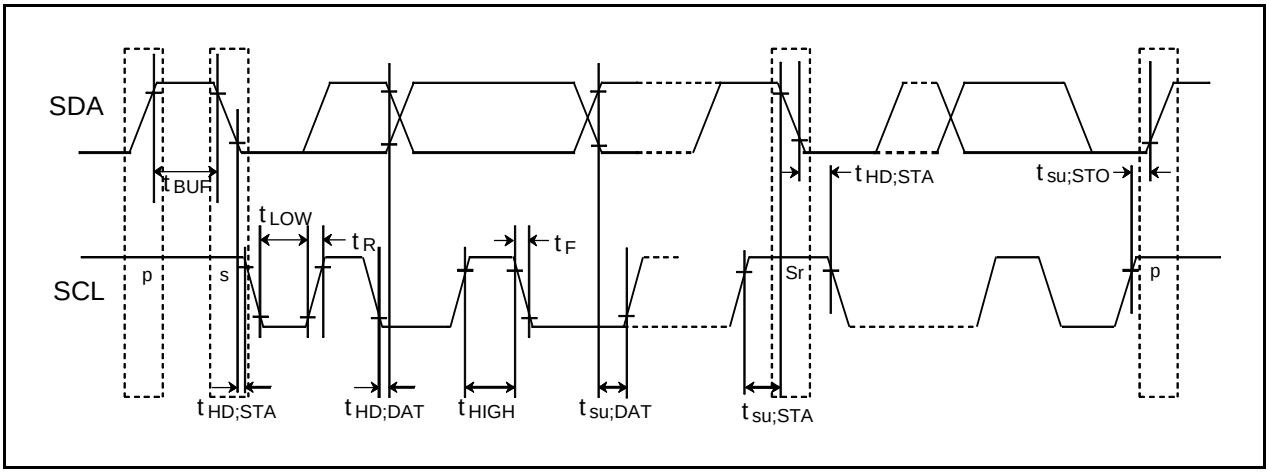


Figure 31.27 Multi-master I²C-bus

J-Version, V_{CC} = 3 V

Timing Requirements
(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = −40°C to 85°C unless otherwise specified)

31.3.2.9 Serial bus interface

Table 31.48 Serial Bus Interface

Symbol	Characteristic		Measurement condition	Standard			Unit
				Min.	Typ.	Max.	
$t_{c(SSCK)}$	SSCK clock cycle time			250			ns
$t_{w(SSCKH)}$	SSCK clock high pulse width			0.4		0.6	$t_{c(SSCK)}$
$t_{w(SSCKL)}$	SSCK clock low pulse width			0.4		0.6	$t_{c(SSCK)}$
$t_{r(SSCK)}$	SSCK clock rising time	Master				1	t_{CYC} (1)
		Slave				1	µs
$t_{f(SSCK)}$	SSCK clock falling time	Master				1	t_{CYC} (1)
		Slave				1	µs
$t_{su(SSIO-SSCK)}$	SSO, SSI data input setup time			100			ns
$t_{h(SSCK-SSIO)}$	SSO, SSI data input hold time			1			t_{CYC} (1)
$t_{su(SCS-SSCK)}$	$\overline{SCS}$ setup time	Slave		1 t_{CYC} + 50 (1)			ns
$t_{h(SSCK-SCS)}$	$\overline{SCS}$ hold time	Slave		1 t_{CYC} + 50 (1)			ns
$t_{d(SSCK-SSIO)}$	SSO, SSI data output delay time	Master				1	t_{CYC} (1)
		Slave				80	ns
$t_{en(SCS-SSI)}$	SSI output enable time		3.0 V ≤ V_{CC} ≤ 5.5 V			1.5 t_{CYC} + 100 (1)	ns
$t_{dis(SCS-SSI)}$	SSI output disable time		3.0 V ≤ V_{CC} ≤ 5.5 V			1.5 t_{CYC} + 100 (1)	ns

Note:
1. 1 t_{CYC} is 1/f1 (s).

J-Version, V_{CC} = 3 V

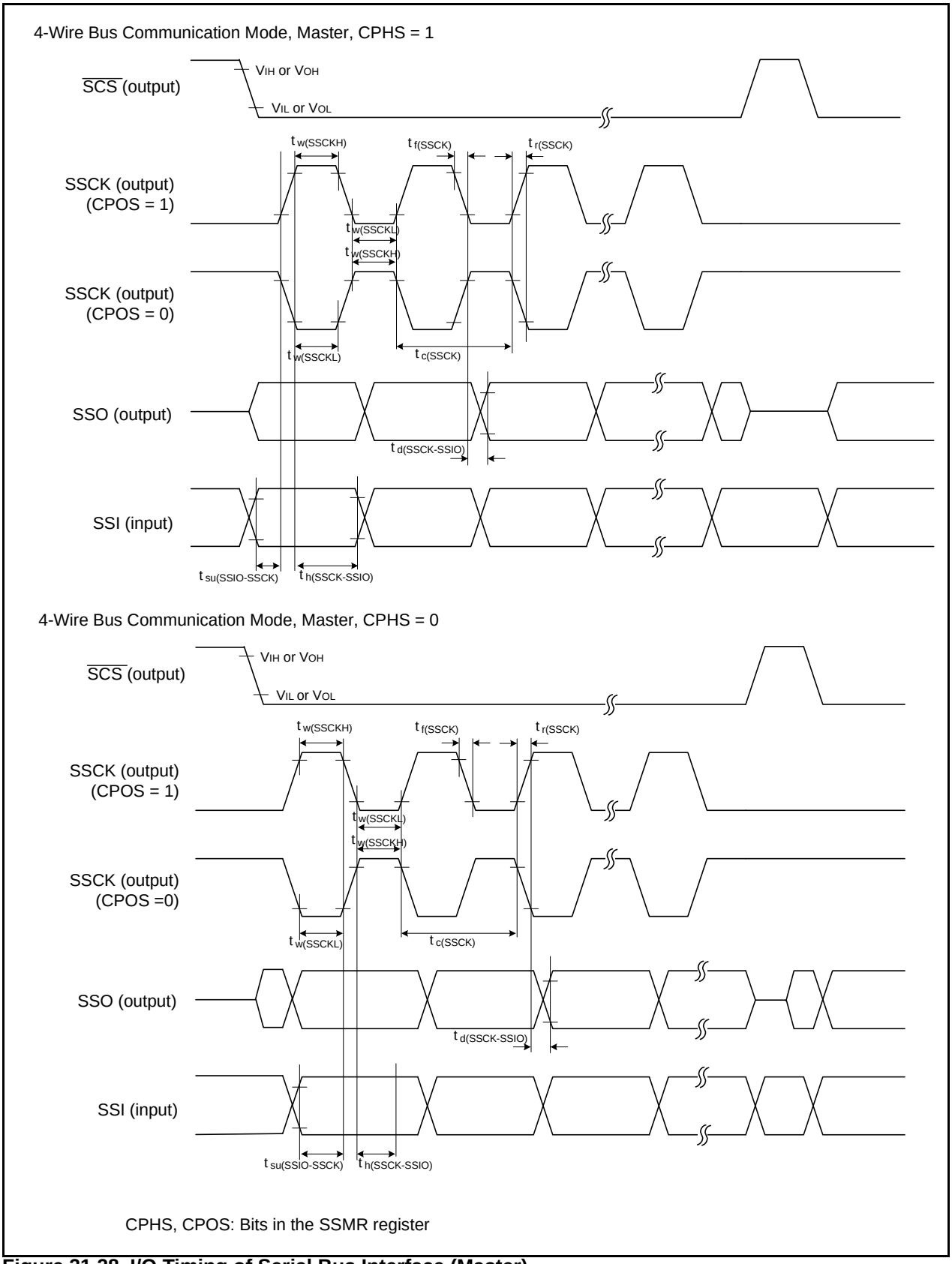


Figure 31.28 I/O Timing of Serial Bus Interface (Master)

J-Version, V_{CC} = 3 V

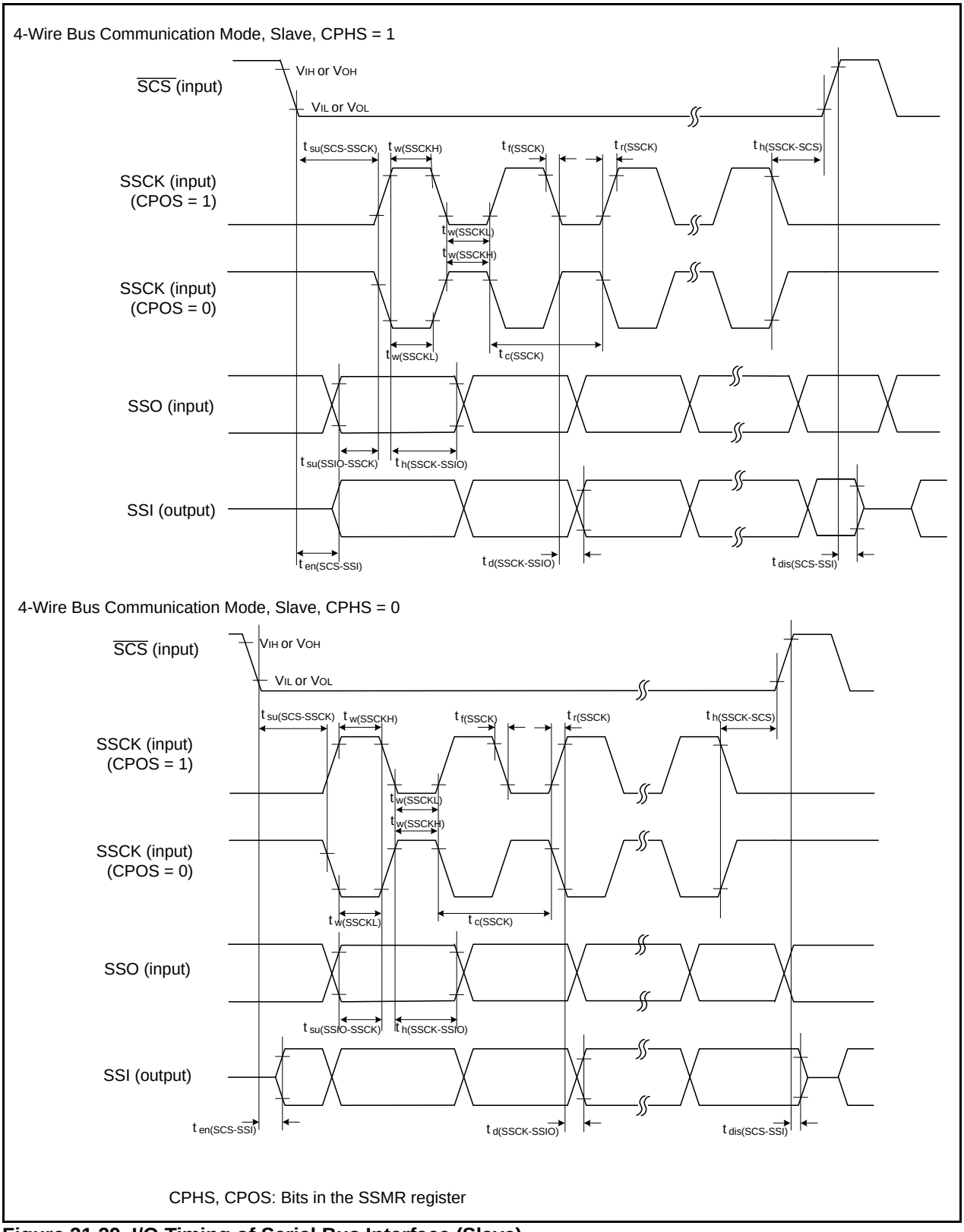


Figure 31.29 I/O Timing of Serial Bus Interface (Slave)

J-Version, V_{CC} = 3 V

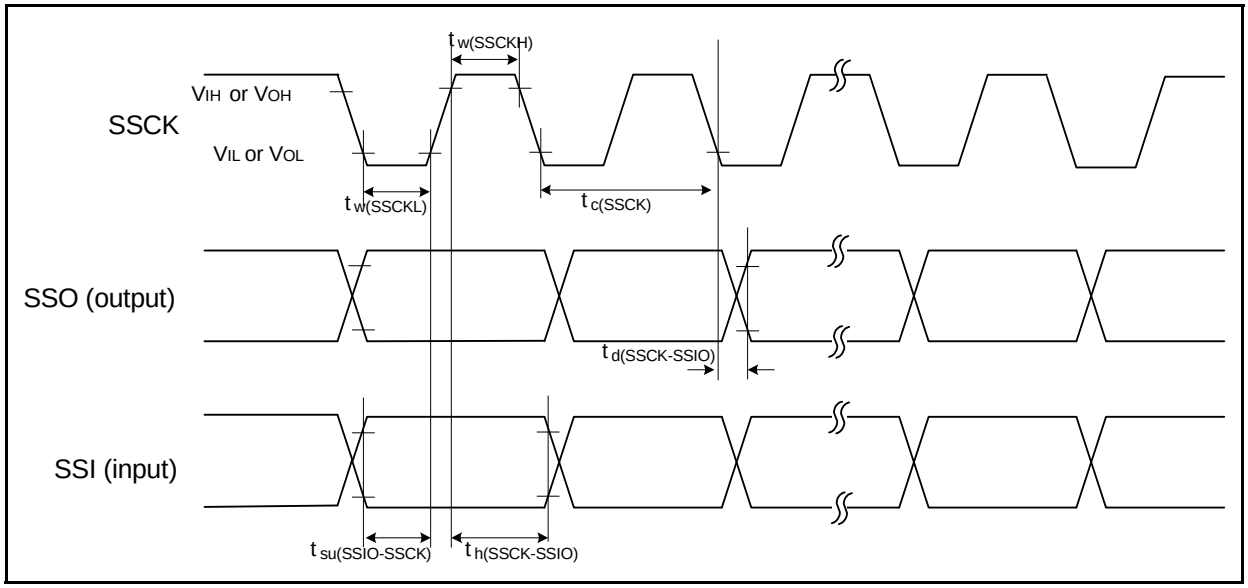


Figure 31.30 I/O Timing of Serial Bus Interface (Synchronous Communication Mode)

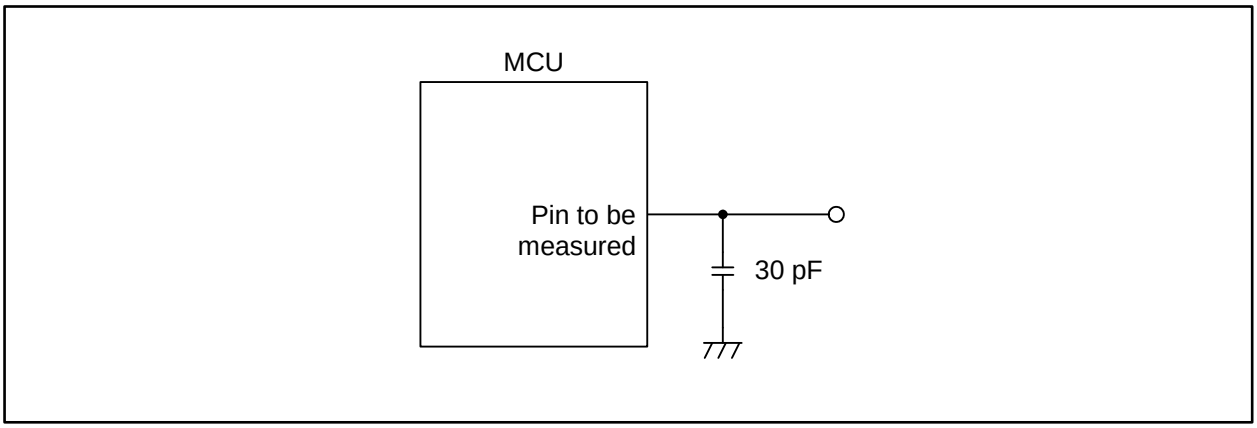


Figure 31.31 Switching Characteristic Measurement Circuit

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31.4 Electrical Characteristics (K-Version, Common to 3 V and 5 V)

31.4.1 Absolute Maximum Rating

Table 31.49 Absolute Maximum Ratings

Symbol	Characteristic		Condition	Rated Value	Unit
V_{CC}	Supply voltage		$V_{CC} = AV_{CC}$	-0.3 to 6.5	V
AV_{CC}	Analog supply voltage		$V_{CC} = AV_{CC}$	-0.3 to 6.5	V
V_{REF}	Analog reference voltage			–0.3 to V_{CC} + 0.1 (1)	V
V_I	Input voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, RESET, CNVSS, VREF		-0.3 to V_{CC} + 0.3	V
V_O	Output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XOUT		-0.3 to V_{CC} + 0.3	V
P_d	Power consumption		-40°C ≤ T_{opr} ≤ 85°C	300	mW
			85°C < T_{opr} ≤ 125°C	250	mW
T_{opr}	Operating temperature range	While CPU operation		-40 to 125	°C
		While flash memory program and erase operation	Programming area	0 to 60	
			Data area	-40 to 125	
T_{stg}	Storage temperature range			-65 to 150	°C

Note:
1. Maximum value is 6.5 V.

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31.4.2 Recommended Operating Conditions

Table 31.50 Operating Conditions (1)

V_{CC} = 3.0 V to 5.5 V, T_{opr} = -40°C to 125°C unless otherwise specified.

Symbol	Characteristic			Standard			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply voltage			3.0		5.5	V
AV_{CC}	Analog supply voltage				V_{CC}		V
V_{SS}	Ground voltage				0		V
AV_{SS}	Analog ground voltage				0		V
V_{IH}	High level input voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7	Input level 0.50 V_{CC}	0.7 V_{CC}		V_{CC}	V
			Input level 0.70 V_{CC}	0.85V_{CC}		V_{CC}	V
		XIN, $\overline{\text{RESET}}$, CNVSS		0.8 V_{CC}		V_{CC}	
		SDAMM, SCLMM	When I^2C-bus input level selected	0.7 V_{CC}		V_{CC}	V
			When SMBUS input level selected	2.1		V_{CC}	V
V_{IL}	Low level input voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7	Input level 0.50 V_{CC}	0		0.3 V_{CC}	V
			Input level 0.70 V_{CC}	0		0.45V_{CC}	V
		XIN, $\overline{\text{RESET}}$, CNVSS		0		0.2 V_{CC}	V
		SDAMM, SCLMM	When I^2C-bus input level selected	0		0.3 V_{CC}	V
			When SMBUS input level selected	0		0.8	V
$I_{OH(sum)}$	High peak output current	Sum of $I_{OH(peak)}$ at P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6 to P8_7, P9_0 to P9_7, P10_0 to P10_7				-80.0	mA
$I_{OH(peak)}$	High level peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6 to P8_7, P9_0 to P9_7, P10_0 to P10_7				-10.0	mA
$I_{OH(avg)}$	High level average output current (2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6 to P8_7, P9_0 to P9_7, P10_0 to P10_7				-5.0	mA
$I_{OL(sum)}$	Low peak output current	Sum of $I_{OL(peak)}$ at P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7				80.0	mA
$I_{OL(peak)}$	Low level peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7				10.0	mA
$I_{OL(avg)}$	Low level average output current (2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7				5.0	mA
$f_{(XIN)}$	Main clock input oscillation frequency (2)			0		20	MHz
$f_{(XCIN)}$	Sub clock oscillation frequency				32.768	50	kHz
$f_{(PLL)}$	PLL clock oscillation frequency (2)			10		32	MHz
$f_{(BCLK)}$	CPU operation frequency			0		32	MHz
$t_{su(PLL)}$	Wait time to stabilize PLL frequency synthesizer					1	ms

Notes:
1. The mean output current is the mean value within 100 ms.
2. Refer to “Figure 31.1 “Main clock input oscillation frequency, PLL clock oscillation frequency”” for the relationship between main clock oscillation frequency/PLL clock oscillation frequency and supply voltage.

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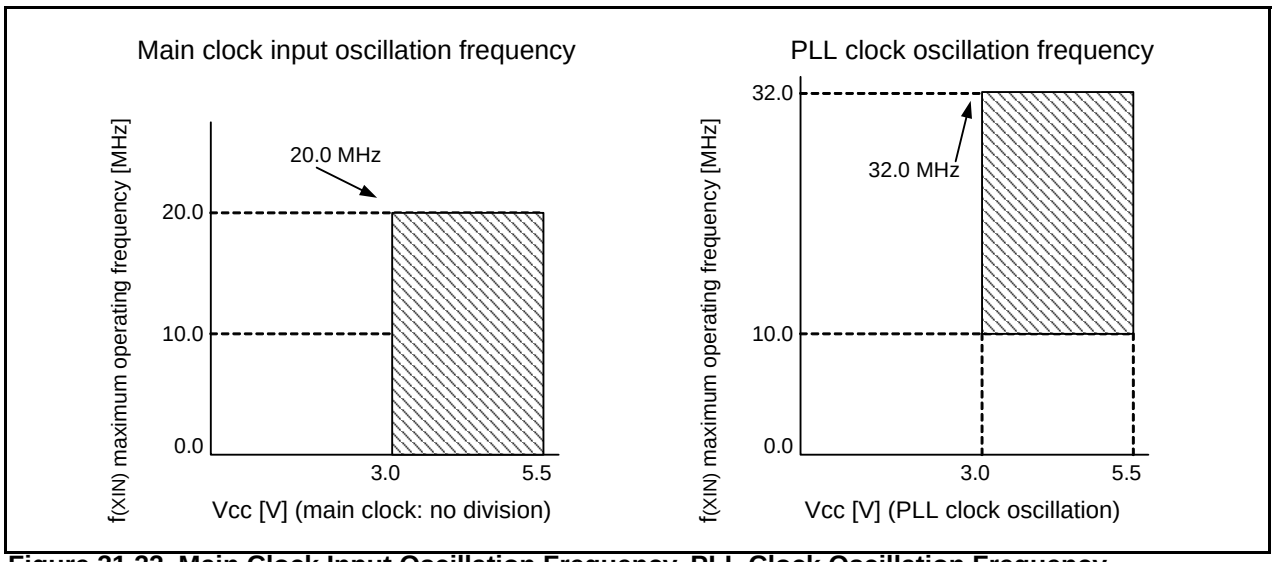

Figure 31.32 Main Clock Input Oscillation Frequency, PLL Clock Oscillation Frequency

Table 31.51 Recommended Operating Conditions (2/2) (1)

V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_{opr} = -40°C to 125°C unless otherwise specified.
The ripple voltage must not exceed $V_{r(VCC)}$ and/or $dV_{r(VCC)}/dt$.

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$V_{r(VCC)}$	Allowable ripple voltage	V_{CC} = 5.0 V			0.5	Vp-p
		V_{CC} = 3.0 V			0.3	Vp-p
$dV_{r(VCC)}/dt$	Ripple voltage falling gradient	V_{CC} = 5.0 V			0.3	V/ms
		V_{CC} = 3.0 V			0.3	V/ms

Note:
1. The device is operationally guaranteed under these operating conditions.

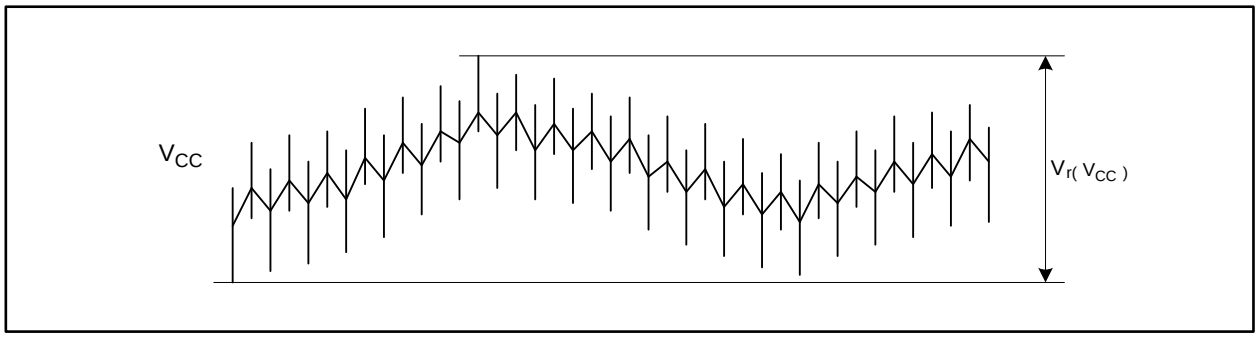

Figure 31.33 Ripple Waveform

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31.4.3 A/D Conversion Characteristics

Table 31.52 A/D Conversion Characteristics (1)

$V_{CC} = AV_{CC} = V_{REF} = 3.0$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V at $T_{opr} = -40°C$ to 125°C unless otherwise specified.

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Resolution	$V_{REF} = V_{CC}$			10	Bits
I_{NL}	Integral non-linearity error	$V_{REF} = V_{CC} = 5.0$ V (2)			±3	LSB
		$V_{REF} = V_{CC} = 3.3$ V (2)			±5	LSB
—	Absolute accuracy	$V_{REF} = V_{CC} = 5.0$ V (2)			±3	LSB
		$V_{REF} = V_{CC} = 3.3$ V (2)			±5	LSB
ϕAD	A/D operating clock frequency	4.0 V ≤ V_{CC} ≤ 5.5 V	2		25	MHz
		3.2 V ≤ V_{CC} ≤ 4.0 V	2		16	MHz
		3.0 V ≤ V_{CC} ≤ 3.2 V	2		10	MHz
—	Tolerance level impedance			3		kΩ
D_{NL}	Differential non-linearity error	See note 2			±1	LSB
—	Offset error (4)	See note 2			±3	LSB
—	Gain error (4)	See note 2			±3	LSB
t_{CONV}	10-bit conversion time	$V_{REF} = V_{CC} = 5$V, ϕAD = 25 MHz	1.60			µs
t_{samp}	Sampling time		0.6			µs
V_{REF}	Reference voltage		3.0		V_{CC}	V
V_{IA}	Analog input voltage (3)		0		V_{REF}	V

Notes:
1. Use when $AV_{CC} = V_{CC}$
2. Flash memory rewrite disabled. Except for the analog input pin, set the pins to be measured as input ports and connect them to V_{SS}. See Figure 31.34 “A/D Accuracy Measure Circuit”.
3. When analog input voltage is over reference voltage, the result of A/D conversion is 3FFh.

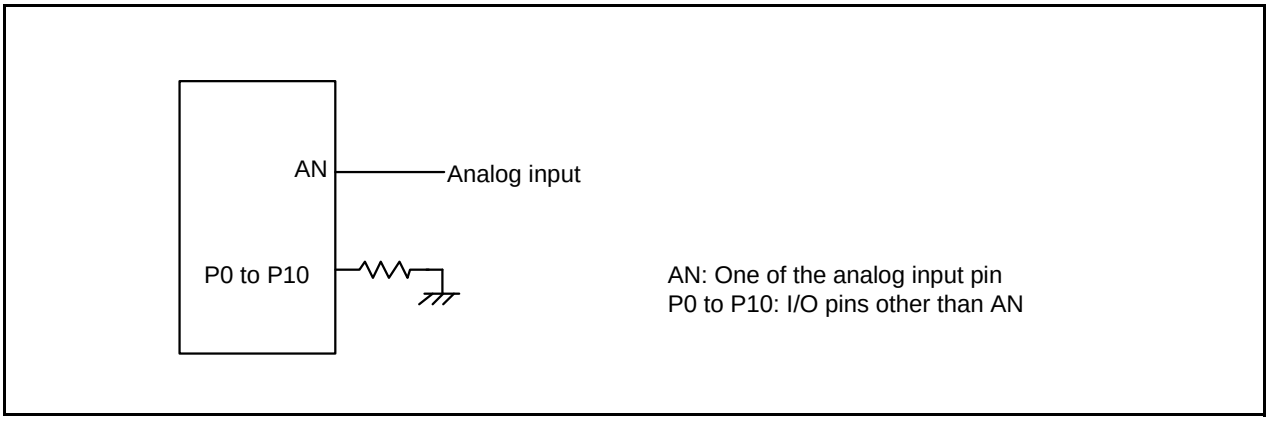

Figure 31.34 A/D Accuracy Measure Circuit

31.4.4 D/A Conversion Characteristics

Table 31.53 D/A Conversion Characteristics

$V_{CC} = AV_{CC} = V_{REF} = 3.0$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V at $T_{opr} = -40°C$ to 125°C unless otherwise specified.

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute accuracy				2.5	LSB
t_{SU}	Setup time				3	µs
R_O	Output resistance		5	6	8.2	kΩ
I_{VREF}	Reference power supply input current	See Notes 1 and 2			1.5	mA

Notes:
1. This applies when using one D/A converter, with the D/A register for the unused D/A converter set to 00h.
2. The current consumption of the A/D converter is not included. Also, the I_{VREF} of the D/A converter will flow even if the ADSTBY bit in the ADCON1 register is 0 (A/D operation stopped (standby)).

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31.4.5 Flash Memory Electrical Characteristics

Table 31.54 CPU Clock When Operating Flash Memory ($f_{(BCLK)}$)

V_{CC} = 3.0 to 5.5 V at T_{opr} = -40°C to 125°C, unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	CPU rewrite mode				16 (1)	MHz
$f_{(SLOW\_R)}$	Slow read mode				5 (3)	MHz
-	Low current consumption read mode			fC	35	kHz
-	Data flash read				20 (2)	MHz

Notes:
1. Set the PM17 bit in the PM1 register to 1 (one wait).
2. When the frequency is over this value, set the FMR17 bit in the FMR1 register to 0 (one wait) or the PM17 bit in the PM1 register to 1 (one wait)
3. Set the PM17 bit in the PM1 register to 1 (one wait). No wait states are required if the 125 kHz on-chip oscillator clock or sub clock is used as the clock source of the CPU clock.

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Table 31.55 Flash Memory (Program ROM 1, 2) Electrical Characteristics

V_{CC} = 3.0 to 5.5 V at T_{opr} = 0°C to 60°C, unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	Program/erase cycles (1, 3, 4)	V_{CC} = 3.3 V, T_{opr} = 25°C	1,000 (2)			times
-	2 words program time	V_{CC} = 3.3 V, T_{opr} = 25°C		150	4000	µs
	Lock bit program time	V_{CC} = 3.3 V, T_{opr} = 25°C		70	3000	µs
-	Block erase time	V_{CC} = 3.3 V, T_{opr} = 25°C		0.2	3.0	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend				$5 + \frac{3}{f(BCLK)}$	ms
-	Interval from erase start/restart until following suspend request		0			µs
-	Suspend interval necessary for auto-erasure to complete (7)		20			ms
-	Time from suspend until erase restart				$30 + \frac{1}{f(BCLK)}$	µs
-	Program, erase voltage		3.0		5.5	V
-	Read voltage	Topr = -40°C to 125°C	3.0		5.5	V
-	Program, erase temperature		0		60	°C
t_{PS}	Flash Memory Circuit Stabilization Wait Time				50	µs
-	Data hold time (6)	Ambient temperature = 55°C	20			year

Notes:
1. Definition of program and erase cycles:
   The program and erase cycles refer to the number of per-block erasures. If the program and erase cycles are n (n = 1,000), each block can be erased n times. For example, if a 64 KB block is erased after writing 2 word data 16,384 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
2. Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. It is advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact a Renesas Electronics sales office.
6. The data hold time includes time that the power supply is off or the clock is not supplied.
7. After an erase start or erase restart, if an interval of at least 20 ms is not set before the next suspend request, the erase sequence cannot be completed.

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Table 31.56 Flash Memory (Data Flash) Electrical Characteristics

V_{CC} = 3.0 to 5.5 V at T_{opr} = -40°C to 125°C, unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	Program/erase cycles (1, 3, 4)	V_{CC} = 3.3 V, T_{opr} = 25°C	10,000 (2)			times
-	2 words program time	V_{CC} = 3.3 V, T_{opr} = 25°C		300	4000	µs
-	Lock bit program time	V_{CC} = 3.3 V, T_{opr} = 25°C		140	3000	µs
-	Block erase time	V_{CC} = 3.3 V, T_{opr} = 25°C		0.2	3.0	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend				$5 + \frac{3}{f(BCLK)}$	ms
-	Interval from erase start/restart until following suspend request		0			µs
-	Suspend interval necessary for auto-erasure to complete (7)		20			ms
-	Time from suspend until erase restart				$30 + \frac{1}{f(BCLK)}$	µs
-	Program, erase voltage		3.0		5.5	V
-	Read voltage		3.0		5.5	V
-	Program, erase temperature		–40		125	°C
t_{PS}	Flash Memory Circuit Stabilization Wait Time				50	µs
-	Data hold time (6)	Ambient temperature = 55 °C	20			year

Notes:

1. Definition of program and erase cycles
   The program and erase cycles refer to the number of per-block erasures.
   If the program and erase cycles are n (n = 10,000), each block can be erased n times.
   For example, if a 4 KB block is erased after writing 2 word data 1,024 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
2. Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 256 groups before erasing them all in one operation. In addition, averaging the erasure cycles between blocks A and B can further reduce the actual erasure cycles. It is also advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact a Renesas Electronics sales office.
6. The data hold time includes time that the power supply is off or the clock is not supplied.
7. After an erase start or erase restart, if an interval of at least 20 ms is not set before the next suspend request, the erase sequence cannot be completed.

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31.4.6 E2PROM Emulation Data Flash

Table 31.57 E²PROM Emulation Data Flash Electrical Characteristics

V_{CC} = 3.0 to 5.5 V at T_{opr} = -40°C to 125°C, unless otherwise specified.

Symbol	Characteristic		Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase cycles (1)		100000			times
—	Word program time (2-byte program)			100	2000	µs
—	Read time (2-byte read)				1	µs
—	Block erase time (32-byte block)			15	200	ms
t_{PS}	Flash memory circuit stabilization wait time (sleep mode to normal mode)			35	50	µs
—	Data hold time (2)	Ambient temperature = 55°C (3, 4)	20			years

Notes:

1. Definition of program/erase cycles definition
   This value represents the number of erasure per block.
   If the flash memory is programmed/erased n times, each block can be erased n times.
   i.e. If a word write is performed in different 16 addresses in a block and then the block is erased, it is considered the programming/erasure is performed just once. However a write in the same address more than once for one erasure is disabled. (overwrite disabled).
2. The data hold time includes the periods when the supply voltage is not applied and no clock is provided.
3. This data hold time includes (3000) hours in Ambient temperature = 125°C.
4. Please contact a Renesas Electronics sales office regarding data retention time other than the above.

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31.4.7 Voltage Detector and Power Supply Circuit Electrical Characteristics

Table 31.58 Voltage Detector 0 Electrical Characteristics

The measurement condition is V_{CC} = 3.0 to 5.5 V, T_{opr} = -40°C to 125°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level V_{det0}	When V_{CC} is falling.	2.70	2.85	3.00	V
$t_{d(E-A)}$	Waiting time until voltage detector operation starts (1)	V_{CC} = 3.0 to 5.0 V			100	µs

Note:
1. Necessary time until the voltage detector operates when setting to 1 again after setting the VC25 bit in the VCR2 register to 0.

Table 31.59 Voltage Detector 2 Electrical Characteristics

The measurement condition is V_{CC} = 3.0 to 5.5 V, T_{opr} = -40°C to 125°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet2_0	Voltage detection level Vdet2_0	When V_{CC} is falling		3.21		V
Vdet2_1	Voltage detection level Vdet2_1			3.36		V
Vdet2_2	Voltage detection level Vdet2_2			3.51		V
Vdet2_3	Voltage detection level Vdet2_3			3.66		V
Vdet2_4	Voltage detection level Vdet2_4		3.51	3.81	4.11	V
Vdet2_5	Voltage detection level Vdet2_5			3.96		V
Vdet2_6	Voltage detection level Vdet2_6			4.10		V
Vdet2_7	Voltage detection level Vdet2_7			4.25		V
-	Hysteresis width at the rising of V_{CC} in voltage detector 2			0.15		V
$t_{d(E-A)}$	Waiting time until voltage detector operation starts (1)	V_{CC} = 3.0 to 5.0 V			100	µs

Note:
1. Necessary time until the voltage detector operates after setting to 1 again after setting the VC27 bit in the VCR2 register to 0.

Table 31.60 Power-On Reset Circuit

The measurement condition is T_{opr} = -40°C to 125°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient		2.0		50000	mV/ms
t_{fth}	External power V_{CC} fall gradient				50000	mV/ms
V_{por}	Voltage at which power-on reset enabled (1)				0.1	V
$t_{w(por)}$	Hold time at which power-on reset enabled		1.0			ms

Note:
1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS1 address to 0.

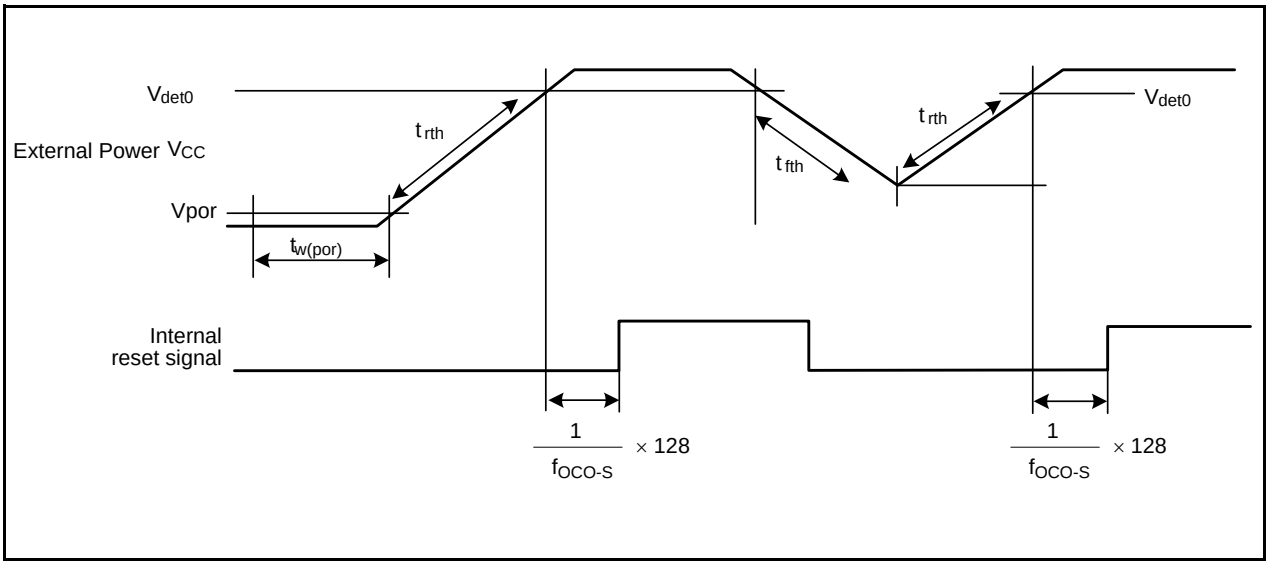


Figure 31.35 Power-On Reset Circuit Electrical Characteristics

Table 31.61 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during powering-on	VCC = 3.0 V to 5.5V			5	ms
$t_{d(R-S)}$	STOP release time				300	µs
$t_{d(W-S)}$	Low power mode wait mode release time				300	µs

Note:
1. When V_{CC} = 5 V.

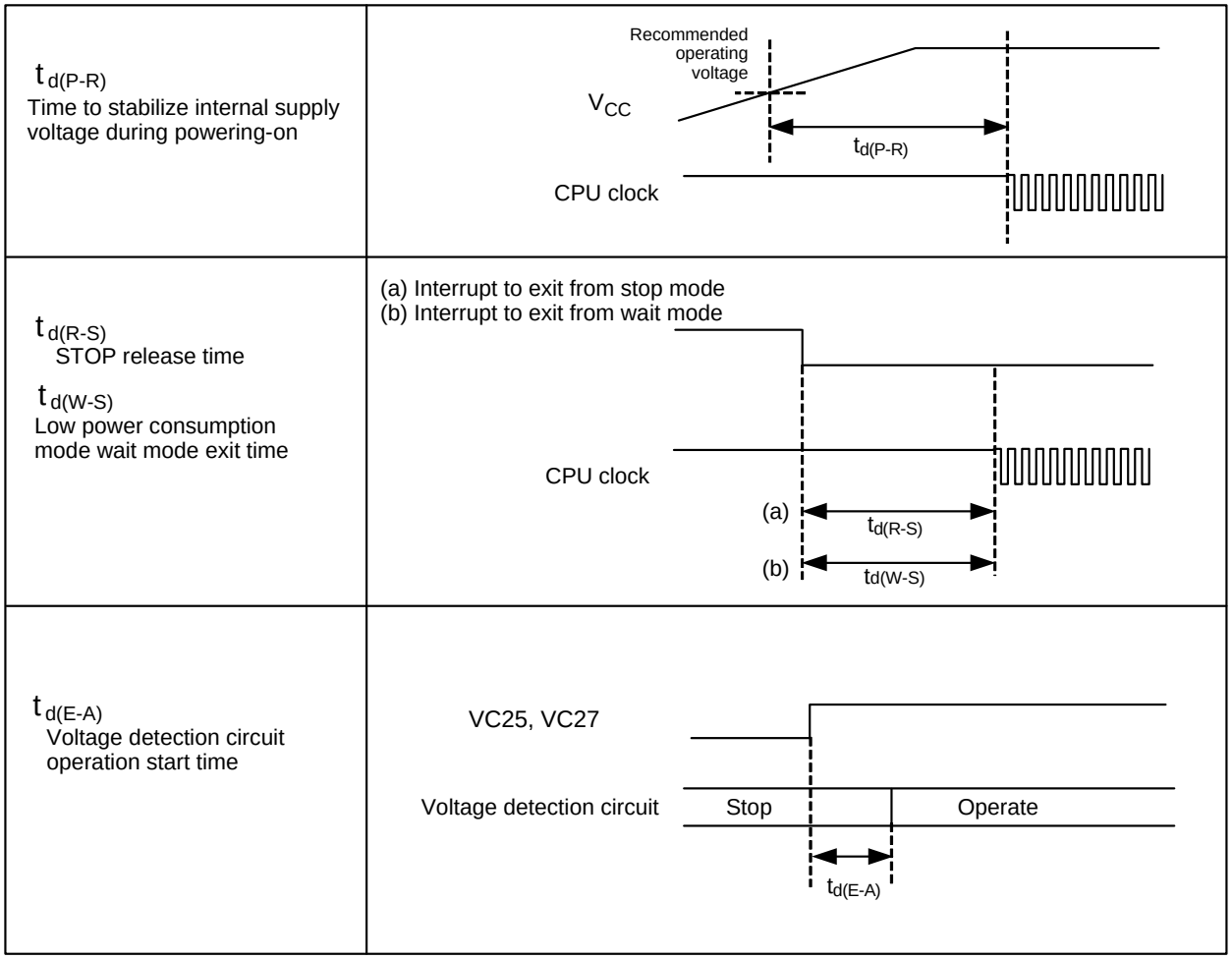


Figure 31.36 Power Supply Circuit Timing Diagram

31.4.8 Oscillator Electrical Characteristics

Table 31.62 On-Chip Oscillator Electrical Characteristics

V_{CC} = 3.0 to 5.5 V, T_{opr} = –40°C to 125°C, unless otherwise specified

Symbol	Characteristic	Value			Unit
		Min.	Typ.	Max.	
f_{OCO-S}	125 kHz on-chip oscillator oscillation frequency	100	125	150	kHz
f_{OCO40M}	40 kHz on-chip oscillator oscillation frequency	32	40	48	MHz
f_{WDT}	Dedicated 125 kHz on-chip oscillator for the watchdog timer oscillation frequency	100	125	150	kHz

31.5 Electrical Characteristics (K-Version, V_{CC} = 5 V)

31.5.1 Electrical Characteristics

K-Version, V_{CC} = 5 V

Table 31.63 Electrical Characteristics (1)

V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V at T_{opr} = −40°C to 125°C, $f_{(BCLK)}$ = 32 MHz unless otherwise specified.

Symbol	Parameter			Measuring Condition	Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	HIGH output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6 to P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OH}=−5 mA	V_{CC}−2.0		V_{CC}	V
V_{OH}	HIGH output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6 to P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OH} = −200 µA	V_{CC}−0.3		V_{CC}	V
V_{OH}	HIGH output voltage	XOUT	HIGH POWER	I_{OH} = −1 mA	V_{CC}−2.0		V_{CC}	V
			LOW POWER	I_{OH} = −0.5 mA	V_{CC}−2.0		V_{CC}	
	HIGH output voltage	XCOUT	HIGH POWER	With no load applied		2.5		V
			LOW POWER	With no load applied		1.6		
V_{OL}	LOW output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OL} = 5 mA			2.0	V
V_{OL}	LOW output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OL} = 200 µA			0.45	V
V_{OL}	LOW output voltage	XOUT	HIGH POWER	I_{OL} = 1 mA			2.0	V
			LOW POWER	I_{OL} = 0.5 mA			2.0	
	LOW output voltage	XCOUT	HIGH POWER	With no load applied		0		V
			LOW POWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	TA0IN to TA4IN, TB0IN to TB5IN, $\overline{INT0}$ to $\overline{INT7}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS3}$, SCL2, SDA2, CLK0 to CLK4, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD4, ZP, IDU, IDW, IDV, SD, INPC1_0 to INPC1_7, SSI0, SSCK0, $\overline{SCS0}$, LIN0IN, CRX0, CRX1			0.2		0.4V_{CC}	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$			0.2		2.5	V
V_{T+}-V_{T-}	Hysteresis	XIN			0.2		0.8	V
I_{IH}	HIGH input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$, CNVSS		V_I = 5 V			5.0	µA
I_{IL}	LOW input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 toP9_7, P10_0 to P10_7 XIN, $\overline{RESET}$, CNVSS		V_I = 0 V			−5.0	µA
R_{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6 to P8_7, P9_0 to P9_7, P10_0 to P10_7		V_I = 0 V	30	50	170	kΩ
R_{fXIN}	Feedback resistance	XIN				1.5		MΩ
R_{fXCIN}	Feedback resistance	XCIN				15		MΩ
V_{RAM}	RAM retention voltage			At stop mode	2.0			V

K-Version, V_{CC} = 5 V

Table 31.64 Electrical Characteristics (2)

T_{opr} = –40°C to 125°C unless otherwise specified.

Symbol	Parameter	Measuring Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC} = 4.2 V to 5.5 V) In single-chip mode, the output pins are open and other pins are V_{SS}	High speed mode	$f_{(BCLK)}$ = 32 MHz, XIN = 8 MHz (square wave), PLL multiply-by-8 125 kHz on-chip oscillator operating		25	45	mA
			$f_{(BCLK)}$ = 20 MHz, XIN = 20 MHz (square wave), 125 kHz on-chip oscillator operating		21	39	mA
			$f_{(BCLK)}$ = 16 MHz, XIN = 16 MHz (square wave), 125 kHz on-chip oscillator operating		17		mA
		40 MHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator operating 125 kHz on-chip oscillator operating No division		21	39	mA
			Main clock stopped 40 MHz on-chip oscillator operating 125 kHz on-chip oscillator operating Divide-by-8		6		mA
		125 kHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Divide-by-8 FMR22 = FMR23 = 1 (Low-current consumption read mode)		190	580	µA
		Low power mode	$f_{(BCLK)}$ = 32 kHz On Flash memory (2) FMR22 = FMR23 = 1 (Low-current consumption read mode)		200		µA
		Wait mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Peripheral clock operating T_{opr} = 25°C		25		µA
			Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Peripheral clock operating T_{opr} = 105°C		85		µA
			Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Peripheral clock operating T_{opr} = 125°C		125		µA
		Stop mode	T_{opr} = 25°C		3	15	µA
			T_{opr} = 105°C		60		µA
			T_{opr} = 125°C		100		µA
		During flash memory program	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC} = 5.0 V		20.0		mA
		During flash memory erase	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC} = 5.0 V		30.0		mA
I_{det2}	Low voltage detection dissipation current				3		µA
I_{det0}	Reset area detection dissipation current				6		µA

Note:

1. This indicates the memory in which the program to be executed exists.

K-Version, V_{CC} = 5 V

31.5.2 Timing Requirements (Peripheral Functions and Others)

(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = –40°C to 125°C unless otherwise specified)

31.5.2.1 Reset Input ($\overline{\text{RESET}}$ Input)

Table 31.65 Reset Input ($\overline{\text{RESET}}$ Input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(RSTL)}$	$\overline{\text{RESET}}$ input low pulse width	10		µs

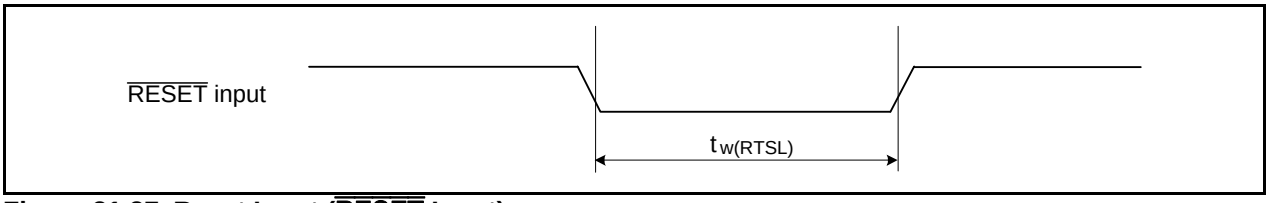


Figure 31.37 Reset Input ($\overline{\text{RESET}}$ Input)

31.5.2.2 External Clock Input

Table 31.66 External Clock Input (XIN input) (1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	50		ns
$t_{w(H)}$	External clock input high pulse width	20		ns
$t_{w(L)}$	External clock input low pulse width	20		ns
t_r	External clock rise time		9	ns
t_f	External clock fall time		9	ns

Note:
1. The condition is V_{CC} = 5.0V.

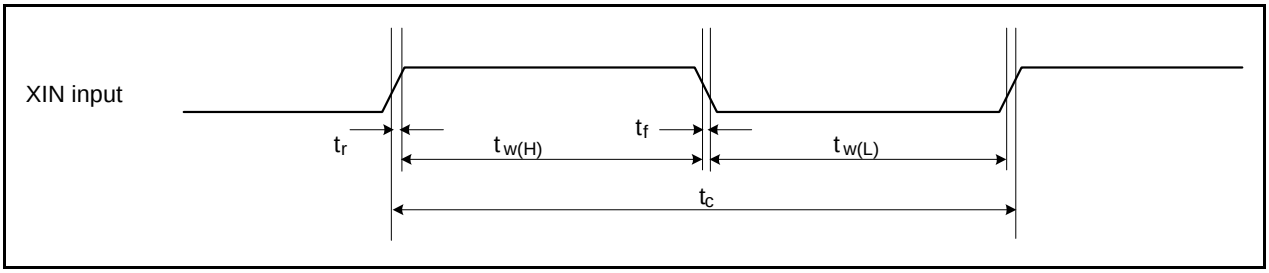


Figure 31.38 External Clock Input (XIN Input)

K-Version, V_{CC} = 5 V

Timing Requirements
(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = −40°C to 125°C unless otherwise specified)

31.5.2.3 Timer A Input

Table 31.67 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	100		ns
$t_{w(TAH)}$	TAiIN input high pulse width	40		ns
$t_{w(TAL)}$	TAiIN input low pulse width	40		ns

Table 31.68 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	400		ns
$t_{w(TAH)}$	TAiIN input high pulse width	200		ns
$t_{w(TAL)}$	TAiIN input low pulse width	200		ns

Table 31.69 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	200		ns
$t_{w(TAH)}$	TAiIN input high pulse width	100		ns
$t_{w(TAL)}$	TAiIN input low pulse width	100		ns

Table 31.70 Timer A Input (External Trigger Input in PWM Mode, Programmable Output Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high pulse width	100		ns
$t_{w(TAL)}$	TAiIN input low pulse width	100		ns

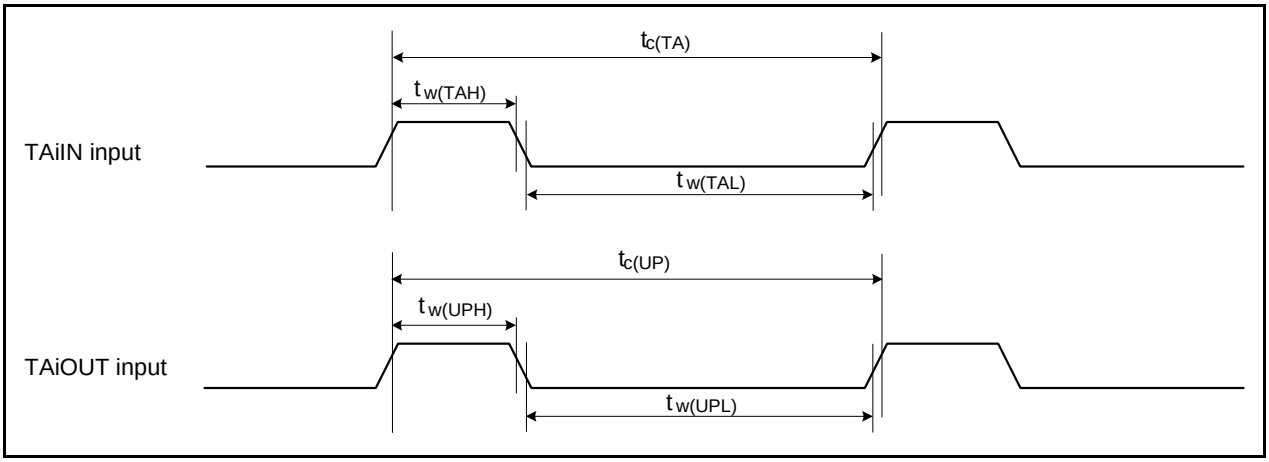


Figure 31.39 Timer A Input

K-Version, V_{CC} = 5 V

Timing Requirements
(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = −40°C to 125°C unless otherwise specified)

Table 31.71 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	800		ns
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	200		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	200		ns

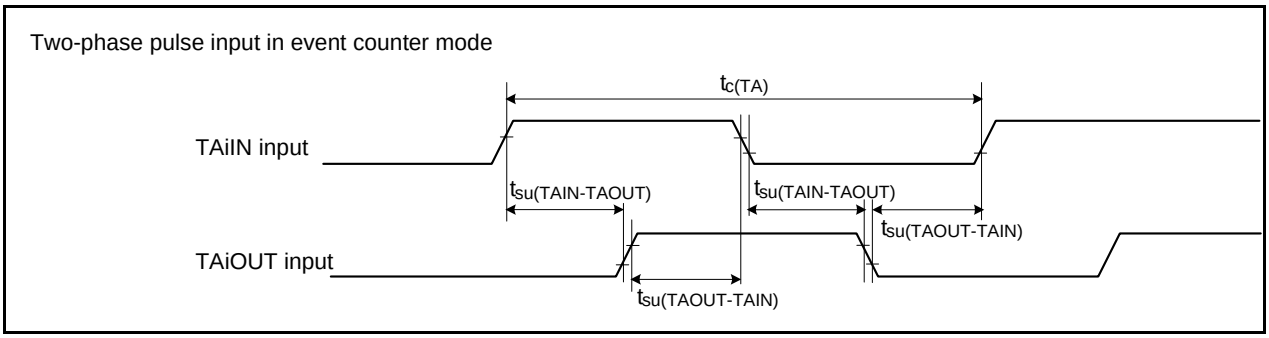


Figure 31.40 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

K-Version, V_{CC} = 5 V

Timing Requirements
(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = −40°C to 125°C unless otherwise specified)

31.5.2.4 Timer B Input

Table 31.72 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input low pulse width (counted on both edges)	80		ns

Table 31.73 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high pulse width	200		ns
$t_{w(TBL)}$	TBiIN input low pulse width	200		ns

Table 31.74 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high pulse width	200		ns
$t_{w(TBL)}$	TBiIN input low pulse width	200		ns

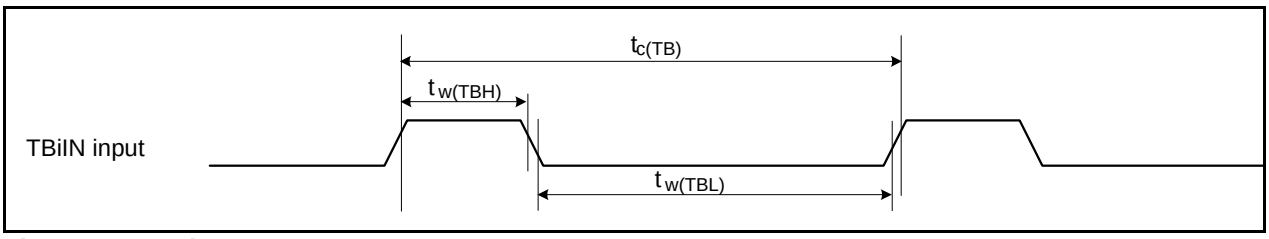


Figure 31.41 Timer B Input

K-Version, V_{CC} = 5 V

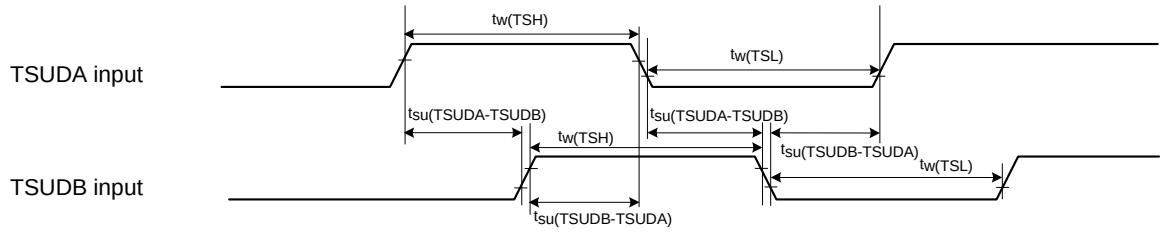
Timing Requirements
(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = −40°C to 125°C unless otherwise specified)

31.5.2.5 Timer S Input

Table 31.75 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TSH)}$	TSUDA, TSUDB input high pulse width	2		µs
$t_{w(TSL)}$	TSUDA, TSUDB input low pulse width	2		µs
$t_{su(TSUDA-TSUDB)}$	TSUDB input setup time	1		µs
$t_{su(TSUDB-TSUDA)}$	TSUDA input setup time	1		µs

Two-phase pulse input in two-phase pulse signal processing mode



Note:
1. When the TSUDA and TSUDB phases are interchanged, $t_{su(TSUDA-TSUDB)}$ and $t_{su(TSUDB-TSUDA)}$ are also interchanged.

Figure 31.42 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)

K-Version, V_{CC} = 5 V

Timing Requirements
(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = −40°C to 125°C unless otherwise specified)

31.5.2.6 Serial Interface

Table 31.76 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200		ns
$t_{w(CKH)}$	CLKi input high pulse width	100		ns
$t_{w(CKL)}$	CLKi input low pulse width	100		ns
$t_{d(C-Q)}$	TXDi output delay time		80	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	70		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

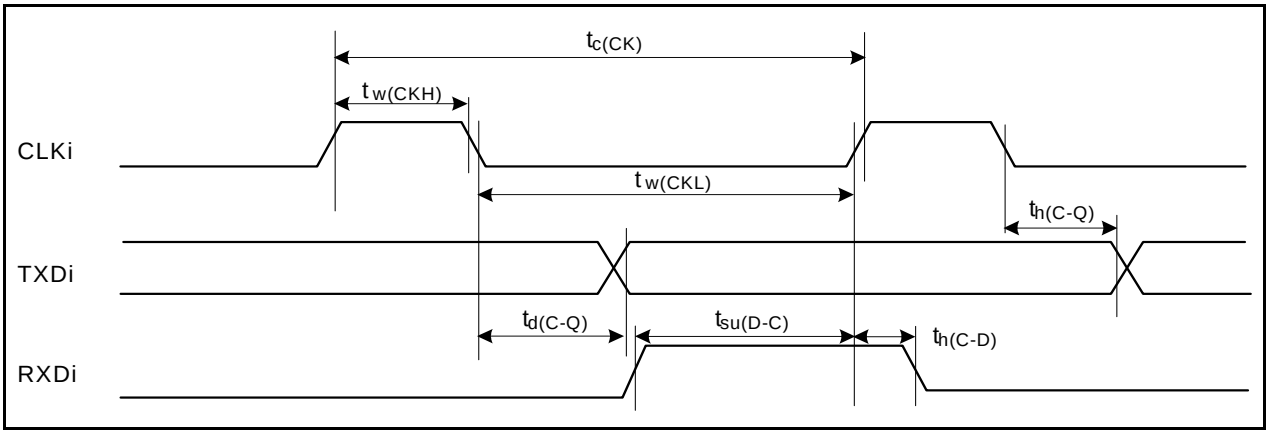


Figure 31.43 Serial Interface

31.5.2.7 External Interrupt $\overline{INTi}$ Input

Table 31.77 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input high pulse width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ input low pulse width	250		ns

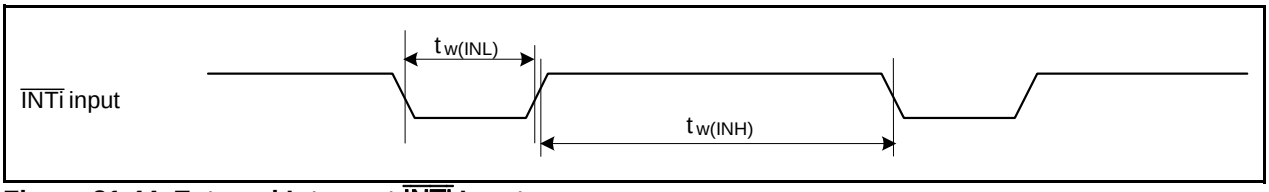


Figure 31.44 External Interrupt $\overline{INTi}$ Input

K-Version, V_{CC} = 5 V

Timing Requirements
(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = −40°C to 125°C unless otherwise specified)

31.5.2.8 Multi-master I²C-bus

Table 31.78 Multi-master I²C-bus

Symbol	Parameter	Standard Clock Mode		Fast-mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		µs
$t_{HD;STA}$	Hold time in start condition	4.0		0.6		µs
t_{LOW}	Hold time in SCL clock 0 status	4.7		1.3		µs
t_R	SCL, SDA signals' rising time		1000	20 + 0.1 Cb	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	µs
t_{HIGH}	Hold time in SCL clock 1 status	4.0		0.6		µs
t_F	SCL, SDA signals' falling time		300	20 + 0.1 Cb	300	ns
$t_{su;DAT}$	Data setup time	250		100		ns
$t_{su;STA}$	Setup time in restart condition	4.7		0.6		µs
$t_{su;STO}$	Stop condition setup time	4.0		0.6		µs

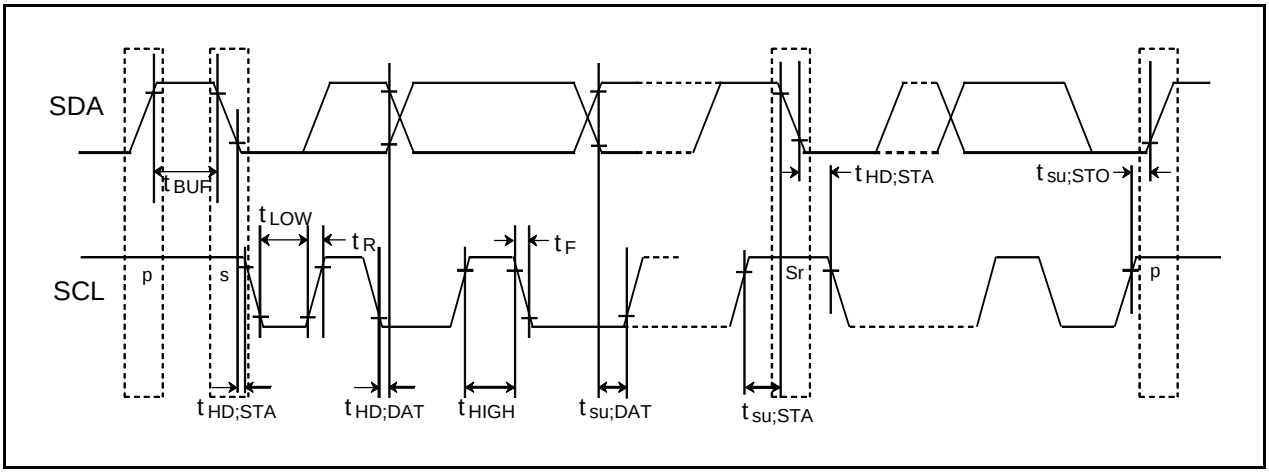


Figure 31.45 Multi-master I²C-bus

K-Version, V_{CC} = 5 V

Timing Requirements
(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = −40°C to 125°C unless otherwise specified)

31.5.2.9 Serial bus interface

Table 31.79 Serial Bus Interface

Symbol	Characteristic		Measurement condition	Standard			Unit
				Min.	Typ.	Max.	
$t_{c(SSCK)}$	SSCK clock cycle time			250			ns
$t_{w(SSCKH)}$	SSCK clock high pulse width			0.4		0.6	$t_{c(SSCK)}$
$t_{w(SSCKL)}$	SSCK clock low pulse width			0.4		0.6	$t_{c(SSCK)}$
$t_{r(SSCK)}$	SSCK clock rising time	Master				1	t_{CYC} (1)
		Slave				1	µs
$t_{f(SSCK)}$	SSCK clock falling time	Master				1	t_{CYC} (1)
		Slave				1	µs
$t_{su(SSIO-SSCK)}$	SSO, SSI data input setup time			100			ns
$t_{h(SSCK-SSIO)}$	SSO, SSI data input hold time			1			t_{CYC} (1)
$t_{su(SCS-SSCK)}$	$\overline{SCS}$ setup time	Slave		1 t_{CYC} + 50 (1)			ns
$t_{h(SSCK-SCS)}$	$\overline{SCS}$ hold time	Slave		1 t_{CYC} + 50 (1)			ns
$t_{d(SSCK-SSIO)}$	SSO, SSI data output delay time	Master				1	t_{CYC} (1)
		Slave				80	ns
$t_{en(SCS-SSI)}$	SSI output enable time		3.0 V ≤ V_{CC} ≤ 5.5 V			1.5 t_{CYC} + 100 (1)	ns
$t_{dis(SCS-SSI)}$	SSI output disable time		3.0 V ≤ V_{CC} ≤ 5.5 V			1.5 t_{CYC} + 100 (1)	ns

Note:
1. 1 t_{CYC} is 1/f1 (s).

K-Version, V_{CC} = 5 V

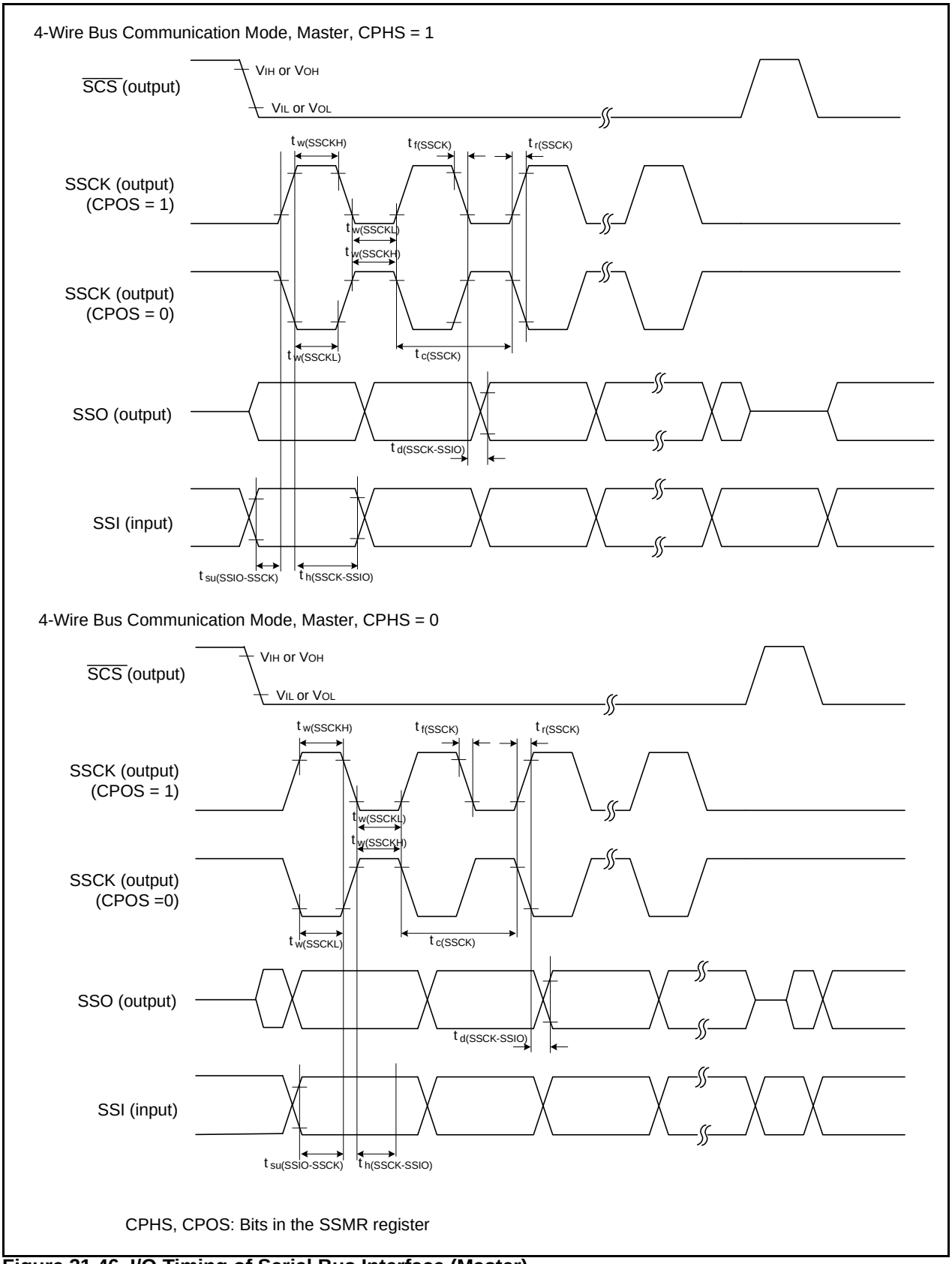


Figure 31.46 I/O Timing of Serial Bus Interface (Master)

K-Version, V_{CC} = 5 V

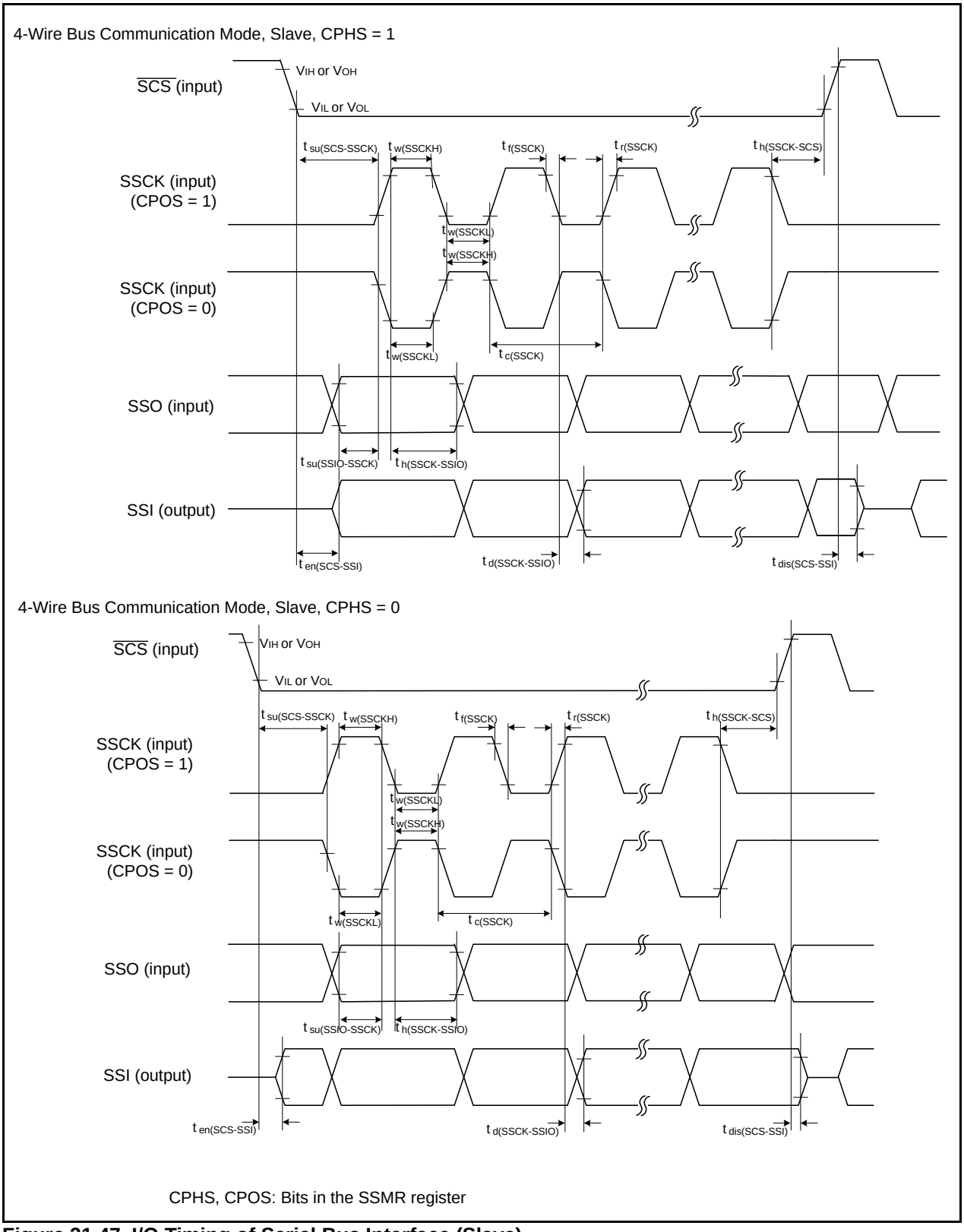


Figure 31.47 I/O Timing of Serial Bus Interface (Slave)

K-Version, V_{CC} = 5 V

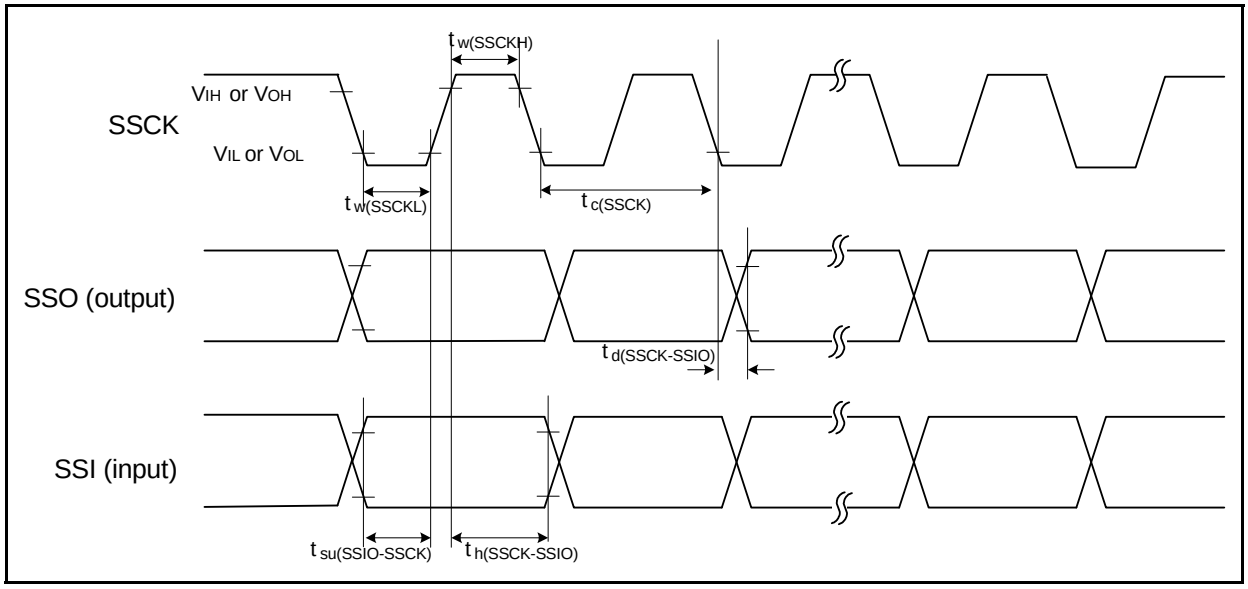


Figure 31.48 I/O Timing of Serial Bus Interface (Synchronous Communication Mode)

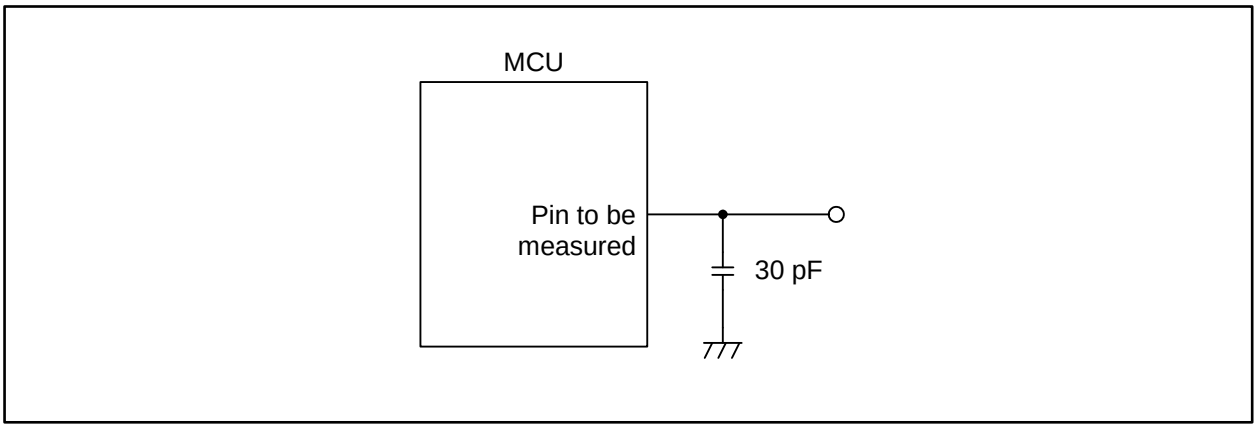


Figure 31.49 Switching Characteristic Measurement Circuit

31.6 Electrical Characteristics (K-Version, V_{CC} = 3 V)

31.6.1 Electrical Characteristics

K-Version, V_{CC} = 3 V

Table 31.80 Electrical Characteristics (1)

V_{CC} = 3.0 to 3.6 V, V_{SS} = 0 V at T_{opr} = −40°C to 125°C, $f_{(BCLK)}$=32 MHz unless otherwise specified.

Symbol	Parameter			Measuring Condition	Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	HIGH output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6 to P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OH} = −1 mA	V_{CC}−0.5		V_{CC}	V
V_{OH}	HIGH output voltage XOUT		HIGH POWER	I_{OH} = −0.1 mA	V_{CC}−0.5		V_{CC}	V
			LOW POWER	I_{OH} = −50 µA	V_{CC}−0.5		V_{CC}	
	HIGH output voltage XCOUT		HIGH POWER	With no load applied		2.5		V
			LOW POWER	With no load applied		1.6		
V_{OL}	LOW output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OL} = 1mA			0.5	V
V_{OL}	LOW output voltage XOUT		HIGH POWER	I_{OL} = 0.1mA			0.5	V
			LOW POWER	I_{OL} = 50µA			0.5	
	LOW output voltage XCOUT		HIGH POWER	With no load applied		0		V
			LOW POWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	TA0IN to TA4IN, TB0IN to TB5IN, $\overline{INT0}$ to $\overline{INT7}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS3}$, SCL2, SDA2, CLK0 to CLK4, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD4, ZP, IDU, IDW, IDV, SD, INPC1_0 to INPC1_7, SSI0, SSCK0, $\overline{SCS0}$, LIN0IN, CRX0, CRX1					0.4V_{CC}	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$					1.8	V
V_{T+}-V_{T-}	Hysteresis	XIN					0.8	V
I_{IH}	HIGH input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$, CNVSS		V_I = 3V			4.0	µA
I_{IL}	LOW input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$, CNVSS		V_I = 0V			−4.0	µA
R_{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6 to P8_7, P9_0 to P9_7, P10_0 to P10_7		V_I = 0V	50	100	500	kΩ
R_{fXIN}	Feedback resistance XIN					3.0		MΩ
R_{fXCIN}	Feedback resistance XCIN					25		MΩ
V_{RAM}	RAM retention voltage			At stop mode	2.0			V

K-Version, V_{CC} = 3 V

Table 31.81 Electrical Characteristics (2)

T_{opr} = −40°C to 125°C unless otherwise specified.

Symbol	Parameter	Measuring Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC} = 3.0 V to 3.6 V) In single-chip mode, the output pins are open and other pins are V_{SS}	High speed mode	$f_{(BCLK)}$ = 32 MHz, XIN = 8 MHz (square wave), PLL multiply-by-8 125 kHz on-chip oscillator operating		23	43	mA
			$f_{(BCLK)}$ = 20 MHz, XIN = 20 MHz (square wave), 125 kHz on-chip oscillator operating		20	38	mA
			$f_{(BCLK)}$ = 16 MHz, XIN = 16 MHz (square wave), 125 kHz on-chip oscillator operating		16		mA
		40 MHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator operating 125 kHz on-chip oscillator operating No division		20	38	mA
			Main clock stopped 40 MHz on-chip oscillator operating 125 kHz on-chip oscillator operating Divide-by-8		6		mA
		125 kHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Divide-by-8 FMR22 = FMR23 = 1 (Low-current consumption read mode)		190	580	µA
		Low power mode	$f_{(BCLK)}$ = 32 kHz On ROM FMR22 = FMR23 = 1 (Low-current consumption read mode)		200		µA
		Wait mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Peripheral clock operating T_{opr} = 25°C		25		µA
			Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Peripheral clock operating T_{opr} = 105°C		85		µA
			Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Peripheral clock operating T_{opr} = 125°C		125		µA
		Stop mode	T_{opr} = 25°C		2	12	µA
			T_{opr} = 105°C		60		µA
			T_{opr} = 125°C		100		µA
		During flash memory program	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC} = 3.0 V		20.0		mA
		During flash memory erase	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC} = 3.0 V		30.0		mA
I_{det2}	Low voltage detection dissipation current				3		µA
I_{det0}	Reset area detection dissipation current				6		µA

K-Version, V_{CC} = 3 V

31.6.2 Timing Requirements (Peripheral Functions and Others)

(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = −40°C to 125°C unless otherwise specified)

31.6.2.1 Reset Input ($\overline{\text{RESET}}$ Input)

Table 31.82 Reset Input ($\overline{\text{RESET}}$ Input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(RSTL)}$	$\overline{\text{RESET}}$ input low pulse width	10		µs

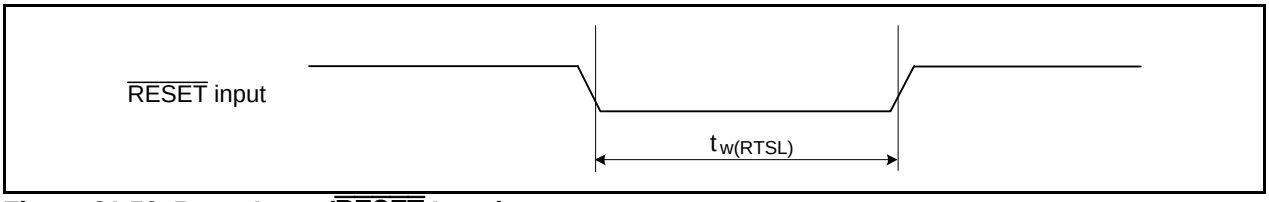


Figure 31.50 Reset Input ($\overline{\text{RESET}}$ Input)

31.6.2.2 External Clock Input

Table 31.83 External Clock Input (XIN input) (1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	50		ns
$t_{w(H)}$	External clock input high pulse width	20		ns
$t_{w(L)}$	External clock input low pulse width	20		ns
t_r	External clock rise time		9	ns
t_f	External clock fall time		9	ns

Note:
1. The condition is V_{CC} = 3.0V.

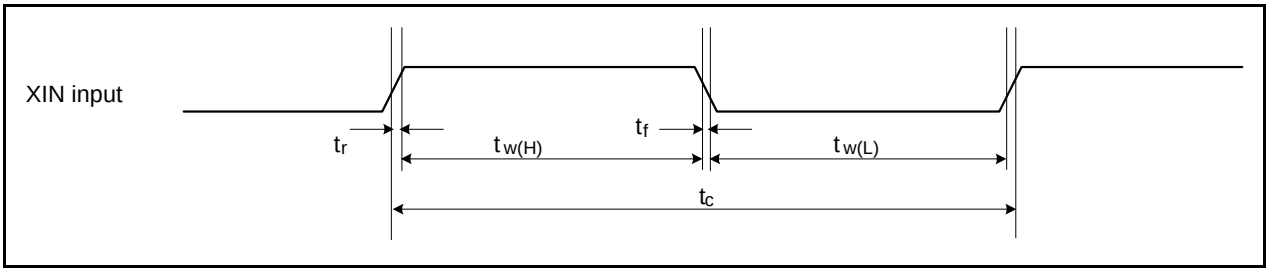


Figure 31.51 External Clock Input (XIN Input)

K-Version, V_{CC} = 3 V

Timing Requirements
(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = –40°C to 125°C unless otherwise specified)

31.6.2.3 Timer A Input

Table 31.84 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	150		ns
$t_{w(TAH)}$	TAiIN input high pulse width	60		ns
$t_{w(TAL)}$	TAiIN input low pulse width	60		ns

Table 31.85 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	600		ns
$t_{w(TAH)}$	TAiIN input high pulse width	300		ns
$t_{w(TAL)}$	TAiIN input low pulse width	300		ns

Table 31.86 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	300		ns
$t_{w(TAH)}$	TAiIN input high pulse width	150		ns
$t_{w(TAL)}$	TAiIN input low pulse width	150		ns

Table 31.87 Timer A Input (External Trigger Input in PWM Mode, Programmable Output Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high pulse width	150		ns
$t_{w(TAL)}$	TAiIN input low pulse width	150		ns

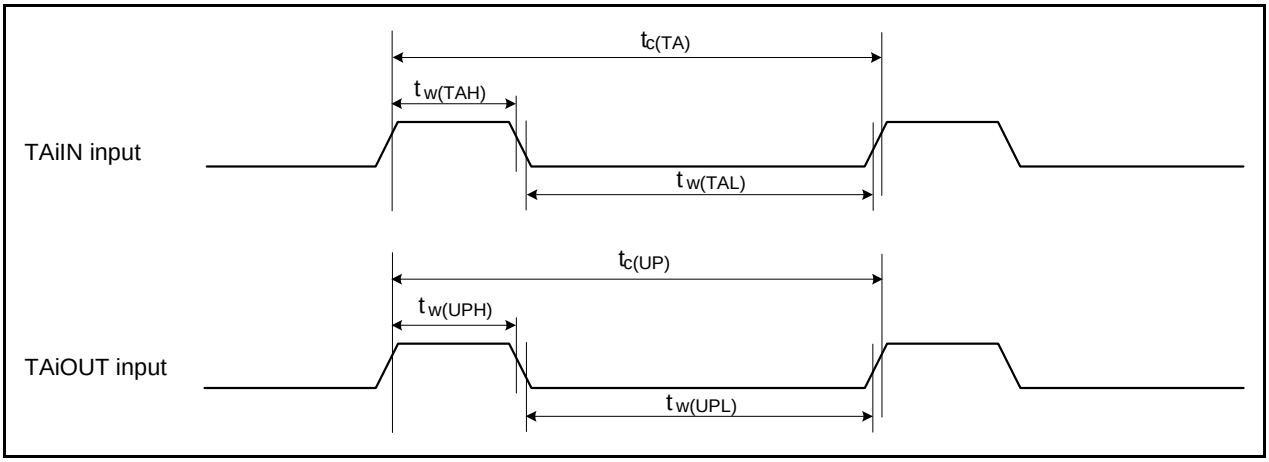


Figure 31.52 Timer A Input

K-Version, V_{CC} = 3 V

Timing Requirements
(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = –40°C to 125°C unless otherwise specified)

Table 31.88 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	2		µs
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	500		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	500		ns

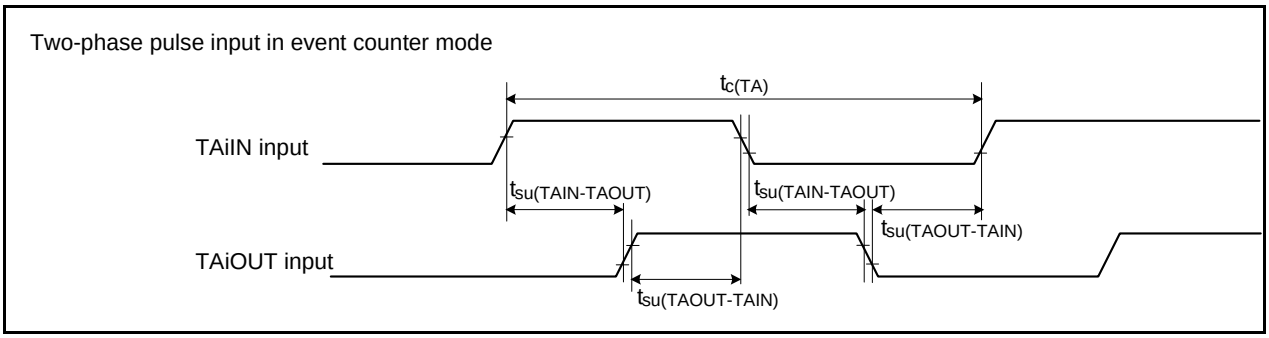


Figure 31.53 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

K-Version, V_{CC} = 3 V

Timing Requirements
(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = –40°C to 125°C unless otherwise specified)

31.6.2.4 Timer B Input

Table 31.89 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on one edge)	60		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on both edges)	120		ns
$t_{w(TBL)}$	TBiIN Input low pulse width (counted on both edges)	120		ns

Table 31.90 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input high pulse width	300		ns
$t_{w(TBL)}$	TBiIN input low pulse width	300		ns

Table 31.91 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input high pulse width	300		ns
$t_{w(TBL)}$	TBiIN input low pulse width	300		ns

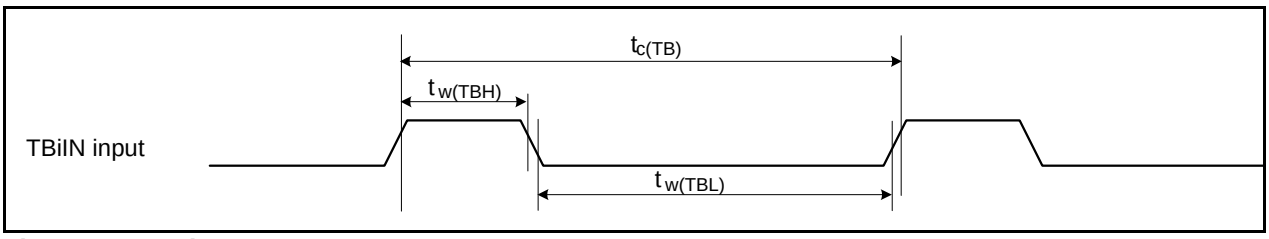


Figure 31.54 Timer B Input

K-Version, V_{CC} = 3 V

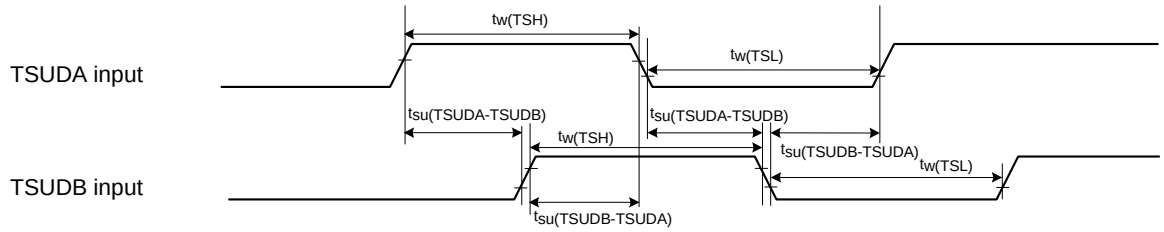
Timing Requirements
(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = –40°C to 125°C unless otherwise specified)

31.6.2.5 Timer S Input

Table 31.92 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TSH)}$	TSUDA, TSUDB input high pulse width	2		µs
$t_{w(TSL)}$	TSUDA, TSUDB input low pulse width	2		µs
$t_{su(TSUDA-TSUDB)}$	TSUDB input setup time	1		µs
$t_{su(TSUDB-TSUDA)}$	TSUDA input setup time	1		µs

Two-phase pulse input in two-phase pulse signal processing mode



Note:
1. When the TSUDA and TSUDB phases are interchanged, $t_{su(TSUDA-TSUDB)}$ and $t_{su(TSUDB-TSUDA)}$ are also interchanged.

Figure 31.55 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)

K-Version, V_{CC} = 3 V

Timing Requirements
(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = –40°C to 125°C unless otherwise specified)

31.6.2.6 Serial Interface

Table 31.93 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300		ns
$t_{w(CKH)}$	CLKi input high pulse width	150		ns
$t_{w(CKL)}$	CLKi input low pulse width	150		ns
$t_{d(C-Q)}$	TXDi output delay time		160	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	100		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

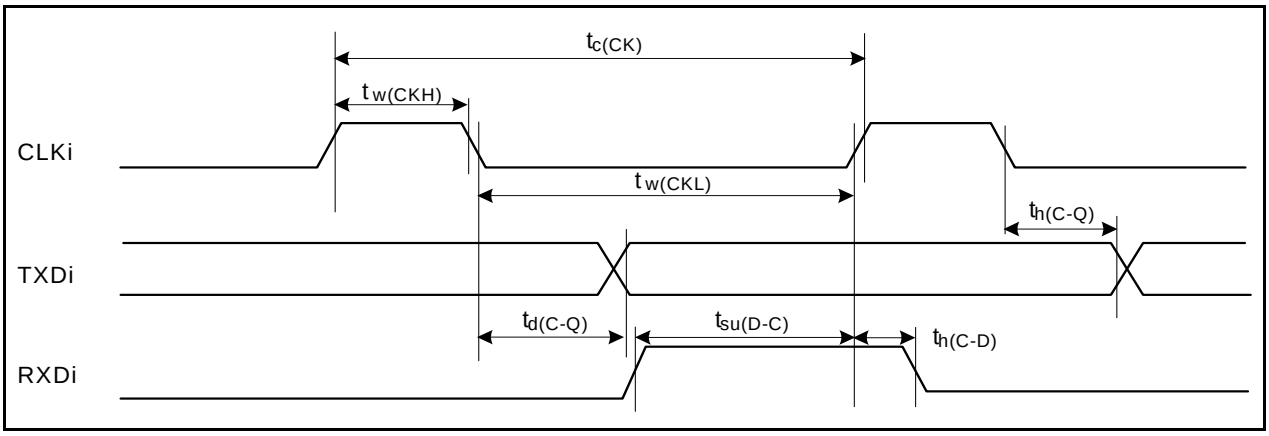


Figure 31.56 Serial Interface

31.6.2.7 External Interrupt $\overline{INTi}$ Input

Table 31.94 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input HIGH Pulse Width	380		ns
$t_{w(INL)}$	$\overline{INTi}$ Input LOW Pulse Width	380		ns

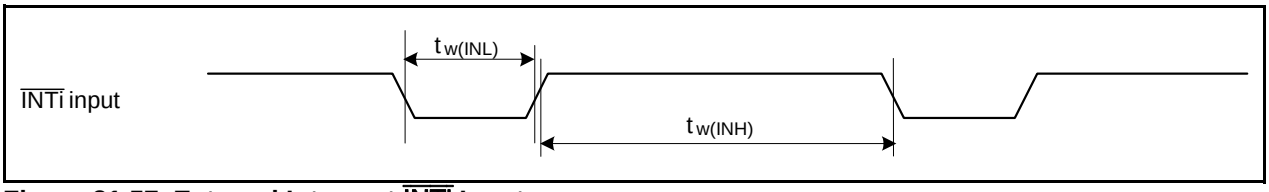


Figure 31.57 External Interrupt $\overline{INTi}$ Input

K-Version, V_{CC} = 3 V

Timing Requirements
(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = –40°C to 125°C unless otherwise specified)

31.6.2.8 Multi-master I²C-bus

Table 31.95 Multi-master I²C-bus

Symbol	Parameter	Standard Clock Mode		Fast-mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		µs
$t_{HD;STA}$	Hold time in start condition	4.0		0.6		µs
t_{LOW}	Hold time in SCL clock 0 status	4.7		1.3		µs
t_R	SCL, SDA signals' rising time		1000	20 + 0.1 Cb	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	µs
t_{HIGH}	Hold time in SCL clock 1 status	4.0		0.6		µs
t_F	SCL, SDA signals' falling time		300	20 + 0.1 Cb	300	ns
$t_{su;DAT}$	Data setup time	250		100		ns
$t_{su;STA}$	Setup time in restart condition	4.7		0.6		µs
$t_{su;STO}$	Stop condition setup time	4.0		0.6		µs

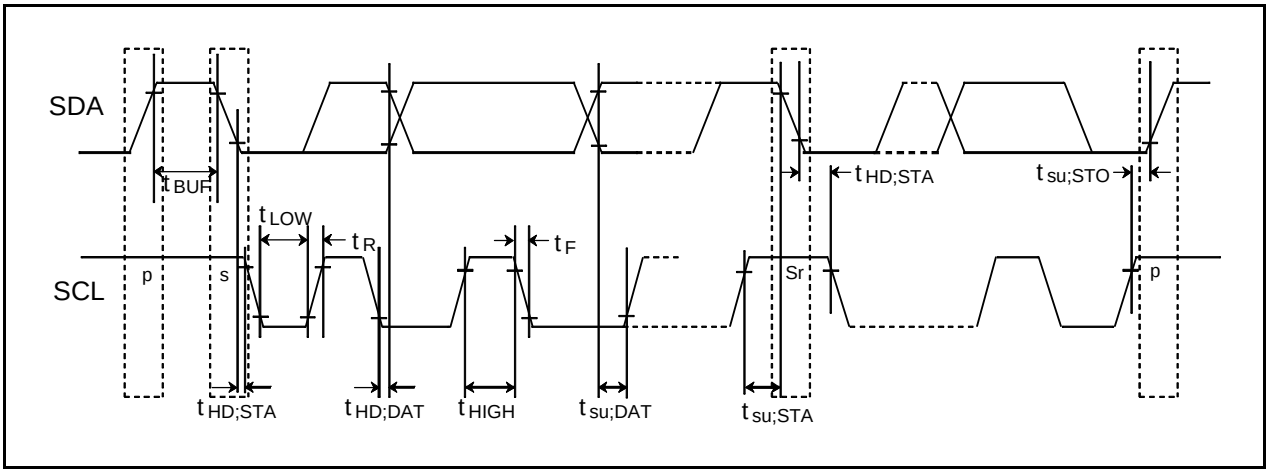


Figure 31.58 Multi-master I²C-bus

K-Version, V_{CC} = 3 V

Timing Requirements
(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = −40°C to 125°C unless otherwise specified)

31.6.2.9 Serial bus interface

Table 31.96 Serial Bus Interface

Symbol	Characteristic		Measurement condition	Standard			Unit
				Min.	Typ.	Max.	
$t_{c(SSCK)}$	SSCK clock cycle time			250			ns
$t_{w(SSCKH)}$	SSCK clock high pulse width			0.4		0.6	$t_{c(SSCK)}$
$t_{w(SSCKL)}$	SSCK clock low pulse width			0.4		0.6	$t_{c(SSCK)}$
$t_{r(SSCK)}$	SSCK clock rising time	Master				1	t_{CYC} (1)
		Slave				1	µs
$t_{f(SSCK)}$	SSCK clock falling time	Master				1	t_{CYC} (1)
		Slave				1	µs
$t_{su(SSIO-SSCK)}$	SSO, SSI data input setup time			100			ns
$t_{h(SSCK-SSIO)}$	SSO, SSI data input hold time			1			t_{CYC} (1)
$t_{su(SCS-SSCK)}$	$\overline{SCS}$ setup time	Slave		1 t_{CYC} + 50 (1)			ns
$t_{h(SSCK-SCS)}$	$\overline{SCS}$ hold time	Slave		1 t_{CYC} + 50 (1)			ns
$t_{d(SSCK-SSIO)}$	SSO, SSI data output delay time	Master				1	t_{CYC} (1)
		Slave				80	ns
$t_{en(SCS-SSI)}$	SSI output enable time		3.0 V ≤ V_{CC} ≤ 5.5 V			1.5 t_{CYC} + 100 (1)	ns
$t_{dis(SCS-SSI)}$	SSI output disable time		3.0 V ≤ V_{CC} ≤ 5.5 V			1.5 t_{CYC} + 100 (1)	ns

Note:
1. 1 t_{CYC} is 1/f1 (s).

K-Version, V_{CC} = 3 V

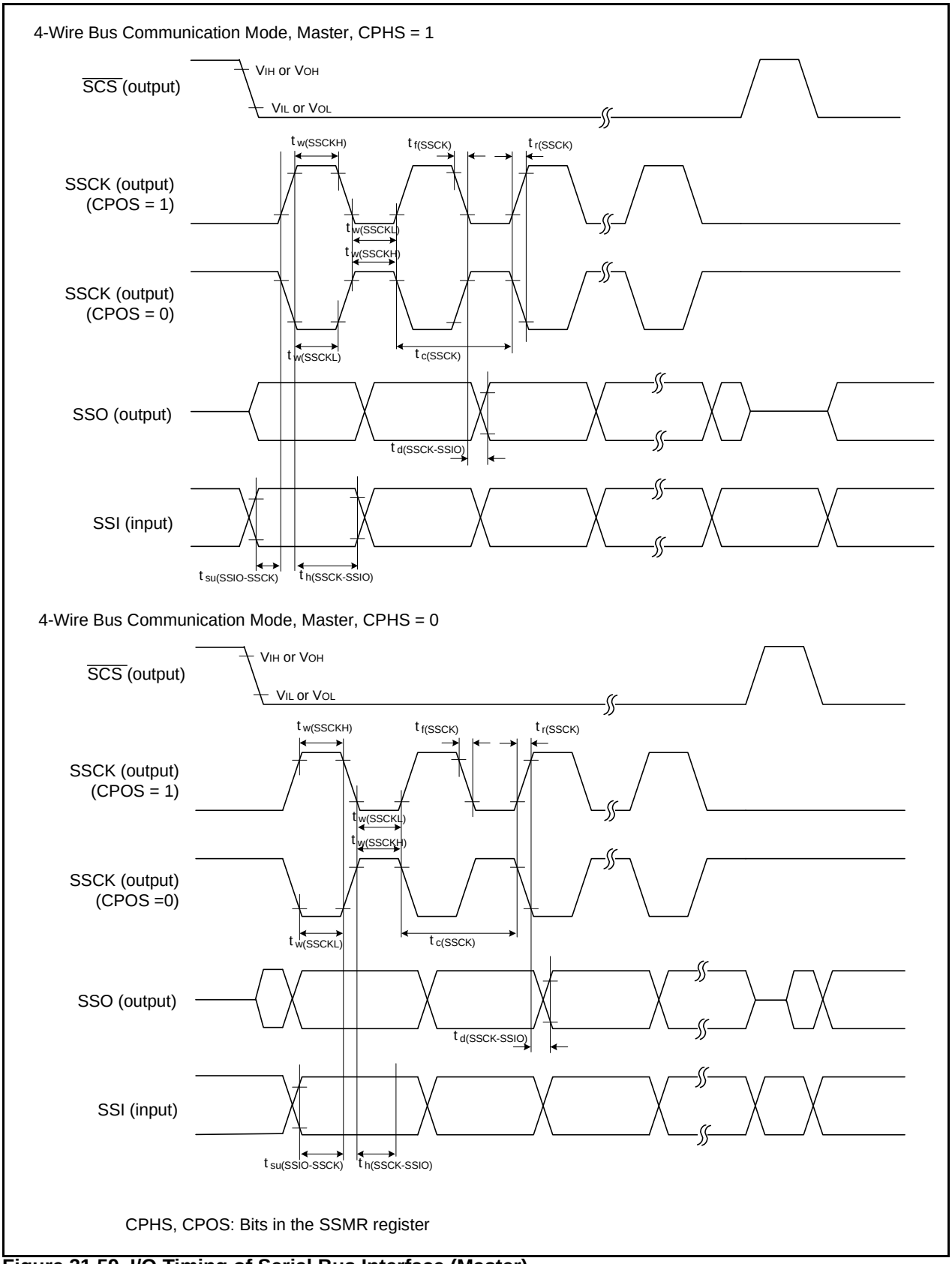


Figure 31.59 I/O Timing of Serial Bus Interface (Master)

K-Version, V_{CC} = 3 V

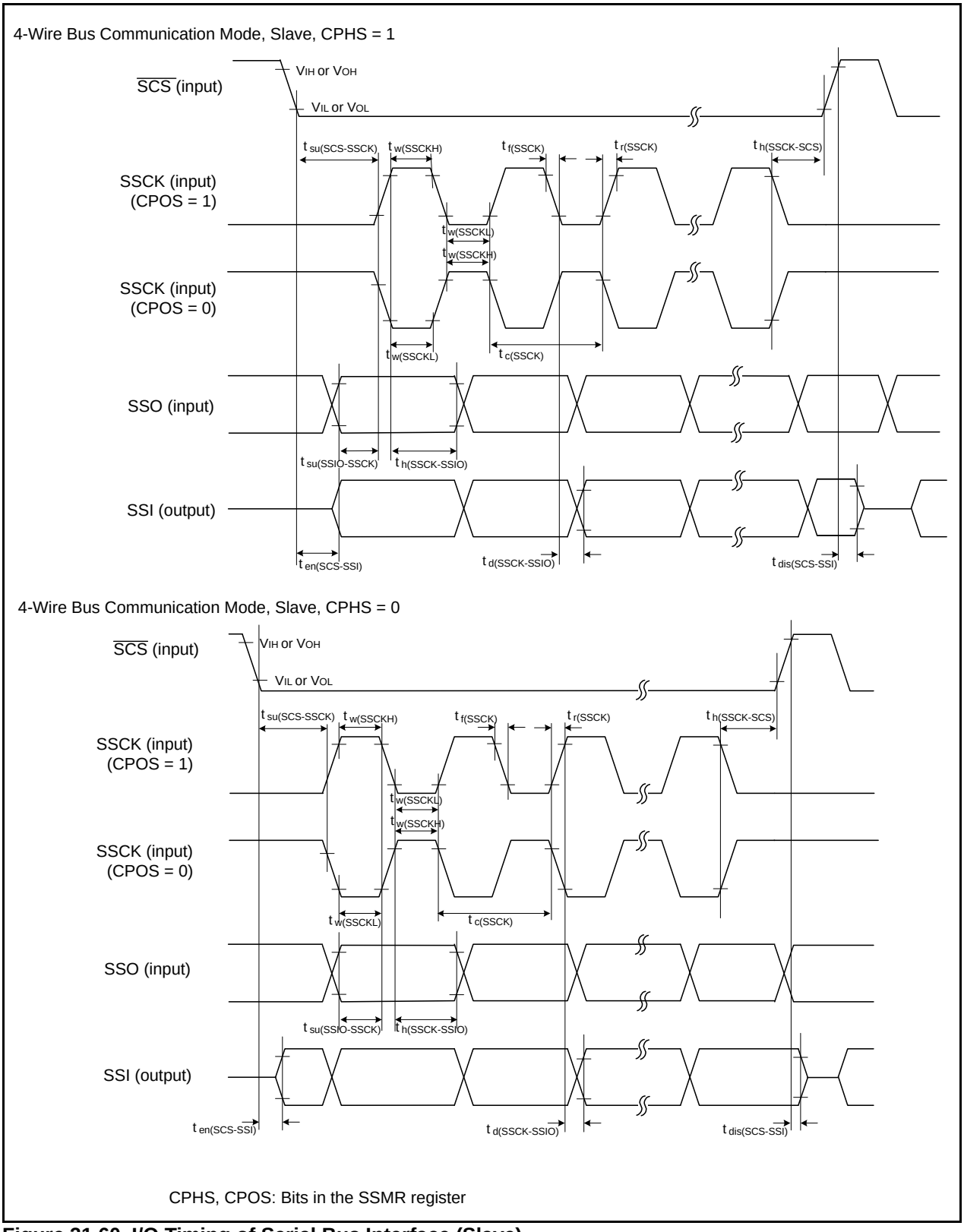


Figure 31.60 I/O Timing of Serial Bus Interface (Slave)

K-Version, V_{CC} = 3 V

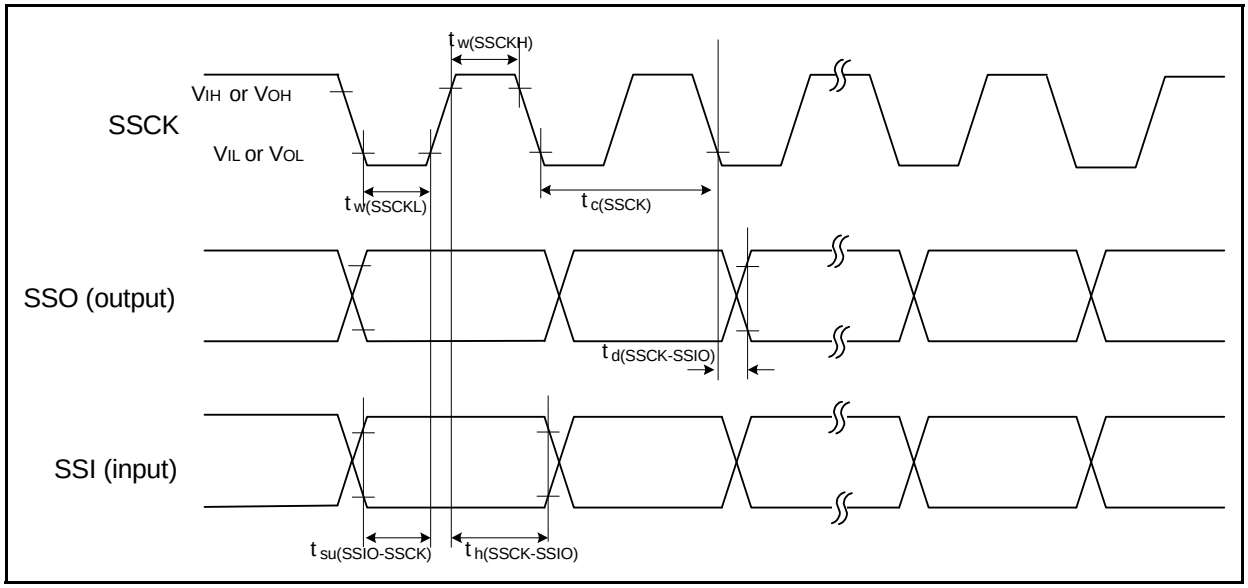


Figure 31.61 I/O Timing of Serial Bus Interface (Synchronous Communication Mode)

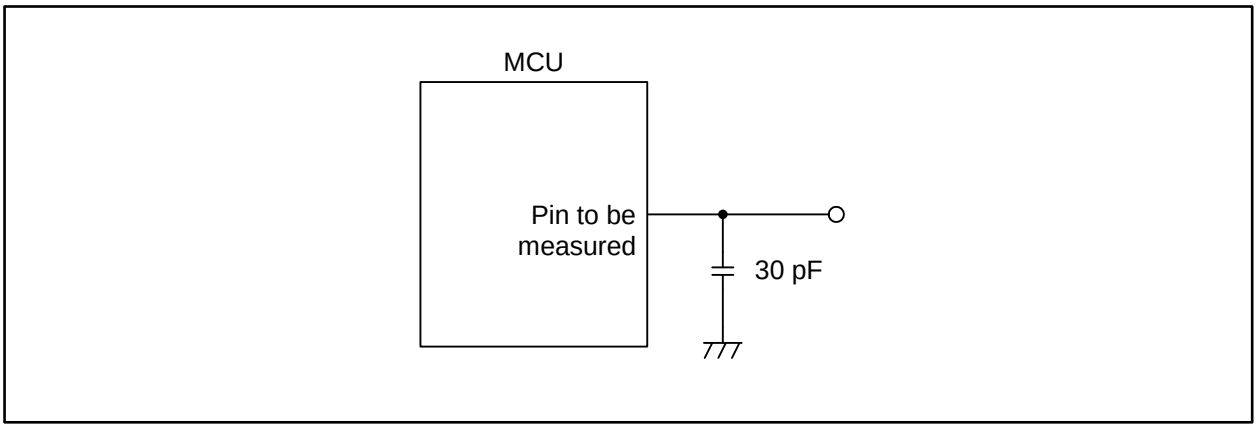


Figure 31.62 Switching Characteristic Measurement Circuit

32. Usage Notes

32.1 Notes on Noise

Connect a bypass capacitor (approximately 0.1 µF) across pins VCC and VSS using the shortest and thickest possible wiring. Figure 32.1 shows the Bypass Capacitor Connection.

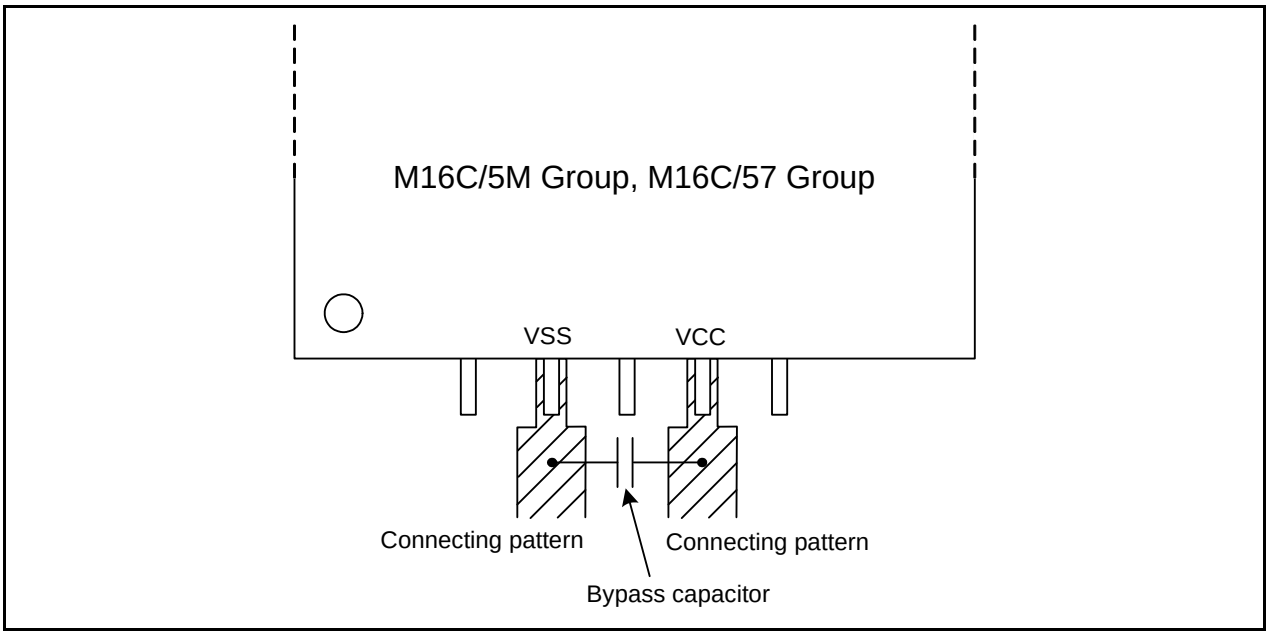


Figure 32.1 Bypass Capacitor Connection

32.2 Notes on SFRs

32.2.1 Register Settings

Table 32.1 lists Registers with Write-Only Bits and registers whose function differs between reading and writing. Set these registers with immediate values. Do not use read-modify-write instructions. When establishing the next value by altering the existing value, write the existing value to the RAM as well as to the register. Transfer the next value to the register after making changes in the RAM.
Read-modify-write instructions can be used when writing to the no register bits.

Table 32.1 Registers with Write-Only Bits

Address	Register	Symbol
0249h	UART0 Bit Rate Register	U0BRG
024Bh to 024Ah	UART0 Transmit Buffer Register	U0TB
0259h	UART1 Bit Rate Register	U1BRG
025Bh to 025Ah	UART1 Transmit Buffer Register	U1TB
0269h	UART2 Bit Rate Register	U2BRG
026Bh to 026Ah	UART2 Transmit Buffer Register	U2TB
0299h	UART4 Bit Rate Register	U4BRG
029Bh to 029Ah	UART4 Transmit Buffer Register	U4TB
02A9h	UART3 Bit Rate Register	U3BRG
02ABh to 02AAh	UART3 Transmit Buffer Register	U3TB
02B6h	I2C0 Control Register 1	S3D0
02B8h	I2C0 Status Register 0	S10
0303h to 0302h	Timer A1-1 Register	TA11
0305h to 0304h	Timer A2-1 Register	TA21
0307h to 0306h	Timer A4-1 Register	TA41
030Ah	Three-Phase Output Buffer Register 0	IDB0
030Bh	Three-Phase Output Buffer Register 1	IDB1
030Ch	Dead Time Timer	DTT
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2
0327h to 0326h	Timer A0 Register	TA0
0329h to 0328h	Timer A1 Register	TA1
032Bh to 032Ah	Timer A2 Register	TA2
032Dh to 032Ch	Timer A3 Register	TA3
032Fh to 032Eh	Timer A4 Register	TA4
037Dh	Watchdog Timer Refresh Register	WDTR
037Eh	Watchdog Timer Start Register	WDTS
D4C9h	CAN1 Receive FIFO Pointer Control Register	C1RFPCR
D4CBh	CAN1 Transmit FIFO Pointer Control Register	C1TFPCR
D7C9h	CAN0 Receive FIFO Pointer Control Register	C0RFPCR
D7CBh	CAN0 Transmit FIFO pointer Control Register	C0TFPCR

Table 32.2 Read-Modify-Write Instructions

Function	Mnemonic
Transfer	MOV*Dir*
Bit processing	BCLR, BM*Cnd*, BNOT, BSET, BTSTC, and BTSTS
Shifting	ROLC, RORC, ROT, SHA, and SHL
Arithmetic operation	ABS, ADC, ADCF, ADD, DEC, DIV, DIVU, DIVX, EXTS, INC, MUL, MULU, NEG, SBB, and SUB
Decimal operation	DADC, DADD, DSBB, and DSUB
Logical operation	AND, NOT, OR, and XOR
Jump	ADJNZ, SBJNZ

32.3 Notes on Protection

After setting the PRC2 bit to 1 (write enabled), by writing to a given SFR, the PRC2 bit becomes 0 (write disabled). Change the registers protected by the PRC2 bit in the next instruction after setting the PRC2 bit to 1. Make sure there are no interrupts or DMA transfers between the instruction that sets the PRC2 bit to 1 and the next instruction.

32.4 Notes on Resets

32.4.1 Power Supply Rising Gradient

When supplying power to the MCU, make sure that the power supply voltage applied to the VCC pin meets the SVCC conditions.

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
SVCC	Power supply rising gradient (VCC) (Voltage range: 0 to 2)	0.05			V/ms

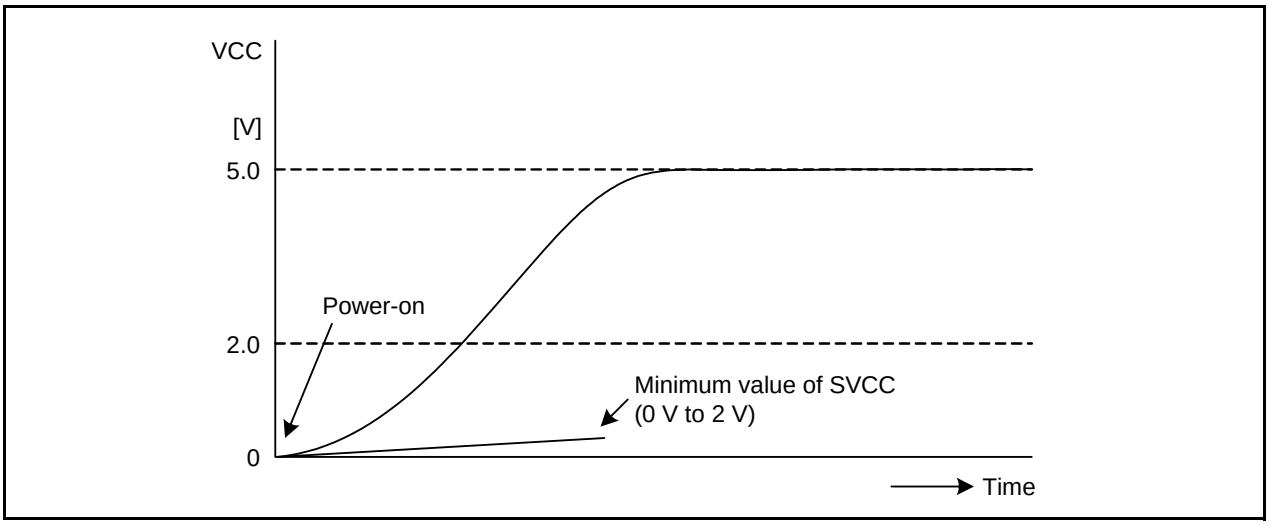


Figure 32.2 SVCC Timing

32.4.2 Power-On Reset

Use the voltage monitor 0 reset together with the power-on reset. To use the power-on reset, set the LVDAS bit in the OFS1 address to 0 (voltage monitor 0 reset enabled after hardware reset). In this case, the voltage monitor 0 reset is enabled (the VW0C0 bit and bit 6 in the VW0C register are 1, and the VC25 bit in the VCR2 register is 1) after power-on reset. Do not disable these bits by a program.

32.4.3 OSDR Bit (Oscillation Stop Detect Reset Detect Flag)

When an oscillator stop detect reset is generated, the MCU is reset and then stopped. This state is canceled by hardware reset or voltage monitor 0 reset.

Note that the OSDR bit in the RSTFR register is not affected by a hardware reset, but becomes 0 (not detected) from a voltage monitor 0 reset.

32.4.4 Hardware Reset When VCC < Vdet0

If a hardware reset is executed when the LVDAS bit in the OFS1 address is 0 (voltage monitor 0 reset enabled after hardware reset) and VCC < Vdet0, the MCU executes the program at the address indicated by the reset vector when changing the signal applied to the $\overline{\text{RESET}}$ pin from low to high. A voltage monitor 0 reset is not generated.

32.5 Notes on Clock Generator

32.5.1 Oscillator Using a Crystal or a Ceramic Resonator

To connect a crystal/ceramic resonator follow the instructions below:

- The oscillation characteristics are tied closely to the user's board design. Perform a careful evaluation of the board before connecting an oscillator.
- Oscillator structure depends on a crystal/ceramic resonator. The M16C/5M Group, M16C/57 Group MCUs contain a feedback resistor, but an additional external feedback resistor may be required. Contact the manufacturer of crystal/ceramic resonator regarding circuit constants, as they are dependent on the a crystal/ceramic resonator or stray capacitance of the mounted circuit.
- Check output from the CLKOUT pin to confirm that the clock generated by the oscillator is properly transmitted to the MCU.

The procedure for outputting a clock from the CLKOUT pin is listed below. Set the clock output from the CLKOUT pin to 25 MHz or lower.

Outputting the main clock

(1) Set the PRC0 bit in the PRCR register to 1 (write enabled).
(2) Set the CM11 bit in the CM1 register, the CM07 bit in the CM0 register, and the CM21 bit in the CM2 register all to 0 (main clock selected).
(3) Select the clock output from the CLKOUT pin (see the table below).
(4) Set the PRC0 bit in the PRCR register to 0 (write disabled).

Table 32.3 Output from CLKOUT Pin When Selecting Main Clock

Bit Setting		Output from the CLKOUT Pin
PCLKR register	CM0 register	
PCLK5 bit	Bits CM01 to CM00	
1	00b	Clock with the same frequency as the main clock
0	10b	Main clock divided by 8
0	11b	Main clock divided by 32

Outputting the sub clock

(1) Set the PRC0 bit in the PRCR register to 1 (write enabled).
(2) Set the CM07 bit in the CM0 register to 1 (sub clock selected).
(3) Set the PCLK5 bit in the PCLKR register to 0, and bits CM01 to CM00 in the CM0 register to 01b (fC output from CLKOUT pin).
(4) Set the PRC0 bit in the PRCR register to 0 (write disabled).

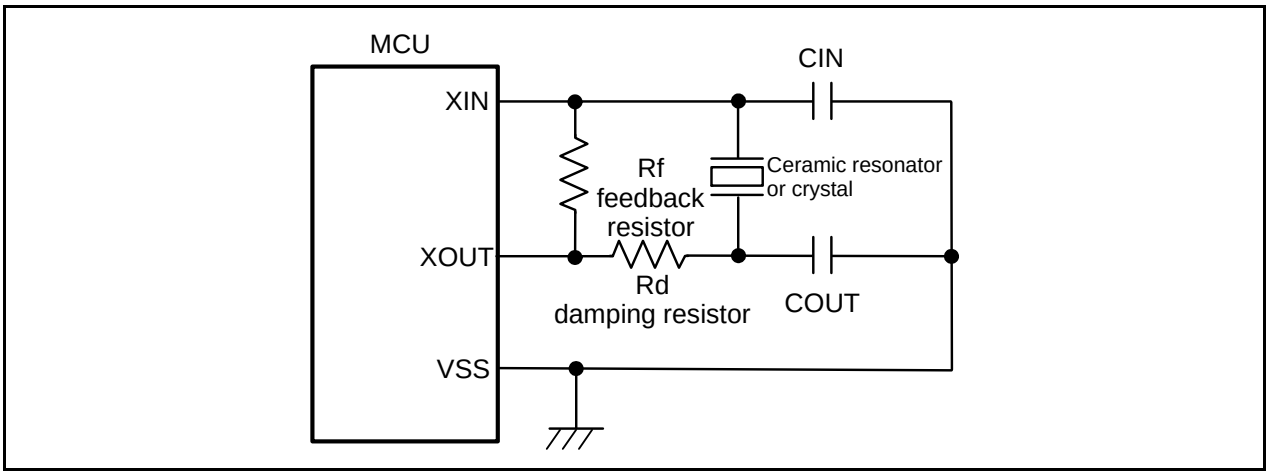


Figure 32.3 Oscillator Example

32.5.2 Noise Countermeasure

32.5.2.1 Clock I/O Pin Wiring

- Connect the shortest possible wiring to the clock I/O pin.
- Connect (a) the capacitor's ground lead connected to the crystal/ceramic resonator, and (b) the MCU's VSS pin, with the shortest possible wiring (maximum 20 mm).

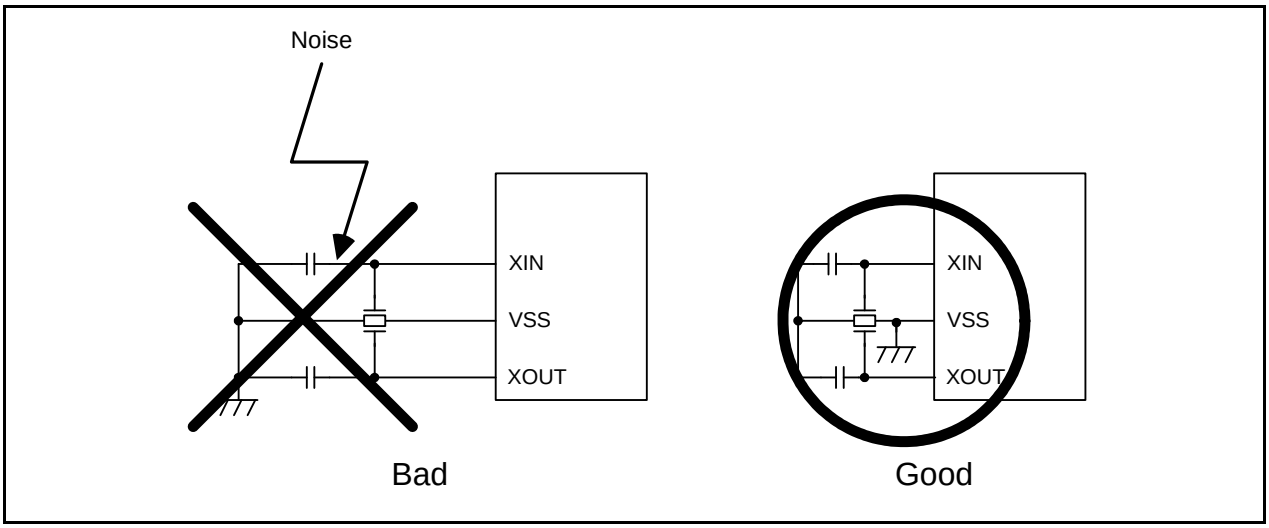


Figure 32.4 Clock I/O Pin Wiring

Reason:
When noise enters the clock I/O pin, the clock waveform becomes unstable, which causes an error in operation or a program runaway. Also, if a potential difference attributed to the noise occurs between the VSS level of the MCU and the VSS level of the crystal/ceramic resonator, an accurate clock is not input to the MCU.

32.5.2.2 Large Current Signal Line

For large currents that exceed the MCU's current range, wire the signal lines as far away from the MCU as possible (especially the crystal/ceramic resonator).

Reason:
In the system using the MCU, there are signal lines for controlling motors, LEDs, and thermal heads. When a large current flows through these signal lines, noise is generated due to mutual inductance.

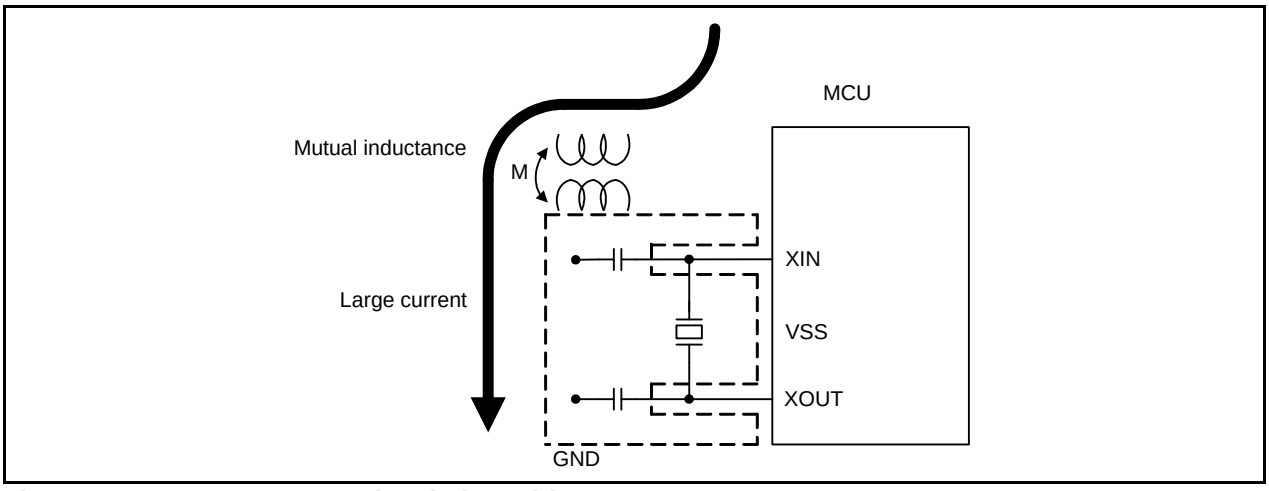


Figure 32.5 Large Current Signal Line Wiring

32.5.2.3 Signal Line Whose Level Changes at a High-Speed

For a signal line whose level changes at a high-speed, wire it as far away from the crystal/ceramic resonator and its wiring pattern as possible. Do not wire it across or extend it parallel to a clock-related signal line or other signal lines which are sensitive to noise.

Reason:
A signal whose level changes at a high-speed (such as the signal from the TAiOUT pin) affects other signal lines due to the level change at rising or falling edges. Specifically, when the signal line crosses the clock-related signal line, the clock waveform becomes unstable, which causes an error in operation or a program runaway.

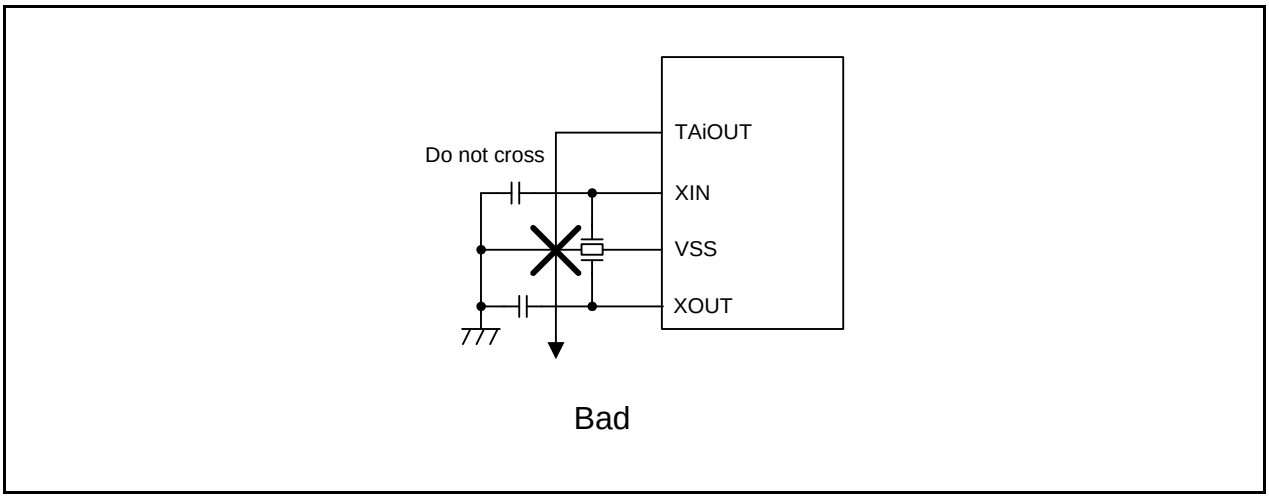


Figure 32.6 Wiring of Signal Line Whose Level Changes at High-Speed

32.5.3 CPU Clock

(Technical update number: TN-M16C-109-0309)
When an external clock is input from the XIN pin and the main clock is used as the CPU clock, do not stop the external clock.

32.5.4 Oscillator Stop/Restart Detect Function

- In the following cases, set the CM20 bit to 0 (oscillator stop/restart detect function disabled), and then change the setting of each bit.
  - When the CM05 bit is set to 1 (main clock stopped)
  - When the CM10 bit is set to 1 (stop mode)
- To enter wait mode while using the oscillator stop/restart detect function, set the CM02 bit to 0 (peripheral function clock f1 not turned off during wait mode).
- This function cannot be used if the main clock frequency is 2 MHz or lower. In that case, set the CM20 bit to 0 (oscillator stop/restart detect function disabled).
- While the CM27 bit is 1 (oscillation stop/restart detect interrupt), when the FRA01 bit is 1 (40 MHz on-chip oscillator selected), set the FRA00 bit to 1 (40 MHz on-chip oscillator on). (Do not set the FRA00 bit to 0 while FRA01 bit is 1, and vice versa.)

32.5.5 PLL Frequency Synthesizer

To use the PLL frequency synthesizer, stabilize the supply voltage within the acceptable range of power supply ripple.

Table 32.4 Acceptable Range of Power Supply Ripple

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$f_{(ripple)}$	Power supply ripple allowable frequency (VCC)				10	kHz
$V_{P-P(ripple)}$	Power supply ripple allowable amplitude voltage	(VCC = 5 V)			0.5	V
		(VCC = 3 V)			0.3	V
$V_{CC(\lvert\Delta V/\Delta T\rvert)}$	Power supply ripple rising/falling gradient	(VCC = 5 V)			0.3	V/ms
		(VCC = 3 V)			0.3	V/ms

f(ripple)
Power supply ripple allowable frequency (VCC)

Vp-p(ripple)
Power supply ripple allowable amplitude voltage

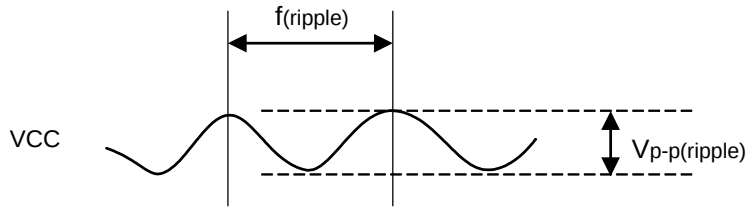


Figure 32.7 Voltage Fluctuation Timing

32.6 Notes on Power Control

32.6.1 CPU Clock

When switching the CPU clock source, wait until oscillation of the switched clock source is stable. After exiting stop mode, wait until oscillation stabilizes before changing the division.

32.6.2 Wait Mode

- Insert four or more NOP instructions following the WAIT instruction. When entering wait mode, because the instruction queue prefetches instructions that follow the WAIT instruction, prefetched instructions are sometimes executed prior to the interrupt routine used to exit wait mode. As shown below, when the instruction to set the I flag to 1 is allocated just before the WAIT instruction, interrupt requests are not accepted before the WAIT instruction is executed.

  The following is an example program for entering wait mode:

```
Program Example: FSET    I          ;
                 WAIT               ; Enter wait mode
                 NOP                ; Insert at least four NOP instructions
                 NOP
                 NOP
                 NOP
```

- Do not enter wait mode from PLL operating mode. To enter wait mode from PLL operating mode, first enter medium-speed mode, then set the PLC07 bit to 0 (PLL off).
- Do not enter wait mode from low current consumption read mode. To enter wait mode from low current consumption read mode, set the FMR23 bit in the FMR2 register to 0 (low current consumption read mode disabled).
- Do not enter wait mode from CPU rewrite mode. To enter wait mode from CPU rewrite mode, first set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled), then disable the DMA transfer.
- Set the PLC07 bit in the PLC0 register to 0 (PLL off). When the PLC07 bit is 1 (PLL on), current consumption cannot be reduced even in wait mode.

32.6.3 Stop Mode

- When exiting stop mode by a hardware reset, drive the $\overline{\text{RESET}}$ pin low for 20 fOCO-S cycles or more.
- Set the MR0 bit in the TAiMR register (i = 0 to 4) to 0 (pulse not output) when using timer A to exit stop mode.
- When entering stop mode, insert a JMP.B instruction immediately after executing an instruction that sets the CM10 bit in the CM1 register to 1 (stop mode), and then insert at least four NOP instructions. When entering stop mode, the instruction queue reads ahead the instructions following the instruction which sets the CM10 bit to 1. Thus, some of the instructions may be executed before the MCU enters stop mode or before the interrupt routine for returning from stop mode. As shown below, when the instruction to set the I flag to 1 is allocated just before the instruction to set the CM10 bit to 1, interrupt requests are not accepted before entering stop mode.

The following is an example program for entering stop mode:

```
Program Example:  FSET   I
                  BSET   0, CM1   ; Enter stop mode
                  JMP.B  L2       ; Insert a JMP.B instruction
          L2:
                  NOP             ; At least four NOP instructions
                  NOP
                  NOP
                  NOP
```

- The CLKOUT pin outputs a high-level signal in stop mode. Thus, if stop mode is entered right after output on the CLKOUT pin changes state from high to low, the low-level duration of the output signal to the CLKOUT pin becomes shorter.

- Do not enter stop mode from PLL operating mode. To enter stop mode from PLL operating mode, first enter medium-speed mode, then set the PLC07 bit to 0 (PLL off).
- Do not enter stop mode from low current consumption read mode. To enter stop mode from low current consumption read mode, set the FMR23 bit in the FMR2 register to 0 (low current consumption read mode disabled).
- Do not enter stop mode from CPU rewrite mode. To enter stop mode from CPU rewrite mode, first set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled), then disable the DMA transfer.
- Do not enter stop mode when the oscillator stop/restart detect function is enabled. To enter stop mode, set the CM20 bit in the CM2 register to 0 (oscillator stop/restart detect function disabled).
- Do not enter stop mode when the FMR01 bit is 1 (CPU rewrite mode enabled), and do not enter stop mode when the flash memory is stopped (bits FMR01 and FMSTP are 1).

32.6.4 Low Current Consumption Read Mode

- Enter low current consumption read mode through slow read mode (see Figure 9.4 “Setting and Canceling Low Current Consumption Read Mode” for details).
- When the FMR23 bit in the FMR2 register is 1 (low current consumption read mode enabled), do not set the FMSTP bit to 1 (flash memory stopped). Also, when the FMSTP bit is 1, do not set the FMR23 bit to 1.
- When the FMR01 bit in the FMR0 register to 1 (CPU rewrite mode enabled), do not set the FMR23 bit in the FMR2 register to 1 (low current consumption read mode enable).

32.6.5 Slow Read Mode

- When the FMR01 bit in the FMR0 register to 1 (CPU rewrite mode enabled), do not set the FMR22 bit in the FMR2 register to 1 (slow read mode enabled).

32.7 Notes on Programmable I/O Ports

Note

The 80-pin package has no P4_0 to P4_7, P5_0 to P5_7, P9_4.
The 64-pin package has no P0_4 to P0_7, P1_0 to P1_4, P3_4 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P9_4 to P9_7.

32.7.1 Pin Assignment Control

Bits PACR2 to PACR0 in the PACR register are 000b after reset. Set 010b (64-pin package), 011b (80-pin package) or 100b (100-pin package) to select the pin package, depending on the product.
After setting bits PACR2 to PACR0, set the programmable I/O ports and I/O pins for peripherals.

32.7.2 Influence of $\overline{SD}$

When a low-level signal is applied to the $\overline{SD}$ pin while the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on $\overline{SD}$ pin enabled), the following pins become high-impedance: P7_2/CLK2/TA1OUT/V/RXD1, P7_3/$\overline{CTS2}$/$\overline{RTS2}$/TA1IN/$\overline{V}$/TXD1, P7_4/TA2OUT/W/LIN0OUT, P7_5/TA2IN/$\overline{W}$/LIN0IN, P8_0/TA4OUT/U/TSUDA, P8_1/TA4IN/$\overline{U}$/TSUDB

32.7.3 Input Voltage Threshold

The input threshold voltage differs in the programmable I/O port and peripherals. When the programmable I/O port and peripheral is sharing the same pin, and the pin input level is lower than VIH and higher than VIL (input voltage is neither high or low), the input signal voltage level may be determined differently between the programmable I/O port and peripheral because the input voltage thresholds for those two are not necessarily the same.

32.8 Notes on Interrupts

32.8.1 Reading Address 00000h

Do not read address 00000h by a program. When a maskable interrupt request is accepted, the CPU reads interrupt information (interrupt number and interrupt request priority level) from address 00000h during the interrupt sequence. At this time, the IR bit of the accepted interrupt is cleared to 0 (interrupt not requested).

If address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts becomes 0. This may cause problems such as interrupts being canceled or an unexpected interrupt request being generated.

32.8.2 SP Setting

Set a value in the SP (USP, ISP) before accepting an interrupt. The SP (USP, ISP) is set to 0000h after reset. Therefore, if an interrupt is accepted before setting a value in the SP (USP, ISP), the program may go out of control.

Set a value in the ISP at the beginning of the program. For the first instruction after reset only, all interrupts are disabled.

32.8.3 $\overline{\text{NMI}}$ Interrupt

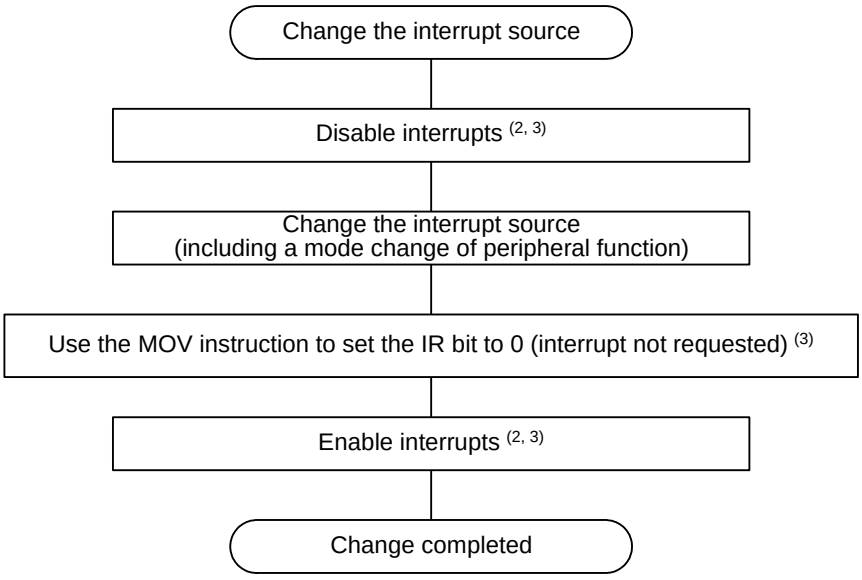
- When not using the $\overline{\text{NMI}}$ interrupt, set the PM24 bit in the PM2 register to 0 ($\overline{\text{NMI}}$ interrupt disabled).
- The $\overline{\text{NMI}}$ interrupt is disabled after reset. The $\overline{\text{NMI}}$ interrupt is enabled by setting the PM24 bit in the PM2 register to 1. Set the PM24 bit to 1 when a high-level signal is applied to the $\overline{\text{NMI}}$ pin. When the PM24 bit is set to 1 while a low-level signal is applied, an $\overline{\text{NMI}}$ interrupt is generated. Once the $\overline{\text{NMI}}$ interrupt is enabled, it cannot be disabled until the MCU is reset.
- The MCU cannot enter stop mode while the PM24 bit is 1 ($\overline{\text{NMI}}$ interrupt enabled) and input on the $\overline{\text{NMI}}$ pin is low. When input on the $\overline{\text{NMI}}$ pin is low, the CM10 bit in the CM1 register is fixed to 0.
- Do not enter wait mode while the PM24 bit is 1 ($\overline{\text{NMI}}$ interrupt enabled) and a low signal is input to the $\overline{\text{NMI}}$ pin. When the $\overline{\text{NMI}}$ pin is driven low, the CPU clock remains active even though the CPU stops, and therefore, the current consumption of the chip does not drop. In this case, the normal condition is restored by the next interrupt generation.
- Set the low- and high-level durations of the input signal to the $\overline{\text{NMI}}$ pin to 2 CPU clock cycles + 300 ns or more.

32.8.4 Changing an Interrupt Source

When the interrupt source is changed, the IR bit in the interrupt control register may become 1 (interrupt requested). To use an interrupt, change the interrupt source, and then set the IR bit to 0 (interrupt not requested).

In this section, the changing of an interrupt source refers to all elements used in changing the interrupt source, polarity, and timing assigned to each software interrupt number. Therefore, if a mode change of any peripheral function involves changing the source, polarity or timing of an interrupt, be sure to clear the IR bit for that interrupt to 0 (interrupt not requested) after making such changes. Refer to the descriptions of the individual peripheral functions for details of the interrupts.

Figure 32.8 shows the Procedure for Changing the Interrupt Generate Source.



IR bit: A bit in the interrupt control register

Notes:
1. Execute the above settings individually. Do not use one instruction to execute two or more settings simultaneously.
2. Use the I flag for the INTi interrupt (i = 0 to 7).
   For the interrupts from peripheral functions other than the INTi interrupt, disable the peripheral function that is the source of the interrupt so as not to generate an interrupt request before changing the interrupt source. In this case, if the maskable interrupts can all be disabled without causing a problem, use the I flag. Otherwise, use corresponding bits ILVL2 to ILVL0 in the interrupt control register whose interrupt source is to be changed.
3. Refer to 32.8.5 “Rewriting the Interrupt Control Register” for details about the instructions to be used and the notes to be taken for instruction execution.

Figure 32.8 Procedure for Changing the Interrupt Generate Source

32.8.5 Rewriting the Interrupt Control Register

To modify the interrupt control register, follow either of the procedures below:

- Modify in places where no interrupt requests corresponding to the interrupt control register may occur.
- If an interrupt request can be generated, disable that interrupt and then rewrite the interrupt control register.

When using the I flag to disable an interrupt, set the I flag as shown in the sample program code below. (Refer to 32.8.6 “Instruction to Rewrite the Interrupt Control Register” for rewriting the interrupt control registers using the sample program code.)

Examples 1 through 3 show how to prevent the I flag from becoming 1 (interrupt enabled) before the contents of the interrupt control register is rewritten, owing to the effects of the internal bus and the instruction queue buffer.

Example 1: Using the NOP instruction to pause the program until the interrupt control register is modified

```
INT_SWITCH1:
    FCLR    I               ; Disable interrupts.
    AND.B   #00H, 0055H     ; Set the TA0IC register to 00h.
    NOP                     ;
    NOP
    FSET    I               ; Enable interrupts.
```

Example 2: Using a dummy read to delay the FSET instruction

```
INT_SWITCH2:
    FCLR    I               ; Disable interrupts.
    AND.B   #00H, 0055H     ; Set the TA0IC register to 00h.
    MOV.W   MEM, R0         ; Dummy read.
    FSET    I               ; Enable interrupts.
```

Example 3: Using the POPC instruction to change the I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I               ; Disable interrupts.
    AND.B   #00H, 0055H     ; Set the TA0IC register to 00h.
    POPC    FLG             ; Enable interrupts.
```

32.8.6 Instruction to Rewrite the Interrupt Control Register

- Do not use the BTSTC and BTSTS instructions to rewrite the interrupt control registers.
- Use the AND, OR, BCLR, BSET, or MOV instruction to rewrite interrupt control registers.
  When an interrupt request is generated for the register being rewritten while executing an AND, OR, BCLR, or BSET instruction, the IR bit becomes 1 (interrupt requested) and remains 1.

32.8.7 $\overline{\text{INT}}$ Interrupt

- Either a low level of at least tw(INL) width or a high level of at least tw(INH) width is necessary for the signal input to pins $\overline{\text{INT0}}$ through $\overline{\text{INT7}}$, regardless of the CPU operation clock.
- If the POL bit in registers INT0IC to INT5IC or bits IFSR7 to IFSR0 in the IFSR register are changed, the IR bit may inadvertently become 1 (interrupt requested). Be sure to set the IR bit to 0 (interrupt not requested) after changing any of these register bits.
- If the POL bit in registers INT6IC to INT7IC, bits IFSR31 to IFSR30 in the IFSR3A register, or bits IFSR45 to IFSR44 in the IFSR4A register are changed, the IR bit may inadvertently become 1 (interrupt requested). Set the IR bit to 0 (interrupt not requested) after changing these bits.

32.9 Notes on the Watchdog Timer

After the watchdog timer interrupt is generated, use the WDTR register to refresh the watchdog timer counter.

32.10 Notes on DMAC

32.10.1 Write to the DMAE Bit in the DMiCON Register (i = 0 to 3)

(Technical update number: TN-M16C-92-0306)
When both of the following conditions are met, follow steps (1) and (2) below.

Conditions

- Write 1 (DMAi is in active state) to the DMAE bit when it is 1.
- A DMA request may be generated simultaneously when writing to the DMAE bit.

Steps

(1) Set bits DMAE and DMAS in the DMiCON register to 1 simultaneously. (1)
(2) Make sure the DMAi circuit is in an initialized state (2) by a program.
If DMAi is not in an initialized state, repeat these two steps.

Notes:

1. The DMAS bit does not change even if set to 1. However, it becomes 0 when set to 0 (DMA not requested). Therefore, when writing to the DMiCON register to set the DMAE bit to 1, set the value to be written to the DMAS bit to 1 to retain its state immediately before writing.
   Similarly, when writing to the DMAE bit with a read-modify-write instruction, set the DMAS bit to 1 to retain the DMA request that was generated while executing the instruction.
2. Read the TCRi register to verify whether DMAi is in an initialized state.
   If the read value is equal to the value that was written to the TCRi register before the DMA transfer started, DMAi is in an initialized state. When a DMA request is generated after writing to the DMAE bit, the read value is a value written to the TCRi register minus 1. If the read value is a value in the middle of a transfer, DMAi is not in an initialized state.

32.10.2 Changing the DMA Request Source

When the DMS bit or any of bits from DSEL4 to DSEL0 in the DMiSL register is changed, the DMAS bit in the DMiCON sometimes becomes 1 (DMA requested). Set the DMAS bit to 0 (DMA not requested) after changing the DMS bit or bits DSEL4 to DSEL0 in the DMiSL register.

32.11 Notes on Timer A

32.11.1 Common Notes on Multiple Modes

32.11.1.1 Register Setting

The timer stops after reset. Set the mode, count source, counter value, etc., using registers TAiMR, TAi, TAi1, UDF, TRGSR, PWMFS, TACS0 to TACS2, TAPOFS, TCKDIVC0, PCLKR, and bits TAZIE, TA0TGL, and TA0TGH in the ONSF register before setting the TAiS bit in the TABSR register to 1 (count started) (i = 0 to 4).

Set the TCDIV00 bit in the TCKDIVC0 register before setting other registers associated with timer A. After changing the TCDIV00 bit, set other registers associated with timer A again.

Always make sure registers TAiMR, UDF, TRGSR, PWMFS, TACS0 to TACS2, TAPOFS, TCKDIVC0, PCLKR, and bits TAZIE, TA0TGL, TA0TGH in the ONSF register are modified while the TAiS bit is 0 (count stopped), regardless of whether after reset or not.

32.11.1.2 Event or Trigger

When bits TAiTGH to TAiTGL in the registers ONSF or TRGSR are 01b, 10b, or 11b, an event or a trigger occurs when an interrupt request of the selected timer is generated. An event or trigger occurs while an interrupt is disabled because an interrupt request signal is generated regardless of the I flag, IPL, or interrupt control registers.

For some modes of the timers selected using bits TAiTGH to TAiTGL, an interrupt request is generated by a source other than overflow or underflow.

For example, when using pulse-period measurement mode or pulse-width measurement mode in timer B2, an interrupt request is generated at an active edge of the measurement pulse. For details, refer to the “Interrupt request generation timing” in each mode’s specification table.

32.11.1.3 Influence of $\overline{SD}$

When a low-level signal is applied to the $\overline{SD}$ pin while the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on $\overline{SD}$ pin enabled), the following pins become high-impedance: P7_2/CLK2/TA1OUT/V/RXD1, P7_3/$\overline{CTS2}$/$\overline{RTS2}$/TA1IN/$\overline{V}$/TXD1, P7_4/TA2OUT/W/LIN0OUT, P7_5/TA2IN/$\overline{W}$/LIN0IN, P8_0/TA4OUT/U/TSUDA, P8_1/TA4IN/$\overline{U}$/TSUDB

32.11.2 Timer A (Timer Mode)

32.11.2.1 Reading the Timer

The counter value can be read from the TAi register at any time while counting. However, if the counter is read at the same time as it is reloaded, the read value is FFFFh. Also, if the counter is read before it starts counting, or after a value is set in the TAi register while not counting, the set value is read.

32.11.3 Timer A (Event Counter Mode)

32.11.3.1 Reading the Timer

While counting, the counter value can be read at any time by reading the TAi register. However, while reloading, FFFFh can be read in underflow, and 0000h in overflow. When the counter is read before it starts counting and after a value is set in the TAi register while not counting, the set value is read.

32.11.4 Timer A (One-Shot Timer Mode)

32.11.4.1 Stop While Counting

When setting the TAiS bit to 0 (count stopped), the following occurs:

- The counter stops counting and reload register values are reloaded.
- The TAiOUT pin outputs a low-level signal when the POFSi bit in the TAPOFS register is 0, and outputs a high-level signal when it is 1.
- After one cycle of the CPU clock, the IR bit in the TAiIC register becomes 1 (interrupt requested).

32.11.4.2 Delay between the Trigger Input and Timer Output

As the one-shot timer output is synchronized with an internally generated count source, when an external trigger is selected, a maximum 1.5 cycle delay of the count source occurs between the trigger input to the TAiIN pin and timer output.

32.11.4.3 Changing Operating Modes

The IR bit becomes 1 when the timer operating mode is set by any of the following:

- Selecting one-shot timer mode after reset
- Changing the operating mode from timer mode to one-shot timer mode
- Changing the operating mode from event counter mode to one-shot timer mode

To use the timer Ai interrupt (IR bit), set the IR bit to 0 after the changes listed above are made.

32.11.4.4 Retrigger

When a trigger occurs while counting, the counter reloads the reload register to continue counting after generating a retrigger and decrementing once. To generate a trigger while counting, generate a retrigger after at least one cycle of the timer count source has elapsed following the previous trigger. When an external trigger is generated, do not generate a retrigger for 300 ns before the count value becomes 0000h. The one-shot timer may stop counting.

32.11.5 Timer A (Pulse Width Modulation Mode)

32.11.5.1 Changing Operating Modes

The IR bit becomes 1 when setting a timer operating mode with any of the following:

- Selecting PWM mode or programmable output mode after reset
- Changing the operating mode from timer mode to PWM mode or programmable output mode
- Changing the operating mode from event counter mode to PWM mode or programmable output mode

To use the timer Ai interrupt (IR bit), set the IR bit to 0 by a program after the changes listed above are made.

32.11.5.2 Stop While Counting

When setting the TAiS bit to 0 (count stopped) during PWM pulse output, the following occur:
When the POFSi bit in the TAPOFS register is 0:

- Counting stops
- When the TAiOUT pin is high, the output level goes low and the IR bit becomes 1.
- When the TAiOUT pin is low, both the output level and the IR bit remain unchanged.

When the POFSi bit in the TAPOFS register is 1:

- Counting stops.
- When the TAiOUT pin output is low, the output level goes high and the IR bit is set to 1.
- When the TAiOUT pin output is high, both the output level and the IR bit remain unchanged.

32.11.6 Timer A (Programmable Output Mode)

32.11.6.1 Changing the Operating Mode

The IR bit becomes 1 when setting a timer operating mode with any of the following:

- Selecting PWM mode or programmable output mode after reset
- Changing the operating mode from timer mode to PWM mode or programmable output mode
- Changing the operating mode from event counter mode to PWM mode or programmable output mode

To use the timer Ai interrupt (IR bit), set the IR bit to 0 by a program after the changes listed above are made.

32.11.6.2 Stop While Counting

When setting the TAiS bit to 0 (count stopped) during pulse output, the following occur:
When the POFSi bit in the TAPOFS register is 0:

- Counting stops.
- When the TAiOUT pin is high, the output level goes low.
- When the TAiOUT pin is low, the output level remains unchanged.
- The IR bit remains unchanged.

When the POFSi bit in the TAPOFS register is 1:

- Counting stops
- When the TAiOUT pin output is low, the output level goes high.
- When the TAiOUT pin output is high, the output level remains unchanged.
- The IR bit remains unchanged.

32.12 Notes on Timer B

Note

Timers B3 to B5 are not available in the 64-pin and 80-pin packages. Do not use these timers with the 64-pin and 80-pin packages.

32.12.1 Common Notes on Multiple Modes

32.12.1.1 Register Setting

The timer is stopped after reset. Set the mode, count source, etc., using registers TBiMR, TBCS0 to TBCS3, TBi, TCKDIVC0, PCLKR, PPWFS1, and PPWFS2 before setting the TBiS bit in the TABSR or TBSR register to 1 (count started) (i = 0 to 5).
Rewrite registers TBiMR, TBCS0 to TBCS3, TCKDIVC0, PCLKR, PPWFS1, and PPWFS2 while the TBiS bit is 0 (count stopped), regardless of whether after reset or not.

32.12.2 Timer B (Timer Mode)

32.12.2.1 Reading the Timer

While counting, the counter value can be read at any time by reading the TBi register. However, FFFFh is read while reloading. When the counter is read before it starts counting and after a value is set in the TBi register while not counting, the set value is read.

32.12.3 Timer B (Event Counter Mode)

32.12.3.1 Reading the Timer

While counting, the counter value can be read at any time by reading the TBi register. However, FFFFh is read while reloading. When the counter is read before it starts counting and after a value is set in the TBi register while not counting, the set value is read.

32.12.3.2 Event

When the TCK1 bit in the TBiMR register is 1, an event occurs when an interrupt request of the selected timer is generated. An event or trigger occurs while an interrupt is disabled because an interrupt request signal is generated regardless of the I flag, IPL, or interrupt control registers.
When the timer selected by the TCK1 bit uses pulse-period measurement mode or pulse-width measurement mode, an interrupt request is generated at an active edge of the measurement pulse.

32.12.4 Timer B (Pulse Period/Pulse Width Measurement Modes)

32.12.4.1 MR3 Bit in the TBiMR Register

To clear the MR3 bit to 0 by writing to the TBiMR register while the TBiS bit is 1 (count started), be sure to set the same value as previously set to bits TMOD0, TMOD1, MR0, MR1, TCK0, and TCK1, and set bit 4 to 0.

32.12.4.2 Interrupts

The IR bit in the TBiIC register becomes 1 (interrupt requested) when an active edge of a measurement pulse is input, or timer Bi overflows (i = 0 to 5). The source of an interrupt request can be determined by setting the MR3 bit in the TBiMR register within the interrupt routine.
Use the IR bit in the TBiIC register to detect overflows only. Use the MR3 bit only to determine the interrupt source.

32.12.4.3 Event or Trigger

When timer Bi in pulse-period measurement mode or pulse-width measurement mode is used as an event or trigger for timer A or timer B other than timer Bi, an event or trigger occurs at both the overflow and active edge of the measurement pulse.

32.12.4.4 Operations between Count Start and the First Measurement

When a count is started and the first active edge is input, an undefined value is transferred to the reload register. At this time, a timer Bi interrupt request is not generated.

The value of the counter is undefined after reset. If the count is started in this state, the MR3 bit may become 1 and a timer Bi interrupt request may be generated after the count starts before an active edge is input. When a value is set in the TBi register while the TBiS bit is 0 (count stopped), the same value is written to the counter.

32.12.4.5 Pulse Period Measurement Mode

When an active edge and overflow are generated simultaneously, input is not recognized at the active edge because an interrupt request is generated only once. Use this mode so an overflow is not generated, or use pulse width measurement mode.

32.12.4.6 Pulse Width Measurement Mode

In pulse width measurement, pulse widths are measured successively. Check whether the measurement result is a high-level width or a low-level width in the user program.
When an interrupt request is generated, read the TBiIN pin level in the interrupt routine, and check whether it is the edge of an input pulse or overflow. The TBiIN pin level can be read from bits in the register of ports sharing a pin.

32.13 Notes on Three-Phase Motor Control Timer Function

32.13.1 Timer A and Timer B

Refer to 15.5 “Notes on Timer A” and 16.5 “Notes on Timer B”.

32.13.2 Influence of $\overline{SD}$

When a low-level signal is applied to the $\overline{SD}$ pin while the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on $\overline{SD}$ pin enabled), the following pins become high-impedance: P7_2/CLK2/TA1OUT/V/RXD1, P7_3/$\overline{CTS2}$/$\overline{RTS2}$/TA1IN/$\overline{V}$/TXD1, P7_4/TA2OUT/W/LIN0OUT, P7_5/TA2IN/$\overline{W}$/LIN0IN, P8_0/TA4OUT/U/TSUDA, P8_1/TA4IN/$\overline{U}$/TSUDB

32.14 Notes on Timer S

32.14.1 Register Access

The explanation for some bits and registers states, “the value written to this register or this bit is reflected to the internal circuit when the clock is synchronized with the base timer count source (fBT1)”. When writing these bits or registers, the written value is not reflected to the internal circuits immediately. After writing the value, prewrite operations are performed for up to one fBT1 cycle. When reading these bits or registers immediately after writing the value, the value before writing may be read.

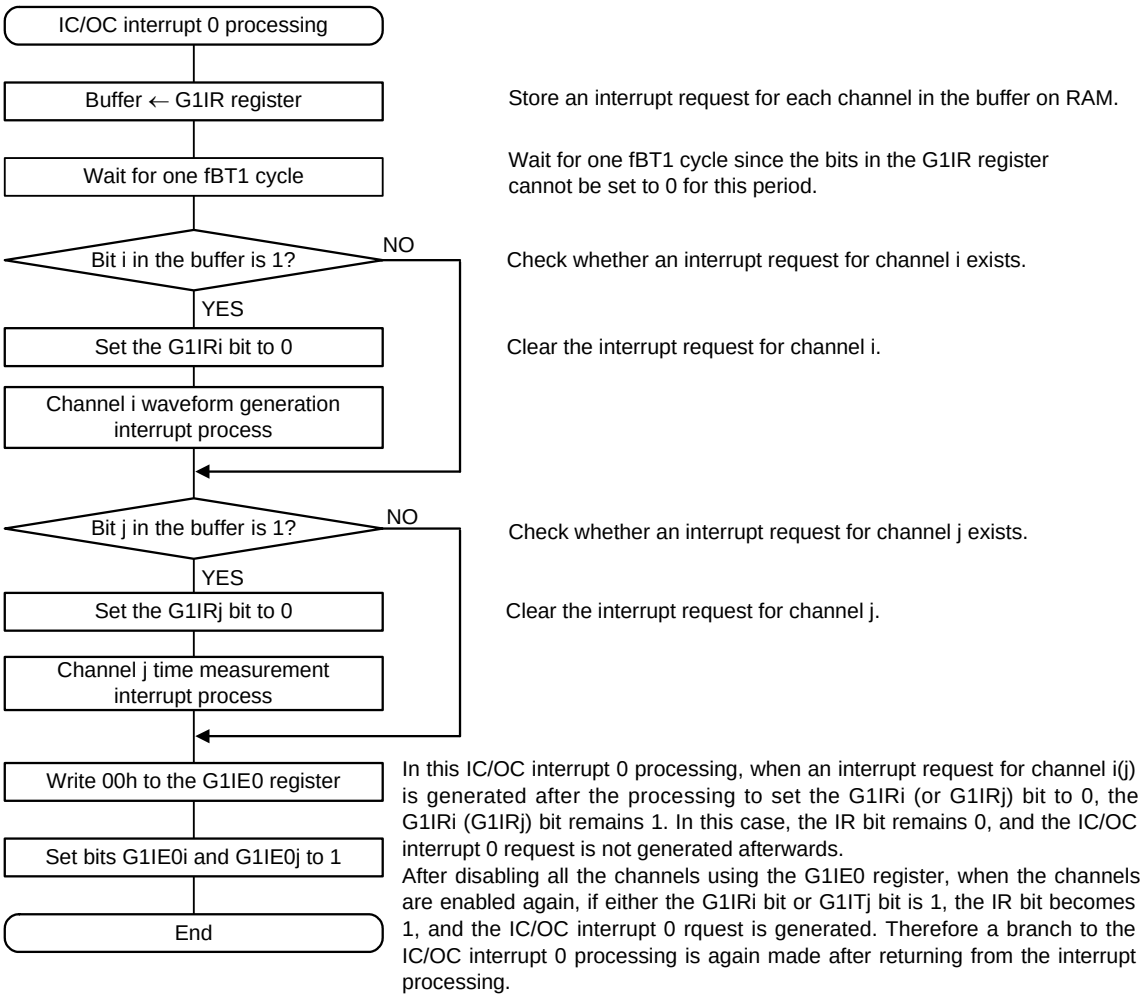
32.14.2 Changing the G1IR Register

Set the G1IRj bit in the G1IR register (j = 0 to 7) to 0 by a program since it does not become 0 automatically with an interrupt request reception.

However, the G1IRj bit cannot be set to 0 for one fBT1 cycle after this bit becomes 1. Wait for one or more fBT1 cycles after the G1IRj bit becomes 1, then set this bit to 0.

To write 0 to the G1IRj bit, use the AND and BCLR instructions to avoid deleting requests for other channels.

Figure 32.9 shows “IC/OC Interrupt 0 Operation Example”. As shown in the operation example, disable interrupt requests for all channels once at the last part of an interrupt process, then enable them again.



i = 0 to 7; j = 0 to 7 (however, j and i cannot be the same value)
G1IRi, G1IRj: Bits in the G1IR register
G1IE0i, G1IE0j: Bits in the G1IE0 register

The above assumes the following:
With IC/OC interrupt 0, a waveform generation interrupt is processed for channel i, and a time measurement interrupt for channel j.
Interrupt requests for the other channels are disabled with the G1IE0 register.

Figure 32.9 IC/OC Interrupt 0 Operation Example

32.14.3 Changing Registers ICOCiIC (i = 0, 1)

While the G1IEij bit in the G1IEi register is 1 (IC/OC interrupt 1 request enabled), use the AND, OR, BCLR, or BSET instruction to change bits ILVL2 to ILVL0 in the ICOCiIC register at the point where a channel j interrupt request may be generated (j = 0 to 7). The IR bit becomes 1 (interrupt requested) if a channel j interrupt is generated while executing these instructions.
If the MOV instruction is used to perform the above, when a channel j interrupt request is generated while executing the MOV instruction, the IR bit does not become 1, and the interrupt request is ignored. The G1IRj bit in the G1IR register becomes 1 (interrupt requested) at this timing. If the G1IRj remains 1, subsequent IC/OC interrupt i requests are not generated.

When timer S is initialized, change registers ICOCiIC after registers ICOCiIC and G1IR are both set to 00h.

32.14.4 Output Waveform During the Base Timer Reset with the BTS bit

When the BTS bit in the G1BCR1 register is set to 0 (base timer reset), the waveform output pin level remains as it is at that point. This output level is held until the base timer value matches the G1POj register value after the BTS bit is set to 1 (base timer starts counting).

32.14.5 OUTC1_0 Pin Output During the Base Timer Reset with the G1PO0 register

While the RST1 bit in the G1BCR1 register is set to 1 (the base timer is reset when the base timer matches the G1PO0 register), when the base timer matches the G1PO0 register, the base timer is reset after two fBT1 cycles. During the two fBT1 cycles from when the base timer value matches the G1PO0 register value to the base timer being reset, the OUTC1_0 pin is driven high. Thus set the EOC0 bit in the G1OER register to 1 (output disabled).

32.14.6 Interrupt Request When Selecting Time Measurement Function

When the FSCj bit (j = 0 to 7) in the G1FS register is set to 1, and the IFEj bit in the G1FE register is also set to 1, the G1IRj bit in the G1IR register, or the IR bits in registers ICOCiIC (i = 0, 1) or ICOCHjIC (j = 0 to 3) may become 1 (interrupt requested) after a maximum of two fBT1 cycles.
When using IC/OC interrupt i or IC/OC channel j interrupt, set bits FSCj and IFEj to 1, then perform the following:

(1) Wait for two or more fBT1 cycles.
(2) Set the IR bit in the ICOCiIC register and/or the ICOCHjIC register to 0.
(3) Wait for three or more fBT1 cycles after the time measurement function is selected. Set the G1IR register to 00h after setting the IR bit in the ICOCiIC register to 0.

32.15 Notes on Task Monitor Timer

32.15.1 Register Settings

After reset, the task monitor timer counter is stopped. After setting the counter value and count source by setting registers TMOS register and TMOSCS, set the TMOS0S bit in the TMOSSR register to 1 (start counting).
Change the TMOSCS register value when the TMOS0S bit is 0 (stop counting).

32.15.2 Reading the Timer

While the task monitor timer is counting, the counter value can be read at any given time by reading the TMOS register. However, when reading the counter at its reload timing, the value is read as FFFFh. When the task monitor timer stops counting and after setting the value to the TMOS register, the setting value can be read until the counter starts counting.

32.16 Notes on Real-Time Clock

32.16.1 Starting and Stopping the Count

The real-time clock uses the TSTART bit for instructing the count to start or stop, and the TCSTF bit which indicates count started or stopped. Bits TSTART and TCSTF are in the RTCCR1 register.

The real-time clock starts counting and the TCSTF bit becomes 1 (count started) when the TSTART bit is set to 1 (count started). It takes up to two cycles of the count source until the TCSTF bit becomes 1 after setting the TSTART bit to 1. During this time, do not access registers associated with the real-time clock (1) other than the TCSTF bit.

Similarly, when setting the TSTART bit to 0 (count stopped), the real-time clock stops counting and the TCSTF bit becomes 0 (count stopped). It takes up to three cycles of the count source until the TCSTF bit becomes 0 after setting the TSTART bit to 0. During this time, do not access registers associated with the real-time clock other than the TCSTF bit.

Note:

1. Registers associated with the real-time clock: RTCSEC, RTCMIN, RTCHR, RTCWK, RTCCR1, RTCCR2, RTCCSR, RTCCSEC, RTCCMIN, and RTCCHR.

32.16.2 Register Settings (Time Data, etc.)

Write to the following registers/bits when the real-time clock is stopped:

- Registers RTCSEC, RTCMIN, RTCHR, RTCWK, and RTCCR2
- Bits H12H24 and RTCPM in the RTCCR1 register
- Bits RCS0 to RCS4 in the RTCCSR register

The real-time clock is stopped when bits TSTART and TCSTF in the RTCCR1 register are 0 (real-time clock stopped).

Set the RTCCR2 register after setting the registers and bits mentioned above (immediately before the real-time clock count starts).

Figure 20.4 shows Time and Day Change Procedure (No Compare Mode or Compare Mode 1), and Figure 20.5 shows Time and Day Change Procedure (Compare Mode 2 or Compare Mode 3).

32.16.3 Register Settings (Compare Data)

Write to the following registers when the BSY bit in the RTCSEC register is 0 (not while data is updated).

- Registers RTCCSEC, RTCCMIN, and RTCCHR

32.16.4 Time Reading Procedure in Real-Time Clock Mode

In real-time clock mode, read time data bits (1) when the BSY bit in the RTCSEC register is 0 (not while data is updated).

When reading multiple registers, if data is rewritten between reading registers, an errant time will be read. To prevent this, use one of the following steps when reading:

- Using an interrupt
  In the real-time clock periodic interrupt routine, read the values necessary from the appropriate time data bits.
- Monitoring by a program 1
  Monitor the IR bit in the RTCTIC register by a program and read necessary values of time data bits after the IR bit becomes 1 (periodic interrupt requested).
- Monitoring by a program 2
  Read the time data according to Figure 32.10 “Time Data Reading”.

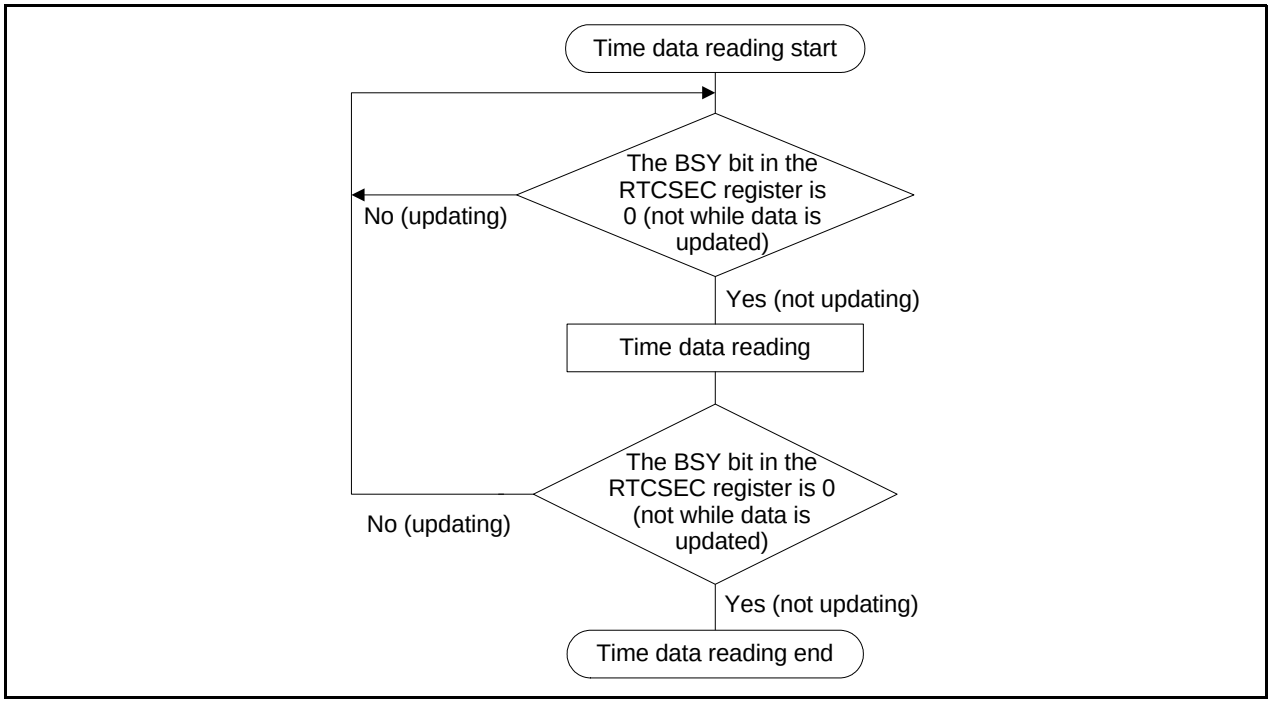


Figure 32.10 Time Data Reading

Also, when reading multiple registers, read them as continuously as possible.

Note:

1. Time data bits are as follows:
   Bits SC12 to SC10 and SC03 to SC00 in the RTCSEC register
   Bits MN12 to MN10 and MN03 to MN00 in the RTCMIN register
   Bits HR11 to HR10 and HR03 to HR00 in the RTCHR register
   Bits WK2 to WK0 in the RTCWK register
   The RTCPM bit in the RTCCR1 register

32.17 Notes on Serial Interface UARTi (i = 0 to 4)

Note

Pins CLK4, RXD4, and TXD4 do not exist in the 64-pin package. Do not access the UART4 associated registers.

32.17.1 Common Notes on Multiple Modes

32.17.1.1 Influence of $\overline{SD}$

When a low-level signal is applied to the $\overline{SD}$ pin while the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on $\overline{SD}$ pin enabled), the following pins become high-impedance: P7_2/CLK2/TA1OUT/V/RXD1, P7_3/$\overline{CTS2}$/$\overline{RTS2}$/TA1IN/$\overline{V}$/TXD1, P7_4/TA2OUT/W/LIN0OUT, P7_5/TA2IN/$\overline{W}$/LIN0IN, P8_0/TA4OUT/U/TSUDA, P8_1/TA4IN/$\overline{U}$/TSUDB

32.17.1.2 Register Setting

Set the OCOSEL0 or OCOSEL1 bit in the UCLKSEL0 register before setting other registers associated with UART0 to UART4. After changing the OCOSEL0 or OCOSEL1 bit, set other registers associated with UART0 to UART4 again.

32.17.2 Clock Synchronous Serial I/O Mode

32.17.2.1 Transmission/Reception

When the $\overline{RTS}$ function is used with an external clock, the $\overline{RTSi}$ pin (i = 0 to 3) outputs a low-level signal, which informs the transmitting side that the MCU is ready for a receive operation. The $\overline{RTSi}$ pin outputs a high-level signal when a receive operation starts. Therefore, transmit timing and receive timing can be synchronized by connecting the $\overline{RTSi}$ pin to the $\overline{CTSi}$ pin on the transmitting side. The $\overline{RTS}$ function is disabled when an internal clock is selected.

32.17.2.2 Transmission

If the transmission is started while an external clock is selected and the TXEPT bit in the UiC0 register (i = 0 to 4) is 1 (no data present in transmit register), meet the last requirement at either of the following timings:

External clock level:

- The CKPOL bit in the UiC0 register is 0 (transmit data is output at the falling edge of transmit/receive clock and receive data is input at the rising edge) and the external clock is high.
- The CKPOL bit is 1 (transmit data is output at the rising edge of transmit/receive clock and receive data is input at the falling edge) and the external clock is low.

Requirements to start transmission (in no particular order):

- The TE bit in the UiC1 register is 1 (transmission enabled).
- The TI bit in the UiC1 register is 0 (data present in the UiTB register).
- When the $\overline{CTS}$ function is selected, input on the $\overline{CTSi}$ pin is low.

32.17.2.3 Reception

In clock synchronous serial I/O mode, a shift clock is generated by activating a transmitter. Set the UARTi-associated registers for a transmit operation even if the MCU is used for a receive operations only. Dummy data is output from the TXDi pin (i = 0 to 4) while receiving.

When an internal clock is selected, a shift clock is generated by setting the TE bit in the UiC1 register to 1 (transmission enabled) and placing dummy data in the UiTB register. When an external clock is selected, set the TE bit to 1 (transmission enabled), set dummy data in the UiTB register, and input an external clock to the CLKi pin to generate a shift clock.

If data is received consecutively, an overrun error occurs when the RI bit in the UiC1 register is 1 (data present in the UiRB register) and the next receive data is received in the UARTi receive register. Then, the OER bit in the UiRB register becomes 1 (overrun error occurred). At this time, the UiRB register is undefined. When an overrun error occurs, program the transmitting and receiving sides to retransmit the previous data. If an overrun error occurs again, the IR bit in the SiRIC register remains unchanged.

To receive data consecutively, set dummy data in the low-order byte in the UiTB register for each receive operation.

If the reception is started while an external clock is selected and the TXEPT bit in the UiC0 register is 1 (no data present in transmit register), meet the last requirement at either of the timings below.

External clock level:

- The CKPOL bit in the UiC0 register is 0 (transmit data is output at the falling edge of transmit/receive clock and receive data is input at the rising edge) and the external clock is high.
- The CKPOL bit is 1 (transmit data is output at the rising edge of transmit/receive clock and receive data is input at the falling edge) and the external clock is low.

Requirements to start reception (in no particular order):

- The RE bit in the UiC1 register is 1 (reception enabled).
- The TE bit in the UiC1 register is 1 (transmission enabled).
- The TI bit in the UiC1 register is 0 (data present in the UiTB register).

32.17.3 Special Mode 1 (I^2C Mode)

32.17.3.1 Generating Start and Stop Conditions

(Technical update number: TN-16C-130A/EA)

When generating start, stop, and restart conditions, set the STSPSEL bit in the U2SMR4 register to 0 and wait for more than a half cycle of the transmit/receive clock. Then set each condition generation bit (STAREQ, RSTAREQ, and STPREQ) from 0 to 1.

32.17.3.2 IR Bit

Set the following bits first, and then set the IR bit in each UART2 interrupt control register to 0 (interrupt not requested).

Bits SMD2 to SMD0 in the U2MR register, the IICM bit in the U2SMR register, the IICM2 bit in the U2SMR2 register, the CKPH bit in the U2SMR3 register

32.17.3.3 Setup and Hold Times When Generating a Start/Stop Condition

When generating a start condition, the hold time (t_{HD}:STA) is a half cycle of the SCL clock. When generating a stop condition, the setup time (t_{SU}:STO) is a half cycle of the SCL clock.

When the SDA digital delay function is enabled, take delay time into consideration (see 21.3.3.7 “SDA Digital Delay”).

The following shows a calculation example of hold and setup times when generating a start/stop condition.

Calculation example when setting 100 kbps

- U2BRG count source: f1 = 20 MHz
- U2BRG register setting value: n = 100 - 1
- SDA digital delay setting value: DL2 to DL0 are 101b (5 or 6 cycles of U2BRG count source)

f_{SCL} (theoretical value) = f1 / (2(n+1)) = 20 MHz / (2 × (99 + 1)) = 100 kbps

t_{DL} = delay cycle count / f1 = 6 / 20 MHz = 0.3 μs

$t_{HD:STA}$ (theoretical value) = 1 / (2f_{SCL} (theoretical value)) = 1 / (2 × 100 kbps) = 5 μs

$t_{SU:STO}$ (theoretical value) = 1 / (2f_{SCL} (theoretical value)) = 1 / (2 × 100 kbps) = 5 μs

$f_{HD:STA}$ (actual value) = $t_{HD:STA}$ (theoretical value) - t_{DL} = 5 μs - 0.3 μs = 4.7 μs

$f_{SU:STO}$ (actual value) = $t_{SU:STO}$ (theoretical value) + t_{DL} = 5 μs + 0.3 μs = 5.3 μs

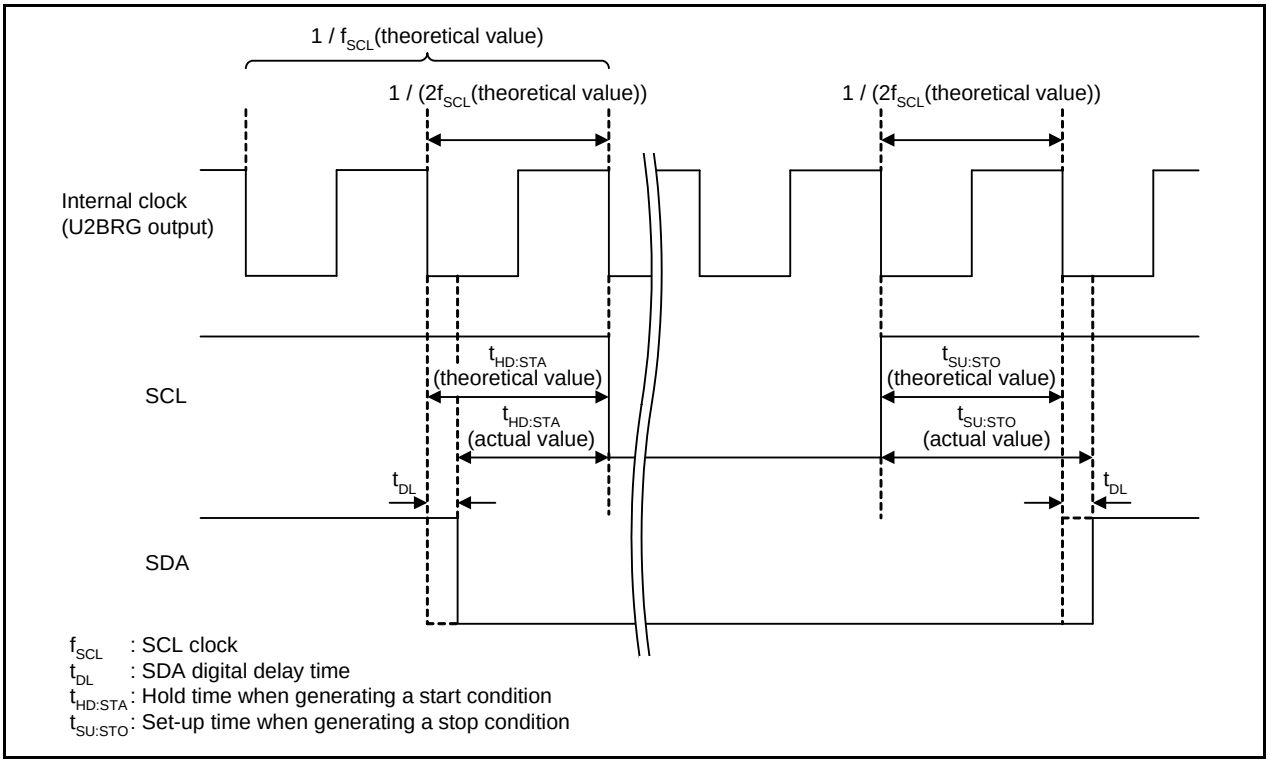


Figure 32.11 Setup and Hold Times When Generating Start and Stop Conditions

32.17.3.4 Restrictions on the Bit Rate When Using the U2BRG Count Source

In I^2C mode, set the U2BRG register to a value of 03h or greater.

A maximum of three U2BRG count source cycles are necessary until the internal circuit acknowledges the SCL clock level. The connectable I^2C-bus bit rate is one-third or less than the U2BRG count source speed. If a value between 00h to 02h is set to the U2BRG register, bit slippage may occur.

32.17.3.5 Restart Condition in Slave Mode

When a restart condition is detected in slave mode, the successive processes may not be executed correctly. In slave mode, do not use a restart condition.

32.17.3.6 Requirements to Start Transmission/Reception in Slave Mode

When transmission/reception is started in slave mode and the TXEPT bit in the UiC0 register is 1 (no data present in transmit register), meet the last requirement when the external clock is high.
Requirements to start transmission (in no particular order):

- The TE bit in the U2C1 register is 1 (transmission enabled).
- The TI bit in the U2C1 register is 0 (data present in the UiTB register).

Requirements to start reception (in no particular order):

- The RE bit in the U2C1 register is 1 (reception enabled).
- The TE bit in the U2C1 register is 1 (transmission enabled).
- The TI bit in the U2C1 register is 0 (data present in the UiTB register).

32.17.4 Special Mode 4 (SIM Mode)

(Technical update number: TN-M16C-101-0309)
After reset is deasserted, a transmit interrupt request is generated by setting bits U2IRS and U2ERE in the U2C1 register to 1 (transmission completed, error signal output), then setting the TE bit to 1 (transmission enabled) and the transmission data to the U2TB register. Therefore, when using SIM mode, make sure to set the IR bit to 0 (interrupt not requested) after setting these bits.

32.18 Notes on Multi-master I2C-bus Interface

32.18.1 Limitation on CPU Clock

When the CM07 bit in the CM0 register is 1 (CPU clock is a sub clock), do not access the registers listed in Table 22.4 “Registers”. Set the CM07 bit to 0 (main clock, PLL clock, or on-chip oscillator clock) to access these registers.

32.18.2 Register Access

Refer to the notes below when accessing the I2C interface control registers. The period from the rising edge of the first clock of the slave address or 1-byte data transmission/reception to the falling edge of an ACK clock is considered to be the transmission/reception period. When the ACKCLK bit is 0 (no ACK clock), the transmission/reception period is from the rising edge of the first clock of the slave address or 1-byte data transmission/reception to the falling edge of the eighth clock.

32.18.2.1 S00 Register

Do not write to the S00 register during transmission/reception.

32.18.2.2 S1D0 Register

Do not change bits other than the IHR bit in the S1D0 register during transmission/reception.

32.18.2.3 S20 Register

Do not change bits other than the ACKBIT bit in the S20 register during transmission/reception.

32.18.2.4 S3D0 Register

- Do not use the bit managing instruction (read-modify-write instruction) to access the S3D0 register. Use the MOV instruction to write to this register.
- Rewrite bits ICK1 and ICK0 when the ES0 bit in the S1D0 register is 0 (I2C interface disabled).

32.18.2.5 S4D0 Register

Rewrite bits ICK4 to ICK2 when the ES0 bit in the S1D0 register is 0 (I2C interface disabled).

32.18.2.6 S10 Register

- Do not use the bit managing instruction (read-modify-write instruction) to access the S10 register. Use the MOV instruction to write to this register.
- Do not write to the S10 register when bits MST and TRX change their values.

Refer to operation examples in 22.3 “Operations” for bits MST and TRX change.

32.19 Notes on Serial Bus Interface

32.19.1 SS0SR register

To write to the SS0SR register, perform the following:

- Use the MOV instruction.
- Read the register once, insert four or more NOP instructions, then write to the register.
- Write 1 to bits which are not set to 0 (bits to which 1 is written will not be changed).

Example of setting the ORER bit (b2) in the SS0SR register to 0

```
MOV.B SS0SR, MEM          ;Read the SS0SR register
NOP                       ;Insert four or more NOP instructions
NOP
NOP
NOP
MOV.B #11100001b, SS0SR   ;Write 0 to b2.
                          ;Write 1 to b7, b6, b5 and b0 since they do not change.
                          ;b4, b3 and b1 are not register bits. Write 0 to these bits.
```

32.20 Notes on LIN Module

32.20.1 Influence of $\overline{SD}$

When a low-level signal is applied to the $\overline{SD}$ pin while the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on $\overline{SD}$ pin enabled), the following pins become high-impedance: P7_2/CLK2/TA1OUT/V/RXD1, P7_3/$\overline{CTS2}$/$\overline{RTS2}$/TA1IN/$\overline{V}$/TXD1, P7_4/TA2OUT/W/LIN0OUT, P7_5/TA2IN/$\overline{W}$/LIN0IN, P8_0/TA4OUT/U/TSUDA, P8_1/TA4IN/$\overline{U}$/TSUDB

32.21 Notes on CAN Module

Note

Do not use CAN function in the M16C/57 Group.
In CAN module 1 channel version in the M16C/5M Group, use CAN0 not CAN1.

32.22 Notes on A/D Converter

Note

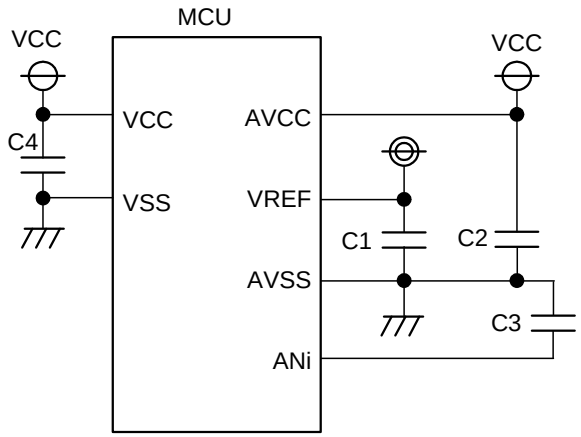
The 100-pin package has no AN2_4. The 64-pin package has no AN0_4 to AN0_7, AN2_0 to AN2_3, AN2_5 to AN2_7.
Do not use these pins as analog pins.

32.22.1 Analog Input Pin

Do not use any pin from AN4 to AN7 as analog input pin if any pin from $\overline{KI0}$ to $\overline{KI3}$ is used as a key input interrupt.

32.22.2 Pin Configuration

To prevent operation errors due to noise or latchup, and to reduce conversion errors, place capacitors between the AVSS pin and the AVCC pin, the VREF pin, and analog inputs (ANi (i = 0 to 7), AN0_i, AN2_i, and AN3_0 to AN3_2). Also, place a capacitor between the VCC pin and VSS pin.



ANi: ANi (i = 0 to 7), AN0_i, AN2_i, and AN3_0 to AN3_2

Notes:
1. Reference values: C1 ≥ 0.47 μF, C2 ≥ 0.47 μF, C3 ≥ 100 pF, C4 ≥ 0.1 μF
2. The traces for the capacitor and MCU should be as short and as wide as much as physically possible.

Figure 32.12 Example of Pin Configuration

32.22.3 Register Access

Set registers associated with A/D converter after setting the CKS3 bit in the ADCON2 register. However the other bits in the ADCON2 register and the CKS3 bit can be set at the same time. After changing the CKS3 bit, set the others in the same way.
Write registers ADCON0 (excluding the ADST bit), ADCON1, and ADCON2 when A/D conversion stops (before a trigger is generated).
After A/D conversion stops, set the ADSTBY bit in the ADCON1 register from 1 to 0.

32.22.4 A/D Conversion Start

When rewriting the ADSTBY bit in the ADCON1 register from 0 (A/D operation stopped) to 1 (A/D operation enabled), wait for one ϕAD cycle or more before starting A/D conversion.

32.22.5 A/D Operation Mode Change

When the A/D operation mode has been changed, reselect analog input pins by using bits CH2 to CH0 in the ADCON0 register or bits SCAN1 to SCAN0 in the ADCON1 register.

32.22.6 State When Forcibly Terminated

If A/D conversion in progress is halted by setting the ADST bit in the ADCON0 register to 0 (A/D conversion stopped), the conversion result is undefined. In addition, the unconverted ADi register (i = 0 to 7) may also become undefined. Do not use any value in ADi registers when setting the ADST bit to 0 by a program during A/D conversion.

32.22.7 A/D Open-Circuit Detection Assist Function

The conversion result in open-circuit depends on the external circuit. Use this function only after careful evaluation of the system.

When A/D conversion starts after changing the AINRST register, follow these steps:

(1) Change bits AINRST1 to AINRST0 in the AINRST register.
(2) Wait for one cycle of ϕAD.
(3) Set the ADST bit in the ADCON0 register to 1 (A/D conversion started).

32.22.8 Detecting Completion of A/D Conversion

In one-shot mode and single sweep mode, use the IR bit in the ADIC register to detect completion of A/D conversion. When not using an interrupt, set the IR bit to 0 by a program after detection.

When 1 is written to the ADST bit in the ADCON0 register, the ADST bit becomes 1 (A/D conversion start) after start processing time elapses (see Table 26.6 “Cycles of A/D Conversion Item”). Therefore when reading the ADST bit immediately after writing 1, 0 (A/D conversion stop) may be read.

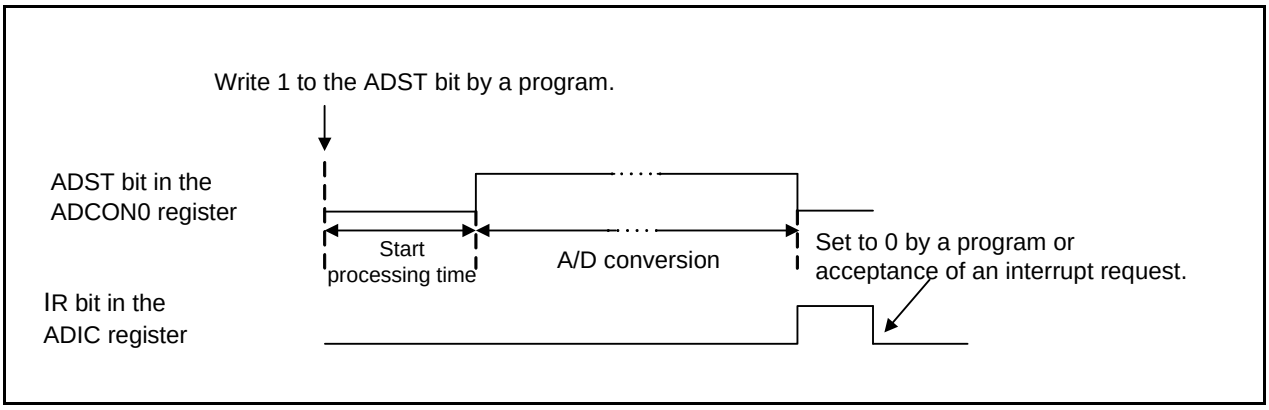


Figure 32.13 ADST Bit Operation

32.22.9 ϕAD

Divide fAD so ϕAD conforms to the standard frequency.

In particular, consider the maximum and minimum values of fOCO40M when the CKS3 bit in the ADCON2 register is 1 (fOCO40M is fAD).

32.23 Notes on D/A Converter

32.23.1 When Not Using the D/A Converter

When not using the D/A converter, set the DA0E bit in the DACON register to 0 (output disabled) and the DA0 register to 00h in order to minimize unnecessary current consumption and prevent current flow to the R-2R resistor.

32.24 Notes on Flash Memory

Note

Pins P4_0 to P4_7, P5_0 to P5_7, P9_4 cannot be used in the 80-pin package.
Pins P0_4 to P0_7, P1_0 to P1_7, P3_4 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P9_4 to P9_7 cannot be used in the 64-pin package. For the 80-pin package and 64-pin package, do not use these pins for the entry of user boot function.

32.24.1 OFS1 Address, OFS2 Address, and ID Code Storage Address

The OFS1 address, OFS2 address, and ID code storage address are part of flash memory. When writing a program to flash memory, write an appropriate value to those addresses simultaneously.

In the OFS1 address, the MCU state after reset and the function to prevent rewrite in parallel I/O mode are selected. The OFS1 address is 0FFFFFh. This is the most significant address of block 0 in program ROM 1 and upper address of reset vector. Also, OFS2 address and the ID code storage address is in block 0 and upper address of the interrupt vector.

The ID code check function cannot be disabled. Even if the protect using the ID code check function is unnecessary, input the appropriate ID code when using a serial programmer or debugger. Without the appropriate ID code, the serial programmer or debugger cannot be used.

ex) Set FEh to the OFS1 address, and set FFh to the OFS2 address

When using an address control instruction and logical addition:

```
.org 0FFDBH
.byte 0FFh
.org 0FFFFCh
RESET:
.lword start | 0FE000000h
```

When using an address control instruction:

```
.org 0FFDBH
.byte 0FFh
.org 0FFFFCh
RESET:
.addr start
.byte 0FEh
```

(Program format varies depending on the compiler. Refer to the compiler manual.)

32.24.2 Reading Data Flash

When 3.0 V < VCC ≤ 5.5 V and f(BCLK) ≥ 20 MHz, one wait must be inserted to execute the program on the data flash and read the data. Set the PM17 in the PM1 register or FMR17 bit in the FMR1 register to insert one wait.

32.24.3 CPU Rewrite Mode

32.24.3.1 Operating Speed

Select a CPU clock frequency of 16 MHz or less by setting the CM06 bit in the CM0 register and bits CM17 and CM16 in the CM1 register before entering CPU rewrite mode (EW0 or EW1 mode). Also, set the PM17 bit in the PM1 register to 1 (wait state).

32.24.3.2 CPU Rewrite Mode Select

Change FMR01 bit in the FMR0 register, FMR11 bit in the FMR1 register, and FMR60 bit in the FMR6 register while in the following state:

- The PM24 bit in the PM2 register is 0 ($\overline{\text{NMI}}$ interrupt disabled).
- High is input to the $\overline{\text{NMI}}$ pin.

Change the FMR60 bit while the FMR00 bit in the FMR0 register is 1 (ready).

32.24.3.3 Prohibited Instructions

Do not use the following instructions in EW0 mode:
UND instruction, INTO instruction, JMPS instruction, JSRS instruction, and BRK instruction.

32.24.3.4 Interrupts (EW0 Mode and EW1 Mode)

- Do not use an address match interrupt during command execution because the address match interrupt vector is located in ROM.
- Do not use a non-maskable interrupt during block 0 erase because fixed vector is located in block 0.

32.24.3.5 Rewrite (EW0 Mode)

If the power supply voltage drops while rewriting the block where the rewrite control program is stored, the rewrite control program is not correctly rewritten. This may prevent the flash memory from being rewritten. If this error occurs, use standard serial I/O mode or parallel I/O mode for rewriting.

32.24.3.6 Rewrite (EW1 Mode)

Do not rewrite any blocks in which the rewrite control program is stored.

32.24.3.7 DMA transfer

In EW0 mode, do not use flash memory as a source of the DMA transfer.
In EW1 mode, do not generate a DMA transfer while the FMR00 bit in the FMR0 register is 0 (auto programming or auto erasing).

32.24.3.8 Wait Mode

To enter wait mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before executing the WAIT instruction.

32.24.3.9 Stop Mode

To enter stop mode, set the FMR01 bit to 0 (CPU rewrite mode disabled), and then disable DMA transfer before setting the CM10 bit in the CM 1 register to 1 (stop mode).

32.24.3.10 Software Command

Observe the notes below when using the following commands.

- Program
- Block erase
- Lock bit program
- Read lock bit status
- Block blank check

(a) The FMR00 bit in the FMR0 register indicates the status while executing these commands. Do not execute other commands while the FMR00 bit is 0 (busy).
(b) Use these commands in 40 MHz on-chip oscillator mode, high-speed mode, medium-speed mode, and PLL operating mode. Do not change clock modes while the FMR00 bit in the FMR0 register is 0 (busy).
(c) After executing the program, block erase, or lock bit program command, perform a full status check per command (Do not execute multiple commands or same command more than once before performing a full status check).
(d) Do not execute the program, block erase, lock bit program, or block blank check command when either or both bits FMR06 and FMR07 in the FMR0 register are 1 (error).
(e) Do not use these commands in slow read mode (when the FMR22 bit is 1) or low current consumption read mode (when both bits FMR22 and FMR23 are 1).

32.24.3.11 Program and Erase Cycles and Execution Time

Execution time of the program, block erase, and lock bit program commands becomes longer as the number of programming and erasing increases.

32.24.3.12 Suspending the Auto-Erase and Auto-Program Operations

When the program, block erase, and lock bit program commands are suspended, the blocks for those commands must be erased. Execute the program and lock bit program commands again after erasing.

Those commands are suspended by the following reset or interrupts:

- Hardware, power-on, voltage monitor 0, voltage monitor 2, oscillator stop detect, watchdog timer, software resets.
- $\overline{\text{NMI}}$, watchdog timer, oscillator stop/restart detect, and voltage monitor 2 interrupts.

32.24.4 User Boot

32.24.4.1 User Boot Mode Program

Note the following when using user boot mode:

- When using user boot mode, make sure to allocate the program to be executed to program ROM 2.
- The LVDAS bit in the OFS1 address and bits WDTRCS1 and WDTRCS0 in the OFS2 address are disabled in boot mode.
- When restarting the MCU in user boot mode after starting it in user boot mode, RAM becomes undefined.
- If addresses 13FF8h to 13FFBh are all 00h, the MCU does not enter standard serial I/O mode. Therefore, the programmer or on-chip debugger cannot be connected.
- As the reset sequence differs, the time necessary for starting the program is longer than in single-chip mode.
- Functions in user boot mode cannot be debugged by the on-chip debugging emulator or full spec emulator.
- While using user boot mode, do not change the input level of the pin used for user boot entry. However, if there is a possibility that the input level may change, perform the necessary processes in user boot mode, then restart the MCU in single-chip mode before the input level changes.
- To use user boot mode after standard serial I/O mode, turn off the power when exiting standard serial I/O mode, and then turn on the power again (cold start). The MCU enters user boot mode under the right conditions.

32.25 Notes on E2PROM Emulation Data Flash

32.25.1 Relation with CPU Rewrite Mode

When the FMR01 bit in the FMR0 register is 1 (CPU rewrite mode enabled), do not set the EWM bit in the E2FM register to 1 (erase/program enabled).

32.25.2 CPU Clock When Rewriting

Rewrite the E2dataFlash in high speed mode, medium speed mode, or PLL operating mode, 40 MHz on-chip oscillator mode.

32.25.3 Clock Transition

To change the mode after rewriting the E2dataFlash, follow the steps below.

(a) Transition to wait mode, stop mode, 125 kHz on-chip oscillator low power mode, or low power mode
  (1) Wait until the RDY bit in the E2FS0 register becomes 1 (ready).
  (2) Set the OM bit in the E2FM register to 0 (E2dataFlash stopped).
  (3) Change modes.

(b) Transition to a mode not listed in (a)
  (1) Wait until the RDY bit in the E2FS0 register becomes 1 (ready).
  (2) Change modes.

REGISTER INDEX

[U]

[V]

[W]

1. Items revised or added in this version

REVISION HISTORY	M16C/5M, M16C/57 Group User's Manual: Hardware

Rev.	Date	Description	
		Page	Summary
1.10	Sep. 01, 2011	Overall	Modified register names are as follows: • "CANi Receive Completion Interrupt Control Register" to "CANi Reception Complete Interrupt Control Register" • "CANi Transmit Completion Interrupt Control Register" to "CANi Transmission Complete Interrupt Control Register" • "CANi Wakeup Interrupt Control Register" to "CANi Wake-up Interrupt Control Register"
		Overall	Changed terminologies are as follows: • "voltage detector 2" to "voltage monitor 2" • "oscillation stop detection reset" to "oscillator stop detect reset" • "detection circuit" to "detector" • "oscillation/oscillator circuit" to "oscillator" • "oscillator" to "a crystal/ceramic resonator" • "oscillator manufacturer" to "manufacturer of crystal/ceramic resonator" • "on-chip oscillator oscillation circuit" to "on-chip oscillator"
		Overview	
		8, 9, 10	Table 1.7 M16C/5M Group Product List (J-Version), Table 1.8 M16C/5M Group Product List (K-Version), Table 1.9 M16C/57 Group Product List (J-Version), and Table 1.10 M16C/57 Group Product List (K-Version): Changed the product statuses.
		25, 26	Table 1.18 Pin Functions (64-Pin, 80-Pin, and 100-Pin Packages), Table 1.19 Pin Functions (100-Pin Package Only), Table 1.21 Pin Functions (100-Pin and 80-Pin Package Only): Changed the explanation of the direction register in the Description column of the I/O port row.
		Resets	
		84	Table 6.1 Types of Resets: Added the "Registers and Bits Not to Reset" column.
		84	Figure 6.1 Reset Circuit Block Diagram: Deleted SFR names from the figure, and the SFR details are described in Table 6.2 Classification of SFRs Which are Reset.
		85	Table 6.2 Classification of SFRs Which are Reset: Added.
		86	Table 6.4 Registers: • Changed the reset value of the RSTFR register from "XX0X 001Xb". • Added note 1.
		87	6.2.2 Reset Source Determine Register (RSTFR): Added "Conditions to become 0" to the explanation of the OSDR bit.
		88	6.3.1 Optional Function Select Address 1 (OFS1): Added "This bit is enabled in single-chip mode, while disabled in boot mode." to the LVDAS bit explanation.
		90	Table 6.7 Pin Status When $\overline{\text{RESET}}$ Pin Level is Low: • Changed the Pin Name column. • Changed note 1.
		91	Figure 6.3 Reset Sequence: Changed the oscillation period of XIN.
		92	6.4.2 Hardware Reset: Changed "20 fOCO-S cycles" to "tw(RSTL)" in (2) of "When the power supply is stable".
		93	6.4.3 Power-On Reset Function: Changed "at 0.8 VCC or more" to "in the range of VIH" in the first paragraph.
		93	Figure 6.5 Example of Power-On Reset Operation: Changed "External power VCC" to "VCC".
		96	Figure 6.6 SVCC Timing: Revised.
		Clock Generator	
		Chap. 8.	Deleted description regarding 0004h Processor Mode Register 0
		115	Figure 8.1 System Clock Generator: • Deleted buffers for peripheral function clock and added the main clock. • Changed a part of PLL frequency synthesizer configuration part
		128	8.3.1 Main Clock: Changed the description in the parenthesis in To start the main clock oscillation, (3).
		129	8.3.2 PLL Clock: Changed the explanation of how to generate PLL clock from the main clock.
		131	8.3.6 Sub Clock (fC): Deleted "P8_5" in the parenthesis
		132	8.4.2 Peripheral Function Clocks (f1, fOCO40M, fOCO-F, fOCO-S, fC32, fC, Main Clock): • Added Lin module to functions which can use f1. • Added descriptions regarding the main clock.
		133	Figure 8.5 Peripheral Function Clocks: Revised
		141	Figure 8.11 Voltage Fluctuation Timing: Changed the range of $f_{(ripple)}$.

Rev.	Date	Description	
		Page	Summary
1.10	Sep. 01, 2011	**Power Control**	
		143	9.2.1 Flash Memory Control Register 0 (FMR0): Changed the FMR01 and FMSTP bit explanations.
		144	9.2.2 Flash Memory Control Register 2 (FMR2): The following changes were made to the FMR23 bit explanation: • Deleted the sentence “When the CM07 bit is 0, ...”. • Added usage restrictions.
		147	9.3.1.6 Low-Speed Mode: Changed the division of fOCO-F for when bits CM21 and FRA01 are both 1.
		147	9.3.1.7 Low Power Mode: Deleted the explanation about the CM06 bit.
		148	Table 9.2 Clocks in Normal Operating Mode: Combined notes 2 to 6 into note 2.
		148, 149, 149	Table 9.3 Clock-Related Bit Setting and Modes, Table 9.4 Selecting Clock Division Related Bits, Table 9.5 Example Settings for 40 MHz On-Chip Oscillator Mode Division Related Bits: Added a legend below each table.
		153	9.3.3 Wait Mode: Changed the explanation about the operation of peripheral functions.
		153	9.3.3.2 Entering Wait Mode: Added a procedure for entering wait mode.
		154	9.3.3.4 Exiting Wait Mode: Deleted the explanations below the table except the explanation about exiting wait mode using an interrupt.
		154	Table 9.7 Resets and Interrupts to Exit Wait Mode and Conditions for Use: • Added an explanation of internal clock in the conditions for use, CM02 = 1 column of the Serial interface row. • Added rows "LIN 0 Low detection" and "LIN0" to the Peripheral function interrupt. • Changed the conditions for use in the Voltage monitor 2 row. • Changed “Usable when fOCO-S is supplied” to “Usable” in the Voltage monitor 0 reset row. • Changed the conditions for use in the Voltage monitor 2 reset row.
		155	9.3.4.1 Entering Stop Mode: Moved some of explanations under Table 9.9 here and added a procedure for entering stop mode.
		156	Table 9.9 Resets and Interrupts to Exit Stop Mode and Conditions for Use: Added the “LIN0 Low detection” row to the Peripheral function interrupt.
		157	Figure 9.2 Stop and Restart of the Flash Memory: • Changed the ranges of the Stop Procedure and Restart Procedure. • Deleted note 4.
		158	9.4.2.1 Slow Read Mode: Added an explanation for when no wait operation is required.
		158, 159	Figure 9.3 Setting and Canceling Slow Read Mode and Figure 9.4 Setting and Canceling Low Current Consumption Read Mode: Deleted the last process, “Restore the CPU clock” from the canceling procedure.
		160	9.5.2 A/D Converter: Deleted the explanation for when A/D conversion is performed.
		160	9.5.3 D/A Converter: Added.
		161	9.6.1 CPU Clock: Added line 2.
		161	9.6.2 Wait Mode: • Added lines 4 and 5 to the first bullet. • Changed the second bullet. • Added the third bullet. • Modified “high-level duration” to “low-level duration” in the fourth bullet.
		161	9.6.3 Stop Mode: • Added lines 6 to 8 to the third bullet. • Changed the fifth bullet. • Added the sixth bullet.
		162	9.6.4 Low Current Consumption Read Mode: Added the third bullet.
		162	9.6.5 Slow Read Mode: Added.
		Programmable I/O Ports	
		180	11.3.5 Pull-Up Control Register 2 (PUR2): Changed the explanation below the register diagram.
		191	11.6.2 Influence of $\overline{SD}$: Added TSUDA and TSUDB to the pins.
		Interrupt	
		196	12.2.2 Interrupt Control Register 1: Added description of IFSR4A to the register explanation.

Rev.	Date	Description	
		Page	Summary
1.10	Sep. 01, 2011	199	12.2.4 Interrupt Source Select Register 4 (IFSR4A): Changed the Function column of the IFSR46 bit.
		200	12.2.5 Interrupt Source Select Register 3 (IFSR3A): Changed the Function column of bits IFSR33, IFSR34, and IFSR35.
		201	12.2.6 Interrupt Source Select Register 2 (IFSR2A): Changed the Function column of the IFSR24 bit.
		211	Table 12.7 Relocatable Vector Tables (2/2): Changed note 5.
		218	12.8 $\overline{\text{INT}}$ Interrupt: Modified set values of the IFSR45 bit and IFSR44 bit to 0 when using $\overline{\text{INT6}}$ and $\overline{\text{INT7}}$ interrupts, respectively.
		219	12.10 Key Input Interrupt: Changed the explanation of the condition for the IR bit in the KUPIC register to become 1.
		225	12.13.7 $\overline{\text{INT}}$ Interrupt: Added description of IFSR4A to the third bullet.
		Watchdog Timer	
		234	13.4.1 Refresh Operation Period: Rewritten.
		Timer A	
		302	15.5.1.3 Influence of $\overline{\text{SD}}$: Added TSUDA and TSUDB to the pins.
		Three-Phase Motor Control Timer Function	
		372	17.5.2 Influence of $\overline{\text{SD}}$: Added TSUDA and TSUDB to the pins.
		Timer S	
		Chap. 18.	Changed the configuration, and added detailed explanations.
		Chap. 18.	Changed terminologies in this chapter are as follows: • “digital debounce function” to “digital debounce filter” • Remove the term “mode” from increment, increment/decrement, and two-phase pulse signal processing. • “channel interrupt” to “IC/OC channel interrupt” • “base timer interrupt” to “IC/OC base timer interrupt” • Appropriate explanations/names are provided for base timer reset depending on its condition. • “fBT1 clock cycles” to “fBT1 cycles”
		374, 375	Figure 18.1 IC/OC Block Diagram (1/2) and Figure 18.2 IC/OC Block Diagram (2/2): Added details.
		376	Table 18.2 I/O Pins: Added note 1 and note 2.
		380	18.2.2 Waveform Generation Register j (G1POj) (j = 0 to 7): Added details.
		381	18.2.3 Waveform Generation Control Register j (G1POCRj) (j = 0 to 7): Changed the explanation of bits MOD1 and MOD0.
		383	18.2.4 Time Measurement Control Register j (G1TMCRj) (j = 0 to 7): • Added some descriptions to the Function columns of bits DF1 and DF0, and the GOC bit. • Changed the register explanation. • Added an explanation to bits DF1 and DF0, and the GSC bit.
		385	18.2.5 Base Timer Register (G1BT): • Changed the Function column in the register diagram. • Changed the explanation since the write operation to this register is disabled.
		386	18.2.6 Base Timer Control Register 0 (G1BCR0): Added the IT bit explanation.
		387	18.2.7 Base Timer Control Register 1 (G1BCR1); Changed the following in the RST1 bit explanation: • Changed the reference target. • Deleted the explanation regarding the G1POj register and moved it to 18.2.2.
		388	18.2.8 Time Measurement Prescaler Register j (G1TPRj) (j = 6 and 7): Added the Set Value column.
		394	18.2.16 Interrupt Request Register (G1IR): Changed the reference target for the procedure.
		397	Table 18.5 Base Timer Specifications: • Added the BTS bit to the Base timer reset conditions. • Deleted “while the base timer is counting” from “Base timer reset value while the base timer is counting”. • Deleted the Write to base timer row. • Deleted the Selectable functions row and moved the contents to 18.3.1.2 and 18.3.1.3.
		398	Figure 18.3 Base Timer Block Diagram: • Added registers G1DV and G1BT. • Added detailed description of two-phase pulse clock.
		398	Table 18.6 Base Timer Associated Register Settings: Added details.

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		Page	Summary
1.10	Sep. 01, 2011	399, 400, 401	18.3.1.1 Increment, 18.3.1.2 Increment/Decrement and 18.3.1.3 Two-Phase Pulse Signal Processing: • Added titles and explanations. • Changed descriptions of interrupt requests in figures for each operation.
		402	Figure 18.7 Two-Phase Pulse Signal Processing (When Using the Base Timer Reset): Deleted the values to indicate timings, and moved the information to the Electrical Characteristics chapter.
		403	Figure 18.8 Base Timer Reset with the G1BTRR Register: • Deleted the description of the base timer overflow request. • Added a condition.
		403, 404	Figure 18.9 Base Timer Reset with the G1PO0 Register and Figure 18.10 Base Timer Reset with $\overline{INT1}$ Pin Input: Added a condition.
		405, 409	18.3.2 Time Measurement Function and 18.3.3 Waveform Generation Function: Moved under 18.3 Operations.
		405	Table 18.10 Time Measurement Function Specifications: • Changed the Interrupt request to the Interrupt request occurrence timing in the Item column. • The explanations for the Gate function and Digital debounce filter in the Selectable functions are simplified.
		406	Table 18.11 Time Measurement Function Associated Registers: • Changed. • Added settings when the gate function is used.
		406	Figure 18.11 Time Measurement Function (1/2): Deleted the description for when the base timer and the G1PO0 register match.
		407	Figure 18.12 Time Measurement Function (2/2): Modified timings mainly.
		408	Figure 18.13 Prescaler and Gate Functions: Modified the timing of the G1IR bit.
		409	18.3.2.1 Gate Function (Channel 6 and 7): Added
		410	Table 18.12 Single-Phase Waveform Output Mode Specifications: • Changed the range of values for m and n. • Changed the Interrupt request to the Interrupt request occurrence timing in the Item column. • Added “or I/O port” to the Specification of the OUTC1_ j pin. • The explanation for the Compare match output in the Selectable functions are simplified.
		411	Table 18.13 Registers and Settings in Single-Phase Waveform Output Mode: Added.
		413	Figure 18.15 Single-Phase Waveform Output Mode Operation (2/2): • Added “when bits IOj1 and IOj0 are 10b” to the description “Output high by compare match”. • Added a condition regarding the EOCj bit in the G1OER register.
		414	Table 18.14 Inverted Waveform Output Mode Specifications: • Changed the range of values for m and n. • Changed the Interrupt request to the Interrupt request occurrence timing in the Item column. • Added “or I/O port” to the Specification of the OUTC1_ j pin.
		415	Table 18.15 Registers and Settings in Inverted Waveform Output Mode: Added.
		417	Figure 18.17 Inverted Waveform Output Mode Operation (2/2): • Added “when bits IOj1 and IOj0 are 10b” to the description “Output high by compare match”.
		418	Table 18.16 SR Waveform Output Mode Specifications: • Changed the range of values for m, n and p. • Changed the Interrupt request to the Interrupt request occurrence timing in the Item column. • Added “or I/O port” to the Specification of the OUTC1_ j pin.
		419	Table 18.17 Registers and Settings in SR Waveform Output Mode: Added.
		421	18.3.4 I/O Port Select Function: The contents of “18.6.1 INPC1_7 Alternate Input Pin” and “18.6.2 P1_7/INPC1_7 Digital Debounce Function” have been left here and these titles have been deleted.
		421	Table 18.18 Pin Settings for Time Measurement and Waveform Generation: Simplified.
		422	18.4 Interrupts: Changed.
		424	18.5.2 Changing the G1IR Register: Changed the explanation.
		425	Figure 18.20 IC/OC Interrupt 0 Operation Example: Changed from “IC/OC Interrupt 0 and 1 Operation”.
		426	18.5.3 Changing Registers ICOCiIC (i = 0, 1): Changed from “Changing Registers ICOCiIC and ICOCHjIC”.
		426	18.5.4 Output Waveform During the Base Timer Reset with the BTS bit and 18.5.5 OUTC1_0 Pin Output During the Base Timer Reset with the G1PO0 register: Changed from “Waveform Generation Function”.
		426	18.5.6 Interrupt Request When Selecting Time Measurement Function: Added.
		Real-Time Clock	
		457	20.4 Interrupts: Added description regarding the IFSR4A register to Table 20.5 and the register explanation.

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		Page	Summary
1.10	Sep. 01, 2011	**Serial Interface UARTi**	
		Chap. 21.	21.3.3.6 SDA Output Control to 21.3.3.10 Initialization of Transmission/Reception: Revised.
		Chap. 21.	21.8.2 Clock Asynchronous Serial I/O Mode (UART Mode): Deleted.
		Chap. 21.	Changed terminologies in this chapter are as follows: • “transfer clock“ to “transmit/receive clock” • “transfer data length” to “character length” • “transfer data format” to “bit order”
		460	21.1 Introduction: Changed the layout of the introduction, including tables.
		466	21.2.3 UARTi Transmit/Receive Mode Register (UiMR) (i = 0 to 4): Added an explanation to bits SMD2 to SMD0 for when the bits are set to 000b.
		467	21.2.4 UARTi Bit Rate Register (UiBRG) (i = 0 to 4): Changed the setting range in I^2C mode.
		467	21.2.5 UARTi Transmit Buffer Register (UiTB) (i = 0 to 4): Added “or I^2C mode” after “When character length is 9 bits long,...”.
		468	21.2.6 UARTi Transmit/Receive Control Register 0 (UiC0) (i = 0 to 4): Changed the first and second paragraphs in the NCH bit explanation.
		473	21.2.9 UART2 Special Mode Register 4 (U2SMR4): • Changed the bit names of bits SCLHI and SWC9. • Changed the Function column of bits STSPSEL, ACKC, SCLHI, and SWC9. • Added an explanation to each existing bit explanation. • Added bit explanations for the other bits.
		476	21.2.11 UART2 Special Mode Register 2 (U2SMR2): • Changed the bit names of bits SWC, ALS, and STAC. • Changed the functions of bits other than b7.
		479	21.3 Operations: Inserted the title.
		479	Table 21.5 Clock Synchronous Serial I/O Mode Specifications: Changed note 1 and note 2.
		480	Table 21.6 Pin Functions in Clock Synchronous Serial I/O Mode: • Added the I/O column. • Changed “the port direction bit corresponding to xxx pin” to “the port direction bit sharing pin” in the Method of Selection column. • Added the Input, Input port row to the RXDi pin.
		481	Table 21.7 Registers Used and Settings in Clock Synchronous Serial I/O Mode: • Added UCLKSEL0 and PCLKR rows to the Register column. • Added b8 to UiTB. • Added b8, b11, and b13 to b15 to UiRB. • Added b4 to b6 to UiMR.
		484	21.3.1.3 Continuous Receive Mode: • Added an explanation for when using an external clock. • Added Figure 21.6 Operation Example in Continuous Receive Mode.
		486, 495	21.3.1.5 $\overline{CTS}$/$\overline{RTS}$ Function, 21.3.2.5 $\overline{CTS}$/$\overline{RTS}$ Function: Deleted the CRD and CRS bit explanation and added a reference to a table that includes similar information.
		486	21.3.1.6 Processing When Terminating Communication or When an Error Occurs: Moved the contents of “21.2.1 Transmit/Receive Register Initialization” here and rewrote the explanation.
		487	Table 21.8 UART Mode Specifications: Deleted note 2.
		488	Table 21.9 I/O Pin Functions in UART Mode: • Added the I/O column. • Changed “the port direction bit corresponding to xxx pin” to “the port direction bit sharing pin” in the Method of Selection column. • Modified “$\overline{RTS}$ input” to “$\overline{RTS}$ output”.
		489	Table 21.10 Registers Used and Settings in UART Mode: • Added the UCLDSEL0 and PCLKR rows. • Added b11 to UiRB. • Changed the order of notes, and changed note 4.
		491	Figure 21.9 Receive Timing in UART Mode: Changed “UiBRG count source” to “Clock divided by UiBRG”.
		495	21.3.2.6 Processing When Terminating Communication or When an Error Occurs: Moved the contents of “21.3.2 Transmit/Receive Circuit Initialization” here and rewrote the explanation.

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		Page	Summary
1.10	Sep. 01, 2011	496	Table 21.12 I²C Mode Specifications: • Changed the setting value of U2BRG register n from “00h to FFh” in the Transfer clock row. • Changed note 1 and note 2.
		497	Figure 21.14 Internal Clock Configuration: Added.
		497	Table 21.13 I/O Pin Functions in I²C Mode: Added note 1, and the previous note 1 became note 2.
		498	Table 21.14 Registers Used and Settings in I²C Mode (1/2): • Added UCLKSEL0 and PCLKR to the Register column. • Added “When receiving, set FFh.” to b0 to b7 of U2TB in the Function column. • Added b8 to U2TB. • Added b13 to b15 to U2RB. • Added b4 to b6 to U2MR.
		499	Table 21.15 Registers Used and Settings in I²C Mode (2/2): • Changed the function of the SWC bit and CKPH bit. • Deleted the IFSR2A register.
		500	Table 21.16 I²C Mode Functions: • Added an explanation above the table. • Rewrote all of the content.
		501	Figure 21.15 Transfer to U2RB Register and Interrupt Timing: • Deleted “(1) IICM2 = 0 (ACK and NACK interrupts), CKPH = 0 (no clock delay)” and “(3) IICM2 = 1 (UART transmit/receive interrupt), CKPH = 0”.
		502	21.3.3.1 Detecting Start and Stop Conditions: Added the last paragraph.
		502	Figure 21.16 Detecting Start and Stop Conditions: Revised.
		503	Figure 21.17 STSPSEL Bit Functions: Revised.
		504	Figure 21.18 Register Setting Procedures for Condition Generation: Added.
		505	21.3.3.3 Arbitration: Rewritten.
		505	21.3.3.4 SCL Control and Clock Synchronization: Added, including Figure 21.19 and Figure 21.20.
		507	21.3.3.5 SCL Clock Frequency: Added, including Figure 21.21.
		511	Table 21.18 Special Mode 2 Specifications: Changed “While transmission” to “For transmit interrupt”, and “While receiving” to “For receive interrupt”.
		513	Table 21.20 Registers Used and Settings in Special Mode 2: • Added UCLKSEL0 and PCLKR to the Register column. • Added b8 to U2TB. • Added b8, b11, and b13 to b15 to U2RB. • Added b4 to b6 to U2MR. • Deleted note 1.
		515	Table 21.21 Registers Used and Settings in IE Mode: Deleted the IFSR2A register.
		517	Table 21.22 SIM Mode Specifications: Changed note 2.
		519	Figure 21.30 Transmit/Receive Timing in SIM Mode: Added the timing when the IR bit in the S2TIC register becomes 1.
		522-523	21.4 Interrupts, 21.4.1 Interrupt Related Registers and 21.4.2 Reception Interrupt: Added.
		524	21.5.1 Common Notes on Multiple Modes: Added.
		524, 525	21.5.2.2 Transmission and 21.5.2.3 Reception: Changed the explanations about the external clock level into bulleted lists.
		526-527	21.5.3.3 Setup and Hold Times When Generating a Start/Stop Condition to 21.5.3.6 Requirements to Start Transmission/Reception in Slave Mode: Added.
		527	21.5.4 Special Mode 4 (SIM Mode): Changed the conditions to generate a transmit interrupt request.
		Multi-Master I²C-bus Interface	
		Chap. 22.	Changed terminology “High-speed clock mode” to “Fast-mode”.
		545	22.2.8 I2C0 Status Register 0 (S10): Changed explanations for the following bits. • LRB bit: Rewritten. • AL bit: Changed “master-slave mode” to “master receive mode” in the third and fourth bullets of the Conditions to become 1. • PIN bit: Deleted the description about the MSLAD bit from the second last bullet in the Conditions become 0. • PIN bit: Rewrote the conditions for the SCLMM pin not to output a low signal.
		560	22.3.6 Arbitration Lost: Changed “When the ALS bit in the S1D0 register is 1” to “When the ALS bit in the S1D0 register is 0” in the eighth line from the bottom.

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		Page	Summary
1.10	Sep. 01, 2011	564	Figure 22.15 Operation When Transmitted/Received a Slave Address or Data: Changed the description of bits TRX, ADR0, and AAS in parenthesis for when a slave address is received.
		570	22.3.10.5 Slave Transmission: Added an explanation for when arbitration lost is detected.
		Serial Bus Interface	
		578	23.2.4 SS0 Control Register H (SS0CRH): Added explanations for when the RSSTP bit is 1, and 0.
		579	23.2.5 SS0 Control Register L (SS0CRL): • In the register diagram, changed the Bit Name and Function of the SRES bit, and changed not 1. • Added a description to the SOL explanation.
		596	23.3.2.3 Data Reception: Changed the description of the timing for the RSSTP bit to become 1 in the explanation for when ending receive data operation in master mode.
		579	23.2.5 SS0 Control Register L (SS0CRL): • Changed the Bit Name and the Function for the SRES bit, and note 1 in the register diagram. • Added an explanation regarding the SRES bit to the SOL bit explanation. • Added the SRES bit explanation.
		582	23.2.8 SS0 Status Register (SS0SR): • Modified the Function of the TDRE bit. • Changed the register explanation. • Added an explanation for when the bit is set to 0 to the TDRE explanation.
		590	23.3.1.7 Error Processing: Added
		594	23.3.2.2 Data Transmission: • Changed the third paragraph. • Deleted the sentence “Make sure that the ORER bit is set to 0 before data transmission.”.
		594	Figure 23.6 Transmit Operation Example in Synchronous Serial Communication Mode: Changed the figure to indicate master transmission with transmit data register empty interrupt enabled.
		595	Figure 23.7 Example of Data Transmission Flow in Synchronous Serial Communication Mode: Changed.
		597	Figure 23.9 Example of Data Reception Flow While in Master Mode of the Synchronous Serial Communication Mode: Changed.
		598	Figure 23.10 Example of Data Transmission/Reception Flow in Synchronous Communication Mode: Changed.
		582	23.3.3 4-Wire Serial Bus Mode: Changed the third paragraph below the Figure 23.11.
		604	Figure 23.13 Transmit Operation Example in 4-wire Serial Bus Mode: Added arrows to indicate the point of “TXI interrupt request generated” in (1) and (2).
		606	Figure 23.14 Receive Operation Example in 4-wire Serial Bus Mode: Changed the timing for the RSSTP bit to become 1, to the point after the RDRF bit becomes 0.
		607	23.3.3.4 $\overline{\text{SCS0}}$ Pin Control and Arbitration: Changed “CSS1 and CSS0 are set to 10b” to “CSS1 and CSS0 are set to 10b or 11b” in line 1.
		609	23.5 Notes on Serial Bus Interface: Added
		LIN Module	
		Chap. 24.	Changed term in this chapter is as follows: • “break dominant” to “break”
		Chap. 24.	Changed the sentence in notes from “The input signal Low time counting is indicated in wake-up reception.” to “The input signal Low time counting is used on wake-up reception.”.
		611	Figure 24.1 LIN Module Block Diagram: Added “dedicated LIN channel 0 registers” to “LIN0 common registers”.
		612	24.1.1.1 LWBR0 Bit: Added an explanation for when this bit is set to 1.
		614	24.1.4 LIN Self-test Control Register (LSTC): Added an explanation for when reading each bit to the Function in the figure above.
		616	24.1.6.1 LCKS Bit: Added an explanation of relation with the LWBR0 bit, and the L0MST register.
		619	24.1.9.1 WUTL Bit: Added an explanation of relation with bits LWBR0, and LCKS.
		623	24.1.12.2 OM1 Bit: Written.
		624	24.1.13.1 FTS Bit, 24.1.13.2 RTS Bit: • Changed “This bit is set to 1...” to “The bit remains 1”. • Added error detection to the case to become 0 automatically.
		625	24.1.14 LIN0 Mode Status Register(L0MST): Modified “LIN0” to “LIN” in the register diagram.

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		Page	Summary
1.10	Sep. 01, 2011	626	24.1.15 LIN0 Status Register (L0ST): Changed “an interrupt is generated” to “the LIN0 interrupt request is generated” in each bit explanation.
		626, 628	24.1.15.1 FTC Bit, 24.1.15.2 FRC Bit, 24.1.16.1 BER Bit, 24.1.16.2 PBER Bit: Added LIN wake-up mode to the case to set 0 before the next communication starts.
		627	24.1.15.3 ERR Bit: Changed “in LIN operation mode” to “in LIN wake-up mode or LIN operation mode”.
		630	24.1.17 LIN0 Response Field Setting Register (L0RFC): Added details to the Function column of RFDL.
		633	24.1.19 LIN0 Checksum Buffer Register (L0CB): • Deleted “Writing is disabled.” when the RFT bit = 1. • Added a sentence “Write operation is invalid when in LIN reset mode and LIN wake-up mode.”.
		635	24.2 Operational Mode: Deleted the explanation about transition between operational modes.
		636	24.2.1 LIN Reset Mode: • Changed the explanation. • Changed the following in the registers which retain their previous values after entering this mode. •LSTC register: Deleted. •L0MD register: Deleted the explanation in the parenthesis. •L0CB register: Added.
		636	24.2.4 LIN Self-test Mode: Changed the explanation.
		638	Table 24.5 Processing in Response Transmission: Changed the LIN Module Processing in (4).
		639	Table 24.6 Processing in Response Reception: Changed the LIN Module Processing in (4).
		646	24.7.2 Operation of Wake-up Reception: Changed the third paragraph.
		647	Figure 24.32 Input Signal Low Time Counting: Added note 1.
		650	Table 24.9 Operational Status: Changed note 2.
		651	Table 24.10 Error Status Types: Changed note 1.
		653	24.10 LIN Interrupt: Changed “by logical OR as interrupt request “LIN0 interrupt”” to “by logical OR, and output LIN0 interrupt request” in the second paragraph.
		653	Figure 24.36 LIN0 Interrupt Block Diagram: Revised.
		654	24.11 LIN Self-test Mode: Changed the last two paragraphs.
		646	24.11.1 Entry into LIN Self-test Mode: Changed.
		656	24.11.2 Transmission in LIN Self-test Mode, 24.11.3 Reception in LIN Self-test Mode and 24.11.4 Exit from LIN Self-test Mode: Rewritten.
		657	24.12 Notes on LIN Module: Added.
		CAN Module	
		662	25.1.1 CANi Control Register (CiCTLR) (i = 0, 1): Changed note 2 and note 3.
		A/D Converter	
		728	Table 26.1 A/D Converter Specifications: Changed pin numbers of “(AN2_0 to AN2_3, AN2_5 to AN2_7)” in the Analog input pins.
		729	Figure 26.1 A/D Converter Block Diagram: Unified upper data bus and lower data bus with a single data bus.
		730	26.2 Registers: Added an explanation about CKS3.
		737	26.3.1 A/D Conversion Cycle: Changed the sentence that describes to select multiple pins.
		Flash Memory	
		783	Table 29.12 Modes after Executing Commands (in EW0 Mode): Changed the command mode of the clear status register.
		803	29.8.6.8 Block Blank Check Command: Changed the explanation below Figure 29.23.
		813	29.10 Parallel I/O Mode: Changed the title number from “29.9.6.” to “29.10”.
		817	29.11.4 User Boot: Changed the second note from the bottom.
		Electrical Characteristics	
		J version, Common to 3 V and 5 V	
		831	Table 31.1 Absolute Maximum Ratings: Deleted VREF from the V_I.
		842	Table 31.14 On-Chip Oscillator Electrical Characteristics: Added the Dedicated 125 kHz on-chip oscillator for the watchdog timer oscillation frequency.

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		Page	Summary
1.10	Sep. 01, 2011	**J-Version, V_{CC} = 5 V**	
		851	Figure 31.14 Multi-master I²C-bus: Changed t_{HD};DTA to t_{HD};DAT and t_{su};DTA to t_{su};DAT.
		852	Table 31.31 Serial Bus Interface: Added the standard for slave to $td_{(SSCK-SSIO)}$.
		J-Version, V_{CC} = 3 V	
		864	Figure 31.27 Multi-master I²C-bus: Changed t_{HD};DTA to t_{HD};DAT and t_{su};DTA to t_{su};DAT.
		865	Table 31.48 Serial Bus Interface: Added the standard for slave to $td_{(SSCK-SSIO)}$.
		K version, Common to 3 V and 5 V	
		880	Table 31.62 On-Chip Oscillator Electrical Characteristics: Added the Dedicated 125 kHz on-chip oscillator for the watchdog timer oscillation frequency.
		K-Version, V_{CC} = 5 V	
		889	Figure 31.45 Multi-master I²C-bus: Changed t_{HD};DTA to t_{HD};DAT and t_{su};DTA to t_{su};DAT.
		890	Table 31.79 Serial Bus Interface: Added the standard for slave to $td_{(SSCK-SSIO)}$.
		K-Version, V_{CC} = 3 V	
		902	Figure 31.58 Multi-master I²C-bus: Changed t_{HD};DTA to t_{HD};DAT and t_{su};DTA to t_{su};DAT.
		903	Table 31.96 Serial Bus Interface: Added the standard for slave to $td_{(SSCK-SSIO)}$.
		Usage Notes	
		Chap. 32.	32.1 OFS1 Address and ID Code Storage: Deleted since same description is in the Flash chapter.
		911	Figure 32.2 SVCC Timing: Revised.
		915	Figure 32.7 Voltage Fluctuation Timing: Changed the range of $f_{(ripple)}$.
		916	32.6.1 CPU Clock: Added line 2.
		916	32.6.2 Wait Mode: • Added lines 4 and 5 to the first bullet. • Changed the second bullet. • Added the third bullet.
		916	32.6.3 Stop Mode: • Added lines 6 to 8 to the third bullet. • Changed the fifth bullet. • Added the sixth bullet.
		917	32.6.4 Low Current Consumption Read Mode: Added the third bullet.
		917	32.6.5 Slow Read Mode: Added.
		918, 925, 931	32.7.2, 32.11.1.3, 32.13.2 Influence of $\overline{SD}$: Added TSUDA and TSUDB to the pins.
		922	32.8.7 $\overline{INT}$ Interrupt: Added description of IFSR4A to the third bullet.
		932	32.14.2 Changing the G1IR Register: Changed the explanation.
		933	Figure 32.9 IC/OC Interrupt 0 Operation Example: Changed from “IC/OC Interrupt 0 and 1 Operation”.
		934	32.14.3 Changing Registers ICOCiIC (i = 0, 1): Changed from “Changing Registers ICOCiIC and ICOCHjIC”.
		934	32.14.4 Output Waveform During the Base Timer Reset with the BTS bit and 32.14.5 OUTC1_0 Pin Output During the Base Timer Reset with the G1PO0 register: Changed from “Waveform Generation Function”.
		934	32.14.6 Interrupt Request When Selecting Time Measurement Function: Added.
		938	32.17.1 Common Notes on Multiple Modes: Added.
		938, 939	32.17.2.2 Transmission and 32.17.2.3 Reception: Changed the explanations about the external clock level into bulleted lists.
		940-941	32.17.3.3 Setup and Hold Times When Generating a Start/Stop Condition to 32.17.3.6 Requirements to Start Transmission/Reception in Slave Mode: Added.
		941	32.17.4 Special Mode 4 (SIM Mode): Changed the conditions to generate a transmit interrupt request.
		943	32.19 “Notes on Serial Bus Interface”: Added
		944	32.20 Notes on LIN Module: Added
		952	32.24.4 User Boot: Changed the second note from the bottom.

Refer to 2. “Items revised or added in previous versions” for the items revised or added in previous versions.

2. Items revised or added in previous versions

REVISION HISTORY	M16C/5M, M16C/57 Group User's Manual: Hardware

Rev.	Date	Page	Revision History
0.13	Oct 02, 2009	—	Initial release
0.20	Dec 25, 2009		**The manual in general**
		—	0019h register name changed to “Voltage Detector 2 Flag Register”
		—	001Ah register name changed to “Voltage Detector Operation Enable Register”
		—	0028h register name changed to “Voltage Detector 2 Level Select Register”
		—	002Ah register name changed to “Voltage Monitor 0 Control Register”
		—	002Ch register name changed to “Voltage Monitor 2 Control Register”
		—	0088h register name changed to “E2 Data Flash Command Register”; reset value changed to “00h”
		—	0092h “E2 Data Flash Control Register” reset value changed to “XXXX XXX0b”
		—	0094h “E2 Data Flash Status Register 1” reset value changed to “XXXX XXX0b”
		—	0366h “Port Control Register” reset value changed to “0XX0 0XX0b”
		—	03A2h “Open-Circuit Detection Assist Function Register” reset value changed to “XX00 XXXXb”
		—	03B4h “SFR Snoop Address Register” reset value changed to “XXXX XXXXb”
			Overview
		3, 5, 7	Table 1.2 “Specifications (100-pin Version) (2/2)”, Table 1.4 “Specifications (80-pin Version) (2/2)”, and Table 1.6 “Specifications (64-pin Version) (2/2)” note 1 added
		4	Table 1.3 “Specifications (80-pin Version) (1/2)” specification for A/D converter modified
		12-14	Figure 1.3 “M16C/5M, M16C/57 Group 100-Pin Block Diagram”, Figure 1.4 “M16C/5M, M16C/57 Group 80-Pin Block Diagram”, and Figure 1.5 “M16C/5M, M16C/57 Group 64-Pin Block Diagram” “Voltage detector”, “Power-on reset”, and “On-chip debugger” added
		24	Table 1.17 “Pin Functions (64-Pin, 80-Pin, and 100-Pin Packages)” “Three-phase motor control timer output” modified to “Three-phase motor control timer”; Note 1 added
			Special Function Registers (SFRs)
		33	Table 4.2 SFR List (2) “the VW2C3 bit” in note 2 modified to “bits VW2C2 and VW2C3”
		34	Table 4.3 SFR List (3) “A/D Conversion Interrupt Control Register” deleted from 004Dh
		83	Table 4.52 “Registers with Write-Only Bits” the order of registers changed; “CAN1 Receive FIFO Pointer Control Register”, “CAN1 Transmit FIFO Pointer Control Register”, “CAN0 Receive FIFO Pointer Control Register”, and “CAN0 Transmit FIFO pointer Control Register” added
			Resets
		87	Figure 6.1 “Reset Circuit Block Diagram” illustration for the VD2LS register added
			Voltage Detector
		100	Table 7.2 “Register List” notes 4 and 6 added; “the VW2C3 bit” in note 7 modified to “Bits VW2C2 and VW2C3”
		103	7.2.3 “Voltage Monitor Function Select Register (VWCE)” “PCR3” corrected to “PRC3”
		104	7.2.4 “Voltage Detector 2 Level Select Register (VD2LS)” RW for b7 to b4 modified to RW; Function for VD2LS0 to VD2LS3 modified; PCR3 corrected to “PRC3”
		106	7.2.6 “Voltage Monitor 2 Control Register (VW2C)” "The VW2C3 bit" in the 4th line modified to "Bits VW2C2 and VW2C3"
		108	7.3 “Optional Function Select Area” description for “programmed products” added
		108	7.3.1 “Option Function Select Address 1 (OFS1)” three lines below the register diagram deleted
		108	“LVDAS (Voltage Detector 0 Start Bit) (b6)” added
		84	7.4.1 “Digital Filter” “next sampling timing” modified to “third sampling timing” in the sixth line.
			Clock Generator
		116-118	8.1 “Introduction”, Table 8.1 “Clock Generator Specifications”, and Figure 8.1 “System Clock Generator” description for “Dedicated 125 kHz on-chip oscillator for watchdog timer” deleted (moved to 13. “Watchdog Timer”)
		121	“CM01-CM00 (Clock Output Function Select Bit) (b1-b0)” “the CM01 and CM00 bit settings enabled” in the second line modified to “selected by the CM01 and CM00 bit”
		122	“CM06 (Main Clock Division Select Bit) (b6)” description of the second bullet deleted
		124	“CM15 (XIN-XOUT Drive Level Select Bit) (b5)” description modified
		127	8.2.5 “Peripheral Clock Select Register (PCLKR)” Bit Name for PCLK0 corrected
		129	8.2.7 “Processor Mode Register 2 (PM2)” “PRC0” in the first line below the register diagram modified to “PRC1”
		138	Figure 8.5 “Peripheral Clocks” “LIN module” and “Serial bus interface” added
			Power Control
		148	“FMR01 (CPU Rewrite Mode Select Bit) (b1)” “FMSTP (Flash Memory Stop Bit) (b3)” “located in an area other than the flash memory” modified to “in the RAM”
		150	“FMR23 (Low-Current Consumption Read Mode Enable Bit) (b3)” the second paragraph modified

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0.20	Dec 25, 2009	159	Table 9.7 “Resets and Interrupts to Exit Wait Mode and Usage Conditions” usage conditions for “Multi-master I^2C bus” and “Voltage detection 0 reset” modified
		164	9.4 “Stopping Flash Memory” “an area other than the flash memory” modified to “the RAM”
			Processor Mode
		171	Table 10.2 “Register List” description for Processor Mode Register 2 deleted
		174	10.3 “Software Wait” note 1 deleted (moved to 31.1.5 and 31.4.5 “Flash Memory Electrical Characteristics”)
			Programmable I/O Ports
		176	11.2 “I/O Ports and Pins” diagrams for I/O ports revised; Table 11.3 “I/O Ports (Basic)” to Table 11.8 “I/O Ports (XC)” added
		189-190	11.3.7 to 11.3.9 “Input Threshold Select Register 0/1/2” description for the input level added
		196	11.4.2 “Priority Level of Peripheral Function I/O” added
		199	Table 11.12 “Unassigned Pin Handling in Single-Chip Mode” description for NC added
			Interrupts
		206	12.2.2 “Interrupt Control Register 1” the register diagram modified
		206	“IR (Interrupt Request Bit) (b3)” description modified to “Do not write 1 when the IR bit is 0”
		212	12.2.7 “Interrupt Source Select Register (IFSR)” function for IFSR6 and IFSR7 modified
		217	12.4.4 “INT Instruction Interrupt” interrupt numbers in the second line modified
		232	12.10 “Key Input Interrupt” the last sentence deleted
		235	12.13.2 “SP Setting” the second paragraph added
			Watchdog Timer
		239	Table 13.1 “Watchdog Timer Specification” “Dedicated 125 kHz on-chip oscillator for watchdog timer” added to fWDT
		240	Figure 13.1 “Watchdog Timer Block Diagram” “Dedicated 125 kHz on-chip oscillator for watchdog timer” added
		245	13.3.1 “Option Function Select Address 1 (OFS1)” three lines below the register diagram deleted
		246	13.3.2 “Option Function Select Address 2 (OFS2)” three lines below the register diagram deleted
		246	“WDTUFS1 to WDTUFS0 (Watchdog Timer Initial Set Bit) (b0-b1)” CSPR0 corrected to CSPRO
		249	13.4.3 “Count Source Protect Mode Enabled” description added below Table 13.4
			DMAC
		260	Table 14.4 “DMA Request Sources for DMA1” “Both edges of INT1” moved to 00111b
		261	Table 14.5 “DMA Request Sources for DMA2” “Both edges of INT2” moved to 00110b;”Timer B3” moved to 00111b; “Timer B4” moved to 01000b; “Timer B5” moved to 01001b
		262	14.3.2 “DMA Request” “interrupts” in the 12th line modified to “the interrupt control registers”
			Timer A
		272	Figure 15.2 “Timer A Configuration” “programmable output mode” deleted from Timer A0 and Timer A3
		284	“TA0TGH and TA0TGL (Timer A0 Event/Trigger Select Bit) (b7-b6)” “TA0GH to TA0GL” corrected to “TA0TGH to TA0TGL”
		295	15.3.1.3 “Count Source” the second paragraph deleted; the third paragraph modified
		295	Table 15.9 “Registers and the Setting in Event Counter Mode (When Not Processing Two-Phase Pulse Signal) (1)” setting for PCLKR, TCKDIVC0, and TACS0 to TACS2 modified to “- (setting unnecessary)”
		299	Table 15.11 “Registers and the Setting in Event Counter Mode (When Processing Two-Phase Pulse Signal) (1)” setting for PCLKR, TCKDIVC0, TACS0 to TACS2, TAiTGH to TAiTGL in ONSF modified to “- (setting unnecessary)”
			Timer B
		322	Note modified
		322	Table 16.1 “Specifications of Timer B” description for A/D trigger mode deleted
		325	Table 16.3 “Register List” Timer B2 Special Mode Register deleted
		295	16.3.1.3 “Count Source” the second paragraph deleted; the third paragraph modified
		338	Table 16.8 “Registers and the Setting in Event Counter Mode (1)” setting for PCLKR, TCKDIVC0, and TBCS0 to TBCS1 modified to “- (setting unnecessary)”
		341	Table 16.9 “Specifications of Pulse Period/Pulse Width Measurement Modes” specification for “Write to timer” the second bullet deleted
			Three-Phase Motor Control Timer
		362	17.2.8 “Timer B2 Special Mode Register (TB2SC)” description for b4 to b2 modified

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0.20	Dec 25, 2009	390	17.5.1 “Timer A, Timer B” the reference corrected
		390	17.5.2 “Forced Cutoff Input” RXD1, TXD1, LIN0OUT, and LIN0IN added
			Timer S
		—	“phase-delayed waveform” modified to “inverted waveform”
		—	Description of $\overline{\text{INT5}}$ and IDU deleted
		391	Table 18.1 “IC/OC Specifications” specification for Channel interrupts corrected
		397	“MOD1 and MOD0 (Operating Mode Select Bit) (b1-b0)” the second line modified
		400	18.2.5 “Base Timer Register (G1BT)” description added to function
		413	Table 18.5 “Base Timer Specifications” “while the base timer is counting” added to “Base timer reset value”; “and the BTS bit is 0” added to function for “Read from base timer” and “Write to base timer”
		418	18.3.2 “Base Timer Reset While Base Timer is Counting” the title changed
		428	Table 18.14 “Inverted Waveform Output Mode Specifications” “single-waveform” “single-phase waveform” in specifications for “Selectable functions” modified to “phase-delayed waveform”
		431	Table 18.15 “SR Waveform Output Mode Specifications” “(n > m)” added to specifications for output waveform; “single-phase waveform” in specifications for selectable function modified to “SR waveform”; Note 1 deleted
			Serial Interface UARTi (i = 0 to 4)
		477-491	21.1 “Registers” description for registers revised; Table 21.1 “Registers (1/2)” added; Register diagrams revised
		478	21.1.1 “Peripheral Clock Select Register (PCLKR)” added
		508	Table 21.11 “I/O Pin Functions in I^2C Mode” added
		511	Table 21.14 “I^2C Mode Functions” description for “Store received data” deleted; Notes 3 and 4 deleted; Description for “Read received data” modified
		517	21.5 “Special Mode 2 (UART2)” the third and fourth lines deleted
		517	Table 21.16 “Special Mode 2 Specifications” note 1 deleted
		518	Table 21.17 “I/O Pin Functions in Special Mode 2” added
		519	Table 21.18 “Registers and Settings in Special Mode 2 $^{(2)}$” function for CKDIR modified
		520	21.5.1 “Clock Phase Setting Function” the sixth and seventh lines deleted
		520	Diagrams for “Transmit and Receive Timing (CKPH = 0) in Slave Mode (External Clock)” and “Transmit and Receive Timing (CKPH = 1) in Slave Mode (External Clock)” deleted
		528	21.8 “Notes on Serial Interface UARTi (i = 0 to 4)” LIN0OUT and LIN0IN added
		528	21.8.1.1 “Transmission/Reception” “(i = 0 to 3)” added to the second line
		528	21.8.1.3 “Reception” “the RE bit” in the third paragraph corrected to “the RI bit”
		529	21.8.2.1 “Transmission/Reception” “(i = 0 to 3)” added to the second line
			Multi-Master I^2C-bus Interface
		530	Table 22.1 “Multi-Master I^2C Interface Specifications” description for “Timeout detection” in selectable functions modified
		531	Table 22.2 “Detections by I^2C Interface” function for slave address match modified
		536	“BC2 to BC0 (Bit counter) (b2 to b0)” description modified
		544	“WIT (Data Receive Interrupt Enable Bit) (b1)” "slave address transmission/reception" in the 12th line modified to "slave address reception"
		551	Table 22.9 “Functions by Write Access to the S10 Register” “Selects communication mode” divided into four modes
		553	“PIN (I^2C-bus Interface Interrupt Request Bit) (b4)” description added to the third bullet in “Conditions to become 0”
		557	Table 22.11 “CCR4 to CCR0 Bit Settings and Bit Rates (fVIIC = 4 MHz)” “167” in high-speed clock mode and “16.7” in standard clock mode modified to “166” and “16.6” respectively
		559	22.3.2 “Generation of Start Condition” description added to (2); “after the falling edge of the BB bit” in the 14th line modified to “after the BB bit changes from 1 to 0”
		563	Figure 22.10 “Start Condition Overlap Protect Operation” illustration for bits MST and TRX modified
		563	22.3.5 “Start Condition Overlap Protect” “and the S00 register” added to the second line below Figure 22.10
		565	22.3.6 “Arbitration Lost” description for (a) modified; The last paragraph added
		571	22.3.9 “Timeout Detection” description for the last bullet deleted
		573	22.3.10.2 “Master Transmission” “Check whether ACK presents” deleted from (B)
		574	22.3.10.3 “Master Reception” “Check whether ACK presents” deleted from (B)
		575	22.3.10.4 “Slave Reception” (2) deleted from (A); “1 (no ACK presents)“ modified to “0 (ACK presents)“; (2) added to (c)
		573	22.3.10.5 “Slave Transmission” “Check whether ACK presents” deleted from (B)

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0.20	Dec 25, 2009	578	Table 22.15 “I2C-bus Interrupt” “Completion of transmitting slave address“ deleted from interrupt source
		580	22.5.2.6 “S10 Register” the third line modified
			Serial Bus Interface
		581-614	This chapter revised; register diagrams modified
		581	Table 23.1 “Registers” added
		596	23.3.2 “Synchronous Serial Communication Mode” five lines above Table 23.2 deleted
		614	Table 23.7 “Serial Bus Interface Related Register” added; description below Table 23.7 added
			A/D Converter
		732	Table 26.1 “A/D Converter Specifications” specification for “Integral nonlinearity error” modified
		735	26.2 “Registers” description for the PCR register deleted
		739	26.2.4 “A/D Control Register 0 (ADCON0)” CKS0 (Frequency Select Bit 0) (b7) “Set the CKS3 bit before selecting the bits CKS0 to CKS2” added
		630	26.3.1 “A/D Conversion Cycle” “Divide fAD so ϕAD conforms the standard frequency.” added
			CRC Calculator
		766	28.1 “Introduction” the last sentence deleted
		766	Figure 28.1 “CRC Calculator Block Diagram” modified
		767	28.2 “Registers” the order of register diagrams changed
			Flash Memory
		775	“FMR00 (RY/BY status flag) (b0)” two conditions added to “Conditions to become 0”
		776	“FMR02 (Lock bit disable select bit) (b2)” the last sentence added
		781	“FMR60 (EW1 mode select bit) (b0)” the last sentence added
		787	29.8 “CPU Rewrite Mode” the third paragraph for the suspend function added
		787	Table 29.10 “EW0 Mode and EW1 Mode” “Mode after program or erase” modified to “Mode after program/erase, or during program/erase suspend”; “and bits FMR32 and FMR33 in the FMR3 register” added to the both modes for flash memory status detection
		790	Figure 29.4 “Suspend Request” “suspend is requested” modified to “request a suspend”
		797	Figure 29.12 “Block Blank Check Command” “command sequence error” detection added
		797	29.8.4.8 “Block Blank Check Command” two paragraphs added below Figure 26.12
		799	Table 29.16 “Errors and FMR0 Register States” “block blank check, or read lock bit status” added to error occurrence conditions for command sequence error
		800	29.8.5.2 “Handling Procedure for Errors” the seventh line in “Erase error” added
		802-804	Figure 29.15 “Program Flowchart in EW0 Mode (Suspend Function Enabled)” to Figure 29.17 “Lock Bit Program Flowchart in EW0 Mode (Suspend Function Enabled)” “Wait td(SR-SUS)” added
		813	Table 29.18 “Forced Erase Function” “No ID match” added to function for “0 (ROM code protect enabled)”
		816	29.9.5 “Standard Serial I/O Mode 2” “The main clock is used” added
		816	Table 29.21 “Pin Functions (Flash Memory Standard Serial I/O Mode 2)” “when the main clock is used” deleted from description for XIN and XOUT
		819	29.10.3.10 “Software Command” (e) added
			E2PROM Emulation Data Flash
		820-830	This chapter revised; diagrams revised
		821	Table 30.2 “Register List” added
		829	30.5 “Interrupt” added
		829	30.6 “Notes on E2PROM Emulation Data Flash” added
			Electrical Characteristics
		59-83	This chapter revised; pins in tables for “Absolute Maximum Ratings”, “Operating Conditions”, and “Electrical Characteristics (1)” modified
		59	Table 31.1 “Absolute Maximum Ratings” “Analog reference voltage” added; Note 1 added
		60, 863	Table 31.2 and Table 31.48 “Operating Conditions (1)” “High peak output current” and “Low peak output current” added
		833, 864	Table 31.3 and Table 31.49 “Recommended Operating Conditions (2/2) (1)”, and Figure 31.2 and Figure 31.25 “Ripple Waveform” added
		834, 865	Table 31.4 and Table 31.50 “A/D Conversion Characteristics (1)” “A/D operating clock frequency” added; Note 3 added
		835	31.1.4 “D/A Conversion Characteristics” added
		836	Table 31.6 “CPU Clock When Operating Flash Memory ($f_{(BCLK)}$)” “(wait state)” in note 2 modified to “one wait”
		837, 868	Table 31.7 and Table 31.53 “Flash Memory (Program ROM 1, 2) Electrical Characteristics” conditions for read voltage added

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0.20	Dec 25, 2009	839	31.1.6 “E2PROM Emulation Data Flash” added
		838	Table for “Low Voltage Detection Circuit Electrical Characteristics” replaced by Table 31.10 “Voltage Detector 0 Electrical Characteristics” and Table 31.11 “Voltage Detector 2 Electrical Characteristics”
		841	Figure 31.4 and Figure 31.27 “Power-On Reset Circuit Electrical Characteristics” t_{fth} modified
		841	Table 31.13 “Power Supply Circuit Timing Characteristics” moved to below Figure 31.4; “td(E-A)” deleted (moved to Table 31.10 and Table 31.11); Maximum value for td(W-S) modified to “300”
		842, 873	Figure 31.5 and Figure 31.28 “Power Supply Circuit Timing Diagram” “VC26” modified to “VC25”
		842, 873	Table 31.14 and Table 31.60 “On-chip Oscillator Oscillation Circuit Electrical Characteristics” conditions added below the table title; Minimum value and maximum value for f_{OCO40M} modified to “32” and “48” respectively
		843, 854, 874, 882	Table 31.15, Table 31.32, Table 31.61, and Table 31.76 “Electrical Characteristics (1)” “SCL, SDA”, and “TA2OUT“ modified to “SCL2, SDA2”, and “TA0OUT” respectively; “ZP, IDU, IDW, IDV, SD, INPC1_0 to INPC1_7, SSI0, SSCK0, $\overline{SCS0}$, LIN0IN, CRX0, CRX1” added to parameter for V_{T+}-V_{T-}
		844, 855, 875, 883	Table 31.16, Table 31.33, Table 31.62, and Table 31.77 “Electrical Characteristics (3)” “During flash memory program” and “During flash memory erase” added
		845, 856, 876, 884	31.2.2.1, 31.3.2.1, 31.5.2.1, and 31.6.2.1 “Reset Input ($\overline{RESET}$ Input)” added; Table 31.17, Table 31.34, Table 31.63, Table 31.78 “Reset Input ($\overline{RESET}$ Input)” and Figure 31.6, Figure 31.16, Figure 31.29 Figure 31.37 “Reset Input ($\overline{RESET}$ Input)” added
		845-849	Figure 31.7 “External Clock Input (XIN Input)” to Figure 31.12 “External Interrupt $\overline{INTi}$ Input” added (replaced Timing Diagram (1) and (2))
		850, 861	Figure 31.13, Figure 31.23, Figure 31.36, and Figure 31.44 “Multi-master I^2C-bus” the title changed
		851	31.2.2.8 “Serial bus interface” added
		852	Figure 31.14 “Timing of Serial Bus Interface” added
		853	Figure 31.15 “Switching Characteristic Measurement Circuit” added
		856-860	Figure 31.17 “External Clock Input (XIN Input)” to Figure 31.22 “External Interrupt $\overline{INTi}$ Input” added (replaced Timing Diagram (1) and (2))
		871	Table for “Low Voltage Detection Circuit Electrical Characteristics” replaced by Table 31.56 “Voltage Detector 0 Electrical Characteristics” and Table 31.57 “Voltage Detector 2 Electrical Characteristics”
		872	Table 31.59 “Power Supply Circuit Timing Characteristics” moved to below Figure 31.25; “td(E-A)” deleted (moved to Table 31.56 and Table 31.57); Maximum value for td(W-S) modified to “300”
		876-880	Figure 31.30 “External Clock Input (XIN Input)” to Figure 31.35 “External Interrupt $\overline{INTi}$ Input” added (replaced Timing Diagram (1) and (2))
		884-888	Figure 31.38 “External Clock Input (XIN Input)” to Figure 31.43 “External Interrupt $\overline{INTi}$ Input” added (replaced Timing Diagram (1) and (2))
			Usage Notes
		890	32.1 “OFS1 Address, OFS2 Address, and ID Code Storage Address” “OFS2 address” added to the title and the ninth line; “set FFh to the OFS2 address”, “org 0FFDBH“, and “byte 0FFh“ added to description for example
		892	Table 32.1 “Registers with Write-Only Bits” the order of registers changed; “CAN1 Receive FIFO Pointer Control Register”, “CAN1 Transmit FIFO Pointer Control Register”, “CAN0 Receive FIFO Pointer Control Register”, and “CAN0 Transmit FIFO pointer Control Register” added
		902	32.9.2 “SP Setting” the second paragraph added
		916	32.14.1 “Timer A, Timer B” the reference corrected
		916	32.14.2 “Forced Cutoff Input” RXD1, TXD1, LIN0OUT, and LIN0IN added
		923	32.18 “Notes on Serial Interface UARTi (i= 0 to 4)” LIN0OUT and LIN0IN added
		923	32.18.1.1 “Transmission/Reception” “(i = 0 to 3)” added to the second line
		923	32.18.1.3 “Reception” “the RE bit” in the third paragraph corrected to “the RI bit”
		924	32.18.2.1 “Transmission/Reception” “(i = 0 to 3)” added to the second line
		925	32.19.2.6 “S10 Register” the third line modified
		929	32.22 “Notes on D/A Converter” added
		931	32.23.3.10 “Software Command” (e) added
1.01	Jul 22, 2010	**Overall**	
		Overall	Changed table titles from “Register List“ to “Registers”.
		Overall	Changed terms from “fOCOF” and “fOSO-S” to “on-chip oscillator clock”.
		Overall	00A1h E^2dataFlash Status Register 0: Changed the reset value from 00h.
		Overall	D400h to D41Fh: Changed the register name from “CAN1 Acceptance Mask Register i” to “CAN1 Mask Register i”

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1.01	Jul 22, 2010	Overall	03DCh D/A Control Register: Changed the reset value from XXXX XX00b.
		Overall	03F3h Port P9 Direction Register: Changed the rest value from 000X 0000b.
		Overview	
		3	Table 1.2 Specifications (100-pin Package) (2/2): • Added "E^{2}dataFlash" to note 1. • Changed the Specification column for current consumption from TBD.
		5	Table 1.4 Specifications (80-pin Package) (2/2): Added "E^{2}dataFlash" to note 1.
		7	Table 1.6 Specifications (64-pin Package) (2/2): Added "E^{2}dataFlash" to note 1.
		12-14	Figure 1.3, Figure 1.4, Figure 1.5 Block Diagram (100-pin, 80-pin, 64-pin): • Deleted "8-bit" from the description for the UART/clock synchronous serial interface. • Added "(1 channel)" to the description for the Multi-master I^{2}C-bus. • Added "(1)" to the CAN module and E^{2}dataFlash. • Moved "dedicated 125 kHz on-chip oscillator for the watchdog timer" to description for the watchdog timer. • Added "(8-bit x 1 circuit)" to the description for the D/A converter. • Unified note 1 and note 2, and added description for the CAN module and E^{2}dataFlash to note 1.
		15, 18, 21	Figure 1.6, Figure 1.7, Figure 1.8 Pin Assignments (100-pin, 80-pin, 64-pin): Added TSUDA and TSUDB to P8_0 and P8_1, respectively.
		16, 19, 22	Table 1.11, Table 1.13, Table 1.15 Pin Names (1/2) (100-pin, 80-pin, 64-pin): Added TSUDA and TSUDB to P8_0 and P8_1, respectively.
		24	Table 1.17 Pin Functions (64-Pin, 80-Pin, and 100-Pin Packages): • Deleted "pin" or "pins" from "input pin/pins" and "output pin/pins". • Added "Pins" to "AVCC and AVSS" in the Description column of Analog power supply. • Added "via a resistor" to the Description column of CNVSS. • Added "(1)" to the Description column of the Sub clock input/output. • Deleted "$\overline{\text{INT2}}$ is used to input Zphase of timer A" from the Description column of the $\overline{\text{INT}}$ interrupt input. • Added UART0 to UART3 to the Signal Name column of the Serial interface. • Added UART2 to the Signal Name column of I^{2}C mode.
		25	Table 1.18 Pin Functions (64-Pin, 80-Pin, and 100-Pin Packages): • Deleted "pin" or "pins" from "input pin/pins" and "output pin/pins". • Added "TSUDA, TSUDB" to the Pin Name column of Timer S. • Changed "Input pin" and "Output pin" to "Receive data input" and "Transmit data output" in the Description column of the CAN Module, respectively. • Changed "4 input ports" to "4 bits" in the Description column of the I/O port.
		26	Table 1.19 Pin Functions (100-Pin Package Only): • Changed "4 input ports" to "4 bits" in the Description column of the I/O port. • Changed "Timer" to "Timer B" in the Signal Name column.
		26	Table 1.21 Pin Functions (100-Pin and 80-Pin Package Only): • Changed "4 input ports" to "4 bits" in the Description column of the I/O port.
		Memory	
		30	3. Memory: Changed the description for E^{2}dataFlash.
		31	Figure 3.1 Memory Map: • Deleted "E^{2}dataFlash" and "15000h" • Added "ID code write address", "OFS1 address", and "OFS2 address". • Added note 2. • Added note symbols "(1)" and "(2)".
		Special Function Registers (SFRs)	
		79	4.2.1 Register Settings: Added the description for read-modify-write instructions.
		80	Table 4.49 Read-Modify-Write Instructions: Added
		Protection	
		81	5.2.1 Protect Register (PRCR): Changed the description for bit 7 in the register diagram. Added the description for PRC7 to the explanation about protect bits.
		Reset	
		Chap. 6	Changed "oscillation stop detection reset" to "oscillator stop detect reset".
		85	Table 6.3 Registers: Added note 1.
		92	6.4.2 Hardware Reset: Changed "20 fOCO-S cycles" to "$\frac{1}{fOCO-S} \times 20$ cycles" in (4) for "When the power is turned on".
		96	Figure 6.6 SVCC Timing: Added the title.
		Voltage Detector	
		101	7.2.3 Voltage Monitor Function Select Register (VWCE): Changed "voltage detector 2" to "voltage monitor 2".

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1.01	Jul 22, 2010	112	Figure 7.6 Voltage Monitor 2 Interrupt/Reset Operation Example: Added “or above” to note 1.
		Clock Generator	
		114	Table 8.1 Clock Generator Specifications: Changed the description for the Clock frequency row.
		115	Figure 8.1 System Clock Generator: Changed a part of the main clock.
		118	8.2.2 System Clock Control Register 0 (CM0): • Deleted I/O port names from the Function column. • Modified bit explanations. • Added description for 40 MHz on-chip oscillator mode to the CM05 bit explanation.
		120	8.2.3 System Clock Control Register 1 (CM1): • Changed “XIN-XOUT drive level select bit” to “XIN-XOUT drive capacity select bit”. • Added “The PLC07 bit in the PLC0 register is 1 (PLL on).” and “A low is input to the $\overline{\text{NMI}}$ pin.” to the CM10 bit explanation.
		122	8.2.4 Oscillation Stop Detection Register (CM2): Modified bit explanations.
		124	8.2.5 Peripheral Clock Select Register (PCLKR): Modified the bit explanation.
		125	8.2.6 PLL Control Register 0 (PLC0): Modified bit explanations.
		126	8.2.7 Processor Mode Register 2 (PM2): • Corrected typo “CM20 register” to “CM2 register” in the PM21 bit explanation. • Added “Once the PM21 bit is set to 1, it cannot be set to 0 by a program (writing 0 has no effect)” to the PM21 bit explanation.
		127	8.2.8 40 MHz On-Chip Oscillator Control Register 0 (FRA0): Changed the bit name from “40 MHz on-chip oscillator select bit” to “On-chip oscillator select bit”.
		129	8.3.1 Main Clock: • Changed “oscillator” to “ceramic resonator or crystal”. • Changed the title of Figure 8.2 Main Clock Connection Example.
		130	Figure 8.3 Relation between Main Clock and PLL Clock: Changed note 2.
		131	8.3.4 fOCO-F: Changed the description for the clock division in the first sentence.
		131	8.3.5 125 kHz On-Chip Oscillator Clock (fOCO-S): • Added the description for “when the CSPRO bit in the CSPR register is 1” to the first paragraph. • Changed “the CM14 bit becomes 1” to “the CM14 bit becomes 0” in the last paragraph.
		132	Figure 8.4 Sub Clock Connection Example: Changed the title.
		133	8.4.1 CPU Clock and BCLK: • Added “fOCO-F” to the third paragraph. • Deleted the description for the clock division when fOCO-F is selected as the clock source for the CPU clock. • Changed the description for “when entering stop mode”.
		133	8.4.2 Peripheral Function Clocks (f1, fOCO40M, fOCO-F, fOCO-S, fC32, fC): • Changed “fOCO-F divided by 2, 4, or 8” to “fOCO-F divided by 1 (no division)”. • Deleted the A/D converter from description for fOCO-F. • Added the description about the PM25 bit to the explanation for fC.
		135	8.6 System Clock Protection Function: Modified the description.
		136	8.7.1 Operation When CM27 Bit is 0 (Oscillator Stop Detect Reset): Added “voltage monitor 0 reset” to the description for status cancellation.
		138	8.7.3 Using the Oscillator Stop/Restart Detect Function: Moved the description of the first, second, and fourth bullets in the previous version to 8.8 Interrupt.
		138	8.8 Interrupt: Added the description about the detect flag for oscillator stop/restart detect.
		142	8.9.5 PLL Frequency Synthesizer: Changed “to meet the power supply ripple standard” to “within to the acceptable range of power supply ripple”.
		Power Control	
		145	9.2.2 Flash Memory Control Register 2 (FMR2): Modified the first sentence and corrected typos “(slow read mode disabled)” to “(low current consumption read mode disabled” in the explanations about bits FMR22 and FMR23.
		146	9.3.1.3 40 MHz On-Chip Oscillator Mode: Changed the description for the clock division of fOCO-F in the first paragraph.
		147	9.3.1.6 Low-Speed Mode: Deleted “divided by 2, 4, or 8” from the second paragraph.
		147	9.3.1.7 Low Power Mode: Changed “middle speed (divide-by-8) mode” to “the divide-by-8 mode”.
		148	Table 9.2 Clocks in Normal Operating Mode: Changed “fOCO-F divided by 2, 4, or 8” to “fOCO-F divided by 1”.
		151	9.3.2 Clock Mode Transition Procedure: Added “low-speed mode” to e.

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1.01	Jul 22, 2010	158	Table 9.10 CPU Clock After Exiting Stop Mode • Changed the description for the clock division of fOCO-F. • Deleted note 1.
		153, 155	9.3.3.4 Exiting Wait Mode: • Changed “Voltage detector 0 reset”, “Voltage detector 2 reset,” and “Voltage detector 2 interrupt” to “voltage monitor 0 reset”, “voltage monitor 2 reset”, and “voltage monitor 2 interrupt”, respectively, in the paragraph below Table 9.7. • Changed the order of settings in the second paragraph below Table 9.7.
		156	9.3.4.1 Entering Stop Mode: Deleted “However, when the PM21 bit in the PM2 register is 1 (disables a clock change) or when the CSPRO bit in the CSPR register is 1 (watchdog timer count source protect mode enabled), writing the CM10 bit has no effect and the MCU does not enter stop mode.” from the first paragraph.
		157	9.3.4.3 Exiting Stop Mode: • Changed “Voltage detector 0 reset” and “Voltage detector 2 interrupt” to “voltage monitor 0 reset” and “voltage monitor 2 interrupt”, respectively, in the paragraph below Table 9.9. • Added a sentence before (1). • Changed the order of settings in the second paragraph below Table 9.9. • Changed “the peripheral function interrupts or NMI interrupt” to “an interrupt” in the paragraph after (3).
		159	9.4 Power Control in Flash Memory: Added the title.
		159	Figure 9.2 Stop and Restart of the Flash Memory: • Changed “Oscillate main clock” to “Start oscillating main clock or 40 MHz on-chip oscillator”. • Deleted “program A”.
		161	9.4.2.2 Low Current Consumption Read Mode: Deleted “To enter low current consumption read mode, set or the sub clock or fOCO-S divided by 8 or 16 as the CPU clock”.
		164	9.6.3 Stop Mode: • Added “(stop mode)” to and deleted “(all clock stop)” from the third bullet.
		Processor Mode	
		167	10.2.2 Program 2 Area Control Register (PRG2C): Added “Refer to 29.7 "User Boot Function" for details.” to the PRG2C0 bit explanation.
		169	10.4 Bus Hold: Added.
		Programmable I/O Ports	
		175	Figure 11.5 I/O Ports (NMI): Changed the figure.
		181	11.3.4 Pull-Up Control Register 1 (PUR1): Changed the description for b3 to b0.
		182	11.3.5 Pull-Up Control Register 2 (PUR2): • Changed “P9_4” to “P9_3” in the Bit Name column of the PU22 bit. • Changed “P9_5” to “P9_4” in the Bit Name column of the PU23 bit.
		185	11.3.8 Input Threshold Select Register 1 (VLT1): Changed the description for b3 to b0.
		185	11.3.9 Input Threshold Select Register 2 (VLT2): Changed the Bit Name column of VLT22 and VLT23.
		188	11.3.12 Port Pi Direction Registers (PDi) (i = 0 to 10): Changed the reset value for PD9 from “000X 0000b“.
		192	Figure 11.10 Unassigned Pin Handling Ports: Changed “P0 to P3, P6 to P10” to “Ports P0 to P10”.
		193	11.6.2 Influence of $\overline{SD}$: Changed the description.
			Interrupts
		Chap. 12	Changed “Oscillation stop/restart detection” to “Oscillator stop/restart detect”.
		194	Table 12.2 I/O Pins: Changed “i = 0 to 5” to “i = 0 to 7” below the table.
		196	Table 12.4 Registers (2/2): • Added “CAN 1 Wakeup Interrupt Control Register” to the Register column of 0073h. • Added “CAN 1 Error Interrupt Control Register” to the Register column of 0074h.
		198, 199	12.2.2 Interrupt Control Register 1 and 12.2.3 Interrupt Control Register 2: Moved to the description for symbols and addresses to tables below the register diagram.
		199	12.2.3 Interrupt Control Register 2: Changed “IFSR43” to “IFSR45” in the explanations about bits IR and POL.
		201	12.2.4 Interrupt Source Select Register 4 (IFSR4A): Changed “LIN” to “LIN0” in the Function column of IFSR45.
		202	12.2.5 Interrupt Source Select Register 3 (IFSR3A): Changed “($\overline{INT7}$ to $\overline{INT6}$ Interrupt Polarity Switch Bit)” to “($\overline{INT7}$ and $\overline{INT6}$ interrupt polarity select bit)” in the explanation about bits IFSR31 and IFSR30.
		204	12.2.7 Interrupt Source Select Register (IFSR): • Changed “Interrupt source select bit” to “Interrupt request source select bit” in the Bit Name column of IFSR6 and IFSR7. • Changed “($\overline{INT5}$ to $\overline{INT0}$ Interrupt Polarity Switch Bit)” to “($\overline{INT5}$-$\overline{INT0}$ interrupt polarity select bit)” in the explanation about bits IFSR5 to IFSR0.

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1.01	Jul 22, 2010	210	12.5.1.3 Watchdog Timer Interrupt: Changed “initialize the watchdog timer” to “refresh the watchdog timer”
		211	12.6.1 Fixed Vector Tables: Changed “used by the ID code check function” to “used for the ID code check function and OFS1 address”.
		214	12.7.1.2 IR Bit: Added the second paragraph.
		215	Figure 12.3 Time Required for Executing Interrupt Sequence: Changed “accept instructions” to “prefetch” in note 1.
		221	12.10 Key Input Interrupt: Changed the description.
		222	12.11 Address Match Interrupt: Deleted the five lines before Table 12.11.
		225	Figure 12.11 Procedure for Changing the Interrupt Generate Source: Changed “for the interrupt” to “in the interrupt control register” in note 2.
		226	12.13.5 Rewriting the Interrupt Control Register: Changed “no requests for” to “no interrupt requests corresponding to” in the first bullet.
		227	12.13.7 $\overline{\text{INT}}$ Interrupt: Added the third bullet.
		Watchdog Timer	
		Chap. 13	Changed “Watchdog timer counter reset value conditions” to “Watchdog timer counter refresh timing”.
		228	Table 13.1 Watchdog Timer Specifications: Changed the description for Prescaler divide ratio in the Selectable functions row.
		229	Figure 13.1 Watchdog Timer Block Diagram: Corrected typos “WDTC” to “WDC”.
		231	13.2.1 Voltage Monitor 2 Control Register (VW2C): • Deleted “voltage monitor 1 reset” from the description under the register diagram. • Deleted the first bullet from the description for Conditions to become 0 in the VW2C3 bit explanation.
		232	13.2.2 Count Source Protection Mode Register (CSPR): Changed description for b6 to b0 from “Reserved bits” in the register diagram.
		236	13.4.1 Refresh Operation Period: Deleted a sentence before Figure 13.2.
		DMAC	
		241	Table 14.1 DMAC Specifications: • Corrected typo “DMAiCON” to “DMiCON” in the Specifications column of DMA transfer start. • Changed “SARi or DARi pointer” to “SARi or DARi register” in Specifications of Reload timing for forward address pointer and DMAi transfer counter
		242	Figure 14.1 DMAC Block Diagram: Unified “Data bus low-order bits” and “Data bus high-order bits”.
		248-249	Table 14.3 to Table 14.6 Source of DMA Request: Changed “$\overline{\text{INT}}$i” to “the $\overline{\text{INT}}$i pin”. Changed “SS0 Receive register full” to “SS0 receive data register full”. Changed “SS0 Transmission register empty” to “SS0 transmit data register empty”.
		250	Table 14.7 Timing at Which the DMAS Bit Value Changes: Changed the description for the peripheral function.
		251	14.3.3 Transfer Cycles: Added “and the source and destination addresses are both odd addresses”.
		256	Figure 14.5 DMA Transfer Initiated by External Sources: Changed “DMAS bit in DMA0” and “DMAS bit in DMA1” to “DMAS bit in the DM0CON register” and “DMAS bit in the DM1CON register”, respectively.
		Timer A	
		259	Figure 15.1 Timer A and B Count Sources: Deleted the divide-by-2 circuit on fOCO-F.
		260	Figure 15.2 Timer A Configuration: • Added note 1 and “i = 0 to 4”. • Corrected typo “TAiGH to TAiGL” to “TAiTGH to TAiTGL”.
		265	15.2.4 Timer A Count Source Select Register i (TACSi) (i = 0 to 2): Changed the title.
		272	15.2.11 One-Shot Start Flag (ONSF): Changed the last sentence of the TA0TGH-TA0TGL bit explanation.
		273	15.2.12 Trigger Select Register (TRGSR): Changed the last sentence of the bit explanation about bits TA1TGH-TA1TGL, TA2TGH-TA2TGL, TA3TGH-TA3TGL, and TA4TGH-TA4TGL.
		277	15.3.1.3 Count Source: Changed "fOCO-F divided by 2, 4, or 8" to "fOCO-F divided by 1 (no division)".
		279, 283, 287, 292, 296	Table 15.7, Table 15.9, Table 15.11, Table 15.13, and Table 15.15 Registers and Settings: • Added TAOW • Changed “TAiTGH and TAiTGL” to “TA0TGH to TA0TGL” in the Bit column of ONSF.
		282	Table 15.8 Event Counter Mode Specifications (When Not Using Two-Phase Pulse Signal Processing): • Deleted “by a program” from the first bullet in the Count source row. • Added “When selecting reload type:” to the Specification column of Number of counts.

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1.01	Jul 22, 2010	286	Table 15.10 Event Counter Mode Specifications (When Processing Two-Phase Pulse Signal with Timers A2, A3, and A4): • Changed “free-running mode” to “free-run type” in the Count operations row. • Added “When selecting reload type:” to the Specification column of Number of counts.
		290	Figure 15.9 Relationship between the Two-Phase Pulse (A-Phase and B-Phase) and the Z-Phase: Added “(Z phase)”.
		291	Table 15.12 One-Shot Timer Mode Specifications: • Changed “continues” to “restarts” in the third bullet in the Count operations row. • Changed “(timer starts)” to “(one-shot timer start)” in the fifth bullet in the Count start condition row.
		295	Table 15.14 PWM Mode Specifications: Deleted “When the MR2 bit in the TAiMR register is 0:” and “When the MR2 bit in the TAiMR register is 1:” from the Count start condition row.
		300	15.3.7 Programmable Output Mode (Timers A1, A2, and A4): Added “0” to bit 5 in the programmable output mode timer Ai mode register diagram.
		305	15.5 Notes on Timer A: Revised. • Added 15.5.1 Common Notes on Multiple Modes. • Added lines 5 and 6 to 15.5.1.1 Register Setting. • Added 15.5.1.2 Event or Trigger. • Changed the description of 15.5.1.3 Influence of $\overline{SD}$.
		Timer B	
		309	Figure 16.1 Timer A and B Count Sources: Deleted the divide-by-2 circuit on fOCO-F.
		309	Table 16.1 Timer B Specifications: Changed “3” to “6” in the interrupt source row.
		311	Figure 16.3 Timer B Block Diagram: • Added description for “PPWFS22 to PPWFS20”. • Changed TBCS1 to TBCS3 in the description for bits TCS0 to TCS7. • Added “and j = 5 if i = 3” above the table. • Added “Timer B3”,”Timer B4”, and Timer B5” to the table.
		311	Table 16.2 I/O Ports: Changed “corresponding to the pin” to “sharing the same pin” in note 1.
		314	16.2.3 Timer Bi Register (TBi) (i = 0 to 5): Added “fj : Count source frequency” to the register diagram.
		316	16.2.5 Pulse Period/Pulse Width Measurement Mode Function Select Register i (PPWFSi) (i = 1, 2): • Corrected typos “TB11” and “TB1” to “TB1” and “TB11”, respectively, in the description for “1” in the Function column of PPWFS11. • Corrected typos "TB21" and "TB2" to "TB2" and "TB21", respectively, in the description for "1" in the Function column of PPWFS12.
		322	16.3.1.3 Count Source: Changed "fOCO-F divided by 2, 4, or 8" to "fOCO-F divided by 1 (no division)".
		324, 327, 331, 332	Figure 16.4, Figure 16.5, Figure 16.6, and Figure 16.7 Operation Example: Changed “TBiS bit in the TABSR register” to “TBiS bit in the TABSR register or TBSR register”.
		325	Table 16.8 Registers and Settings in Event Counter Mode (1): Changed “TBCS1” to “TBCS3” in the Register column.
		326	16.3.3 Event Counter Mode: • Changed “TBj overflow or underflow” to “Timer Bj” in the Function column of TCK1 in the register diagram. • Added the TCK1 bit explanation.
		328	Table 16.9 Specifications of Pulse Period/Pulse Width Measurement Modes: • Moved previous note 3 to the description for TBiS before notes. • Added a note (note 3)
		329	Table 16.10 Registers and Settings in Pulse Period/Pulse Width Measurement Modes (1): Added “or PPWFS2” to the Function and Setting column of TBi1.
		330	16.3.4 Pulse Period/Pulse Width Measurement Modes: Deleted the title before the register diagram.
		331, 332	Figure 16.6 and Figure 16.7 Operation Example in Pulse Width Measurement Mode: Added “and PPWFS22 to PPWFS20” and “and PPWFS2” to the second bullet.
		334	16.5 Notes on Timer B: Revised. • Added 16.5.1 Common Notes on Multiple Modes. • Added 16.5.3.2 Event. • Added 16.5.4.3 Event or Trigger.
		Three-Phase Motor Control Timer	
		Chap. 17	Changed “Three-Phase Motor Control Timer” to “Three-Phase Motor Control Timer Function”
		375	17.5.2 Influence of $\overline{SD}$: Changed the section title and description.
		Timer S	
		Chap. 18	Changed “P8_0” and “P8_1” to ”TSUDA” and “TSUDB”, respectively.

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1.01	Jul 22, 2010	376	Table 18.1 IC/OC Specifications: Added “j = 0 to 7” below the table.
		377	Figure 18.1 IC/OC Block Diagram: • Added the 40 MHz on-chip oscillator to the clock generator. • Added description of bits FRA01 and CM21.
		378	Table 18.2 I/O Pins: Added pins TSUDA, TSUDB, and $\overline{\text{INT1}}$
		381	18.2.2 Waveform Generation Register j (G1POj) (j = 0 to 7): Changed the description in lines 1 and 2 under the register diagram.
		382	18.2.3 Waveform Generation Control Register j (G1POCRj) (j = 0 to 7) Changed the last sentence of the explanation about bits MOD1 and MOD0.
		384	18.2.4 Time Measurement Control Register j (G1TMCRj) (j = 0 to 7): Added “internal circuit” to the last sentence of the explanation about bits GT, GOC, and GSC.
		385	18.2.5 Base Timer Register (G1BT): Added “the state is released” to line 9 under the register diagram.
		386	18.2.6 Base Timer Control Register 0 (G1BCR0): Changed lines 1 to 4 in the explanation about bits BCK1 and BCK0.
		387	18.2.7 Base Timer Control Register 1 (G1BCR1): • Added “while the RST1 bit is 1” to line 3 in the RST1 bit explanation. • Changed the BTS bit explanation. Added “(increment mode)” and “(increment/ decrement mode)” to the last sentence in the explanation about bits UD1 and UD0.
		388	18.2.8 Time Measurement Prescaler Register j (G1TPRj) (j = 6 and 7): Changed the first sentence of the description under the register diagram.
		389	18.2.9 Function Enable Register (G1FE): Changed the first sentence of the description under the register diagram.
		391	18.2.11 Base Timer Reset Register (G1BTRR): Changed the description in lines 1 and 2 under the register diagram.
		392	18.2.13 Waveform Output Master Enable Register (G1OER): Changed “set the EOCj bit to 0” to “set the EOCj bit to 1” in line 4 under the register diagram.
		393	18.2.14 Timer S I/O Control Register 0 (G1IOR0): Changed the first sentence of the description under the register diagram.
		394	18.2.15 Timer S I/O Control Register 1 (G1IOR1): Changed the first sentence of the description under the register diagram.
		395	18.2.16 Interrupt Request Register (G1IR): Changed the description under the register diagram.
		398	Table 18.5 Base Timer Specifications: • Changed the first bullet in the Specification column of the Write to base timer. • Deleted the last 4 lines of the second bullet in the Specification column of the Selectable functions.
		399	Table 18.6 Base Timer Associated Registers (Time Measurement/Waveform Generation Function): Changed “Select a base timer timing” to “Select a base timer reset timing” in the Function column of RST4
		403	Figure 18.7 Base Timer Reset with the G1PO0 Register: • Corrected typo from “G1IR0 register” to “G1IR0 bit in the G1IR register” • Changed “base timer interrupt” and “channel 0 interrupt” to “IC/OC base timer interrupt request” and “IC/OC channel 0 interrupt request”, respectively.
		404	Figure 18.8 Base Timer Reset with $\overline{\text{INT1}}$ Pin Input: Changed note 2.
		404	Table 18.7 In Increment Mode: Deleted “Increment Operation”.
		405	18.4 Time Measurement Function: Changed line 1.
		405	Table 18.10 Time Measurement Function Specifications: Deleted “the interrupt request is generated” from the Specification column of Interrupt request.
		406	Figure 18.9 Time Measurement Function (1/2): Changed “at falling edge” to “at rising edge” in the first bullet.
		407	Figure 18.10 Time Measurement Function (2/2): Added “However, values in the G1TMj register change.” to note 2 in (2).
		409	18.5 Waveform Generation Function: Changed line 1.
		409	Table 18.12 Waveform Generation Associated Registers and Settings: Changed “Select output disabled” to “Select output enabled in the Function column of G1OER.
		413	18.5.2 Inverted Waveform Output Mode: Changed description in line 3 to 5.
		416	18.5.3 Set/Reset Waveform Output Mode (SR Waveform Output Mode): Changed “G1POCRi register (i = 0 to 7)” to “G1POCRj register (j = 0, 2, 4, 6)” in line 1.
		421	18.7 Interrupts: Changed lines 6 to 7.
		423	18.8.1 Register Access: Added.
		423	18.8.2 Changing the G1IR Register: Changed the title and description.
		Real-Time Clock	
		432	Table 20.1 Real-Time Clock Specifications: Changed “timer stops” to “count stopped” in the Specification column of Write to timer.

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1.01	Jul 22, 2010	**Serial Interface UARTi**	
		Chap. 21	Changed “reverse” to “inverse” or “inverted.
		461	Figure 21.2 UARTi Transmit / Receive Unit • Unified “Data bus low-order bits” and “Data bus high-order bits”. • Deleted CKDIR from the explanation about bits.
		467	21.1.6 UARTi Transmit/Receive Control Register 0 (UiC0) (i = 0 to 4): Deleted the CRS bit explanation under the register diagram.
		476	21.1.13 Pin Assignment Control Register (PACR) Added “1 0 0: 100-pin version” to the Function column of PACR0 to PACR2
		500	Figure 21.15 STSPSEL Bit Functions: Added the explanations for bits.
		506	Figure 21.17 Transmit and Receive Timing in Master Mode (Internal Clock): Added the explanations for bits.
		Multi-Master I^2C-bus Interface	
		Chap. 22	Changed “Free format select” to “Free data format select”.
		522	22.2.3 I2C0 Control Register 0 (S1D0): Changed “the P2_0/SDAMM pin and P2_1/ SCLMM pin” to “the SCLMM pin and SDAMM pin”.
		529	Figure 22.4 Interrupt Request Generation Timing in Receive Mode: Deleted “7th bit”, “8th bit” and “1st bit”.
		533	22.2.8 I2C0 Status Register 0 (S10) Deleted “the MSLAD bit in the S4D0 register is 1 (registers S0D0 to S0D2)” from the seventh bullet of the PIN bit explanation.
		539	Figure 22.5 I^2C-bus Interface Clock: Deleted “CCR4 to CCR0, FASTMODE: Bits in the S20 register” and “PCLK0: Bit in the PCLKR register”.
		540	Table 22.10 Bit Rate of Internal SCL Output and Duty Cycle: Moved “-4 to +2 fVIIC cycles” and “-2 to +2 fVIIC cycles” from notes into the table.
		541	22.3.1.3 Receiving a Slave Address in Wait Mode and Stop Mode: Modified the second paragraph.
		547	Figure 22.11 Start Condition Overlap Protect Function Enable Period: Deleted “1st bit”, “2nd bit”, and “3rd bit”, and “8th bit”.
		553	Figure 22.16 Timeout Detection Timing: • Deleted description for “Timeout detection enabled”. • Deleted “1st bit”, “2nd bit”, and “3rd bit”.
		559	Figure 22.21 I^2C Interface Interrupts: Moved the bit explanation after the bit name.
		562	22.5.2.4 S3D0 Register and 22.5.2.6 S10 Register: Added “Use the MOV instruction to write to this register.” to the first bullet.
		Serial Bus Interface	
		570	23.2.8 SS0 Status Register (SS0SR): Changed “one or more NOP instructions” to “four or more NOP instructions” in the description under the register diagram.
		592	Figure 23.13 Transmit Operation Example in 4-wire Serial Bus Mode: Corrected typo “SSiMR” to “SS0MR”.
		CAN Module	
		712	25.6.2 Transmission: Corrected typo “SENDTDATA” to “SENTDATA”.
		A/D Converter	
		Chap. 26.	Changed “precharge” to “charge”.
		715	Figure 26.1 A/D Converter Block Diagram: Changed “Initializing cycle 2 cycles” to “2 cycles”.
		718	26.2.2 A/D Register i (ADi) (i = 0 to 7): Added "Read the ADi register in 16-bit units.” to the description under the register diagram.
		719	26.2.3 A/D Control Register 2 (ADCON2): Changed “Frequency select bit” to “Frequency select bit 2” in the Bit Name column of CKS2.
		720	26.2.4 A/D Control Register 0 (ADCON0): • Changed the Function column of CH2 to CH0 in the register diagram. • Changed “ADCON2” to “ADCON0” in the description under the register diagram.
		722	26.2.5 A/D Control Register 1 (ADCON1): • Changed the reset value from “XX00 X000b”. • Changed the Function column of SCAN1 and SCAN0. • Changed the description for (b7-b6).
		725	26.3.2.2 External Trigger: • Added “$\overline{\text{ADTRG}}$” to the first bullet. • Added Figure 26.5 A/D Conversion Start Timing When External Trigger Input.
		726	26.3.5 Open-Circuit Detection Assist Function: Changed the first paragraph.
		727	Figure 26.6 A/D Open-Circuit Detection Example on AVCC (Preconversion Charge), Figure 26.7 A/D Open-Circuit Detection Example on AVSS (Preconversion discharge): Added the switch right to the Analog input ANi.

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1.01	Jul 22, 2010	728	Table 26.7, Table 26.9, Table 26.11, Table 26.13 Specifications for each mode: Modified the Specification column of Reading of A/D conversion result.
		729, 731, 733, 735	Table 26.8, Table 26.10, Table 26.12, Table 26.14 Registers and Settings: Replaced the register diagrams by the tables.
		729, 731, 733, 735	Figure 26.8, Figure 26.9, Figure 26.10, Figure 26.11 Operation Example in each mode: • Added “Single” to “A/D conversion”. • Added an arrow and “Time” at the bottom of the figure.
		738	26.7.1 Analog Input Pin: Changed the description.
		738	26.7.2 ϕAD Frequency: Deleted.
		738	26.7.3 Register Access: Changed “exclude bit 6” to “excluding the ADST bit” in line 4.
		739	26.7.9 ϕAD: Added.
		D/A Converter	
		743	27.4.1 When Not Using the D/A Converter: • Changed “the DA0E bit” to “the DA0E bit in the DACON register”. • Changed “the DAi register” to “the DA0 register”.
		CRC Calculator	
		Chap. 28	Changed “CRC operation” to “CRC calculation”.
		748	Figure 28.2 CRC Calculation When Using CRC-CCITT: Changed “reverse” to “inverse” or “invert”.
		Flash Memory	
		751	Table 29.2 Flash Memory Rewrite Modes Overview: Added “CPU operating mode” and “On-board rewrite”.
		752	29.2 Memory Map: Deleted “or memory expansion” from the last sentence.
		754	29.3.1 Flash Memory Control Register 0 (FMR0): Added the description for the FMR22 bit to the last paragraph of the FMSTP bit explanation.
		763	29.7 User Boot Mode: Added.
		763	29.7.1 User Boot Function • Changed “level” to “input level” in the first paragraph under Table 29.6. • Deleted “The content of the OFS1 address is valid.” from the second paragraph under Table 29.6.
		765	Table 29.9 Addresses of Selectable Ports for Entry: Divided the Address column into columns “13FF9h” and “13FF8h”.
		765	Table 29.10 Example Settings of User Boot Code Area: Added.
		766	Figure 29.4 Program Starting Address in User Boot Mode: Added.
		767	29.8 CPU Rewrite Mode: • Deleted “Erase-write 0 mode“ and “erase-write 1 mode” from line 9. • Added the last sentence.
		767	Table 29.11 EW0 Mode and EW1 Mode: • Changed the EW1 Mode column of State during auto write and auto erase. • Corrected typo “FRA0” to “FMR0” in the EW0 Mode column of Flash memory status detection. • Changed note 1.
		768	29.8.1 EW0 Mode: • Deleted “the flash memory is reset. The flash memory restarts after a certain period of time” from the third bullet under Figure 29.5. • Changed the last paragraph.
		769	Table 29.12 Modes after Executing Commands (in EW0 Mode): Added.
		770-772	Figure 29.6 Program Flowchart in EW0 Mode (Suspend Function Enabled), Figure 29.7 Block Erase Flowchart in EW0 Mode (Suspend Function Enabled), Figure 29.8 Lock Bit Program Flowchart in EW0 Mode (Suspend Function Enabled): • Added “I flag ← 0”. • Changed “FMR33” and “FMR32” to “FMR00”. • Moved “I flag ← 1”.
		774	29.8.2 EW1 Mode: • Deleted “the flash memory is reset. The flash memory restarts after a certain period of time” from the third bullet under Figure 29.5. • Added the description for the CSPRO bit to the last paragraph.
		775	Table 29.13 Modes after Executing Commands (in EW1 Mode): Added.

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1.01	Jul 22, 2010	776-778	Figure 29.11 Program Flowchart in EW1 Mode (Suspend Function Enabled), Figure 29.12 Block Erase Flowchart in EW1 Mode (Suspend Function Enabled), Figure 29.13 Lock Bit Program Flowchart in EW1 Mode (Suspend Function Enabled): • Added "I flag ← 0". • Moved "I flag ← 1".
		778	Figure 29.13 Lock Bit Program Flowchart in EW1 Mode (Suspend Function Enabled): • Changed "the highest-order block address" to "BA address".
		783	Table 29.16 Software Commands: Added note 1.
		785, 786	29.8.6.4 Program Command, 29.8.6.5 Block Erase Command: Deleted the description for the status register in EW0 mode.
		788	Figure 29.22 Read Lock Bit Status Command: • Changed "FMR16 = 0?" to "Read the FMR16 bit". • Changed "Block is locked" and "Block is not locked" to "Read lock bit status completed".
		789	Figure 29.23 Block Blank Check Command: • Changed "FMR07=0?" to "Read the FMR07 bit". • Changed "Blank" and "Not blank" to "Block blank check completed".
		789	29.8.6.8 Block Blank Check Command: Added the last paragraph.
		791	Table 29.19 Errors and FMR0 Register States: Changed note 1.
		795	29.9.2 Forced Erase Function: Added "the ROMCR bit in the OFS1 address is 1 (ROMCP1 bit enabled)" to the first paragraph.
		795	29.9.3 Standard Serial I/O Mode Disable Function: Added "the ROMCR bit in the OFS1 address is 1 (ROMCP1 bit enabled)" to the second paragraph.
		796, 798	Table 29.22, Table 29.24 Pin Functions (Flash Memory Standard Serial I/O Mode 1, 2): Added a sentence to the Description column of VREF.
		799	29.9.6.1 ROM Code Protect Function: Added the description for the ROMCR bit.
		800	29.10.1 Functions to Prevent Flash Memory from Being Rewritten in the previous version: Deleted.
		800	29.10.1 OFS1 Address, OFS2 Address, and ID Code Storage Address: Added.
		801	29.10.3.2 CPU Rewrite Mode Select: Added the description for the FMR60 bit.
		801	29.10.3.7 DMA transfer: Added the description for EW0 mode.
		802	29.10.3.10 Software Command: • Changed (b). • Added "or same command more than once" to (c). • Added the description for slow read mode to (e).
		802	29.10.3.12 Suspending the Auto-Erase and Auto-Program Operations: Added the details on reset to the first bullet.
		803	29.10.4.1 User Boot Mode Program: • Unified "29.10.4.1 Location of User Boot Mode Program" and "29.10.4.2 Entering User Boot Mode After Standard Serial I/O Mode" in the previous version. • Added the description of the second to seventh bullets.
		E^2PROM Emulation Data Flash	
		Chap. 30	Changed the command name from "write" to "program".
		Chap. 30	Changed "transfer" to "transmit/receive".
		Chap. 30	Changed "transfer format" to "bit order".
		Chap. 30	Changed "sleep mode" and "normal operating" to "E^2dataFlash stopped" and "E^2dataFlash operating", respectively.
		804	30.1 Overview: Changed description.
		804	Table 30.1 E^2dataFlash Specifications: • Added "(After erase, the memory value is 1.)" in the Specification column of the Unit to be erased. • Changed the ECC enabled column of the Error connection. • Added the description for ECC below the table.
		804	Figure 30.1 E^2dataFlash Block Diagram: • Added "E^2dataFlash address". • Added the description under the figure.
		805	30.2.1 E2dataFlash Address Register (E2FA): Added the description under the register diagram.
		806	30.2.2 E2dataFlash Command Register (E2FI): • Added the description under the register diagram. • Revised the table for the setting values.

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1.01	Jul 22, 2010	807	30.2.4 E2dataFlash Mode Register (E2FM): • Changed the RST bit name from “Reset bit” to “E^{2}dataFlash reset bit”. • Deleted “sleep mode” from the Function column of the RST bit. • Added the description under the register diagram. • Changed the RST bit explanation. • Deleted the description for prevention of overwriting from the EWM bit explanation. • Added the ECC bit explanation.
		808	30.2.5 E2dataFlash Control Register (E2FC): Added the RIE bit explanation.
		808	30.2.6 E2dataFlash Status Register 1 (E2FS1): Added the OMM bit explanation.
		809	30.2.7 E2dataFlash Status Register 0 (E2FS0): • Changed the description under the register diagram. • Added the explanations about bits WERR, EERR, and RDY.
		810	30.3 Block Configuration: Added the description of E^{2}dataFlash memory.
		810	Figure 30.2 E^{2}dataFlash Memory Configuration: Changed from “upper byte” to “upper 8 bits of the E2FD register”.
		811	30.4 Operational Procedures: Added the description.
		811	Figure 30.3 Read Operation Example: • Added “Set an even address when ECC is disabled”. • Added “E^{2}dataFlash” to “interrupt use” • Changed note 1.
		812	Figure 30.4 Program Operation Example: • Added “Set an even address when ECC is disabled”. • Added “E^{2}dataFlash” to “interrupt use” • Changed “WERR bit in the E2FS0 register is 0” to “Full status check”. • Changed note 1.
		813	Figure 30.5 Block Erase Operation Example: • Added “Set an even address when ECC is disabled”. • Added “E^{2}dataFlash” to “interrupt use” • Changed “EERR bit in the E2FS0 register is 1” to “Full status check”. • Added “The memory value becomes 1 after erase” to note 1. • Changed note 2.
		814	30.5 Full Status Check: Added.
		816	30.7.1 Relation with CPU Rewrite Mode: the title added.
		816	30.7.2 CPU Clock When Rewriting: Added.
		816	30.7.3 Clock Transition: Added.
		Electrical Characteristics	
		J version, Common to 3 V and 5 V	
		818	Table 31.2 Operating Conditions (1): • Changed the maximum value of $I_{OH(sum)}$ from “80”. • Changed the maximum value of $I_{OL(sum)}$ from “-80.”
		825	Table 31.9 E^{2}PROM Emulation Data Flash Electrical Characteristics: • Deleted “(“ and “)” from values. • Added “(2-byte program)” to “Word program time”. • Added “Read time (2-byte read)”. • Changed “Flash memory circuit start-up stabilization time” to “Flash memory circuit stabilization wait time (sleep mode to normal mode)”.
		826	Table 31.11 Voltage Detector 2 Electrical Characteristics: Added Vdet2_0 to Vdet2_3, and Vdet2_5 to Vdet2_7.
		J-Version, VCC = 5 V	
		829	Table 31.15 Electrical Characteristics (1): Changed the maximum value of V_T+-V_T- from “2.5”.
		830	Table 31.16 Electrical Characteristics (2): Updated values from TBD.
		835	31.2.2.5 Timer S Input: Added.
		838	31.2.2.9 Serial bus interface: • Deleted tables for Serial Bus Interface (Timing requirements) and Serial Bus Interface (Switching Characteristics), and the figure for Timing of Serial Bus Interface. • Added Table 31.31 Serial Bus Interface, Figure 31.15 I/O Timing of Serial Bus Interface (Master), Figure 31.16 I/O Timing of Serial Bus Interface (Slave), and Figure 31.17 I/O Timing of Serial Bus Interface (Synchronous Communication Mode).
		J-Version, VCC = 3 V	
		842	Table 31.32 Electrical Characteristics (1): Changed the maximum value of V_T+-V_T- from “1.8”.
		843	Table 31.33 Electrical Characteristics (2): Updated values from TBD.
		848	31.3.2.5 Timer S Input: Added.

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1.01	Jul 22, 2010	851	31.3.2.9 Serial bus interface: Added.
		K-Version, Common to 3 V and 5 V	
		855	Table 31.49 Absolute Maximum Ratings: Changed the value of Power consumption for 85°C < T_{opr} ≤ 125°C from TBD.
		856	Table 31.50 Operating Conditions (1): • Changed the maximum value of $I_{OH(sum)}$ from “80”. • Changed the maximum value of $I_{OL(sum)}$ from “-80”.
		863	Table 31.57 E^2PROM Emulation Data Flash Electrical Characteristics: • Deleted “(“ and “)” from values. • Added “(2-byte program)” to “Word program time”. • Added “Read time (2-byte read)”. • Changed “Flash memory circuit start-up stabilization time” to “Flash memory circuit stabilization wait time (sleep mode to normal mode)”.
		864	Table 31.59 Voltage Detector 2 Electrical Characteristics: Added Vdet2_0 to Vdet2_3, and Vdet2_5 to Vdet2_7.
		K-Version, VCC = 5 V	
		867	Table 31.63 Electrical Characteristics (1): Changed the maximum value of V_T+-V_T- from “2.5”.
		868	Table 31.64 Electrical Characteristics (2): Updated values from TBD.
		873	31.5.2.5 Timer S Input: Added.
		876	31.5.2.9 Serial bus interface: Added.
		K-Version, VCC = 3 V	
		880	Table 31.80 Electrical Characteristics (1): Changed the maximum value of V_T+-V_T- from “1.8”.
		881	Table 31.81 Electrical Characteristics (2): Updated values from TBD.
		886	31.6.2.5 Timer S Input: Added.
		889	31.6.2.9 Serial bus interface: Added.
		Usage Notes	
		893	32.1 OFS1 Address, OFS2 Address, and ID Code Storage Address: • Added description for the OFS2 address. • Corrected typos “.org 0FFDBH” and “.org 0FFFCh” to “.org 0FFFDBH and“.org 0FFFFCh”, respectively.
		895	32.3.1 Register Settings: Added the description for read-modify-write instructions.
		896	Table 32.2 Read-Modify-Write Instructions: Added
		898	Figure 32.2 SVCC Timing: Added the title.
		902	32.6.5 PLL Frequency Synthesizer: Changed “to meet the power supply ripple standard” to “within to the acceptable range of power supply ripple”.
		904	32.7.3 Stop Mode: Added “(stop mode)” to and deleted “(all clock stop)” from the third bullet.
		905	32.8.2 “Influence of $\overline{SD}$”: Changed the description.
		907	Figure 32.8 Procedure for Changing the Interrupt Generate Source: Changed “for the interrupt” to “in the interrupt control register” in note 2.
		908	32.9.5 Rewriting the Interrupt Control Register: Changed “no requests for” to “no interrupt requests corresponding to” in the first bullet.
		909	32.9.7 $\overline{INT}$ Interrupt: Added the third bullet.
		912	32.12 Notes on Timer A: Revised. • Added 32.12.1 Common Notes on Multiple Modes. • Added lines 5 and 6 to 32.12.1.1 Register Setting. • Added 32.12.1.2 Event or Trigger. • Changed the description of 32.12.1.3 Influence of $\overline{SD}$.
		916	32.13 Notes on Timer B: Revised. • Added 32.13.1 Common Notes on Multiple Modes. • Added 32.13.3.2 Event. • Added 32.13.4.3 Event or Trigger.
		918	32.14.2 Influence of $\overline{SD}$: Changed the section title and description.
		919	32.15.1 Register Access: Added.
		919	32.15.2 Changing the G1IR Register: Changed the title and description.
		925	32.18 Notes on Serial Interface UARTi (i = 0 to 4): Changed “(i = 0 to 2, 5 to 7)” to “(i = 0 to 4)”
		927	32.19.2.4 S3D0 Register and 32.19.2.6 S10 Register:Added “Use the MOV instruction to write to this register.” to the first bullet.
		929	32.21.1 Analog Input Pin: Changed the description.
		929	32.21.2 ϕAD Frequency: Deleted.

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1.01	Jul 22, 2010	929	32.21.3 Register Access: Changed “exclude bit 6” to “excluding the ADST bit” in line 4.
		930	32.21.9 ϕAD: Added.
		931	32.22.1 When Not Using the D/A Converter: • Changed “the DA0E bit” to “the DA0E bit in the DACON register”. • Changed “the DAi register” to “the DA0 register”.
		932	32.23.1 Functions to Prevent Flash Memory from Being Rewritten in the previous version: Deleted.
		932	32.23.1 OFS1 Address, OFS2 Address, and ID Code Storage Address: Added.
		933	32.23.3.2 CPU Rewrite Mode Select: Added the description for the FMR60 bit.
		933	32.23.3.7 DMA transfer: Added the description for EW0 mode.
		934	32.23.3.10 Software Command: • Changed (b). • Added “or same command more than once” to (c). • Added the description for slow read mode to (e).
		934	32.23.3.12 Suspending the Auto-Erase and Auto-Program Operations: Added the details on reset to the first bullet.
		935	32.23.4 User Boot: • Unified “32.23.4.1 Location of User Boot Mode Program” and “32.23.4.2 Entering User Boot Mode After Standard Serial I/O Mode” in the previous version. • Added the description of the second to seventh bullets.
		936	32.24.1 Relation with CPU Rewrite Mode: the title added.
		936	32.24.2 CPU Clock When Rewriting: Added.
		936	32.24.3 Clock Transition: Added.

Refer to 1. “Items revised or added in this version” for the items revised or added in this version.

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