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Renesas Electronics Corporation

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RENESAS

Customer Notification

QB-V850ESFJ3™

In-Circuit-Emulator

Operating Precautions

Target Device

V850ES/FJ3
μPD70F3380

Global Document No. U18402EE3V0IF00 (3rd edition)
Document No. EASE-CN-0005-1.2
Date Published February 2006

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Global Document No. U18402EE3V0IF00 (3rd edition)

(A) Product Version

1. Product Code: QB-V850ESFJ3 'B'

Cautions: 1. In conjunction with the usable EXEC version a qualified device file (Dxxxxx.800) is additionally necessary for the corresponding device, which has to be emulated. Make sure that you use the appropriated version of the device file.

2. For operation with Green Hills MULTI a dedicated version of the
- EX850G32.dll (Version E1.72e or later) and
- 850eserv.exe (Version 3.2388 or later) is required.

3. DataFlash access is not supported by the IAR EW-V850-Full-EE or IAR EW-V850-KS64 products (both V3.20) yet.
DataFlash support will be added in a later version of the IAR Embedded Workbench.

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(B) Table of Operating Precautions

No.	Outline	Control Code	QBV850ESFJ3		
				B	
1	Access of UAnRX register during break (Specification change notice)		✗	✗	
2	Access of CBnRX register during break (Specification change notice)		✗	✗	
3	Access of CnRGPT register during break (Specification change notice)		✗	✗	
4	Access of CnTGPT register during break (Specification change notice)		✗	✗	
5	Access of CnGNCTRL register during break (Specification change notice)		✗	✗	
6	DMA transfer forcible termination (Specification change notice)		✗	✗	
7	Program execution and DMA transfer in internal RAM (Specification change notice)		✗	✗	
8	Emulator hangs up on internal RESET (Direction of use)		✗	✗	
9	Emulator hangs up while downloading data or setting software break (Specification change notice)		✗	✗	
10	External RAM connection (Technical limitation)		✗	✗	
11	POC circuit and clock monitor (Technical limitation)		✗	✗	
12	Flash mask option (Technical limitation)		✗	✗	
13	Illegal break during program execution in internal RAM (1) (Specification change notice)		✗	✗	
14	Reset input during break (Technical limitation)		✗	✗	
15	Entering and releasing STOP mode when the RESET pin is masked (Specification change notice)		✗	✗	
16	Illegal break during program execution in internal RAM (2) (Specification change notice)		✗	✗	
17	Emulation of data flash		✗	✓	

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No.	Outline	Control Code	QBV850ESFJ3	B	
18	Caution on mounting target device		✗	✓	
19	AD converter operation in stop mode		✗	✗	
20	Setting of branch latency		✗	✗	
21	Memory mapping of DataFlash using the ID debugger		✗	✗	

✓ Not applicable

✗ Applicable

Note: The Control Code is indicated by the letter appearing at the 2nd position from the left in the serial number of the product.

Global Document No. U18402EE3V0IF00 (3rd edition)

(C) Description of Operating Precautions

No. 1	Access of UAnRX register during break (n = 0...3) (Specification change notice)

Details

An overrun error occurs under the following conditions (a) to (c):

(a) If a break occurs after reading the UART receive buffer register (UAnRX) and the UAnRX register is displayed in the I/O register window of the debugger, an overrun error occurs when UART reception is performed for the next time.

(b) If a software break occurs immediately after reading the UART receive buffer register (UAnRX), an overrun error occurs when UART reception is performed the next time regardless of whether or not the UAnRX register is displayed in the I/O register window.

(c) If a DMA transfer from the UART receive buffer register (UAnRX) is performed during a break**NOTE**, an overrun error occurs when UART reception is performed the next time.

Note: Including breaks by the RAM monitor function or DMM function. However the realtime RAM monitor function does not cause this behaviour since it does not set breaks.

Remark: An overrun error also occurs when the UART receives data multiple times during a break (This complies with the specification of the emulator).

Workaround

(a) Do not display the UAnRX register in the I/O register window.
(b) Set a hardware break when setting a break immediately after reading the UAnRX register
(c) There is no workaround.

No. 2	Access of CBnRX register during break (n = 0...3) (Specification change notice)

Details

When the CSIBn receive data register (CBnRX) is read, it usually starts the next reception operation. Under the following conditions (a) and (b), however, the next reception operation is not started even if CBnRX is read.

(a) If a software break occurs immediately after reading the CSIBn receive register (CBnRX).
(b) If a DMA transfer from the CSIBn receive data register (CBnRX) is performed during a break**NOTE**. As a result the communication stops or the DMA controller stops.

Note: Including breaks by the RAM monitor function or DMM function. However the realtime RAM monitor function does not cause this behaviour since it does not set breaks.

Workaround

(a) Set a hardware break when setting a break immediately after reading the CBnRX register.
(b) There is no workaround.

No. 3	Access of CnRGPT register during break (n = 0...3) (Specification change notice)

Details

Under the following conditions (a) and (b), the read pointer (RGPT) that should be incremented is not incremented and the same data as previously read is read again.

(a) If a software break occurs immediately after reading the CANn module receive history list register (CnRGPT)
(b) If a DMA transfer from the CANn module receive history list register (CnRGPT) is performed during a break**NOTE**.

Note: Including breaks by the RAM monitor function or DMM function. However the realtime RAM monitor function does not cause this behaviour since it does not set breaks.

Workaround

(a) Set a hardware break when setting a break immediately after reading the CnRGPT register.
(b) There is no workaround.

No. 4	Access of CnTGPT register during break (n = 0...3) (Specification change notice)

Details

Under the following conditions (a) and (b), the read pointer (TGPT) that should be incremented is not incremented and the same data as previously transmitted is transmitted again.

(a) If a software break occurs immediately after reading the CANn module transmit history list register (CnTGPT).
(b) If a DMA transfer from the CANn module transmit history list register (CnTGPT) is performed during a break**NOTE**.

Note: Including breaks by the RAM monitor function or DMM function. However the realtime RAM monitor function does not cause this behaviour since it does not set breaks.

Workaround

(a) Set a hardware break when setting a break immediately after reading the CnTGPT register.
(b) There is no workaround.

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No. 5	Access of CnGNCTRL register during a break (n = 0...3) (Specificatin change notice)

Details

When a register access is performed in the following sequence, an unexpected forcible shutdown may occur after the sequence is complete.

Sequence :
(1) The EFSD bit of the CANn module control register (CnGMCTRL) is set.
(2) The I/O register**NOTE** is accessed.
(3) The GOM bit of the CANn mode control register (CnGMCTRL) is cleared.

Note: I/O register access except for clearing the GOM bit of the CnGMCTRL register

The conditions under which a forcible shutdown takes place are shown below:
(a) If a break occurs immediately after the I/O register access in (2) occurs.
(b) If a break by the RAM monitor function or the DMM function occurs immediately after the I/O register access in (2) occurs.
(c) Stepwise execution is performed for the I/O register access in (2).

Workaround

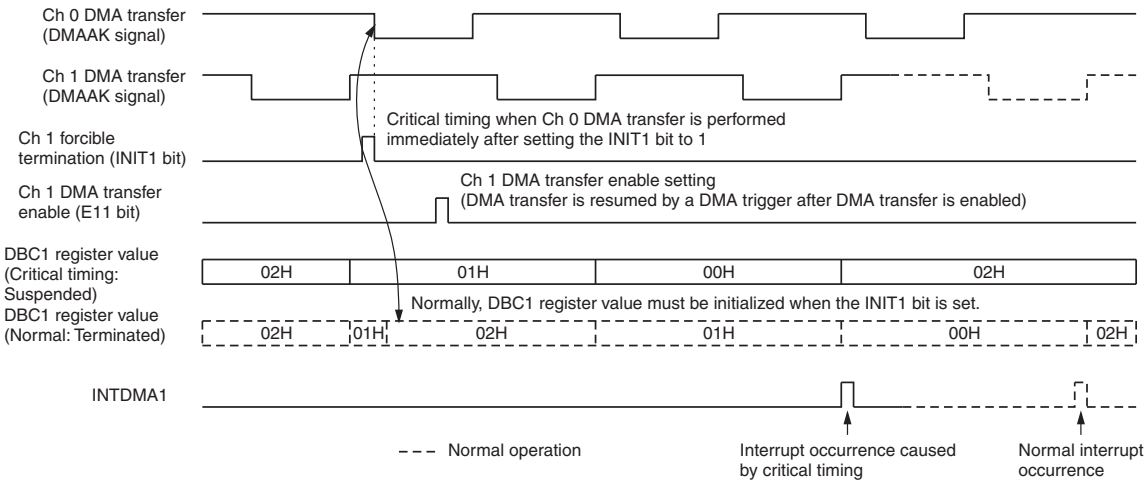
Be sure to set the EFSD bit and clear the GOM bit successively when executing a forcible shutdown. Do not perform a register access in the above sequence when not performing a forcible shutdown.

No. 6	DMA transfer forcible termination (Specification change notice)

Details

When terminating a DMA transfer by setting the corresponding INITn bit of the DCHCn register, the transfer may not be terminated, but just suspended, even though the INITn bit is set (1). As a result, when the DMA transfer of a channel that should have been terminated is resumed, the DMA transfer will terminate after an unexpected number of transfers are completed and a DMA transfer completion interrupt may occur. In addition, a DMA transfer of a channel n for which the INITn bit is set after forcible termination may be performed once again with the initialized value (n = 0 to 3).
The critical situation occurs if a DMA transfer is executed immediately after a forcible termination is set (by setting the INITn bit), refer to figure below.
The critical timing does not depend on the number of transfer channels, transfer type, transfer target, transfer mode, or trigger, and can occur with any combination of the above elements that can be set under the specifications. In addition, another channel may affect the occurrence of this critical timing.

Operation example: Both DMA channels, ch 0 and ch 1, are in single transfer mode, and ch 1 DMA transfer count is 3 (DBC1 register value = 02H).



The following registers are buffer register with a 2-stage FIFO configuration of master and slave:

- DMA source address register (DSAnH, DSAnL)
- DMA destination address register (DDAnH, DDAnL)
- DMA transfer count register (DBCn)

If these registers are overwritten during a DMA transfer, or in the DMA suspended status, the value is written to the master register, and reflected in the slave register when the DMA transfer of the overwritten channel is terminated.
The “initialization” in the figure above means that the contents of the master register are reflected in the slave register.

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No. 6	DMA transfer forcible termination (Specification change notice)

(cont.)

Workaround

The critical situation can be avoided by implementing any of the following procedures.

<1> Stop all transfers from DMA channels temporarily.

The following measure is effective if the program does not assume that the TCn bit of the DCHCn register is 1 except for the following workaround processing. (Since the TCn bit of the DCHCn register is cleared (0) when it is read, execution of the following procedure b) under <5> clears this bit.)

Procedure to avoid the critical timing:

<1> Disable interrupts (DI state)

<2> Read the DMA restart register (DRST) and transfer the ENn bit of each channel to a general purpose register (value A).

<3> Write 00H to the DMA restart register (DRST) twice**Note**.

By executing twice**Note**, the DMA transfer is definitely stopped before proceeding to <4>.

<4> Set (1) the INITn bit of the DCHCn register of the channel that should be terminated forcibly.

<5> Perform the following operations for value A read in (2) to obtain value B.

a) Clear (0) the bit of the channel that is not terminated forcibly.

b) If the TCn and ENn bits of the channel that is not terminated forcibly are 1, clear (0) the bit of the channel.

<6> Write value B in <5> to the DRST register.

<7> Enable interrupts (EI state)

Note: Execute three times if the transfer target (transfer source or transfer destination) is the internal RAM.

Remarks: 1. Be sure to execute <5> to prevent the ENn bit from being set illegally for channels that are terminated normally during the period of <2> and <3>

2. n = 0 to 3

<2> Repeat setting the INITn bit until the forcible DMA transfer termination is correctly performed (n = 0 to 3)

Procedure to avoid the critical timing:

<1> Copy the initial transfer count of the channel that should be terminated forcibly to a general-purpose register.

<2> Set (1) the INITn bit of the DCHCn register of the channel that should be terminated forcibly.

<3> Read the value of the DMA transfer count register (DBCn) of the channel that should be terminated forcibly and compare the value with the one copied in <1>. If the value do not match, repeat <2> and <3>.

Remarks: 1. When the DBCn register is read in procedure <3>, the remaining transfer count will be read if the DMA is stopped due to this bug. If the forcible DMA termination is performed correctly, the initial transfer count will be read.

2. Note that it may take some time for forcible termination to take effect if this workaround is implemented in an application in which DMA transfer other than for channels subject to forcible termination are frequently performed.

No. 7	Program execution and DMA transfer in internal RAM (Specification change notice)

Details

When a DMA transfer for the internal RAM and a bit manipulation instruction (SET1, CLR1, or NOT1) allocated in the internal RAM or a data access instruction for a misaligned address are executed simultaneously, the CPU may deadlock due to conflict between the internal bus operations. At this time, only a reset can be acknowledged, an NMI or an maskable interrupt cannot be acknowledged any more.

Unaffected cases

The critical situation does not occur if no instruction is executed in the internal RAM, or no DMA transfer is performed on the internal RAM.

Workaround

Implement any of the following workarounds.

- Do not perform a DMA transfer for the internal RAM when an instruction allocated in the internal RAM is being executed.
- Do not execute an instruction allocated in the internal RAM when a DMA transfer for the internal RAM is being performed.

No. 8	Emulator hangs up on internal reset (Technical limitation)

Details

The emulator may hang up when a reset is generated by watchdog timer 2 or the low-voltage detector (LVI).

Workaround

There is no workaround.

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No. 9	Emulator hangs up while downloading data or setting software break (Specification change notice)

Details

The emulator may hang up when an active signal is connected to the WAIT or HLDRQ pin during program download or when a software break point is set to the internal ROM.

Workaround

When WAIT and HLDRQ are not used mask these signals using the pinmask function of the debugger.
When WAIT and HLDRQ are used do not connect an active signal to the WAIT or HLDRQ input pin during download or when a software break point is set to the internal ROM.

The above behaviour can be avoided using the following software components:
- ID850: Use the version 2.81 or later of the ID850 debugger.
- Green Hills Multi: Use the V1.57 or later of the exec.dll.

No. 10	External RAM connection (Technical limitation)

Details

When external RAM on the target system is connected to the CS0 area (0x100000 - 0x1fffff) and the bus control pins are active the data in this area may be overwritten by downloading data to the internal ROM area or by setting a software breakpoint in this area.

Workaround

Initialize the data in external RAM by program run after downloading data to the CS0 area or use a hardware break for the external RAM.

The above behaviour can be avoided using the following software components:
- ID850: Use the version 2.81 or later of the ID850 debugger.
- Green Hills Multi: Use the V1.57 or later of the exec.dll.

No. 11	POC circuit and clock monitor (Technical limitation)

Details

Emulation of the POC circuit and the clock monitor is not possible.

Workaround

There is no workaround.

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No. 12	Flash mask option (Technical limitation)

Details

Overwriting the data of the option data area (0x0000007A) for the flash mask option is possible. However, independent of the value written the emulator operates as if the setting of the above address was 0x00.

Workaround

There is no workaround.

The above behaviour can be avoided using the following software components:
- ID850: Use the version 2.81 or later of the ID850 debugger.
- Green Hills Multi: Use the V1.57 or later of the exec.dll.

No. 13	Illegal break during program execution in internal RAM (1) (Specification change notice)

Details

An illegal break may occur when a peripheral I/O register is accessed during program execution in internal RAM.

Workaround

Cancel the fail-safe break setting for the internal RAM in the debugger.
- In ID850QB debugger:
Click the button “Detail” in the “Fail-safe Break” field in the “Configuration” window and clear the check box for “Internal RAM”.
- In the MULTI debugger:
Cancel the fail-save break for “ramgrd” and “ramgrdv” using the target command “flsf”

No. 14	Reset input during break (Technical limitation)

Details

The QB-V850ESFJ3 may hang up if a break occurs when the RESET pin is active (low level).

Workaround

Mask the RESET pin using the pin mask function of the debugger.

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No. 15	Entering and releasing STOP mode when the RESET pin is masked (Specification change notice)

Details

When the RESET pin is masked using the pin mask function of the debugger and watchdog timer 2 is used in reset mode, the CPU's internal operating clock is switched to the internal ring oscillator clock after STOP mode is released, depending on the timing for entering and releasing STOP mode (one of (1) to (4) of the below table). After the clock is switched to the ring oscillator clock, the CPU continues the operation with the ring oscillator clock until a reset is ececuted by the debugger.

No.	Operating clock for watchdog timer 2	Timing at which CPU operation clock switches to ring oscillator clock
1	Main clock	STOP mode is entered during the period from when a reset of watchdog timer 2 occurs until the reset is released **Note**.
2	Subclock	STOP mode is entered during the period from when a reset of watchdog timer 2 occurs until the reset is released **Note**.
3	Ring oscillator clock	STOP mode is entered during the period from when a reset of watchdog timer 2 occurs until the reset is released **Note**.
4		The internal oscillation clock is stopped during the the period from when a reset of watchdog timer 2 occurs until the rset is released **Note**, and then STOP mode is entered.

Note The period in which watchdog timer 2 generates a reset signal while the reset signal of watchdog timer 2 is masked as a result of masking RESET using the pin mask function of the debugger.

Workaround

Do not use watchdog timer 2.
To generate a reset of watchdog timer 2, do not mask the RESET pin using the pin mask function of the debugger.

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No. 16	Illegal break during program execution in internal RAM (2) (Specification change notice)

Details

A non-map break occurs if all of the following conditions are satisfied, even if the program itself is correct:
- A program is executed in the internal RAM.
- Data access for the internal RAM area is performed twice successively.
- A branch occurs to the internal ROM area using a JR or JARL instruction immediately after the above successive data access or one NOP instruction after the above successive data access.

Workaround

Implement either one of the following workarounds.

1.
- When using ID850QB:
Click the “Detail” button in the fail save break field in the configuration window and clear the check box for “Internal RAM”.
- When using MULTI:
Cancel the fail save break for “ramgrd” and “ramgrdv” using the target command “flsf”.

2.
Insert two or more NOP instructions between the successive data access for the internal RAM area and the instruction to branch to the internal ROM area.

No. 17	Emulation of Data Flash

Details

Data flash cannot be emulated.

Workaround

There is no workaround.
This restriction will be corrected by upgrading the debugger and device file.

No. 18	Caution on mounting target device

Details

Keep the voltage within the following range when mounting a target device.
VDD = EVDD = BVDD, 3.3 to 4.5 V
AVREF0 = 4.0 to 4.5 V

Workaround

There is no workaround.

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No. 19	AD converter operation in stop mode

Details

During a break the AD converter is stopped even if a break of peripheral functions is not enabled.

Workaround

There is no workaround.

No. 20	Setting of branch latency

Details

The branch latency to access the IROM memory is not set correctly.
The restriction only applies to devices with ≤256KB of ROM.

Workaround

Two different sets of device files will be available with different settings of the branch latency.

No. 21	Memory mapping of DataFlash using the ID Debugger

Details

When using the ID Debugger memory mapping of the DataFlash area cannot be done if no power is supplied from a target.

Workaround

Only work with a connected and powered target or connect VDD, EVDD, and BVDD artificially.

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(D) Cautions

Cautions on Extension Probe

- When using the extension probe, there is a restriction on the maximum operating frequency at which a high-speed signal such as a clock or external bus can be propagated. (See the table below.)
- With the QB-V850ESFJ3, the maximum operating frequency of the target device is 48 MHz, but it is 32 MHz when the clock signals are used.

Use of Clock Signal (CLKOUT, BUSCLK, SDCLK, etc.)	Use of External Bus	Upper Limit of Frequency When Using Extension Probe
Used	Used	32 MHz
	Not used	
Not used	Used	64 MHz
	Not used	80 MHz

- An impedance of approx. 50 Ohm is applied to the extension probe.
- The signal level decreases by approx. 0.1 V when it passes through the extension probe. This degrades the precision of analog signal propagation upon A/D conversion, etc.
- A delay of approx. 5 ns (propagation delay) occurs when a signal passes through the extension probe. Consequently, it may be necessary to set data waits or address waits when using the external bus.
- Be sure to connect IECUBE and the target to the GND line of the extension probe when using the extension probe; otherwise the level of the propagated signal may degraded.

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(E) Valid Specification

Item	Date pulished	Document No.	Document Title
1	September 2005	U17793EE1V0UM00	V850ES/FJ3 Preliminary User's Manual
2	April 2004	U15943EJ3V0UM00	V850ES Architecture Manual

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(F) Revision History

Item	Date pulished	Document No.	Comment
1	December 2005	EASE-CN-0005-1.0	First release
2	January 2006	EASE-CN-0005-1.1	Update of Table of valid items
3	Fabruary 2006	EASE-CN-0005-1.2	Update of (A) Cautions; Added No.19-21; Removed restriction on No.17

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