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RENESAS

User's Manual

PFESiP® EP-1 Evaluation Board

FPGA Design Guide

This document is valid in Japan.

Document No. A19351EJ1V1UM00 (1st Edition)
Date published November 2008 NS

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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PREFACE

Readers This manual is intended for users who understand the functions of the microcontroller function chip with an on-chip V850E2 CPU core (PFESiP/V850EP1) and wish to evaluate developing PFESiP EP-1 Series products using the chip.
This document is valid in Japan.

Purpose This manual is intended to help users, who wish to evaluate full-scale prototyping of PFESiP EP-1 Series products using the PFESiP/V850EP1, understand how to use the development evaluation board.
Using the PFESiP EP-1 Evaluation Board Lite is recommended for users evaluating the introduction of PFESiP EP-1 Series products.

How to Read This Manual It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, microcontrollers, SRAM, page ROM, and SDRAM.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representation:	xxxZ (Add Z after pin or signal name)
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ..... XXXX or XXXXB
	Decimal XXXX
	Hexadecimal ...XXXXH
Prefix indicating power of 2 (address space, memory capacity):	K (kilo): 2^{10} = 1,024
	M (mega): 2^{20} = $1,024^2$
	G (giga): 2^{30} = $1,024^3$
Data type:	Word ... 32 bits
	Halfword ... 16 bits
	Byte ... 8 bits

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such. Furthermore, some related documents may be intended for individual customers, because the documents are prepared in the development/planning stage of each core.

Documents related to PFESiP EP-1 Series

Document Name	Document No.
V850E2 Architecture User's Manual	U17135E
PFESiP EP-1 Series Design Manual	A19068E
PFESiP/V850EP1 Product Data User's Manual	A19069E
PFESiP/V850EP1 Hardware (CPU Function) User's Manual	A19070E
PFESiP/V850EP1 Hardware (USB Function) User's Manual	A19071E
PFESiP/V850EP1 USB Function Sample Sofware Application Note	A19349E

Documents related to PFESiP EP-1 Evaluation Board

Document Name	Document No.
PFESiP EP-1 Evaluation Board Technical Information User's Manual	A19350E
PFESiP EP-1 Evaluation Board Ordering Information User's Manual	A19352E
PFESiP EP-1 Evaluation Board FPGA Design Guide User's Manual	This manual
PFESiP EP-1 Evaluation Board Lite Technical Information User's Manual	A19354E

Documents related to development tools (User's Manual)

Document Name			Document No.
RX850 Pro (Real-time OS)	Ver.3.21	Basics	U18165E
	Ver.3.20	Installation	U17421E
	Ver.3.21	Technical	U18164E
	Ver.3.20	Task Debugger	U17422E
PM+ Ver.6.30 Project Manager			U18416E
QB-V850MINI On-chip Debug Emulator			U17638E
ID850QB Ver.3.20 Integrated Debugger	Operation		U17964E
RX850V4 Ver.4.22 Real-Time OS	Fanctionalities		U16643E
	Task Debugger		U16811E
AZ850V4 Ver.4.10 System Performance Analyzer			U17093J

Documents related to FPGA (Reference)

Document Name	Document No.
Fundamentals of FPGA Design v8 (issued by Technical Support Center, Xilinx, Inc.)	Rev1.1 '06/03

This document is a training course textbook for persons starting to design Xilinx FPGAs by using the ISE software tool. This document cannot be downloaded from the Xilinx Web site. Please note that the training course is offered free of charge and attending the course is recommended. See the following URL for details.

http://japan.xilinx.com/support/training/abstracts/fundamentals.htm

A few copies of the document are available and can be lent out if obtaining the document is difficult. Contact pfesip@ml.necel.com if a copy is needed.

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CHAPTER 1 OVERVIEW

The PFESiP EP-1 Evaluation Board is a development evaluation board for assisting the development of PFESiP EP-1 Series products.

It can be used for the software development of the PFESiP EP-1 Series-dedicated microcontroller PFESiP/V850EP1 and for user logic development and verification using the on-board FPGA.

The PFESiP/V850EP1 has an on-chip high-performance 32-bit RISC-type CPU core (V850E2 (NBA85E2S) core).

The basic functions of PFESiP EP-1 Series products based on the PFESiP/V850EP1 can be evaluated using this board.

As the on-board FPGA, the Virtex®-4 Family LX Series made by Xilinx® is employed and the XC4VLX40 is mounted as standard. The FPGA size can be changed.

This chapter describes how to use the FPGA mounted on the PFESiP EP-1 Evaluation Board.

1.1 Overview of Board

The PFESiP EP-1 Evaluation Board is a development evaluation board for assisting the development of PFESiP EP-1 Series products.

The functions of the embedded array (EA-9HD) that is provided with the user logic paired with the PFESiP/V850EP1 within the PFESiP EP-1 Series SiP can be used for developing and verifying the user logic by integrating the functions into the on-board FPGA (Virtex-4 Family LX Series[Note] made by Xilinx).

Furthermore, a more systematic evaluation can be performed by connecting the PFESiP EP-1 Evaluation Board to the user board using system expansion connectors.

On-board memory required for a general system is also provided.

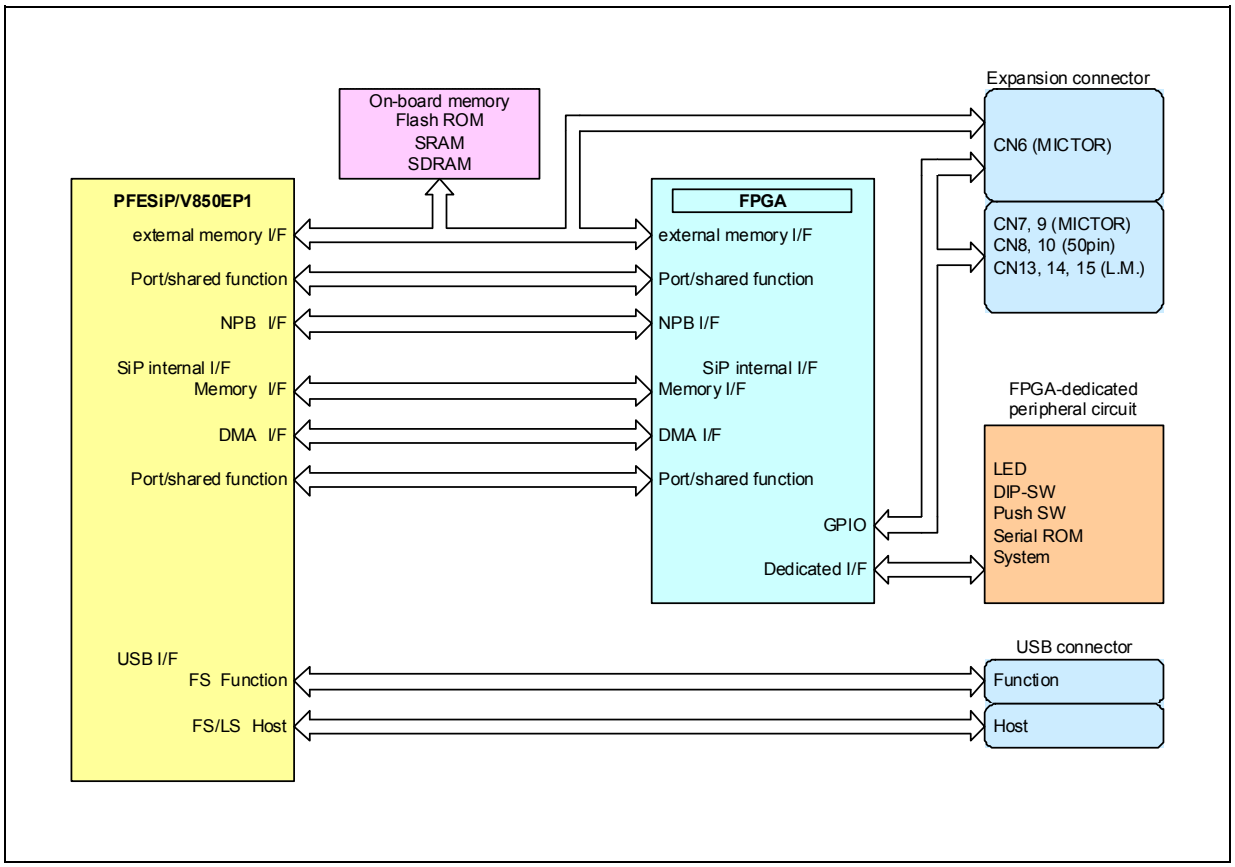
Note that the load capacitance of the PFESiP EP-1 Evaluation Board is not always equivalent, in contrast to the environment of actual SiP products, because the signals originally connected within the SiP are connected to the FPGA on-board.

Note The integration degree and the speed grade of the mounted FPGA differ for each board.
See the PFESiP EP-1 Evaluation Board Selection Guide for the types of FPGAs that can be mounted.

1.2 On-Board FPGA Use Range

With the SiP internal connection pins of the PFESiP/V850EP1, the peripheral circuits of the PFESiP/V850EP1 can be freely expanded within the FPGA, because almost all external I/Fs are connected to the FPGA. Furthermore, an external expansion board can be connected to the PFESiP/V850EP1 via the FPGA, because all expansion connectors are connected to the FPGA.

Figure 1-1. Overview of Connections Between PFESiP/V850EP1 and FPGA



Caution Not all signals are connected to each interface. This must be separately checked.

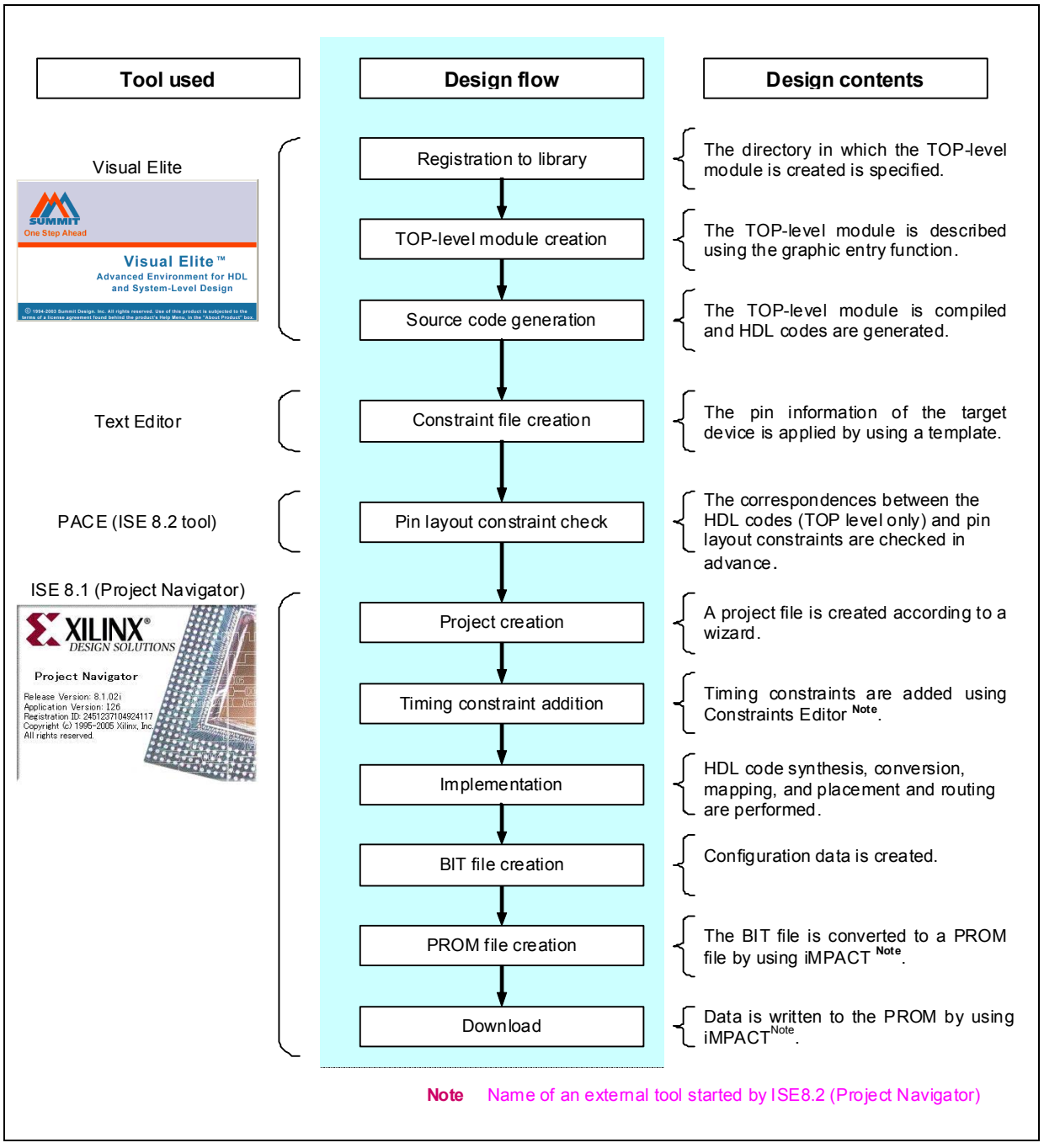
1.3 FPGA Design Procedure

This section explains the procedure of the sequence from creating HDL source codes (mainly TOP level) using the Summit Design™ graphic entry tool Visual Elite™ 2006.1 and the Xilinx FPGA development tool ISE8.2 to logic synthesis of the HDL source codes, placement and routing, and downloading to the FPGA mounted on the PFESiP EP-1 Evaluation Board.

1.3.1 Design flow

The development flow for FPGAs is shown below.

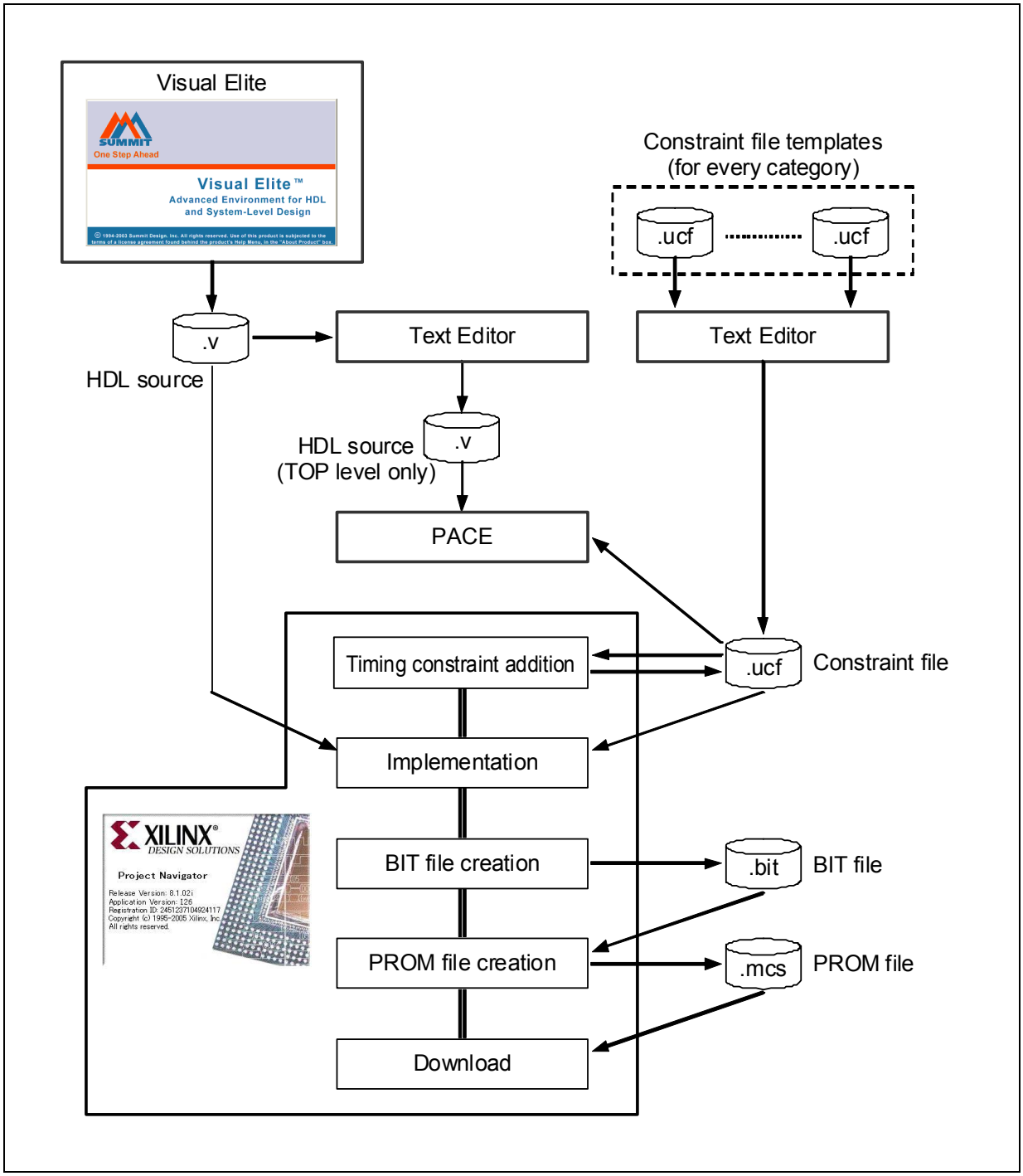
Figure 1-2. FPGA Design Flow



1.3.2 File flow

The correlation of files in the development flow for FPGAs is shown below.

Figure 1-3. File Correlation



CHAPTER 2 ISE 8.2 MANIPULATION PROCEDURE

See the Xilinx seminar document, Fundamentals of FPGA Design v8 (Rev1.1, March 2006) for the ISE 8.2 (Project Navigator) manipulation procedure. (This document is written in Japanese.)

This chapter describes cautions and supplementary information regarding each step.

2.1 ISE Option Setting (Board Restrictions)

Caution This option setting is a measure to handle the restrictions of the PFESiP EP-1 Evaluation Board. Cancel this setting for FPGA development other than for this board.

Set the environmental variables via the following procedure so that the clock input pin (N-side) of the FPGA can be used for the global clock.

<1> Select [System] from the [Control Panel].
<2> Select the [Detail Setting] tab.
<3> Click the [Environmental Variables] button.
<4> Click the [New] button of “System Environmental Variables”.
<5> Enter “XIL_PLACE_ALLOW_LOCAL_BUFG_ROUTING” in “Variable Name”.
<6> Enter “1” in “Variable Value”.
<7> Click the [OK] button and end the setting (twice).

2.2 Source File Preparation

2.2.1 HDL source preparation

This section assumes that an HDL source is separately prepared.

2.2.2 Constraint file (pin layout constraint) preparation

The pin names and pin layout of the PFESiP EP-1 Evaluation Board on-board FPGA are predetermined[Note].

This information is provided as pin layout constraints in the form of template files (text files) (divided into multiple files of different categories). A constraint file can be easily created by extracting only the required pin layout information from these template files and including the information in a single file.

Note the following points when creating a constraint file.

- Comment out the definitions of unused pins, because an error occurs if definitions of unused pins are described (left) in the UCF.
- Change the default IOSTANDARD constraints to “LVCMOS33” n together with LOC, because the constraints are “LVCMOS25”.
  # This is already reflected in the template file.
  (Example) NET "pin_name" LOC = "pin_location" | IOSTANDARD = LVCMOS33 ;
- Pins not defined (omitted to be defined) in the UCF must be checked, because they are automatically assigned.

Note Pin names can be arbitrarily changed, because changing pin names is not prohibited; however, be sure to reflect the changed pin names in the pin layout constraints.

2.2.3 Pin layout constraint check procedure

The validity of the pin definitions and pin layout constraints of the HDL source can be checked in advance via the following procedure.

<1> Create an HDL source in which only the TOP level is described.

<2> Start PACE from the [Start] button.

Click the [Start] button and select [All programs] → [Xilinx ISE8.2] → [Accessories] → [PACE].

<3> Specify the HDL source created in step <1>, the constraint file, and the target device.

Click [File] → [Open…].

[1] Constraints File: Set the constraint file.

[2] Design File: Specify the HDL source.

Click the [Select Parts] button and specify the target device.

[3]
- Family: Select “Vertex4”.
- Device: Specify the integration degree such as “XC4VLX40” or “XC4VLX80”.
- Package: Select “FF1148”.
- Speed: Specify a speed grade such as “–11”.

Click the [OK] button.

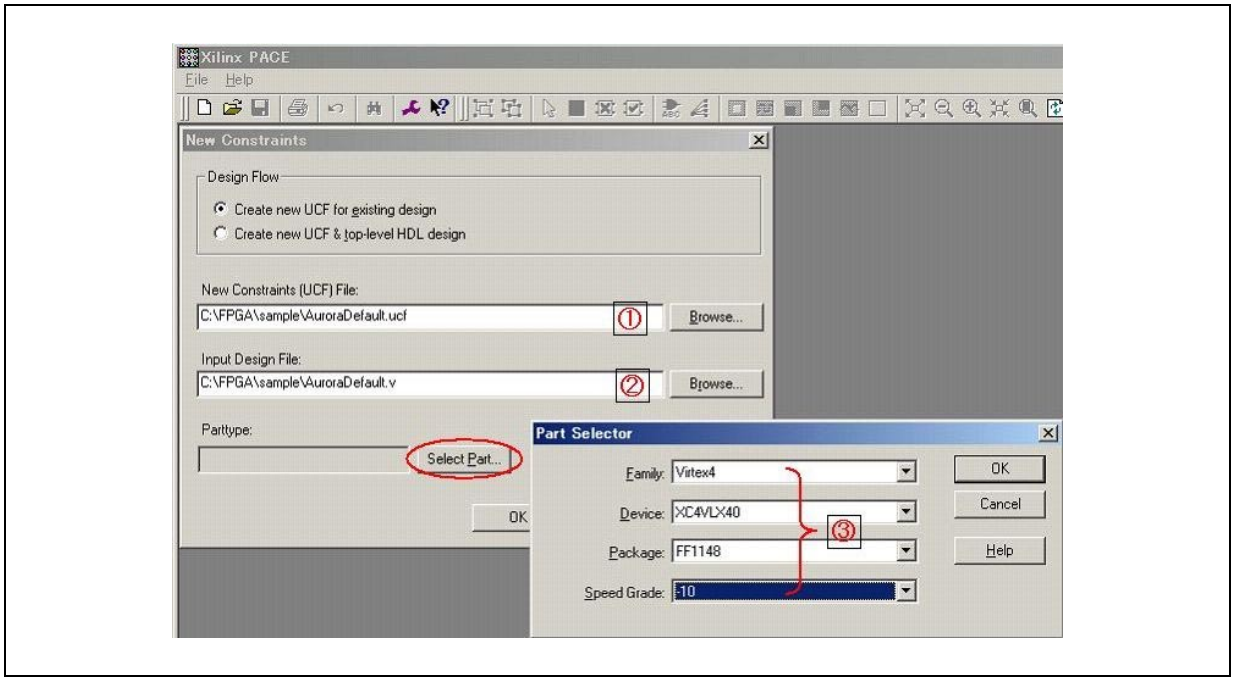
<4> Check the results in the [Design Object List ? I/O Pins] window.

Confirm that the pin constraints are added in the “Loc” column for the listed “I/O Name”.

Cautions 1. Note that an I/O pin for which the “Loc” column is blank will be automatically reallocated. Make sure that the descriptions in the HDL source and pin layout constraints match and that pin layout is reliably performed.

2. If a pin to which the pin layout constraints are added is deleted (identified as an unused pin as a result) by HDL code synthesis, an error will occur during implementation.

Figure 2-1. PACE Execution Screen



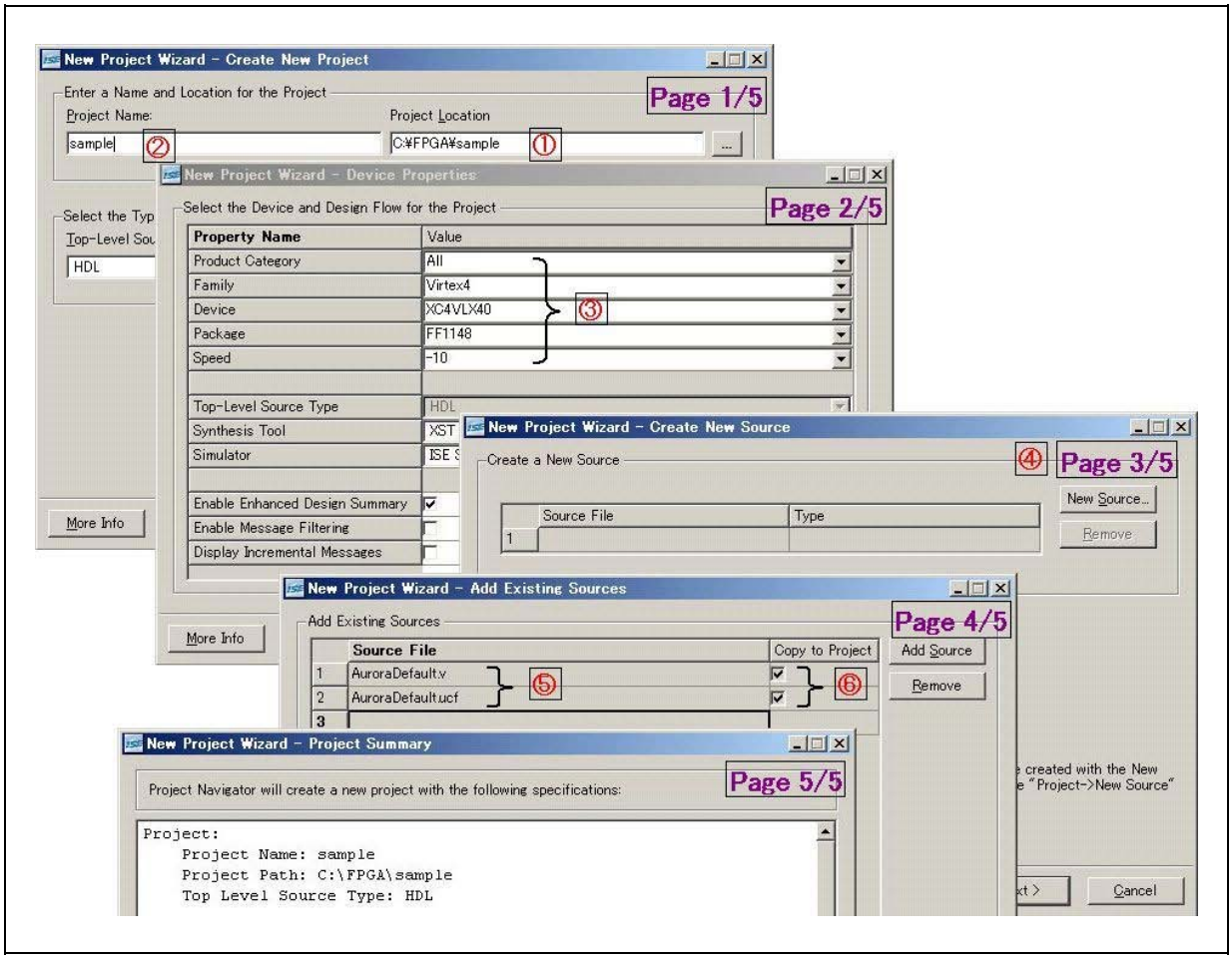
2.3 Project Creation

Remark Fundamentals of FPGA Design v8, 3a-13 to 3a-15 ○ ISE screen explanation, project creation

Create a new project by referring to the document in the remark mentioned above.
Supplementary information regarding the setting items in the New Project Wizard is described below.

<1> Specify the parent directory in which to create a project.
<2> The project name entered is also reflected to <1> at the same time and becomes the project directory name.
<3> Specify the target FPGA1 product type.
Family: Select “Virtex-4”.
Device: Specify the integration degree such as “XC4VLX40” or “XC4VLX80”.
Packagev: Select “FF1148”.
Speed: Specify a speed grade such as “–11”.
<4> Page 3/5 is not required to be set (because a source is not created in ISE).
<5> Specify the HDL source and constraint file.
<6> If these items are checked, the file specified in <5> will be copied to the project directory.
Check these items if the source file is to be managed other than in the project directory.
<7> Execute reading of the specified source after clicking the [Finish] button on page 5/5 and end the setting.

Figure 2-2. New Project Wizard Execution Screen



2.4 Timing Constraint Addition

Remark Fundamentals of FPGA Design v8, 6-11 to 6-23 ○ Explanation of timing constraints (global constraints)
6-24 to 6-31 ○ How to use the Constraints Editor

Add the timing constraints by referring to the document mentioned in the remark above.

2.5 Implementation

2.5.1 Implementation execution

Remark Fundamentals of FPGA Design v8, 3a-17 to 3a-18 ○ Implementation execution method

Perform the implementation by referring to the document mentioned in the remark above.

2.5.2 Result check

Remark Fundamentals of FPGA Design v8,

4-1 to 4-8	○ Map report
4-9 to 4-14	○ Placement and routing report
4-15 to 4-21	○ Static timing report (after mapping)
4-22 to 4-24	○ Static timing report (after placement and routing)
4-25 to 4-29	○ Pad report

Check the implementation result by referring to the document mentioned in the remark above.
Supplementary information regarding the pad report is described below.

- Check that all I/O pins have been placed according to the pin layout constraints.
  <1> Click [Pinout Report] and display the pad report.
  <2> Click the row title [Signal Name] and sort the rows by the pin names.
  <3> Check that “LOCATED” is added to the row title [Constraint] section.

2.6 BIT File Creation

A BIT file (*.bit) is created from the implementation results, according to the following procedure.
Directly downloading to the FPGA can be performed using this BIT file.

2.6.1 Unused-pin option setting

Set options according to the following procedure so that the unused pins of the FPGA are set to “Float”.

1. Select the [Generate Programming File] process in the [Processes] window.
2. Right-click to select the [Properties…] command and open the [Process Properties] dialog box.
3. Select [Configuration Options] from [Category].
   Select “Float” from the “Unused IOB Pins” drop-down list in the “Property Name” column.

Caution Pins pulled up within the PFESiP/V850EP1 exist as the PFESiP/V850EP1 external pins, so be sure to set the unused FPGA pins connected with these pins to “Float”. (The default setting in ISE 8.2 is “Pull Down”.)

2.6.2 Generate execution

1. Display [Generate Programming File] by expanding the directory tree in the [Processes] window.
2. Double-click [Programming File Generation Report].

Caution Be sure to create a PROM file according to 2.7 PROM File Creation after creating a BIT file.

2.7 PROM File Creation

Create a PROM file (*.mcs) from the BIT file according to the following procedure.
A PROM file is required for downloading to the FPGA configuration PROM.

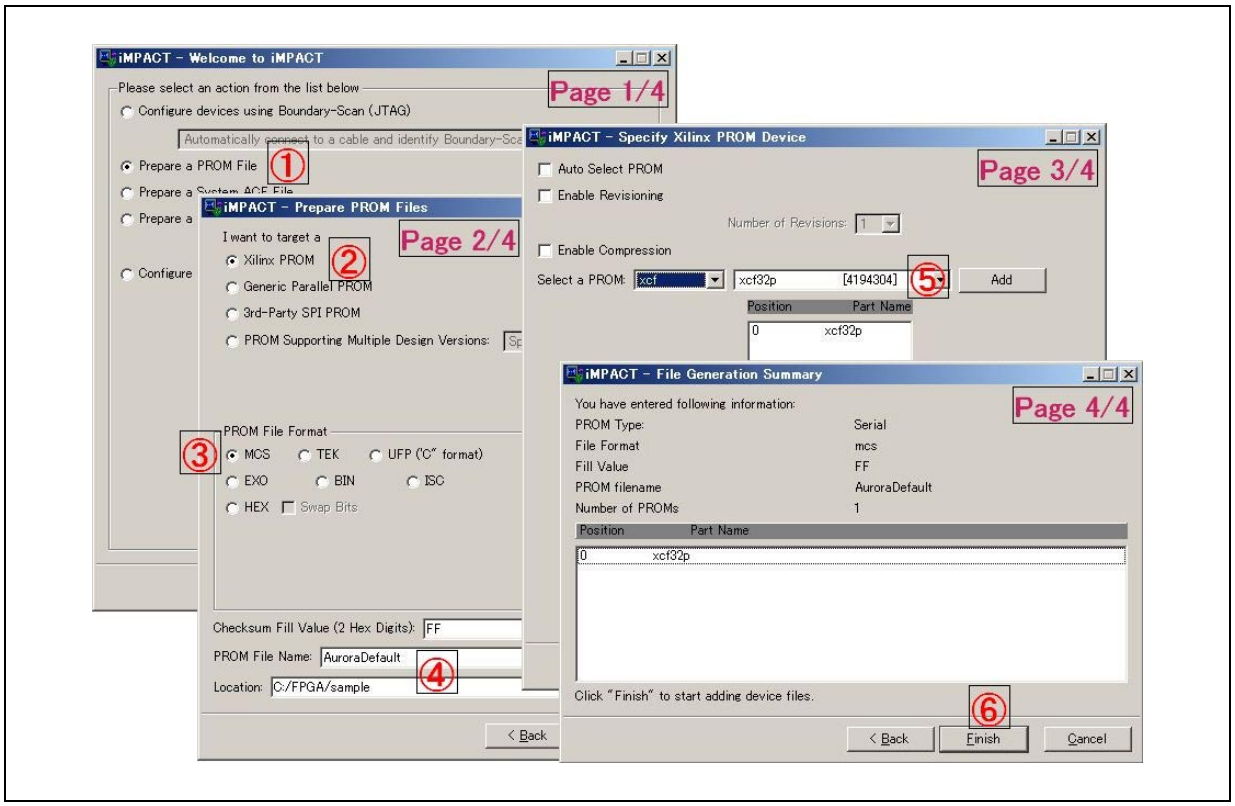
2.7.1 Wizard execution (1)

1. Display [Generate Programming File] by expanding the directory tree in the [Processes] window.
2. Double-click [Generate PROM, ACE, or JTAG File] to start iMPACT and a wizard.

Supplementary information regarding the setting items in the wizard is described below.

<1> Instruct to create a PROM file (*.mcs).
Please select an action from the list below: “Prepare a PROM File”
<2> Instruct the file format of the PROM file (*.mcs).
I want to target: “Xilinx PROM”
<3> PROM File Format: “MCS”
<4> Specify the file name and path of the PROM file to be created.
<5> Select the PROM device and click the [Add] button.
“xcf”
“xcf32p [4194304]”
<6> Set the connection status between the PROM and FPGA after clicking the [Finish] button on page 4/4.

Figure 2-3. Wizard Execution Screen of iMPACT

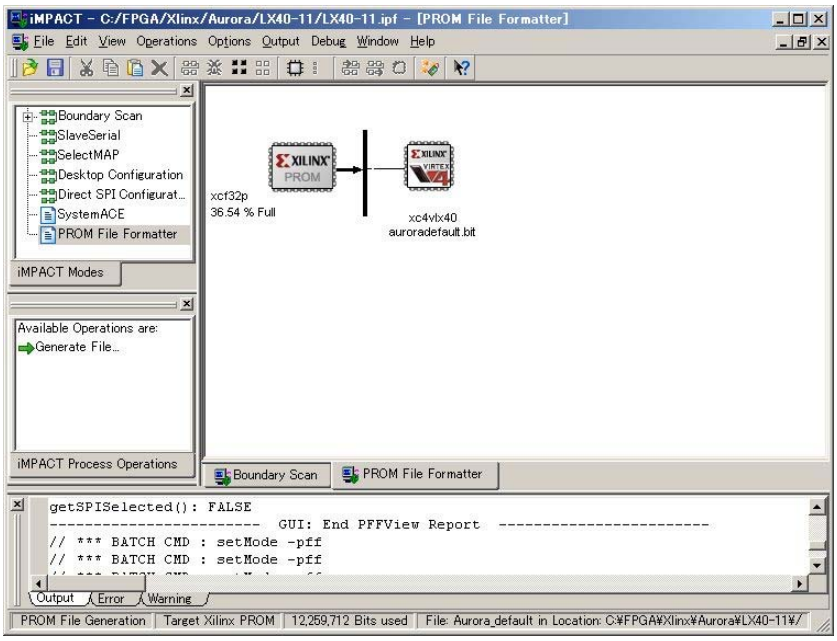


2.7.2 Wizard execution (2)

Answer the messages that are displayed and specify the connection between the PROM and FPGA.

1. Click the [OK] button in the first message box.
2. Specify the BIT file that is the conversion source file.
3. Click the [No] button in the second message box.
   The PROM and FPGA have a one-to-one correspondence on the PFESiP EP-1 Evaluation Board.
4. Click the [OK] button in the third message box and end the wizard.

Figure 2-4. Wizard End Screen of iMPACT



2.7.3 Generate execution

A PROM file is created from the BIT file.

1. Double-click [Generate File…] in the [iMPACT Process] window.

2.8 Download

Download the PROM file (*.mcs) converted from the BIT file (*.bit) to the on-board PROM, according to the following procedure.

Caution Check that converting a PROM file from the BIT file via the procedure in 2.7 PROM File Creation has been executed. (Note this, because this is often omitted.)

2.8.1 Download cable connection

Connect CN5 (see the **PFESiP EP-1 Evaluation Board Technical Information User's Manual**) of the PFESiP EP-1 Evaluation Board to a PC using a download cable (parallel cable IV or platform cable USB).

Remark When using platform cable USB as the download cable, three types of device drivers must be installed every time it is connected to a PC (tool specifications).

2.8.2 Starting iMPACT

Downloading the PROM file to the PROM is performed by starting iMPACT via ISE 8.2 (Project Navigator).

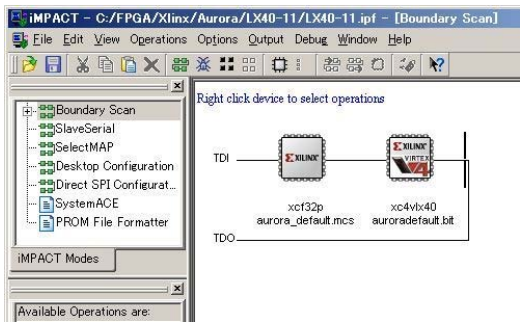
1. Display [Generate Programming File] by expanding the directory tree in the [Processes] window.
2. Double-click [Configure Device (iMPACT)] to start iMPACT.

2.8.3 Downloading to PROM

The PROM file is downloaded to the PROM according to the following procedure.

1. Double-click [Boundary Scan] in the [Flows] window.
2. Click [Initialize Chain] in the [File] menu to display the connection status of the JTAG chain.
3. Specifying the BIT file (*.bit) will be requested. Specify the BIT file. (The specification can also be canceled.)
4. Subsequently, specifying the PROM file (*.mcs) will be requested. Specify the PROM file.
5. Click the PROM device in the JTAG chain displayed by performing step 2.

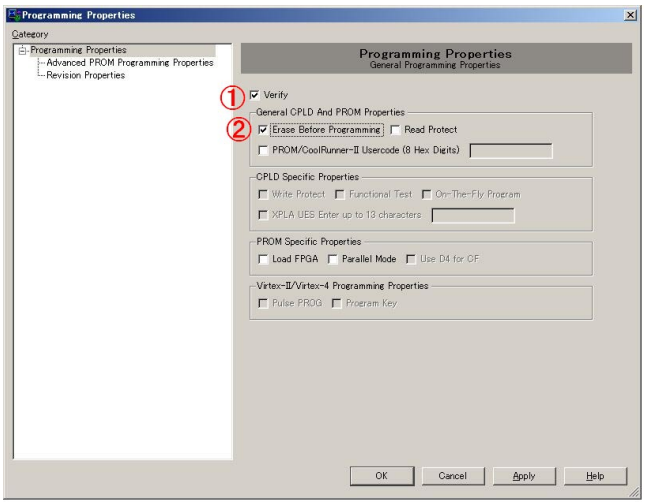
Figure 2-5. PROM Device Selection Screen



6. Click [Program…] in the [Operations] menu.
7. Specify the following and click the [OK] button in the [Programming Properties] dialog box.
   <1> Check “Verify”.
   <2> Check “Erase Before Programming”.

Remark The progress state display may not be updated while erasing the PROM.

Figure 2-6. Programming Properties Setting Screen



CHAPTER 3 FPGA UDL DESIGN GUIDE

3.1 FPGA Pin Design

3.1.1 Pins requiring processing

The FPGA has pins that must be processed (see Table 3-1).

Be sure to process these pins appropriately when implementing the UDL (user designed logic) for the FPGA.

Table 3-1. FPGA Pins Requiring Processing

Type	Pin Name	I/O	Recommended Processing When Unused	Comment
System	FRESET	out	Fix to “H”	Required for starting PFESiP/V850EP1
Serial FROM Note1	SROM_CLK	3s	Pull Up	Serial ROM pin protection
	SROM_CS	3s	Pull Up	Serial ROM pin protection
	SROM_D	3s	Pull Up	Serial ROM pin protection
SROM_Q	Pull Up Note2	in		FPGA pin protection
PAD	PAD[12:10] Note2	io Note2	Pull Up	FPGA pin protection
GPIO	GPIO[287:0]	io Note2	Pull Up	FPGA pin protection

Notes 1. When using a serial FROM, a dedicated circuit must be built-in as the UDL.

2. The io definition is used to enable the pull-up option without a dummy circuit, due to the following reasons.

- The pull-up option is disabled for an output pin.
- An input pin without a drive destination will be deleted during synthesis.

Remark The pin names conform to the definitions in the constraint file templates.
Pin names can be arbitrarily changed, but the definitions in the pin layout constraints must be changed accordingly.

3.1.2 Unused pins

When pins other than the pins requiring processing (Table 3-1) are unused, no descriptions such as definitions in HDL or pin layout constraints are required. The pin processing state in this case depends on the unused-pin option settings[Note] in ISE8.2.

Set the default statuses of unused pins of the FPGA to “Float”, because the PFESiP EP-1 Evaluation Board includes the pull-up/pull-down processing within the PFESiP/V850EP1 pins and on the board.

Table 3-2. Unused FPGA Pins

Type	Pin Name	I/O	Recommended Processing When Unused	Comment
Unused pin	All pins except pins in Table 3-1.	–	‘Float’	Depends on unused-pin option settings Note

Note See **2.6.1 Unused-pin option setting** for how to set the unused-pin options.

3.1.3 FPGA-dedicated external circuit

The following pins can be used for the FPGA-dedicated external circuit.

These pins are uniquely used with the UDL or can be arbitrarily used, such as connecting them to the external pins of the PFESiP/V850EP1 by using the UDL.

Table 3-3. FPGA-Dedicated External Circuit Pins

Type	Pin Name	I/O	Recommended Processing When Unused	Comment
LED	LED [7:0]	out	“L” or “H”	LEDs are lit with “L”
Switch	DIPSW [7:0]	in	“float”	
	SW_NMI	in	“float”	
	SW_INTP7	in	“float”	
General-purpose clock	CLK2P	in	“float”	On-board general-purpose OSC4
	CN_CLK	in	“float”	Input from CN6-115 pin
CN9 (MICTOR)	GPIO [110:0] Note	in/out	Pull Up	
CN6 (MICTOR)	GPIO [239:220] Note	in/out	Pull Up	
CN7 (MICTOR)	GPIO [219:111] Note	in/out	Pull Up	
CN10 (general-purpose 50-pin)	GPIO [162:123] Note GPIO [122:111] Note	in/out	Pull Up	
CN8 (general-purpose 50-pin)	GPIO [259:220] Note	in/out	Pull Up	
CN13 (MICTOR)	GPIO [208:128] Note	in/out	Pull Up	
CN14 (MICTOR)	GPIO [318:240] Note	in/out	Pull Up	

Note GPIO [287:0] is a pin requiring processing.
See **3.1 FPGA Pin Design** for the processing when the pin is unused.

Remark The pin names conform to the definitions in the constraint file templates.
Pin names can be arbitrarily changed, but the definitions in the pin layout constraints must be changed accordingly.

3.1.4 Connection with PFESiP/V850EP1 system pins

The following pins of the FPGA are connected to the system pins of the PFESiP/V850EP1.

These pins are used with the UDL or can be arbitrarily used, such as for outputting to the external expansion connectors by using the UDL.

Table 3-4. PFESiP/V850EP1 System Pin Connections

Type	Pin Name	I/O	Recommended Processing When Unused	Comment
PFESiP/V850EP1 system pin	VBRESTOZ	in	“Float”	
	VBCLKOUT	in	“Float”	

Remark The pin names conform to the definitions in the constraint file templates.
Pin names can be arbitrarily changed, but the definitions in the pin layout constraints must be changed accordingly.

3.1.5 Connection with PFESiP/V850EP1 port (shared-function) pins

The following pins of the FPGA are connected to the port (shared-function) pins of the PFESiP/V850EP1.

These pins are used with the UDL or can be arbitrarily used, such as for outputting to the external expansion connectors by using the UDL.

Table 3-5. PFESiP/V850EP1 Port (Shared) Pin Connections

Port (I/O)		Shared Function (I/O)		FPGA	Recommended Processing When Unused	comment
P0 [7:0]	io	INTPZ [7:0]	out	√	“Float”	
P1 [0]	io	INTPZ [8]	out	√	“Float”	JP2 must be 1-2.
P1 [7:1]		INTPZ [15:9]		√	“Float”	
P7 [0]	io	SELFREFZ	–	(JP20)	“Float”	Depends on JP20 setting
Other than above		(Omitted)		√	“Float”	

Remark The pin names conform to the definitions in the constraint file templates.
Pin names can be arbitrarily changed, but the definitions in the pin layout constraints must be changed accordingly.

3.1.6 Connection with PFESiP/V850EP1 SiP internal memory interface pins

The following pins of the FPGA are connected to the SiP internal memory interface pins of the PFESiP/V850EP1.

These pins are used with the UDL or can be arbitrarily used, such as for outputting to the external expansion connectors by using the UDL. Furthermore, since STBUSCLK is connected to CN7, these pins can be arbitrarily used, such as for inputting to one of the FPGAs when these boards are stacked.

Table 3-6. PFESiP/V850EP1 SiP Internal Memory Interface Pin Connections

Pin Name	I/O	FPGA	CN7	Recommended Processing When Unused	Comment
SCSZ [3:0]	in	√	×	“Float”	
SA [20:0]	in	√	×	“Float”	
D [15:0]	Io	√	×	“Float”	
SRDZ	in	√	×	“Float”	
SWRZ [1:0]/SBENZ [1:0]	in	√	×	“Float”	
SIOWRZ	in	√	×	“Float”	
SIORDZ	in	√	×	“Float”	
SWRSTBZ	in	√	×	“Float”	
SWAITZ	out	(JP40)	×	“Float”	Depends on JP40 setting
SHLDRQZ	out	√	×	“Float”	
SHLDAKZ	in	√	×	“Float”	
SBCYSTZ	in	√	×	“Float”	
STBUSCLK	in	√	√	“Float”	
SREFRQZ	in	√	×	“Float”	
SRESTOZ	in	√	×	“Float”	

Remark The pin names conform to the definitions in the constraint file templates.
Pin names can be arbitrarily changed, but the definitions in the pin layout constraints must be changed accordingly.

3.1.7 Connection with PFESiP/V850EP1 external memory interface pins

The following pins of the FPGA are connected to external memory interface pins of the PFESiP/V850EP1, on-board memory, and external expansion connector CN6. These pins are used with the UDL or can be arbitrarily used, such as for inputting or outputting to the external expansion connectors (except CN6) by using the UDL.

Table 3-7. PFESiP/V850EP1 External Memory Interface Pin Connections

Pin Name	I/O	FPGA	CN6	Memory	Recommended Processing When Unused	comment
CSZ [0]	in	√	√	√	“Float”	
CSZ [7:1]	in	√	√	√	“Float”	P7 [7:1]
A [1:0]	Io	√	√	√	“Float”	P6 [7:6]
A [19:2]	in	√	√	√	“Float”	
A [25:20]	in	√	√	√	“Float”	P6 [5:0]
D [15:0]	in	√	√	√	“Float”	
D [31:16]	in	√	√	√	“Float”	P9 [7:0], P10 [7:0]
RDZ	in	√	√	√	“Float”	
WRZ [3:0] / BENZ [3:0]	out	√	√	√	“Float”	
IOWRZ	out	√	√	√	“Float”	P8 [0]
IORDZ	in	√	√	√	“Float”	P8 [1]
DQM [3:0]	in	√	√	√	“Float”	
SDWEZ	in	√	√	√	“Float”	
SDCASZ	in	√	√	√	“Float”	
SDRASZ	in	√	√	√	“Float”	
SDCKE	in	√	√	√	“Float”	
WRSTBZ	in	√	√	√	“Float”	
WAITZ	out	(JP20)	(JP20)	×	“Float”	Depends on settings of P7 [0] and JP20
HLDRQZ	out	(JP20)	(JP20)	×	“Float”	Depends on settings of P8 [3] and JP20
HLDAKZ	in	√	√	×	“Float”	P8 [2]
BCYSTZ	in	√	√	×	“Float”	
BUSCLK	in	√	√	√	“Float”	
REFRQZ	in	√	√	×	“Float”	P8 [4]
SELFREFZ	out	(JP20)	(JP20)	×	“Float”	Depends on settings of P8 [5] and JP20

Remark The pin names conform to the definitions in the constraint file templates.
Pin names can be arbitrarily changed, but the definitions in the pin layout constraints must be changed accordingly.

[MEMO]

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