

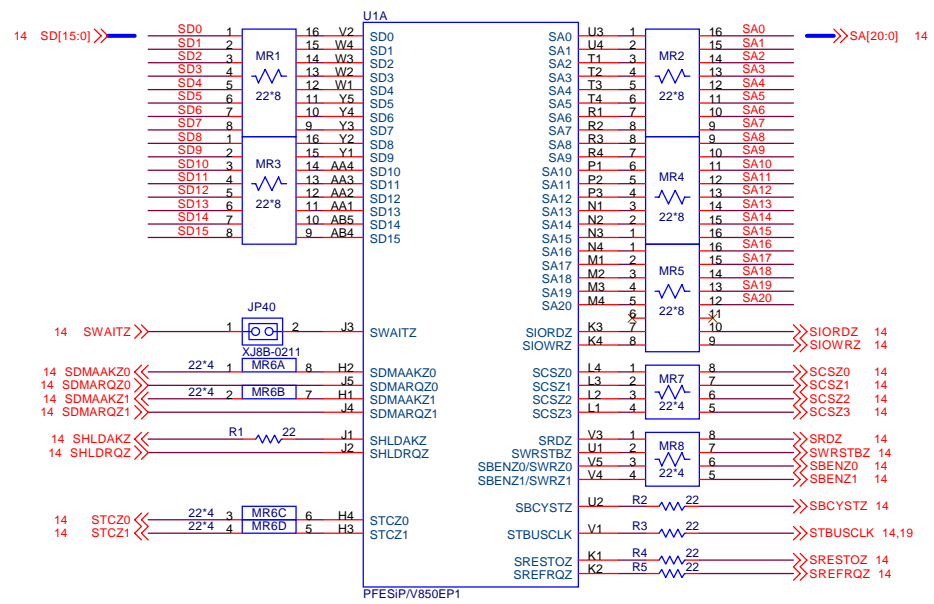
PFESiP EP-1 Evaluation Board

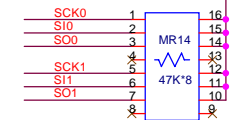
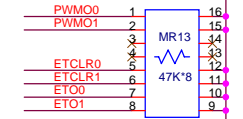
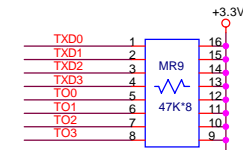
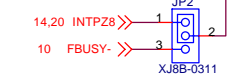
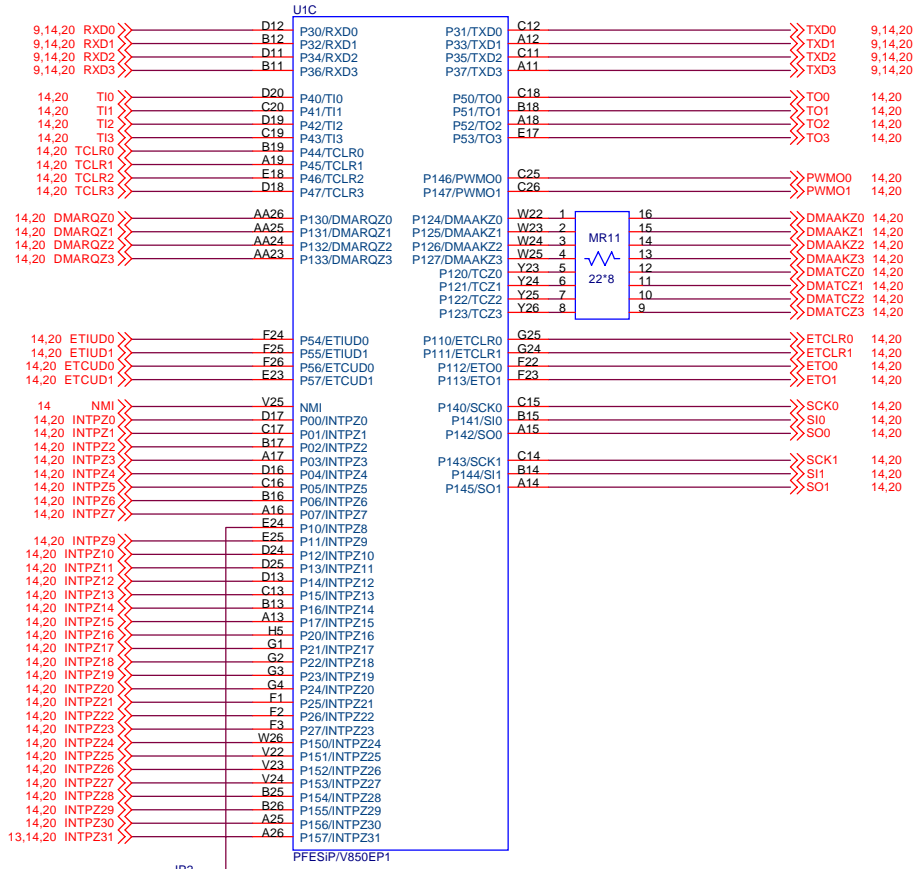
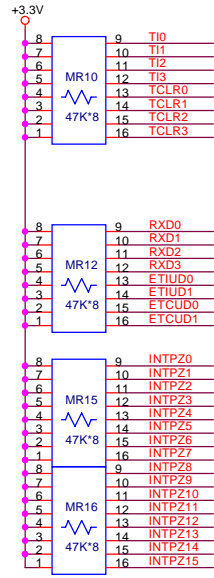
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Date	Revision	Page	Description of Changes
2006.12.21	0.0		初版
2006.12.26	0.0	8	(U3)LCX126 -> LCX125変更。これに伴い、VBUSDETラインを回路変更。
2007.03.28	0.1	21	R107(470)を 2.2K に変更

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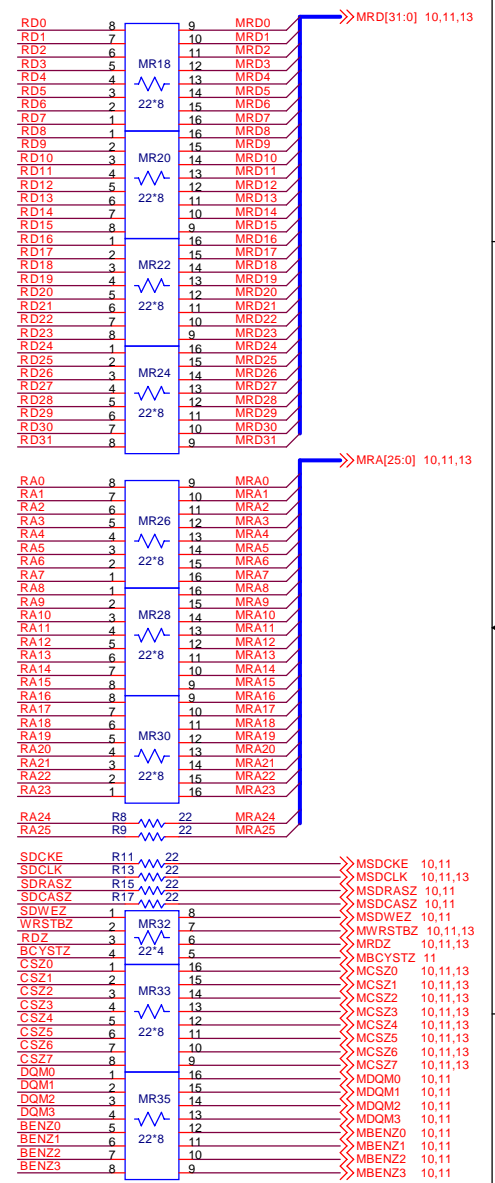
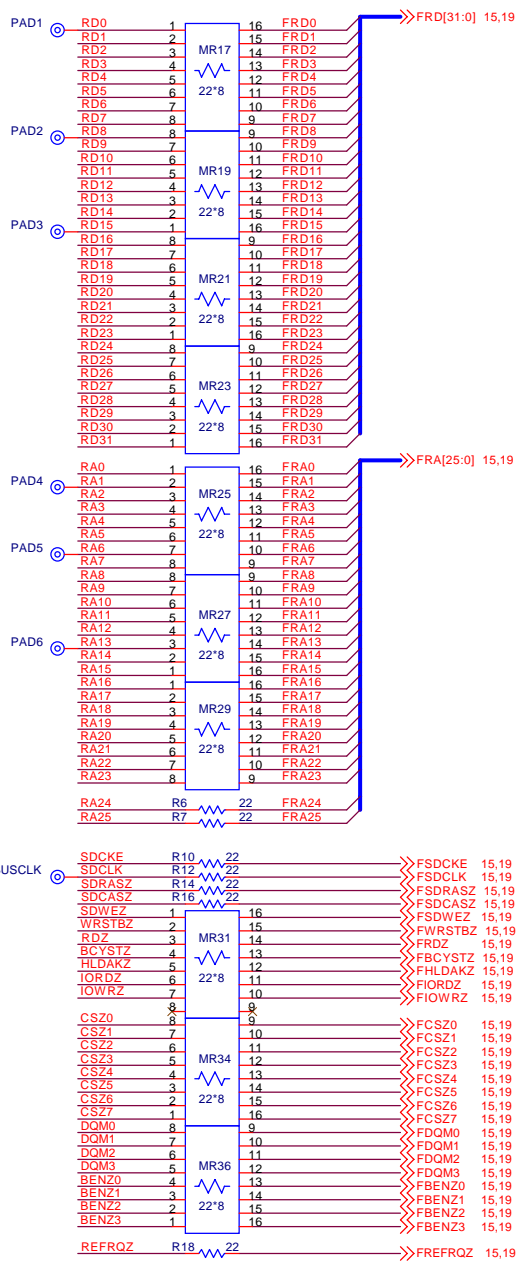




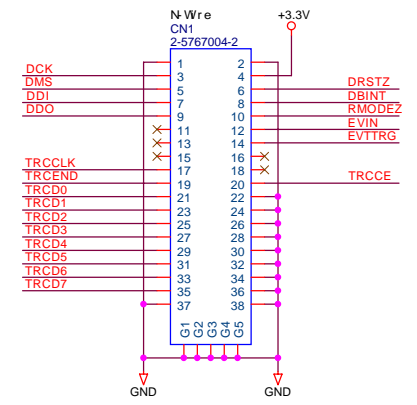
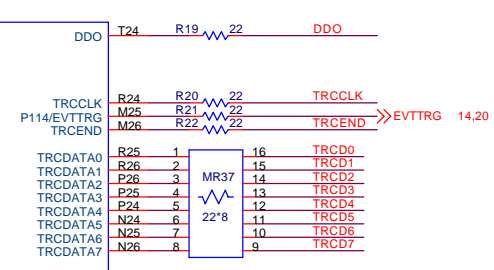
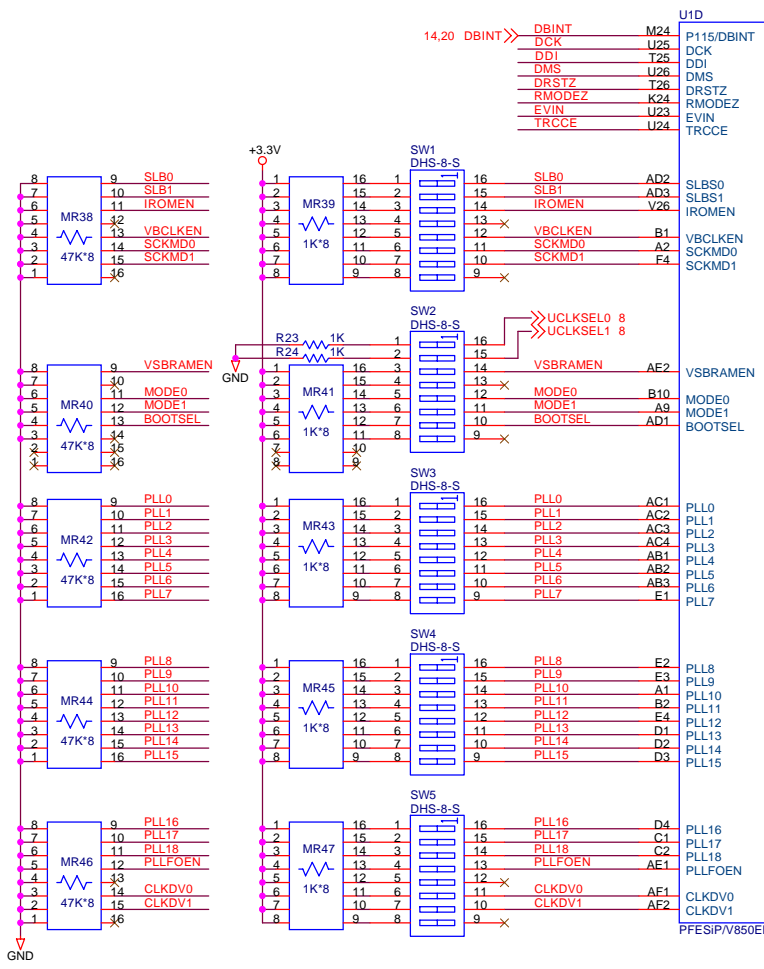
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RD3	AE24	D3	AE9	RA4	
RD4	AE25	D4	AE7	RA5	
RD5	AE26	D5	AE7	RA6	
RD6	AE25	D6	AE7	RA7	
RD7	AE26	D7	AE7	RA8	
RD8	AE26	D8	AE8	RA9	
RD9	AD25	D9	AE8	RA10	
RD10	AC24	D10	AD8	RA11	
RD11	AC25	D11	AC8	RA12	
RD12	AB23	D12	AC9	RA13	
RD13	AB24	D13	AD9	RA14	
RD14	AB25	D14	AE9	RA15	
RD15	AB26	D15	AE9	RA16	
RD16	AD15	P90/D16	AD10	RA17	
RD17	AC15	P92/D18	AD10	RA18	
RD18	AE15	P93/D19	AD10	RA19	
RD19	AE15	P94/D20	AD5	RA20	
RD20	AC16	P95/D21	AE5	RA21	
RD21	AD16	P96/D22	AE4	RA22	
RD22	AE16	P97/D23	AE3	RA23	
RD23	AE16	P100/D24	AE3	RA24	
RD24	AE17	P101/D25	AE3	RA25	
RD25	AD17	P102/D26			
RD26	AC17	P103/D27			
RD27	AE17	P104/D28	AD13	SDCKE	
RD28	AC18	P105/D29	AE13	SDCLK	
RD29	AD18	P106/D30	AC11	SDRASZ	
RD30	AE18	P107/D31	AD11	SDCASZ	
RD31	AE18		AE19	CSZ0	
			AE19	CSZ1	
			AC20	CSZ2	
			AD20	CSZ3	
			AE20	CSZ4	
			AC21	CSZ5	
			AD21	CSZ6	
			AE11	SDWEZ	
			AE13	BCYSTZ	
			AD12	DQM0	
			AE12	DQM1	
			AE12	DQM2	
			AE11	DQM3	
			AC22	HLDAKZ	
			AB22	IORDZ	
			AE21	IOWRZ	
			AD19	RDZ	
			AC19	WRSTBZ	
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			AD14	BENZ1	
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			AF14	BENZ3	

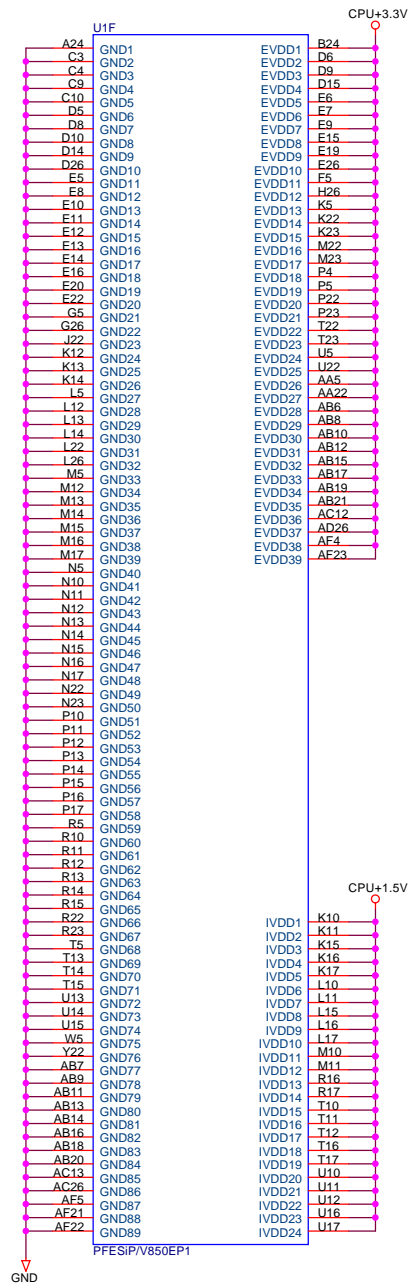
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 11,15 WAITZ >> AC10
 15 SELFREFZ >> AD23

PFESIP/V850EP1

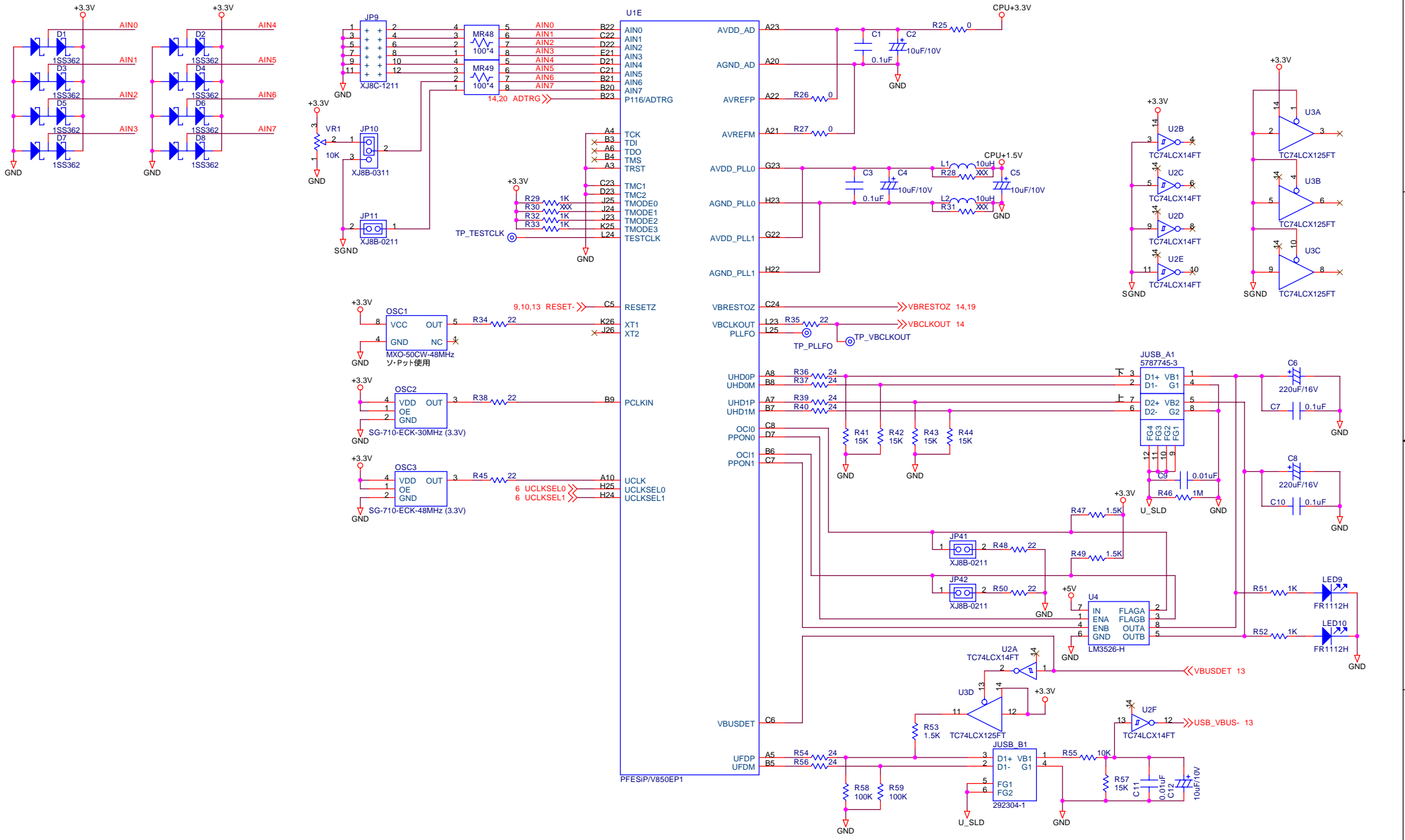


CPU(MEMC)		Midas lab	
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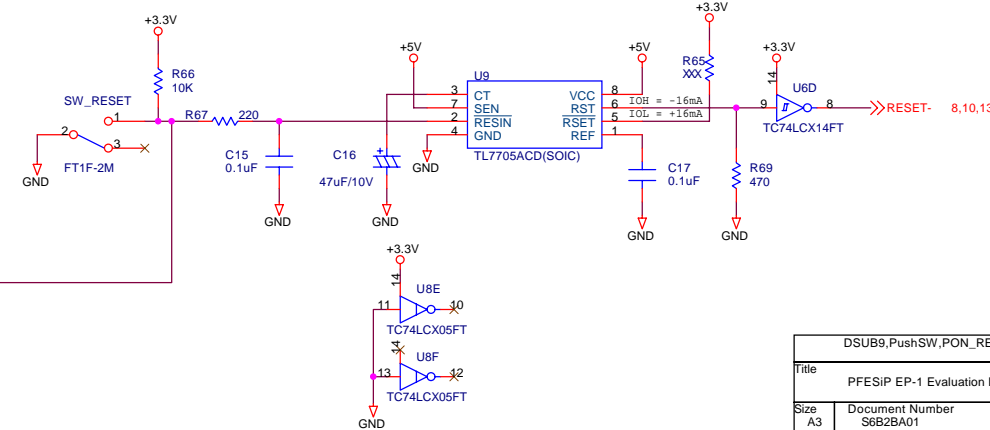
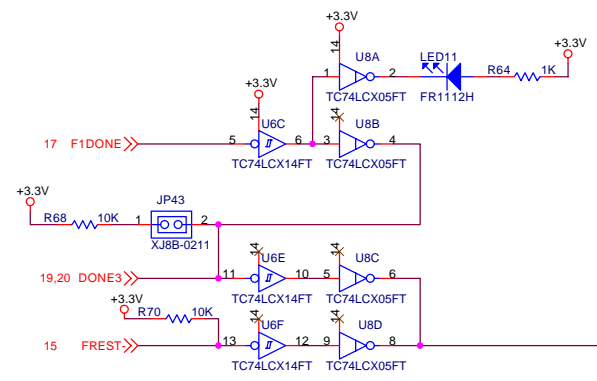
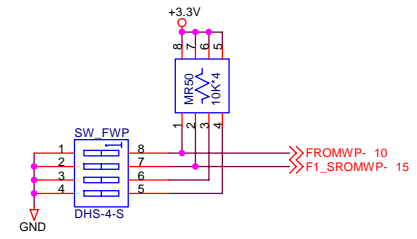
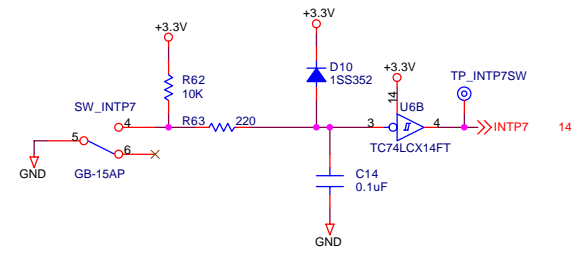
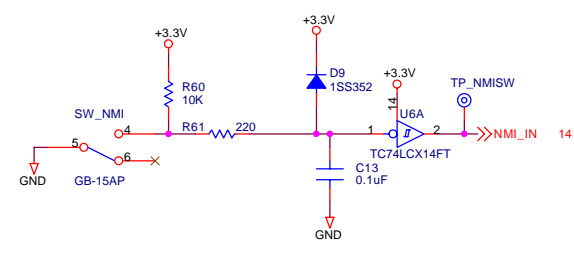
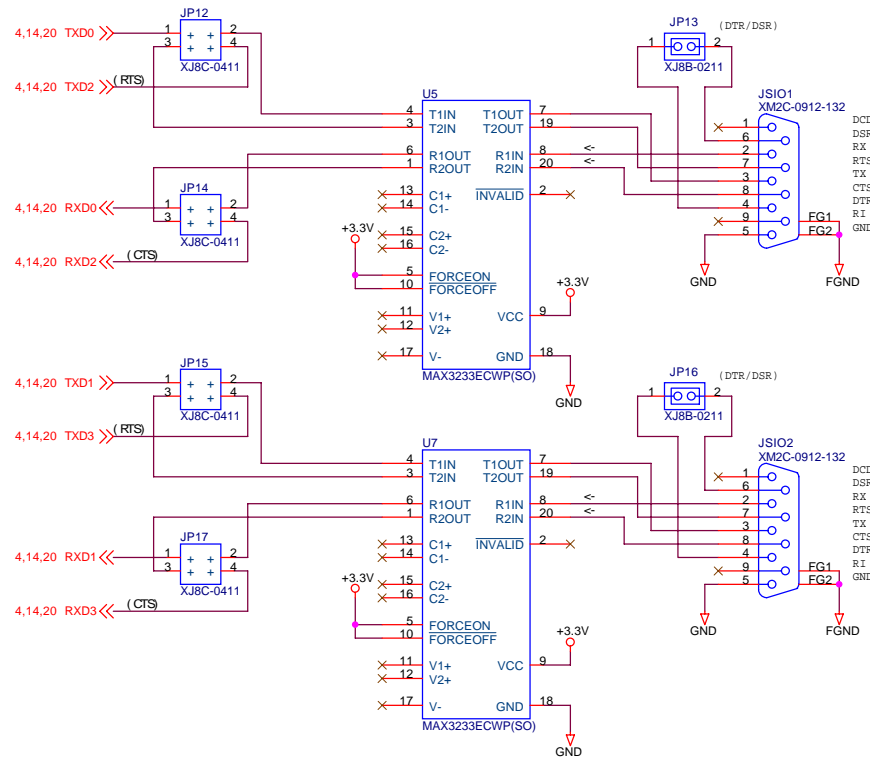




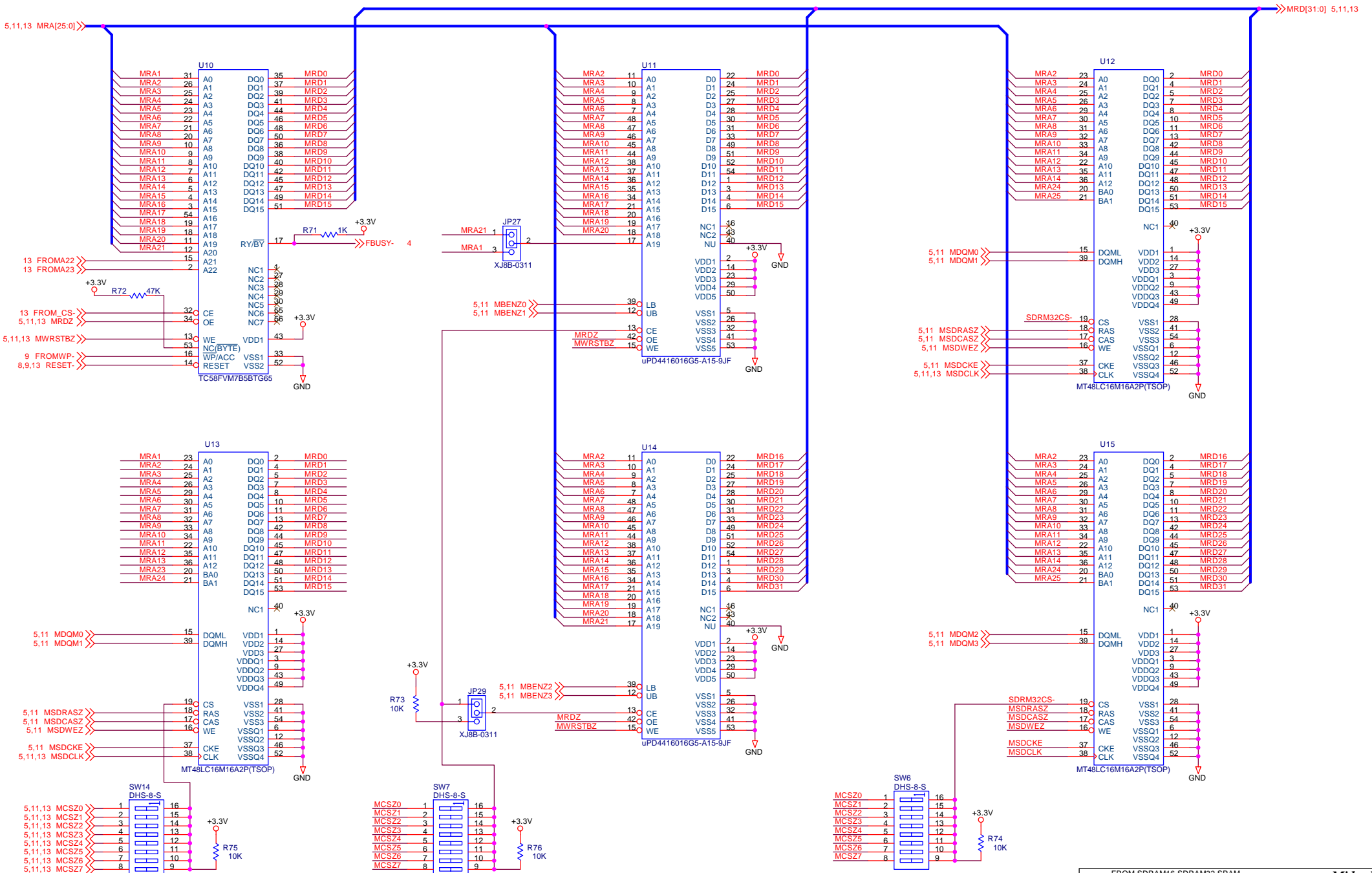
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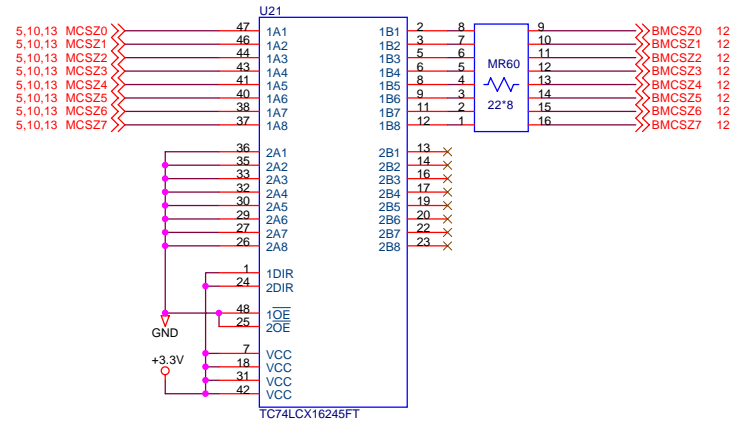
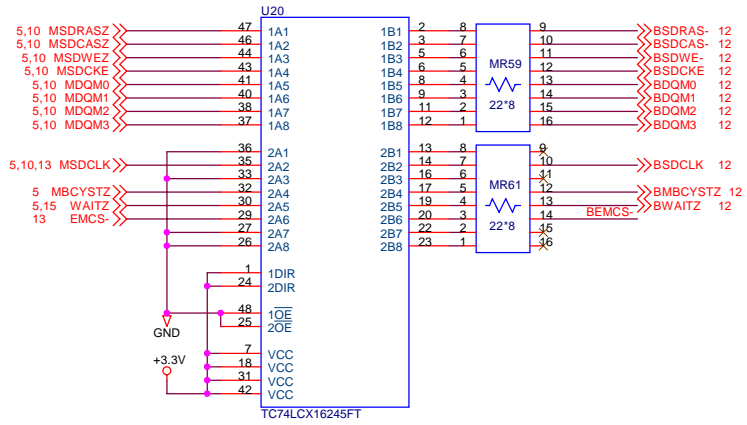
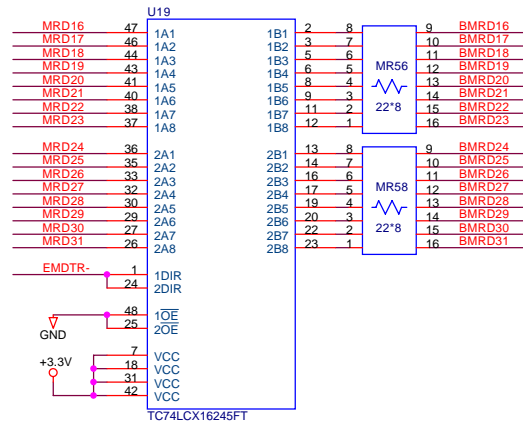
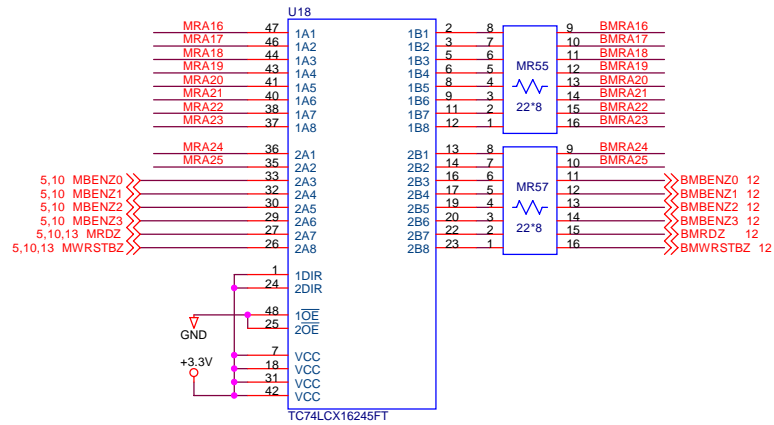
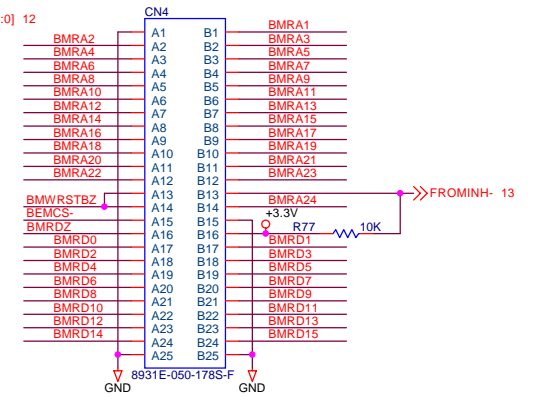
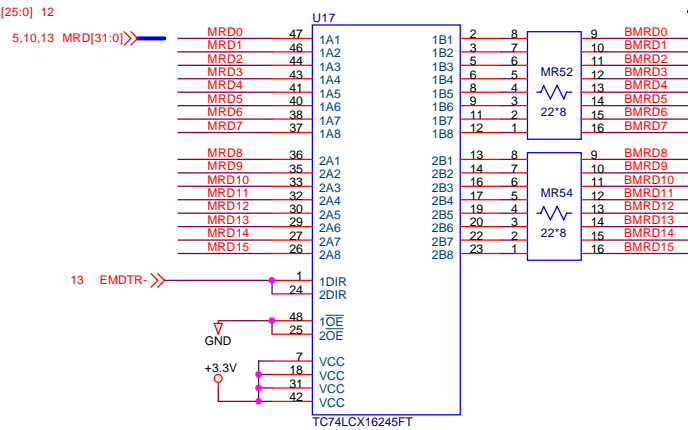
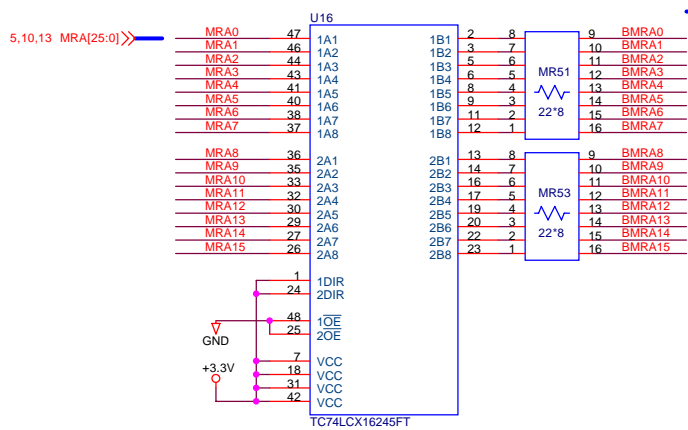
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Title PFESIP EP-1 Evaluation Board		
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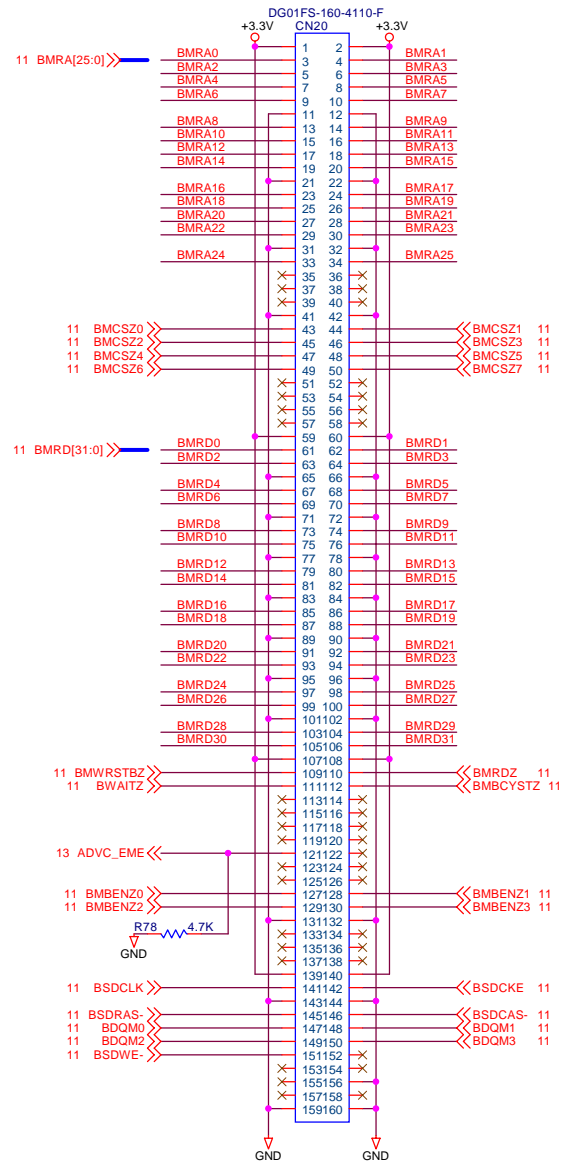


DSUB9,PushSW,PON_RES		Midas lab	
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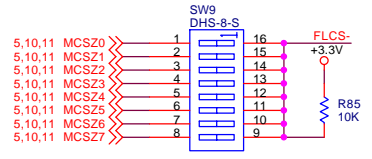
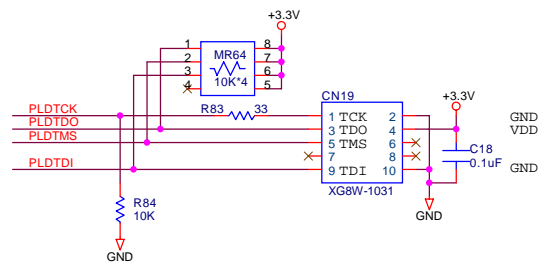
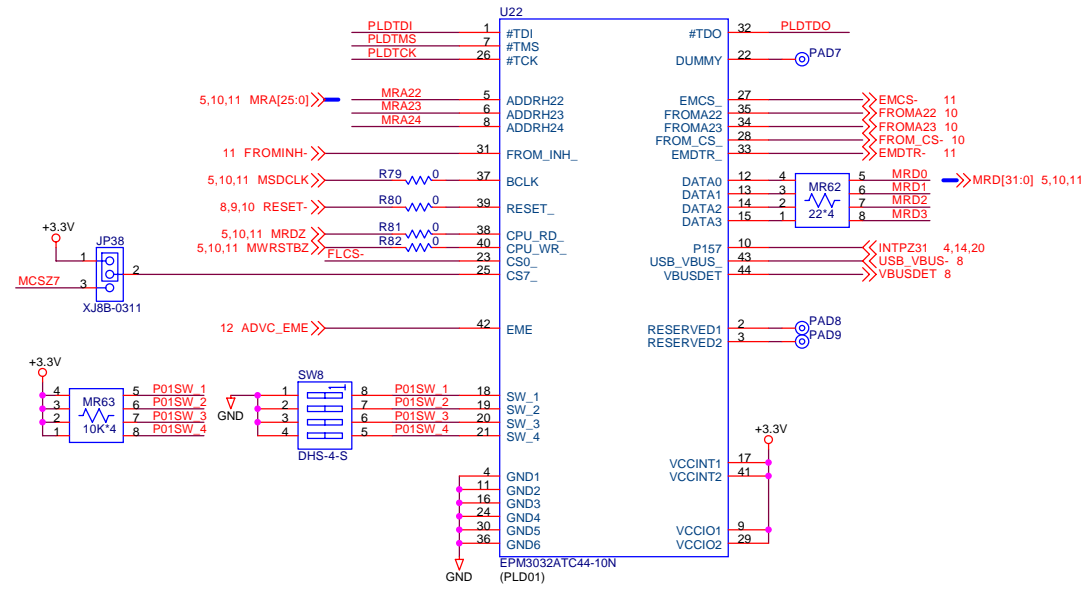


FROM.SDRAM16,SDRAM32,SRAM		Midas lab
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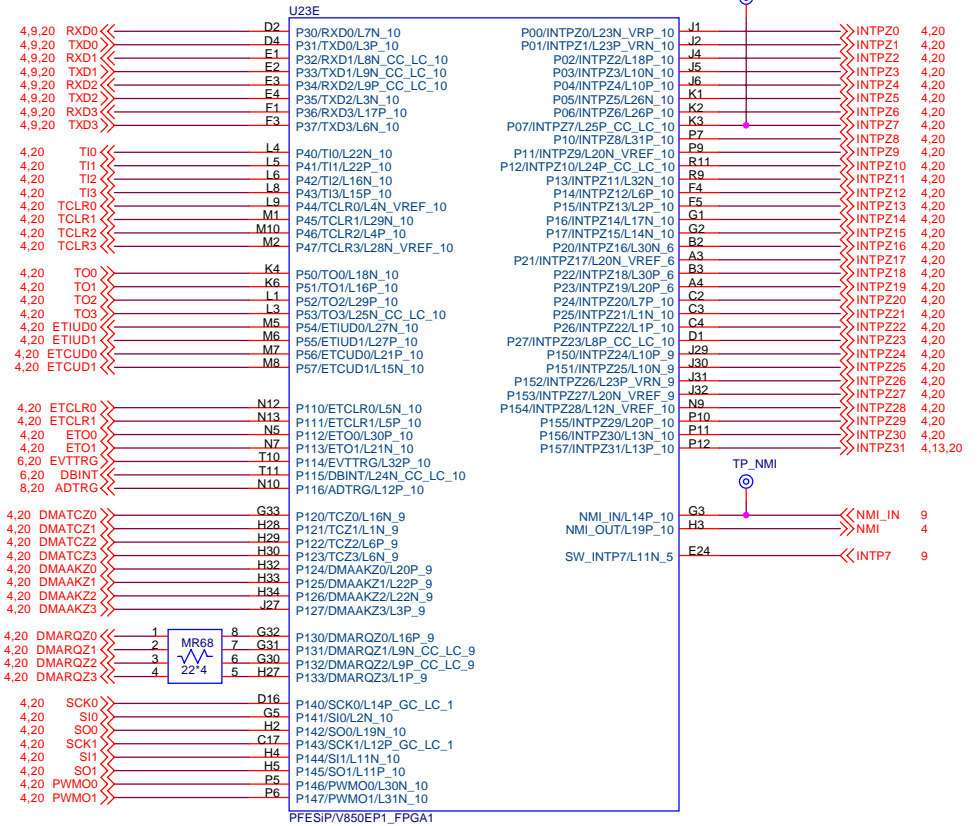
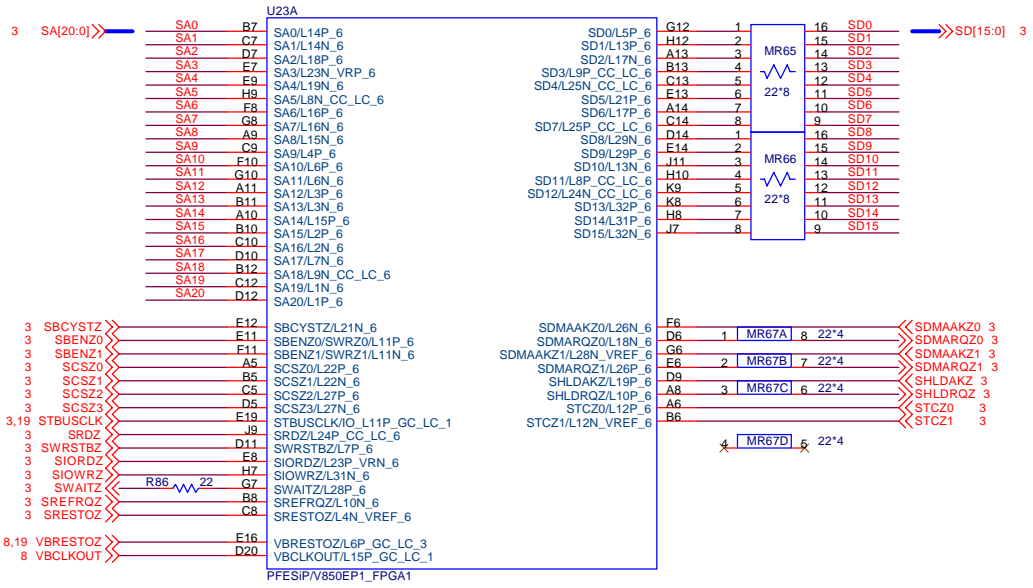


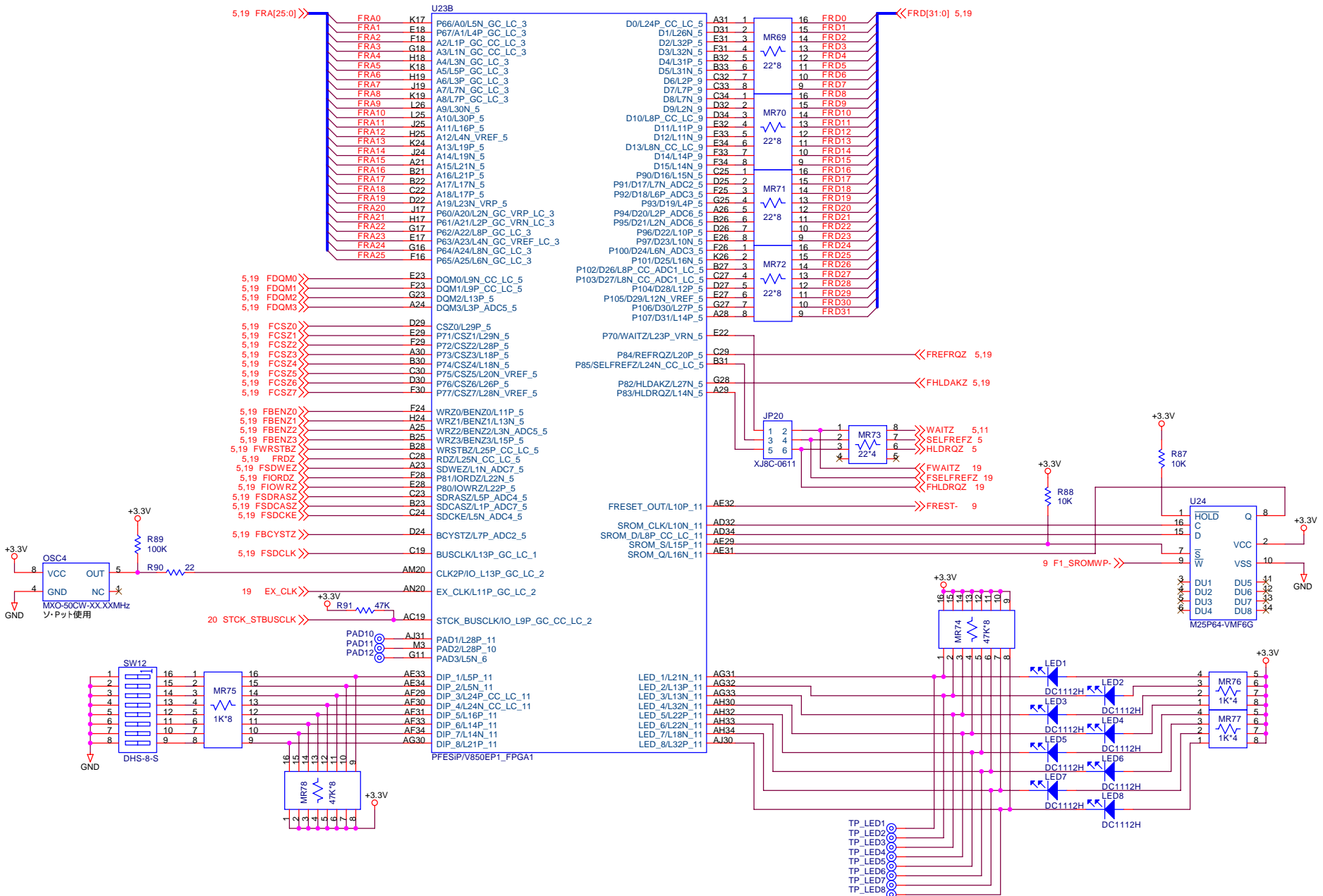


EMEM+BusTRC I/F(YDC)		Midas lab
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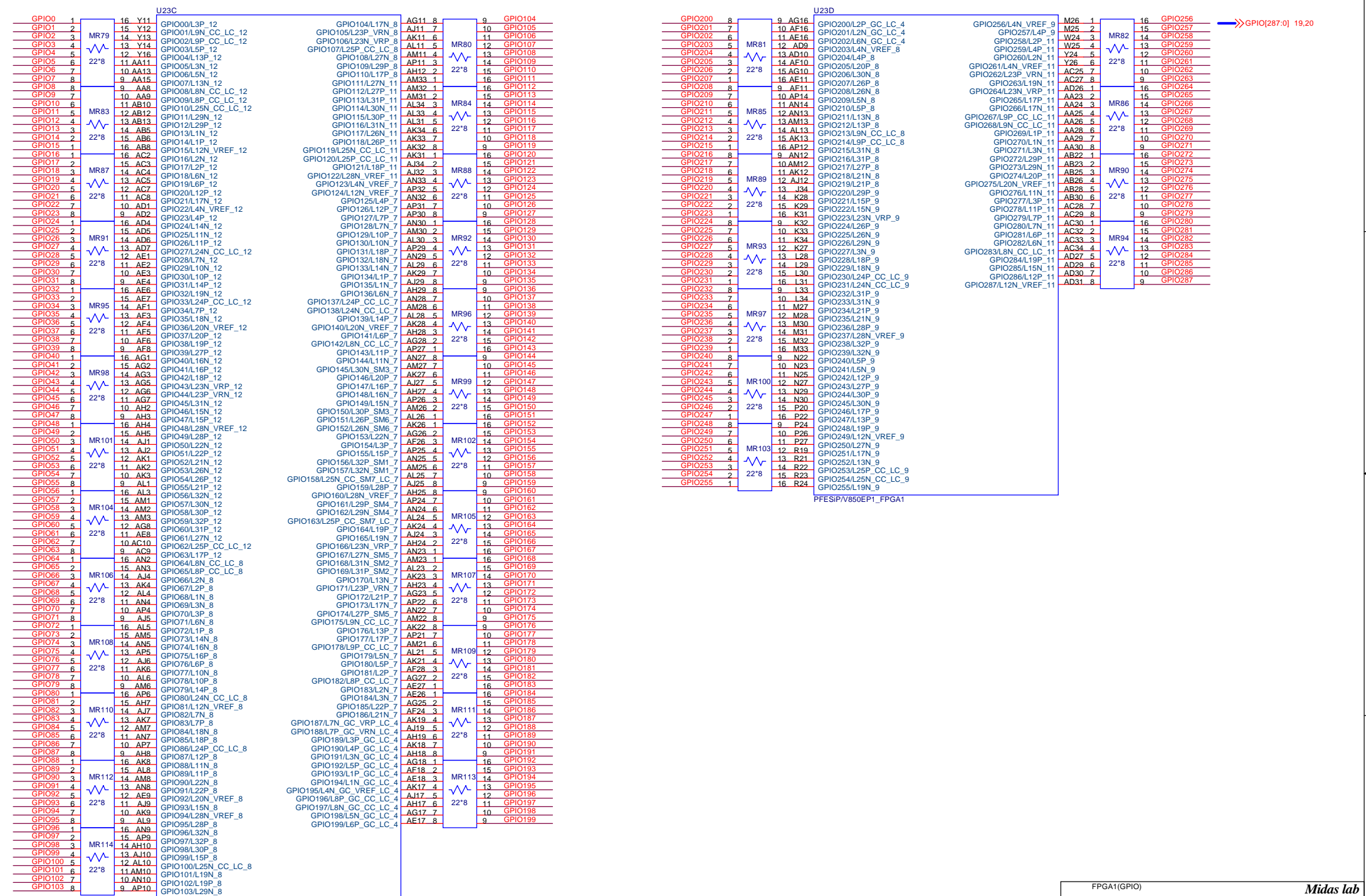


PLD01		Midas lab
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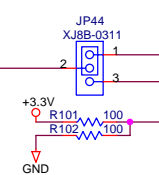
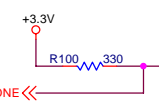
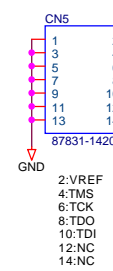
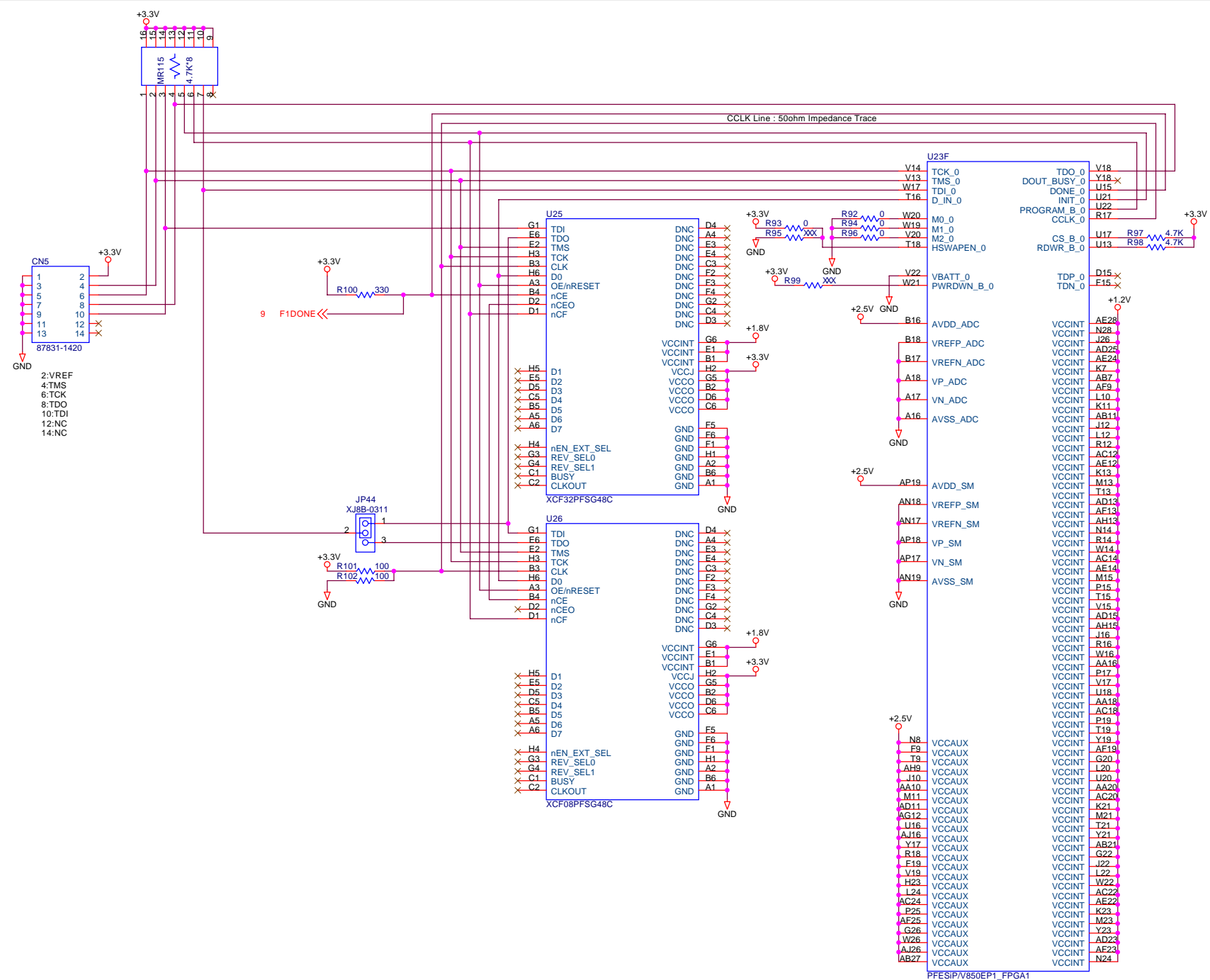




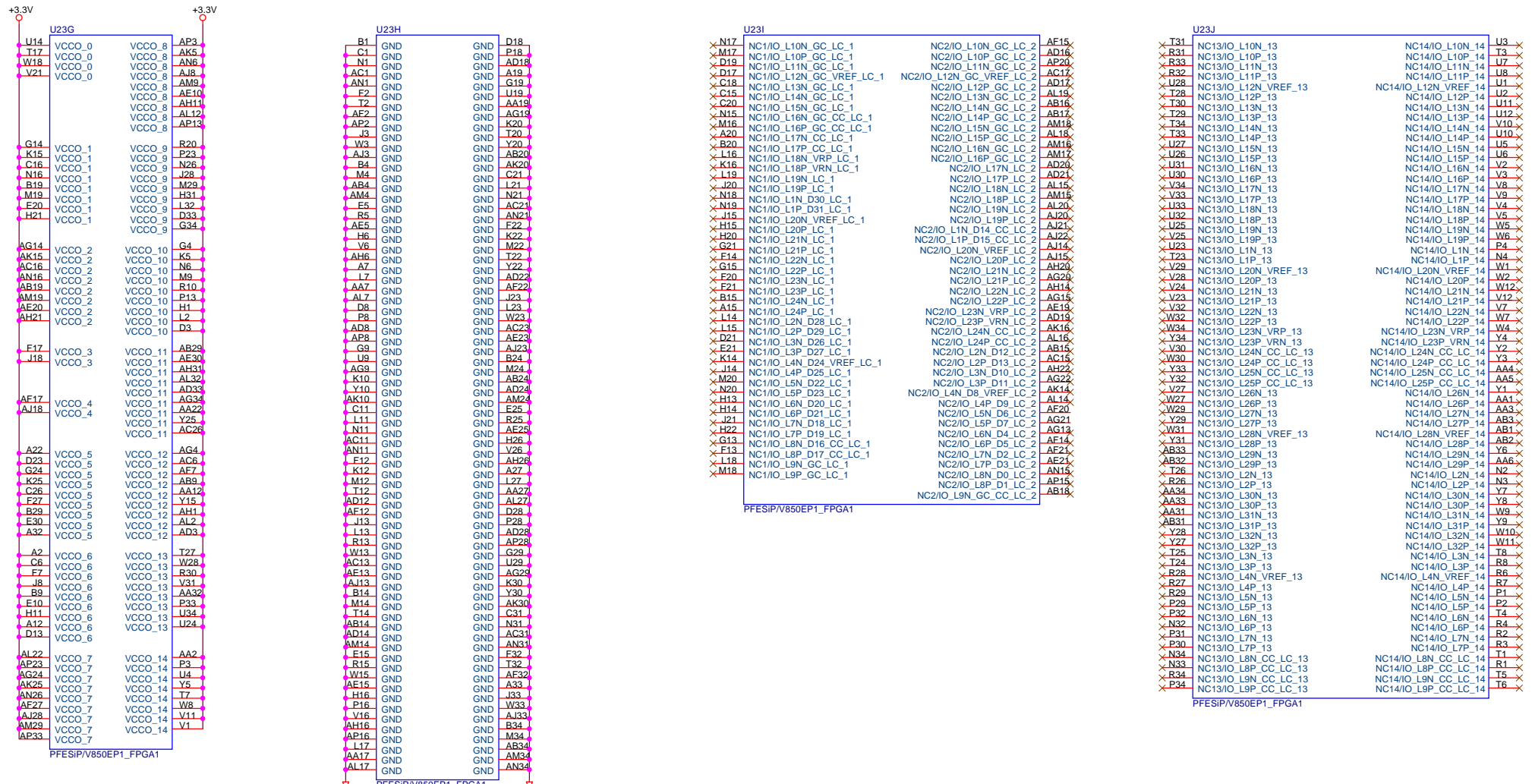
FPGA1(MEM I/F, MISC)		Midas lab
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FPGA1(GPIO)		Midas lab	
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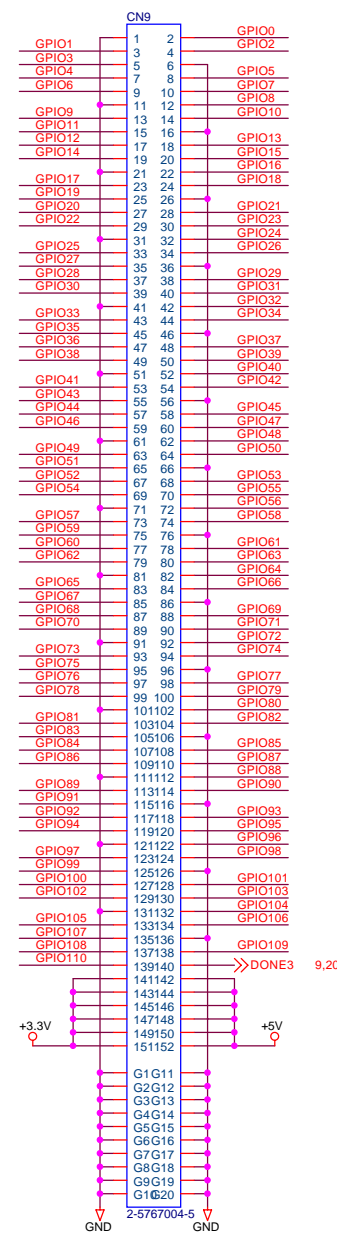
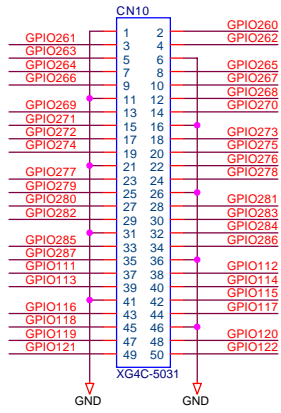
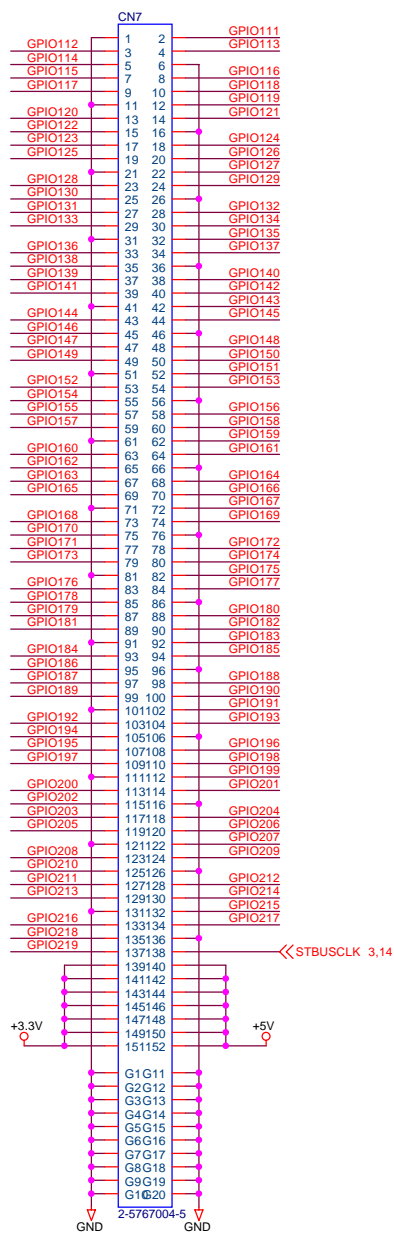
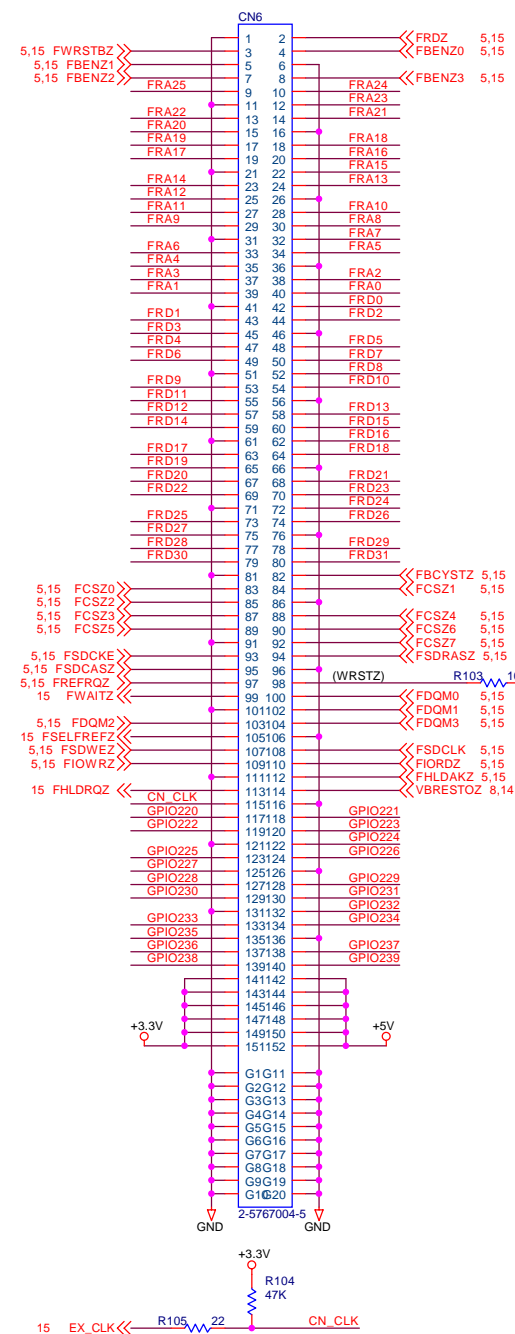
FPGA1(Configuration)		Midas lab
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FPGA1(P)			Midas lab		
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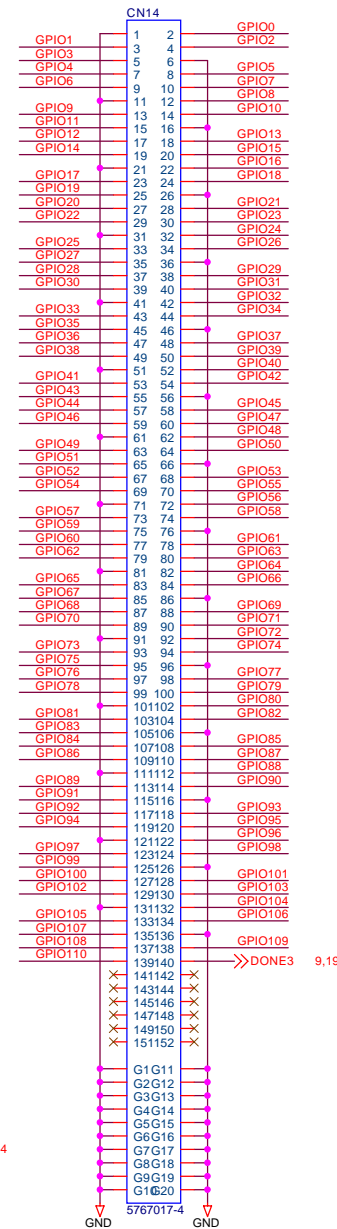
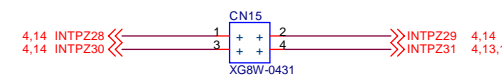
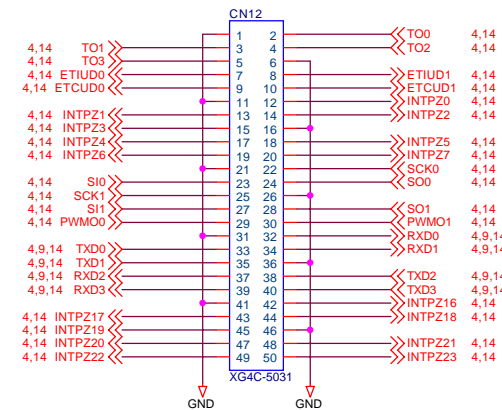
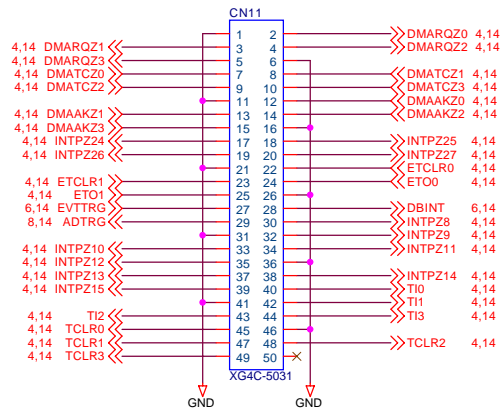
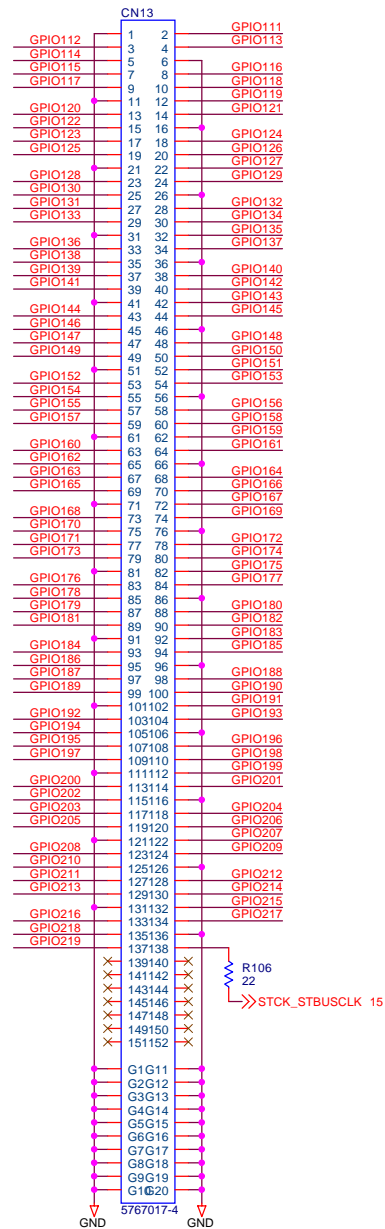
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5,15 FRA[25:0] >>>

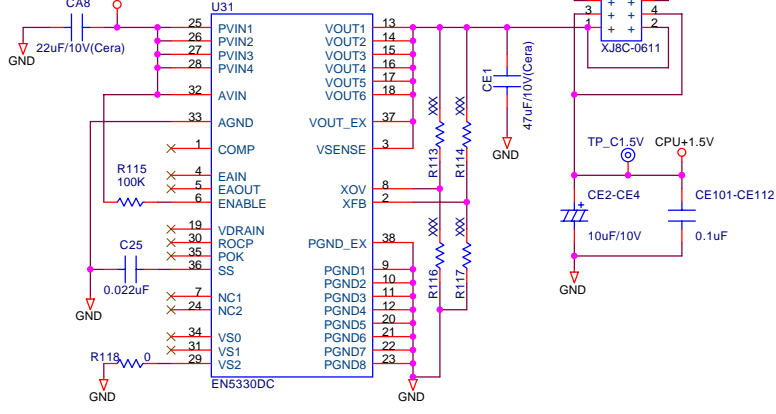
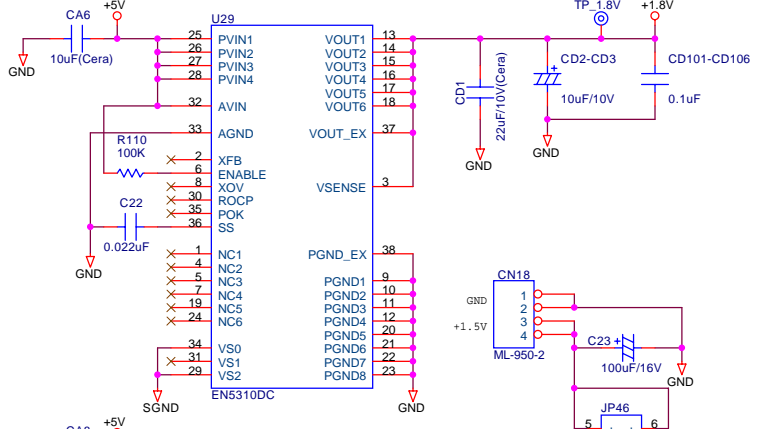
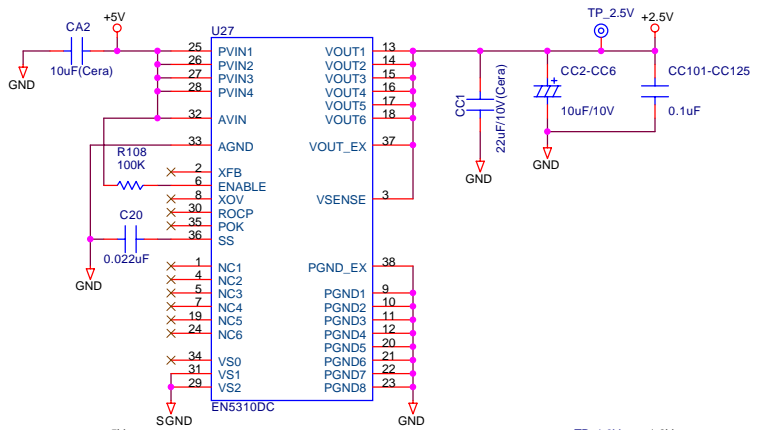
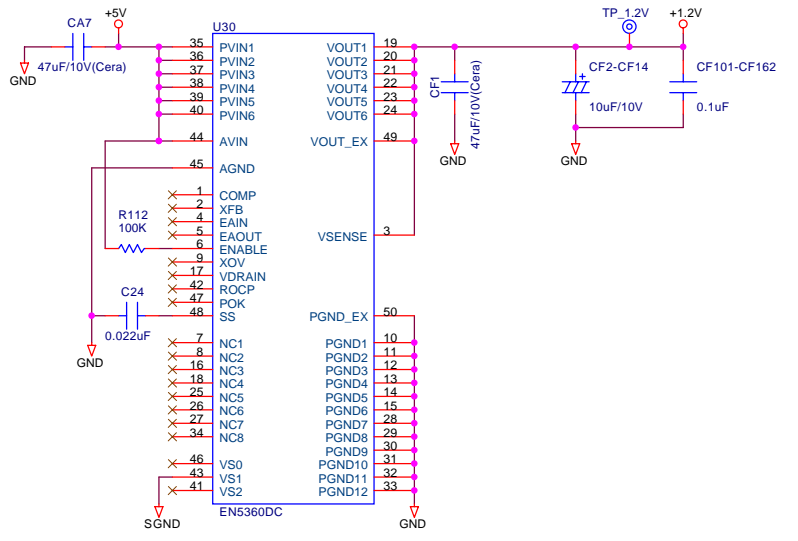
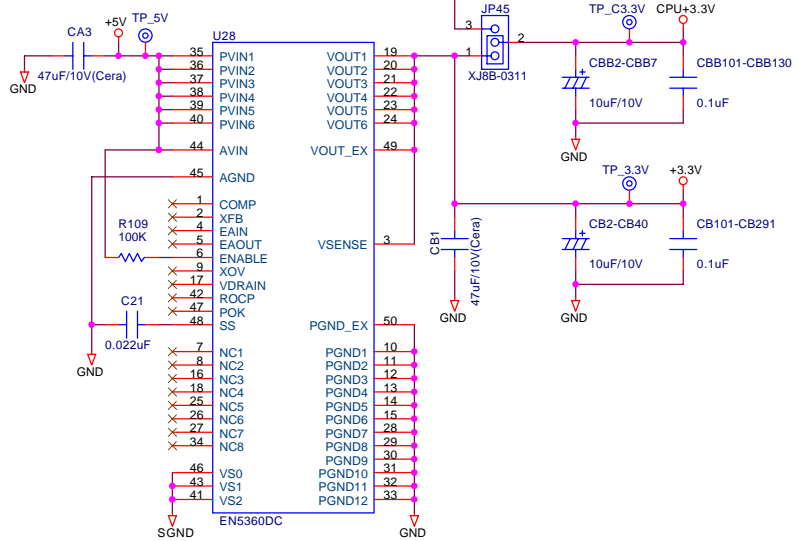
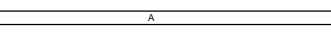
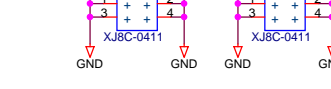
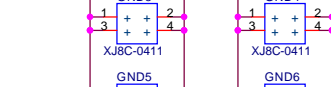
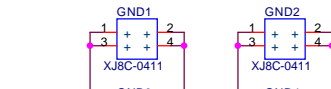
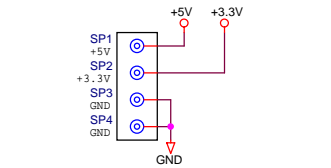
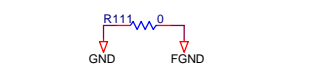
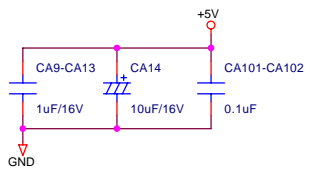
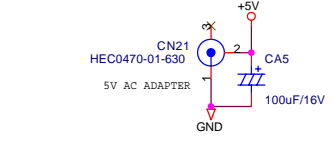
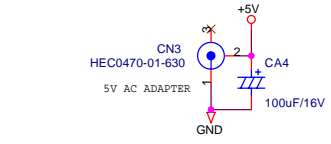
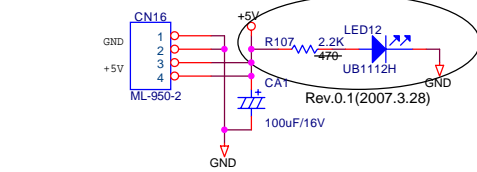


GPIO CONN1(Mictor152,DIP50)		Midas lab	
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16,19 GPIO[287:0]



GPIO CONN2(Mictor152,DIP50)		Midas lab	
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